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ФАКУЛЬТЕТ «Информатика и системы управления»
КАФЕДРА «Программное обеспечение ЭВМ и информационные технологии»

Отчёт

по лабораторной работе №4

Название «Разработка RTL ядра ускорителя вычислений на платформе Xilinx Alveo»

Дисциплина «Архитектура ЭВМ»

Вариант 3

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Введение

Целью данной лабораторной работы является изучение архитектуры гетерогенных вычислительных систем и технологии разработки ускорителей вычислений на базе ПЛИС фирмы Xilinx.

Для достижения данной цели необходимо выполнить следующие **задачи**:

- 1) Изучить основные сведения о платформе Xilinx Alveo U200.
- 2) Разработать RTL описание ускорителя вычислений по индивидуальному варианту.
- 3) Выполнить генерацию ядра ускорителя.
- 4) Выполнить синтез и сборку бинарного модуля ускорителя.
- 5) Разработать и отладить тестирующее ПО на серверной хост-платформе.
- 6) Провести тесты работы ускорителя вычислений.

1 Функциональная схема разрабатываемой аппаратной системы

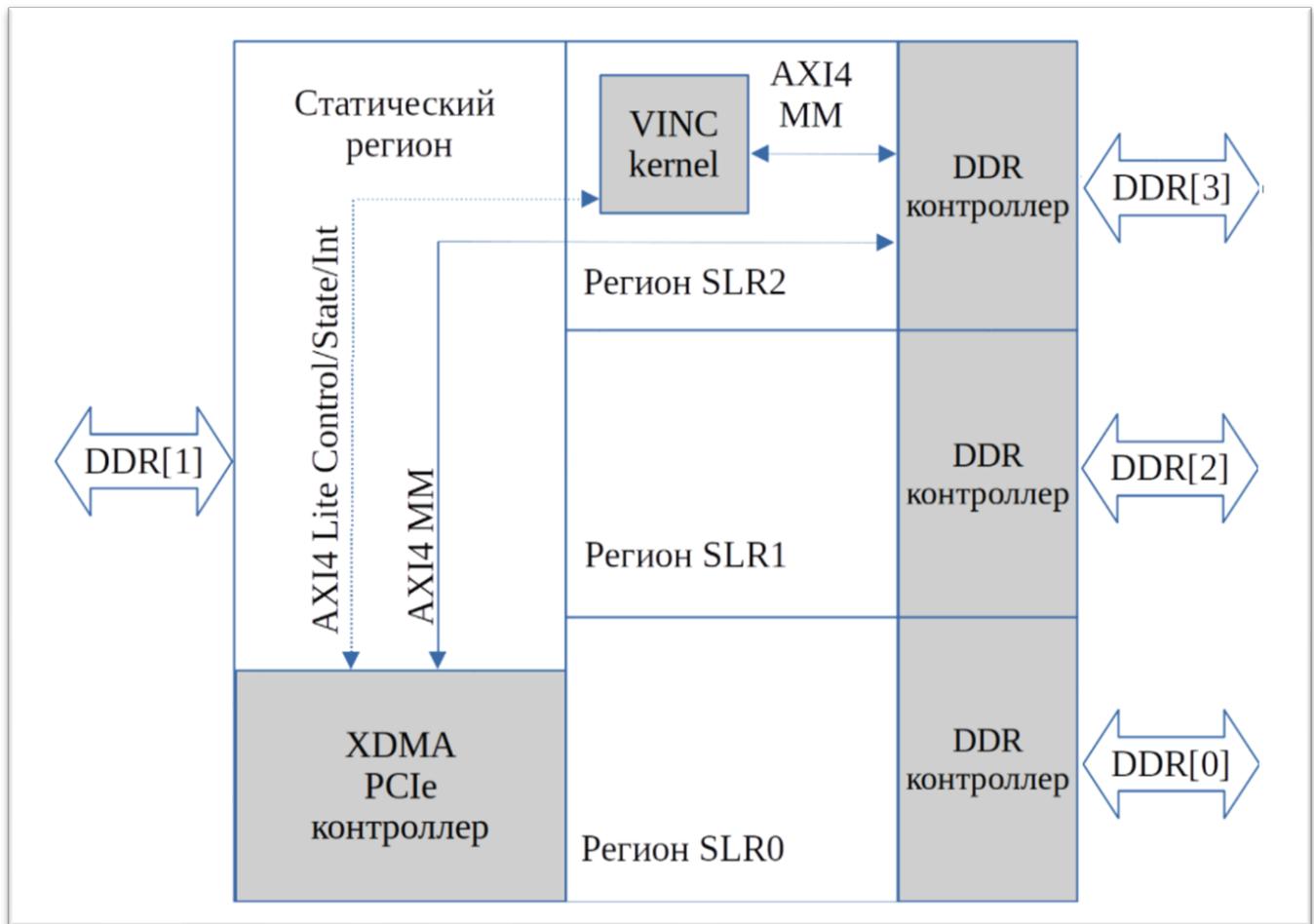


Рисунок 1.1 — Схема аппаратной системы

2 Моделирование исходного проекта VINC

В данном разделе приведены диаграммы, иллюстрирующие процесс рукопожатия и пакетного чтения.

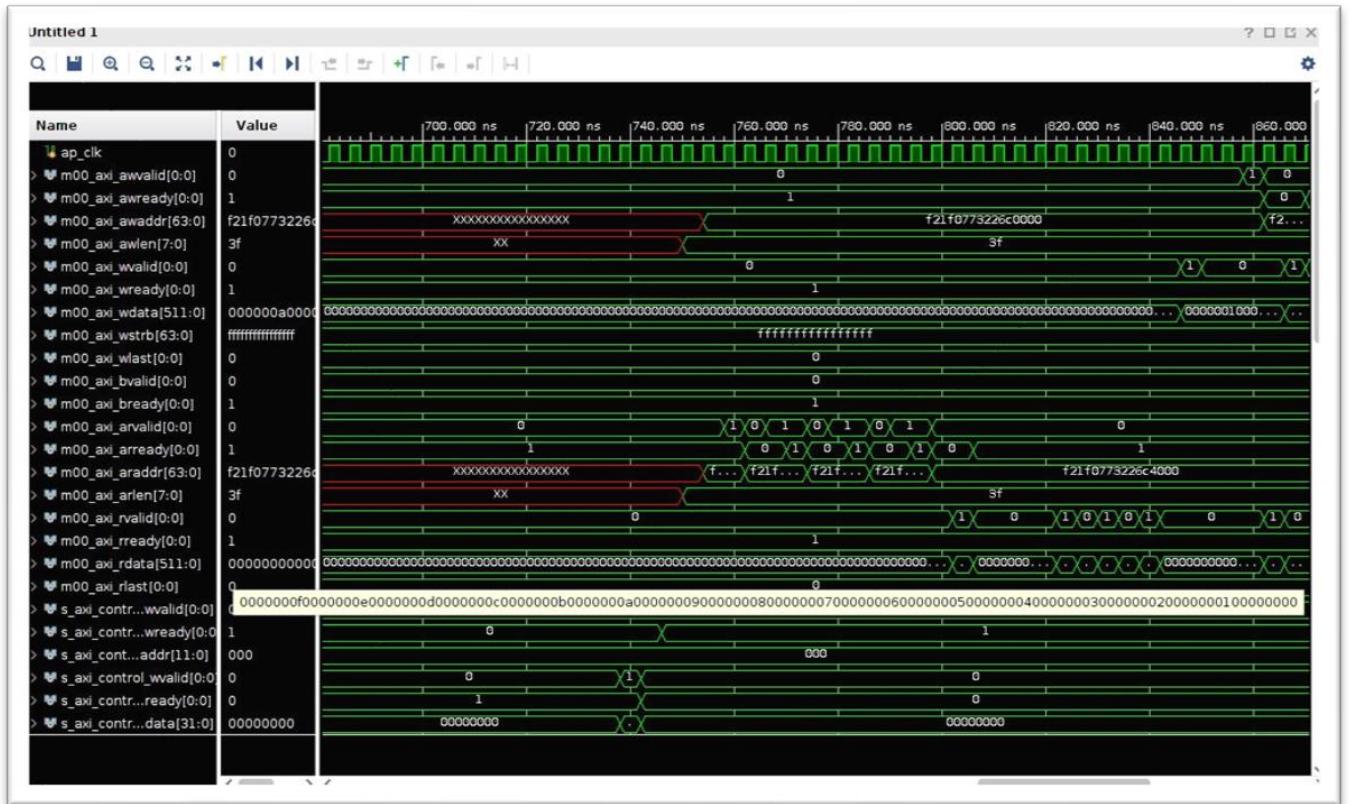


Рисунок 2.1 — Транзакция чтения данных вектора на шине AXI4 MM из DDR памяти

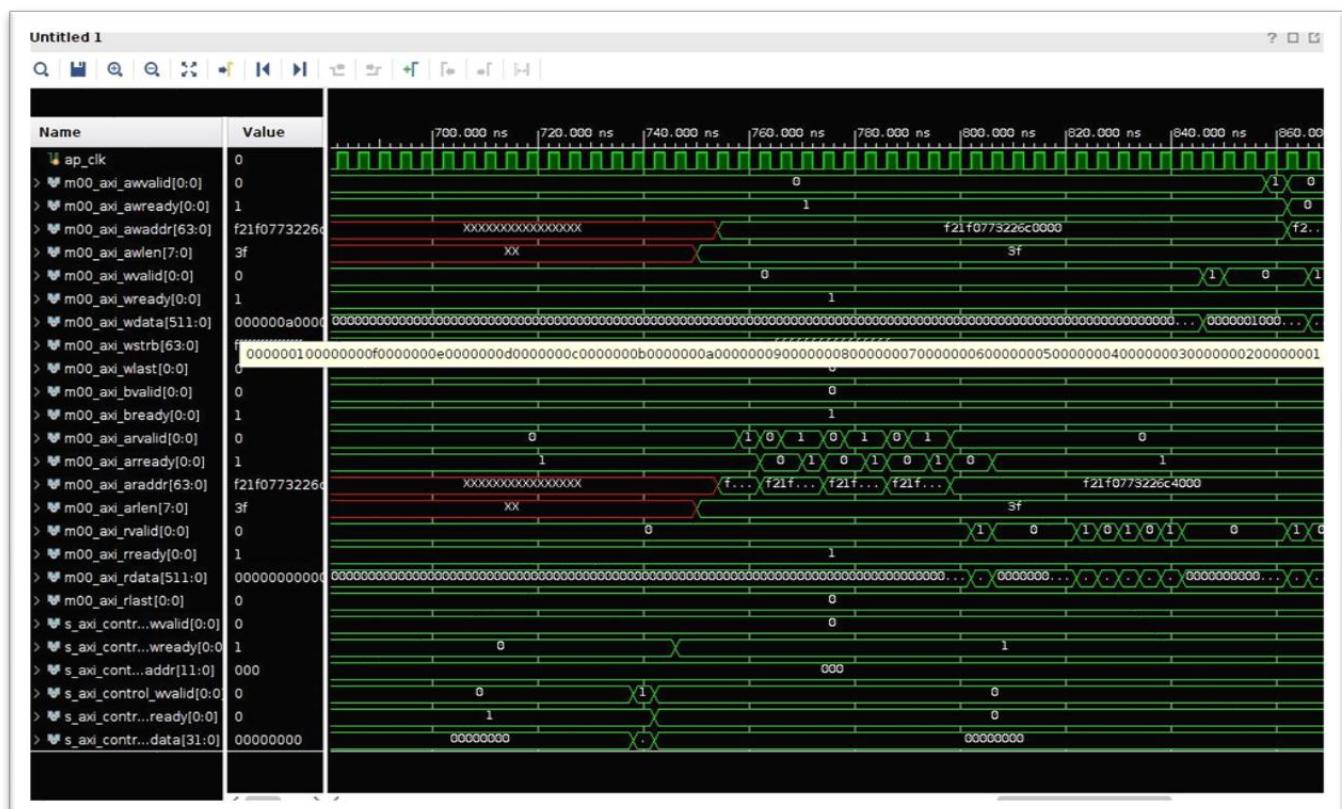


Рисунок 2.2 — Транзакция записи результата инкремента данных на шине AXI4-MM

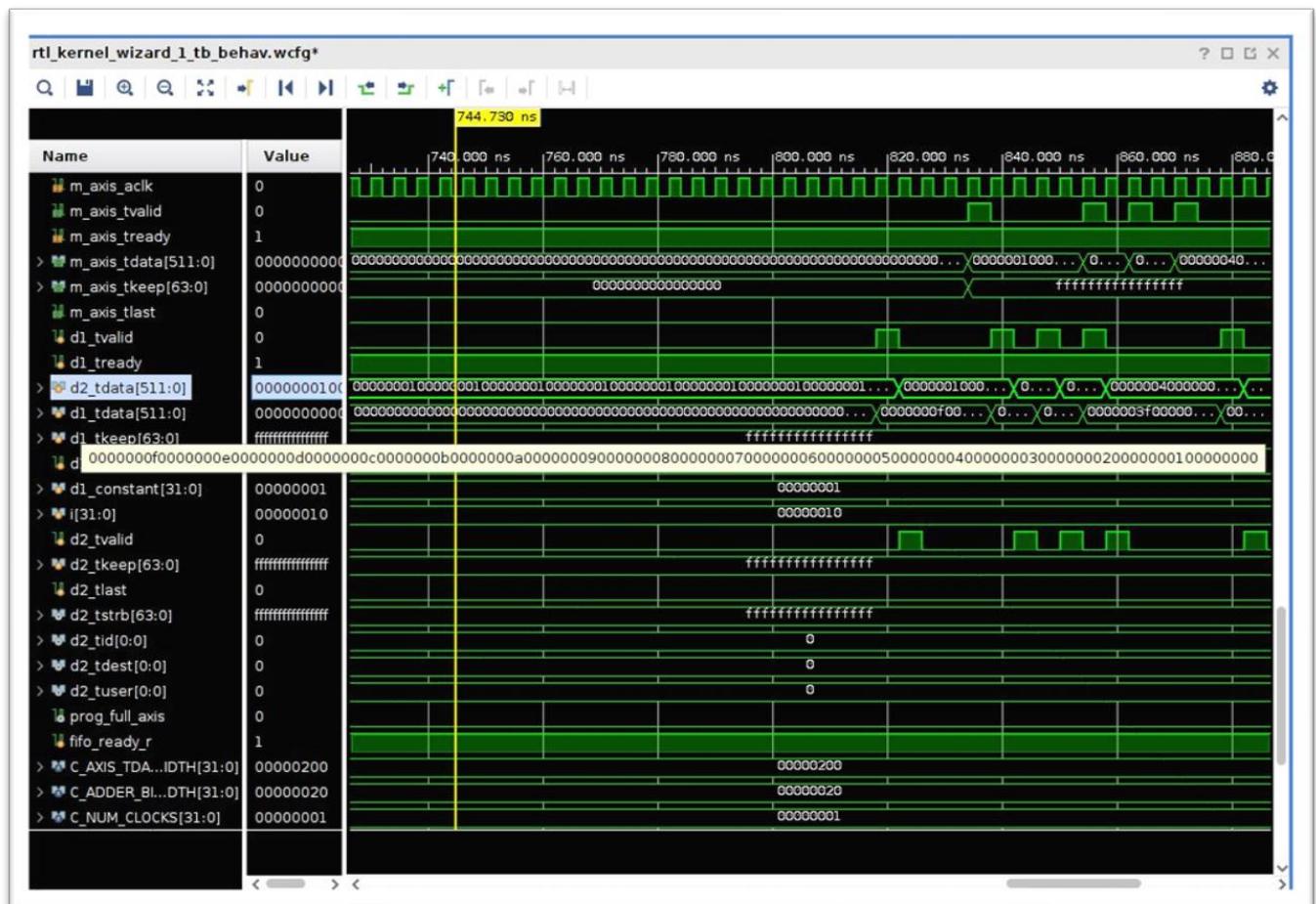


Рисунок 2.3 — Инкремент данных

3 Моделирование измененного проекта VINC

Изменим модуль `rtl_kernel_wizard_2_example_adder.v`, чтобы ускоритель выполнял предложенную функцию:

$$R[i] = (A[i] - 1) * 4 \quad (3.1)$$

Ниже представлен фрагмент листинга кода.

Листинг 3.1 — Листинг изменённой функции

```
1 always @ (posedge s_axis_aclk) begin
2   for (i = 0; i < LP_NUM_LOOPS; i = i + 1) begin
3     d2_tdata[i*C_ADDER_BIT_WIDTH+:C_ADDER_BIT_WIDTH] <=
4       (d1_tdata[C_ADDER_BIT_WIDTH*i+:C_ADDER_BIT_WIDTH] - 1) * 4;
5   end

```

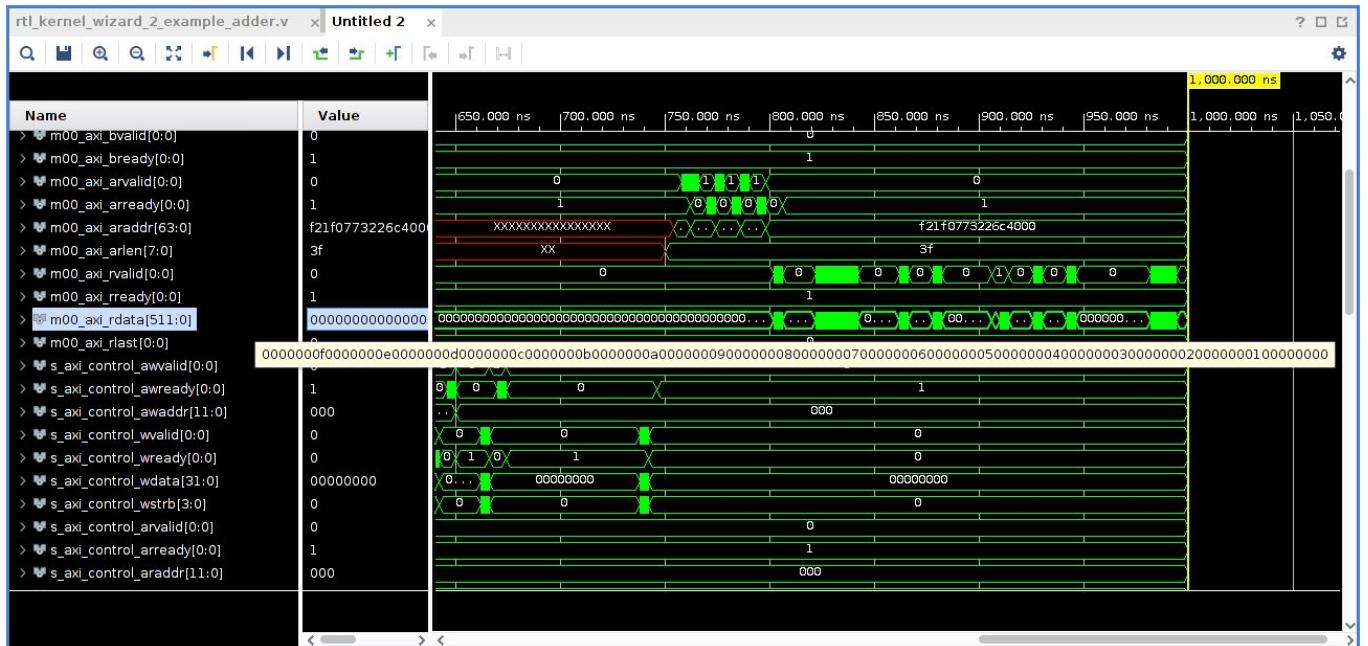


Рисунок 3.1 — Транзакция чтения

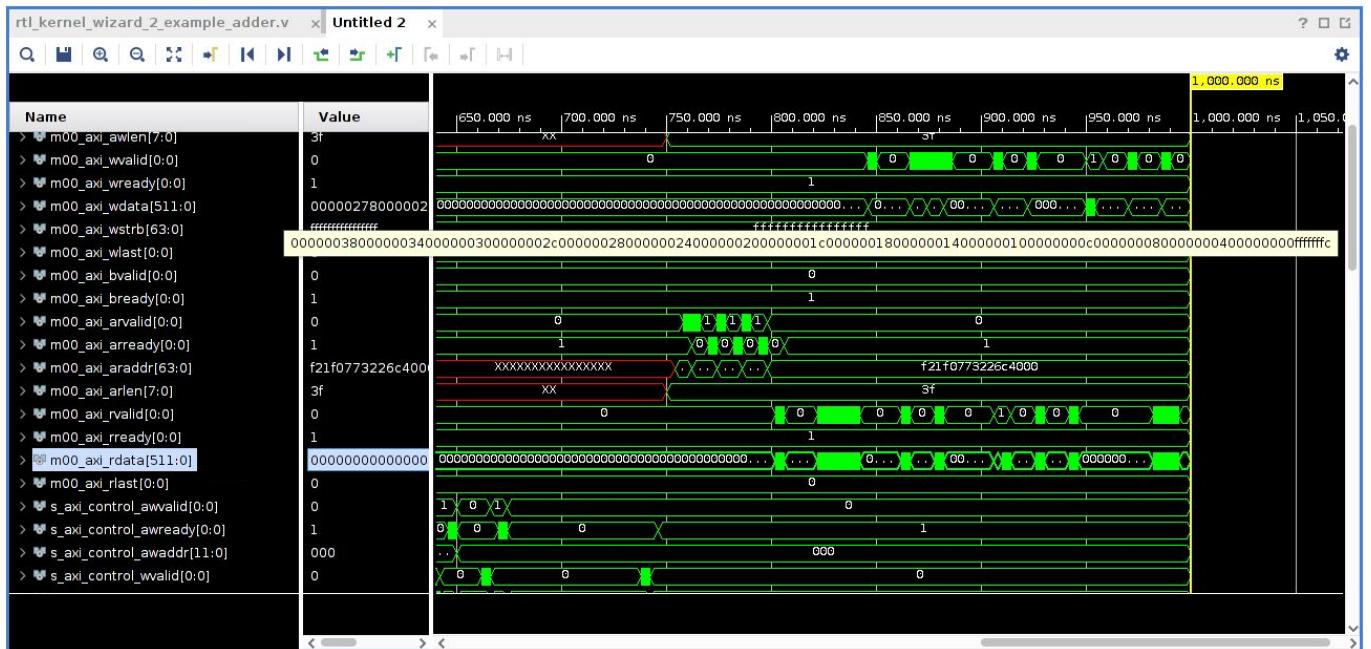


Рисунок 3.2 — Транзакция записи

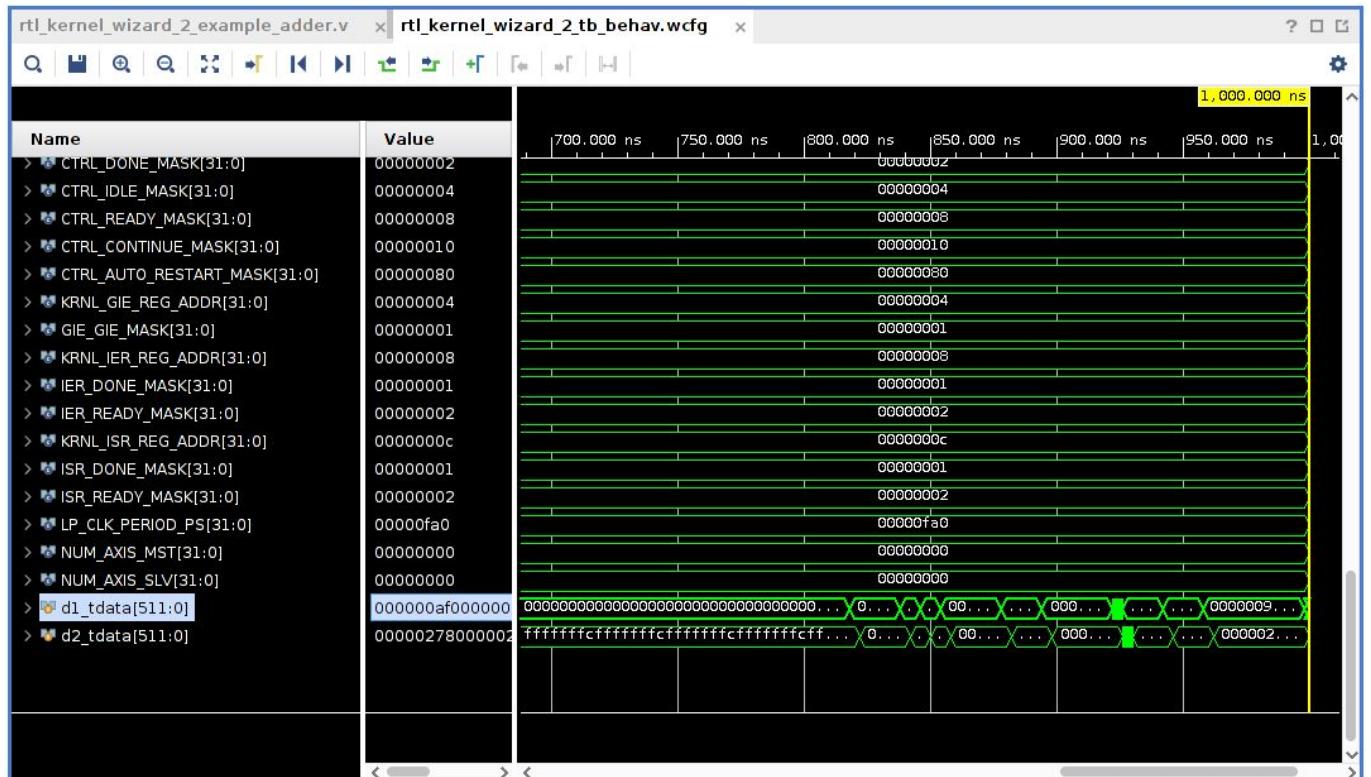


Рисунок 3.3 — Изменение данных в модуле

3.1 Конфигурационный файл линковки

```
[connectivity]
nk=rtl_kernel_wizard_2:1:vinc0
slr=vinc0:SLR1
sp=vinc0.m00_axi:DDR[2]

[vivado]
prop=run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore
prop=run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore
prop=run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true
prop=run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore
prop=run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore
```

3.2 Содержимое файла xclbin.info

```
Build Date: 2020-11-16 00:19:11
Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9
=====
xclbin Information
-----
Generated by: v++ (2020.2) on 2020-11-18-05:13:29
Version: 2.8.743
Kernels: rtl_kernel_wizard_2
Signature:
Content: Bitstream
UUID (xclbin): fab9772d-552c-4009-9fa0-8e2dc8ad29e4
Sections: DEBUG_IP_LAYOUT, BITSTREAM, MEM_TOPOLOGY,
IP_LAYOUT, CONNECTIVITY, CLOCK_FREQ_TOPOLOGY, BUILD_METADATA,
EMBEDDED_METADATA, SYSTEM_METADATA,
GROUP_CONNECTIVITY, GROUP_TOPOLOGY
=====
Hardware Platform (Shell) Information
-----
Vendor: xilinx
Board: u200
Name: xdma
Version: 201830.2
Generated Version: Vivado 2018.3 (SW Build: 2568420)
Created: Tue Jun 25 06:55:20 2019
FPGA Device: xcu200
Board Vendor: xilinx.com
Board Name: xilinx.com:au200:1.0
Board Part: xilinx.com:au200:part0:1.0
Platform VBNV: xilinx_u200_xdma_201830_2
Static UUID: c102e7af-b2b8-4381-992b-9a00cc3863eb
```

Feature ROM TimeStamp: 1561465320

Clocks

Name: DATA_CLK

Index: 0

Type: DATA

Frequency: 300 MHz

Name: KERNEL_CLK

Index: 1

Type: KERNEL

Frequency: 500 MHz

Memory Configuration

Name: bank0

Index: 0

Type: MEM_DDR4

Base Address: 0x4000000000

Address Size: 0x4000000000

Bank Used: No

Name: bank1

Index: 1

Type: MEM_DDR4

Base Address: 0x5000000000

Address Size: 0x4000000000

Bank Used: No

Name: bank2

Index: 2

Type: MEM_DDR4

Base Address: 0x6000000000

Address Size: 0x4000000000

Bank Used: Yes

Name: bank3

Index: 3

Type: MEM_DDR4

Base Address: 0x7000000000

Address Size: 0x4000000000

Bank Used: No

Name: PLRAM[0]

Index: 4

Type: MEM_DRAM
Base Address: 0x30000000000
Address Size: 0x20000
Bank Used: No

Name: PLRAM[1]
Index: 5
Type: MEM_DRAM
Base Address: 0x3000200000
Address Size: 0x20000
Bank Used: No

Name: PLRAM[2]
Index: 6
Type: MEM_DRAM
Base Address: 0x3000400000
Address Size: 0x20000
Bank Used: No

=====

Kernel: rtl_kernel_wizard_2

Definition

Signature: rtl_kernel_wizard_2 (uint inp_param, int* axi00_ptr0)

Ports

Port: s_axi_control
Mode: slave
Range (bytes): 0x1000
Data Width: 32 bits
Port Type: addressable

Port: m00_axi
Mode: master
Range (bytes): 0xFFFFFFFFFFFFFFF
Data Width: 512 bits
Port Type: addressable

Instance: vinc0
Base Address: 0x1800000

Argument: inp_param
Register Offset: 0x010
Port: s_axi_control

Memory: <not applicable>

Argument: axi00_ptr0

Register Offset: 0x018

Port: m00_axi

Memory: bank2 (MEM_DDR4)

=====

Generated By

Command: v++

Version: 2020.2 - 2020-11-18-05:13:29 (SW BUILD: 0)

Command Line: v++ --config ./Alveo_lab1.cfg --connectivity.nk

rtl_kernel_wizard_2:1:vinc0 --connectivity.slr vinc0:SLR1

--connectivity.sp vinc0.m00_axi:DDR[2] --input_files

./rtl_kernel_wizard_2.xo --link --optimize 0 --output vinc.xclbin

--platform xilinx_u200_xdma_201830_2 --report_level 0 --target hw

--vivado.prop run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore

--vivado.prop run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore

--vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true

--vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore --vivado.prop
run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore

Options: --config ./Alveo_lab1.cfg

--connectivity.nk rtl_kernel_wizard_2:1:vinc0

--connectivity.slr vinc0:SLR1

--connectivity.sp vinc0.m00_axi:DDR[2]

--input_files ./rtl_kernel_wizard_2.xo

--link

--optimize 0

--output vinc.xclbin

--platform xilinx_u200_xdma_201830_2

--report_level 0

--target hw

--vivado.prop run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore

--vivado.prop run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore

--vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true

--vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore

--vivado.prop run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore

=====

User Added Key Value Pairs

<empty>

=====

3.3 Содержимое файла vinc.log

INFO: [v++ 60-1306] Additional information associated with this v++ link can be found at:

Reports:

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/re

Log files:

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lo

INFO: [v++ 60-1548] Creating build summary session with primary output

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/vinc.r

at Mon Oct 11 23:09:22 2021

INFO: [v++ 60-1316] Initiating connection to rulecheck server, at Mon Oct 11 23:09:24 2021

INFO: [v++ 60-1315] Creating rulecheck session with output

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/re

at Mon Oct 11 23:09:43 2021

INFO: [v++ 60-895] Target platform:

/opt/xilinx/platforms/xilinx_u200_xdma_201830_2/xilinx_u200_xdma_201830_2.xpfm

INFO: [v++ 60-1578] This platform contains Device Support Archive

'/opt/xilinx/platforms/xilinx_u200_xdma_201830_2/hw/xilinx_u200_xdma_201830_2.dsa'

INFO: [v++ 74-74] Compiler Version string: 2020.2

INFO: [v++ 60-1302] Platform 'xilinx_u200_xdma_201830_2.xpfm' has been explicitly enabled for this release.

INFO: [v++ 60-629] Linking for hardware target

INFO: [v++ 60-423] Target device: xilinx_u200_xdma_201830_2

INFO: [v++ 60-1332] Run 'run_link' status: Not started

INFO: [v++ 60-1443] [23:10:50] Run run_link: Step system_link: Started

INFO: [v++ 60-1453] Command Line: system_link --xo

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/rtl_k

--config

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin

--xpfm /opt/xilinx/platforms/xilinx_u200_xdma_201830_2/xilinx_u200_xdma_201830_2.xpfm

--target hw --output_dir

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin

--temp_dir

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin

INFO: [v++ 60-1454] Run Directory:

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin

INFO: [SYSTEM_LINK 60-1316] Initiating connection to rulecheck server, at Mon Oct 11 23:11:08

2021

INFO: [SYSTEM_LINK 82-70] Extracting xo v3 file

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/rtl_k

INFO: [SYSTEM_LINK 82-53] Creating IP database

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin

INFO: [SYSTEM_LINK 82-38] [23:11:14] build_xd_ip_db started:

/data/Xilinx/Vitis/2020.2/bin/build_xd_ip_db -ip_search 0 -sds-pf

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin

-clkid 0 -ip

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin

-o

/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin

```

INFO: [SYSTEM_LINK 82-37] [23:11:57] build_xd_ip_db finished successfully
Time (s): cpu = 00:00:35 ; elapsed = 00:00:43 . Memory (MB): peak = 1557.895 ; gain = 0.000 ;
    free physical = 57836 ; free virtual = 295751
INFO: [SYSTEM_LINK 82-51] Create system connectivity graph
INFO: [SYSTEM_LINK 82-102] Applying explicit connections to the system connectivity graph:
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
INFO: [SYSTEM_LINK 82-38] [23:11:57] cfgen started: /data/Xilinx/Vitis/2020.2/bin/cfgen -nk
    rtl_kernel_wizard_2:1:vinc0 -slr vinc0:SLR1 -sp vinc0.m00_axi:DDR[2] -dmclkid 0 -r
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    -o
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
INFO: [CFGGEN 83-0] Kernel Specs:
INFO: [CFGGEN 83-0]   kernel: rtl_kernel_wizard_2, num: 1 {vinc0}
INFO: [CFGGEN 83-0] Port Specs:
INFO: [CFGGEN 83-0]   kernel: vinc0, k_port: m00_axi, sptag: DDR[2]
INFO: [CFGGEN 83-0] SLR Specs:
INFO: [CFGGEN 83-0]   instance: vinc0, SLR: SLR1
INFO: [CFGGEN 83-2228] Creating mapping for argument vinc0.axi00_ptr0 to DDR[2] for directive
    vinc0.m00_axi:DDR[2]
INFO: [SYSTEM_LINK 82-37] [23:12:31] cfgen finished successfully
Time (s): cpu = 00:00:33 ; elapsed = 00:00:34 . Memory (MB): peak = 1557.895 ; gain = 0.000 ;
    free physical = 57870 ; free virtual = 295785
INFO: [SYSTEM_LINK 82-52] Create top-level block diagram
INFO: [SYSTEM_LINK 82-38] [23:12:31] cf2bd started: /data/Xilinx/Vitis/2020.2/bin(cf2bd --linux
    --trace_buffer 1024 --input_file
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    --ip_db
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    --cf_name dr --working_dir
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    --temp_dir
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    --output_dir
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    --target_bd pfm_dynamic.bd
INFO: [CF2BD 82-31] Launching cf2xd: cf2xd -linux -trace-buffer 1024 -i
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    -r
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    -o dr.xml
INFO: [CF2BD 82-28] cf2xd finished successfully
INFO: [CF2BD 82-31] Launching cf_xsds: cf_xsds -disable-address-gen -bd pfm_dynamic.bd -dn dr -dp
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
INFO: [CF2BD 82-28] cf_xsds finished successfully
INFO: [SYSTEM_LINK 82-37] [23:12:51] cf2bd finished successfully

```

```

Time (s): cpu = 00:00:15 ; elapsed = 00:00:19 . Memory (MB): peak = 1557.895 ; gain = 0.000 ;
    free physical = 57841 ; free virtual = 295761
INFO: [v++ 60-1441] [23:12:51] Run run_link: Step system_link: Completed
Time (s): cpu = 00:01:46 ; elapsed = 00:02:02 . Memory (MB): peak = 1721.133 ; gain = 0.000 ;
    free physical = 57920 ; free virtual = 295835
INFO: [v++ 60-1443] [23:12:51] Run run_link: Step cf2sw: Started
INFO: [v++ 60-1453] Command Line: cf2sw -sdsl
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    -rtd
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    -nofilter
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    -xclbin
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    -o
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
INFO: [v++ 60-1454] Run Directory:
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
INFO: [v++ 60-1441] [23:13:14] Run run_link: Step cf2sw: Completed
Time (s): cpu = 00:00:19 ; elapsed = 00:00:22 . Memory (MB): peak = 1721.133 ; gain = 0.000 ;
    free physical = 58006 ; free virtual = 295921
INFO: [v++ 60-1443] [23:13:14] Run run_link: Step rtd2_system_diagram: Started
INFO: [v++ 60-1453] Command Line: rtd2SystemDiagram
INFO: [v++ 60-1454] Run Directory:
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
INFO: [v++ 60-1441] [23:13:26] Run run_link: Step rtd2_system_diagram: Completed
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:13 . Memory (MB): peak = 1721.133 ; gain = 0.000 ;
    free physical = 57220 ; free virtual = 295135
INFO: [v++ 60-1443] [23:13:26] Run run_link: Step vpl: Started
INFO: [v++ 60-1453] Command Line: vpl -t hw -f xilinx_u200_xdma_201830_2 --remote_ip_cache
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/.ipca
    --output_dir
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    --log_dir
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    --report_dir
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/rep
    --config
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    -k
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    --webtalk_flag Vitis --temp_dir
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    --no_info --iprepo
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
    --messageDb

```

```
/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lis
/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lis
INFO: [v++ 60-1454] Run Directory:
/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lis

***** vpl v2020.2 (64-bit)
**** SW Build (by xbuild) on 2020-11-18-05:13:29
** Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.

INFO: [VPL 60-839] Read in kernel information from file
'/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lis
INFO: [VPL 74-74] Compiler Version string: 2020.2
INFO: [VPL 60-423] Target device: xilinx_u200_xdma_201830_2
INFO: [VPL 60-1032] Extracting hardware platform to
/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lis
WARNING: /data/Xilinx/Vitis/2020.2/tps/lnx64/jre9.0.4 does not exist.
[23:21:34] Run vpl: Step create_project: RUNNING...
[23:21:24] Run vpl: Step create_project: Started
Creating Vivado project.
[23:22:03] Run vpl: Step create_project: Completed
[23:22:03] Run vpl: Step create_bd: Started
[23:24:20] Run vpl: Step create_bd: RUNNING...
[23:29:37] Run vpl: Step create_bd: RUNNING...
[23:31:34] Run vpl: Step create_bd: RUNNING...
[23:33:35] Run vpl: Step create_bd: RUNNING...
[23:35:19] Run vpl: Step create_bd: RUNNING...
[23:37:12] Run vpl: Step create_bd: RUNNING...
[23:38:59] Run vpl: Step create_bd: RUNNING...
[23:39:15] Run vpl: Step create_bd: Completed
[23:39:15] Run vpl: Step update_bd: Started
[23:39:20] Run vpl: Step update_bd: Completed
[23:39:20] Run vpl: Step generate_target: Started
[23:42:09] Run vpl: Step generate_target: RUNNING...
[23:44:02] Run vpl: Step generate_target: RUNNING...
[23:45:27] Run vpl: Step generate_target: RUNNING...
[23:47:17] Run vpl: Step generate_target: RUNNING...
[23:48:53] Run vpl: Step generate_target: RUNNING...
[23:50:38] Run vpl: Step generate_target: RUNNING...
[23:52:22] Run vpl: Step generate_target: RUNNING...
[23:54:10] Run vpl: Step generate_target: Completed
[23:54:10] Run vpl: Step config_hw_runs: Started
[23:54:15] Run vpl: Step generate_target: RUNNING...
[23:56:20] Run vpl: Step config_hw_runs: RUNNING...
[23:56:31] Run vpl: Step config_hw_runs: Completed
[23:56:31] Run vpl: Step synth: Started
[23:59:27] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.
```


[00:32:40] Block-level synthesis in progress, 19 of 66 jobs complete, 7 jobs running.
[00:33:48] Block-level synthesis in progress, 19 of 66 jobs complete, 8 jobs running.
[00:34:28] Block-level synthesis in progress, 21 of 66 jobs complete, 6 jobs running.
[00:35:10] Block-level synthesis in progress, 21 of 66 jobs complete, 6 jobs running.
[00:35:53] Block-level synthesis in progress, 21 of 66 jobs complete, 8 jobs running.
[00:36:32] Block-level synthesis in progress, 22 of 66 jobs complete, 7 jobs running.
[00:37:22] Block-level synthesis in progress, 22 of 66 jobs complete, 7 jobs running.
[00:38:01] Block-level synthesis in progress, 22 of 66 jobs complete, 8 jobs running.
[00:38:41] Block-level synthesis in progress, 22 of 66 jobs complete, 8 jobs running.
[00:39:33] Block-level synthesis in progress, 22 of 66 jobs complete, 8 jobs running.
[00:40:15] Block-level synthesis in progress, 22 of 66 jobs complete, 8 jobs running.
[00:41:18] Block-level synthesis in progress, 23 of 66 jobs complete, 7 jobs running.
[00:42:31] Block-level synthesis in progress, 23 of 66 jobs complete, 8 jobs running.
[00:43:11] Block-level synthesis in progress, 25 of 66 jobs complete, 6 jobs running.
[00:43:57] Block-level synthesis in progress, 25 of 66 jobs complete, 6 jobs running.
[00:44:38] Block-level synthesis in progress, 25 of 66 jobs complete, 8 jobs running.
[00:45:23] Block-level synthesis in progress, 26 of 66 jobs complete, 7 jobs running.
[00:46:04] Block-level synthesis in progress, 27 of 66 jobs complete, 6 jobs running.
[00:46:50] Block-level synthesis in progress, 27 of 66 jobs complete, 6 jobs running.
[00:47:37] Block-level synthesis in progress, 28 of 66 jobs complete, 7 jobs running.
[00:48:25] Block-level synthesis in progress, 30 of 66 jobs complete, 5 jobs running.
[00:49:01] Block-level synthesis in progress, 30 of 66 jobs complete, 5 jobs running.
[00:49:52] Block-level synthesis in progress, 30 of 66 jobs complete, 8 jobs running.
[00:50:33] Block-level synthesis in progress, 31 of 66 jobs complete, 7 jobs running.
[00:51:23] Block-level synthesis in progress, 31 of 66 jobs complete, 7 jobs running.
[00:52:00] Block-level synthesis in progress, 31 of 66 jobs complete, 8 jobs running.
[00:52:38] Block-level synthesis in progress, 32 of 66 jobs complete, 7 jobs running.
[00:53:16] Block-level synthesis in progress, 33 of 66 jobs complete, 6 jobs running.
[00:53:54] Block-level synthesis in progress, 33 of 66 jobs complete, 7 jobs running.
[00:54:31] Block-level synthesis in progress, 34 of 66 jobs complete, 6 jobs running.
[00:55:14] Block-level synthesis in progress, 34 of 66 jobs complete, 7 jobs running.
[00:55:53] Block-level synthesis in progress, 35 of 66 jobs complete, 7 jobs running.
[00:56:38] Block-level synthesis in progress, 35 of 66 jobs complete, 7 jobs running.
[00:57:21] Block-level synthesis in progress, 35 of 66 jobs complete, 7 jobs running.
[00:58:11] Block-level synthesis in progress, 35 of 66 jobs complete, 8 jobs running.
[00:58:49] Block-level synthesis in progress, 35 of 66 jobs complete, 8 jobs running.
[00:59:31] Block-level synthesis in progress, 37 of 66 jobs complete, 6 jobs running.
[01:00:15] Block-level synthesis in progress, 38 of 66 jobs complete, 5 jobs running.
[01:00:56] Block-level synthesis in progress, 38 of 66 jobs complete, 7 jobs running.
[01:01:33] Block-level synthesis in progress, 38 of 66 jobs complete, 7 jobs running.
[01:02:18] Block-level synthesis in progress, 39 of 66 jobs complete, 7 jobs running.
[01:02:55] Block-level synthesis in progress, 40 of 66 jobs complete, 6 jobs running.
[01:03:38] Block-level synthesis in progress, 41 of 66 jobs complete, 5 jobs running.
[01:04:16] Block-level synthesis in progress, 41 of 66 jobs complete, 7 jobs running.
[01:05:02] Block-level synthesis in progress, 42 of 66 jobs complete, 6 jobs running.
[01:05:39] Block-level synthesis in progress, 42 of 66 jobs complete, 7 jobs running.


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[01:38:40] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:39:30] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:40:10] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:40:49] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:41:28] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:42:15] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:42:55] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:43:42] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:44:22] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:45:07] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:45:46] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:46:35] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:47:16] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:48:05] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.
[01:48:44] Block-level synthesis in progress, 66 of 66 jobs complete, 0 jobs running.
[01:49:31] Block-level synthesis in progress, 66 of 66 jobs complete, 0 jobs running.
[01:50:12] Top-level synthesis in progress.
[01:50:51] Top-level synthesis in progress.
[01:51:30] Top-level synthesis in progress.
[01:52:21] Top-level synthesis in progress.
[01:53:01] Top-level synthesis in progress.
[01:53:53] Top-level synthesis in progress.
[01:54:32] Top-level synthesis in progress.
[01:55:17] Top-level synthesis in progress.
[01:55:55] Top-level synthesis in progress.
[01:56:33] Top-level synthesis in progress.
[01:57:12] Top-level synthesis in progress.
[01:57:59] Top-level synthesis in progress.
[01:58:40] Top-level synthesis in progress.
[01:59:25] Top-level synthesis in progress.
[02:00:06] Top-level synthesis in progress.
[02:00:53] Top-level synthesis in progress.
[02:01:33] Top-level synthesis in progress.
[02:02:14] Top-level synthesis in progress.
[02:03:04] Top-level synthesis in progress.
[02:03:49] Top-level synthesis in progress.
[02:04:35] Run vpl: Step synth: Completed
[02:04:35] Run vpl: Step impl: Started
[03:23:21] Finished 2nd of 6 tasks (FPGA linking synthesized kernels to platform). Elapsed time:
          04h 09m 41s

[03:23:21] Starting logic optimization..
[03:32:43] Phase 1 Generate And Synthesize MIG Cores
[04:25:06] Phase 2 Generate And Synthesize Debug Cores
[04:59:11] Phase 3 Retarget
[05:02:07] Phase 4 Constant propagation
```

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[05:04:13] Phase 5 Sweep
[05:11:52] Phase 6 BUFG optimization
[05:14:03] Phase 7 Shift Register Optimization
[05:15:19] Phase 8 Post Processing Netlist
[05:34:41] Finished 3rd of 6 tasks (FPGA logic optimization). Elapsed time: 02h 11m 20s

[05:34:41] Starting logic placement..
[05:40:11] Phase 1 Placer Initialization
[05:40:11] Phase 1.1 Placer Initialization Netlist Sorting
[05:59:00] Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
[06:11:45] Phase 1.3 Build Placer Netlist Model
[06:30:12] Phase 1.4 Constrain Clocks/Macros
[06:31:38] Phase 2 Global Placement
[06:31:38] Phase 2.1 Floorplanning
[06:35:55] Phase 2.1.1 Partition Driven Placement
[06:36:41] Phase 2.1.1.1 PBP: Partition Driven Placement
[06:38:39] Phase 2.1.1.2 PBP: Clock Region Placement
[06:44:59] Phase 2.1.1.3 PBP: Compute Congestion
[06:45:38] Phase 2.1.1.4 PBP: UpdateTiming
[06:48:26] Phase 2.1.1.5 PBP: Add part constraints
[06:49:13] Phase 2.2 Update Timing before SLR Path Opt
[06:50:37] Phase 2.3 Global Placement Core
[07:32:36] Phase 2.3.1 Physical Synthesis In Placer
[07:49:48] Phase 3 Detail Placement
[07:49:48] Phase 3.1 Commit Multi Column Macros
[07:50:31] Phase 3.2 Commit Most Macros & LUTRAMs
[07:57:37] Phase 3.3 Small Shape DP
[07:57:37] Phase 3.3.1 Small Shape Clustering
[08:01:20] Phase 3.3.2 Flow Legalize Slice Clusters
[08:02:00] Phase 3.3.3 Slice Area Swap
[08:09:56] Phase 3.4 Place Remaining
[08:10:37] Phase 3.5 Re-assign LUT pins
[08:12:50] Phase 3.6 Pipeline Register Optimization
[08:12:50] Phase 3.7 Fast Optimization
[08:18:23] Phase 4 Post Placement Optimization and Clean-Up
[08:18:23] Phase 4.1 Post Commit Optimization
[08:31:06] Phase 4.1.1 Post Placement Optimization
[08:31:46] Phase 4.1.1.1 BUFG Insertion
[08:31:46] Phase 1 Physical Synthesis Initialization
[08:35:22] Phase 4.1.1.2 BUFG Replication
[08:40:15] Phase 4.1.1.3 Replication
[08:48:59] Phase 4.2 Post Placement Cleanup
[08:50:16] Phase 4.3 Placer Reporting
[08:50:16] Phase 4.3.1 Print Estimated Congestion
[08:52:22] Phase 4.4 Final Placement Cleanup
[10:22:46] Finished 4th of 6 tasks (FPGA logic placement). Elapsed time: 04h 48m 04s
```

```

[10:22:46] Starting logic routing..
[10:30:51] Phase 1 Build RT Design
[10:44:33] Phase 2 Router Initialization
[10:44:33] Phase 2.1 Fix Topology Constraints
[10:45:16] Phase 2.2 Pre Route Cleanup
[10:45:57] Phase 2.3 Global Clock Net Routing
[10:49:40] Phase 2.4 Update Timing
[11:07:11] Phase 2.5 Update Timing for Bus Skew
[11:07:11] Phase 2.5.1 Update Timing
[11:13:42] Phase 3 Initial Routing
[11:13:42] Phase 3.1 Global Routing
[11:20:59] Phase 4 Rip-up And Reroute
[11:20:59] Phase 4.1 Global Iteration 0
[11:53:17] Phase 4.2 Global Iteration 1
[11:59:48] Phase 4.3 Global Iteration 2
[12:07:19] Phase 5 Delay and Skew Optimization
[12:07:19] Phase 5.1 Delay CleanUp
[12:07:19] Phase 5.1.1 Update Timing
[12:16:28] Phase 5.2 Clock Skew Optimization
[12:17:07] Phase 6 Post Hold Fix
[12:17:07] Phase 6.1 Hold Fix Iter
[12:17:56] Phase 6.1.1 Update Timing
[12:24:37] Phase 7 Route finalize
[12:25:21] Phase 8 Verifying routed nets
[12:26:43] Phase 9 Depositing Routes
[12:32:42] Phase 10 Route finalize
[12:33:24] Phase 11 Post Router Timing
[12:42:16] Finished 5th of 6 tasks (FPGA routing). Elapsed time: 02h 19m 30s

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[12:42:16] Starting bitstream generation..
[15:19:30] Creating bitmap...
[16:22:03] Writing bitstream ./pfm_top_i_dynamic_region_my_rm_partial.bit...
[16:22:46] Finished 6th of 6 tasks (FPGA bitstream generation). Elapsed time: 03h 40m 29s
[16:28:52] Run vpl: Step impl: Completed
[16:29:03] Run vpl: FINISHED. Run Status: impl Complete!
INFO: [v++ 60-1441] [16:29:55] Run run_link: Step vpl: Completed
Time (s): cpu = 01:29:58 ; elapsed = 17:16:28 . Memory (MB): peak = 1721.133 ; gain = 0.000 ;
          free physical = 73455 ; free virtual = 311619
INFO: [v++ 60-1443] [16:29:55] Run run_link: Step rtdgen: Started
INFO: [v++ 60-1453] Command Line: rtdgen
INFO: [v++ 60-1454] Run Directory:
      /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_xilinx
INFO: [v++ 60-991] clock name 'clkwiz_kernel_clk_out1' (clock ID '0') is being mapped to clock
      name 'DATA_CLK' in the xclbin

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INFO: [v++ 60-991] clock name 'clkwiz_kernel2_clk_out1' (clock ID '1') is being mapped to clock
      name 'KERNEL_CLK' in the xclbin
INFO: [v++ 60-1230] The compiler selected the following frequencies for the runtime controllable
      kernel clock(s) and scalable system clock(s): Kernel (DATA) clock: clkwiz_kernel_clk_out1 =
      300, Kernel (KERNEL) clock: clkwiz_kernel2_clk_out1 = 500
INFO: [v++ 60-1453] Command Line: cf2sw -a
      /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
      -sds1
      /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
      -xclbin
      /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
      -rtd
      /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
      -o
      /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
INFO: [v++ 60-1652] Cf2sw returned exit code: 0
INFO: [v++ 60-2311] HPISystemDiagram::writeSystemDiagramAfterRunningVivado, rtdInputFilePath:
      /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
INFO: [v++ 60-2312] HPISystemDiagram::writeSystemDiagramAfterRunningVivado,
      systemDiagramOutputFilePath:
      /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
INFO: [v++ 60-1618] Launching
INFO: [v++ 60-1441] [16:30:15] Run run_link: Step rtdgen: Completed
Time (s): cpu = 00:00:19 ; elapsed = 00:00:20 . Memory (MB): peak = 1721.133 ; gain = 0.000 ;
      free physical = 73424 ; free virtual = 311588
INFO: [v++ 60-1443] [16:30:15] Run run_link: Step xclbinutil: Started
INFO: [v++ 60-1453] Command Line: xclbinutil --add-section
      DEBUG_IP_LAYOUT:JSON:/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
      --add-section
      BITSTREAM:RAW:/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
      --force --target hw --key-value SYS:dfx_enable:true --add-section
      :JSON:/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
      --append-section
      :JSON:/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
      --add-section
      CLOCK_FREQ_TOPOLOGY:JSON:/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
      --add-section
      BUILD_METADATA:JSON:/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
      --add-section
      EMBEDDED_METADATA:RAW:/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
      --add-section
      SYSTEM_METADATA:RAW:/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin
      --output
      /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/vinc
INFO: [v++ 60-1454] Run Directory:
      /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/lin

```

```
XRT Build Version: 2.8.743 (2020.2)
Build Date: 2020-11-16 00:19:11
Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9
Creating a default 'in-memory' xclbin image.

Section: 'DEBUG_IP_LAYOUT'(9) was successfully added.
Size    : 440 bytes
Format   : JSON
File    :
'/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/1

Section: 'BITSTREAM'(0) was successfully added.
Size    : 40651402 bytes
Format   : RAW
File    :
'/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/1

Section: 'MEM_TOPOLOGY'(6) was successfully added.
Format   : JSON
File    : 'mem_topology'

Section: 'IP_LAYOUT'(8) was successfully added.
Format   : JSON
File    : 'ip_layout'

Section: 'CONNECTIVITY'(7) was successfully added.
Format   : JSON
File    : 'connectivity'

Section: 'CLOCK_FREQ_TOPOLOGY'(11) was successfully added.
Size    : 274 bytes
Format   : JSON
File    :
'/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/1

Section: 'BUILD_METADATA'(14) was successfully added.
Size    : 2903 bytes
Format   : JSON
File    :
'/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/1

Section: 'EMBEDDED_METADATA'(2) was successfully added.
Size    : 2760 bytes
Format   : RAW
File    :
'/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/1
```

```

Section: 'SYSTEM_METADATA'(22) was successfully added.
Size    : 5622 bytes
Format   : RAW
File    :
  '/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/1

Section: 'IP_LAYOUT'(8) was successfully appended to.
Format : JSON
File   : 'ip_layout'
Successfully wrote (40673304 bytes) to the output file:
  /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/vinc.xclbin
Leaving xclbinutil.

INFO: [v++ 60-1441] [16:30:19] Run run_link: Step xclbinutil: Completed
Time (s): cpu = 00:00:00.69 ; elapsed = 00:00:04 . Memory (MB): peak = 1721.133 ; gain = 0.000 ;
          free physical = 73317 ; free virtual = 311597
INFO: [v++ 60-1443] [16:30:19] Run run_link: Step xclbinutilinfo: Started
INFO: [v++ 60-1453] Command Line: xclbinutil --quiet --force --info
  /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/vinc.xclbin
  --input
  /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/vinc.xclbin
INFO: [v++ 60-1454] Run Directory:
  /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/1
INFO: [v++ 60-1441] [16:30:24] Run run_link: Step xclbinutilinfo: Completed
Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak = 1721.133 ; gain = 0.000 ;
          free physical = 73359 ; free virtual = 311640
INFO: [v++ 60-1443] [16:30:24] Run run_link: Step generate_sc_driver: Started
INFO: [v++ 60-1453] Command Line:
INFO: [v++ 60-1454] Run Directory:
  /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/1
INFO: [v++ 60-1441] [16:30:24] Run run_link: Step generate_sc_driver: Completed
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.06 . Memory (MB): peak = 1721.133 ; gain =
          0.000 ; free physical = 73317 ; free virtual = 311598
INFO: [v++ 60-244] Generating system estimate report...
INFO: [v++ 60-1092] Generated system estimate report:
  /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/rep
INFO: [v++ 60-586] Created
  /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/vinc.xclbin
INFO: [v++ 60-586] Created vinc.xclbin
INFO: [v++ 60-1307] Run completed. Additional information can be found in:
  Guidance:
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/rep
  Timing Report:
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/rep
  Vivado Log:
    /iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/rep

```

Steps Log File:

```
/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/_x/log
```

INFO: [v++ 60-2343] Use the vitis_analyzer tool to visualize and navigate the relevant reports.

Run the following command.

vitis_analyzer

```
/iu_home/iu7123/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/exports/vinc...
```

INFO: [v++ 60-791] Total elapsed time: 17h 21m 35s

INFO: [v++ 60-1653] Closing dispatch client.

4 Тестирование

4.1 Модификация модуля host_example.cpp

Изменим содержимое файла host_example.cpp таким образом, чтобы выполнялось корректное тестирование функции, предложенной в варианте.

Листинг 4.1 — Измененный код проверки результата

```
1 // Check Results
2 for (cl_uint i = 0; i < number_of_words; i++) {
3     printf("i=%d, input=%d, output=%d\n", i, h_axi00_ptr0_input[i], h_axi00_ptr0_output[i]);
4     if ((h_data[i] - 1) * 4 != h_axi00_ptr0_output[i]) {
5         printf("ERROR in rtl_kernel_wizard_2::m00_axi - array index %d (host addr 0x%03x) -
6             input=%d (0x%x), output=%d (0x%x)\n", i, i*4, h_data[i], h_data[i],
7             h_axi00_ptr0_output[i], h_axi00_ptr0_output[i]);
8         check_status = 1;
9     }
10 }
```

4.2 Результаты тестирования

Результаты тестирования приведёны ниже.

```
i=0, input=-4, output=-4
i=1, input=0, output=0
i=2, input=4, output=4
i=3, input=8, output=8
i=4, input=12, output=12
...
i=4091, input=16360, output=16360
i=4092, input=16364, output=16364
i=4093, input=16368, output=16368
i=4094, input=16372, output=16372
i=4095, input=16376, output=16376
INFO: Test completed successfully.
```

Заключение

В ходе лабораторной работы были изучены архитектура гетерогенных вычислительных систем и технологии разработки ускорителей вычислений на базе ПЛИС фирмы Xilinx. Была выполнена генерация ядра ускорителя с последующим синтезом, сборкой и тестированием бинарного модуля ускорителя.