One-Dimensional Logic Gate Assignment and Interval Graphs

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Abstract—**This paper gives a graph-theoretic approach to the design of one-dimensional logic gate arrays using MOS or I^2L units. The incidence relation between gates and nets is represented by a graph $H=(V,E)$, and a possible layout of gates and nets is characterized by an interval graph $\hat{H}=(V,E\cup F)$, where F is called an *augmentation*. It is shown that the number of tracks required for between-gate wiring is equal to the clique number (chromatic number) of $\hat{H}$, and hence the optimum placement problem is converted to that of *minimum clique number augmentation*. This turns out to be an NP-complete problem. Instead a polynomial-time algorithm for finding a minimal augmentation is presented, where an augmentation is *minimal* if no proper subset of it is an augmentation. An algorithm for gate sequencing with respect to a given augmentation is also presented.**

I. Introduction

RECENT advances in microelectronics have brought renewed interests in layout design, a field which has so far depended primarily on manual effort and experiences of design engineers. There exist very few fundamental results and theoretical methods. One main difficulty seems to lie in obtaining analytic characterizations of problems which are practically meaningful. The problem of linear placement is a notable exception. The problem is to determine the optimum positions of modules which lie in a single row. It is important in the design of one-dimensional logic gate arrays using MOS or I^2L units, and the main purpose is to minimize the chip areas [1]–[3]. Recently, linear placement has also been found useful in solving the general placement problem [4]. Although there exist various algorithms for obtaining suboptimum linear placement, most depend on heuristics and the method of branch and bound [5], [6]. In this paper we introduce a new formulation of the problem using graph theory. It converts the practical problem of finding a minimum-track placement into that of generating an optimum interval graph with minimum chromatic number. Both theoretical results and efficient computational algorithms are obtained.

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In Section II, we give the problem formulation with a brief sketch of the elementary properties of interval graphs. In Section III, we present a method of obtaining a proper gate sequence and a track assignment. In Section IV, a method is presented to find a minimal augmentation which plays a key role in our approach. Examples and comments next follow.

II. Problem Formulation

In Fig. 1, a NAND gate is shown together with its circuit schematic and layout schematic. A complex logic function can be realized with gates interconnected as a one-dimensional array. In the detailed layout, in-gate wiring is done along the vertical columns and between-gates connections are made horizontally. At the intersection of vertical gates and horizontal wires, there is either a terminal of a transistor as A, C, D, and P or a straight connector as B shown in Fig. 1(c). Also, the width of each gate and the separation distance between two neighboring gates are predetermined according to physical constraints. Therefore, the total horizontal dimension of an array is considered fixed. The vertical spacing determines the total chip area and is to be minimized. This can be achieved by finding an optimum sequence of the gates. For example, an optimum realization of logic array is shown in Fig. 2. Each gate is represented by a vertical line. Horizontal wires are assigned to tracks.

The gate sequencing problem is a linear placement problem. In general, there are given a set of modules, numbered as $1,2,\cdots,m$ and a set of nets, numbered as $1,2,\cdots,n$ together with a net list which specifies the connection pattern. A net corresponds to a horizontal wire which interconnects modules assigned to the net. Thus a placement may be considered to be a permutation $\pi=(\pi_1,\pi_2,\cdots,\pi_m)$ of the first m integers such that module π_i is placed in the ith position on a row. The most commonly used objective function for minimization is the total wire length. However, in the gate sequencing problem, as we have discussed, a different criterion must be used. We want to minimize the necessary number of tracks.

Before going further we introduce a few definitions related to interval graphs. A graph $G=(V,E)$ is an *interval graph* if there exists a set of finite closed intervals

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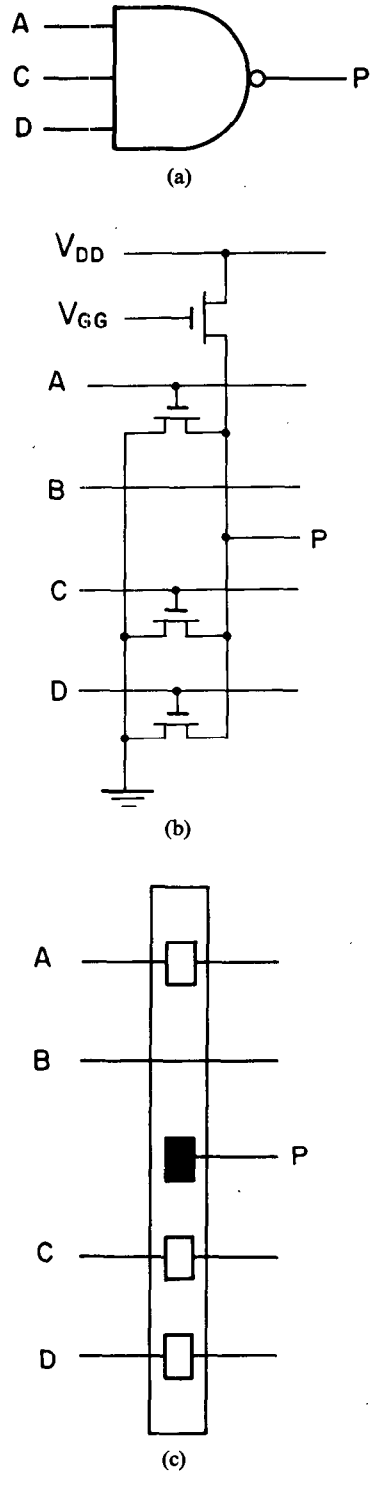


Fig. 1. (a) A NAND gate. (b) Its circuit schematic. (c) Its layout schematic.

$\{I(v)\}_{v\in V}$ such that $(u,v)\in E$ implies and is implied by $I(u)\cap I(v)\neq\emptyset$. The set of intervals is called a *realization* of the graph G.

For each permutation of modules we can draw horizontal intervals corresponding to nets, from which we obtain an interval graph corresponding to the gate sequence. The set of vertices of the interval graph is the set of nets. The vertices are adjacent if and only if the corresponding

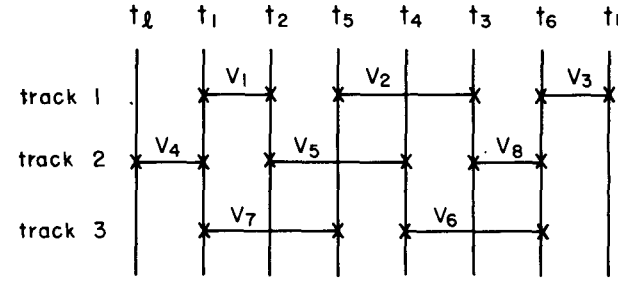


Fig. 2. A logic array realized with three tracks.

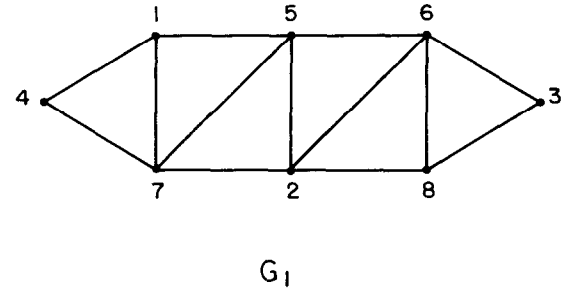


Fig. 3. Interval graph G_1 corresponding to the placement in Fig. 2.

intervals intersect when they are placed on the same track. It should be noted that the intervals are closed, and hence two intervals intersect each other even if their common point represents an end point of the respective intervals. The interval graph which corresponds to the placement in Fig. 2 is shown in Fig. 3.

For a given permutation of modules, the intervals should be placed in tracks so that the required number of tracks is kept as small as possible. This is similar to the coloring problem in graph theory. If we designate a specific color for each track, then the restriction that no two overlapping intervals can be placed in the same track is exactly the same as the restriction on graph coloring that no two adjacent vertices are colored by the same color. Therefore, the necessary number of tracks is the chromatic number of the corresponding interval graph. It is well known that the chromatic number of an interval graph is equal to the clique number or the maximum cardinality of all cliques [7].

Let us first introduce the necessary terminology. Let

$$T=\{t_l,t_1,t_2,\cdots,t_m,t_r\} \tag{1}$$

be the set of modules or gates, where t_l and t_r are boundary gates representing the nets to be extracted to the left and to the right, respectively. Let

$$V=\{v_1,v_2,\cdots,v_n\} \tag{2}$$

be the set of nets. We assume that there are m internal gates and n nets. The set of nets connected to gate t will be denoted by $V(t)$, and the set of gates to which net v is connected will be denoted by $T(v)$. Without loss of generality, we assume that

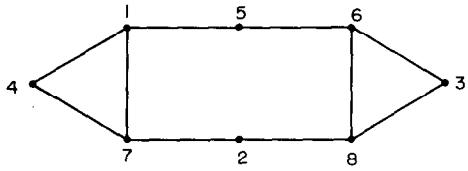
$$|V(t_i)|\geq 1, \qquad \text{for all } t_i \tag{3}$$

and

$$|T(v_j)|\geq 2, \qquad \text{for all } v_j. \tag{4}$$

gates	nets
t_ℓ	4
t_1	1, 4, 7
t_2	1, 5
t_3	2, 8
t_4	5, 6
t_5	2, 7
t_6	3, 6, 8
t_r	3

(a)

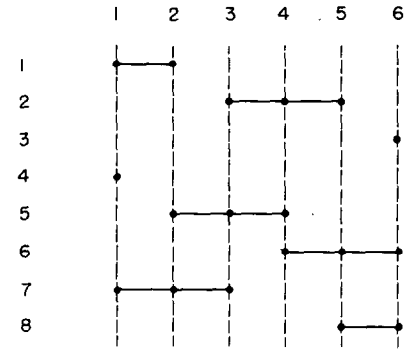


(b)

Fig. 4. Net list specification for the logic array in Fig. 2 in terms of a table and its connection graph $\boldsymbol{H}$.

$$A = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

(a)



(b)

Fig. 5. (a) v.d.c. matrix of the interval graph G_1 in Fig. 3. (b) The canonical realization of the v.d.c. matrix A.

The net list specification can be given by a table listing all the gates and the nets which are associated to each gate. Based on this, we construct a graph, called a *connection graph*,

$$H=(V,E) \tag{5}$$

where V is the set of n vertices representing the n nets. The edges are defined by

$$E=\{(x,y)|\exists t \text{ s.t. } x,y\in V(t)\} \tag{6}$$

that is, two vertices are adjacent if and only if there exists a common gate of the two corresponding nets. For the example of Fig. 2 the table specification and its connection graph $\boldsymbol{H}$ are given in Fig. 4. It is obvious that $\boldsymbol{H}$ is a subgraph of the interval graph in Fig. 3.

From the above, it is clear that the linear placement problem to minimize the number of tracks can be stated in terms of graph theory as follows: given a graph $\boldsymbol{H}$, find a supergraph by adding a set of edges, which is an interval graph and has the least clique number.

For the time being we ignore the boundary gates t_l and t_r because their fixed locations introduce further constraint on the problem. This will be taken care of in Section IV. In the following we will briefly present some fundamental properties of interval graphs. Special attention will be placed to the matrix representation of interval graphs.

It is obvious that every clique of an interval graph has its vertices corresponding to mutually overlapping intervals. A clique is called *dominant* if it is maximal, i.e., if it is not a proper subset of another clique. The total number of dominant cliques does not exceed $|V|$ [8].

Let $G=(V,E)$ be an interval graph with dominant cliques $C_1, C_2, \cdots, C_p$. Then a v.d.c. matrix (vertex versus dominant clique matrix) $A=[a_{ij}]$ is an $n\times p$ 0,1 matrix defined by

$$a_{ij}=\begin{cases} 1, & \text{if vertex } i\in C_j \\ 0, & \text{otherwise} \end{cases}$$

where $|V|=n$. The matrix is said to have the *consecutive ones property* if the ones in each row occur in consecutive positions. Fulkerson and Gross give the following theorem [9].

Theorem 1

A graph is an interval graph if and only if there exists an ordering of dominant cliques such that the v.d.c. matrix has the consecutive ones property.

The consecutive ones property of a v.d.c. matrix defines a *canonical realization*. In the ith row, let $l(i)$ be the leftmost column having one and $r(i)$ be the right most column having one. Then $l(i)\leqslant r(i)$. Let the interval $[l(i),r(i)]$ correspond to the ith vertex. In this way we obtain a set of intervals called the canonical realization of matrix A. The following theorem due to Fulkerson and Gross [9] is almost self-evident.

Theorem 2

Let A be a v.d.c. matrix, having the consecutive ones property, of an interval graph $G=(V,E)$. Then the cannonical realization of A is a realization of G.

For the graph G_1 in Fig. 3, the dominant cliques are $\{1,4,7\}$, $\{1,5,7\}$, $\{2,5,7\}$, $\{2,5,6\}$, $\{2,6,8\}$, and $\{3,6,8\}$. The v.d.c. matrix with the consecutive ones property is shown in Fig. 5(a). Its canonical realization is given in Fig. 5(b).

Finally, it should be pointed out that efficient algorithms on interval graphs are available: for an interval graph, all the dominant cliques can be listed in $0(|V|+|E|)$ time by the application of a lexicographic breadth first search [8]. Based on a data structure called PQ-trees we can determine an ordering of dominant cliques for which the v.d.c. matrix has the consecutive ones property in $0(|V|+|E|)$ time [10].

III. Gate Sequencing and Track Assignment

As stated in Section II, the problem of finding an optimum linear placement with minimum tracks can be formulated in terms of graph theory. Given a connection graph $H=(V,E)$, find a supergraph

$$\hat{H}=(V,E\cup F) \tag{7}$$

by adding a set of edges F to H such that the resulting graph $\hat{H}$ is an interval graph with minimum clique number. The set F is called an *augmentation* if $E\cap F=\varnothing$. An augmentation which leads to a least clique number is what we want. Unfortunately, this problem turns out to be NP complete [11]. A related problem of finding an augmentation F with a minimum $|F|$ is also NP complete [11]. Thus, like many combinatorial problems, we will aim at a *minimal augmentation*. A minimal augmentation is one such that no proper subset is an augmentation. In the example of Fig. 3, $G_1=(V,E\cup F_1)$ is an interval graph and may be viewed as that generated from the connection graph $H=(V,E)$ in Fig. 4. It is easy to see that F_1 in G_1 is a minimal augmentation.

In the present section we assume that the supergraph H has been obtained from H with a minimal augmentation F. The dominant cliques of H are next determined and a v.d.c. matrix with the consecutive ones property is obtained as described in the preceding section. The first problem we consider here is to find a proper gate sequence from the $n\times p$ v.d.c. matrix A, where p represents the number of dominant cliques. Let

$$C=\{C_1,C_2,\cdots,C_p\} \tag{8}$$

be the complete set of dominant cliques of $\hat{H}$, where C_j corresponds to the jth column of A. Each C_j includes a set of vertices represented by the nonzero positions in the jth column of A. From the matrix A, we also know that, for each vertex v_i, there associates a closed interval $[l(i),r(i)]$ in the ith row as discussed before.

To discuss the gate sequencing problem, it should be noted that, for any gate t, there exists a dominant clique C_j in $\hat{H}$ such that $V(t)\subseteq C_j$, where $V(t)$ is the set of vertices pertaining to gate t. This statement is obvious since $V(t)$ is a clique in H, and so in $\hat{H}$.

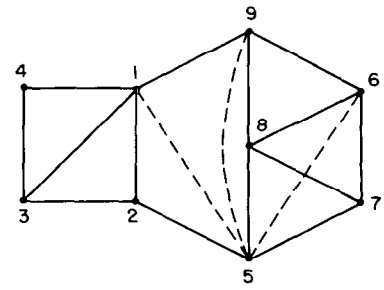


Fig. 6. Connection graph H and a minimal augmentation $F=\{(1,5),(5,9),(5,6)\}$ for Example 1.

TABLE I
Net Specification for Example 1

Gates	V(t)
t_ℓ	1,4
t_1	3,4
t_2	1,2,3
t_3	2,5
t_4	1,9
t_5	9
t_6	6,8,9
t_7	5,7,8
t_r	6,7

To determine C_j for each $V(t)$, we first form an interval

$$[L(t),R(t)]=\bigcap_{v_i\in V(t)}[l(i),r(i)]. \tag{9}$$

Then $L(t)\leqslant j\leqslant R(t)$ implies and is implied by $V(t)\subseteq C_j$.

Now we pick up arbitrarily for each gate t a dominant clique $C_{d(T)}\supseteq V(t)$, where

$$L(t)\leqslant d(t)\leqslant R(t). \tag{10}$$

Then we can obtain a gate sequence, or in other words an ordering of gates

$$t_{\pi(0)},t_{\pi(1)},\cdots,t_{\pi(m)},t_{\pi(m+1)}$$

such that

$$d(t_{\pi(0)})\leqslant d(t_{\pi(1)})\leqslant\cdots\leqslant d(t_{\pi(m)})\leqslant d(t_{\pi(m+1)}) \tag{11}$$

where $(\pi(0),\pi(1),\cdots,\pi(m),\pi(m+1))$ has to be considered to be a permutation of integers $1,\cdots,m$ and letters l and r.[1] Now we can state the following assertion.

Theorem 3

Let $t_{\pi(0)},\cdots,t_{\pi(m+1)}$ be a gate sequence satisfying (10) and (11), and let $H^*=(V,E^*)$ be the interval graph corresponding to the gate sequence. Then H^* coincides with $\hat{H}=(V,\hat{E})=(V,E\cup F)$ provided that F is a minimal augmentation.

[1]Two virtual gates t_l and t_r should be placed at the left-most and right-most ends, respectively, as pointed out in the preceding section. This constraint will be taken into consideration in the following section.

Proof: We first show $E^* \subseteq \hat{E}$. To prove this let $(u,v) \in E^*$. For the given gate sequence, let $I(u)$ and $I(v)$ be intervals corresponding to nets u and v, respectively. Then $(u,v) \in E^*$ implies that $I(u)$ and $I(v)$ overlap. Therefore, there exist gates t_1 and t_2 such that $u \in V(t_1)$, $v \in V(t_2)$ and $d(t_1) \leqslant d(t_2)$. Due to (9) and (10) we have $l(u) \leqslant d(t_1) \leqslant d(t_2) \leqslant r(v)$. Similarly we obtain $l(v) \leqslant r(u)$ and hence

$$[l(u), r(u)] \cap [l(v), r(v)] \neq \varnothing.$$

Since intervals $[l(u), r(u)]$ and $[l(v), r(v)]$ correspond to u and v, respectively, in the canonical realization of A, there follows that $(u,v) \in \hat{E}$.

If E^* is a proper subset of $\hat{E}$, then $E^* - E$ is an augmentation which is a proper subset of a minimal augmentation $F = \hat{E} - E$. This is a contradiction. Therefore $E^* = \hat{E}$ and $H^* = \hat{H}$. Q.E.D.

A gate sequence satisfying (11) can be obtained in $0(am)$ time, where a is the average value of $|V(t)|$'s.

Example 1: Consider a net specification given in Table I, where $m=7$ and $n=9$. The corresponding connection graph H is given in Fig. 6. By adding edges of a minimal augmentation $F = \{(1,5),(5,9),(5,6)\}$, $\hat{H} = (V, E \cup F)$ becomes an interval graph, since a v.d.c. matrix A of $\hat{H}$ has the consecutive ones property as shown below.

$$A = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 0 \end{bmatrix}. \tag{12}$$

For each gate t the interval $[L(t), R(t)]$ is computed and is summarized in Table II, with a possible choice for $d(t)$. Therefore, the gate sequence

$$t_l, t_1, t_2, t_3, t_4, t_6, t_5, t_7, t_r$$

is legitimate for the corresponding sequence $d(t)$'s is nondecreasing. The realization for this gate sequence is shown in Fig. 7.

The problem we consider next is to place the set of nets (vertices) on proper tracks so that the number of used tracks is equal to the clique number of $\hat{H} = (V, E \cup F)$. Once a gate sequence has been determined, an efficient algorithm, so-called "left edge" algorithm, is available for obtaining such a track assignment [12]. However, it should be stressed here that a track assignment can be obtained directly from the interval graph $\hat{H}$ without fixing a gate sequence. To be more precise, a v.d.c. matrix with the consecutive ones property derived from $\hat{H}$ associates the order of dominant cliques of $\hat{H}$. Now the "left edge" algorithm applied to the dominant clique ordering, rather than gate ordering, leads to an optimum track assignment.

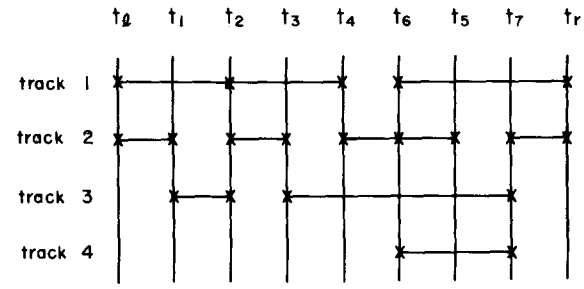


Fig. 7. A realization for Example 1.

TABLE II
INTERVALS $[L(t), R(t)]$ FOR EXAMPLE 1

Gates	[L(t), R(t)]	d(t)
t_l	[1, 1]	1
t_1	[1, 1]	1
t_2	[2, 2]	2
t_3	[3, 3]	3
t_4	[4, 4]	4
t_5	[4, 5]	5
t_6	[5, 5]	5
t_7	[6, 6]	6
t_r	[6, 6]	6

It is not difficult to prove that this process can be done in $0(|V|)$ time.

IV. Minimal Augmentation

In this section we first explain how to obtain a minimal augmentation. Then we present a method to take care of boundary gates.

Given a graph $H = (V, E)$ and an ordering $v_1, v_2, \cdots, v_n$ of vertices, define for $1 \leqslant i \leqslant n$

$$V_i = \{v_1, v_2, \cdots, v_{i-1}, v_i\}.$$

Let the section graph determined by V_3 be

$$H_3 = (V_3, E_3)$$

where

$$E_3 = \{(v_i, v_j) | v_i, v_j \in V_3, (v_i, v_j) \in E\}.$$

This is necessarily an interval graph for a graph having fewer than four vertices is an interval graph.

The section graph determined by V_4

$$H_4 = (V_4, E_4)$$

is not an interval graph if H_3 is a path and v_4 is connected to its two end vertices as is illustrated in Fig. 8(a). Then by adding an edge connecting v_4 and the intermediate vertex, the graph becomes an interval graph as shown in Fig. 8(b). Let F_4 be the set consisting of this single edge in this case and be the empty set otherwise. Thus $\hat{H}_4 =$

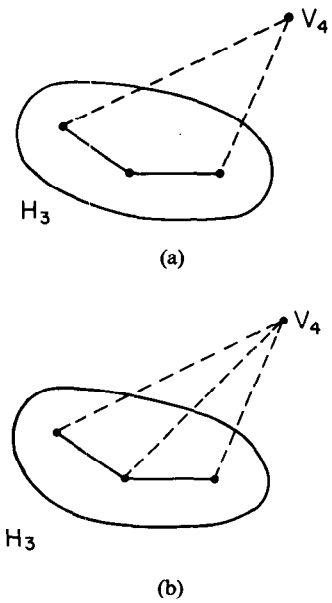


Fig. 8. (a) H_4 which is not an interval graph. (b) $\hat{H}_4$, an interval graph.

$(V_4, \hat{E}_4)=(V_4, E_4 \cup F_4)$ is an interval graph. It should be clear that F_4 is a minimal augmentation with respect to H_4, which consists of edges incident with v_4.

The above idea can be extended to the general case $4 \leqslant i \leqslant n$. We can assume

$$\hat{H}_{i-1}=(V_{i-1}, \hat{E}_{i-1})$$

is given as an interval graph. Then we add vertex v_i and edges in E connecting v_i and vertices of V_{i-1}, that is,

$$H_i=(V_i, E_i)$$

where

$$E_i=\hat{E}_{i-1} \cup \{(v_i, v) | v \in V_{i-1}, (v_i, v) \in E\}.$$

Let F_i be a minimal augmentation with respect to H_i, which consists of edges incident with v_i. Such a set exists because the graph becomes an interval graph if edges are added such that v_i is adjacent to all the vertices of V_{i-1}. This is seen as follows. Let $\{I(v)\}_{v \in V_{i-1}}$ be a realization of interval graph $\hat{H}_{i-1}$. Let $I(v_i)$ be an interval covering all the intervals $\{I(v)\}_{v \in V_{i-1}}$. Then this is a realization of the graph obtained by adding edges so that v_i is adjacent to all the vertices of V_{i-1}.

Thus by adding edges of F_i we obtain an interval graph

$$\hat{H}_i=(V_i, \hat{E}_i)=(V_i, E_i \cup F_i).$$

Repeating this process we finally obtain an interval graph

$$\hat{H}=(V, E \cup F)$$

where

$$F=F_4 \cup F_5 \cup \cdots \cup F_n.$$

Theorem 4

The set F thus obtained is a minimal augmentation.

Proof: To prove the assertion by contradiction, assume that a proper subset F' of F is an augmentation. Then there exists a unique partition of F' such that $F'=F_4' \cup \cdots \cup F_n'$ and $F_i' \subseteq F_i$ for $4 \leqslant i \leqslant n$. Let k be the first index such that $F_k' \subseteq F_k$. Note that $\hat{H}_k'=(V_k', E_k \cup F_k')$ is an interval graph for it is a section graph of interval graph $(V, F \cup F')$. Therefore, F_k' is an augmentation with respect to $H_k=(V_k, E_k)$. Since F_k' is a proper subset of a minimal augmentation F_k with respect to H_k, this is the desired contradiction. Q.E.D.

Based on this theorem an algorithm of finding a minimal augmentation has been developed, which runs in $0(|V| \cdot (|E|+|F|))$ time. This is presented in a separate paper [11].

So far we have not paid any attention to the constraint that two distinguished gates t_l and t_r are to be placed at the end-most positions. According to the method of finding a gate sequence as described in the preceding section, we can always obtain a gate sequence subject to the constraint if a v.d.c. matrix, having the consecutive ones property, of interval graph $\hat{H}=(V, E \cup F)$ is given such that the first column includes $V(t_l)$ and the last column includes $V(t_r)$. An augmentation is said to satisfy the boundary condition or, in short, to be a *B augmentation* if there exists such a v.d.c. matrix. A minimal B augmentation is one such that no proper subset is a B augmentation.

Remark: It is easy to obtain such a v.d.c. matrix if it exists [10].

Thus we have shown above that if F is a minimal B augmentation then there is a gate sequence placing t_l and t_r as the left-most and the right-most gates, respectively, for which the interval graph corresponding to the gate sequence is exactly $\hat{H}=(V, E \cup F)$.

Conversely, assume that there is a gate sequence which places t_l and t_r at the correct positions. Let $H^*=(V, E^*)=(V, E \cup F^*)$ be the corresponding interval graph. For notational simplicity, let $t_l, t_1, \cdots, t_m, t_r$ be the gate sequence. For each gate t, let $C(t)$ be the clique consisting of nets, each of which pertains to t or passes through t. It should be obvious that all dominant cliques are found among $C(t_l), C(t_1), C(t_2), \cdots, C(t_m), C(t_r)$. Reading this from left to right, let $C_1, C_2, \cdots, C_p$ be dominant cliques obtained in this order. Then a v.d.c. matrix A having $C_1, \cdots, C_p$ as the 1st, $\cdots$, the pth columns has the consecutive ones property, and

$$V(t_l) \subseteq C(t_l) \subseteq C_1 \qquad V(t_r) \subseteq C(t_r) \subseteq C_p. \tag{13}$$

Hence F^* is a B augmentation. This justifies our policy of finding a minimal B augmentation and then determining a proper gate sequence subject to the constraint on the two distinguished gates t_l and t_r.

In what follows our main concern is how to obtain a minimal B augmentation. Before going further we assume hereafter that

$$V(t_l) \cap V(t_r)=\varnothing. \tag{14}$$

If there exists a net $v \in V(t_l) \cap V(t_r)$, net v connects the left most gate t_l and the right-most gate t_r; it occupies one full track. Such a net v can be excluded at the outset, and

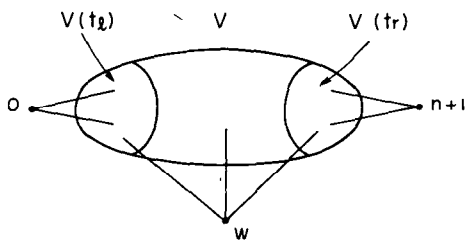


Fig. 9. Graph $H'=(V',E')$ formed from $H=(V,E)$.

only afterwards it needs to be added to occupy a new track.

Instead of applying the algorithm of finding a minimal augmentation to H, we form a new graph H' from H and then apply the algorithm to H'. We add three more vertices 0, $n+1$, and w to the connection graph $H=(V,E)$. The new graph $H'=(V',E')$ is defined as follows and is shown in Fig. 9:

$$V'=V\cup\{0,n+1,w\}$$

and

$$E'=E\cup\{(0,v)|v\in V(t_l)\}\cup\{(n+1,v)|v\in V(t_r)\}\cup\{(w,v)|v\in V\}$$

thus

$$|V'|=|V|+3 \quad \text{and} \quad |E'|\leqslant|E|+2|V|. \tag{15}$$

Let $v_1,\cdots,v_k$ be an arbitrary ordering of vertices of $V-V(t_l)-V(t_r)$, and let α' be an ordering of V' such that vertices of $V(t_l)$, vertices of $V(t_r)$, 0, $n+1$, w, $v_1,\cdots,v_k$ are ordered in this way. We apply the algorithm to H' with ordering α' and obtain a minimal augmentation with respect to H'. We can prove the following theorem.

Theorem 5

Set F thus obtained is a minimal B augmentation with respect to connection graph $H=(V,E)$.

A proof is given in the appendix. From (15) this can be done in $0(|V|\cdot(|E|+|F|))$ time provided that H is connected and hence $|V|\leqslant|E|+1$.

Example 2: Consider a net specification as shown in Table III, where $m=3$ and $n=5$. The connection graph H is shown in Fig. 10(a), which is an interval graph as seen in Fig. 10(b). The extended graph H' is shown in Fig. 10(c). Since $V(t_l)=\{1,3,4\}$ and $V(t_r)=5$, we take an ordering α'

$$1,3,4,5,0,6,w,2.$$

Then $F=\{(2,4)\}$ is a minimal B augmentation. Dominant cliques of $\hat{H}=(V,E\cup F)$ are $C_1=\{1,2,3,4\}$ and $C_2=\{3,4,5\}$. A v.d.c. matrix A is the following:

$$A=\begin{bmatrix}1&0\\1&0\\1&1\\1&1\\0&1\end{bmatrix}.$$

It is easily seen that $V(t_l)\subseteq C_1$ and $V(t_r)\subseteq C_2$.

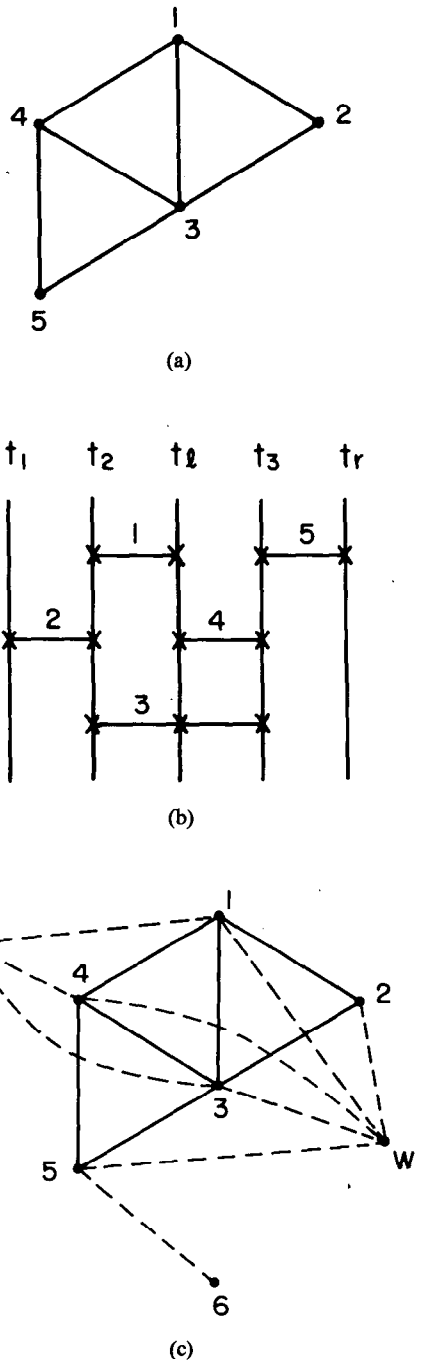


Fig. 10. (a) Connection graph H. (b) A realization of H. (c) Extended graph H'.

TABLE III
NET SPECIFICATION FOR EXAMPLE 2

Gates	V(t)
t_ℓ	1,3,4
t_1	2
t_2	1,2,3
t_3	3,4,5
t_r	5

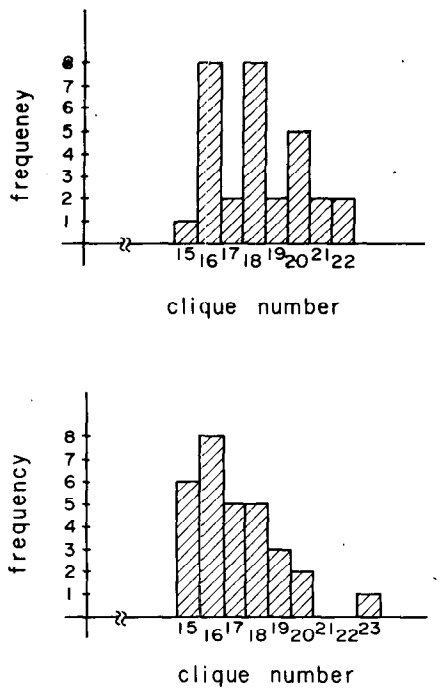


Fig. 11. (a) Distribution of clique number for Data 1. (b) Distribution of clique number for Data 2.

TABLE IV
LEAST AND AVERAGE CLIQUE NUMBER OF H

Data No.	No. of gates	No. of nets	No. of edges of H	Least clique number	Average clique number
1	48	48	161	15	18.2
2	48	49	173	15	17.1
3	48	48	176	13	15.4
4	48	50	288	18	21.2
5	48	48	222	9	13.2
6	48	48	294	12	16.3
7	48	49	359	17	20.3

V. Computational Results and Discussions

A Fortran program run on a NEC ACOS 77/700 computer was implemented to examine the property of minimal augmentations. Seven problems of approximately the same size were provided as test data. Using the program, 30 minimal augmentations for each problem were obtained based on randomly generated vertex orderings, and then the least and average clique numbers of the resulting interval graphs were calculated. Table IV summarizes the computational results with the problem sizes. Fig. 11 illustrates the distribution of clique numbers of the resulting interval graphs for Data 1 and 2.

The results suggest us a good heuristic method to obtain nearly optimum solution; that is to obtain several minimal augmentations based on randomly generated vertex orderings and then to choose the best solution. In these problems, the computer time for obtaining a minimal augmentation was about 4 s. The heuristic algorithm has been compared with those based on branch and bound [5],[6] and it is observed that is finds solutions with less or equal clique numbers for all the problems in Table IV.

For practical use, our program can readily be improved by appending (1) a constructive algorithm to obtain a good vertex orderings and/or (2) an iterative improvement scheme starting from a minimal augmentation.

VI. Appendix
Proof of Theorem 5

We prove the theorem step by step. Let $\boldsymbol{H}_0=(V_0,E_0)$ be the section graph of the connection graph $\boldsymbol{H}=(V,E)$ determined by $V_0=V(t_l)\cup V(t_r)$. Our algorithm of finding a minimal augmentation with respect to $\boldsymbol{H}'$ starts with finding a minimal augmentation F_0 with respect to $\boldsymbol{H}_0$ to construct an interval graph $\boldsymbol{H}_0=(V_0,E_0\cup F_0)$. We first show a key property of $\boldsymbol{H}_0$. Since every vertex of $\boldsymbol{H}_0$ belongs to either $V(t_l)$ or $V(t_r)$ and both $V(t_l)$ and $V(t_r)$ are cliques, it is clear that two distinct dominant cliques C_l and C_r including $V(t_l)$ and $V(t_r)$, respectively, are uniquely determined, unless V_0 itself is the only one dominant clique. Based on this we give the following lemma.

Lemma 1: C_l and C_r are placed at the endmost positions for any v.d.c. matrix having the consecutive ones property of $\hat{\boldsymbol{H}}_0$.

Proof: Suppose C_l lies between C_r and another dominant clique, say C_j. Then, from the consecutive ones property, $v\in C_j\cap C_r$ implies $v\in C_l$. Since every vertex belongs to C_l or C_r, it follows that $C_j\subseteq C_l$. This contradicts the maximality of C_j. Hence C_l must be placed at one of the end-most positions. The assertion for C_r can also be proved in the same way. Q.E.D.

Our algorithm is next followed by the stage of adding vertices $\{0,n+1,w\}$ and the edges incident with them.

Let $\boldsymbol{H}_0'=(V_0',E_0')$ be the section graph of $\boldsymbol{H}'=(V',E')$ determined by $V_0'=\{0,n+1,w\}\cup V_0$. We next prove that $\hat{\boldsymbol{H}}_0'=(V_0',E_0'\cup F_0)$ is an interval graph, where F_0 is the augmentation of $\boldsymbol{H}_0$ given above. For this purpose we give a realization of $\hat{\boldsymbol{H}}_0$ as follows. Consider a v.d.c matrix with the consecutive ones property of $\hat{\boldsymbol{H}}_0$, and let C_1 and C_q be the first and last columns (dominant cliques), respectively. Then, from Lemma 1, either $C_l=C_1$ and $C_r=C_q$ or $C_l=C_q$ and $C_r=C_1$. Without loss of generality we assume the former. In the canonical realization, the intervals for a vertex $v_i\in C_l$ and a vertex $v_j\in C_r$ are given by $I(v_i)=[1,r(i)]$ and $I(v_j)=[l(j),q]$, respectively. Now, for each vertex $v_i\in V(t_l)$ and each vertex $v_j\in V(t_r)$, we modify the corresponding intervals from $[1,r(i)]$ to $[0,r(i)]$ and from $[l(j),q]$ to $[l(j),q+1]$, respectively. Clearly, the set of intervals after the modification is still a realization of $\hat{\boldsymbol{H}}_0$. Let $[0,0]$, $[q+1,q+1]$, and $[1,q]$ be intervals for vertices $0,n+1$ and w, respectively. We add these intervals to the above set. Then it is easy to see that the resulting set of intervals is a realization of $\hat{\boldsymbol{H}}_0'=(V_0',E_0'\cup F_0)$.

Since $\hat{\boldsymbol{H}}_0'$ is already an interval graph, there is no need to add edges, which leads to the following lemma.

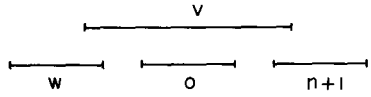


Fig. 12. Interval for v overlaps with that for 0.

Lemma 2: If $x \in \{0, n+1, w\}$ and $y \in V_0'$, then $(x,y) \notin F$.

Next we show the following lemma.

Lemma 3: In any realization of $\hat{H}' = (V', E' \cup F)$, the interval for w lies between those for 0 and $n+1$.

Proof: Suppose on the contrary that the interval for 0 lies between those for $n+1$ and w as shown in Fig. 12. Let $v \in V(t_r)$, then the interval for v overlaps with those for $n+1$ and w, and hence with that for 0. Therefore $(0,v) \in E' \cup F$, which contradicts the assumption (14) or the assertion of Lemma 2. In the same way we can prove that the interval for $n+1$ cannot lie between those for 0 and w. Q.E.D.

Based on the preceding two lemmas we prove the following.

Lemma 4: If $v \in V - V_0$, then $(0,v) \notin F$ and $(n+1,v) \notin F$.

Proof: For definitensess, assume $(0,v) \in F$ and lead to a contradiction. Let $\{I(v)\}_{v \in V'}$ be a realization of interval graph $\hat{H}' = (V', E' \cup F)$. Without loss of generality we can assume from Lemma 3 that intervals $I(0)$, $I(w)$, and $I(n+1)$ lie in this order from left to right. Let $I(v) = [l_v, r_v]$, $I(0) = [l_0, r_0]$, and $I(w) = [l_w, r_w]$. Since $I(v)$ overlaps with $I(0)$ and $I(w)$, there follows

$$l_v \leqslant r_0 < l_w \leqslant r_v.$$

Now modify $I(v)$ from $[l_v, r_v]$ to $[r_0 + \epsilon, r_v]$, where ϵ is a sufficiently small positive number. Then the existing overlap of $I(0)$ with $I(v)$ disappears. On the other hand, all other existing nonempy overlaps remain as they stand. We can show this in the following way. Let $u \neq 0$ be a vertex such that $(u,v) \in E' \cup F$, and assume that the existing overlap of $I(u)$ with $I(v)$ disappears after the modification.

Then,

$$r_u < r_0 + \epsilon$$

for an arbitrary small positive number ϵ, where $I(u) = [l_u, r_u]$. This means

$$r_u \leqslant r_0$$

and then $I(u)$ cannot overlap with $I(w)$. Hence $u = 0$, which is a contradiction.

The argument made above clearly indicates that $F - \{(0,v)\}$ is an augmentation, which contradicts the minimality of F. Q.E.D.

The assertions made in Lemmas 2 and 4 are combined together to give the following key lemma.

Lemma 5: $(x,y) \in F$ implies $x, y \in V$.

Due to the lemma, $\hat{H} = (V, E \cup F)$ is the section graph of interval graph $\hat{H}' = (V', E' \cup F)$ determined by V. Thus $\hat{H}$ is an interval graph and hence F is an augmentation with respect to $H = (V,E)$. Next we show that F satisfies the boundary condition.

Let A' be an $(n+3) \times p'$ v.d.c. matrix of $\hat{H}'$ having the consecutive ones property. Due to the assumption (14) and Lemma 5, $V'(t_l) = \{0\} \cup V(t_l)$ is the only one dominant clique, of H', which contains vertex 0. Similarly, $V'(t_r) = \{n+1\} \cup V(t_r)$ is the unique dominant clique, of $\hat{H}'$, which contains vertex $n+1$. It is also clear that all the other dominant cliques contain vertex w. Let $\{I(v)\}_{v \in V'}$ be the canonical realization of A' and let $C_1', \cdots, C_{p'}'$ be dominant cliques corresponding to the 1st, $\cdots$, p'th columns of A', respectively. Then due to Lemma 3, $I(0) = [1,1]$, $I(w) = [2, p'-1]$, and $I(n+1) = [p', p']$. Therefore $C_1' = V'(t_l)$ and $C_{p'}' = V'(t_r)$.

Now we discard the rows corresponding to vertices $0, n+1$, and w. Then there remains an $n \times p'$ matrix A'' having the consecutive ones property. Note that the first column corresponds to $V(t_l)$ and the last to $V(t_r)$. It should also be noted that all the dominant cliques in $\hat{H}$ have corresponding columns in A''. Therefore, by further discarding nondominant cliques and some redundant dominant cliques, we obtain a v.d.c. matrix A of H having the consecutive ones property. Thus the first column of A includes $V(t_l)$ and the last column $V(t_r)$. This implies that F satisfies the boundary condition.

What remains to be shown is the minimality of F. To prove this by contradiction, assume that a proper subset F^* of F is a B augmentation. Let A^* be a $n \times q$ v.d.c. matrix of $H^* = (V, E \cup F^*)$ having the consecutive ones property. Let $\{I(v)\}_{v \in V}$ be its canonical realization. Since $V(t_l)$ is included in the first column, $v \in V(t_l)$ implies $l_v = 1$ where $I(v) = [l_v, r_v]$. Similarly $v \in V(t_r)$ implies $r_v = q$. Then, for every vertex $v \in V(t_l)$, modify $I(v)$ from $[1, r_v]$ to $[0, r_v]$ and, for every vertex $v \in V(t_r)$, from $[l_v, q]$ to $[l_v, q+1]$. This is still a realization of H^*. Then add three intervals $[0,0]$, $[1,q]$, and $[q+1, q+1]$ for vertices 0, w, and $n+1$. It is easily seen that this is a realization of graph $(V', E' \cup F^*)$ and hence F^* is an augmentation with respect to $H' = (V', E')$. As F^* is a proper subset of a minimal augmentation F with respect to $H' = (V', E')$, this is the desired contradiction. This completes the proof of Theorem 5.

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