1 NOP No instruction retired yet. 2 NOP No instruction retired yet. 3 NOP No instruction retired yet. 4 NOP No instruction retired yet. 5 lbi r0, 0 Instruction in Write Back stage. 6 lbi, r5, 43 Instruction in Write Back stage. 7 lbi, r6, 43 Instruction in Write Back stage. 8 lbi, r7, 43 Instruction in Write Back stage. 9 ld r1, r0, 0 Instruction in Write Back stage. 10 NOP st r5, r1, 0 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 0 (RAW on r1) 11 NOP st r5, r1, 0 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 0 (RAW on r1) 12 st r5, r1, 0 Instruction in Write Back stage. 13 ld r1, r0, 2 Instruction in Write Back stage. 14 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 15 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 16 st r6, r1, 1 Instruction in Write Back stage. 17 Id r1, r0, 4 Instruction in Write Back stage. 18 NOP st r7, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 19 NOP st r7, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 Instruction in Write Back stage. 19 Instruction in Write Back stage. 19 Instruction in Write Back stage.	Cycle	Instruction Retired	Reason
3 NOP	1	NOP	No instruction retired yet.
4 NOP	2	NOP	No instruction retired yet.
5 Ibi r0, 0 Instruction in Write Back stage. 6 Ibi, r5, 43 Instruction in Write Back stage. 7 Ibi, r6, 43 Instruction in Write Back stage. 8 Ibi, r7, 43 Instruction in Write Back stage. 9 Id r1, r0, 0 Instruction in Write Back stage. 10 NOP St r5, r1, 0 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 0 (RAW on r1) 11 NOP St r5, r1, 0 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 0 (RAW on r1) 12 st r5, r1, 0 Instruction in Write Back stage. 13 Id r1, r0, 2 Instruction in Write Back stage. 14 NOP St r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 2 (RAW on r1) 15 NOP St r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 2 (RAW on r1) 16 st r6, r1, 1 Instruction in Write Back stage. 17 Id r1, r0, 4 Instruction in Write Back stage. 18 NOP St r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 4 (RAW on r1) 19 NOP St r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 4 (RAW on r1)	3	NOP	No instruction retired yet.
Solid Ibi r0, 0 Instruction in Write Back stage.	4	NOP	No instruction retired yet.
7 lbi, r6, 43 Instruction in Write Back stage. 8 lbi, r7, 43 Instruction in Write Back stage. 9 ld r1, r0, 0 Instruction in Write Back stage. 10 NOP st r5, r1, 0 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 0 (RAW on r1) 11 NOP st r5, r1, 0 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 0 (RAW on r1) 12 st r5, r1, 0 Instruction in Write Back stage. 13 ld r1, r0, 2 Instruction in Write Back stage. 14 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 15 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 16 st r6, r1, 1 Instruction in Write Back stage. 17 ld r1, r0, 4 Instruction in Write Back stage. 18 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1)	5	lbi r0, 0	Instruction in Write Back stage.
8	6	lbi, r5, 43	Instruction in Write Back stage.
9 Id r1, r0, 0 Instruction in Write Back stage. 10 NOP st r5, r1, 0 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 0 (RAW on r1) 11 NOP st r5, r1, 0 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 0 (RAW on r1) 12 st r5, r1, 0 Instruction in Write Back stage. 13 Id r1, r0, 2 Instruction in Write Back stage. 14 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 2 (RAW on r1) 15 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 2 (RAW on r1) 16 st r6, r1, 1 Instruction in Write Back stage. 17 Id r1, r0, 4 Instruction in Write Back stage. 18 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction Id r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.	7	lbi, r6, 43	Instruction in Write Back stage.
St r5, r1, 0 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 0 (RAW on r1) NOP	8		Instruction in Write Back stage.
of r1 that will be written in by last instruction ld r1, r0, 0 (RAW on r1) 11 NOP st r5, r1, 0 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 0 (RAW on r1) 12 st r5, r1, 0 Instruction in Write Back stage. 13 ld r1, r0, 2 Instruction in Write Back stage. 14 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 15 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 16 st r6, r1, 1 Instruction in Write Back stage. 17 ld r1, r0, 4 Instruction in Write Back stage. 18 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.	9	ld r1, r0, 0	Instruction in Write Back stage.
(RAW on r1) 11 NOP st r5, r1, 0 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 0 (RAW on r1) 12 st r5, r1, 0 Instruction in Write Back stage. 13 ld r1, r0, 2 Instruction in Write Back stage. 14 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 15 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 16 st r6, r1, 1 Instruction in Write Back stage. 17 ld r1, r0, 4 Instruction in Write Back stage. 18 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) Instruction in Write Back stage.	10	NOP	st r5, r1, 0 stalls at its Decode stage to wait for the value
St r5, r1, 0 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 0 (RAW on r1) 12			of r1 that will be written in by last instruction ld r1, r0, 0
of r1 that will be written in by last instruction ld r1, r0, 0 (RAW on r1) 12 st r5, r1, 0 Instruction in Write Back stage. 13 ld r1, r0, 2 Instruction in Write Back stage. 14 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 15 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 16 st r6, r1, 1 Instruction in Write Back stage. 17 ld r1, r0, 4 Instruction in Write Back stage. 18 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.			(RAW on r1)
(RAW on r1) 12 st r5, r1, 0 Instruction in Write Back stage. 13 ld r1, r0, 2 Instruction in Write Back stage. 14 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 15 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 16 st r6, r1, 1 Instruction in Write Back stage. 17 ld r1, r0, 4 Instruction in Write Back stage. 18 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.	11	NOP	st r5, r1, 0 stalls at its Decode stage to wait for the value
12st r5, r1, 0Instruction in Write Back stage.13ld r1, r0, 2Instruction in Write Back stage.14NOPst r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1)15NOPst r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1)16st r6, r1, 1Instruction in Write Back stage.17ld r1, r0, 4Instruction in Write Back stage.18NOPst r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1)19NOPst r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1)20st r7, r1, 1Instruction in Write Back stage.			of r1 that will be written in by last instruction ld r1, r0, 0
13			(RAW on r1)
14NOPst r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1)15NOPst r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1)16st r6, r1, 1Instruction in Write Back stage.17ld r1, r0, 4Instruction in Write Back stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1)19NOPst r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1)20st r7, r1, 1Instruction in Write Back stage.	12	st r5, r1, 0	Instruction in Write Back stage.
of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 15 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 16 st r6, r1, 1 Instruction in Write Back stage. 17 ld r1, r0, 4 Instruction in Write Back stage. 18 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.	13	ld r1, r0, 2	Instruction in Write Back stage.
(RAW on r1) 15 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 16 st r6, r1, 1 Instruction in Write Back stage. 17 ld r1, r0, 4 Instruction in Write Back stage. 18 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.	14	NOP	st r6, r1, 1 stalls at its Decode stage to wait for the value
15 NOP st r6, r1, 1 stalls at its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 16 st r6, r1, 1 Instruction in Write Back stage. 17 ld r1, r0, 4 Instruction in Write Back stage. 18 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.			of r1 that will be written in by last instruction ld r1, r0, 2
of r1 that will be written in by last instruction ld r1, r0, 2 (RAW on r1) 16			(RAW on r1)
(RAW on r1) 16 st r6, r1, 1 Instruction in Write Back stage. 17 ld r1, r0, 4 Instruction in Write Back stage. 18 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.	15	NOP	st r6, r1, 1 stalls at its Decode stage to wait for the value
16st r6, r1, 1Instruction in Write Back stage.17Id r1, r0, 4Instruction in Write Back stage.18NOPst r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1)19NOPst r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1)20st r7, r1, 1Instruction in Write Back stage.			of r1 that will be written in by last instruction ld r1, r0, 2
17			(RAW on r1)
18 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.	16	st r6, r1, 1	Instruction in Write Back stage.
of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.	17	$ld r1, r0, \overline{4}$	Instruction in Write Back stage.
(RAW on r1) 19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.	18	NOP	st r7, r1, 1 stalls ate its Decode stage to wait for the value
19 NOP st r7, r1, 1 stalls ate its Decode stage to wait for the value of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.			of r1 that will be written in by last instruction ld r1, r0, 4
of r1 that will be written in by last instruction ld r1, r0, 4 (RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.			(RAW on r1)
(RAW on r1) 20 st r7, r1, 1 Instruction in Write Back stage.	19	NOP	st r7, r1, 1 stalls ate its Decode stage to wait for the value
20 st r7, r1, 1 Instruction in Write Back stage.			of r1 that will be written in by last instruction ld r1, r0, 4
	20	st r7, r1, 1	Instruction in Write Back stage.

^{*}We are using a bypassing register file, so there are usually two stalls for a data dependency.

*In our design, the processor will detect Halt in the Halt instruction's MEM stage and then end the program. Thus, the Halt instruction will not enter Write Back stage. That's why we put nothing in the cycle number column for Halt in the above table as there is no such cycle that Halt is in Write Back stage.