四川大学期末考试试题（闭卷）

（2017~2018 学年第 2 学期）　　A 卷

课程号：**311039030**　课程名称：**数字逻辑：应用与设计**　任课教师：＿＿＿＿＿＿

适用专业年级：**软件工程 2017 级**　学号：＿＿＿＿＿＿　姓名：＿＿＿＿＿＿

考生承诺

我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

1、已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；

2、不带手机进入考场；

3、考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

考生签名：

题　　号	一(20%)	二(18%)	三(42%)	四(20%)
得　　分				
卷面总分		阅卷时间		

注意事项：1. 请务必将本人所在学院、姓名、学号、任课教师姓名等信息准确填写在试题纸和添卷纸上；

2. **请将答案全部填写在本试题纸上；**

3. 考试结束，请将试题纸、添卷纸和草稿纸一并交给监考老师。

评阅教师	得分

一、单项选择题（本大题共 10 小题，每小题 2 分，共 20 分）

提示：在每小题列出的四个备选项中只有一个是符合题目要求的，请将其代码填写在下表中。错选、多选或未选均无分。

1	2	3	4	5	6	7	8	9	10

1. A pulse in a certain waveform has a frequency of 50 Hz. It repeats itself every

(a) 1 ms　(b) 20 ms　(c) 50 ms　(d) 100 ms

2. The code that has an even-parity error is

(a) 1010011　(b) 1101000　(c) 1001000　(d) 1110111

3. The binary number 10110011100101010001 can be written in octal as

(a) 5471230　(b) 5471241　(c) 2634521　(d) 23162501

4. An example of a product-of-sums expression is

(a) A(B + C) + AC　(b) (A + B)(A + B + C)

(c) A + B + BC　(d) both answers (a) and (b)

5. The AND operation can be produced with

(a) two NAND gates　(b) three NAND gates

(c) one NOR gate　(d) three NOR gates

6. To expand a 2-bit parallel adder to a 4-bit parallel adder, you must

(a) use two 2-bit adders with no interconnections

(b) use two 2-bit adders and connect the sum outputs of one to the bit inputs of the other

(c) use four 2-bit adders with no interconnections

(d) use two 2-bit adders with the carry output of one connected to the carry input of the other

7. For an edge-triggered D flip-flop,

(a) a change in the state of the flip-flop can occur only at a clock pulse edge

(b) the state that the flip-flop goes to depends on the D input

(c) the output follows the input at each clock pulse

(d) all of these answers

8. A J-K flip-flop with J = 1 and K = 1 has a 10 kHz clock input. The Q output is

(a) constantly HIGH (b) constantly LOW

(c) a 10 kHz square wave (d) a 5 kHz square wave

9. A register's functions include

(a) data storage (b) data movement

(c) neither (a) not (b) (d) both (a) and (b)

10. A modulus-12 counter must have

(a) 12 flip-flops (b) 3 flip-flops (c) 4 flip-flops (d) synchronous clocking

评阅教师	得分

二、填空题（本大题共 9 空，每空 2 分，共 18 分）。

1. (18pts) Complete the following table of equivalent values. Use binary numbers with a sign bit and 7 bits for the value.

Decimal	Signed Magnitude	2's Complement code	1's Complement code
		11111111	
-1			
	11111111		

评阅教师	得分

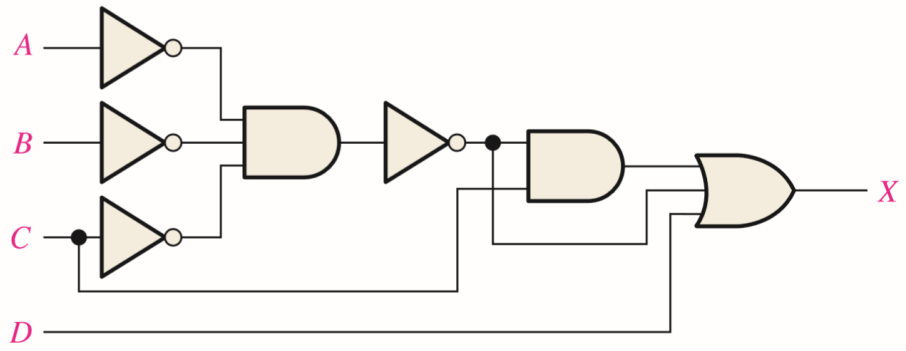
三、分析计算题（本大题共 6 小题，共 42 分）。

1. (共 5 分) Using Boolean algebra, simplify the following expression, and draw the logic diagram using only NOR gates
   BC + (B' + C')D + BC

2. (共 6 分) Implement the basic logic gates (AND, OR, NOT) only by the NAND gates respectively.

3. (共 15 分)Simplify the following expressions using Karnaugh maps.
   (1) f(A, B, C,D) = A'B(C' D' + C'D) + AB(C' D' + C'D) + AB' C'D
   (2) f(A,B,C,D) = (A + B' + C + D')(A' + B + C' + D)(A' + B' + C' + D)
   (3) f(a, b, c, d) =∏(0,3,4,7,8)+∏d(10,11,12,13,14,15)

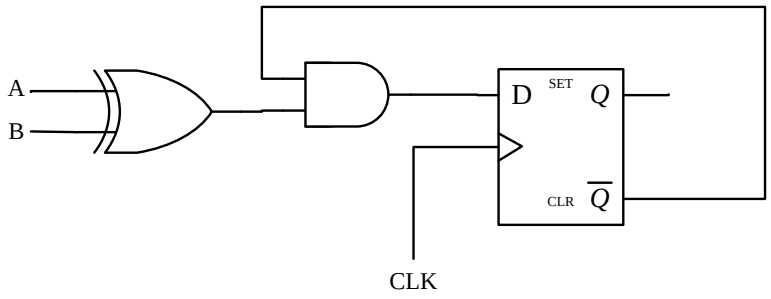
4. (共 6 分) Write the switching expressions for the following logic circuits and Simplify it.

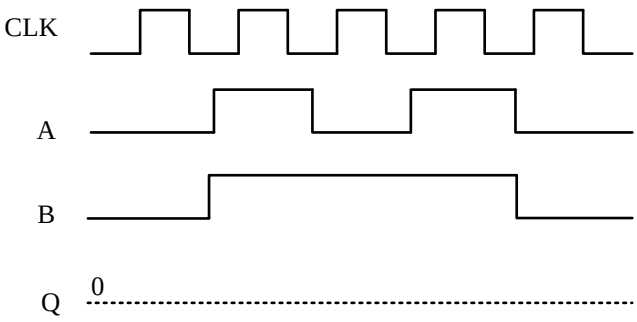


5. (共 5 分) Realize the function shown below using a 3-to-8 decoder and the appropriate logic gates.

   ***F*(*a*,*b*,*c*) =Σ (1,2,6,7)**

6. (共 5 分) Given the logic diagram shown below, complete the partial timing diagram





评阅教师	得分

四、设计题（本大题共 2 小题，共 20 分）。

1. (共 8 分) Consider the following three-variable function:

f(a,b,c) = bc'+ab'+ab

(a) Give its canonical SOP and canonical POS.(4 points)

(b) Implement the function using **more than two methods** (draw out the logic diagram). (4 points)

2. (共 12 分)　Given the state diagram below.

(1) Construct the transition tables for the state diagram.

(2) Using the transition table constructed in problem (1), construct excitation tables using J-K flip-flop.

(3) Derive and simplify the excitation equation for the excitation table developed in problem (2) and the output equation.