## 四川大学期末考试试题 (闭卷)

## (2017~2018 学年第1学期)

B卷

课程号: <u>3</u> 2	11077030	课程名称:	计算机组成和体系统	结构	任课教师:			
适用专业年纪	级: <u>软件</u> J	程 2016 级	学号:					
1、已按要求 2、不带手机	将考试禁止携 进入考场;	带的文具用品或	考生承诺 和《四川大学本科学生考试证 与考试有关的物品放置在指定	定地点;	(修订)》,郑重承诺:			
	考生签名:							
题 号	-(	20%)	二(10%)	三(46%	四(24%)			
得 分								
卷面总分		教师签名		阅卷时间				
# 大き では、								

教务处试题编号: 311-10

评阅教师 得分 二、判断题(本大题共 5 小题,每小题 2 分,共 10 分) 提示: 正确打✓,错误打×,将其结果填写在下表中。				
1	2	3	4	5

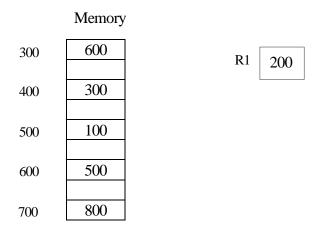
- 1. (共2分)A branch instruction changes the flow of information by changing the PC.
- 2. (共2分) For increasing the overall performance of a system, we have the options of CPU optimization, Memory optimization and I/O optimization
- 3. (共2分)Registers are storage locations within the CPU itself.
- 4. (共2分) MARIE has a common bus scheme, which means a number of entities share the bus.
- 5. (共2分)A fixed length instruction must have a fixed length opcode.

评阅教师	得分	三、	问答题(本大题共6小题,共46分)。
		1.	(共14分) Suppose that a 1M * 16 main memory is built using 128KB * 8

RAM chips and memory is word-addressable.

- a) How many RAM chips are necessary?
- b) How many RAM chips are there per memory word?
- c) How many address bits are needed for each RAM chip?
- d) How many banks will this memory have?
- e) How many address bits are needed for all of memory?
- f) If high-order interleaving is used, where would address  $63_{10}$  be located?
- g) Repeat Exercise for low-order interleaving.
- 2. (共6分) Consider a byte-addressable computer with 24-bit addresses, a cache capable of storing a total of 64KB of data, and blocks of 32 bytes. Show the format of a 24-bit memory address for:
  - a) direct mapped
  - b) associative
  - c) 4-way set associative
- 3. (共8分) The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with 4 fields: an opcode field; a mode field to specify 1 of 7 addressing modes; a register address field to specify 1 of 60 registers; and a memory address field. Assume an instruction is 32 bits long. Answer the following:

- a) How large must the mode field be?
- b) How large must the register field be?
- c) How large must the address field be?
- d) How large is the opcode field?
- 4. (共4分) A nonpipeline system takes 100ns to process a task. The same task can be processed in a 5-stage pipeline with a clock cycle of 20ns.
  - a) Determine the speedup ratio of the pipeline for 100 tasks.
  - b) What is the theoretical speedup that could be achieved with the pipeline system over a nonpipelined system?
- 5. (共6分) Convert the following expressions from infix to reverse Polish (postfix) notation.
- a) X \* Y + W \* Z + V \* U
- b) W \* X + W \* (U \* V + Z)
- c) (W \* (X + Y \* (U \* V)))/(U \* (X + Y))
- 6. (共8分) Suppose we have the instruction Load 400. Given that memory and register R1 contain the values below:



Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	Value Loaded into AC
Immediate	
Direct	
Indirect	
Indexed	

评阅教师 得分

四、计算题(本大题共2小题,共24分)。

1.  $(\sharp 15 \, \%)$  A system implements a paged virtual address space for each process using a one level page table. The maximum size of virtual address space is 32MB. The page table for the running process includes the following valid entries (the  $\rightarrow$  notation indicates that a virtual page maps to the given page frame, that is, it is located in that frame):

姓名:

Virtual page 2 → Page frame 4

Virtual page  $4 \rightarrow \text{Page frame } 1$ 

Virtual page  $1 \rightarrow \text{Page frame } 2$ 

Virtual page  $3 \rightarrow Page frame 16$ 

Virtual page  $0 \rightarrow \text{Page frame } 15$ 

The page size is 512 bytes and the maximum physical memory size of the machine is 4MB.

- a) How many bits are required for each virtual address?
- b) How many bits are required for each physical address?
- c) What is the maximum number of entries in a page table?
- d) To which physical address will the virtual address 511<sub>10</sub> translate?
- e) Which virtual address will translate to physical address 1023<sub>10</sub>?
- 2. (共9分) A 2-way set associative cache consists of four sets. Main memory contains 4K blocks of eight words each.
- a) Show the main memory address format that allows us to map addresses from main memory to cache. Be sure to include the fields as well as their sizes.
- b) Compute the hit ratio for a program that loops 5 times from locations 9 to 53 in main memory.

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