四川大学期末考试试题（闭卷）

（2018~2019 学年第 2 学期）　　A 卷

课程号：**311039030**　课程名称：**数字逻辑：应用与设计**　任课教师：＿＿＿＿＿＿

适用专业年级：**软件工程 2018 级**　学号：＿＿＿＿＿＿　姓名：＿＿＿＿＿＿

考生承诺

我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

1、 已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；

2、 不带手机进入考场；

3、 考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

考生签名：

题　　号	一(20%)	二(18%)	三(42%)	四(20%)
得　　分				
卷面总分		阅卷时间		

注意事项：1. 请务必将本人所在学院、姓名、学号、任课教师姓名等信息准确填写在试题纸和添卷纸上；
2. 请将答案全部填写在本试题纸上；
3. 考试结束，请将试题纸、添卷纸和草稿纸一并交给监考老师。

评阅教师	得分

一、单项选择题（本大题共 10 小题，每小题 2 分，共 20 分）

提示：在每小题列出的四个备选项中只有一个是符合题目要求的，请将其代码填写在下表中。错选、多选或未选均无分。

1	2	3	4	5	6	7	8	9	10

1. The binary number 1000110101000110111 1 can be written in hexadecimal as

   (a) AD467　(b) 8C46F　(c) 8D46F　(d) AE46F

2. The code that has an odd-parity error is

   (a) 1010111　(b) 1101000　(c) 1001010　(d) 1110111

3. The BCD number for decimal 473 is

   (a) 111011010　(b) 110001110011　(c) 010001110011　(d) 010011110011

4. In a 4-variable Karnaugh map, a 2-variable product term is produced by

   (a) a 2-cell group of 1s　(b) an 8-cell group of 1s

   (c) a 4-cell group of 1s　(d) a 4-cell group of 0s

5. The OR operation can be produced with

   (a) two NAND gates　(b) three NAND gates　(c) one NOR gate　(d) three NOR gates

6. A full-adder is characterized by
   (a) two inputs and two outputs (b) three inputs and two outputs
   (c) two inputs and three outputs (d) two inputs and one output
7. The purpose of the clock input to a flip-flop is to
   (a) clear the device (b) set the device
   (c) always cause the output to change states
   (d) cause the output to assume a state dependent on the controlling inputs.
8. A T flip-flop with T = 1 has a 100 kHz clock input. The Q output is
   (a) constantly HIGH (b) constantly LOW
   (c) a 100 kHz square wave (d) a 50 kHz square wave
9. To enter a byte of data serially into an 8-bit shift register, there must be
   (a) one clock pulse (b) two clock pulses (c) four clock pulses (d) eight clock pulses
10. A modulus-14 counter must have
   (a) 12 flip-flops (b) 3 flip-flops (c) 4 flip-flops (d) synchronous clocking

评阅教师	得分

二、填空题（本大题共 9 空，每空 2 分，共 18 分）。

1. (18pts) Complete the following table of equivalent values. Use binary numbers with a sign bit and 7 bits for the value.

Decimal	Signed Magnitude	2's Complement code	1's Complement code
		10101010	
-64			
	01111111		

评阅教师	得分

三、分析计算题（本大题共 6 小题，共 42 分）。

1. (共 6 分) Convert each pair of decimal numbers to the 2's complement code and implement the operation.

   (a) 56 + (-27)　　(b) (-110) + (-84)

2. (共 6 分) Use only NAND gates to implement the following logic expressions

   (a) X = AB + B'C　　(b)　X=A(B+C')

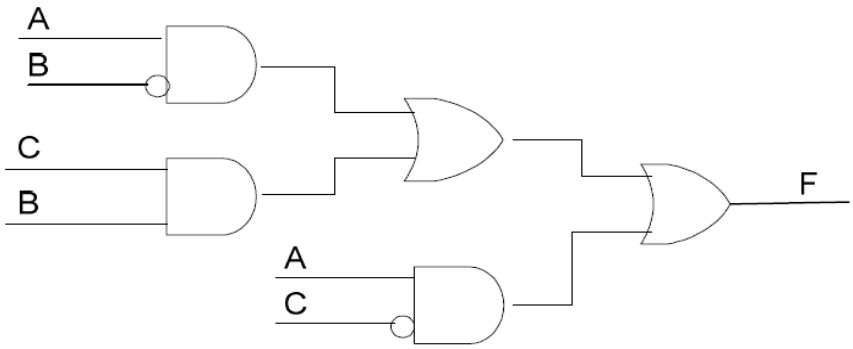
3. (共 15 分)Simplify the following expressions using Karnaugh maps.

   (1) f (A, B, C, D) = ABC'+BC'D'+CD+A'B

   (2) f (A, B, C, D) = ∑m (1,3,7,11,15) +∑d (0,2,5)

   (3) f (W, X, Y, Z) = (X + Y') (W + Z') (X' + Y' + Z') (W + X + Y + Z)

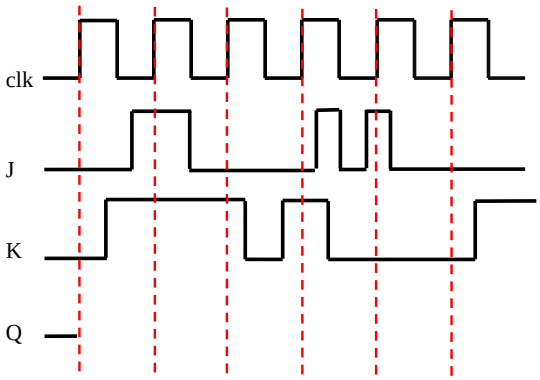
4. (共 5 分) Write the switching expressions for the following logic circuits and Simplify it.



5. (共 5 分) Realize the function shown below using a 4-1 multiplexer and the appropriate logic gates.

   $F(x,y,z) = \Sigma m(3, 4, 6, 7)$

6. (共 5 分) Complete the positive edge triggered JK flip-flop' timing diagram. The initial state of Q equals to 0



评阅教师	得分

四、设计题（本大题共 2 小题，共 20 分）。

1. (共 8 分) Design a comparator has two inputs A = a1a0 and B = b1b0 and output F=f1f0. Output F becomes 00 when A equals to the value of input B, 01 when A is greater than B, and 11 when A is less than B. Using truth table, write out the minimum equations for output f1 and f0, and draw the logic diagram
2. (共12 分) design a three-bit counter that counts in the following sequence: 0, 4, 2, 1, 6, 5, 3, 7, 0, …Find the transition table and the state table for the sequential circuit below. Then implement it with the negative edge triggered JK flip-flops.