四川大学期末考试试题(闭卷)

(2016~2017 学年第 1 学期)

B卷

课程	号: _	311077030 课程名利	r: <u>计算材</u>	几组成和体系	结构	任设	果教师:
适用	专业年	级: 软件工程 2	015 级	学号	:		Ž:
	考生承诺						
我已记	我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定(修订)》,郑重承诺:						
1, 1	已按要求	次将考试禁止携带的文具用品或	或与考试有关的	的物品放置在指	定地点;		
2、 7	下带手机	l进入考场;					
3、 =							
	考生签名:						
题	号	—(30%)	二(40%)	三(1	.8%)	四(12%)
得	分						
阅卷	时间		教师签名		阅卷时间		
; 大辛南西。1 连久必须未上后大兴岭,桥久,兴中,伏阳城市协会举广自华场持军大党和战争。							

- 注意事项:1. 请务必将本人所在学院、姓名、学号、任课教师性名等信息准确填写在试题纸和添卷纸上;
 - 2. 请将答案全部填写在本试题纸上;
 - 3. 考试结束,请将试题纸、添卷纸和草稿纸一并交给监考老师。

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评阅教师	得分	一、简答题(本大题共6小题,每小题5分,共30分)。	
		提示:解释每小题所给名词的含义,若解释正确则给分,若解释错误则无分,若解	释
		不准确或不全面,则酌情扣分。	

1. (共5分) What is RISC and CISC?

2. (共5分) What is pipelining?

注: 试题字迹务必清晰,书写工整。 本题共5页,本页为第1页

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3. (共5分) What is interrupts?

4. (共5分) Explain Indirect Addressing.

5. (共5分) Explain the Spatial locality.

6. (共5分) What is the two types of cache write policies?

注: 试题字迹务必清晰,书写工整。

本题共 5 页,本页为第 2 页

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理程 夕称・	计算机组成和体系结构	任 運粉III:	何军	郭丘	李辉	能住	学是:
沐江五小小	11 异心组从心中不知的	上 木 (大)リー・	ᆘ	オルナヤ	子严	먔 다	子 与 .

ì	照教师 得分 二、填空题(本大题共 20 空,每空 2 分,共 40 分)。
	1. The main components of a von Neumann computer
	is,
2.	The architecture runs programs known as the Von Neumann execution cycle is:, cycle.
3.	A 4M \times 16 main memory required bits to address if it's byte-addressable, and bits to address if it's word-addressable
4.	A 2M \times 16 main memory is built using 256KB \times 8 RAM chips and memory is word-addressable, it requiredRAM chips; the address 14 (dec) would be located bankfor high-order interleaving , and bankfor low-order interleaving counting from 0.
5.	The first two bytes of a 2M x 16 main memory have the following hex values: Byte 0 is FE, Byte 1 is 01, these bytes hold a 16-bit two's complement integer. If the memory is big-endian, its actual decimal value is, if the memory is little-endian, its actual decimal value is
6.	A digital computer has a memory unit with 24 bits per word. The instruction set consists of 150 different operations. All instructions have an operation code part (opcode) and an address part (allowing for only one address). Each instruction is stored in one word of memory. The opcode needed bits, the address part has bits, and the maximum allowable size for memory is
7.	Suppose a computer using direct mapped cache has 2 ²⁰ words of main memory, and a cache of 32 blocks, where each cache block contains 16 words. There areblocks of the main memory, and the format of memory address as bits for tag, bits for block, bits for word fields.
ì	門教师 得分 三、问答题(本大题共3小题,每小题6分,共18分)。

1. (\pm 6 分) Explain the difference between programmed I/O and interrupt-driven I/O.

注: 试题字迹务必清晰,书写工整。 本题共5页,本页为第3页

2. (共6分) Suppose we have the instruction Load 100. Given that memory and register R1 contain the values below:

Memory	<u> </u>	R1	
100	400		200
•••			
200	300		
300	200		
400	100		
•••			
500	600		

Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	Value Loaded into AC
Immediate	
Direct	
Indirect	
Indexed	

3. (\pm 6 分) Define the terms seek time, rotational delay, and transfer time. Explain their relationship.

注: 试题字迹务必清晰,书写工整。 本题共5页,本页为第4页

评阅教师 得分

四、计算题(本大题共1小题,每小题12分,共12分)。

提示: 计算过程中重复性、类似的计算步骤不必全部列出。但若只给出计算结果,则酌情扣分。

- 1. (3 %) Convert the following expressions from reverse Polish notation to infix notation.
- a. WXYZ-+*
- b. UVWXYZ+*+*+
- c. XYZ + VW *Z + +

2. (共9分) Use Huffman algorithm to create Huffman codes for the following rhyme. Use <ws> for whitespace instead of underscores:

GET_THE_WISH_I_WISH_TONIGHT_FIRST_STAR_I_SEE_TONIGHT

注: 试题字迹务必清晰,书写工整。

本题共5页,本页为第5页

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