# 四川大学期末考试试题（闭卷）

## （2018--2019 学年第 1 学期）　　B 卷

课程号：311077030、314056030　课程名称：计算机组成和体系结构　任课教师：＿＿＿＿＿＿

适用专业年级：软件工程 2017 级、网络安全 2017 级　学号：＿＿＿＿＿＿　姓名：＿＿＿＿＿＿

**考生承诺**

我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

1、 已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；

2、 不带手机进入考场；

3、 考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

**考生签名：**

| 题　　号 | 一(40%) | 二(20%) | 三(10%) | 四(30%) |
|---|---|---|---|---|
| 得　　分 | | | | |
| 卷面总分 | | 阅卷时间 | | |

**注意事项：**1. 请务必将本人所在学院、姓名、学号、任课教师姓名等信息准确填写在试题纸和添卷纸上；

2. **请将答案全部填写在本试题纸上；**

3. 考试结束，请将试题纸、添卷纸和草稿纸一并交给监考老师。

| 评阅教师 | 得分 |
|---|---|
| | |

### 一、填空题（本大题共 20 空，每空 2 分，共 40 分）。

1. The main components of a von Neumann computer is ＿＿＿＿＿＿ , ＿＿＿＿＿＿ , ＿＿＿＿＿＿.
2. The architecture runs programs known as the Von Neumann execution cycle is : ＿＿＿＿＿＿, ＿＿＿＿＿＿ , ＿＿＿＿＿＿ cycle
3. Give three different types of buses ＿＿＿＿＿＿, ＿＿＿＿＿＿, ＿＿＿＿＿＿.
4. Flynn’s taxonomy classifies computer architectures based on two properties. They are ＿＿＿＿＿＿, ＿＿＿＿＿＿.
5. Cache is accessed by its ＿＿＿＿＿＿ , whereas main memory is accessed by its ＿＿＿＿＿＿.
6. List 5 addressing mode ＿＿＿＿＿＿, ＿＿＿＿＿＿, ＿＿＿＿＿＿, ＿＿＿＿＿＿, ＿＿＿＿＿＿
7. A 8M × 16 main memory required ＿＿＿＿＿＿ bits to address if it’s byte-addressable, and ＿＿＿＿＿＿bits to address if it’s word-addressable.

| 评阅教师 | 得分 |
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## 二、判断题（本大题共 10 小题，每小题 2 分，共 20 分）

**提示：**正确打✓，错误打×，将其结果填写在下表中。

| 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|
| | | | | |
| **6** | **7** | **8** | **9** | **10** |
| | | | | |

1．If the bus clock rate is 100MHz, then the length of the bus cycle is 10ns.

2．Asynchronous can support a wider variety of devices since it use a protocol to coordinate transaction..

3．In memory，each individual byte has a unique address.

4. The ALU portion of the CPU performs all of the processing ，such as arithmetic operations, logic decisions, and so on.

5．All computers follow a basic machine cycle: the fetch, decode, and execute cycle.

6. When you type a Ctrl-C to stop a program, there is an interrupt set.

7. Most architectures today are accumulator based.

8. SRAM is faster than DRAM.

9. A register is a hardware device that stores binary data, such as addresses, program counters, or data necessary for program execution.

10. L1 cache is faster than L2 cache.

| 评阅教师 | 得分 |
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## 三、问答题（本大题共 2 小题，每小题 5 分，共 10 分）。

1．（共 5 分）Describe programmed I/O， interrupt-driven I/O，Direct Memory Access And Channel I/O.

2.（共 5 分）Explain RAID-0,. RAID-1, RAID-3, RAID-5.

| 评阅教师 | 得分 |
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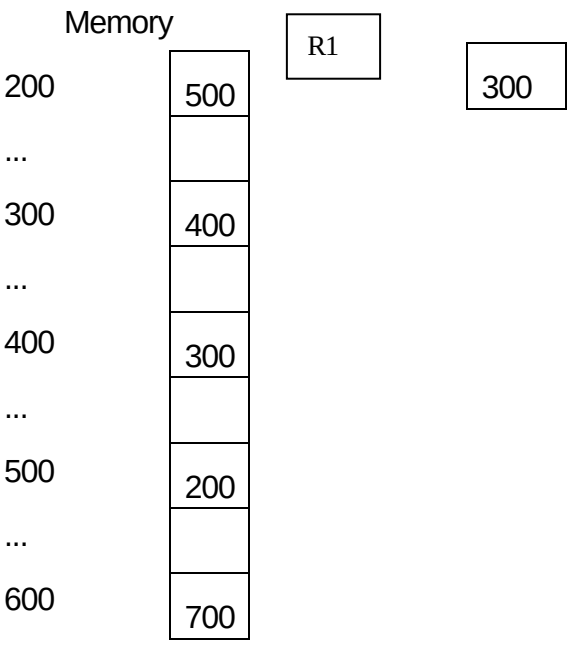
| | |

**四、计算题（本大题共 5 小题，共 30 分）。**

**提示：**计算过程中重复性、类似的计算步骤不必全部列出。但若只给出计算结果，则酌情扣分。

1.（共 8 分）Suppose we have the instruction Load 200. Given that memory and register R1 contain the values below:




Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

| Mode | Value Loaded into AC |
|---|---|
| Immediate | |
| Direct | |
| Indirect | |
| Indexed | |

2.（6 分）Convert the following expressions from reverse Polish notation to infix notation.

a. T X Y P - + *

b. EG T X Y P + * + * +

3. (6 分)Suppose a computer using direct mapped cache has $2^{32}$ words of main memory, and a cache of 1024 blocks, where each cache block contains 32 words.

a. How many blocks of main memory are there?

b. What is the format of a memory address as seen by the cache, i.e., what are the sizes of

the tag, block, and word fields?

4.（共 6 分）A nonpipelined system takes 100ns to process a task. The same task can be processed in a 5-segment pipeline with a clock cycle of 20ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the theoretical speedup that could be achieved with the pipeline system over a nonpipelined system?

5.（共 4 分）A 2-way set-associative cache consists of four sets. Main memory contains 2K blocks of eight words each. Show the main memory address format that allows us to map addresses from main memory to cache. Be sure to include the fields as well as their sizes.