四川大学期末考试试题（闭卷）

（2017~2018 学年第 2 学期）　　B 卷

课程号：**311039030** 课程名称：**数字逻辑：应用与设计** 任课教师：＿＿＿＿＿＿

适用专业年级：**软件工程 2017 级** 学号：＿＿＿＿＿＿ 姓名：＿＿＿＿＿＿

考生承诺

我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

1、已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；

2、不带手机进入考场；

3、考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

考生签名：

题　　号	一(20%)	二(18%)	三(42%)	四(10%)
得　　分				
卷面总分		阅卷时间		

注意事项：1. 请务必将本人所在学院、姓名、学号、任课教师姓名等信息准确填写在试题纸和添卷纸上；

2. **请将答案全部填写在本试题纸上；**

3. 考试结束，请将试题纸、添卷纸和草稿纸一并交给监考老师。

评阅教师	得分

一、单项选择题（本大题共 10 小题，每小题 2 分，共 20 分）

提示：在每小题列出的四个备选项中只有一个是符合题目要求的，请将其代码填写在下表中。错选、多选或未选均无分。

1	2	3	4	5	6	7	8	9	10

1. Which odd-parity code is in correct?

(a) 11111111 (b) 00000000 (c) 10101010 (d) 10101011

2. The number 1001 in BCD is

(a). equal to decimal eight (b). equal to decimal ten (c). equal to decimal nine (d). invalid

3. According to DeMorgan's theorems, the complement of a product of variables is equal to

(a) the complement of the sum (b) the sum of the complements

(c) the product of the complements (d) answers (a), (b), and (c)

4. A pulse in a certain waveform has a frequency of 100 Hz. It repeats itself every

(a) 1 ms (b) 20 ms (c) 50 ms (d) 10 ms

5. All Boolean expressions can be implemented with

(a) NAND gates only　　(b) NOR gates only

(c) combinations of NAND and NOR gates

(d) combinations of AND gates, OR gates, and inverters

(e) any of these

6. Which of the following is not true for an active LOW input S'-R' latch?

(a) S' = 1, R' = 1, Q = NC, Q' = NC　　(b) S' = 0, R' = 1, Q = 1, Q' = 0

(c) S = 1', R' = 0, Q = 1, Q' = 0　　(d) S' = 0, R' = 0, Q = 1, Q' = 1

7. A J-K flip-flop with J = 1 and K = 1 has a 10 kHz clock input. The Q output is

(a) constantly HIGH　　(b) constantly LOW

(c) a 10 kHz square wave　　(d) a 5 kHz square wave

8. The output of a Mealy machine depends on its

(a) inputs　(b) next state　　(c) present state　　(d) answers (a) and (c)

9. An exclusive-OR(XOR) function is expressed as

(a) A'B' + AB　(b) A'B + AB'　(c) (A' + B)(A + B')　(d) (A' + B')(A + B)

10. A JK flip-flop is Hold when

(a) J = 0, K = 0　(b) J = 0, K = 1　(c) J = 1, K = 0　(d) J = 1, K = 1

评阅教师	得分

二、填空题（本大题共 9 空，每空 2 分，共 18 分）。

1. (18pts) Complete the following table of equivalent values. Use binary numbers with a sign bit and 7 bits for the value.

Decimal	Signed Magnitude	2's Complement code	1's Complement code
			01110111
63			
	01111111		

评阅教师	得分

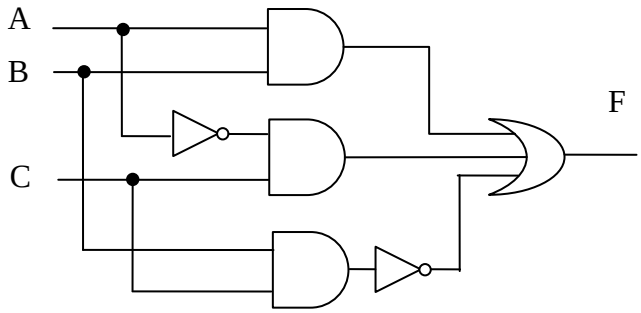
三、分析计算题（本大题共 6 小题，共 42 分）。

1. (共 5 分) Reduce the following using the Boolean algebra rules and draw the logic diagram using only NAND gates:
   F = (AB+C')'+AC'+B

2. (共 6 分) Implement the basic logic gates (AND, OR, NOT) only by the NOR gates respectively.

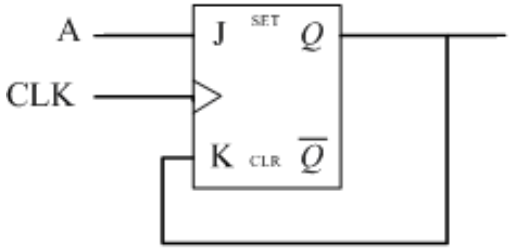
3. (共 15 分)Simplify the following expressions using Karnaugh maps.
   a: f(A,B,C)= A(B + C')(A' + C)(A + B '+ C)(A + B + C')
   b: f(w,x,y,z)=∑(0,3,4,7,8)+∑d(10,11,12,13,14,15)
   c: f(A,B,C,D) = (A' B' + AB')(CD + CD')

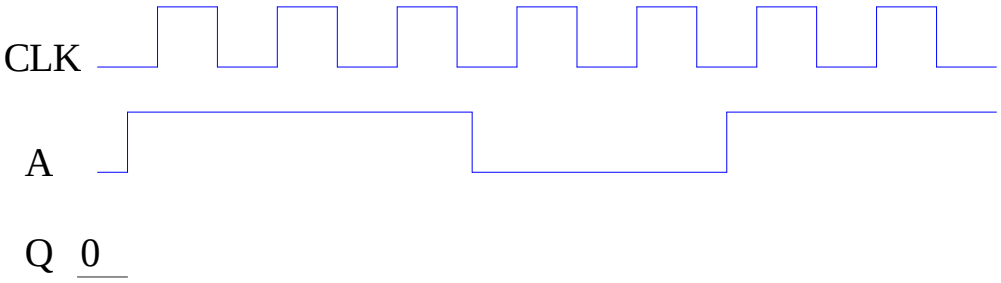
4. (共 6 分) Write the switching expressions for the following logic circuits and Simplify it.



5. (共 5 分) Implement **F(a,b,c) =Σ (1,2,6,7)** using a 4-to-1multiplexer

6. (共 5 分) Given the positive edge triggered J-K flip-flop shown below, complete the timing diagram in the figure





评阅教师	得分

四、设计题（本大题共 2 小题，共 20 分）。

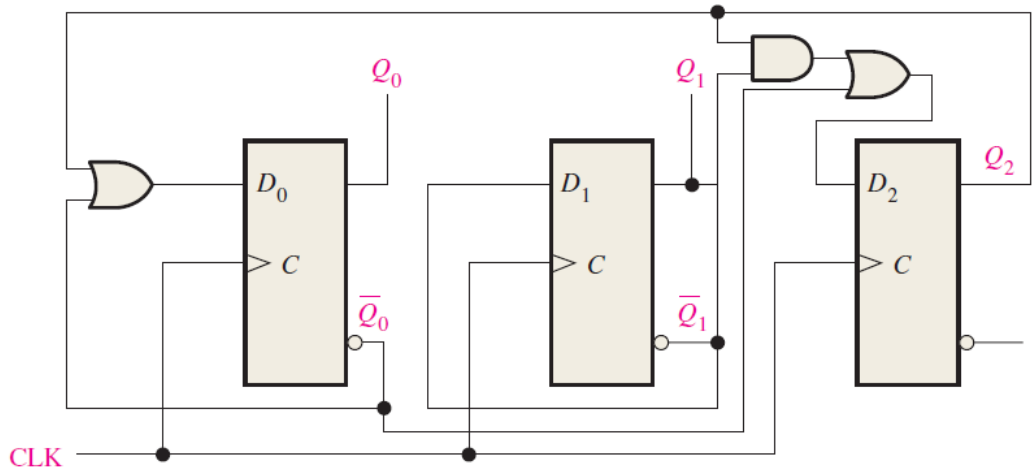
1. (共 8 分) 1. Consider the following three-variable function:

f(a,b,c) = c'+ab'+abc

(a) Give its canonical SOP and canonical POS.(4 points)

(b) Implement the function using more than two methods (draw out the logic diagram). (4 points)

2. (共12分) Given the sequential circuit below



(a) Construct the State Transition Table
(b) Draw the State Diagram from the State Transition Table