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CMOS ICs \rightarrow 4 credit
2



Complementary metal Oxide Silicon.

⇒ Sung Mo Kang Yusuf Leblebiyi
cmos digital IC analysis and design, Second edition,
Morgan Hill 1999

• Moore's law

1965 \rightarrow No of transistors must be doubled by 2 years on a single chip area.

• Revised 1970 \rightarrow no. of transistors must be doubled by eighteen months.

$$\begin{array}{c} W \\ | \\ \text{---} \\ | \\ L \end{array} \Rightarrow W' = \frac{W}{\sqrt{2}} \quad \begin{array}{c} L \\ | \\ \text{---} \\ | \\ \sqrt{2} \end{array}$$
$$A = WL$$
$$A' = \frac{A}{\sqrt{2}}$$

• Technology node \rightarrow now a day 7nm is Technology node (2022)

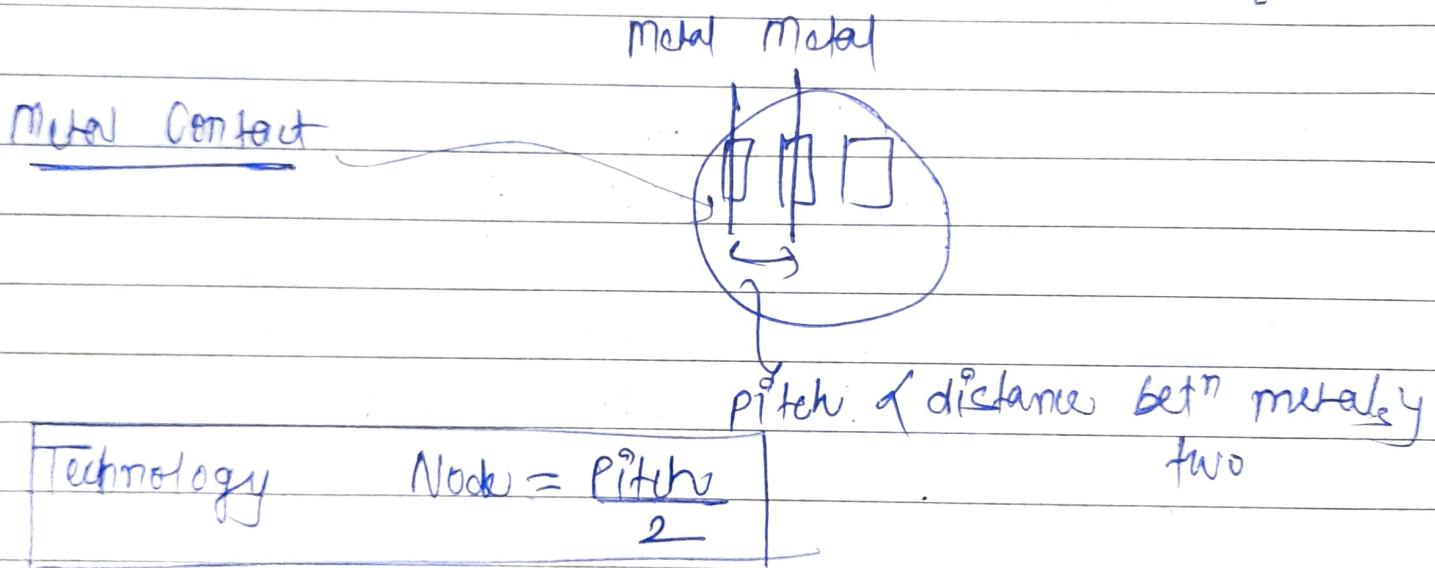
45nm \rightarrow 2DLS

gives reduction in dimension on single and one one
45nm x 0.707

Can accommodate large no. of devices.

$$\begin{aligned} 10\text{mm} &\rightarrow 7\text{mm} \\ 10(1-0.7) &= 10 \times 0.7 = 7\text{mm} \\ 7\text{mm} \times 0.707 &= 5\text{mm} \\ \hline & \frac{1}{\sqrt{2}} \\ & 4949 \end{aligned}$$

→ On a single chip we can fabricate multiple devices



→ CMOS

Bipolar of BJT

- Low power dissipation
- Complex fabrication steps.
- High packing density
- High power transmission
- Low packing density
- Few fabrication steps

(large no. of Capacitance)

- low speed

$$T = R_C$$

(less num of Capacitance)

High speed

- High input impedance

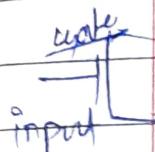
of leakage curr. lowly

low drive current

low input impedance

of base current highly

High drive current



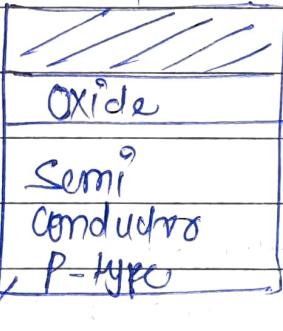
MOS \rightarrow Metal Oxide Semiconductor

- Oxide material



$$\text{dielectric} = 3.9$$

Metal



Capacitor

Na nMOS
Acceptor impurity and there

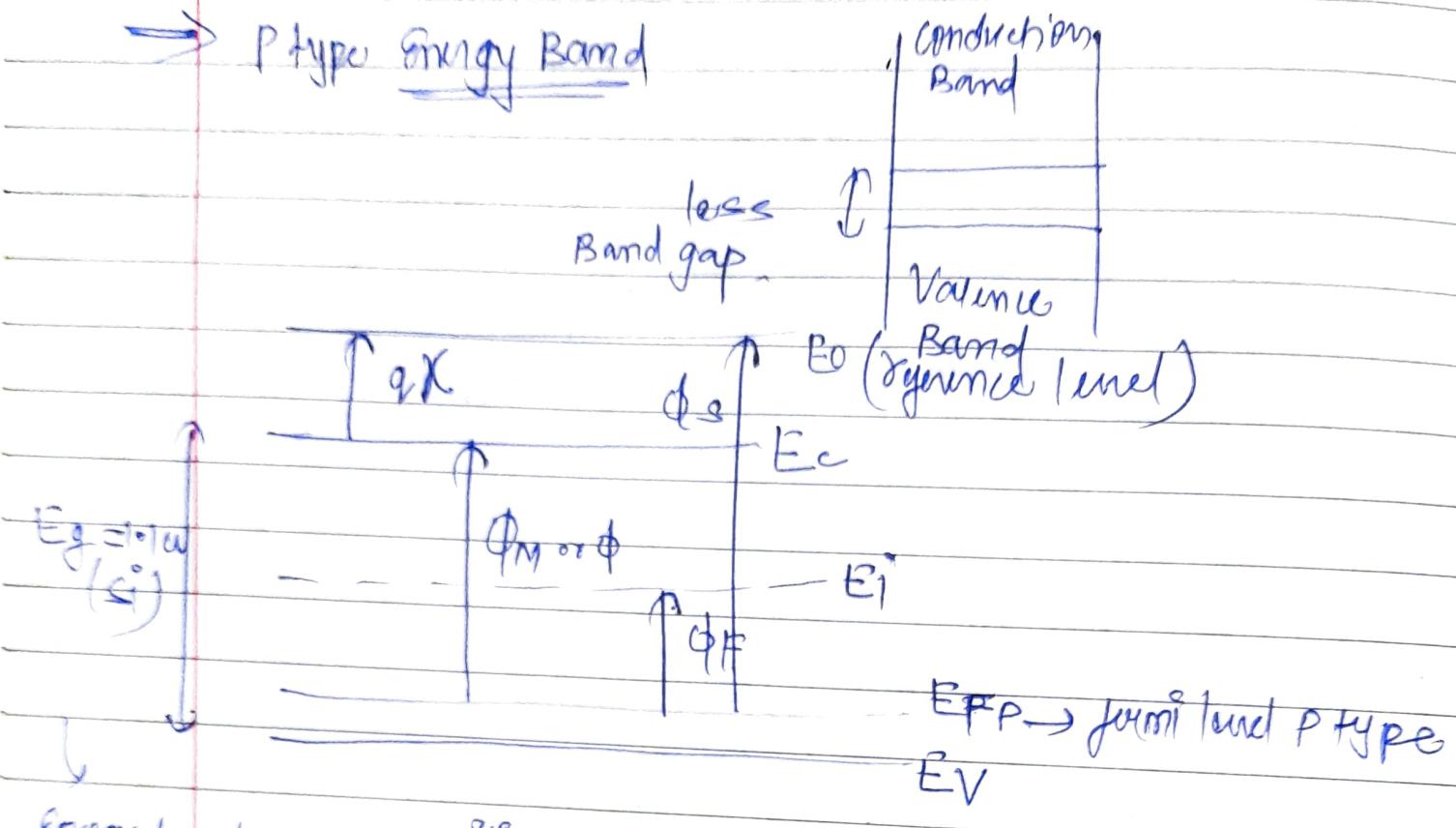
$P_p \approx N_A$
holes & majority carriers

$$n_p = \frac{n_i^2}{N_A}$$

Intrinsic Concentration

$$n_i = 1.5 \times 10^{10} \text{ m}^{-3} (\text{Si}) \rightarrow \underline{\text{Remember}}$$

\Rightarrow P type Energy Band



Energy band gap for Silicon.

χ = electron affinity
 (amount of energy required to move an electron from conduction band to reference level)

$\Rightarrow \phi \rightarrow$ Work function

Fermi potential

$$\phi_F = E_F - E_i$$

P-type $\rightarrow \phi_F$ is negative
 n-type $\rightarrow \phi_F$ is positive

$$\phi_{FP} = \frac{kT}{q} \ln \left(\frac{n_i}{N_A} \right), \text{ P-type}$$

$$\phi_{Fn} = \frac{kT}{q} \ln \left(\frac{N_D}{n_i} \right), \text{ n-type}$$

$$V_T \text{ (thermal voltage)} = 96 \text{ mV } \text{ if } T = 300 \text{ K}$$

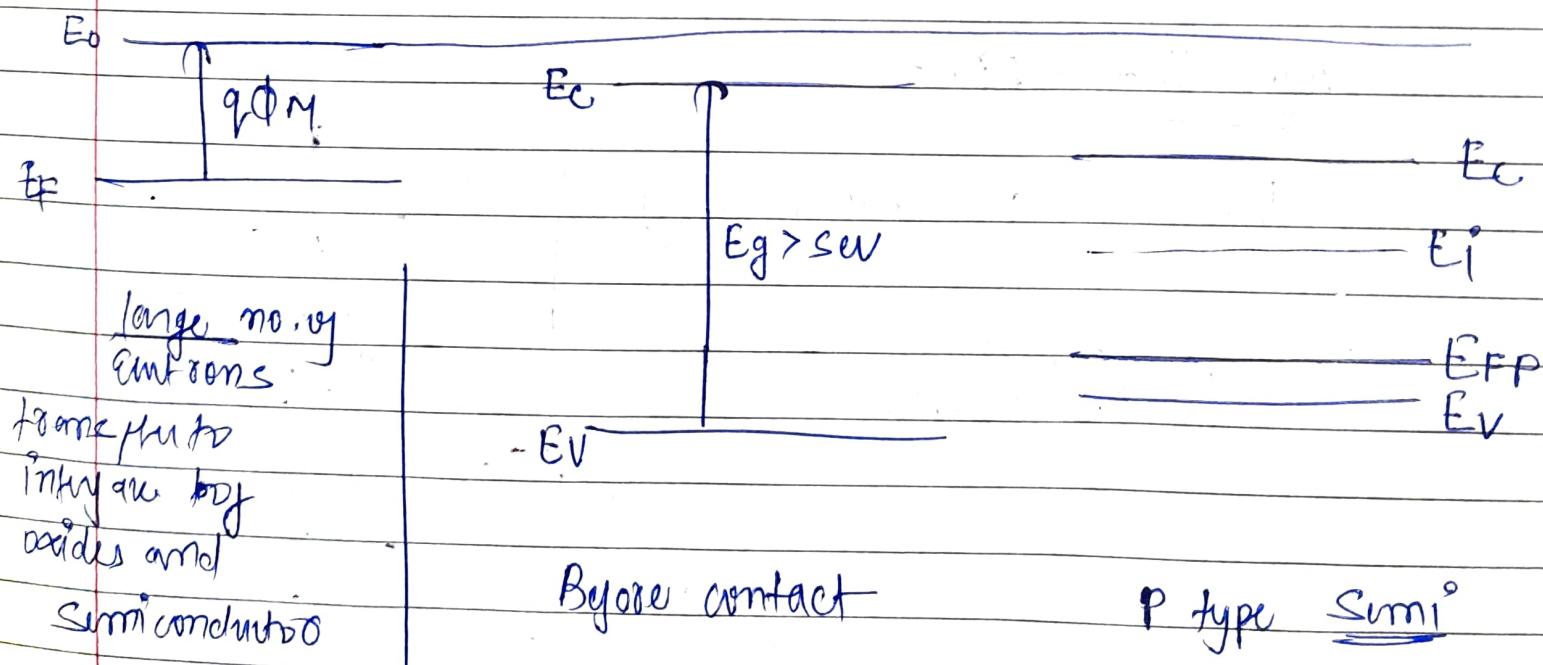
amt. of energy req to move electron from
 $\Rightarrow \phi_s$ of Fermi level to reference level

$$\boxed{\phi_s = q\chi + (E_C - E_F)}$$

Metal

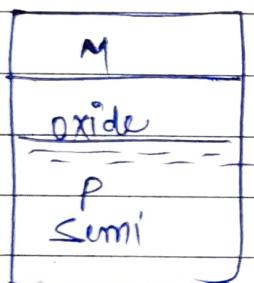
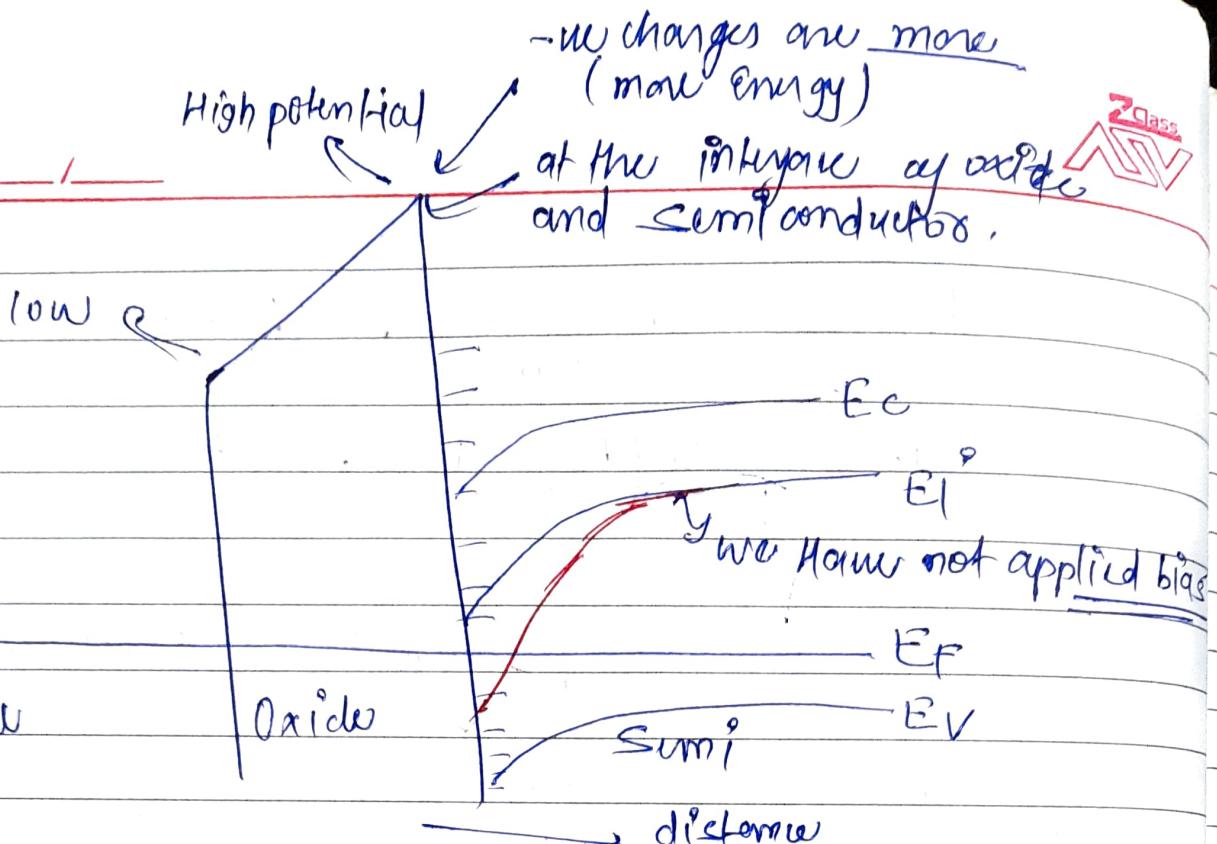
Oxide

Semiconductor



Electrons are more
they have more
energy

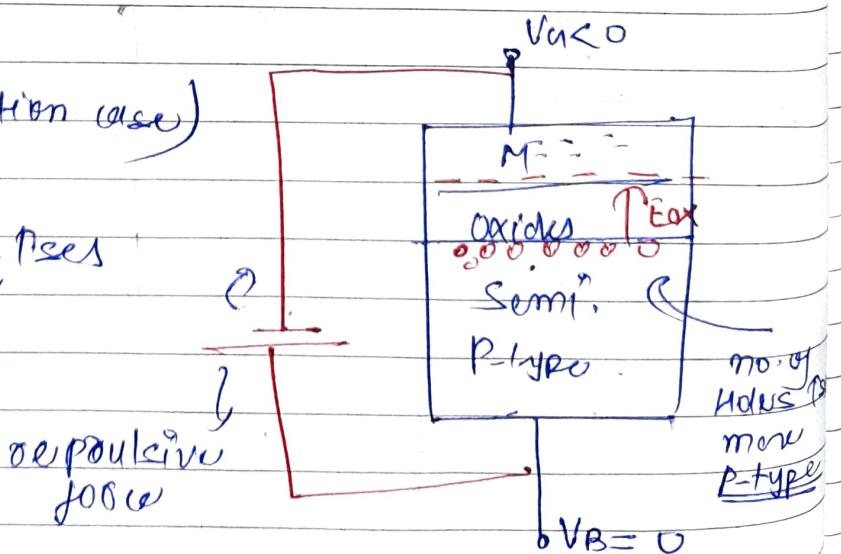
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for injection we apply
copper wires
proper bias

MOS Under Bias

- $V_M < 0$ (accumulation case)

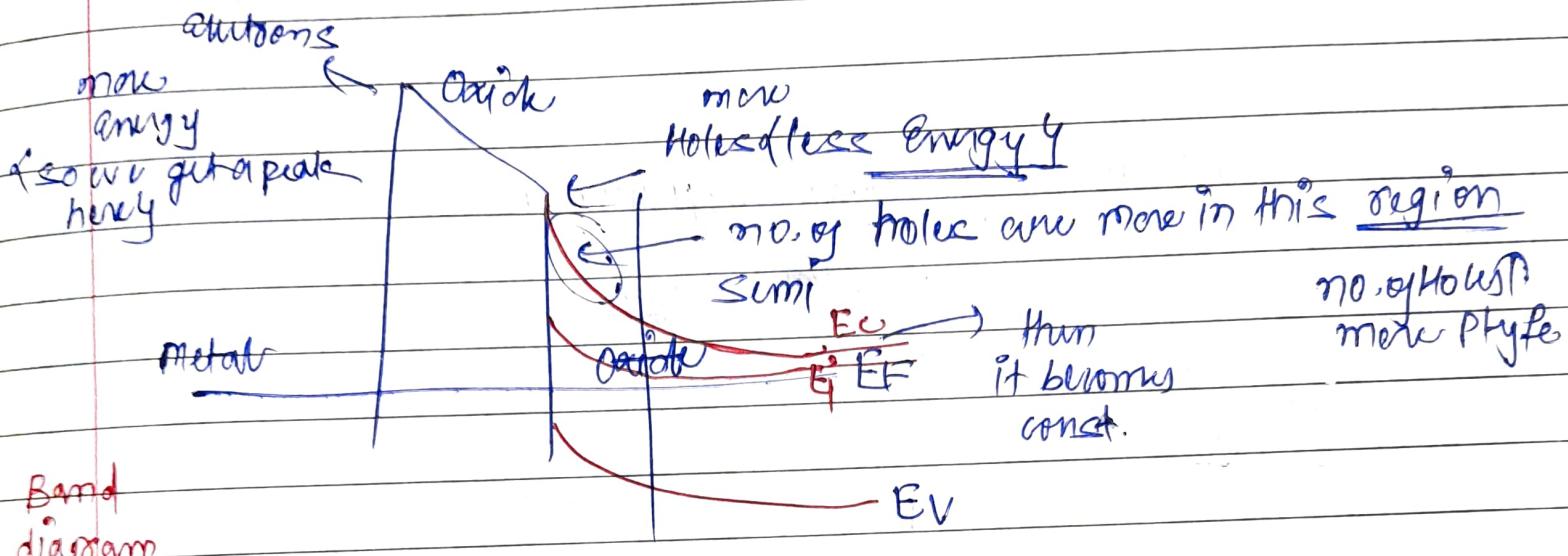


- Holes are accumulated at oxide (SO) interface.

- We have equal number of +ve & -ve charges on

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Oxide / SO interface. due to which electric field from downward to upward dirⁿ.



- $V_{bi} > 0$ (small)

0.34

or

0.44

depletion mode

→ acceptor lone pair created at the interface of Oxide and semi conductor.

- $\psi_b \rightarrow$ Singing potential.

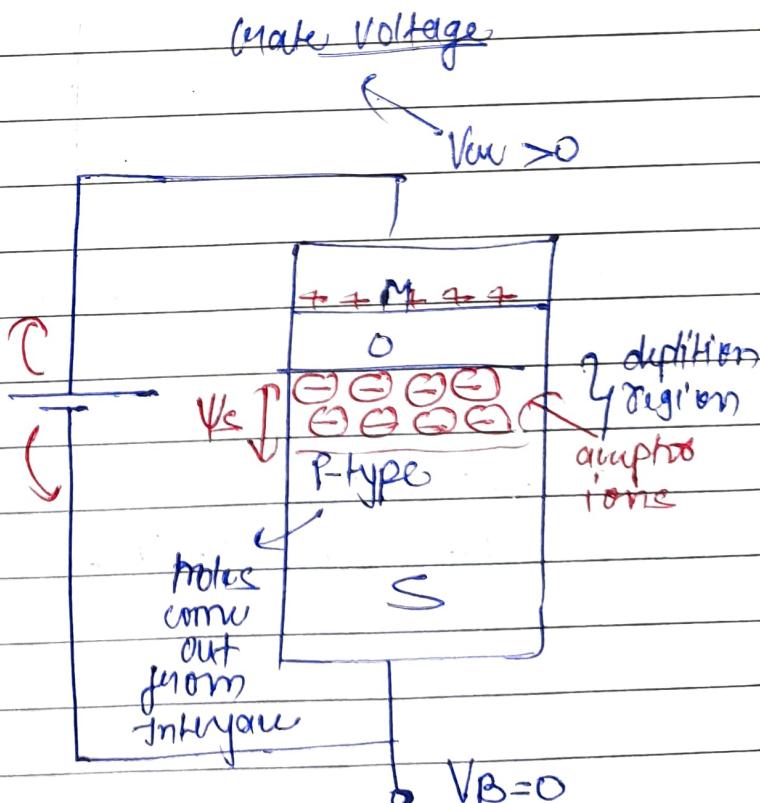
- $N_d \rightarrow$ thickness of depletion region

$$N_d = \sqrt{\frac{q\epsilon_s(\psi_b - \phi_f)}{qN_A}} \rightarrow \text{fermi potential}$$

permeability
of Silicon

charge

acceptor
lon.



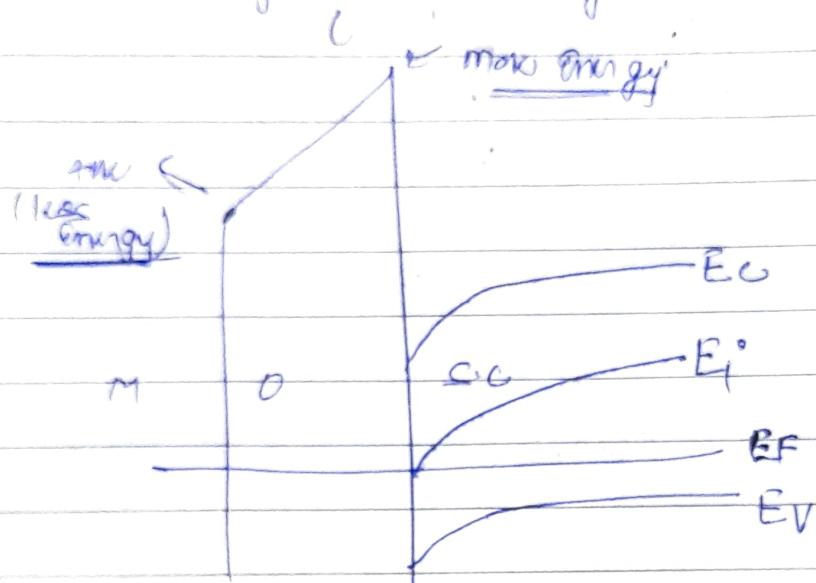
charge in
dipole moment
region

$$Q = -\nabla N_A \chi_d$$

$$\approx -\sqrt{qN_A\epsilon} (\Psi_s - \Phi_F)$$

electrostatic charge

Band diagram under depletion mode



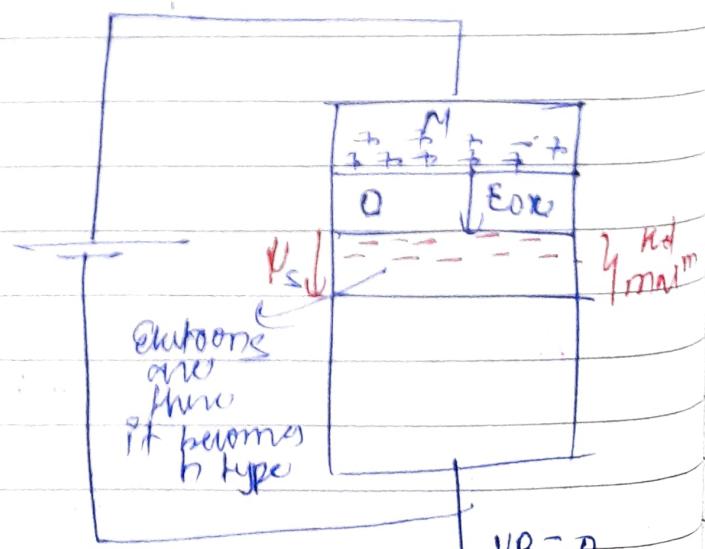
→ there are low power diode

Enhancement type mosfet

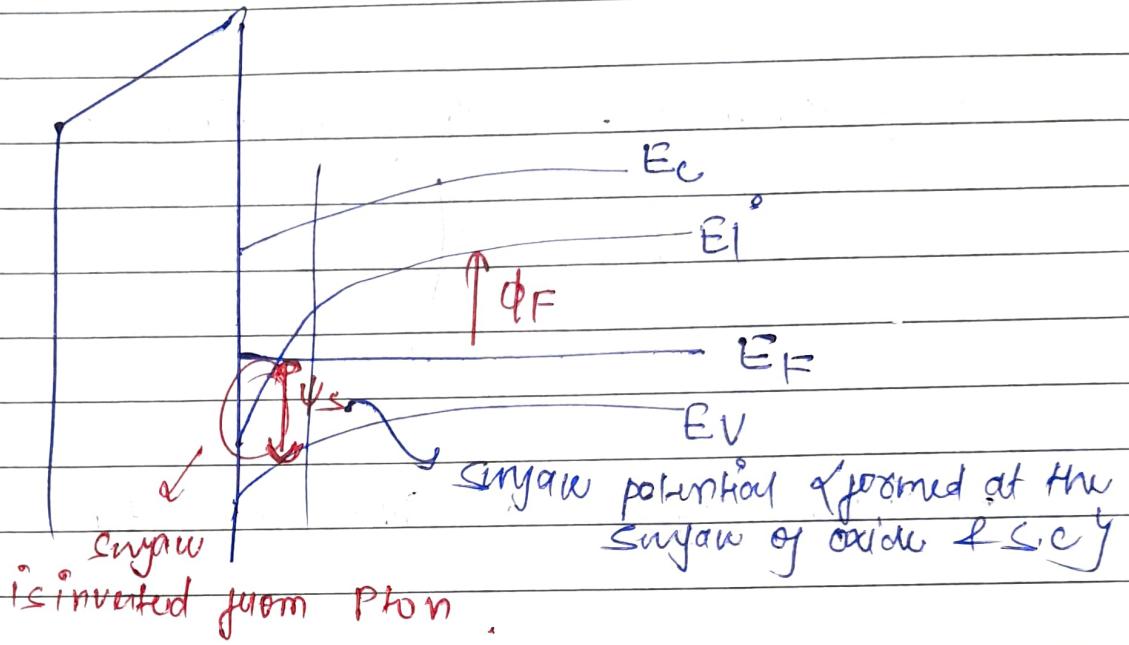
- $V_{ds} > 0$ (High)

~~IG~~
~~IG~~ Insulation Mode

$V_D > 0$



→ Equal number of



E_I° goes down to E_F sinjaw is inverted from Pton.

→ In n-type of Fermi level below conduction band by

→ at Inversion

$\chi_{d\max}$ will be maximum

$$\boxed{\psi_S = -\phi_F}$$

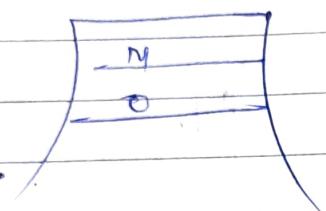
$$\chi_{d\max} = \sqrt{\frac{2E_S i^\circ}{qN_A} [2\phi_F]}$$

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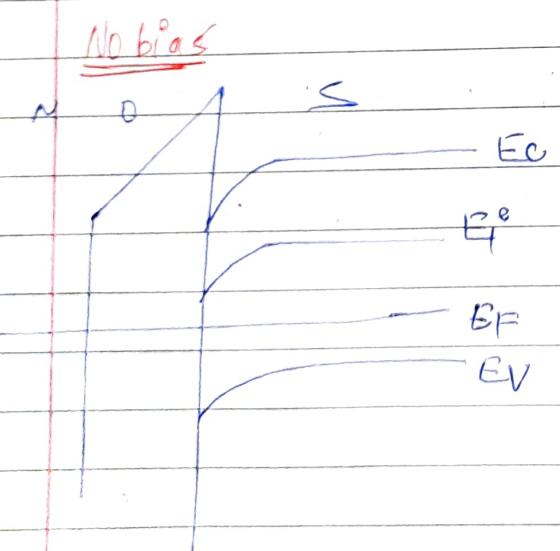
→ Enhancement mode MOSFET

create channel.

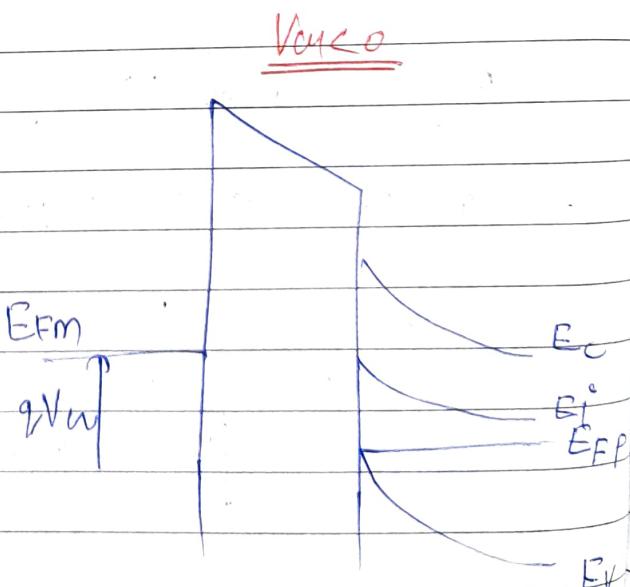
→ depletion mode → always on of wastage of power



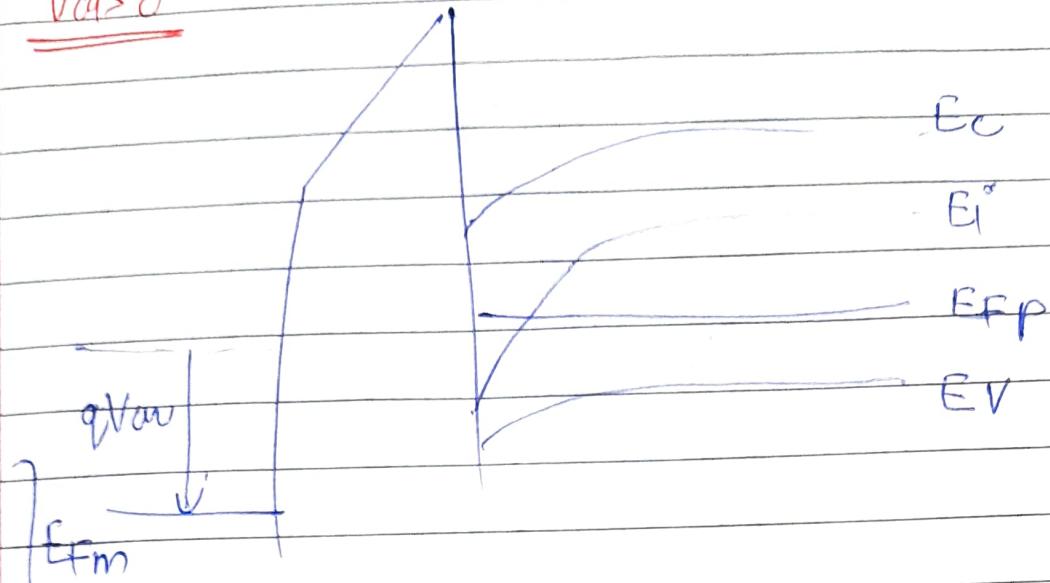
→ now a days we use enhancement type.



Moving electron goes
and fixed in



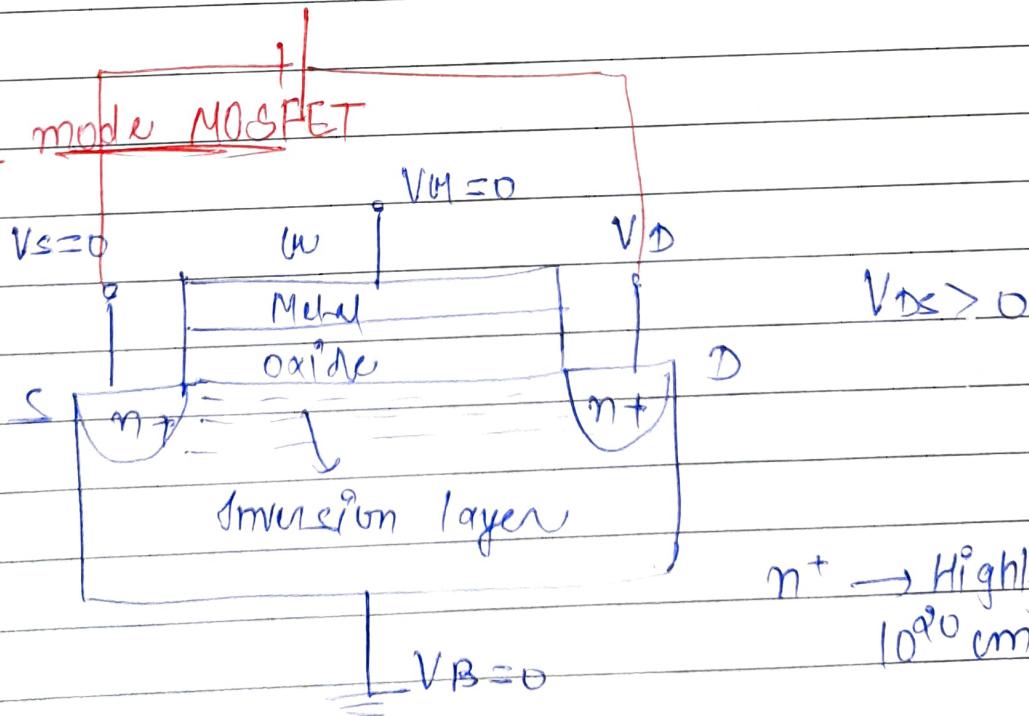
Or one Pses & o,
qVds Pses

$V_{GS} > 0$ 

\rightarrow If $V_{GS} > 0$ no. of free charges Reels in the metal \oplus
 Wilson \downarrow see of qV_{GS} goes down with respect to V_{GS} .

$C \downarrow$

• Enhancement mode MOSFET



S → Source

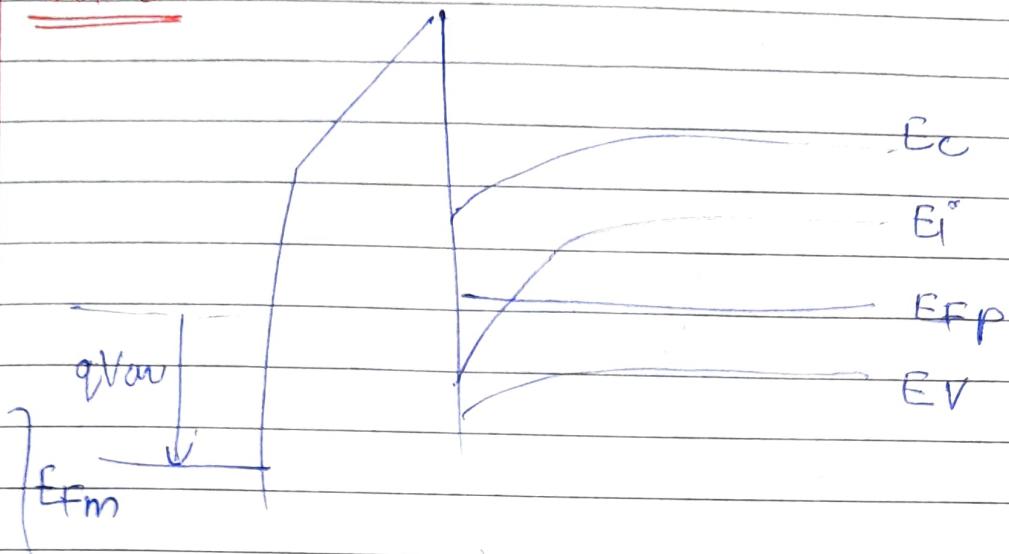
D → drain

G → Gate

B → Body

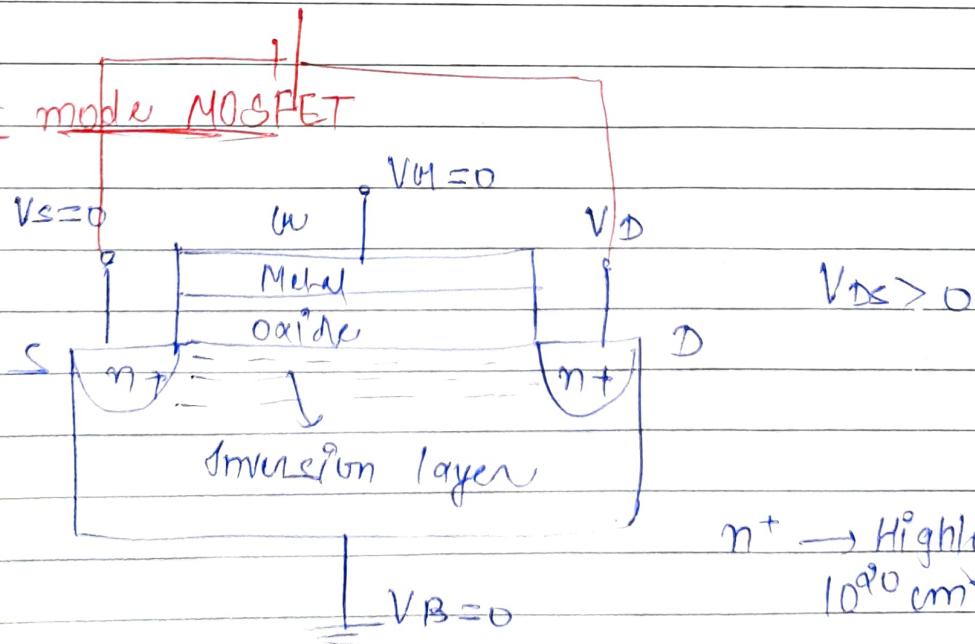
Tone flow from D → S

$n^+ \rightarrow$ Highly doped
 10^{20} cm^{-3}

$V_{ds} > 0$ 

\rightarrow If $V_{ds} > 0$ no. of free charges decreases in the metal \Rightarrow
 Number of qV_{ds} goes down with respect to V_{ds} .

Enhancement mode MOSFET



$n^+ \rightarrow$ Highly doped
 10^{19} cm^{-3}

S → Source

D → drain

G → Gate

B → Body

Tone flow from D → S

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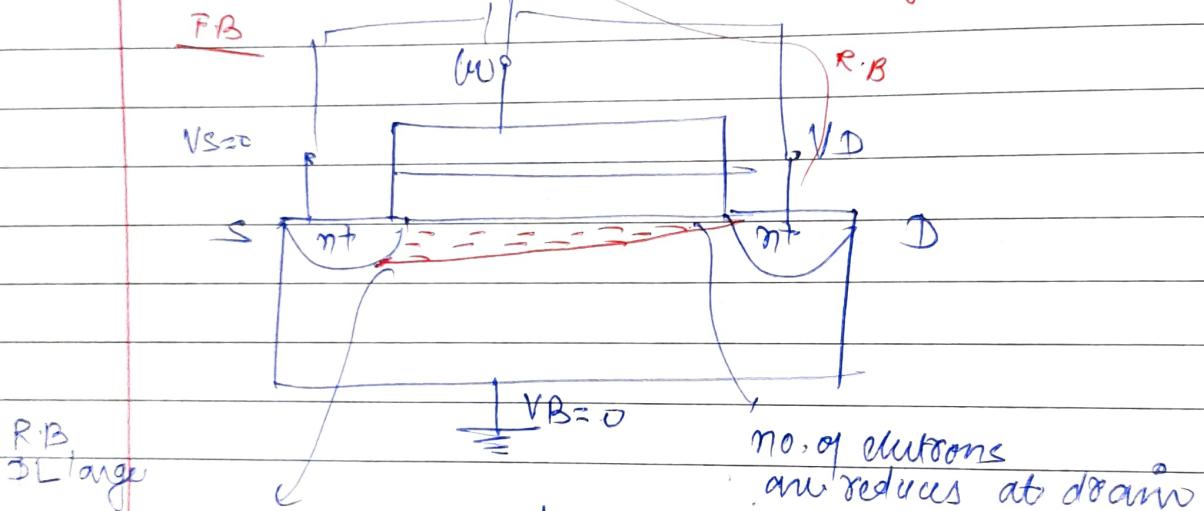
amount of voltage required to
invert channel from P → n

- * $V_{DS} < V_t$ (threshold voltage)
No current will flow, Cut off mode

- * $V_{DS} > V_t$

$$V_{DS} < V_{GS} - V_t$$

- + Ovverdrive Voltage



This is like forward biased so no. of electrons are fed F.B.

$V_{DS} > 0$ slightly greatly due to R_B at drain is large so electrons are reducing

 I_D

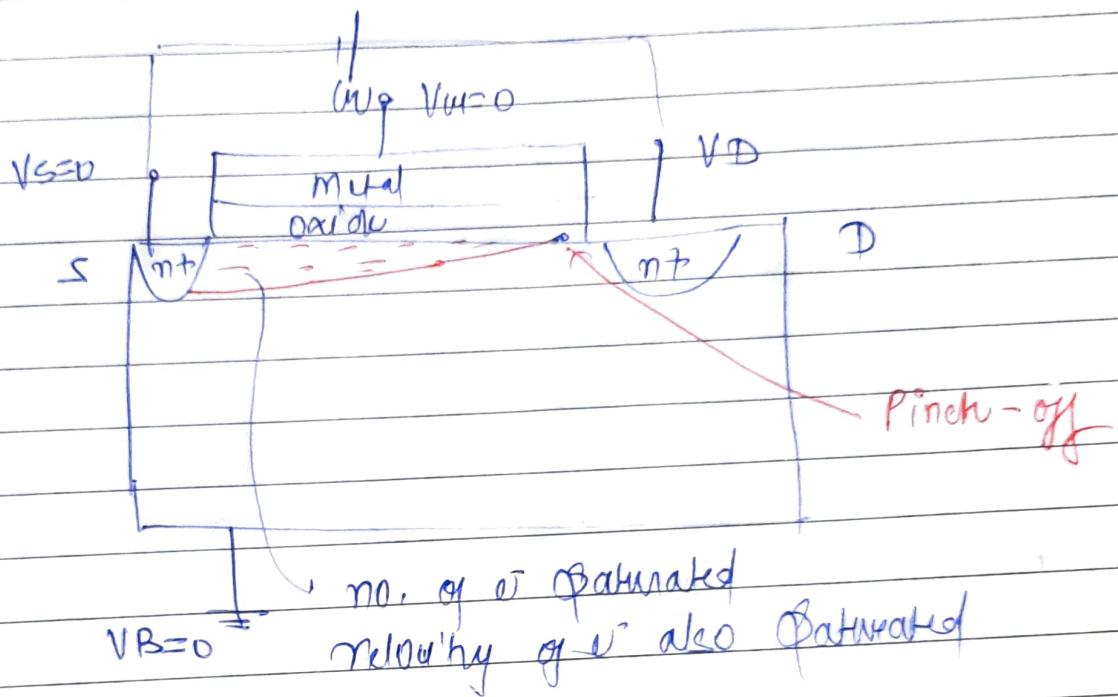
Non linear / Saturation region

$\rightarrow V_{DS}$

$$V_{GMS} > V_G$$

$$V_{DS} \geq V_{GS} - V_t$$

Saturation Region.



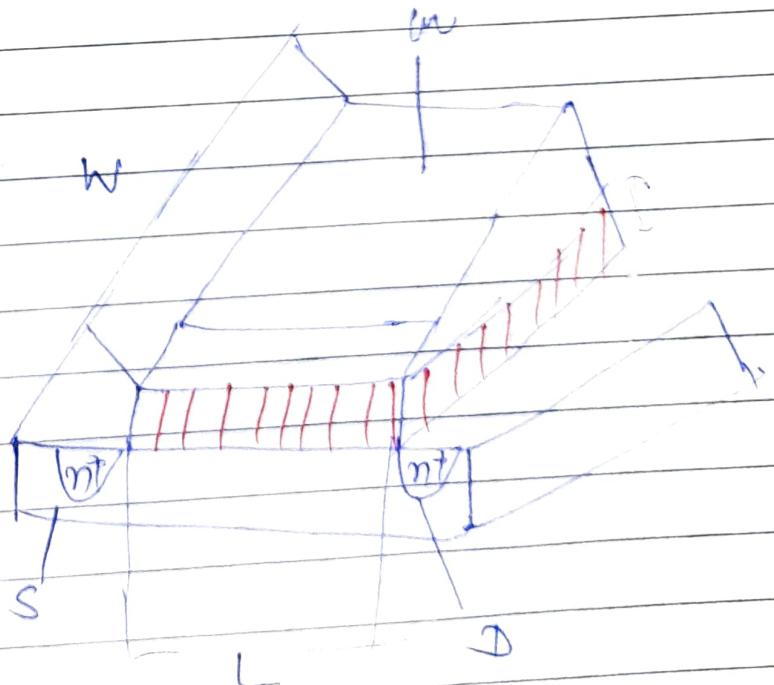
I_D vs V_{DS}

$L \rightarrow$ length

$W \rightarrow$ width

$t_{ox} \rightarrow$ Oxide thickness

I_{DS} is a function of
 V_{DS} and V_{GMS}



$$T_{DS} = \frac{\text{channel charge } Q_C}{\text{transit time } T} \quad \text{--- (1)}$$

$$T = \frac{\text{channel length}}{\text{velocity}} = \frac{L}{V}$$

$$V = \mu E_{DS} \quad \boxed{E_{DS} = \frac{V_{DS}}{L}}$$

$$= \mu \frac{V_{DS}}{L}$$

$$T = \frac{L^2}{\mu V_{DS}} \rightarrow (2)$$

The non-saturated current

Assume that channel is non-saturated at $\frac{V_{DS}}{2}$, $V_g = V_{DS} - V_t$

$$\text{charge carrier} = E_g \epsilon_{ins} \epsilon_0 \quad \checkmark \text{Insulated}$$

$$\text{charge, } Q_C = E_g \epsilon_{ins} \epsilon_0 W L$$

E_g = average electric field gets to channel
 $\epsilon_0 = 8.854 \times 10^{-14} \text{ F/lm}$ $\epsilon_{ins} = 3 \text{ a.g}$

$$E_g = (V_{GS} - V_t) - \frac{V_{DS}}{2}$$

$$Q_C = \frac{WL\epsilon_{ins}\epsilon_0}{t_{ox}} \left((V_{GS} - V_t) - \frac{V_{DS}}{2} \right) \rightarrow (3)$$

(2) + (3) in (1)

$$I_{DS} = \frac{\text{channel charge } (\theta_c)}{\text{transit time } (T)} \quad \rightarrow \textcircled{1}$$

$$T = \frac{\text{channel length}}{\text{velocity}} = \frac{L}{V}$$

$$V = \mu E_{ds}$$

$$\boxed{E_{ds} = \frac{V_{ds}}{L}}$$

$$\therefore \underline{\underline{\mu V_{ds}}}$$

$$T = \frac{L^2}{\mu V_{ds}} \rightarrow \textcircled{2}$$

The non-saturated current

assume that channel is non-saturated at $\frac{V_{ds}}{2}$, $V_g = V_{ds} - V_t$

$$\text{charge / area} = E_g \epsilon_{ins} \epsilon_0$$

↑ insulated

$$\text{charge, } \theta_c = E_g \epsilon_{ins} \epsilon_0 W L$$

E_g = average electric field gets to channel
 $\epsilon_0 = 8.854 \times 10^{-14} \text{ F/Um}$ $\epsilon_{ins} = \underline{\underline{3 \text{ a.u.}}}$

$$E_g = (V_{gs} - V_t) - \frac{V_{ds}}{2}$$

t_{ox}

$$\theta_c = \frac{W L \epsilon_{ins} \epsilon_0}{t_{ox}} \left((V_{gs} - V_t) - \frac{V_{ds}}{2} \right) \rightarrow \textcircled{3}$$

(2) + (3) in (1)

$$\begin{aligned}
 I_{D.S} &= \frac{W L \epsilon_{in} \epsilon_0}{T_{ox}} \left((V_{gs} - V_t) - \frac{V_{ds}}{2} \right) \times \frac{V_{ds}}{L^2} \\
 &= \frac{\epsilon_0 \epsilon_{in} \mu}{T_{ox}} \frac{W}{L} \left((V_{gs} - V_t) - \frac{V_{ds}}{2} \right) \times V_{ds} \\
 &= k_m \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] \\
 &= \beta \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]
 \end{aligned}$$

$$k = \frac{\epsilon_0 \epsilon_{in} \mu}{T_{ox}}$$

$C_g = \frac{\epsilon_{in} \epsilon_0 W L}{T_{ox}}$

gate capacitance

$$K = \frac{C_g \mu}{WL}$$

$$I_{D.S} = \frac{C_g \mu}{L^2} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

\Rightarrow Pathway Current

$$V_{ds} = V_{gs} - V_t$$

$$I_{D.S} = K \frac{W}{L} \left(\frac{(V_{gs} - V_t)^2}{2} \right)$$

$$= \frac{\beta}{2} (V_{gs} - V_t)^2$$

\rightarrow These current are dimension in long channel devices \rightarrow μm range

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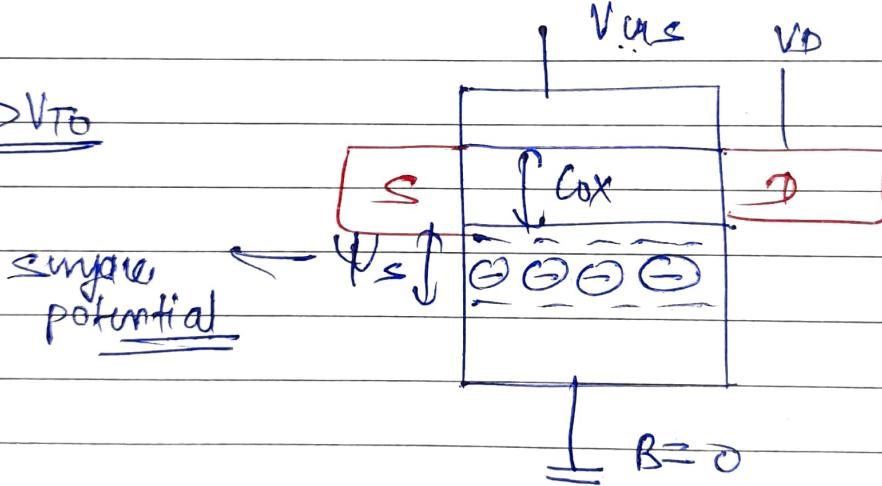
Threshold voltage (V_{TO}) \rightarrow the voltage required to cause surface inversion is called threshold voltage (V_{TO}).

$$V_{TO} = \psi_s - 2\phi_F - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{ox}}{C_{OX}}$$

$$C_{OX} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$Q_{BO} = -\sqrt{2qN_A\epsilon_{ci}|\psi_s - 2\phi_F|}$$

$$\underline{V_{AS} > V_{TO}}$$



Body effect

$$V_T = V_{TO} - \left(\frac{Q_B - Q_{BO}}{C_{OX}} \right)$$

$$= V_{TO} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$$

$$\gamma = \frac{2qN_A\epsilon_{ci}}{C_{OX}}, \text{body effect coefficient}$$

potential diff betn
source & the
body.

Transconductance (g_m)

$$g_m = \frac{dI_D}{dV_{GS}} \quad \text{constant } V_{DS}$$

In Saturation:

$$1 \quad g_m = \beta \left(V_{GS} - V_t \right) \\ = \mu_C \frac{C_{ox} W}{L} \left(V_{GS} - V_t \right)$$

MOSFET Scaling

Moore's

- Constant Voltage Scaling
- Constant Field Scaling

We can't scale the voltage

Constant Field Scaling

Internal field are constant, while dimensions are scaled by S ($S > 1$)

$C_{ox} \rightarrow$ oxide cap. after scaling
 $C_{ox} \rightarrow$ by S

$$C_{ox}' = \frac{C_{ox}}{S} = S C_{ox}$$

$\frac{W}{L}$ unchanged

μ_m is unchanged
 mobility
 minority type

$$\mu_p = 450 \text{ cm}^2/\text{Vs}$$

$$\therefore \mu_m = 1350 \text{ cm}^2/\text{Vs}$$

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$n \rightarrow$ fast mobility 2 to 3 times faster
type than p type.

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Linear

$$I_D' = K_n' \left[(V_{ds}' - V_T') V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$\frac{V_{ds}'}{S} = \frac{V_T'}{S}$$

$$= SK_n \frac{1}{S^2} \left[(V_{ds} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$= \frac{I_D}{S}$$

Saturation region

$$\boxed{I_D' = \frac{I_D}{S}}$$

$$L' = \frac{L}{S}$$

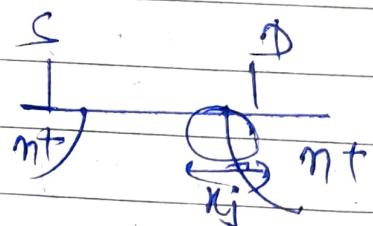
$$W' = \frac{W}{S}$$

$$t_{ox}' = \frac{t_{ox}}{S}$$

depletion region $K_j' = \frac{K_j}{S}$
(longer)

$$V_{DD}' = \frac{V_{DD}}{S}$$

$$V_{TO}' = \frac{V_{TO}}{S}$$



acquisition $\leftarrow N_A' = S N_A$
 $N_D' = S N_D$

depletion width

$$W = \sqrt{\frac{2\epsilon_{Si}(V_{Bi} + V_{DS})}{qN_A}}$$

built in potential

across pn junction

(under mobius case)

$$N_A' = \frac{q\epsilon_{Si}(V_{Bi} + V_{DS})}{(W')^2 q} = \frac{s^2 N_A}{s} = \underline{s N_A}$$

$$\text{Power}, P' = V_{DD}' I_D' = \frac{P}{s^2}$$

Power density, $\frac{P'}{\text{Area}'} = \frac{P}{\text{Area}}$

gate capacitance $C_g' = \frac{W' L' C_{ox}'}{s} = \frac{1}{s} C_g$

Constant-Voltage Scaling

Scaling of voltage may not practical in some cases.

Quantity

Before Scaling

after scaling

dimension

$W/L, t_{ox}, x_j$

reduce by s

doping

V_{DD}, V_T

unchanged

N_A, N_D

multiply by s^2

$(N_A' = N_A s^2)$

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$$C_{ox}' = S C_{ox}$$

$$\textcircled{1} \quad I_D' (\text{linear}) = \frac{Kn'}{2} \left[(V_{ds} - V_T') V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$$b_n' = \frac{1}{L} C_{ox} W$$

same

$$= S I_D (\text{linear})$$

$$I_D' (\text{saturation}) = S I_D (\text{saturation})$$

$$\text{Power } P' = I_D' V_{ds}' = SP$$

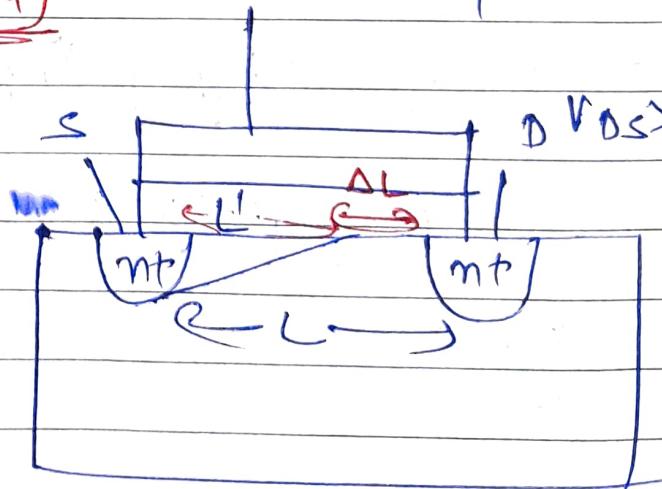
same

$$\text{Power density} = \frac{P'}{A'} = \frac{SP}{A' s^2} = \underline{\underline{s^3 P}} \quad A$$

WL

channel length modulation (CLM)

$V_{ds} > V_T$



$$L' = L - \Delta L$$

→ channel is shortened

$$I_D(\text{sat}) = \mu_n C_{ox} \frac{W}{L} (V_{ds} - V_T)^2$$

$$= \mu_n C_{ox} \left(\frac{W}{L - \Delta L} \right) \frac{W}{2L} (V_{ds} - V_T)^2$$

accounts CLM Effect.

I_{Dss}

To simplify it,

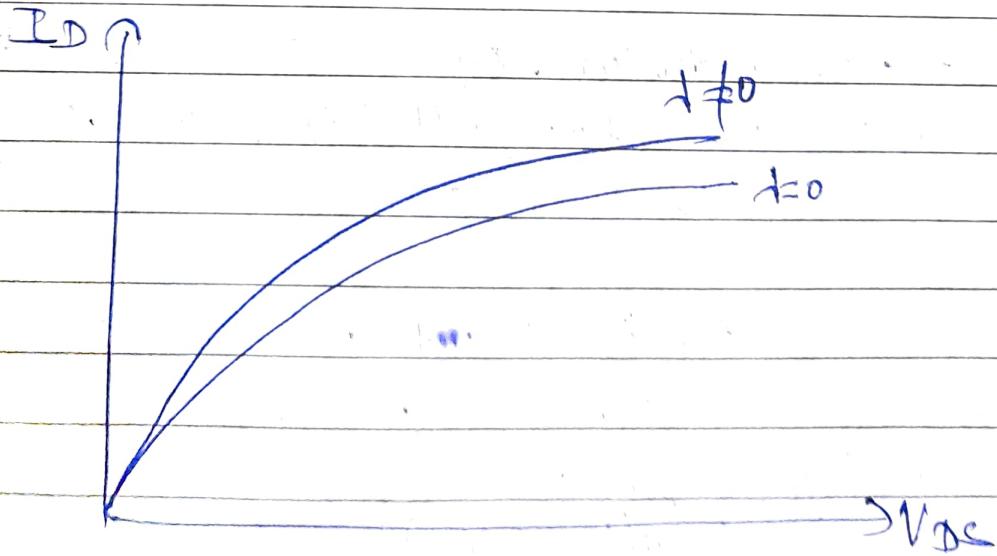
$$L - \Delta L \approx L - \lambda V_{ds}$$

Fitting parameter,

λ is model parameter and is called CLM Coefficient
 λ varies with V_{ds} .

assume $\lambda V_{ds} \ll 1$

$$I_D(\text{sat}) = \mu_n C_{ox} \frac{WL}{2L} (V_{ds} - V_T)^2 (1 + \lambda V_{ds})$$



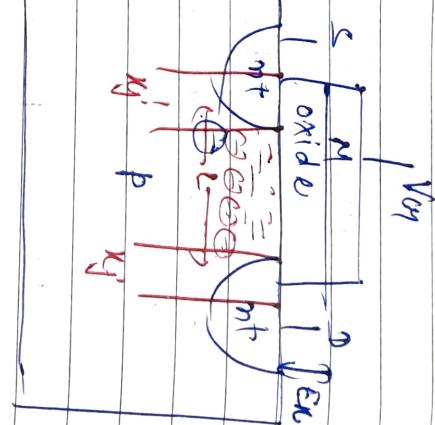
IV Equation for short channel device

→ L comparable with depletion region thickness of ≈ 10 .

→ L_{eff} is equal to x_j'

$$L = 50 \text{ nm}$$

$$x_j' = 30 \quad x_j' = 12$$



→ limitations will be imposed on
drift characteristics,

→ Modification of threshold voltage → V_{th}

→ In short channel devices, carrier velocity is a function of vertical electric field (E_z). E.g. influence the scattering of the carriers.

The surface mobility is reduced w.r.t bulk mobility.
 High \rightarrow low field
 \downarrow
 $m(x_j')^2, m_0 \rightarrow$ low inversion region
 e-easily flow
 $1 + n(V_{bus} - V_t)$
 mobility saturates after certain time.

More \downarrow low field surface mobility
 n empirical coefficient

Technology node
 $L = 50 \text{ nm}, N_f = 1, 2, N_{bus} = 1, 2V, V_t = 0.25, 2, M_{bus} = 1, 2$

→ lateral field (E_y) \propto for reduced channel length

$V_d \propto$ electric field for low value
Saturation at High value

$$V = \mu E$$

$$E_y = \frac{V_{DS}}{L_{eff}}$$

$$E_y = E_{crit} \approx 10^5 \text{ V/cm}$$

(critical field)

$$V_{sat} = 10^7 \text{ cm/s}$$

$v_d = \mu_n (V_{eff}) E_y$, $= V_{sat}$,	$E_y < E_c$ $E_y \geq E_c$
--	-------------------------------

$$I_D = 0, \quad V_{DS} < V_T$$

$$I_D(\text{lin}) = \frac{\mu C_{ox} W}{L} \frac{1}{1 + \left(\frac{V_{DS}}{E_c L} \right)} \left[(V_{DS} - V_T) \frac{V_{DS} - V_{DS}^2}{2} \right]$$

linear current

$$V_{DS} < \frac{(V_{DS} - V_T) E_c L}{(V_{DS} - V_T) + E_c L}$$

$$I_D(\text{sat}) = W V_{sat} C_{ox} \frac{(V_{DS} - V_T)^2}{(V_{DS} - V_T) + E_c L} \left(1 + \frac{dV_{DS}}{dV_{DS}} \right)$$

CLM coefficient

$$V_{DS} \geq V_T$$

$$V_{DS} \geq \frac{(V_{DS} - V_T) E_c L}{(V_{DS} - V_T) + E_c L}$$

MOSFET Capacitance

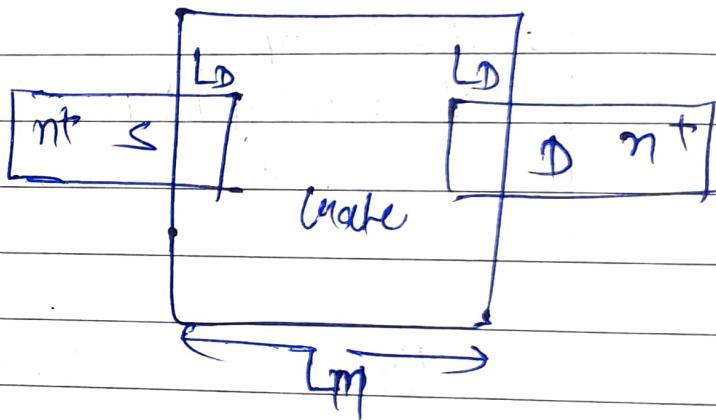
Examining AC characteristic of MOSFET to apply digital circuits, we have to analyze nature and amount of parasitic capacitance

L_M is mask length

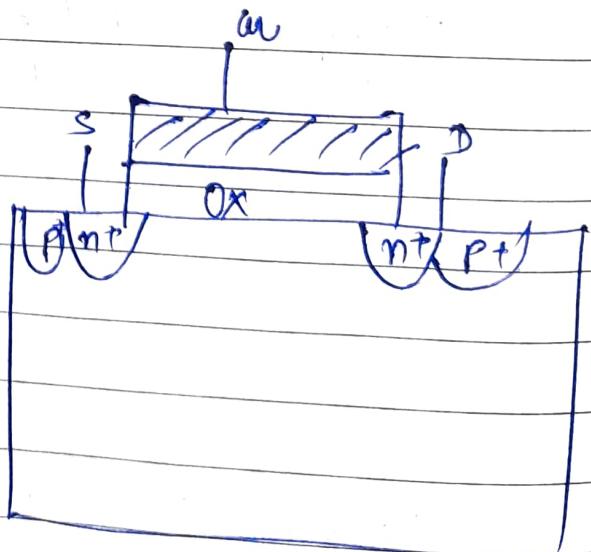
of S & D

$$L = L_M - 2L_D$$

L_D is overlap length

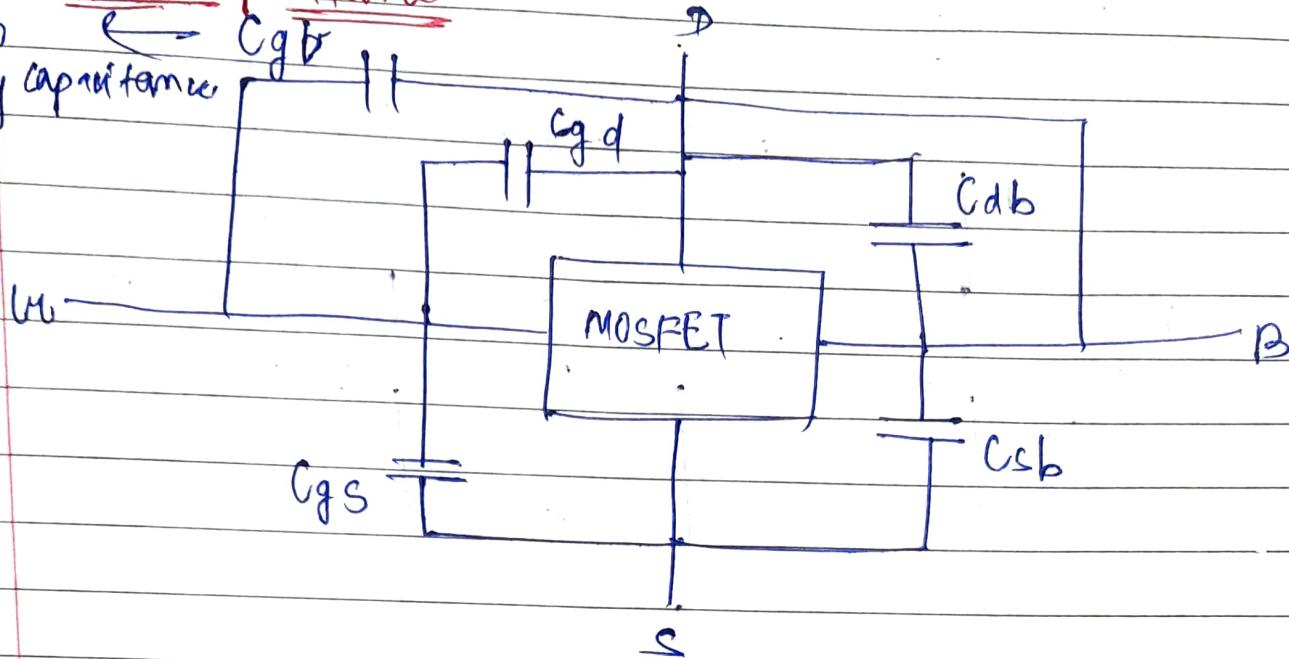


→ channel stop is implant to electrically isolate neighbouring devices on same substrate.



Oxide Capacitance

gate to body capacitance



Due to gate overlap S & D region and result in overlap Capacitance C_{oas} (overlap) $\downarrow \rightarrow$ whether we apply bias or not thus exist.

$$C_{oas}(\text{overlap}) = C_{ox} W L_D \quad \{$$

$$C_{oas}(\quad) = C_{ox} W L_D \quad \}$$

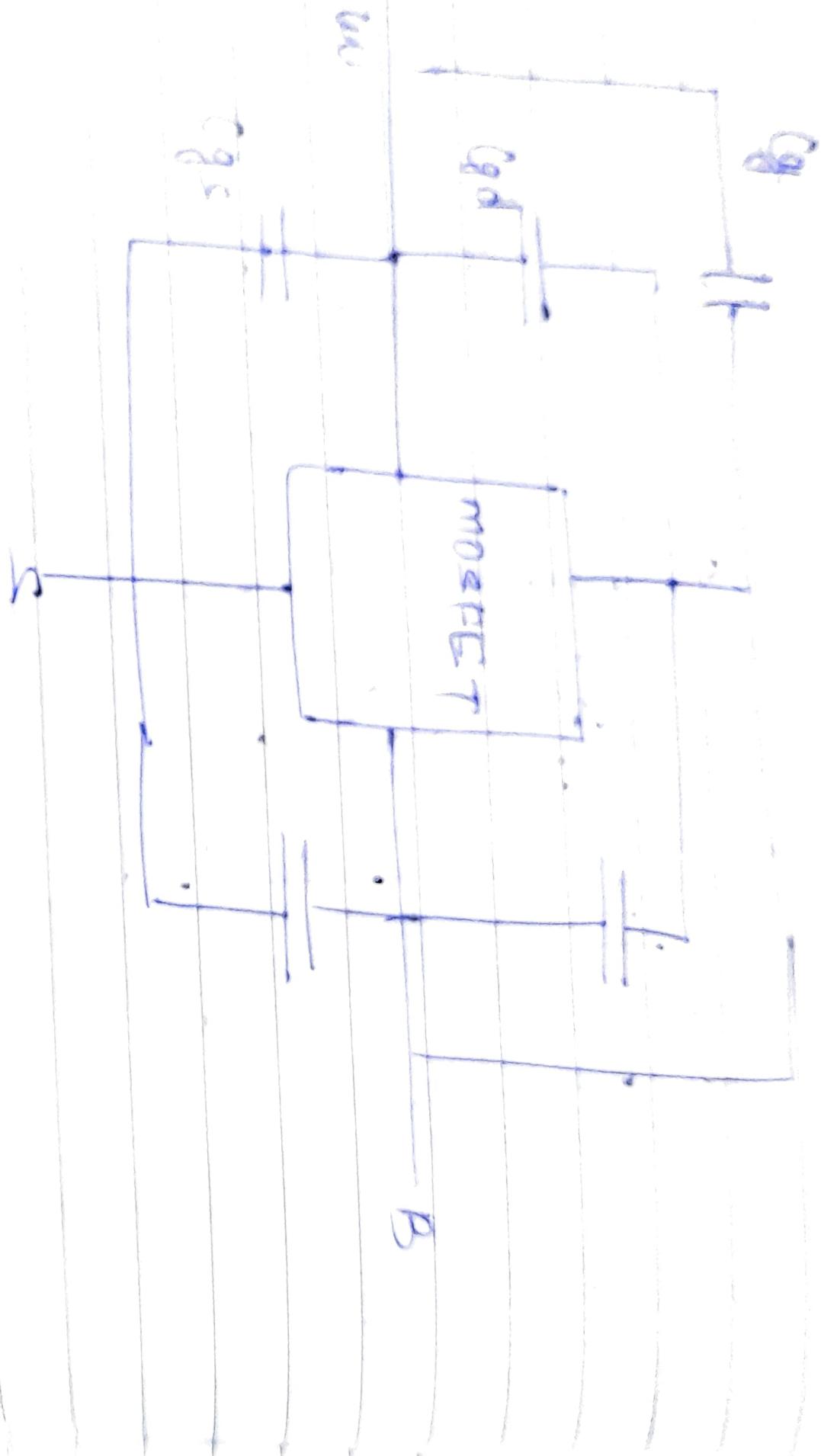
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

independent of Bias

Oxide related Capacitance

1. Cast a spell and Miss

四



Cap.

Cutoff

linear

Parkvation

$$C_{gb}(\text{total})$$

$$C_{ox}WL$$

$$0$$

$$0$$

$$C_{gd}(\text{total})$$

$$C_{ox}WL_D$$

$$C_{ox}WL_D$$

$$C_{gs}(\text{total})$$

$$C_{ox}WL_D$$

$$\frac{1}{2}(C_{ox}W + C_{ox}WL_D)$$

$$\frac{1}{2}(C_{ox}W + C_{ox}WL_D)$$

$$\frac{2}{3}C_{ox}WL + \frac{1}{3}C_{ox}WL_D$$

Cutoff

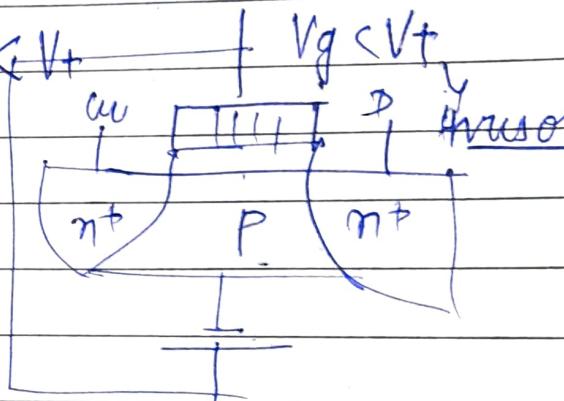
channel is not formed. No conducting channel between S to D.

$$C_{gs}=0 \quad C_{gd}=0$$

$$C_{gb} = C_{ox}WL$$

$$V_{gs} < V_t$$

$$V_g < V_t$$

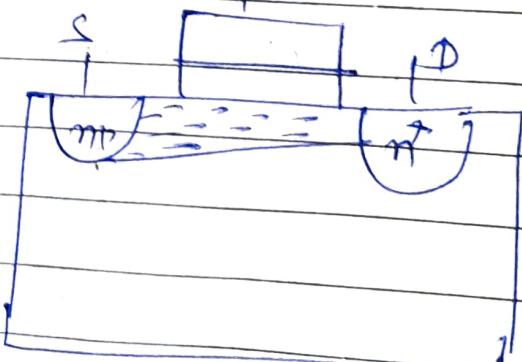


linear mode

The Surface is inverted from p to n, the conducting inversion channel on surface effectively shields source from gate electric field $C_{gb}=0$

Area to channel is equally shared b/w S + D

$$C_{gs} = C_{gd} = \frac{1}{2}C_{ox}WL$$



Date / /

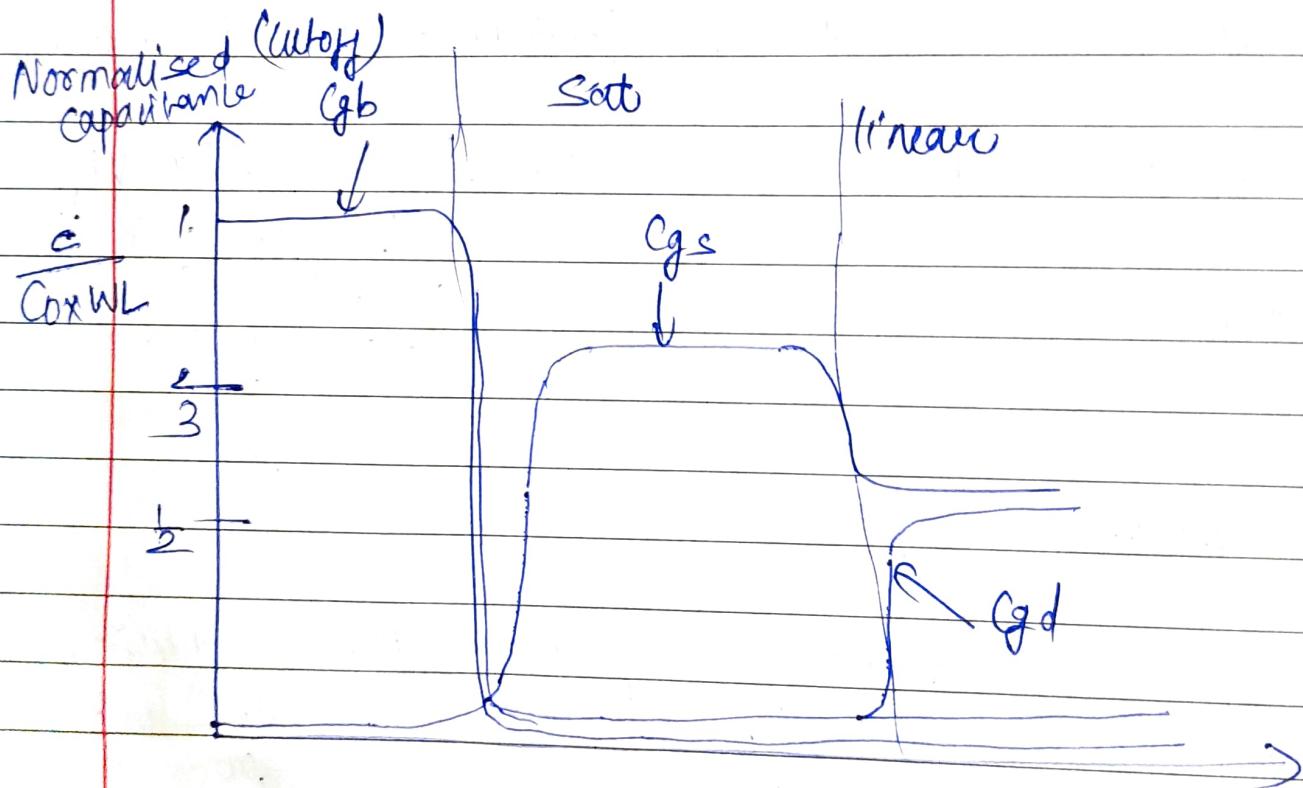
Saturation mode

channel will not reach to drain terminal $C_{gd} = 0$
due to pinch off

Source is still conducting it shields the gate to body

Capacitance $C_{gb} = 0$

$$C_{gs} = \frac{2}{3} C_{ox} WL \text{ (approximated)}$$



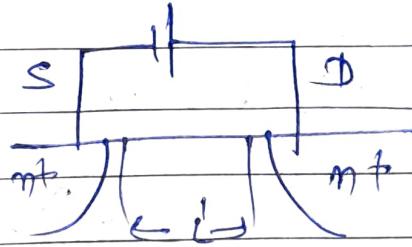
Junction isolated Capacitance

C_{sb} and C_{db}

Both are due to depletion charge surrounding S and D. It's a function of Voltage.

$$N_d = \sqrt{\frac{2\epsilon_{ci}(\phi_0 - V)}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right)}$$

$$\phi_0 = V_f / m \left(\frac{N_A N_D}{n^2} \right)$$



built-in potential.

$$\begin{array}{ll} \text{Junction is FB} & V_{FB} \\ \text{" " RB} & V_{RR} \end{array}$$

Space charge

$$Q_j = Aq \left(\frac{N_A N_D}{N_A + N_D} \right) X_d$$

$$= A \sqrt{\frac{2\epsilon_{ci} q}{\pi} \left(\frac{N_A N_D}{N_A + N_D} \right) (\phi_0 - V)}$$

$$C_j^0 = \left| \frac{dQ_j}{dV} \right| = A \sqrt{\frac{\epsilon_{ci} q}{2} \left(\frac{N_A N_D}{N_A + N_D} \right)} \frac{1}{\sqrt{\phi_0 - V}}$$

$$C_j(V) = \frac{A \cdot C_j^0}{\left(1 - \frac{V}{\phi_0} \right)^m}$$

m is called grading coefficient

$m = \frac{1}{2}$, abrupt junction

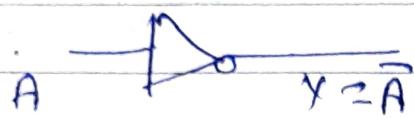
$= \frac{1}{3}$, linearly graded junction

$$C_{j0} = \sqrt{\frac{\epsilon_{ci} q}{2}} \left(\frac{N_A N_D}{N_A + N_D} \right) \frac{1}{\phi_0}$$

zero bias junction capacitance

C_j depends on bias

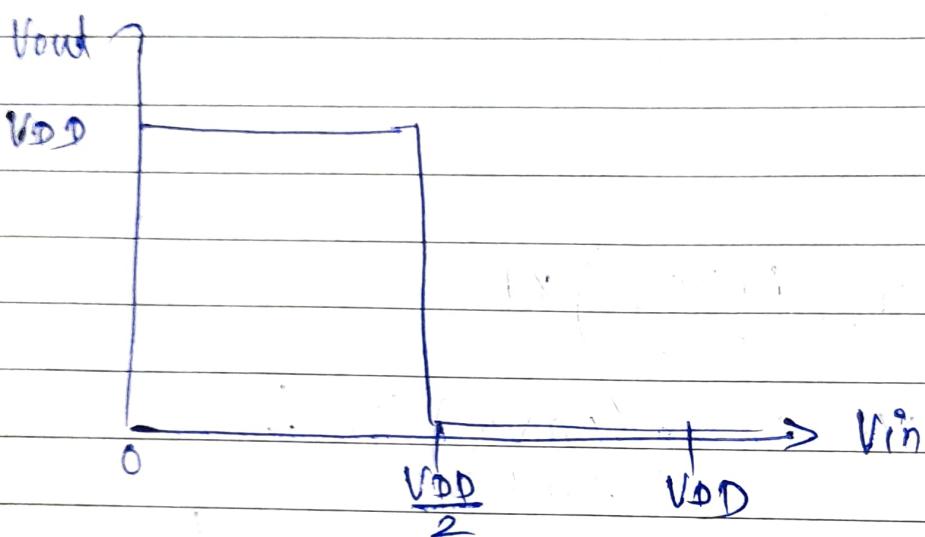
MOS Inverter static characteristics



A	Y
0	1

logic '1' $\rightarrow V_{DD}$
logic '0' $\rightarrow 0$

1	0
---	---



Ideal voltage transfer characteristic
(V_{TC})

Input Voltage betw 0 and $\frac{V_{DD}}{2} = V_{IN}$

Output is V_{DD}

Input $\frac{V_{DD}}{2}$ to V_{DD}

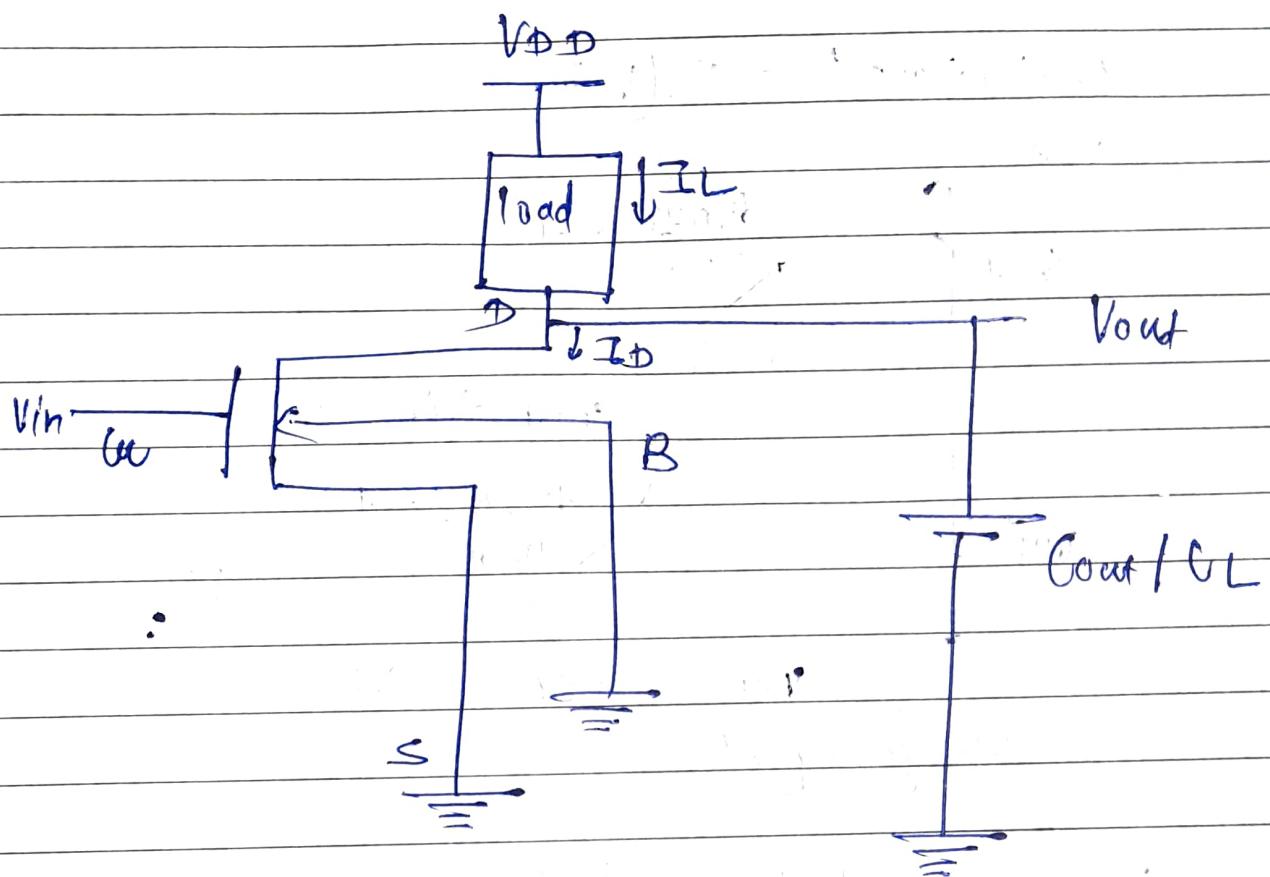
Output is 0

$0 < V_{in} < V_{IN}$
O/p is logic '1'

$V_{IN} \leq V_{in} < V_{DD}$

O/p is logic '0'

$C_{out}/C_L \rightarrow$ Output or load Capacitance



$V_{in} > V_{th}$ Invoked from P to N

⇒ nMOS ON for logic '1'

$V_{in} > V_{th}$

V_{in} is logic '1'

V_{out} is logic '0'

Output will be connected to the ground

& capacitor discharges towards the ground

⇒ V_{in} logic '0', nmos OFF

$V_{in} \leq V_{th}$ { open circuit } → Output is connected to V_{DD}

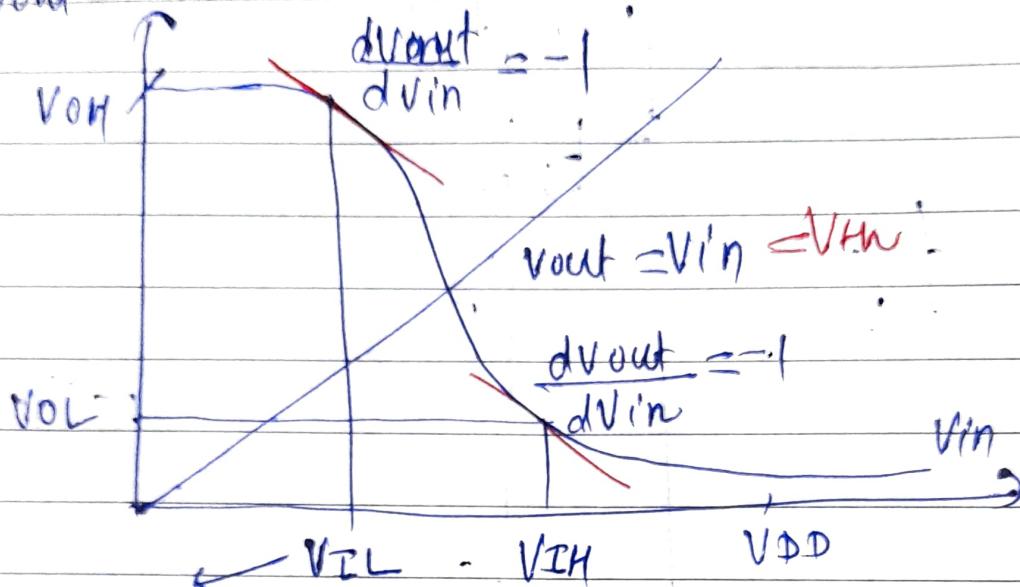
$V_{out} \rightarrow$ logic '1'

V_{out} is logic '1'

Voltage transfer characteristics (VTC)

$$I_D(V_{in}, V_{out}) = I_L(V_L)$$

V_{out}



Voltage Input low

for low input, $V_{out} = V_{on}$

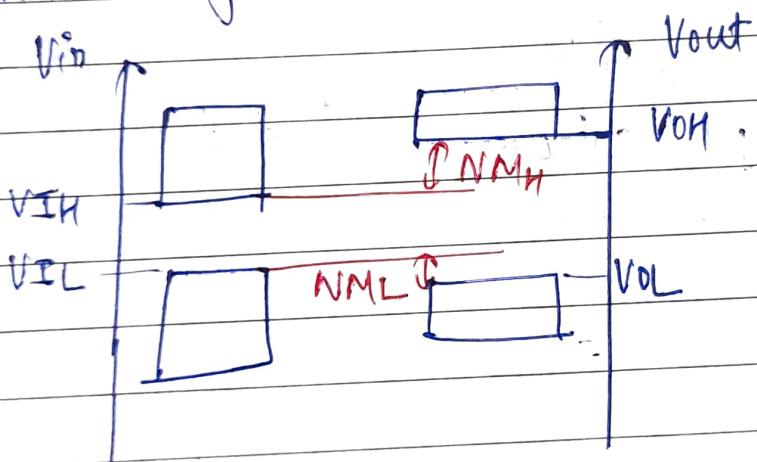
nMOS is in OFF condition and does not conduct current
the voltage drop across R_L is small and output is high

increase V_{in} transistor starts conducting and output starts to rise.

V_{on} Maximum o/p Voltage when o/p is logic '1'
 V_{OL} Minimum

V_{IL} Maximum I/p Voltage which can be taken as logic '0'
 V_{IH} Minimum

- any Input level betⁿ 0 and V_{IL} as logic '0'
V_{DD} and V_{IH} as logic '1'
- any Output level betⁿ lowest available voltage and V_{OL} is
logic '0' o/p
highest logic ''1' o/p'
and V_{OH} as
- Noise margin (NM)
The noise tolerance of digital circuit is called Noise margin.



low signal NM (NM_L)
High NM (NM_H)

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

$$\begin{aligned} V_{out} &= f(V_{in}) \\ &= f(V_{in} + V_{noise}) \end{aligned}$$

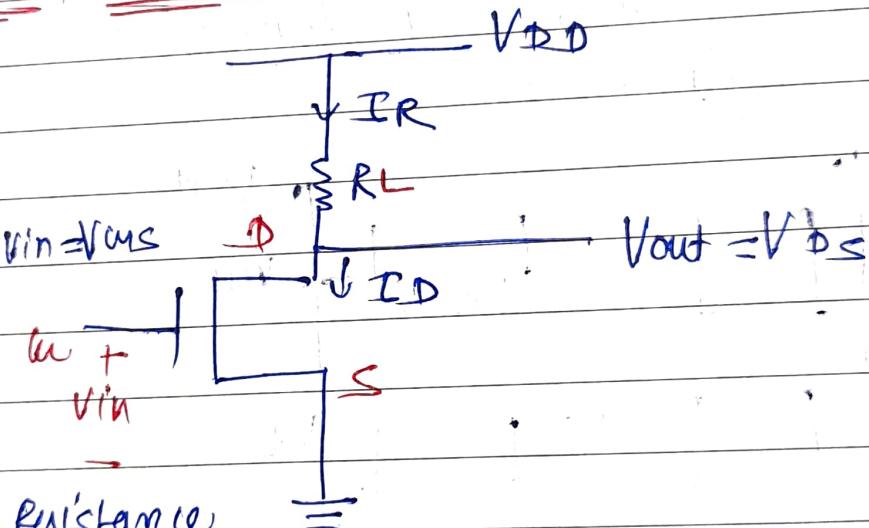
Power

$$P = V_{DD} \cdot I_{DC}$$

$$= \frac{V_{DD}}{2} [I_{DC} (V_{in} = low) + I_{DC} (V_{in} = High)]$$

If low corresponds to logic '0' during soft time
logic '1'

Resistive load Inverter



$$I_D = I_R$$

$$I = 0 \quad V_{SB} = 0$$

Source to body Voltage is 0

Because Body current is 0.

V_{T0} = Threshold voltage

V_{in} < V_{T0} Cut off mode does not conduct Current

V_{in} ≥ V_{T0}, transistor starts Conducting

V_{DS} = V_{out} > V_{DS-sat} transistor in Sat region

V_{Dsat} is smaller than $\frac{V_{DD}}{2}$

$$I_{Dsat} = W V_{Dsat} C_{ox} \frac{(V_{in} - V_{T0})^2}{(V_{in} - V_{T0}) + E_c L}$$

$V_{in} < V_{T0} \rightarrow \text{cutoff}$

$$V_{DS} < V_{DSsat} - V_t$$

$$V_{out} < V_{in} - V_{T0}$$

$V_{in} > V_{out} + V_{T0}$, linear-region

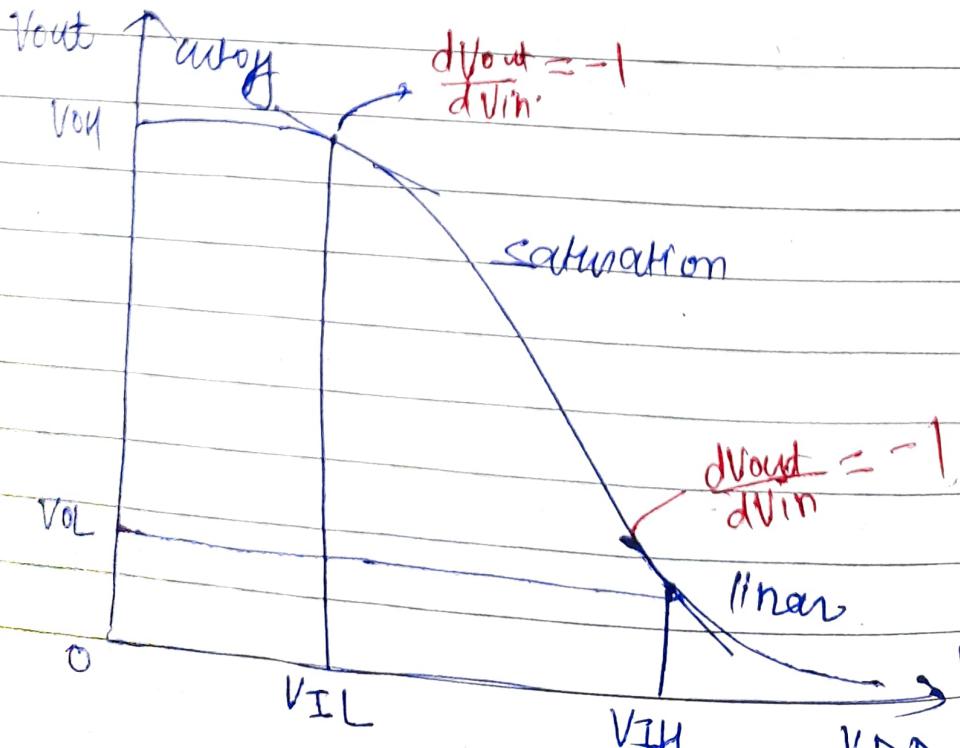
$$V_{DS} \geq V_{DSsat} - V_t, V_{in} \leq V_{out} + V_{T0}$$

$$V_{out} \geq V_{in} - V_{T0}$$

→ Saturation region

$$I_D = \frac{\mu n C_{ox} W}{L} \left(1 - \left(1 + \frac{V_{out}}{E_c L} \right) \right) \left[(V_{in} - V_{T0}) V_{out} - \frac{V_{out}^2}{2} \right]$$

Increase V_{in} , transitions in linear region.



Date / /

V_{OH}

$$V_{out} = V_{DD} - I_R R_L$$

V_{in} low, transistors in cut-off $I_R = 0$

$$\boxed{V_{out} = V_{DD}}$$

V_{OL}

Let, $V_{in} = V_{out} \approx V_{DD}$, transistors in linear region

$$I_R = \frac{V_{DD} - V_{cat}}{R_L}$$

$$\frac{V_{DD} - V_{out}}{R_L} = I_S n \frac{1}{\left(1 + \frac{V_{OL}}{E_c L}\right)}$$

$$\left[(V_{DD} - V_{TO}) V_{OL} - \frac{V_{OL}^2}{2} \right]$$

neglect V_{OL} is small

$$V_{OL}^2 - 2 \left(V_{DD} - V_{TO} + \frac{1}{k_n R_L} \right) V_{OL} + \frac{2}{k_n R_L} V_{DD} = 0$$

$$V_{OL} = V_{DD} - V_{TO} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{TO} + \frac{1}{k_n R_L} \right)^2 - \frac{2 V_{DD}}{k_n R_L}}$$

$$\underline{\underline{V_{IL}}} \quad V_{in} = V_{IL} \quad \frac{dV_{out}}{dV_{in}} = -1$$

Transistor in Saturation

$$\frac{V_{DD} - V_{cat}}{R_L} = W V_{cat} C_ox \frac{(V_{in} - V_{TO})^2}{(V_{in} - V_{TO}) + E_c L}$$

$$\boxed{V_{cat} = \frac{M_n E_c}{2}}$$

V_{in} is just greater than V_{TO} neglect $(V_{in} - V_{TO})$

$E_c \rightarrow$ Critical electric field

$$\frac{V_{DD} - V_{out}}{RL} = \frac{k_n}{2} (V_{in} - V_{TO})^2 ; k_n = \mu n C_{ox} \frac{W}{L}$$

$$\rightarrow \frac{1}{RL} \frac{dV_{out}}{dV_{in}} = k_n (V_{in} - V_{TO})$$

$$\rightarrow \frac{1}{RL} (-1) = k_n (V_{in} - V_{TO})$$

$$\boxed{V_{CL} = V_{TO} + \frac{1}{k_n RL}}$$

$$V_{out}(V_{in} = V_{IH}) \approx V_{DD} - \frac{k_n}{2} (V_{in} - V_{TO})^2 RL$$

$$= V_{DD} - \frac{k_n}{2} \left(\frac{1}{k_n RL} \right)^2 RL$$

$$\boxed{V_{out} \approx V_{DD} - \frac{1}{2k_n RL}}$$

V_{IH} : $V_{in} = V_{IH}$, transistors in linear, $\frac{dV_{out}}{dV_{in}} = -1$

$$\frac{V_{DD} - V_{out}}{RL} = k_n \frac{L}{(1 + \frac{V_{out}}{E_{Cox} L})} \left[(V_{in} - V_{TO}) V_{out} - \frac{V_{out}^2}{2} \right]$$

neglect

$$\frac{V_{DD} - V_{out}}{RL} = k_n \left[(V_{in} - V_{TO}) V_{out} - \frac{V_{out}^2}{2} \right]$$

$$\rightarrow \frac{1}{RL} \frac{dV_{out}}{dV_{in}} = k_n \left[(V_{in} - V_{TO}) \frac{dV_{out}}{dV_{in}} - V_{out} \frac{dV_{out}}{dV_{in}} \right]$$

Date _____ / _____ / _____

Q Unknown Vin and Vout

$$\frac{V_{in} - V_{out}}{R_L} = k_n \left[(V_{in} + V_{out} - \frac{1}{k_m R_L} V_{out}^2) - \frac{1}{k_m R_L} V_{out} - \frac{V_{out}^2}{2} \right]$$

$$V_{in} = V_{in} + V_{out} - \frac{1}{k_m R_L}$$

$$V_{out} (V_{in} = V_{in}) = \sqrt{\frac{8}{3} \frac{V_{in}}{k_m R_L}}$$

$$V_{in} = V_{in} + \sqrt{\frac{8}{3} \frac{V_{in}}{k_m R_L} - \frac{1}{k_m R_L}}$$

Calculate NNH & NNL

 $\rightarrow V_{in}$

HARDIK DAMOR

COMPUTER SCIENCE AND ENGINEERING

Gender- MALE DOB-18/11/2000

Email ID-2021ucp1156@mnit.ac.in (college)

hardikdamor2511@gmail.com(personal)

Contact no.- 7742930191

OBJECTIVE (career objective)

- Seeking an entry-level position to begin my career in a high-level professional environment
- To secure a challenging position in a reputed organization to expand my learnings, Knowledge and skills.

EDUCATIONAL DETAILS

Degree	Board/ Institute	Passing Year	CGPA / %
B.Tech. in CSE	NIT Jaipur (MNIT)	2025	6.18%
Intermediate/+2	RBSE	2021	76.80%
Matriculation	RBSE	2017	90.83%

KEY PROJECTS

- Personal Portfolio

TECHNICAL SKILLS

- Computer Programming Languages: C, C++, HTML,CSS
- Data Structure and Algorithms
- MySQL
- MS Office: MS Word, MS Power Point, MS Excel
- Others: FLAT, Autocad, Concurrent Programming, Parallel Programming, Packet Tracer, WireShark,Proteus

HOBBIES

- Chess, Football
- Book Reading