Presentation Topic

Name of the course :- Basic Electronics Engineering

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(An Autonomous Institute affiliated to Savitribai Phule Pune University)
(NBA and NAAC accredited, ISO 9001:2015 certified)

Unit – 03:Field-Effect Transistor (MOSFET) & Power Devices

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Acknowledgement

- All figures and text in this presentation are taken from book "Electronic Devices – Conventional Current Version," 9th Ed., by Thomas L. Floyd.

Outline

- Difference between BJT and FET
- E-MOSFET
- Construction,
- Working
- Characteristics
- Biasing techniques and CS Amplifier
- Power Devices- SCR and TRIAC
- Construction,
- Working
- Characteristics
- Application

Difference Between BJT and FET

- BJT: Bipolar and FET: Unipolar
- BJT: Current controlled, FET: Voltage Controlled
- FETs are more temperature stable than BJT
- Size of FET is smaller than BJT
- High Input impedance and offer low gain

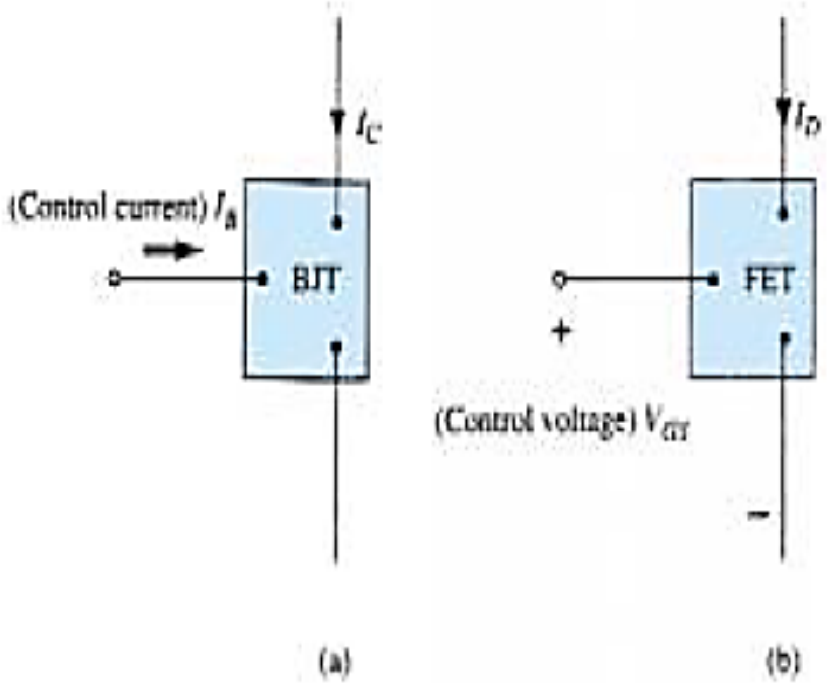


Figure 5.1 (a) Current-controlled and (b) voltage-controlled amplifiers.

Field Effect Transistor (FET): Introduction

- Types of FETs :

  Junction field-effect transistor (JFET)

  metal-oxide-semiconductor field-effect transistor (MOSFET).
- Types of MOSFET:

  depletion D-MOSFET

  enhancement E-MOSFET
- In FET: An *electric field* control the conduction path of the output current
- The MOSFETs are popular in the design and construction of integrated circuits (ICs) for digital computers.
- Its thermal stability and low power dissipation makes it extremely popular in computer circuit design and in VLSI technology

EMOS-FET (Metal Oxide Semiconductor Field Effect Transistor) : Construction

N-channel Enhancement- MOSFET

- A slab of *p*-type silicon substrate and two n-type regions forming the source and drain terminals are connected through metallic contacts to *n*-doped regions,
- The channel is absent between the two *n*-doped regions.
- The SiO2 layer is present to isolate the gate metallic platform from the region between the drain and source

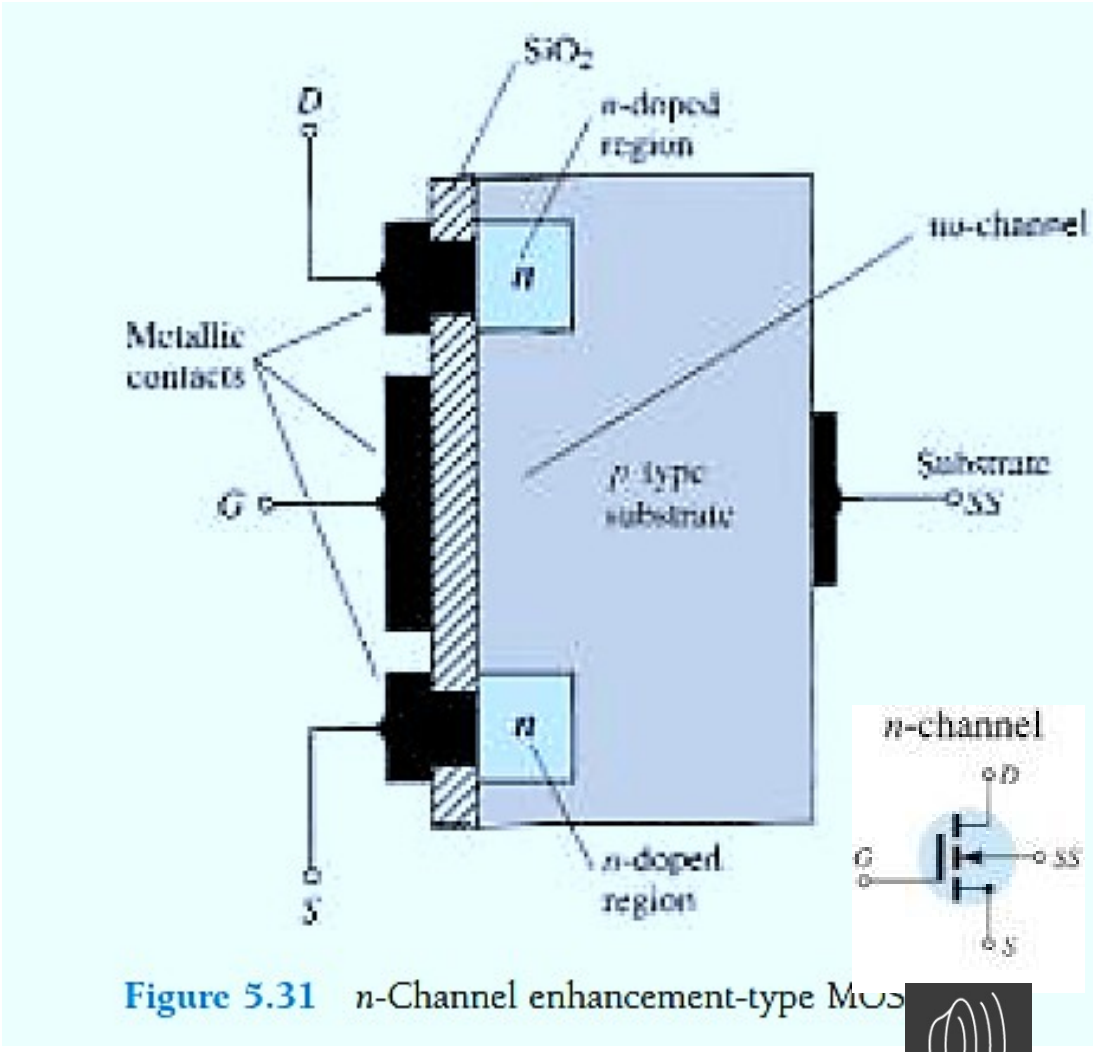
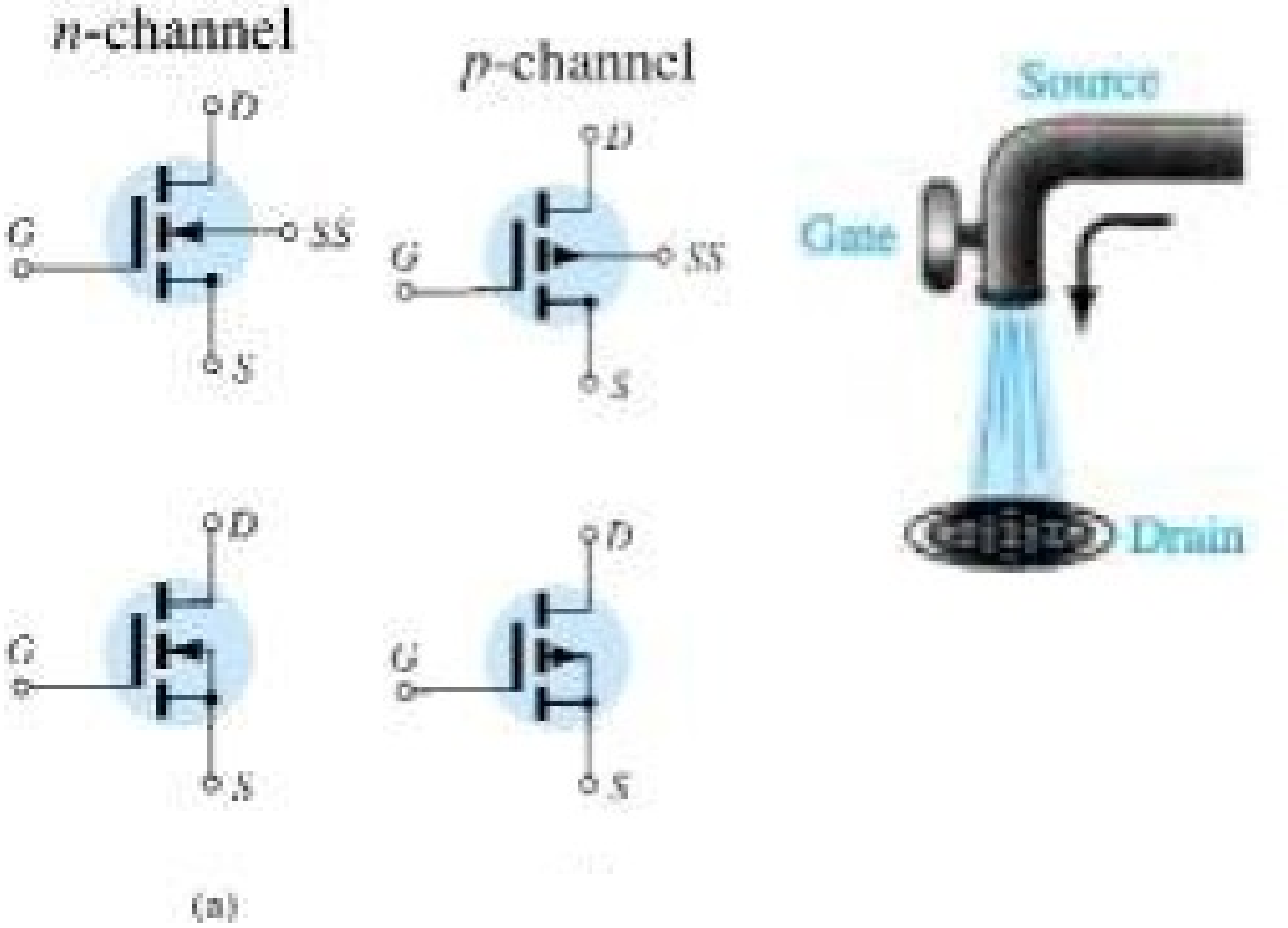


Figure 5.31 *n*-Channel enhancement-type MOS

E-MOSFET: Symbols and Water Analogy



- N-channel EMOSFET

- With *VDS* at +ve voltage,
- *VGS* at 0 V,
- *SS* connected to the source,
- There are two reverse-biased *p-n* junctions between the *n*-doped regions and the *p*-substrate to oppose the IDS
- The absence of an *n*-channel will result in a zero current.

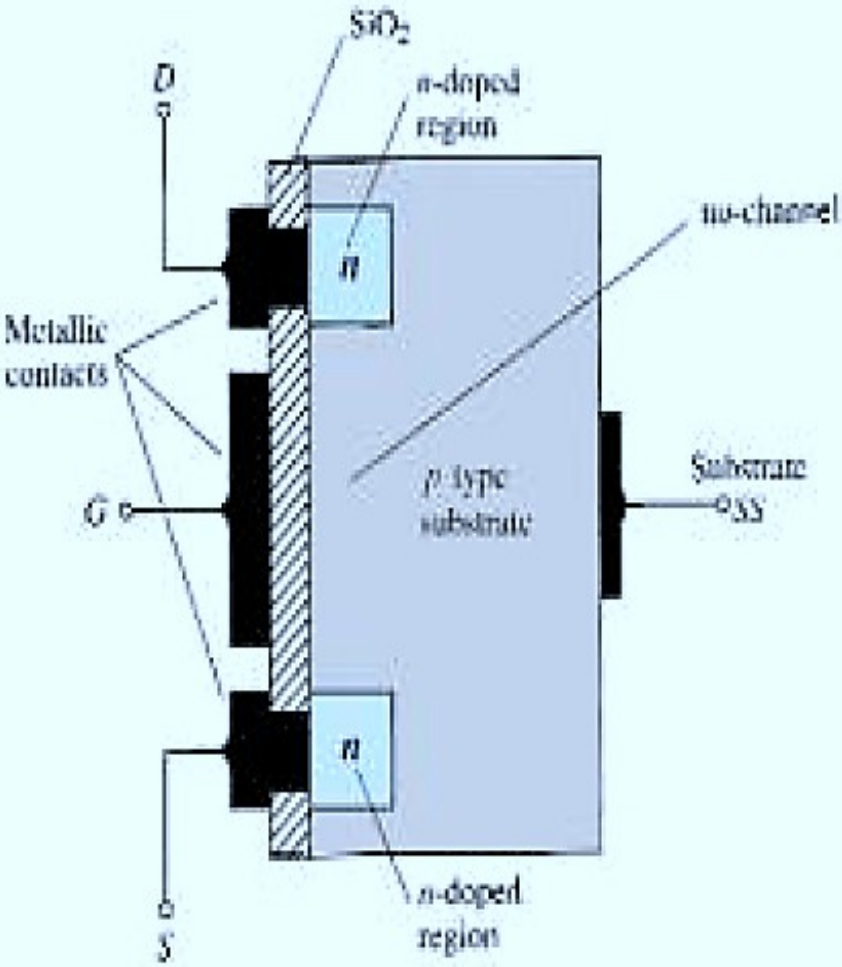
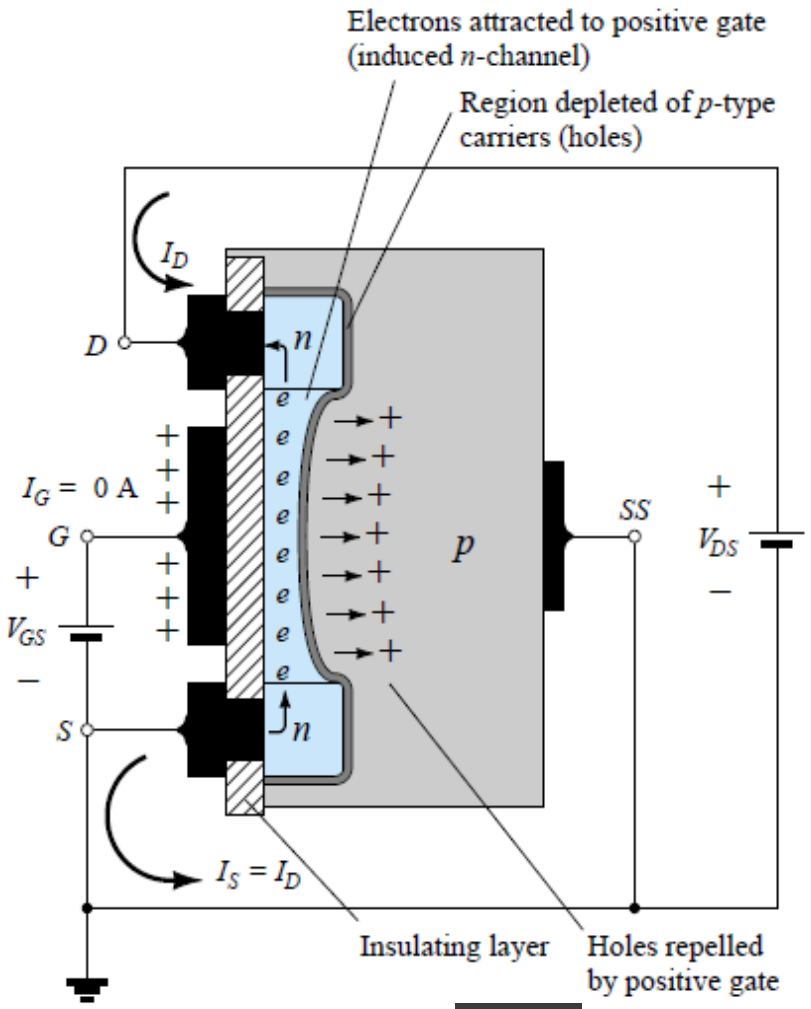


Figure 5.31 *n*-Channel enhancement-type MOSFET.

Channel Formation in E-MOSFET

- *VDS* and *VGS are* positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source.
- The positive potential at the gate will pressure the holes (since like charges repel) in the *p*-substrate along the edge of the SiO2 layer to leave the area and enter deeper regions of the *p*-substrate.
- However, the electrons in the *p*-substrate will be attracted to the positive gate and accumulate near the SiO2 layer.



- The insulating property of SiO2 layer will prevent the electrons from being absorbed at the gate terminal.
- As *VGS* increases, the concentration of electrons near the SiO2 surface increases until the induced *n*-type region can support a measurable flow between drain and source.
- The level of *VGS* that results in the significant increase in drain current is called the *threshold voltage (VT)*.
- Since the channel is nonexistent with *VGS* 0 V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an *enhancement-type MOSFET.*

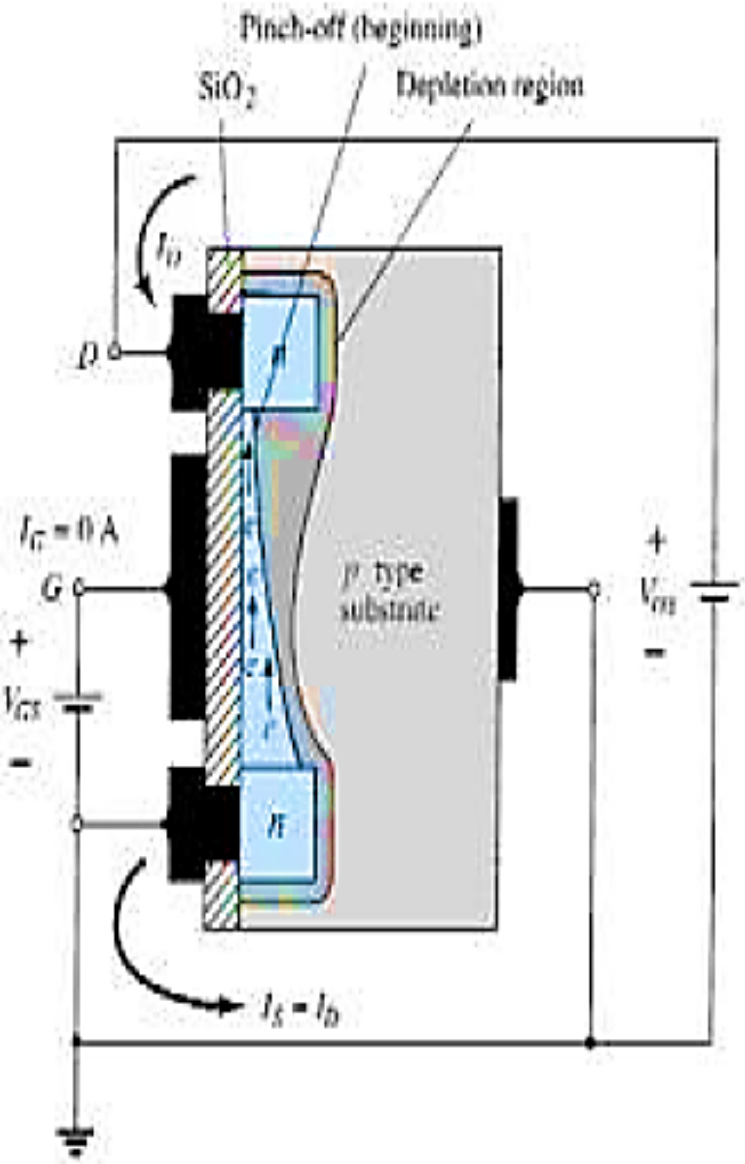
Recap

- Difference between BJT and FET
- Introduction to FET and its types
- Construction of E-MOSFET
- Working of E-MOSFET

Points to be covered

- Pinch-off process
- Transfer characteristics
- Drain Characteristics
- P-channel E-MOSFET
- Configurations (CS, CG, CD)

Fig. Pinch-Off Process

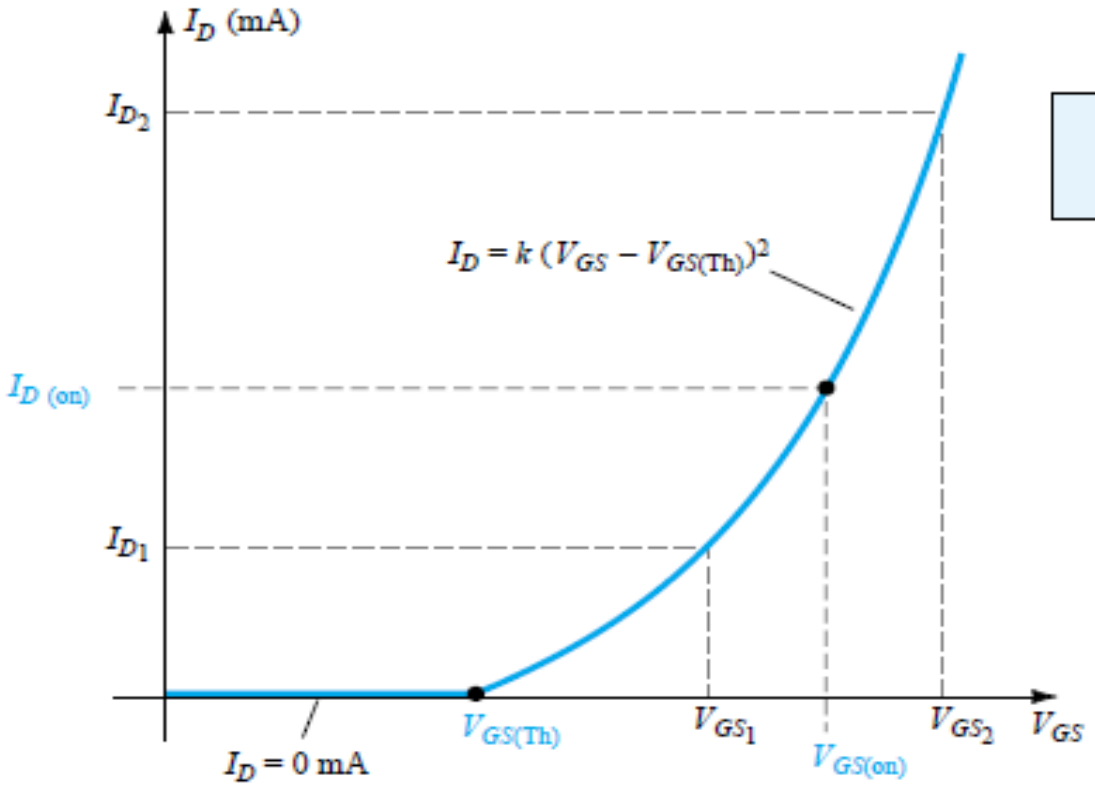


VGS >VT and VDS> VDS(sat)

- The density of free carriers in the induced channel will increase, which increases drain current.
- However, if *VGS* =constant and increase the level of *VDS*> (*VGS*-VGSTh), the drain current will eventually reach a saturation level
- The leveling off of *ID* is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig.

- As $V_{DS} > (V_{GS}-V_T)$, Voltage V_{DG} increases.
- The gate will become less and less positive with respect to the drain.
- This reduction in Gate voltage reduces the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width.
- Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established
- In other words, any further increase in *VDS* at the fixed value of *VGS* will not affect the saturation level of *ID* until breakdown conditions are encountered.

Transfer Characteristics

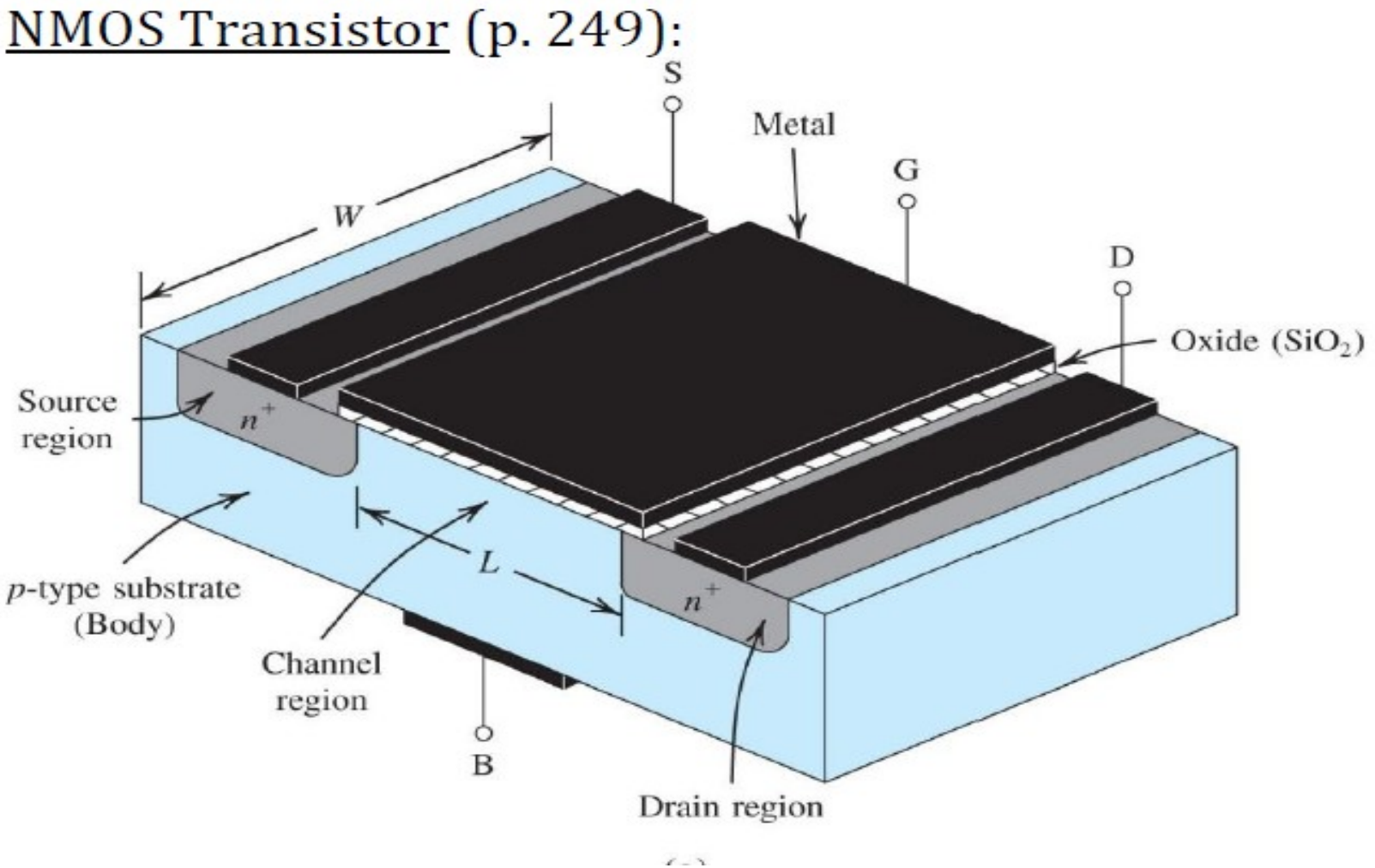


$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

Figure 6.35 Transfer characteristics of an *n*-channel enhancement-type MOSFET.

$$I_D = k(V_{GS} - V_{GS(Th)})^2 \qquad (6.25)$$

Calculation of parameter k



Calculation of transconductance parameter k

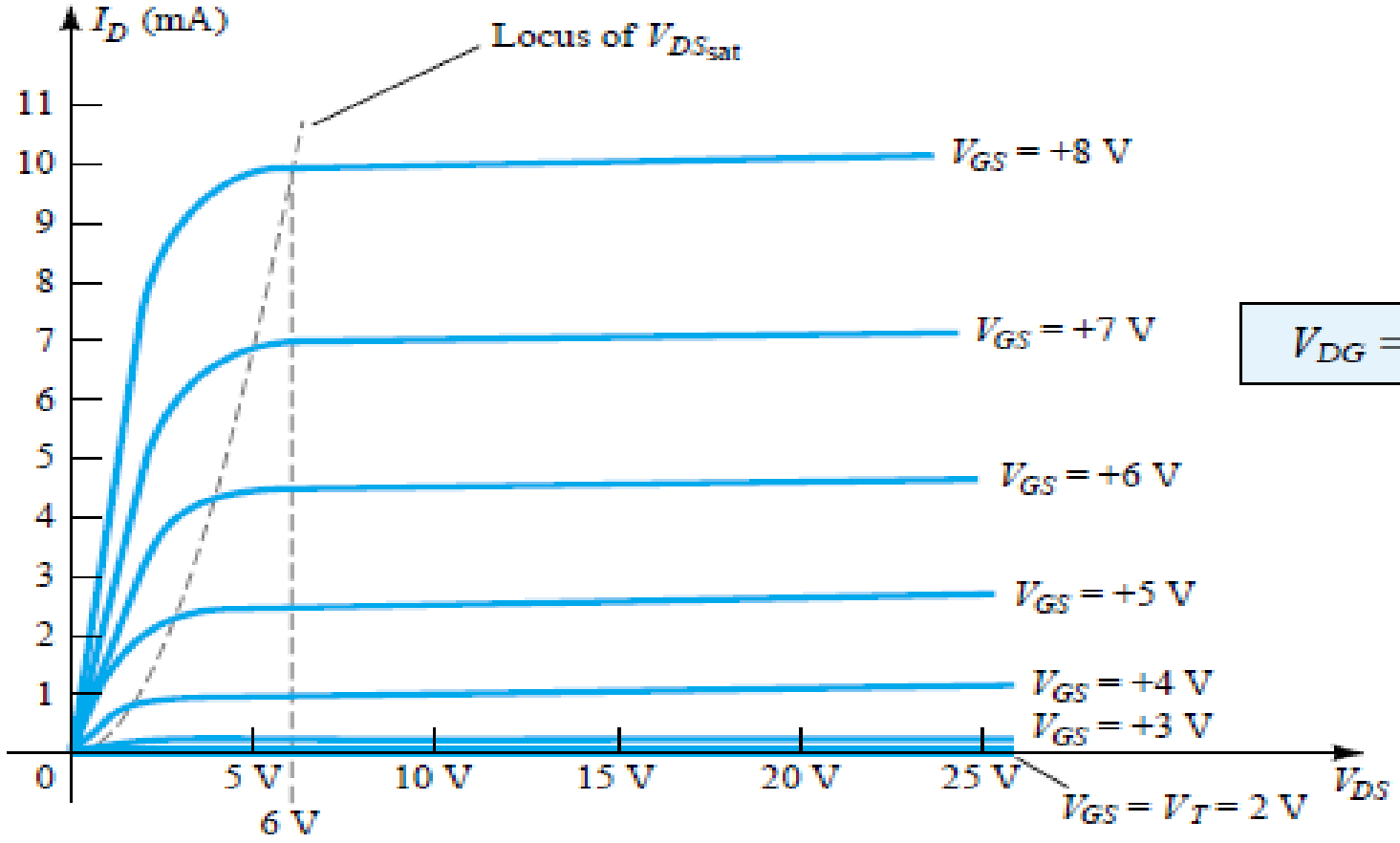
- W=width of Channel, L=length of Channel
- Mu= mobility of charge carriers
- Cox=Capacitance of oxide layer

$$k'_n(W/L) = \mu_n C_{ox}(W/L) = k_n \quad \text{(n-channel) and}$$

$$k'_p(W/L) = \mu_p C_{ox}(W/L) = k_p \quad \text{(p-channel).}$$

Drain Characteristics

$$V_{DSsat} = V_{GS} - V_T$$



$$V_{DG} = V_{DS} - V_{GS}$$

Figure 5.34 Drain characteristics of an *n*-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V^2.

Drain Characteristics

- For a fixed value of *VT*, and the higher the level of *VGS*, the saturation level for *VDS is also more*, as shown by the locus of saturation levels.

$$V_{DSsat} = V_{GS} - V_T$$

- In fact, the saturation level for *VDS* is related to the level of applied *VGS* by applying Kirchhoff's voltage law to the terminal voltages of the MOSFET.

$$V_{DG} = V_{DS} - V_{GS}$$

For VGS < VT, ID=0mA

- The spacing between the levels of *VGS* increased as the magnitude of *VGS* increased, resulting in ever-increasing increments in drain current.

$$I_D = k(V_{GS} - V_T)^2$$

- The squared term results in the nonlinear (curved) relationship between *ID* and *VGS*.
- The *k* term is a constant that is a function of the construction of the device.
- The value of *k* can be determined from the following equation where *ID*(on) and *VGS*(on) are the values for each at a particular point on the characteristics of the device.

Calculation of k from datasheet values (Example)

V_T= 2V, I_D(on)=10mA, V_{GS}(on)=8V, V_{GS}=4V

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \qquad (5.14)$$

Substituting $I_{D(on)} = 10$ mA when $V_{GS(on)} = 8$ V from the characteristics of Fig. 5.34 yields

$$k = \frac{10 \text{ mA}}{(8 \text{ V} - 2 \text{ V})^2} = \frac{10 \text{ mA}}{(6 \text{ V})^2} = \frac{10 \text{ mA}}{36 \text{ V}^2}$$

$$= \mathbf{0.278 \times 10^{-3} \text{ A/V}^2}$$

and a general equation for I_D for the characteristics of Fig. 5.34 results in:

$$I_D = 0.278 \times 10^{-3}(V_{GS} - 2 \text{ V})^2$$

Substituting $V_{GS} = 4$ V, we find that

$$I_D = 0.278 \times 10^{-3}(4 \text{ V} - 2 \text{ V})^2 = 0.278 \times 10^{-3}(2)^2$$

$$= 0.278 \times 10^{-3}(4) = \mathbf{1.11 \text{ mA}}$$

p-Channel Enhancement-Type MOSFETs

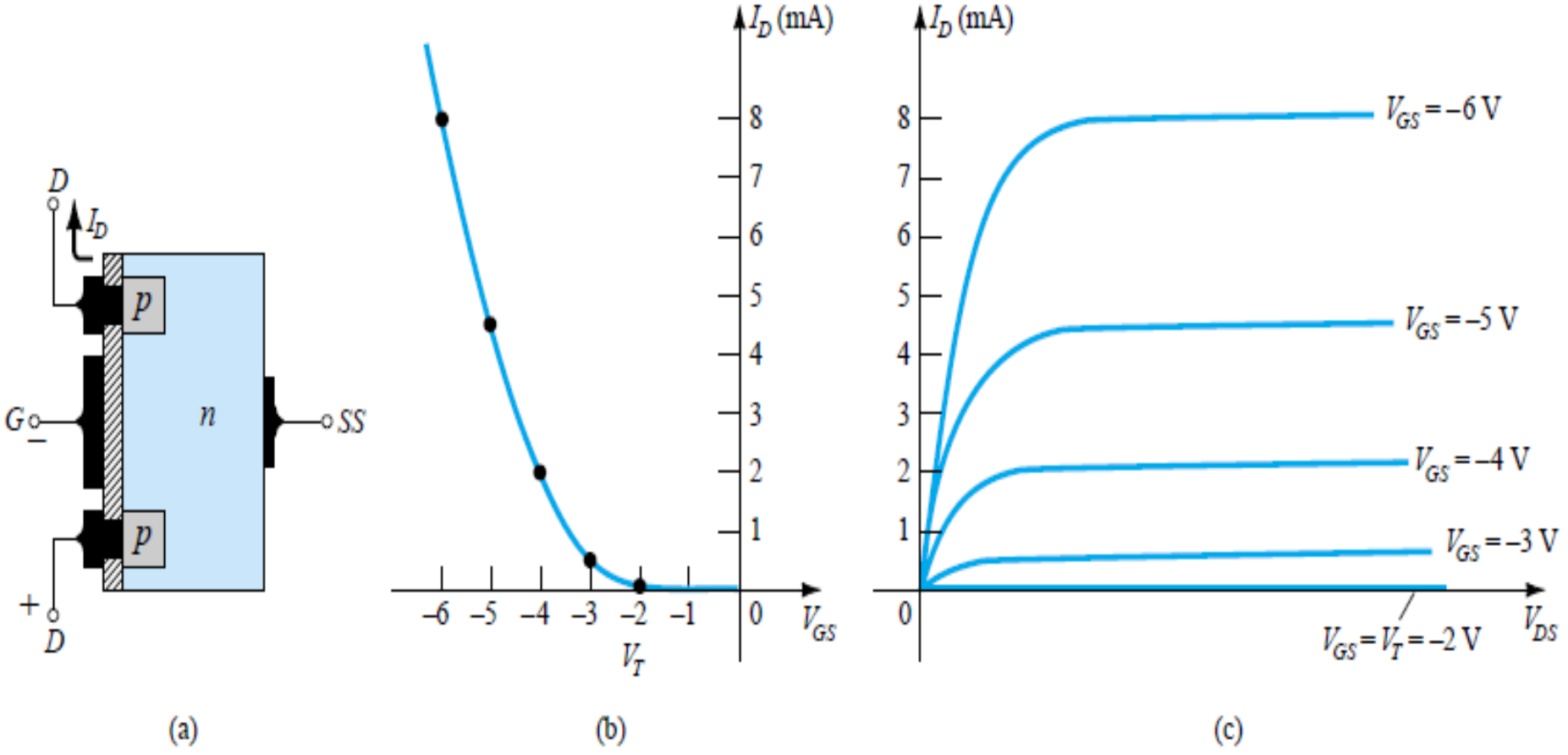


Figure 5.37 *p*-Channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.5 \times 10^{-3}$ A/V^2.

Example 2

The datasheet (see www.fairchild.com) for a 2N7002 E-MOSFET gives $I_{D(on)} = 500$ mA (minimum) at $V_{GS} = 10$ V and $V_{GS(th)} = 1$ V. Determine the drain current for $V_{GS} = 5$ V.

Solution

First, solve for K using Equation 8–4.

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{500\text{ mA}}{(10\text{ V} - 1\text{ V})^2} = \frac{500\text{ mA}}{81\text{ V}^2} = 6.17\text{ mA/V}^2$$

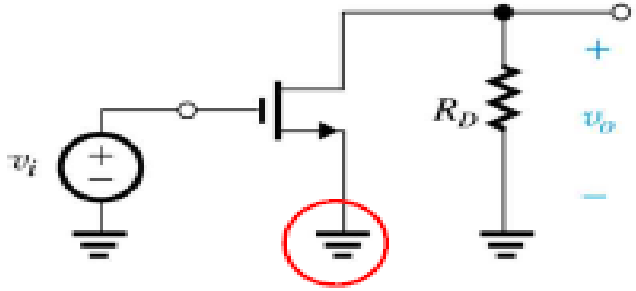
Next, using the value of K, calculate I_D for $V_{GS} = 5$ V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17\text{ mA/V}^2)(5\text{ V} - 1\text{ V})^2 = \mathbf{98.7\text{ mA}}$$

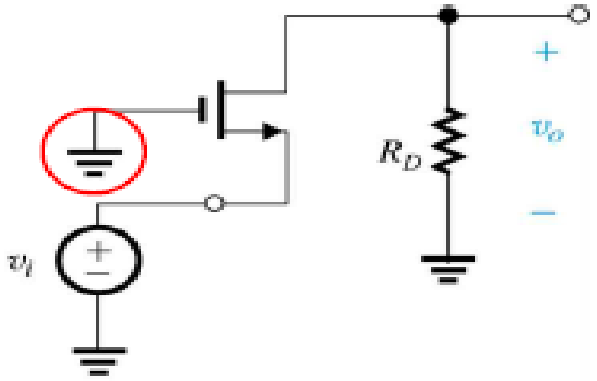
The datasheet for an E-MOSFET gives $I_{D(on)} = 100$ mA at $V_{GS} = 8$ V and $V_{GS(th)} = 4$ V. Find I_D when $V_{GS} = 6$ V.

MOSFET amplifier configurations

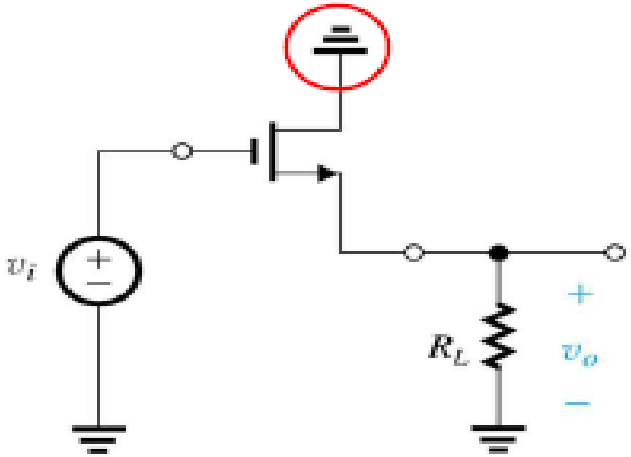
- Three Basic configurations



(a) Common Source (CS)



(b) Common Gate (CG)



(c) Common Drain (CD) *Source follower*

Comparison

Table 11-1 Comparison of common-source, common-drain, and common-gate circuits.

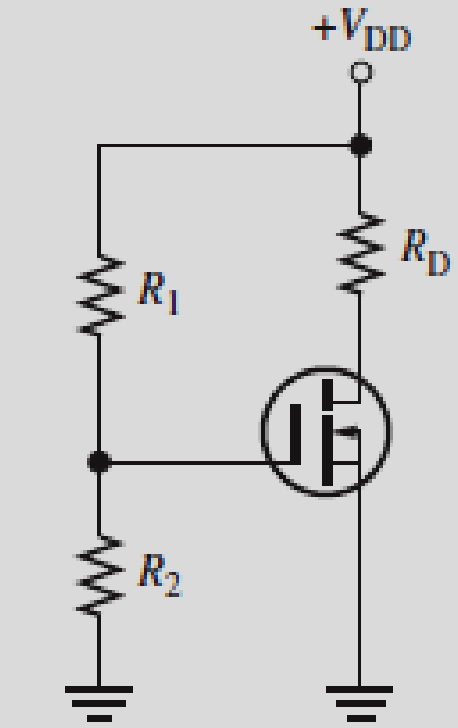
Circuit configuration	Z_i	Z_o	A_v	Phase shift
CS	$\approx R_G$	$\approx R_D$	$-Y_{fs}(R_D \| R_L)$	180°
CD	$\approx R_G$	$\approx 1/Y_{fs}$	≈ 1	0
CG	$\approx 1/Y_{fs}$	$\approx R_D$	$Y_{fs}(R_D \| R_L)$	0

Summary

- Common-Source (*CS*) configuration
  - best suited for the *bulk of gain*
- Common-Source (*CS*) configuration with *Rs* in the source
  - improved performance but *reduced* gain
- Common-Gate (*CG*) configuration
  - low input resistance
  - excellent high-frequency performance
  - unity-gain current amplifier
  - *cascode amplifier*
- Common-Drain (*CD*) or *Source follower*
  - *voltage buffer* for connecting a high-resistance source to
  - a low –resistance load
  - output stage in a multi-stage amplifier

Biasing Technique

- Voltage Divider Bias
  - E-MOSFETs must have a *V*GS >*V*GS(th),



(a) Voltage-divider bias

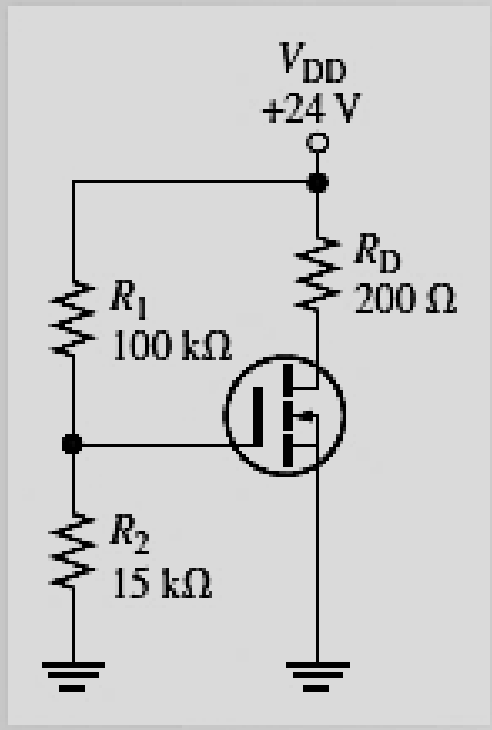
$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$

$$V_{DS} = V_{DD} - I_D R_D$$

Example 2:

Determine V_{GS} and V_{DS} for the E-MOSFET circuit in Figure 8–47. Assume this particular MOSFET has minimum values of $I_{D(on)} = 200$ mA at $V_{GS} = 4$ V and $V_{GS(th)} = 2$ V.

▶ FIGURE 8–47



For the E-MOSFET in Figure 8–47, the gate-to-source voltage is

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{15\,\text{k}\Omega}{115\,\text{k}\Omega}\right)24\,\text{V} = 3.13\,\text{V}$$

To determine V_{DS}, first find K using the minimum value of $I_{D(on)}$ and the specified voltage values.

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{200\,\text{mA}}{(4\,\text{V} - 2\,\text{V})^2} = \frac{200\,\text{mA}}{4\,\text{V}^2} = 50\,\text{mA/V}^2$$

Now calculate I_D for $V_{GS} = 3.13$ V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (50\,\text{mA/V}^2)(3.13\,\text{V} - 2\,\text{V})^2$$
$$= (50\,\text{mA/V}^2)(1.13\,\text{V})^2 = 63.8\,\text{mA}$$

Finally, calculate V_{DS}.

$$V_{DS} = V_{DD} - I_D R_D = 24\,\text{V} - (63.8\,\text{mA})(200\,\Omega) = 11.2\,\text{V}$$

Determine V_{GS} and V_{DS} for the circuit in Figure 8–47 given $I_{D(on)} = 100$ mA at $V_{GS} = 4$ V and $V_{GS(th)} = 3$ V.

Example 3:

The datasheet (see www.fairchild.com) for a 2N7002 E-MOSFET gives $I_{D(on)} = 500$ mA (minimum) at $V_{GS} = 10$ V and $V_{GS(th)} = 1$ V. Determine the drain current for $V_{GS} = 5$ V.

First, solve for K using Equation 8–4.

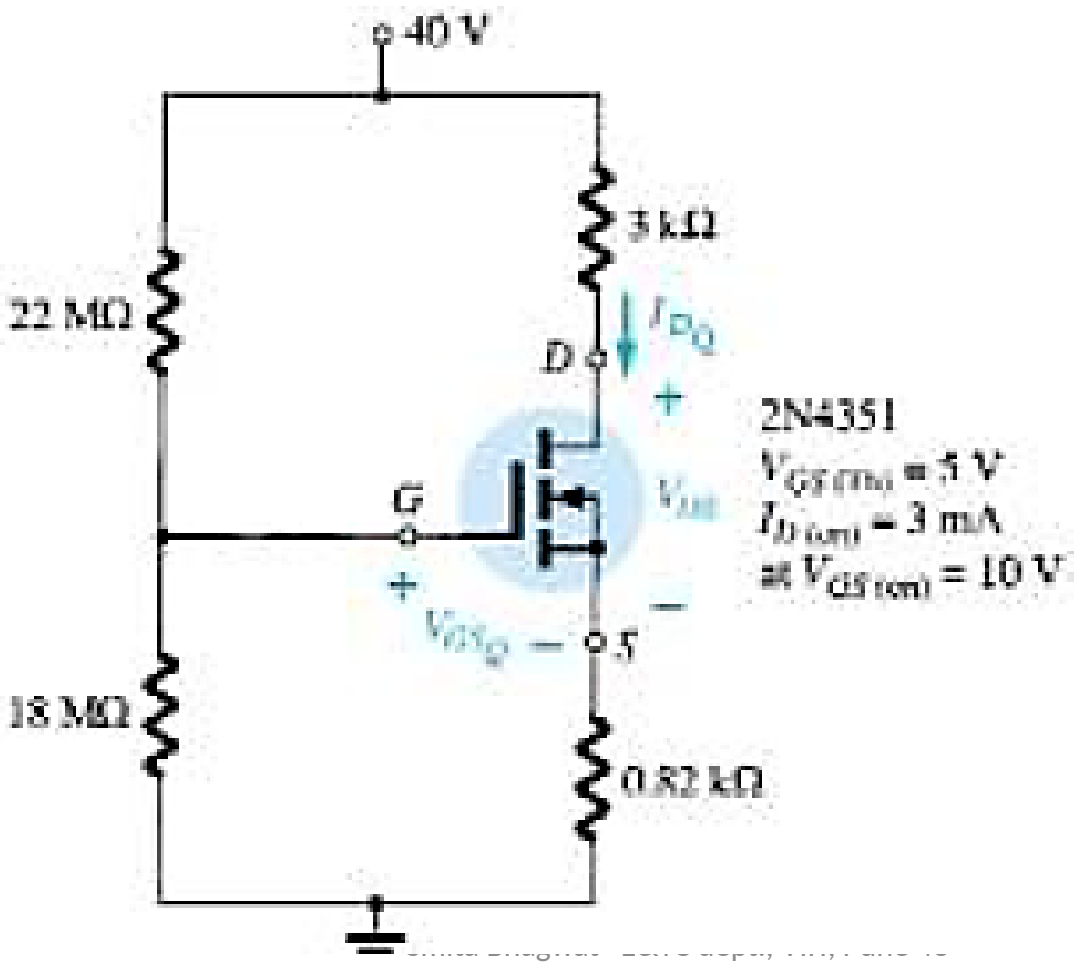
$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{500\,\text{mA}}{(10\,\text{V} - 1\,\text{V})^2} = \frac{500\,\text{mA}}{81\,\text{V}^2} = 6.17\,\text{mA/V}^2$$

Next, using the value of K, calculate I_D for $V_{GS} = 5$ V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17\,\text{mA/V}^2)(5\,\text{V} - 1\,\text{V})^2 = 98.7\,\text{mA}$$

Example 4:

Determine I_{DQ}, V_{GSQ}, and V_{DS} for the network of Fig. 6.43.



$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\ \text{M}\Omega)(40\ \text{V})}{22\ \text{M}\Omega + 18\ \text{M}\Omega} = 18\ \text{V}$$

$$V_{GS} = V_G - I_D R_S = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

When $I_D = 0$ mA,

$$V_{GS} = 18\ \text{V} - (0\ \text{mA})(0.82\ \text{k}\Omega) = 18\ \text{V}$$

as appearing on Fig. 6.44. When $V_{GS} = 0$ V,

$$V_{GS} = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

$$0 = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

$$I_D = \frac{18\ \text{V}}{0.82\ \text{k}\Omega} = 21.95\ \text{mA}$$

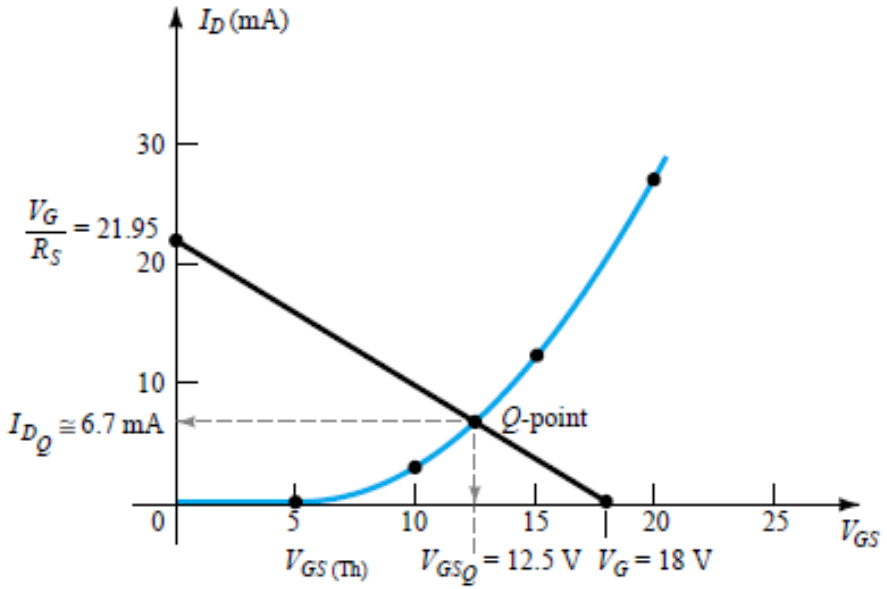


Figure 6.44 Determining the *Q*-point for the network of Example 6.12.

$V_{GS(Th)} = 5\ \text{V}, \qquad I_{D(on)} = 3\ \text{mA with } V_{GS(on)} = 10\ \text{V}$

Eq. (6.26): $$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

$$= \frac{3\ \text{mA}}{(10\ \text{V} - 5\ \text{V})^2} = 0.12 \times 10^{-3}\ \text{A/V}^2$$

$$I_D = k(V_{GS} - V_{GS(Th)})^2$$

$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

$$I_{DQ} \cong \mathbf{6.7\ mA}$$

$$V_{GSQ} = \mathbf{12.5\ V}$$

Eq. (6.33): $$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

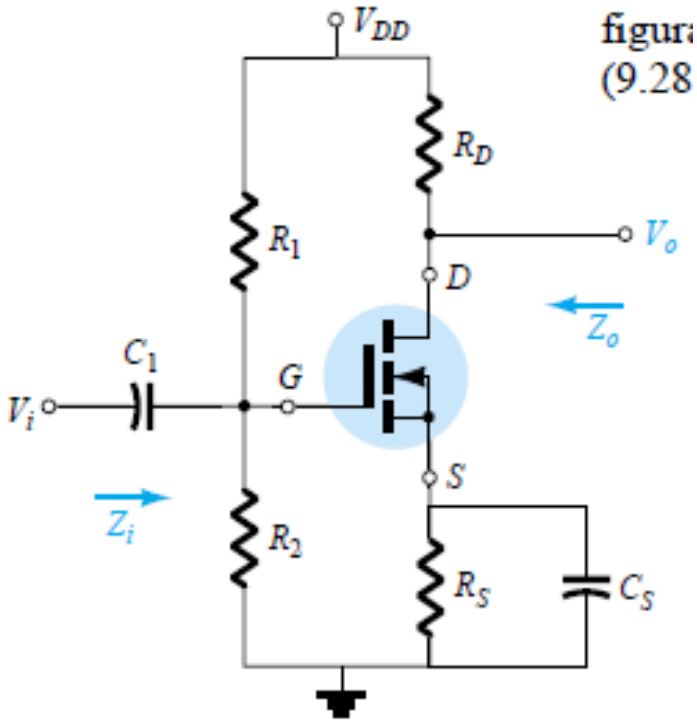
$$= 40\ \text{V} - (6.7\ \text{mA})(0.82\ \text{k}\Omega + 3.0\ \text{k}\Omega)$$

$$= 40\ \text{V} - 25.6\ \text{V}$$

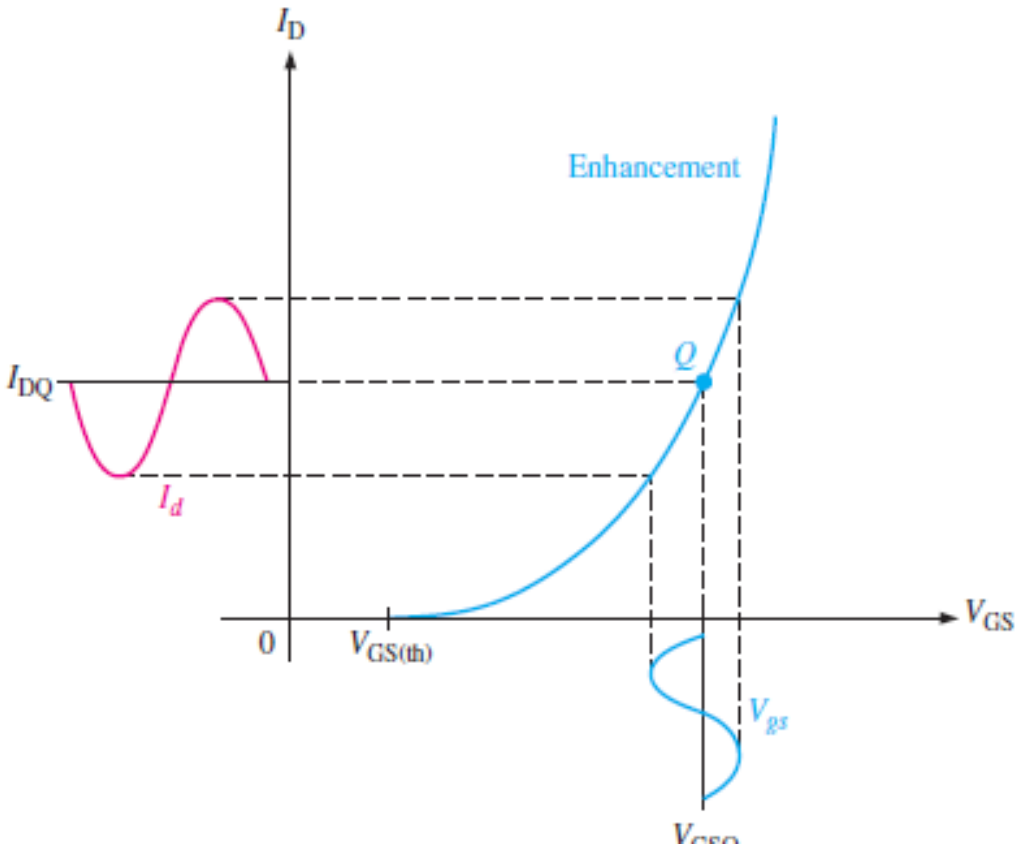
$$= \mathbf{14.4\ V}$$

E-MOSFET CS AMPLIFIER

- A common-source *n*-channel E-MOSFET with voltage-divider bias with an ac source capacitive coupled to the gate.
- The gate is biased with a positive voltage such that *V*GS > *V*GS(th).



- The signal voltage produces a swing in *Vgs* above and below its Q-point value, *V*GSQ.
- This, in turn, causes a swing in *Id* above and below its Q-point value, *I*DQ, as illustrated in



he enhancement

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

$$V_{DS} = V_{DD} - I_D R_D$$