RUPAM SEN

Digital Design Engineer @Vervesemi Microelectronics
Email: *rupam9815@gmail.com* Contact No.: +91-9051410144/8240241792
LinkedIn ID: *https://www.linkedin.com/in/rupam-sen-19007221b/* Bengaluru, Karnataka, India

WORK EXPERIENCE

VERVESEMI MICROELECTRONICS [RTL Design Engineer] **October, 2023 – Present**

- Working with PULPissimo Microprocessor. Designed the interface for RAM. Developing a custom block to convert the JTAG data into SPI data frame, and program this data in SPI Flash memory. The purpose of this project is to enhanced the efficiency of boot loading process.
- Developed RTL for I2C Master and Slave blocks as per STM32 datasheet. It supports 7-bit/10-bit address mode, enable dual address mode (7-bit), repeating start condition, different I2C modes. Developed SV Testbench for Functional Verification, and employed constraint randomization for robust verification.
- Training Project: Designed Verilog HDL based SPI Slave block to support all the testcases in the test plan, execute Functional Verification; Worked on Synthesis flow and verify the design in Gate Level Simulation.

CADENCE DESIGN SYSTEMS [Product Validation Intern] **Aug,2022 – July,2023 (11 months)**

- Worked with Mixed-Signal Product Validation team (Xcelium) as an Intern from August 2022 to July 2023 at Cadence Design Systems, Bengaluru.
- Received comprehensive training and experience on the SV-AMS, Wreal, and RNM techniques.
- Experienced on - Daily regression analysis; Finding the root cause of the failed regression testcases and debugging; the version control system - Perforce.

TECHNICAL SKILL

- **HDL/HVL –** Verilog, System Verilog, Verilog-AMS, UVM
- **Communication Protocols –** UART, I2C, SPI, APB, AXI
- **Programming & Scripting language –** C/C++, Python, Perl, Shell, Makefile
- **EDA Tools –** Xcelium Simulator, Xilinx Vivado, Virtuoso, EDA Playground

PROJECTS

- **Design and Verification of APB_RAM using UVM.**
  The purpose of this project is to understand the APB protocol. Designed a RAM which use APB protocol for write and read operation. Verified the design by using UVM based testbench.

- **Design and Verification of Smart Traffic Light Controller using UVM.**
  In this project a smart traffic light controller is designed using Finite State Machine, which control the traffic signal based on the congestion on the road. Developed UVM based testbench and successfully verified the functionality of the DUT.

- **Tool Used:** Xcelium Simulator
- **GitHub Link:** *https://github.com/RupamSen?tab=repositories*

EDUCATION

Master of Technology [Communication Systems]	*Motilal Nehru National Institute of Technology* (MNNIT), Allahabad	CPI – 9.1/10	2021 - 2023
Bachelor of Technology [ECE]	University of Calcutta – *Institute of Radio Physics and Electronics* (IRPE), Kolkata	8.76/10	2018 - 2021
Bachelor of Science [Physics (Honors)]	University of Calcutta – *Seth Anandram Jaipuria College*, Kolkata	62.37%	2015 - 2018