# **RUPAM SEN**

Digital Design Engineer [RTL] @Vervesemi Microelectronics

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Bengaluru, Karnataka, India

#### **WORK EXPERIENCE**

### **VERVESEMI MICROELECTRONICS [RTL Design Engineer]**

October, 2023 - Present

- ➤ Developed RTL for I2C as per STM32 datasheet.
- > Designed SPI Slave as per given specification as training task, developed testbench, and worked on Synthesis.
- Working on PULPissimo Microprocessor.

# **CADENCE DESIGN SYSTEMS [ Product Validation Intern]**

Aug, 2022 - July, 2023 (11 months)

- ➤ Worked with Mixed-Signal Product Validation team as an Intern from August 2022 to July 2023 at Cadence Design Systems, Bengaluru.
- Received comprehensive training and experience on the SV-AMS, Wreal, and RNM techniques.
- ➤ Daily regression analysis; Debugging the failed testcases and finding root cause of failure regression testcases; work experience in Perforce area.

#### TECHNICAL SKILL

- HDL Verilog, System Verilog, Verilog-AMS
- **Programming & Scripting language –** C/C++, Python, Perl, Shell, Makefile
- Software Xcelium Simulator, Simvision, Virtuoso, EDA Playground, Xilinx Vivado

# **PROJECT**

### Verilog HDL Project [Personal Project]

- Modelled 64-byte depth Synchronous FIFO & Create Verification Environment.
- Smart Traffic Light controller using Finite State Machine, which senses the congestion on the road and accordingly control the traffic signal.

GitHub Link: https://github.com/RupamSen?tab=repositories

## **EDUCATION**

| Master of Technology<br>[Communication Systems] | Motilal Nehru National Institute of<br>Technology (MNNIT), Allahabad                       | CPI - 9.1/10      | 2021 - 2023 |
|---|--|-------------------|-------------|
| Bachelor of Technology<br>[ECE]                 | University of Calcutta – <i>Institute of Radio Physics and Electronics</i> (IRPE), Kolkata | 8.76/10<br>81.97% | 2018 - 2021 |
| Bachelor of Science<br>[Physics (Honours)]      | University of Calcutta – Seth Anandram Jaipuria<br>College, Kolkata                        | 62.37%            | 2015 - 2018 |
| Class XII                                       | Pannalal Institution, Kalyani, WB (WBCHSE)   | 87.8%             | 2015        |
| Class X   | Chatra Ganesh Lal High School, Birbhum, WB(WBBSC)  | 85%               | 2013        |

#### **Achievements**

- Achieved AIR 3302 and score 474 in GATE 2021 conducted by IIT Bombay. (Paper Electronics & Communication)
- Qualify JAM 2018 conducted by IIT Bombay. (Paper Physics)