Zoubin Bi

Tel: +86153-3653-9133 | E-mail: bzb@zju.edu.cn | Github: https://github.com/RupertPaoZ

Education

Zhejiang University
M.Sc of Software Engineering — *Sep. 2022 – Mar. 2025 (expected)*

Zhejiang University
B.Eng of Computer Science — *Aug. 2018 – Jun. 2022*

Experience

Research Assistant
State Key Lab of CAD&CG, Zhejiang University, China — *Sep. 2022 – Present.*

- Research Topic: Compressive sensing and optical system calibration.
- Co-design and co-optimize software-hardware to accelerate geometry acquisition and reconstruction.
- Advisor: Prof. Hongzhi Wu.

Bachelor Thesis
State Key Lab of CAD&CG, Zhejiang University, China — *Sep. 2021 – Apr. 2022*

- Research Topic: Boost local feature matching with global information.
- Advisor: Prof. Hongzhi Wu.

Research

Differentiable Dynamic Visible-Light Tomography
Research Paper (https://svbrdf.github.io/publications/dynamicCT/project.html)

- Joint first-authored paper accepted to **SIGGRAPH Asia 2023**.
- Proposed the first visible-light tomography system for real-time acquisition and reconstruction of general temporally-varying 3D phenomena.
- Proposed a novel differentiable framework to map both tomography acquisition and reconstruction to an autoencoder.
- Built a prototype hardware using fibers and LED arrays, and developed corresponding calibration method.

Real-time Acquisition and Reconstruction of Dynamic Volumes with Neural Structured Illumination
Research Paper

- Joint first-authored paper under review at **CVPR 2024**.
- Proposed a novel framework for real-time acquisition and reconstruction of temporally-varying 3D phenomena with high quality.
- Demonstrated the effectiveness of the framework on a lightweight setup with an off-the-shelf projector, and developed a complete calibration algorithm.

Projects

Computor Cluster
A Small-Scale Computer Cluster for Research — *Mar. 2023 – Apr. 2023*

- Set up a computer cluster by NIS and NFS.
- Use ansible to make server maintenance more efficient and more convenient.
- Achieved consistent environment and 10 Gbps speed across different nodes.

Self-design CPU
ZJU 2020 Computer Architecture Project — *Sep. 2020 – Jan. 2021*

- Desighed a five-stage pipeline using RISC-V Arch as one of the first five students attempting to explore RISC-V Arch at Zhejiang University.
- Designed a L2-cache for this pipeline.

Technical Skills

Languages: C/C++, Python, Java, Golang
Web Development: Echo, RestAPI, PostgreSQL, MySQL, Postman
Computer Graphics & Computer Vision: OpenGL, OpenCV
Data Science, Machine Learning & Deep Learning: NumPy, PyTorch, Pandas, SkLearn
Electronic Design & Embedded Systems: Verilog, RISC-V, ZYNQ, Arduino
System Maintanence: Linux, Docker, Ansible
Tools: Git, GDB, Latex, VS Code, Visual Studio