

# Class Test - 1 (Odd Semester 2021- 22)

Course Name - Advanced Computer Architecture

Course Code - PEC-702B

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Course Code \*

PEC-702B ▼

Course Name \*

Advanced Computer Architecture ▼

1. In which processor, loop control overhead is minimized? \*

- ☐ Scalar Processor
- ☒ Vector Processor
- ☐ IAS Processor
- ☐ Multiprocessor

2. Number of instructions is less in \*

- ☒ Scaler Program
- ☐ Vector Program
- ☐ It cannot be said
- ☐ Equal in both scalar and vector.



3. Number of scaler quantity in a vector is called \*

- ☒ Length
- ☐ Stride
- ☐ Format
- ☐ Number

4. Which of the following is the first field in vector instruction format? \*

- ☐ Base Address
- ☐ Address Offset
- ☒ Op-Code
- ☐ Vector Length

5. Scaler-Vector Product is a \_\_\_\_\_ operation. \*

- ☐ Unary
- ☐ Binary
- ☐ Ternary
- ☒ All of the above types

6. Starting address is also known as \*

- ☐ Address Offset
- ☒ Base Address
- ☐ Displacement
- ☐ None of these



7. A compiler that converts a scalar instruction into corresponding vector instruction is known as \*

- ☐ DSP
- ☐ Analog Compiler
- ☐ GCC Compiler
- ☒ Vectorizing Compiler

8. Vector addition is an example of \_\_\_\_\_ operation \*

- ☐ Unary
- ☒ Binary
- ☐ Ternary
- ☐ None of these

9. If  $UVL > MVL$ , then the problem is known as \*

- ☐ Strip Mining
- ☐ Vector Fitting
- ☐ Vector Filling
- ☐ Vector Mining



10. Vector Stride value is used to access\_\_\_\_\_ vectors. \*

- ☐ One Dimensional
- ☐ Two Dimensional
- ☐ Three Dimensional
- ☒ Multidimensional

11. Which one stores the starting address of next instruction? \*

- ☒ PC
- ☐ SP
- ☐ AC
- ☐ DR

12. Which of the following stores the address of top element of the stack? \*

- ☐ PC
- ☐ AC
- ☒ SP
- ☐ Any Register

13. Which of the following gives  $CPI < 1$ ? \*

- ☐ Array Processor
- ☒ VLIW
- ☐ Vector Processor
- ☐ Scalar Processor



14. Which of the following is not a data hazard? \*

- ☒ RAR
- ☐ RAW
- ☐ WAR
- ☐ WAW

15. Solution of control hazard is \*

- ☐ Strip Mining
- ☐ Vector Fitting
- ☐ Prefetching
- ☐ None of these

16. Which particular stage in instruction cycle is used by ALU? \*

- ☐ IF
- ☐ ID
- ☐ OF
- ☒ EX

17. Which of the following has multiple output? \*

- ☒ Linear Pipelining
- ☐ General Pipelining
- ☐ NOT Gate
- ☐ None of these



18. Which one is also called as Omega network? \*

- ☐ Single stage Shuffle-Exchange interconnection network
- ☒ Multi stage Shuffle-Exchange interconnection network
- ☐ Single stage cube interconnection network
- ☐ Multi stage cube interconnection network

19. If  $T$  = Clock period and  $f$  = Clock frequency, then which statement is true? \*

- ☐  $T = f$
- ☒  $T = 1/f$
- ☐  $T = 2f$
- ☐  $f = 2T$

20. In mesh connected ILLIAC network, number of PE are \*

- ☐ 4
- ☐ 16
- ☐ 32
- ☒ 64

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