CMOS and 10-T PTL Full Adder

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***Abstract*—Approx all the digital circuits contains an arithmetic circuit which is made up of so many full adders. Leakage power reduction and area have become important factors in designing different large circuits. Generally a static CMOS Full Adder is made of 28 Transistors In this lab exercise a low power 10T full adder is designed using complementary pass transistor technology.**

I. Introduction

Designing low power circuits has become important to increase the battery life of digital electronic devices, Thus reducing power consumption of these circuits is important. Full adders are prominent because they are the basic building blocks of many circuits.

II. Theory

The full-adder extends the concept of the half-adder by providing an additional carry-in (Cin) input, as shown in Figure. This is a design with three inputs (A, B, and Cin) and two outputs (Sum and Cout). This cell adds the three binary input numbers to produce sum and carry-out terms.

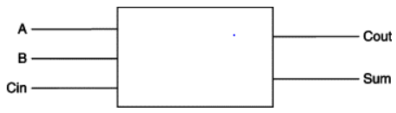


Fig-1: A FA block

The Gate level design and Truth table CMOS of a Full adder is given–

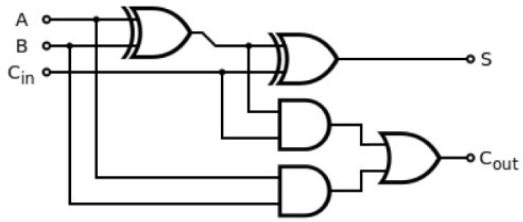


Fig-2: Gate level design of Full adder

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig-3: Truth Table of Full Adder

From the truth table, we can write the boolean expression for the Sum and Carry output.

$$S = A(xor)B(xor)Cin \tag{1}$$

$$Cout = (AB)|(BCin)|(CinA) \tag{2}$$

For adding two number of more than one bit, we use different types of full adders like serial and parallel adder. In which parallel adders are more speed efficient like Carry look ahead adder, Ripple carry adder,etc.

III. Results and Inferences

A. *Design of 28T static CMOS Full Adder*

Schematic below shows a Full adder designed using 28 transistors in which 12 transistors are used to generate Cout and 16 transistors are used to generate Sum output. Just to compare up the noise margin for symetrical VTC, i have given the width of all the PMOS to be 440 nm and the width of NMOS is 200nm. As the CMOS logic is naturally inverting logic. To make it non-inverting I connected one extra inverter to the output of transistor.

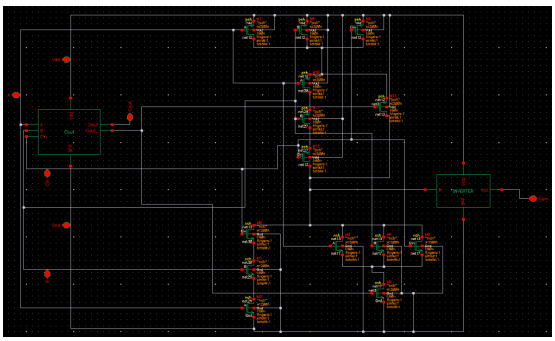


Fig-4: CMOS 28T FA schematic

Schematic below shows a design of Cout circuit that uses 12 transistors.

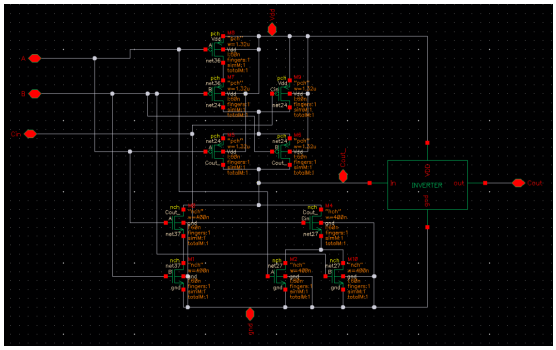


Fig-5: CMOS COUT schematic of FA

Schematic below shows testbench for Full adder to get output for different input patterns.

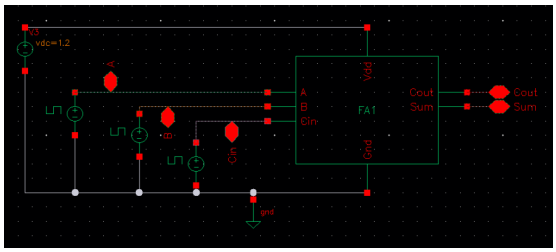


Fig-6: CMOS FA testbench

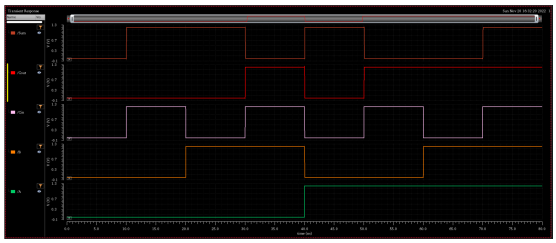


Fig-7: Simulated Transient response of 28T based Full Adder

- For different input patterns, the output of the proposed full adder circuit varies. Simulation has been performed for all possible input patterns.

B. PTL Based design of 10T adder (Using 4T XOR and 2T Mux.

Schematic shown below shows design of a Full adder using 10 transistor only. It is designed by using two XOR gates and a multiplexer. The XOR gate was designed using two NMOS transistors and two PMOS transistors. The multiplexer was implemented using one PMOS and one NMOS transistor.The circuit is designed using complementary pass transistor logic.

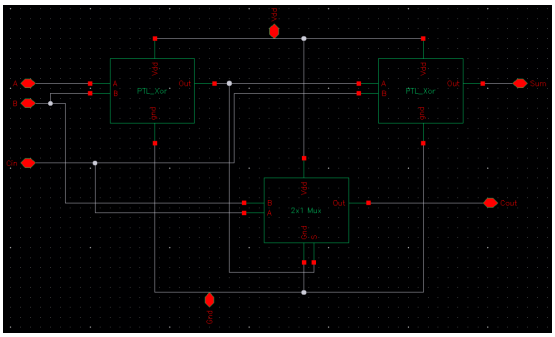


Fig-8: PTL fa circuit

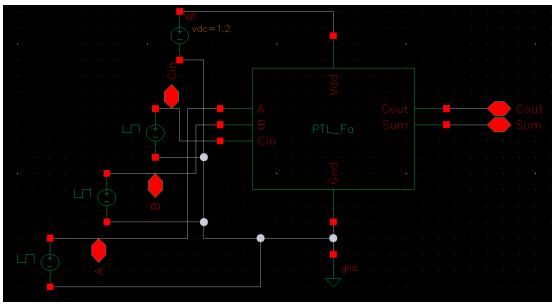


Fig-9: PTL based Full Adder Testbench

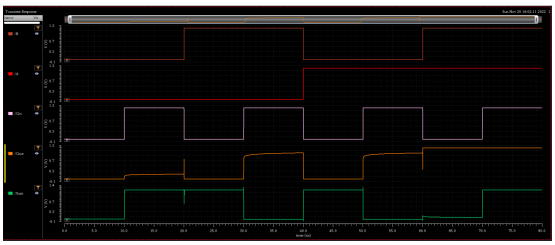


Fig-10: Simulated Transient response of 10T based Full Adder

- With reduction in power consumption of l0T full adder, large systems whose performance is dependent on full adders could be built leading to extended battery life for portable devices. The reduction in the area used by the proposed l0T full adder also signifies the miniaturization of the system.
- As we know that the problem with the Pass Transistor Logic is as it designed using only NMOS, it can not pull the output to the VDD, rather VDD-Vth. But NMOS can produce a perfect zero. So, we do not get a perfect noise margin.
- The second problem that we can observe is that the circuit undergoes a lot of body effect because there is a source to body voltage when ever pulling high.

IV. Verilog design of a 4-bit multiplier

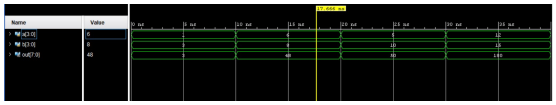
A. *Verilog code-*

```
`timescale 1ns / 1ps

module multiplier(a,b,out);
    input [3:0] a,b;
    output [7:0] out;

assign out = a*b;

endmodule
```

B. *Testbench code -*

```
`timescale 1ns / 1ps


module multiplier_tb;
    reg [3:0]a,b;
    wire [7:0] out;

multiplier DUT (a, b, out);
initial
  begin
    a=4'b0001; b=4'b0011;
    #10 a=4'b0110; b=4'b1000;
    #10 a=4'b0101; b=4'b1010;
    #10 a=4'b1100; b=4'b1111;
    #10

    $finish();


  end
endmodule
```

C. *Simulation of the multiplier -*



V. Conclusion

- Single bit 10 transistor full adder is designed. Complementary Pass Transistor Logic has been used to build the circuit. Area and Power dissipation of the Circuit is reduced compared to the conventional 28T full adder.

VI. References

- Digital Integrated Circuit: A design perspective by Jan M.Rabaey
- https://eepower.com/technical-articles/basic-cmos-logic-gates/
- https://www.electronics-tutorial.net/Digital-CMOS-Design/CMOS-Layout-Design/Layout-Design-Rules/