Design and Implementation of Sense Amplifier

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***Abstract*—In this Assignment Exercise We Design and Implemented Sense Amplifier Based Edge-Triggered Register in 130 nm-CMOS process.**

I. Introduction

Sense amplifiers are one of the most essential circuits in the CMOS memories that plays an important role to reduce the overall sensing delay and voltage. Sense-amplifier circuits accept small input signals and amplify them to generate rail-to-rail swings. Sense amplifier circuits are used extensively in memory cores and in low swing bus drivers to amplify small voltage swings present in heavily loaded wires.

II. Theory

There are many techniques to construct these amplifiers, we designed it with the use of feedback (cross-coupled inverters). The circuit shown in Figure below uses a precharged front-end amplifier that samples the differential input signal on the rising edge of the clock signal. The outputs of front-end are fed into a NAND cross-coupled SR FF that holds the data and guarantees that the differential outputs switch only once per clock cycle. The differential inputs in this implementation don't have to have rail-to-rail swing and hence this register can be used as a receiver for a reduced swing differential bus.

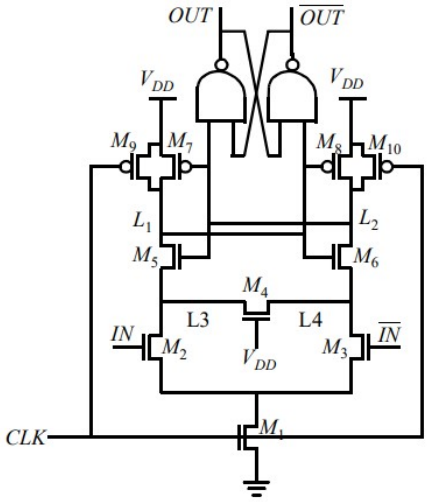


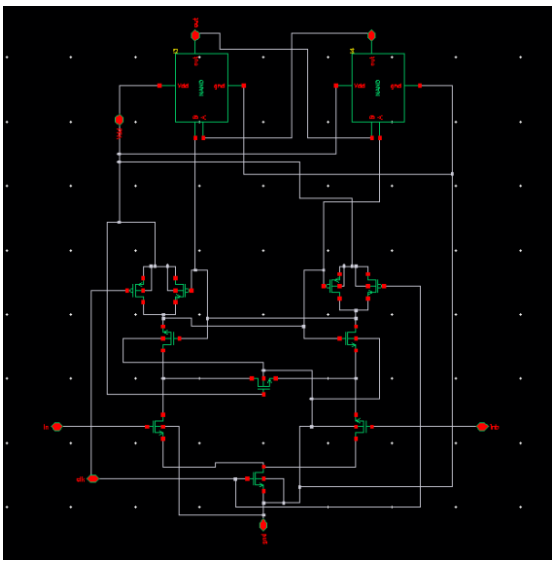
Fig-1: Positive edge-triggered register based on sense-amplifier.

Circuit schematic consists of a cross-coupled inverter (M5 - M8), whose outputs (L1 and L2) are precharged using devices M9 and M10 during the low phase of the clock. As a result, PMOS transistors M7 and M8 to be turned off and the NAND flip flop is holding its previous state. Transistor M1 is similar to an evaluate switch in dynamic circuits and is turned off ensuring that the differential inputs don't affect the output during the low phase of the clock. On the rising edge of the clock, the evaluate transistor turns on and the differential input pair (M2 and M3) is enabled, and the difference between the input signals is amplified on the output nodes on L1 and L2. The cross-coupled inverter pair flips to one of its the stable states based on the value of the inputs. For example, if IN is 1, L1 is pulled to 0, and L2 remains at VDD. Due to the amplifying properties of the input stage, it is not necessary for the input to swing all the way up to VDD and enables the use of low swing signaling on the input wires.

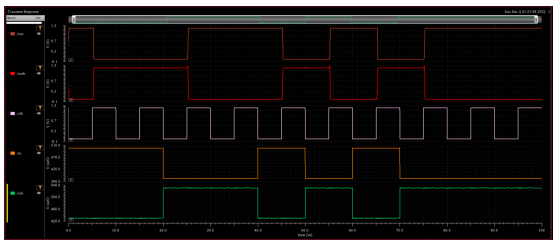
III. Implementation of Sense Amplifier

A. *Schematics of Sense Amplifier:*

Total total number of transistors used in the sense amplifier is 10 + 8(NAND Gate) = 18 transistors.

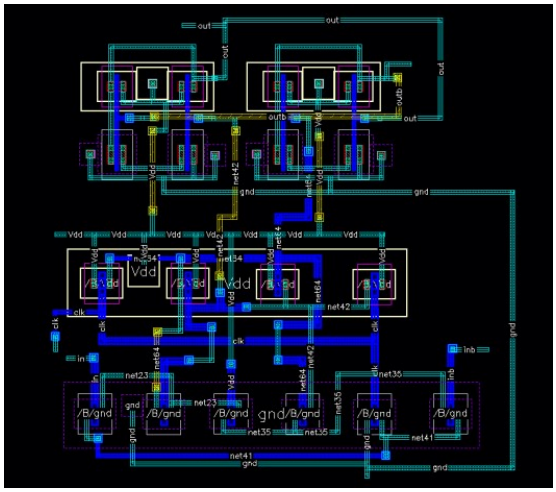


B. *Simulation of Sense Amplifier:*



- Input Signal volatage given in this design is 400mV for logic 0 and 500mV for logic 1.
- Input Compliment Signal voltage given in this design is 430mV for logic 0 and 530mV for logic 1.
- We can see from this plot that, despite the low voltage difference between IN and INbar, the rail-to-rail swing at the output is around 1.2V (1.199V - 49uV).

C. *Layout of Sense Amplifier:*



IV. Conclusion

Approx all the big circuits like processors and so on consists of thousands of registers. So, we need the register to be high speed, power efficient, and made of less hardware as possible. Sense amplifier based register gives better performance and a good way of designing an edge triggered register but as we have seen it takes more number of transistor as compared to that of the master-slave technique.

V. References

Digital Integrated Circuits (2nd Edition) by Jan M. Rabaey
CMOS Invertor and STA concept