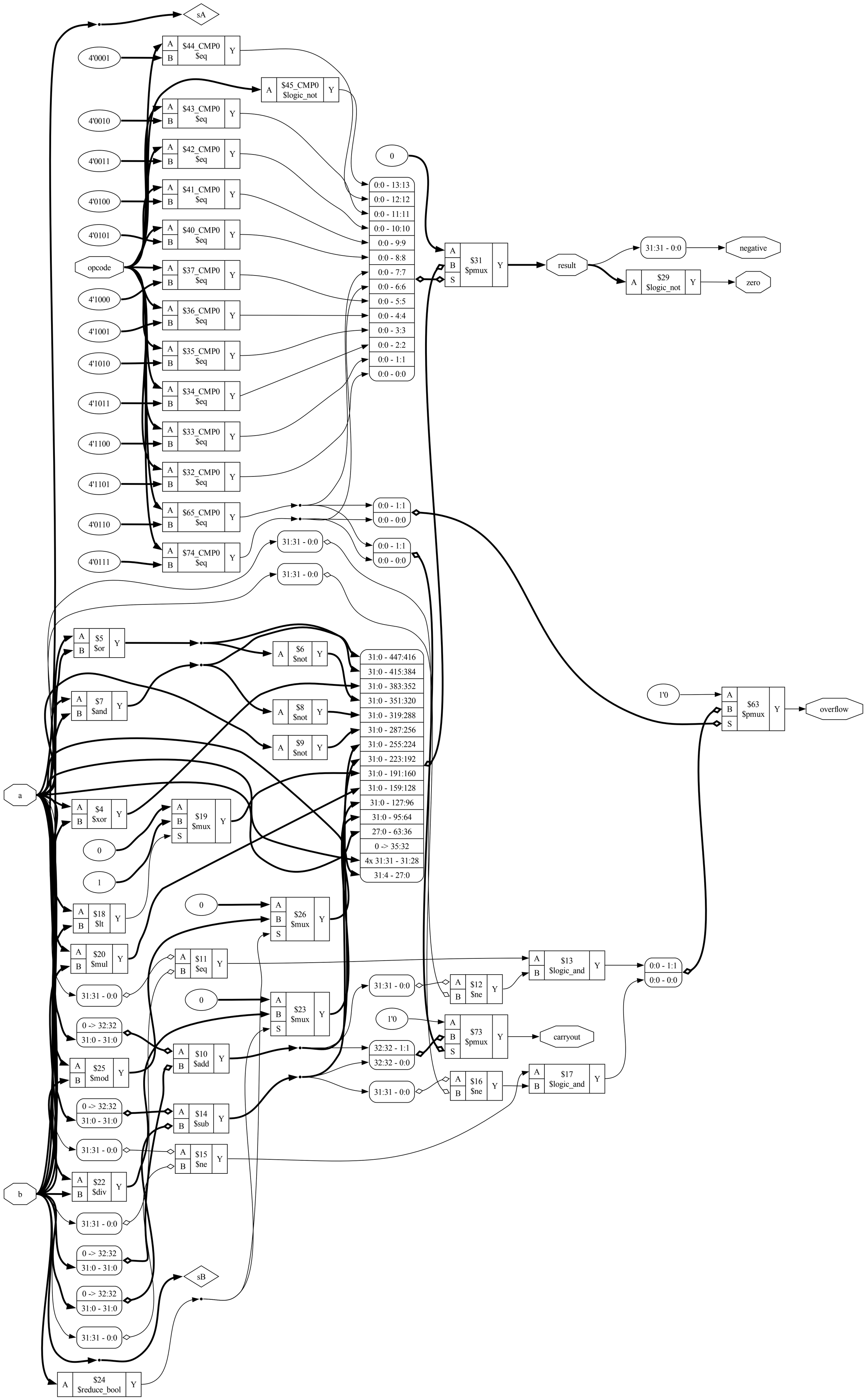
sA
4'0001
4'0010
4'0011
4'0100
4'0101
opcode
4'1000
4'1001
4'1010
4'1011
4'1100
4'1101
4'0110
4'0111
$44_CMP0 $eq
$45_CMP0 $logic_not
$43_CMP0 $eq
$42_CMP0 $eq
$41_CMP0 $eq
$40_CMP0 $eq
$37_CMP0 $eq
$36_CMP0 $eq
$35_CMP0 $eq
$34_CMP0 $eq
$33_CMP0 $eq
$32_CMP0 $eq
$65_CMP0 $eq
$74_CMP0 $eq
0
0:0 - 13:13
0:0 - 12:12
0:0 - 11:11
0:0 - 10:10
0:0 - 9:9
0:0 - 8:8
0:0 - 7:7
0:0 - 6:6
0:0 - 5:5
0:0 - 4:4
0:0 - 3:3
0:0 - 2:2
0:0 - 1:1
0:0 - 0:0
$31 $pmux
result
31:31 - 0:0
negative
$29 $logic_not
zero
31:31 - 0:0
31:31 - 0:0
$5 $or
$6 $not
$7 $and
$8 $not
$9 $not
31:0 - 447:416
31:0 - 415:384
31:0 - 383:352
31:0 - 351:320
31:0 - 319:288
31:0 - 287:256
31:0 - 255:224
31:0 - 223:192
31:0 - 191:160
31:0 - 159:128
31:0 - 127:96
31:0 - 95:64
27:0 - 63:36
0 -> 35:32
4x 31:31 - 31:28
31:4 - 27:0
1'0
$63 $pmux
overflow
a
$4 $xor
$19 $mux
0
1
$18 $lt
$26 $mux
$20 $mul
$11 $eq
$13 $logic_and
31:31 - 0:0
$12 $ne
0:0 - 1:1
0:0 - 0:0
$23 $mux
1'0
$73 $pmux
carryout
0 -> 32:32
31:0 - 31:0
$10 $add
32:32 - 1:1
32:32 - 0:0
$25 $mod
$16 $ne
$17 $logic_and
$14 $sub
$15 $ne
$22 $div
b
sB
$24 $reduce_bool

ALU