INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR

CMOS Design(ECL-312)

Project Report

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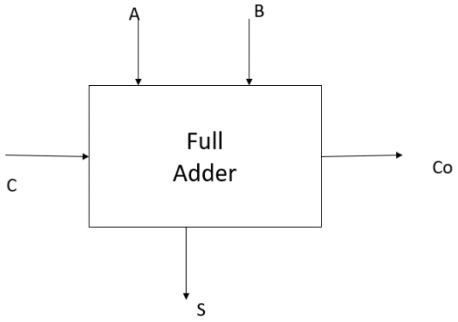
Contents

Aim

Perform the following operations

1. Implement full adder using transmission gate by writing netlist in NGSPICE.
2. Draw the layout of full adder using transmission gate in MicroWind.
3. Implement transmission gate based adiabatic full adder in NGSPICE.
4. Draw the layout of transmission gate based adiabatic full adder

Theory



A,B,C are inputs

S is sum

Co is carry output

* Boolean Expression-

For Sum-

$S=\bar{A}\bar{B}C+\bar{A}B\bar{C}+A\bar{B}\bar{C}+ABC$

$S=ABC+\bar{C}(A+B+C)$

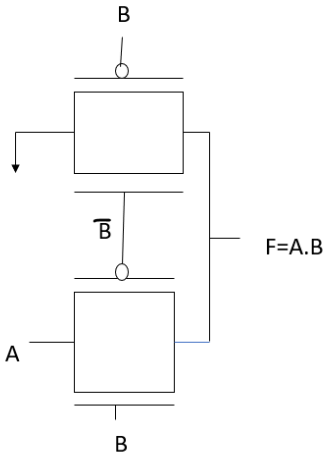
For Carry out-

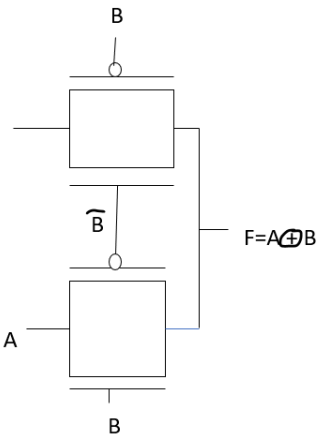
$Co=AB+BC+AC$

$Co=AB+C(A+B)$

- Transmission gate based Full adder-

  Carry generate(G)=A.B
- Carry Propogate(p)=A+B / $A \oplus B$





- Transmission based Adder Expression:-

SUM-

$S=ABC+\overline{A}\overline{B}C+A\overline{B}\overline{C}+\overline{A}B\overline{C}$

$S=C(AB+\overline{A}\overline{B}) + C(A\overline{B}+A\overline{B})$

$S=C(A\odot B) + C(A\oplus B)$

Let-$x=A\oplus B$

$x= A\odot B$

$S=C.X\oplus C.X$

$=X\oplus C$

$S=A\oplus B\oplus C$

$S=P\oplus C$ [$P=A\oplus B$]

Carry out-

Co=AB + BC + AC

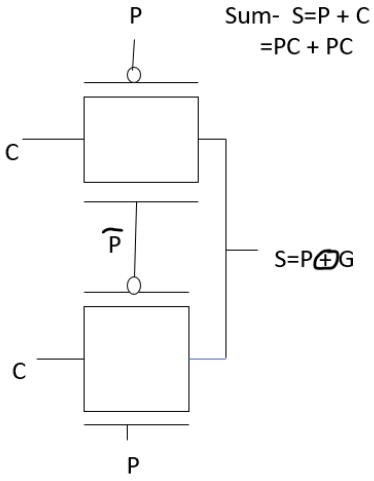
Co=AB + C(A+B)

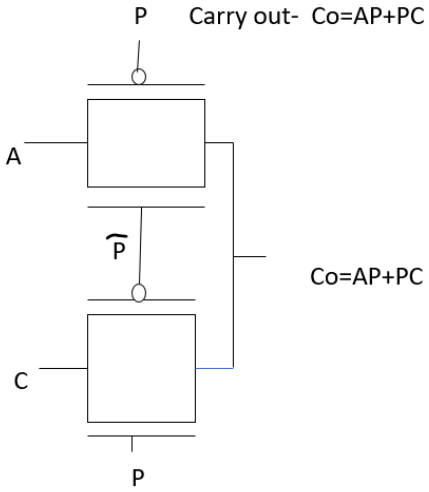
Co=G + PC

= A.B + PC

Co=AP + PC

- Design-





- Comparing above design and expression I make the circuit diagram and layout

- Truth Table-

A	B	C	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Implement full adder using transmission gate by writing netlist in NgSpice

Circuit

Above is the circuit diagram of full adder using transmission gate logic. The detailed node numbering is also shown which is used in writing its netlist.

Netlist-

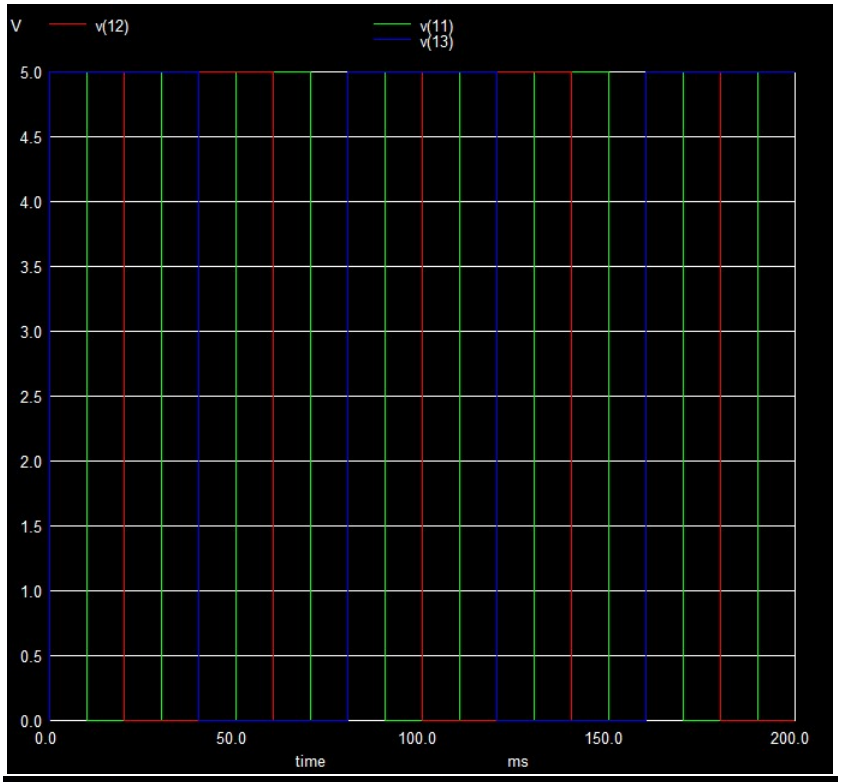
```
**Full Adder using transmssion gate
 .subckt inverter 1 2 3
 mp 2 1 3 3 pmod w=100u l=10u
 mn 2 1 0 0 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
 .model pmod pmos level=54 version=4.7
 .ends

 .subckt trans and 1 2 3 4
 mp 4 3 1 1 pmod w=100u l=10u
 mn 4 2 1 1 nmod w=100u l=10u
 .model nmod nmos level=54 version=4.7
 .model pmod pmos level=54 version=4.7
 .ends

 Vdd 1 0 dc 5V
 Va 11 0 pulse(0 5 0 0 0 10ms 20ms)
 Vb 12 0 pulse(0 5 0 0 0 20ms 40ms)
 Vc 13 0 pulse(0 5 0 0 0 40ms 80ms)
 xa 11 14 1 inverter
 xb 12 15 1 inverter
 xc 13 16 1 inverter
 xa and b' 11 15 12 17 trans and
 xb and a' 14 12 15 17 trans and
 xy 17 18 1 inverter
 xc and y' 13 18 17 19 trans and
 xy and c' 16 17 18 19 trans and
 xc and y 13 17 18 20 trans and
 xa and y' 11 18 17 20 trans and
 .model nmod nmos level=54 version=4.7
 .model pmod pmos level=54 version=4.7
 .tran 0.01ms 200ms
 .control
 run
```

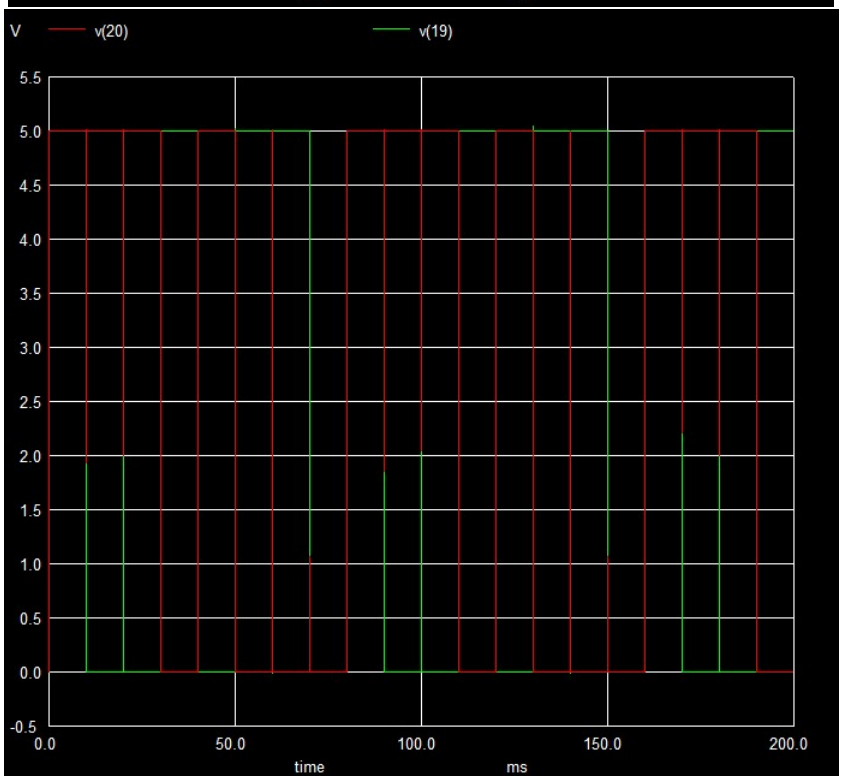
```
plot V(11) V(12) V(13)
plot V(19) V(20)
.endc
.end
```

Output of Netlist-

The node numbering and their corresponding variables are indicated below:

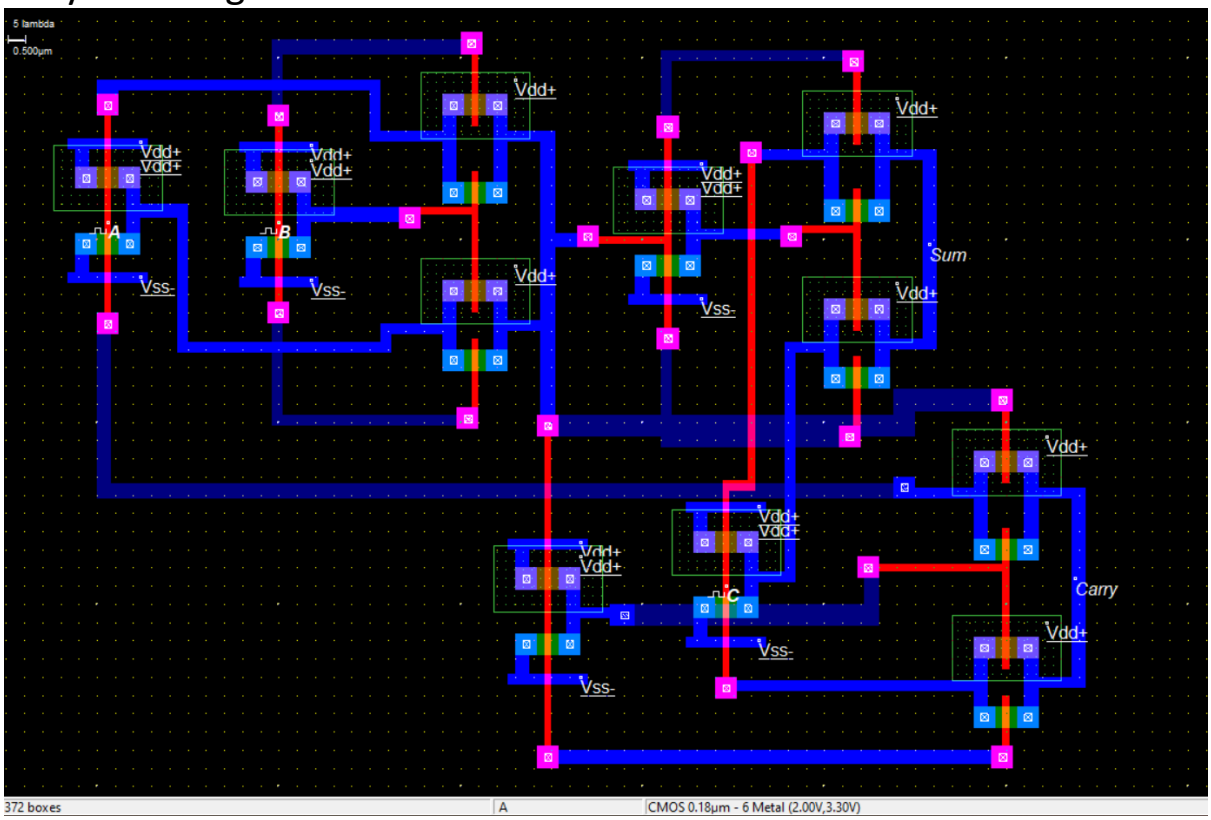
- V(11) ⟶ A
- V(12) ⟶ B
- V(13) ⟶ C
- V(19) ⟶ Sum
- V(20) ⟶ Carry


V
v(12)
v(11)
v(13)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
50.0
100.0
150.0
200.0
time
ms

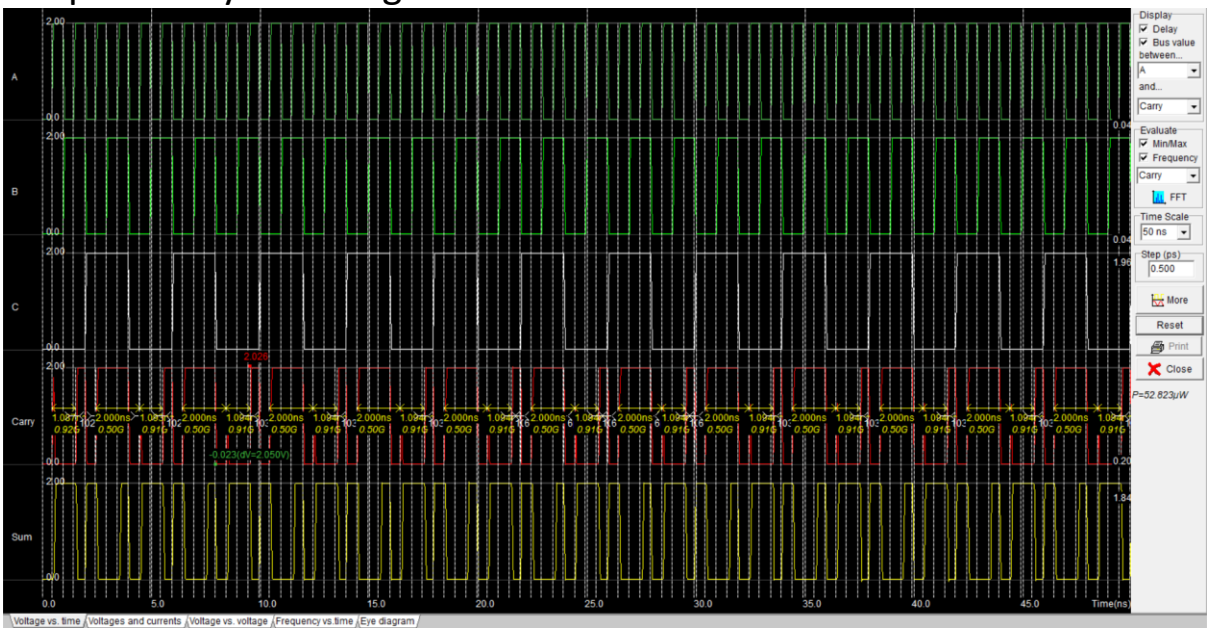

V
v(20)
v(19)
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
0.0
50.0
100.0
150.0
200.0
time
ms

#Draw the layout of full adder using transmission gate in MicroWind-

*Layout Design-



- Output of Layout Design-



We have used 6 transmission gates for constructing a full adder. The layout of the same has been shown above along with its result. The output graph shown some intermediate values since we have used transmission gate for its construction. The power dissipated by the full adder using transmission gate is 52.823μW.

This power can be reduced using the adiabatic circuits, i.e., adiabatic full adder using transmission gate.

- Implement transmission gate based adiabatic full adder in NgSpice

- Circuit Diagram-

Above are the circuit diagrams of adiabatic full adder using transmission gate logic. First we have the normal full adder using transmission gate and the output of that adder is multiplied by a pulsating signal generated through A, B and C which is shown in the second circuit diagram above. The detailed node numbering is also shown which is used in writing its netlist.

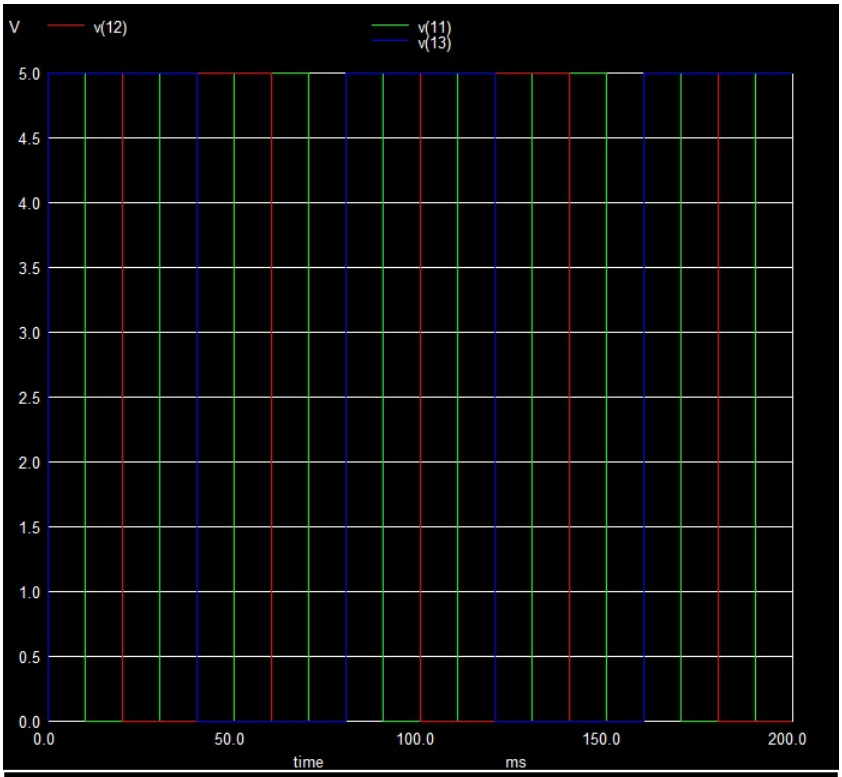
- Netlist

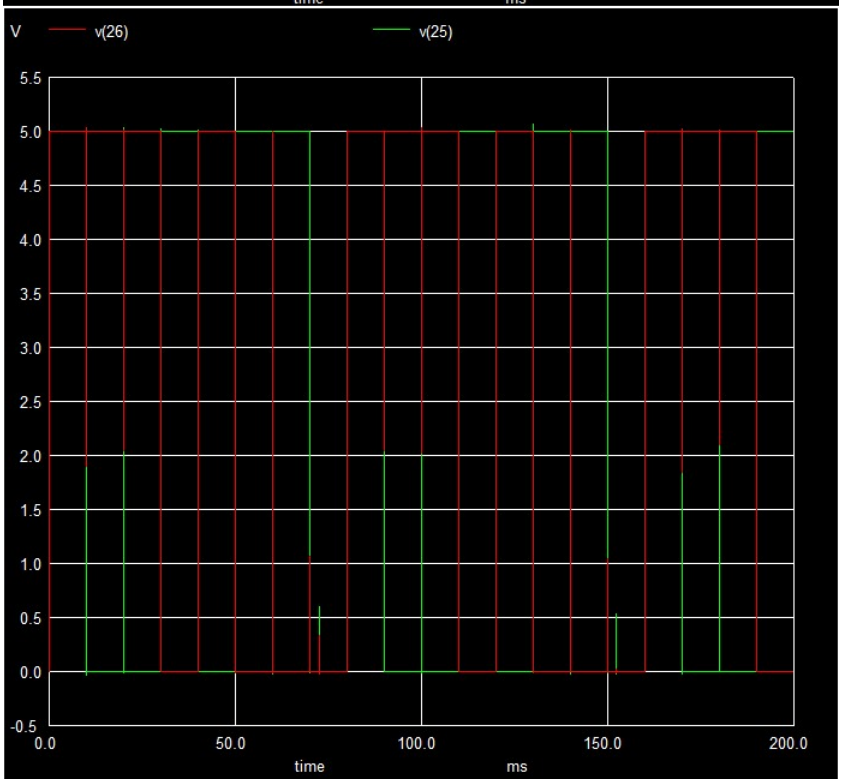
```
**Adiabatic Full Adder using transmssion gate
.subckt inverter 1 2 3
mp 2 1 3 3 pmod w=100u l=10u
mn 2 1 0 0 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
.ends

.subckt trans and 1 2 3 4
mp 4 3 1 1 pmod w=100u l=10u
mn 4 2 1 1 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
.ends

Vdd 1 0 dc 5V
Va 11 0 pulse(0 5 0 0 0 10ms 20ms)
Vb 12 0 pulse(0 5 0 0 0 20ms 40ms)
Vc      13      0 pulse(0 5 0 0       0 40ms 80ms)
xa      11      14      1       inverter
xb      12      15      1       inverter
xc      13      16      1       inverter
xa      and b' 11 15 12 17 trans and
xb      and a' 14 12 15 17 trans and
xy      17 18 1 inverter
xc      and y' 13 18 17 19 trans and
xy      and c' 16 17 18 19 trans and
xc      and y 13 17 18 20 trans and
xa      and y' 11 18 17 20 trans and
xa      and a 11 11 14 21 trans and
```

```
xb      and b 12 12 15 21 trans and
xz      21 22 1 inverter
xz      and z 21 21 22 23 trans and
xc      and c 13 13 16 23 trans and
xp      23 24 1 inverter
xs      and p 19 23 24 25 trans and
xc      and p 20 23 24 26 trans and
.model nmod nmos level=54 version=4.7
 .model pmod pmos level=54 version=4.7
 .tran 0.01ms 200ms
 .control
 run
 plot V(11) V(12) V(13)
 plot V(25) V(26)
 .endc
 .end
```

- Output of Netlist-

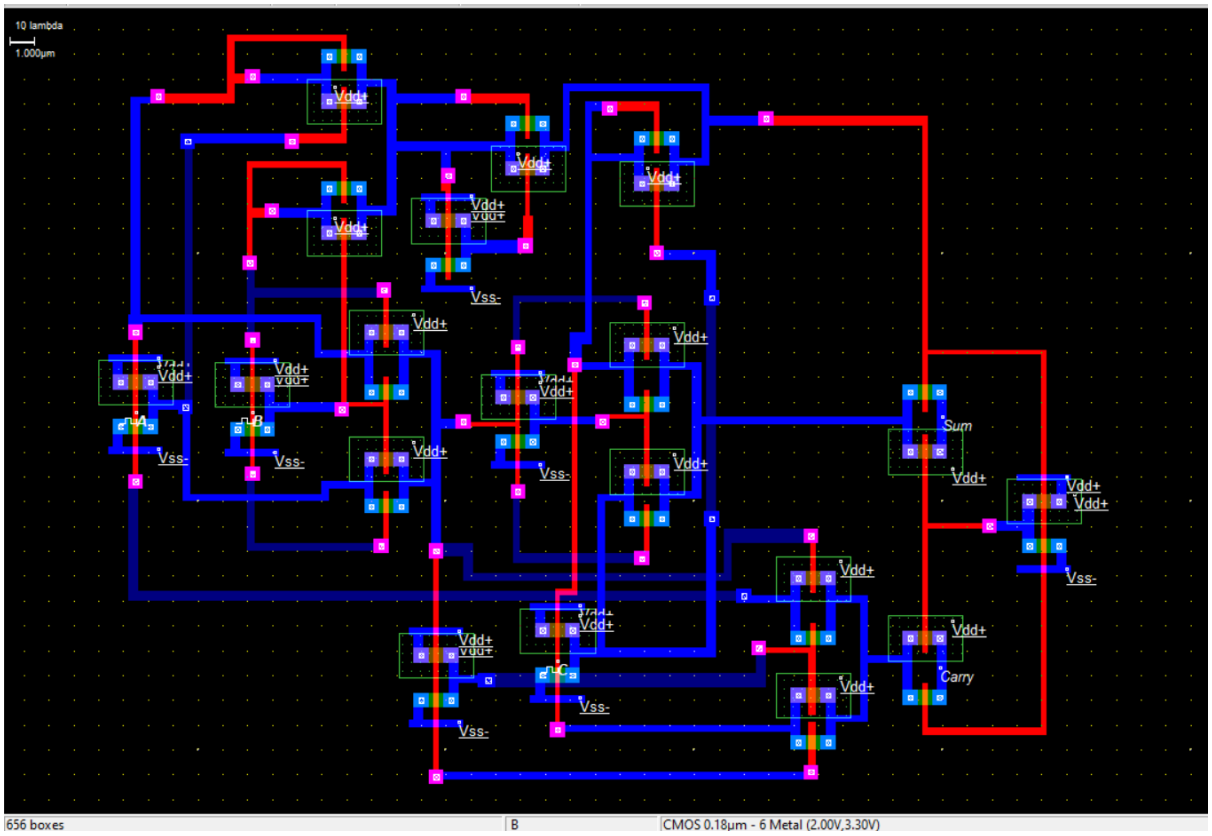
- V(11) → A
- V(12) → B
- V(13) → C
- V(25) → Sum of adiabatic circuit
- V(26) → Carry of adiabatic circuit


V
v(12)
v(11)
v(13)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
50.0
100.0
150.0
200.0
time
ms

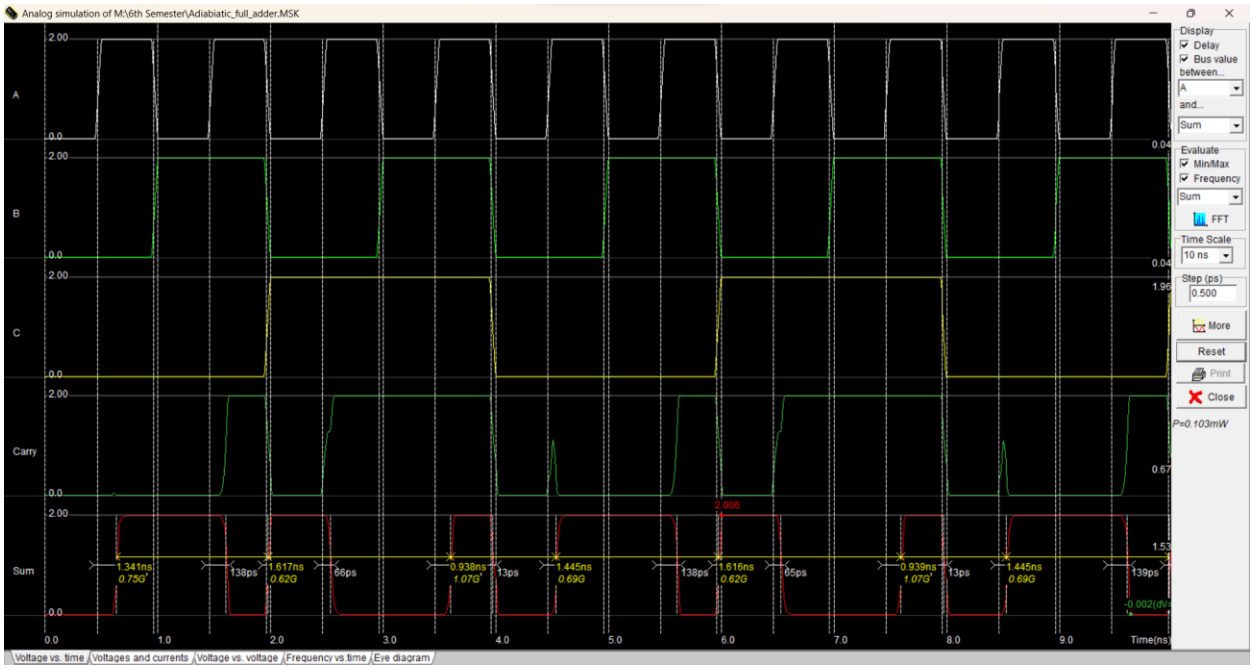

V
v(26)
v(25)
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
0.0
50.0
100.0
150.0
200.0
time
ms

- Draw the layout of transmission gate based adiabatic full Adder

layout Design-



Output of layout Design-



We have initially 6 transmission gate used for initial full adder and then additionally we have 4 extra transmission gate, in total we have 10 transmission gate used in adiabatic full adder using transmission gate logic.

We have given a pulsating signal through A, B and C, which has the expression of, $V_{AC} = A + B + C$.

By multiplying this V_{AC} to sum and carry of normal full adder we have reduced the power dissipation of the total circuit. The power dissipated came out to be 0.103μW.

• Conclussion-

We have got the same output wave forms for the normal full adder using transmis-sion gate and the adiabatic full adder.

The power dissipation of adiabatic full adder using transmission gate is less than the normal full adder using transmission gate. We have reduced the power dissipation upto 48.56% using the adiabatic circuit.