

B.Tech. 2nd Semester End Semester Examination 2022

Basic Electronics Engineering (AV 121)

FM: 40

Time 2 Hrs

Date of Exam: July 11, 2022

Multiple Choice Questions [1 Mark each]

1. For the common-emitter amplifier AC equivalent circuit, all capacitors are

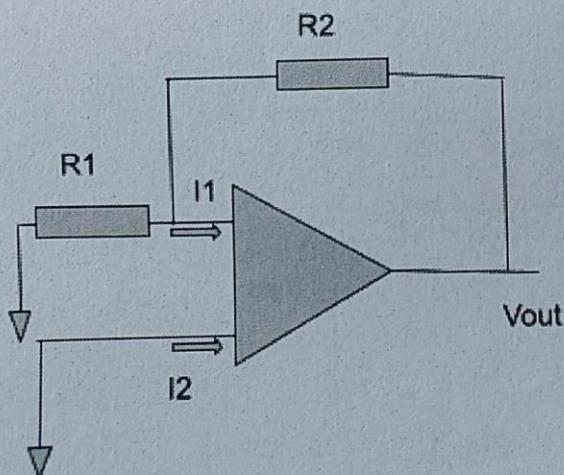
a. effectively short	b. effectively open circuits.
c. not connected to ground	d. connected to ground.
2. The DC emitter current of a transistor is 8 mA. What is the value of r_e ?

a. 320 Ω	b. 13.3 k Ω
c. 3.125 Ω	d. 5.75 Ω
3. When the bypass capacitor is removed from a common-emitter amplifier, the voltage gain

a. Increases	b. decreases
c. has very little effect	d. Becomes zero
4. Determine the value of transconductance for n-channel JFET with $IDSS = 9$ mA, $V_p = -2$ V, $V_{GS} = -1$ V.

a. 7.5 mS	b. 6.5 mS
c. 4.5 mS	d. 5.5 mS
5. In the circuit shown, the op-amp has finite input impedance, infinite voltage gain and zero input offset voltage. The output voltage V_{out} is

a. $-I_2(R_1 + R_2)$	b. I_2R_2
c. I_1R_2	d. $-I_1(R_1 + R_2)$



6. The Boolean expression $(X+Y)(X+Y') + ((XY') + X')$ ' simplifies to

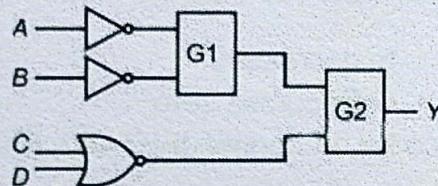
- a. X
- b. Y
- c. XY
- d. X+Y

7. The minimum number of 2-input NAND gates required to implement a 2-input XOR gate is

- a. 4
- b. 5
- c. 6
- d. 9

8. In the figure shown, the output is required to be $Y = AB + C'D'$. The gates G1 and G2 must be, respectively,

- a. NOR, OR
- b. OR, NAND
- c. NAND, OR
- d. AND, NAND



Section A

1. For the JFET bias circuit of Figure 1, determine i) I_{DQ} and V_{GSQ} ii) V_D iii) V_S iv) V_{DS} v) V_{DG}
Given $R_1 = 2.1 \text{ m}\Omega$, $R_2 = 270 \text{ k}\Omega$, $R_D = 2.4 \text{ k}\Omega$ and $R_s = 1.5 \text{ k}\Omega$ and $I_{DSS} = 8 \text{ mA}$ and $V_P = -4 \text{ V}$ [3 marks]

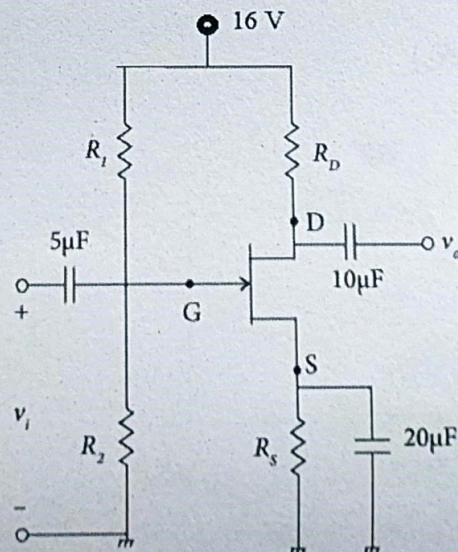
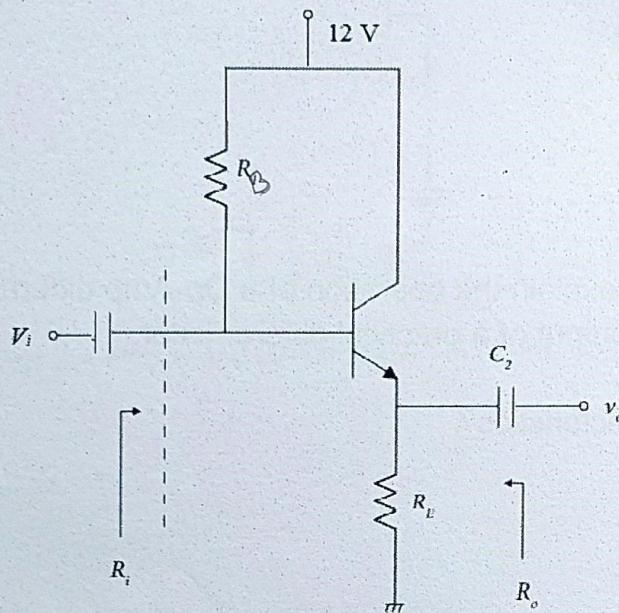


Fig. 1

2. Draw the circuit diagram of a bridge rectifier circuit and plot its transfer characteristic curve considering the ideal and simplified diode model. Obtain the value/expression for the ripple factor and rectification efficiency for the circuit.

[4 marks]

3. Identify the circuit and determine
- Small signal parameters (g_m , r_{π} , r_e)
 - Input resistance
 - Output resistance
 - Voltage gain



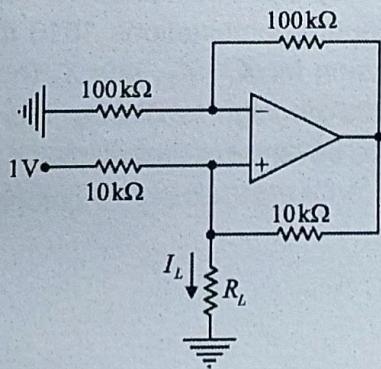
Given $\beta = 100$, $V_A = \infty$, $R_B = 220 \text{ k}\Omega$ and $R_E = 3.3 \text{ k}\Omega$

[4 Marks]

Section B

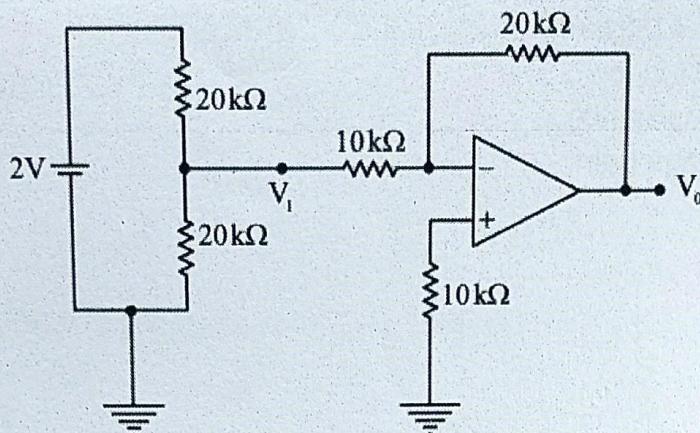
1. In the circuit given below, the OP-AMP is ideal. The value of current I_L in microampere is

[3 marks]



2. In the circuit given below, the OP-AMP is ideal. Compute the output voltage V_o in volt.

[3 marks]



3. With a neat circuit diagram explain the operation of a Op-Amp differentiator and derive an expression for the output of a practical differentiator.

[2 marks]

4. What are ideal Op-Amp characteristics?

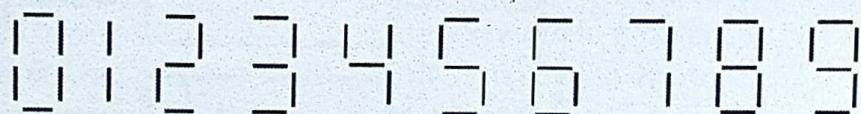
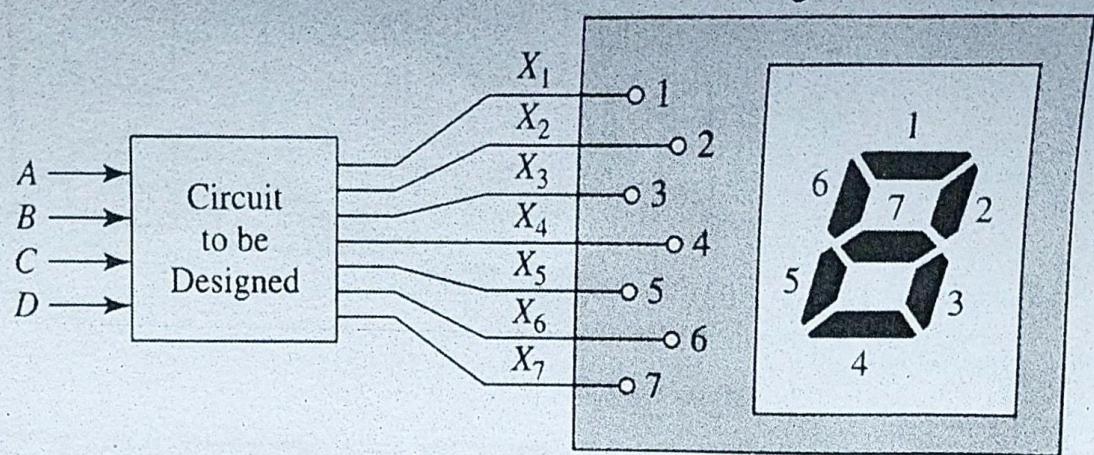
[1 mark]

Section C

1. A seven segment indicator can be used to display any one of the decimal digits 0 through 9 (see figure below). For example, '1' is displayed by lighting segment 2 and 3, '2' by lighting segments 1,2,7, 5 and 4. Displays corresponding to other digits are shown in the figure. A segment is lighted when a logic 1 is applied to the corresponding input (X_1 through X_7) on the display module. For example, to light the segment 1, X_1 should go high (logic 1). Four inputs A, B, C and D correspond to the binary representation of the decimal digits 0 through 9, with A being the most significant bit and D being the least significant bit. Therefore, $ABCD = 0001$ corresponds to decimal 1, $ABCD = 0010$ corresponds to decimal 2 and so on. Assume that, only input combinations representing the digits 0 through 9 can occur as inputs, so the inputs combinations 1010 through 1111 are dont cares. Find the minimized boolean expression for X_1 , X_2 , and X_3 (no need to design for all X_1 through X_7) such that correct segments go high to display the decimal digit (corresponding to the binary input at ABCD) in the seven segment display.

[6 Marks]

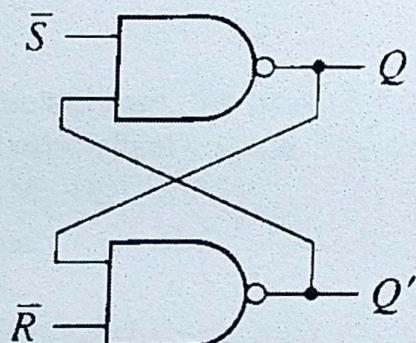
Seven-Segment Indicator



2. For the sequential circuit shown in figure, complete the Truth table (Q^{++}).

[3 Marks]

\bar{S}	\bar{R}	$Q(t_0)$	Q^{++}
1	1	0	
1	1	1	
1	0	0	
1	0	1	
0	1	0	
0	1	1	
0	0	0	
0	0	1	



3. Figure below shows a sequential circuit constructed using two SR latches. The timing diagram for clock input (CLK), its complement (CLK'), S and R inputs are shown in the figure. Draw the corresponding timing diagram for P and Q signals.

[3 Marks]

