Calculator Overview

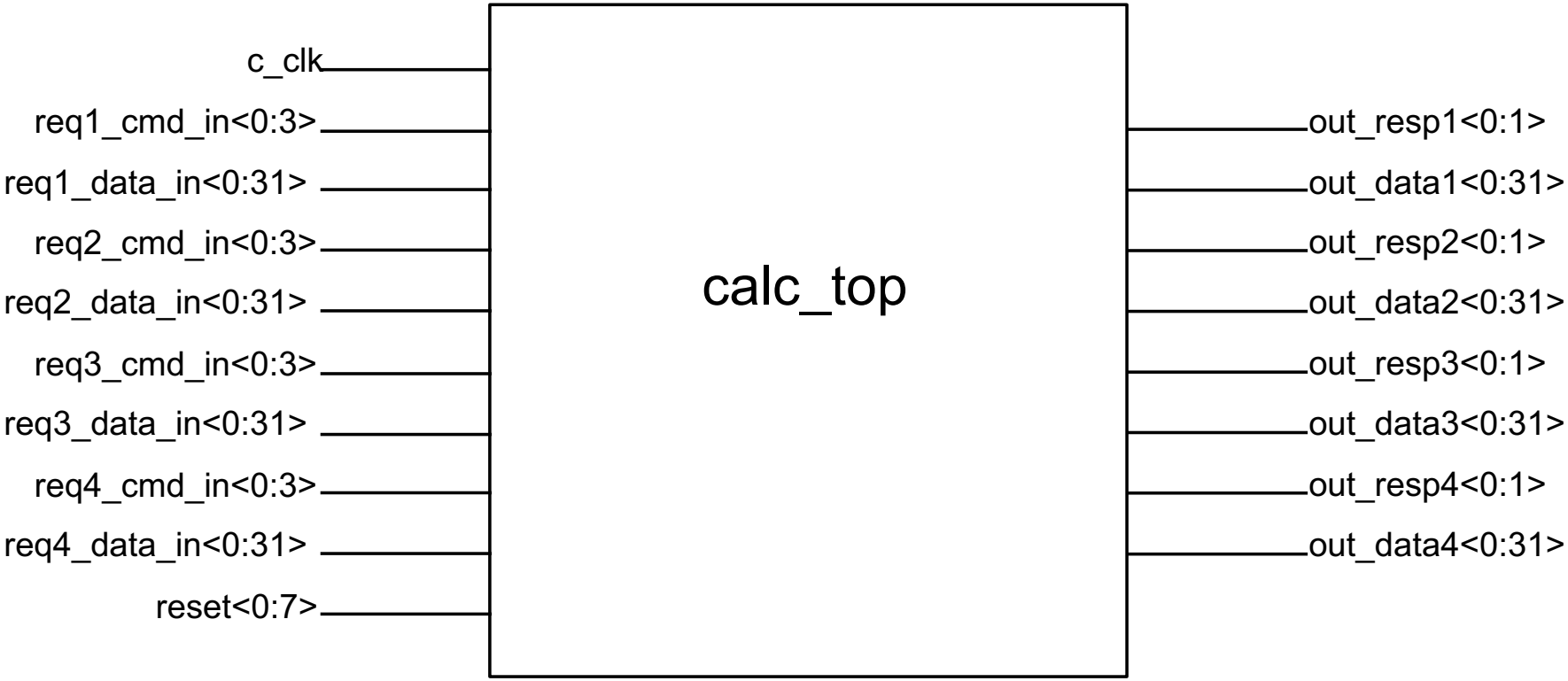
Functional Verification

Calculator Design

- Calculator has 4 functions:
  - Add
  - Subtract
  - Shift left
  - Shift right
- Calculator can handle 4 requests in parallel
  - All 4 requestors use separate input signals
  - All requestors have equal priority
  - Each port must wait for its response prior to sending the next command

Calculator design

- Input/Output description



Calculator Design

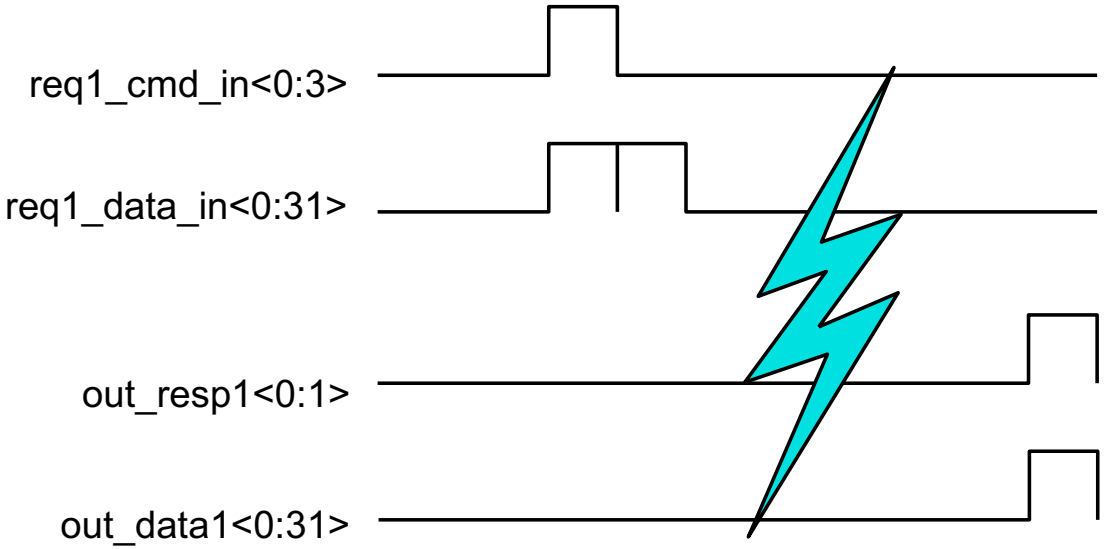
- I/O Description
  - Input commands:
    - 0 - No-op
    - 1 - Add operand1 and operand2
    - 2 - Subtract operand2 from operand1
    - 5 - Shift left operand1 by operand2 places
    - 6 - Shift right operand1 by operand2 places
  - Input Data
    - Operand1 data arrives with command
    - Operand2 data arrives on the following cycle

Calculator Design

- Outputs
  - Response line definition
    - 0 - no response
    - 1 - successful operation completion
    - 2 - invalid command or overflow/underflow error
    - 3 - Internal error
  - Data
    - Valid result data on output lines accompanies response (same cycle)

Calculator Design

- Input/Output timing



Each port must wait for its response prior to sending the next command!

Calculator Design

- Other information
  - Clocking
    - When using a cycle simulator, the clock should be held high (c_clk in the calculator model)
    - The clock should be toggled when using an event simulator
  - Calculator priority logic
    - Priority logic works on first come first serve algorithm
    - Priority logic allows for 1 add or subtract at a time and one shift operation at a time

Calculator Design

- Other information (con't)
  - Resets
    - Hold reset(1:7) to '1111111'b at start of testcase for seven cycles.
    - During the reset period, outputs of the calculator should be ignored
  - Shift operation
    - Only the low order 5 bits of the second operand are used
  - Arithmetic operations are unsigned