Programming Project #1

Due Date: 10/25, 11:59 p.m. ***Please submit via Blackboard. Late submissions are accepted till 10/30, 11:59 p.m., with 10% penalty each day.***

Please name your submission file starting with "LastName_FirstName_PP1".

In this programming project, you are asked to develop a cache simulator and perform tests to observe how cache behaves. This programming project assists you for deep understanding of computer architecture in general, and cache hierarchy and memory systems in particular. This programming project intends to reinforce our discussions in class and your understandings of lecture topics.

Please note that we assume a 32-bit machine and memory addresses fed from trace files are 32-bit byte addresses.

Part 1. Direct-mapped cache

We have provided a functional, sample code to you. In this part of the programming project, you are required to compile the *cachesim.c* to generate the single-level direct-mapped cache simulator. Then run the *cachesim* with provided memory traces and report the result.

To compile the source codes, use a command like below. This command compiles cachesim.c source file and generates a binary, executable file, cachesim. Or, you can use the `make` utility.

```
$ gcc cachesim.c -o cachesim
```

To run the sample simulator, please use a command like below. You need to use the argument *direct* to let simulator know it is the direct-mapped cache, and the argument *tracefile* represents the path of the file that contains the memory traces.

```
$ ./cachesim direct tracefile
```

Requirements of Part 1:

1. The provided sample simulator only measures the total cache hits and misses. Please make modifications to the *cachesim.c* source code to calculate the cache **miss rate** and **hit rate**, and use the print statements to print out the results.
2. Please compile and run the modified simulator and report the hit and miss rate for each given trace.

Part 2. Fully associative and n-way set associative cache

In Part 2 of this programming project, you are asked to further develop the simulator to simulate fully-associative cache and n-way set associative cache.

Requirements of Part 2:

1. Based on the direct-mapped cache simulator, please extend to support the simulation of a

fully-associative cache.

2. Based on the direct-mapped cache simulator, please extend to support the simulation of an *n-way set associative cache*.
3. Both fully-associative cache and n-way set associative cache should replace a cache block (or cache line) with the **random** policy. It means that, if a set is full, then one random block should be picked and evicted. You can use a random number generator function (e.g., `rand()` or `srand()` in C) to generate the random number to select the replacement candidate. This replacement algorithm does not require keeping any information about the access history. Due to its simplicity, it has been used in numerous processors, e.g., ARM processors.
4. Users should be able to use the argument to switch between different cache models: direct-mapped, fully-associative, or n-way set associative.
5. Conduct the evaluation and analysis as specified in detail below.

Evaluation and Analysis for Part 2

The cache under simulation can be configured with different settings, e.g., different cache capacity (or cache size) and different cache line size. For instance, if we configure the cache size as 32KB and the cache line size as 64 bytes, then there are 512 cache lines in total (32KB/64B=512). Given the same cache size of 32KB, if the cache line size changed to 32 bytes, then we will have 1,024 cache blocks in total. Please note that the cache line size affects how to determine the index and tag. In this part, you are asked to perform the following evaluation with given memory traces:

Requirements:

1. Given a fixed cache size of 32KB, test the fully-associative, 8-way set associative, 4-way set associative, and 2-way set associative cache with cache line size of 16 bytes, 32 bytes, and 128 bytes, respectively. Please report the hit and miss rate in each case.
2. Given a fixed cache line size of 64 bytes, test the fully-associative, 8-way set associative, 4-way set associative, and 2-way set associative cache with the cache size of 16KB, 32KB and 64KB, respectively. Please report the hit and miss rate in each case.

Part 3. Two-level cache simulation

In Part 3 of this programming project, you are asked to conduct the simulation of two-level cache.

Requirements of Part 3:

Please simulate a two-level cache. L1 is a 2-way, 64KB cache, with 64B block size. L2 is an 8-way, 1MB cache, with 64B block size. The replacement policy is always a random policy. Please condcut the simulation using the provided trace files and report the hit and miss rate of L1 and L2, in each case.

Expected Submission:

You should submit a single tarball/zipped file through the Blackboard containing the following:

- All your source codes;
- Output files for the result/test cases for each part (in plain ASCII format, NOT screenshots).

- A 2-3 page report summarizing all your test results in a table format, or in charts (i.e., plotting these data via a plotting tool like Excel, gnuplot, MatLab, etc.) and discuss your findings/insights. There is no required format/template, so please be creative.

Grading Criteria:

Please find the detailed grading criteria from the below table. **Please note that we may require an in-person demo for grading this project.**

Part 1	
5%	Correct modification
5%	Correctness of result
Part 2	
10%	Inline comments to briefly describe your code
15%	Correctly implement the fully-associative cache simulation
20%	Correctly implement the n-way set associative cache simulation
10%	Implement the random replacement algorithm
Part 3	
20%	Conduct two-level cache simulation and carry out the specified test cases and report results.
Report	
15%	Quality of the report and level of efforts.

THE END.