Microprocessor   Question Bank
Department of Computer Engineering

Salient Features of 80386DX

1. The 80386DX is a processor that supports
a) 8-bit data operand
b) 16-bit data operand
c) 32-bit data operand
d) all of the mentioned

Answer: d
Explanation: The 80386DX is a 32-bit processor that supports, 8-bit/16-bit/32-bit data operands.

2. The 80386DX has an address bus of
a) 8 address lines
b) 16 address lines
c) 32 address lines
d) 64 address lines

Answer: c
Explanation: The 80386, with its 32-bit address bus, can address up to 4 GB of physical memory.

3. The number of debug registers that are available in 80386, for hardware debugging and control is
a) 2
b) 4
c) 8
d) 16

Answer: c
Explanation: The 80386 offers a set of total eight debug registers DR0-DR7, for hardware debugging and control.

4. The memory management of 80386 supports
a) virtual memory
b) paging
c) four levels of protection

d) all of the mentioned

Answer: d
Explanation: The memory management section of 80386 supports the virtual memory, paging and four levels of protection, maintaining full compatibility with 80286.
5. The 80386 enables itself to organize the available physical memory into pages, which is known as
a) segmentation
b) paging
c) memory division
d) none of the mentioned

Answer: b
Explanation: The concept of paging which is introduced in 80386, enables it to organise the available physical memory into pages of size 4 KB each, under the segmented memory.

6. The 80386 consists of
a) on-chip address translation cache
b) instruction set of predecessors with upward compatibility
c) virtual memory space of 64TB
d) all of the mentioned

Answer: d
Explanation: The 80386 has on-chip address translation cache, and instruction set is upward compatible with all its predecessors.
7. 80386DX is available in a grid array package of
a) 64 pin
b) 128 pin
c) 132 pin
d) 142 pin

Answer: c
Explanation: The 80386DX is available in a 132-pin grid array package.
8. The operating frequency of 80386DX is
a) 12 MHz and 20 MHz
b) 20 MHz and 33 MHz
c) 32 MHz and 12 MHz
d) all of the mentioned

Answer: b
Explanation: The operating frequency of 80386DX is 20MHz and 33 MHz.

9. The 80386 in its protected mode, in its virtual mode of operation, can run the applications of
a) 8086
b) 80286
c) 80287
d) 80387

Answer: a
Explanation: The 80386 can run the applications under protected mode, in its virtual 8086 mode of operation.
10. The 80386 in protected mode, supports all software written for
a) 8086 and 80287
b) 80286 and 80287
c) 80287 and 80387
d) 80286 and 8086
Answer: d
Explanation: The 80386 in protected mode, supports all software written for 8086 and 80286 (to be executed under the control of memory management and protection abilities of 80386).

"Architecture and Signal Descriptions of 80386".

1. Which of the units is not a part of internal architecture of 80386?
a) central processing unit
b) memory management unit
c) bus interface unit
d) none of the mentioned

Answer: d
Explanation: The internal architecture of 80386 is divided into three sections namely, central processing unit, memory management unit and bus interface unit.
2. The central processing unit has a sub-division of
a) memory unit and control unit
b) memory unit and ALU
c) execution unit and instruction unit
d) execution unit and memory unit

Answer: c

Explanation: The central processing unit is further divided into execution unit and instruction unit.

3. The unit that is used for handling data, and calculate offset address is

a) memory management unit

b) execution unit

c) instruction unit

d) bus interface unit

Answer: b

Explanation: The execution unit has eight general purpose and eight special purpose registers, which are either used for handling the data or calculating the offset addresses.

4. The unit that decodes the opcode bytes, received from the 16-byte instruction code queue is

a) memory management unit

b) execution unit

c) instruction unit

d) barrel shifter

Answer: c

Explanation: The instruction unit decodes the opcode bytes, received from the 16-byte instruction code queue, after decoding them so as to pass it to the control section, for deriving the necessary control signals.

5. The unit that increases the speed of all shift and rotate operations is

a) memory management unit

b) execution unit

c) instruction unit

d) barrel shifter

Answer: d

Explanation: The barrel shifter speeds up all shift and rotate operations.

6. The memory management unit consists of

a) segmentation unit

b) paging unit

c) segmentation and paging units

d) none of the mentioned

Answer: c

Explanation: The memory management unit consists of a segmentation unit and a paging unit.

7. The segmentation unit allows
a) maximum size of 4GB segments
b) use of segment address components
c) use of offset address components
d) all of the mentioned

Answer: d
Explanation: The segmentation unit allows the use of two address components. They are: segment and offset for relocation and sharing of code and data.

8. The unit that organizes the physical memory, in terms of pages of 4KB size each is
a) segmentation unit
b) execution unit
c) paging unit
d) instruction unit

Answer: c
Explanation: The paging unit organizes the physical memory, in terms of pages of 4KB size each.

9. The paging unit works under the control of
a) memory management unit
b) segmentation unit
c) execution unit
d) instruction unit

Answer: b
Explanation: The paging unit works under the control of segmentation unit; i.e. each segment is further divided into pages.

10. The unit that provides a four level protection mechanism, for system's code and data against application program is
a) central processing unit
b) segmentation unit
c) bus interface unit
d) none of the mentioned

Answer: b
Explanation: The segmentation unit provides a four level protection mechanism, for protecting and isolating the system's code and data, from those of the application program.

11. The unit that has a prioritizer to resolve the priority of the various bus requests is
a) bus sizing unit
b) data buffer
c) bus control unit

d) execution unit

Answer: c
Explanation: The bus control unit has a prioritizer to resolve the priority of the various bus requests.
12. The unit that interfaces the internal data bus with the system bus is
a) bus sizing unit
b) data buffer
c) bus control unit
d) execution unit

Answer: b
Explanation: The data buffer interfaces the internal data bus with the system bus.
13. The unit that drives the bus enable and address signals A0-A31 is
a) bus sizing unit
b) bus driving unit
c) address driver
d) bus driver

Answer: c
Explanation: The address driver drives the bus enable and address signals A0-A31.
14. Which of the following pin when activated, allows address pipelining?
a) ADS
b) NA
c) AP
d) none of the mentioned

Answer: b
Explanation: The Next Address (NA) input pin, if activated, allows address pipelining, during 80386 bus cycles.
15. The signal that is used to insert WAIT states in a bus cycle in 80386 is
a) HOLD
b) HLDA
c) READY
d) PEREQ

Answer: c
Explanation: READY signal is used to insert WAIT states in a bus cycle, and is useful for interfacing of slow devices with the CPU.
16. The signal which indicates to the CPU, to fetch a data word for the coprocessor is
a) READY

b) NMI
c) HLDA
d) PEREQ

Answer: d
Explanation: The Processor Extension Request (PEREQ) output signal indicates to the CPU to fetch a data word for the coprocessor.
17. The pipeline and dynamic bus sizing units handle
a) data signals
b) address signals
c) control signals
d) all of the mentioned

Answer: c
Explanation: The pipeline and dynamic bus sizing units handle the related control signals.

"Register Organisation of 80386 -1".

1. The 16-bit registers are available with their extended size of 32 bits, by adding the registers with a prefix of
a) X
b) E
c) 32
d) XX

Answer: b
Explanation: A 32 bit register, known as extended register, is represented by the register name with a prefix of E.
2. In a 32-bit register, ESP, the lower 16-bits of the register can be represented by
a) LSP
b) FSP
c) SP
d) none of the mentioned

Answer: c
Explanation: Though the extended size of 32 bits are named as EBP, ESP, ESI and EDI, the names BP, SP, SI and DI represent the lower 16-bits.
3. Which of the following is a data segment register of 80386?

a) ES

b) FS
c) GS
d) all of the mentioned

Answer: d
Explanation: The six segment registers available in 80386 are CS, SS, DS, ES, FS and GS, out of which DS, ES, FS and GS are the four data segment registers.
4. The register width used by the 32-bit addressing modes is
a) 8 bits
b) 16 bits
c) 32 bits
d) all of the mentioned

Answer: d
Explanation: The 32-bit addressing modes may use all the register widths, i.e. 8, 16 or 32 bits.
5. The flag that is additional in flag register of 80386, compared to that of 80286 is
a) VM flag
b) RF flag
c) VM and RF flag
d) none of the mentioned

Answer: c
Explanation: The VM and RF flags are added to the 80286 flag register, to derive the flag register of 80386.
6. The VM (virtual mode) flag is to be set, only when 80386 is in
a) virtual mode
b) protected mode
c) either virtual or protected mode
d) all of the mentioned

Answer: b
Explanation: If VM flag is set, the 80386 enters the virtual 8086 mode within the protected mode. This is to be set only when the 80386 is in protected mode.
7. In protected mode of 80386, the VM flag is set by using
a) IRET instruction
b) task switch operation
c) IRET instruction or task switch operation
d) none of the mentioned

Answer: c

Explanation: The VM flag can be set using the IRET instruction or any task switch operation, only in the protected mode.

8. During the instruction cycle of 80386, any debug fault can be ignored if

a) VM flag is set
b) VM flag is cleared
c) RF is cleared
d) RF is set

Answer: d

Explanation: If RF (resume flag) is set, any debug fault is ignored during the instruction cycle.

9. The RF is not automatically reset after the execution of

a) IRET
b) POPA
c) IRET and POPF
d) IRET and PUSHF

Answer: c

Explanation: The RF is automatically reset after the execution of every instruction, except for the IRET and POPF instructions. Also, it is not cleared automatically after the successful execution of JMP, CALL and INT instructions causing a task switch.

10. The segment descriptor register is used to store

a) attributes
b) limit address of segments
c) base address of segments
d) all of the mentioned

Answer: d

Explanation: The segment descriptor register is used to store the descriptor information like attributes, limit and base addresses of segments.

RegisterOrganisation of 80386 -2

1. The 32-bit control register, that is used to hold global machine status, independent ofthe executed task is

a) CR0
b) CR2
c) CR3
d) all of the mentioned

Answer: d

Explanation: The 80386 has three 32-bit control registers CR0, CR2 and CR3, to hold global machine status, independent of the executed task.

2. The descriptor table that the 80386 supports is

a) GDT (Global descriptor table)

b) IDT (Interrupt descriptor table)

c) LDT (Local descriptor table)

d) TSS (Task state segment descriptor)

e) all of the mentioned

Answer: e

Explanation: The 80386 supports four types of descriptor tables. They are, GDT, IDT, LDT and TSS.

3. The registers that are together, known as system address registers are

a) GDTR and IDTR

b) IDTR and LDTR

c) TR and GDTR

d) LDTR and TR

Answer: a

Explanation: The GDTR and IDTR are known as system address registers.

4. Which of the following is a system segment register?

a) GDTR

b) LDTR

c) IDTR

d) none of the mentioned

Answer: b

Explanation: The LDTR and TR are known as system segment registers.

5. The test register(s) that is provided by 80386 for page cacheing is

a) test control registers

b) page cache registers

c) test control and test status registers

d) test control and page cache registers

Answer: c

Explanation: Two test registers are provided by 80386 for page cacheing, namely test control and test status registers.

6. Among eight debug registers, DR0-DR7, the registers that are reserved by Intel are

a) DR0, DR1, DR2

b) DR4, DR5

c) DR1, DR4
d) DR5, DR6, DR7

Answer: b
Explanation: Out of the eight debug registers, the two registers DR4 and DR5 are Intel reserved.
7. The registers that are used to store four program controllable break point addresses are
a) DR5-DR7
b) DR0-DR1
c) DR6-DR7
d) DR0-DR3

Answer: d
Explanation: The initial four registers, DR0-DR3 store four program controllable break point addresses.
8. The register DR6 hold
a) break point status
b) break point control information
c) break point status and break point control information
d) none of the mentioned

Answer: a
Explanation: The registers DR6 and DR7 respectively hold break point status and break point control information.
9. The flag bits that indicate the privilege level of current IO operations are
a) virtual mode flag bits
b) IOPL flag bits
c) resume flag bits
d) none of the mentioned

Answer: b
Explanation: The IOPL flag bits indicate the privilege level of current IO operations.
10. The registers that are not available for programmers are
a) data and address registers
b) instruction pointers
c) segment descriptor registers
d) flag registers

Answer: c
Explanation: The segment descriptor registers of 80386 are not available for programmers, rather, they are internally used to store the descriptor information.

Addressing Modes of 80386, Data Types of 80386

1. Which of the following is not a scale factor of addressing modes of 80386?
a) 2
b) 4
c) 6
d) 8

Answer: c
Explanation: In case of the scaled the modes, any of the index register values can be multiplied by a valid scale factor to obtain the displacement. The valid scale factors are 1, 2, 4 and 8.

2. Contents of an index register are multiplied by a scale factor that may be added further to get the operand offset in
a) base scaled indexed mode
b) scaled indexed mode
c) indexed mode
d) none of the mentioned

Answer: b
Explanation: In scaled indexed mode, contents of an index register are multiplied by a scale factor that may be added further to get the operand offset.

3. Contents of an index register are multiplied by a scale factor and then added to base register to get the operand offset in
a) base scaled indexed mode
b) scaled indexed mode
c) indexed mode
d) none of the mentioned

Answer: a
Explanation: In base scaled indexed mode, contents of an index register are multiplied by a scale factor and then added to base register to get the operand offset.

4. In based scaled indexed mode with displacement mode, the contents of an index register are multiplied by a scale factor and are added to
a) base register
b) displacement
c) base register and displacement

d) none of the mentioned

Answer: c
Explanation: Contents of an index register are multiplied by a scale factor and the result is addedto a base register and a displacement to get the offset of an operand.
5. The following statement of ALP is an example of
MOV EBX, [EDX*4] [ECX]
a) base scaled indexed mode
b) scaled indexed mode
c) indexed mode
d) based scaled indexed mode with displacement mode

Answer: a
Explanation: Since in base scaled indexed mode, contents of an index register are multiplied by a scale factor and then added to base register to get the operand offset.
6. The following statement is an example of
MOV EBX, LIST [ESI*2]
MUL ECX, LIST [EBP*4]
a) base scaled indexed mode
b) scaled indexed mode
c) indexed mode
d) based scaled indexed mode with displacement mode

Answer: b
Explanation: Since in scaled indexed mode, contents of an index register are multiplied by a scale factor that may be added further to get the operand offset.
7. Bit field can be defined as a group of
a) 8 bits
b) 16 bits
c) 32 bits
d) 64 bits

Answer: c
Explanation: A group of at the most 32 bits(4 bytes) is defined as a bit field.
8. The maximum length of the string in a bit string of contiguous bits is
a) 2 MB
b) 4 MB
c) 2 GB
d) 4 GB

9. The integer word is defined as
a) signed 8-bit data
b) unsigned 16-bit data
c) signed 16-bit data
d) signed 32-bit data

Answer: c
Explanation: The integer word is the signed 16-bit data.
10. A 16-bit displacement that references a memory location using any of the addressing modes is
a) pointer
b) character
c) BCD
d) offset

Answer: d
Explanation: Offset is a 16-bit or 32-bit displacement that references a memory location using any of the addressing modes.
11. A decimal digit can be represented by
a) unsigned integer
b) signed integer
c) unpacked BCD
d) packed BCD

Answer: c
Explanation: Decimal digits from 0-9 are represented by unpacked bytes.

Real AddressMode of 80386, Protected Mode of 80386

1. The instructions available in the 80386 that are not available in its real address mode is
a) addressing techniques
b) instructions for protected address mode
c) instructions for interrupt handling
d) all of the mentioned

Answer: b
Explanation: All the instructions of 80386 are available in this mode except for those designed to work with or for protected address mode.
2. The unit that is disabled in real address mode is
a) central processing unit

b) memory management unit
c) paging unit
d) bus control unit

Answer: c
Explanation: The paging unit is disabled in real address mode.
3. To form a physical memory address, appropriate segment register contents are
a) shifted by left by 4 positions
b) added to 16-bit offset address
c) operated using one of addressing modes
d) all of the mentioned

Answer: d
Explanation: To form a physical memory address, appropriate segment register contents are shifted by left by 4 positions and then added to 16-bit offset address formed using one of addressing modes, in same way as in the 80386 real address mode.
4. The segments in 80386 real mode are
a) overlapped
b) non-overlapped
c) either overlapped or non-overlapped
d) none of the mentioned

Answer: c
Explanation: The segments in 80386 real mode are may be overlapped or non-overlapped.
5. The operation that can be performed on segments in 80386 real mode is
a) read
b) write
c) execute
d) all of the mentioned

Answer: d
Explanation: The segments in 80386 real mode can be read, written or executed, i.e. no protection is available.
6. The selectors contain the segment's
a) segment limit
b) base address
c) access rights byte
d) all of the mentioned

Answer: d
Explanation: In protected mode, the contents of segment registers are used as selectors to

address descriptors which contain the segment limit, base address and access rights byte of the segment.

7. The linear address is calculated by
a) effective address + segment base address
b) effective address − segment base address
c) effective address + physical address
d) effective address − physical address

Answer: a
Explanation: The effective address(offset) is added with segment base address to calculate linear address.

8. If the paging unit is enabled, then it converts linear address into
a) effective address
b) physical address
c) segment base address
d) none of the mentioned

Answer: b
Explanation: The paging unit when enabled, it converts linear address into physical address.

9. If the paging unit is disabled, then the linear address is used as
a) effective address
b) physical address
c) segment base address
d) none of the mentioned

Answer: b
Explanation: The linear address is used as physical address if the paging unit is disabled.

10. The paging unit is enabled only in
a) virtual mode
b) addressing mode
c) protected mode
d) none of the mentioned

Answer: c
Explanation: The paging unit is enabled only in protected mode.

11. For a single task in protected mode, the 80386 can address the virtual memory of
a) 32 GB
b) 64 MB
c) 32 TB

d) 64 TB

Answer: d
Explanation: In protected mode, the 80386 can address 4 GB of physical memory and 64 TB of virtual memory per task.

Segmentation.

1. The bit that indicates whether the segment has been accessed by the CPU or not is
a) base address
b) attribute bit
c) present bit
d) granulary bit

Answer: b
Explanation: The accessed bit or attribute bit (A) indicates whether the segment has been accessed by the CPU or not.
2. The TYPE field of descriptor is used to find the
a) descriptor type
b) segment type
c) descriptor and segment type
d) none

Answer: c
Explanation: The type field decides the descriptor type and hence the segment type.
3. If the segment descriptor bit, S=0, then the descriptor is
a) data segment descriptor
b) code segment descriptor
c) system descriptor
d) all of the mentioned

Answer: c
Explanation: If S=0, then system descriptor. If S=1, then code or data segment descriptor.
4. The bit that indicates whether the segment is page addressable is
a) base address
b) attribute bit
c) present bit
d) granularity bit

Answer: d
Explanation: The granularity bit indicates whether the segment is page addressable.
5. If the Default operation size bit, D=1, the code segment operation size selected is
a) 8-bit
b) 16-bit
c) 32-bit
d) 64-bit

Answer: c
Explanation: If D=1, the segment selected is 32-bit operand segment, else, it is a 16-bit operand segment.
6. The segment descriptor contains
a) access rights
b) limit
c) base address
d) all of the mentioned

Answer: d
Explanation: The segment descriptors are 8-byte quantities containing access right or attribute bits along with the base and limit of the segments.
7. Which of the following is not a type of segment descriptor?
a) system descriptors
b) local descriptors
c) gate descriptors
d) none

Answer: d
Explanation: The five types of segment descriptors of 80386 are:
1. Code or data segment descriptors
2. System descriptors
3.Local descriptors
4.TSS(task state segment) descriptors
5. Gate descriptors
8. The limit field of the descriptor is of
a) 10 bits
b) 8 bits
c) 16 bits
d) 20 bits
Answer: d
Explanation: The limit field of the descriptor is of 20 bits.

9. The starting address of the segment in physical memory is decided by
a) physical memory
b) segment descriptors
c) operating system
d) base address
Answer: c
Explanation: The base address that marks the starting address of the segment in physical memory is decided by the operating system and is of 32 bits.
10. The total descriptors that the 80386 can handle is
a) 2K
b) 8K
c) 4K
d) 16K
Answer: d
Explanation: 80386 can handle total 16K descriptors and hence segments.

Paging

1. The advantage of pages in paging is
a) no logical relation with program
b) no need of entire segment of task in physical memory
c) reduction of memory requirement for task
d) all of the mentioned

Answer: d
Explanation: The advantage of paging scheme is that the complete segment of a task need not be in the physical memory at any time. Only a few pages of the segments, which are required currently for the execution, need to be available in the physical memory.
2. The size of the pages in paging scheme is
a) variable
b) fixed
c) both variable and fixed
d) none

Answer: b
Explanation: The paging divides the memory into fixed size pages.
3. To convert linear addresses into physical addresses, the mechanism that the paging unit uses is
a) linear conversion mechanism

b) one level table mechanism
c) physical conversion mechanism
d) two level table mechanism

Answer: d
Explanation: The paging unit of 80386 uses a two level table mechanism, to convert the linear addresses provided by segmentation unit, into physical addresses.
4. The control register that stores the 32-bit linear address, at which the previous page fault is detected is
a) CR0
b) CR1
c) CR2
d) CR3

Answer: c
Explanation: The control register, CR2, is used to store the 32-bit linear address, at which the previous page fault is detected.
5. Which of the following is not a component of paging unit?
a) page directory
b) page descriptor base register
c) page table
d) page

Answer: b
Explanation: The paging unit handles every task in terms of three components namely page directory, page table and the page itself.
6. The control register that is used as page directory physical base address register is
a) CR0
b) CR1
c) CR2
d) CR3

Answer: d
Explanation: The control register, CR3, is used as page directory physical base address register, to store the physical starting address of the page directory.
7. The bits of CR3, that are always zero are
a) higher 4 bits
b) lower 8 bits
c) higher 10 bits
d) lower 12 bits

Answer: d

Explanation: The lower 12 bits of CR3 are always zero to ensure the page size aligned with the directory.

8. Each directory entry in page directory is maximum of

a) 2 bytes

b) 4 bytes

c) 8 bytes

d) 16 bytes

Answer: b

Explanation: Each directory entry is of 4 bytes, thus a total of 1024 entries are allowed in a directory.

9. The size of each page table is of

a) 2 Kbytes

b) 2 bytes

c) 4 Kbytes

d) 4 bytes

Answer: c

Explanation: Each page table is of 4 Kbytes in size, and may contain a maximum of 1024 entries.

10. The dirty bit(D) is set, before which operation is carried out

a) write

b) read

c) initialization

d) none of the mentioned

Answer: a

Explanation: The dirty bit (D) is set before a write operation to the page is carried out.

11. The bit that is undefined for page directory entries is

a) P-bit

b) A-bit

c) D-bit

d) all of the mentioned

Answer: c

Explanation: The D-bit is undefined for page directory entries.

12. The bit that is used for providing protection is

a) User/Supervisor bit

b) Read bit

c) Write bit

d) all of the mentioned

Answer: d
Explanation: The User/Supervisor (U/S) bit and Read/Write (R/W) bit are used to provide protection.
13. The storage of 32 recently accessed page table entries to optimize the time, is known as
a) page table
b) page descriptor base register
c) page table cache
d) none of the mentioned

Answer: c
Explanation: To optimize the considerable time taken for conversion, a page table cache is provided, which stores the 32 recently accessed page table entries.
14. The page table cache is also known as
a) page table storage
b) storage buffer
c) translation look aside buffer
d) all of the mentioned

Answer: c
Explanation: The page table cache is also known as translation look aside buffer.