IITB CPU

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Design a computing system, IITB-CPU, whose instruction set architecture is provided. Use VHDL as HDL to implement. IITB-CPU is a 16-bit very simple computer developed for the teaching purpose. The IITB-CPU is an 8-register, 16-bit computer system, i.e., it can process 16 bits at a time. It should use point-to-point communication infrastructure.

The problem statement can be found in EE224-IITB-CPU-Project.pdf.

The datapath consists of 13 muxes, one 16 bit ALU, one priority encoder, and two Sign Extenders SE6 and SE9 for 6 and 9 bit inputs giving 16 bit outputs. There is one 7shifter which shifts the input by 7 bits and appending 0s to the right giving a 16 bit output. There are three temporary registers TR1, TR2, TR3 where all the registers are of 16 bits.

The instructions and information regarding the 17 states of the FSM can be found in the file FSM States.pdf and the state transition flows of the Finite State Machine can be found in the file State Transition Diagram.pdf. The components used are shown in the file Datapath.pdf. Output corresponding the selection lines of the muxes are shown in the file Muxes.pdf.

The project folder also has attached the hardware descriptions of the various components in VHDL. The toplevel entity of the project is IITB-CPU.

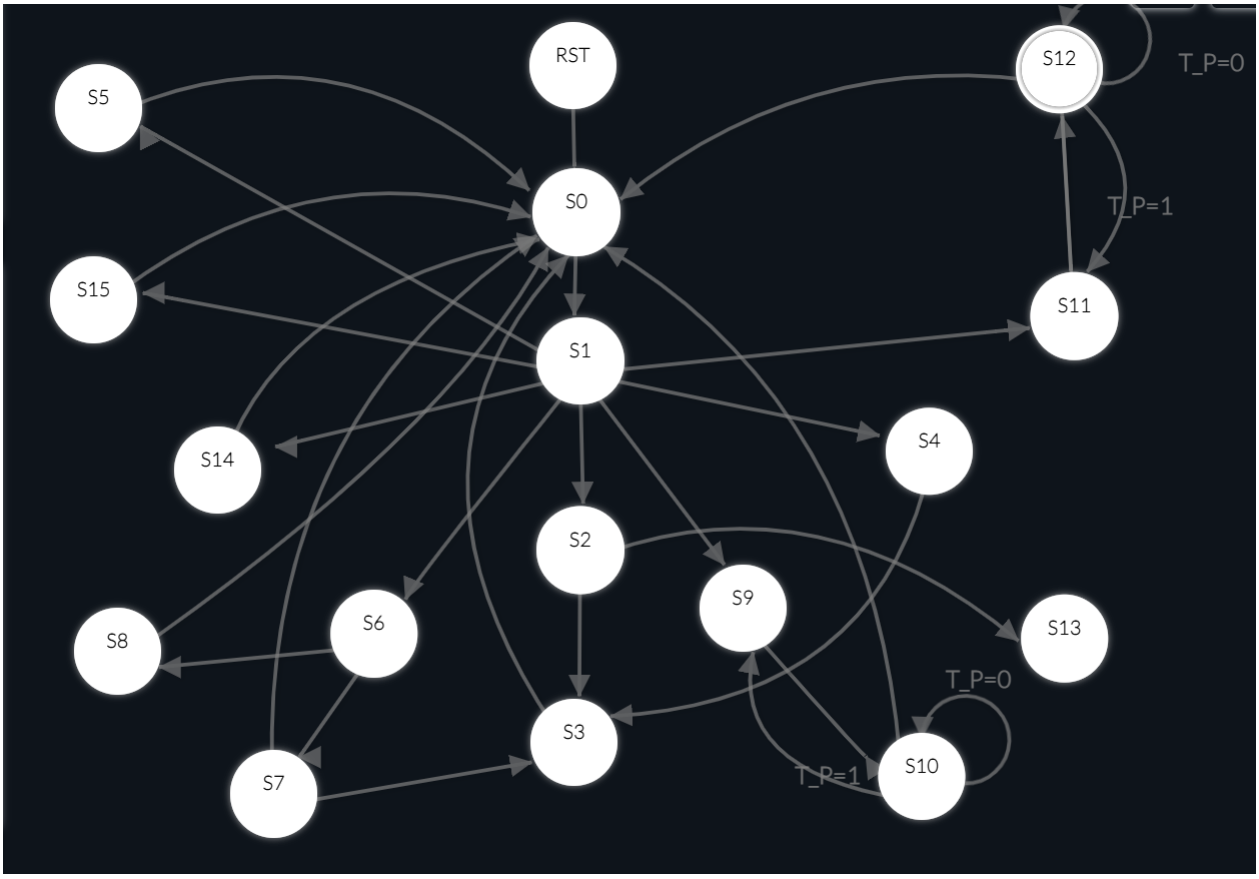

Figure 1: FSM State Diagram

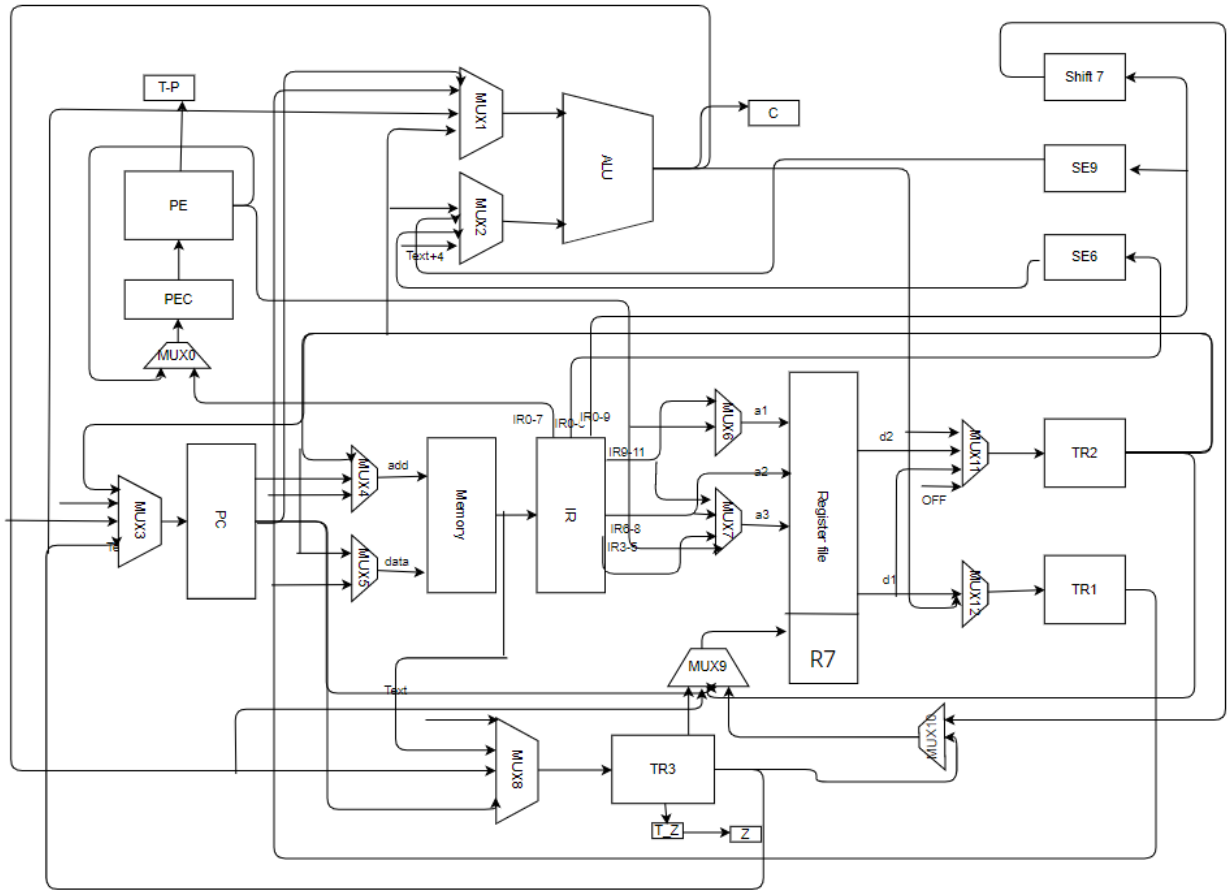

Figure 2: Datapath

References

[1] *https://www.latex-tutorial.com/tutorials/beginners/how-to-use-latex/*

[2] https://charleslabs.fr/en/project-A+basic+VHDL+processor

[3] https://github.com/sammy-87/EE-309-Project-1-multi-cycle-processor-IITB-RISC-

[4] https://domipheus.com/blog/designing-a-cpu-in-vhdl-part-1-rationale-tools-method/