

i)

A ₁	A ₂	t ₃
0	0	alu.out
0	1	PC
1	0	mem.d
1	1	OFF

ii)

B ₁	B ₂	MEM.a
0	0	PC
0	1	t ₂
1	0	off
1	1	t ₁

iii)

C ₁	mem.d
0	t ₁
1	t ₂

iv)

P ₁	RF-a ₁
0	IR ₉₋₁₁
1	PEN-0

v)

E ₁	E ₂	RF-a ₃
0	0	IR ₉₋₁₁
0	1	IR ₆₋₈
1	0	IR ₃₋₅
1	1	PEN-0

vi)

F ₁	RF-d ₃
0	t ₃
1	IR ₀₋₈ + 75

vii)

G ₁	G ₂	ALU-a
0	0	t ₁
0	1	t ₃
1	0	t ₂
1	1	PC

viii)

H ₁	H ₂	ALU.b
0	0	+1
0	1	IR ₀₋₅ + SE6
1	0	t ₂
1	1	IR ₀₋₈ + SE9

ix)

I ₁	t ₁
0	alu.out
1	RF-d ₃

x)

J ₁	J ₂	t ₂
0	0	RF-d ₁
0	1	alu.out
1	0	RF-d ₂
1	1	

xi)

K ₁	K ₂	ALU
0	0	ADD
0	1	ADD
1	0	NAND
1	1	XOR

xii)

L ₁	C
0	Modify
1	Modify

xiii)

L ₂	Z
0	Modify
1	Modify

xiii)

M ₁	M ₂	M ₃	R ₇
1	1	0	PC
0	0	1	t ₃
0	0	0	alu.out
0	1	0	t ₂
others			RF-d ₃

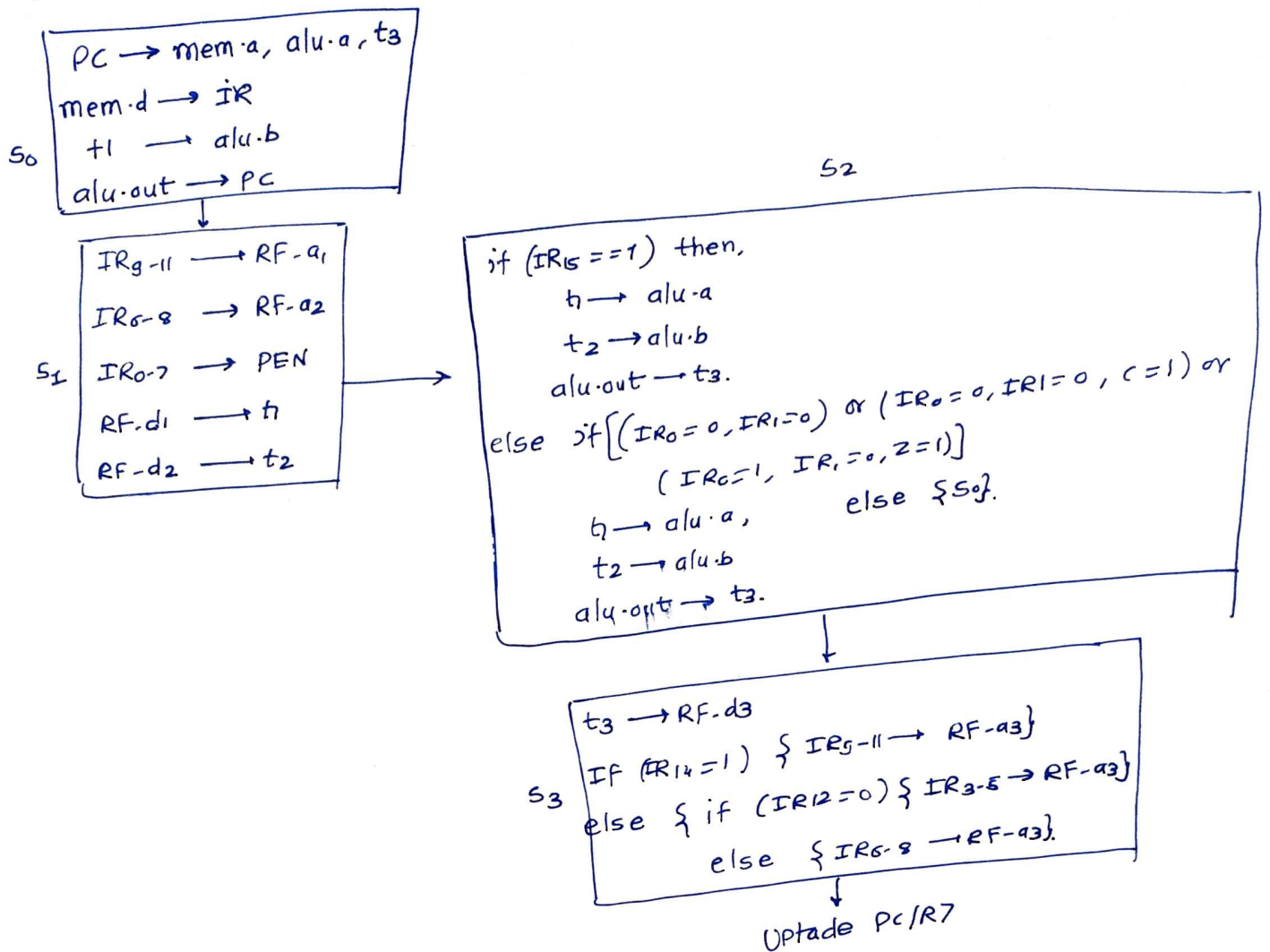
xiv)

N	PE (Register)
0	PE-0
1	IR ₀₋₇

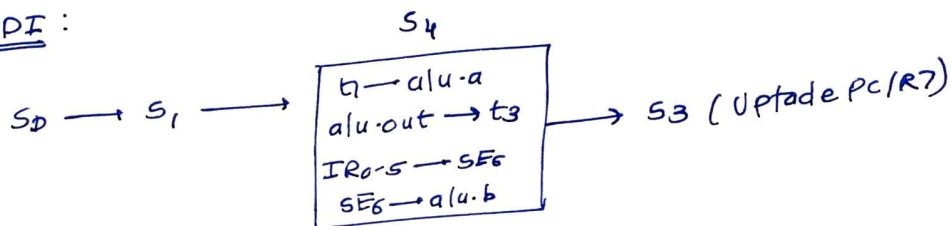
(-xv)

P ₁	P ₂	PC
0	0	alu.out
0	1	t ₃
1	0	t ₂
1	1	off

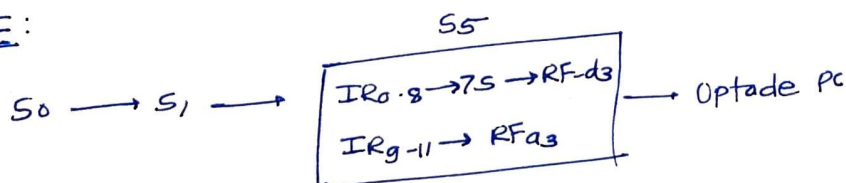
i) ADD, ADC, ADZ, NDU, NDC, NDZ:



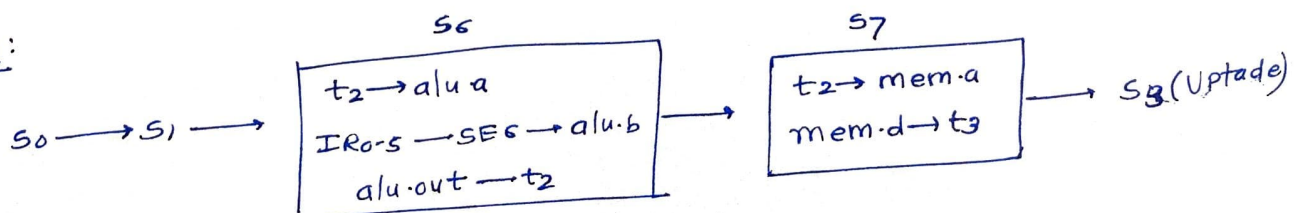
④ ADI:



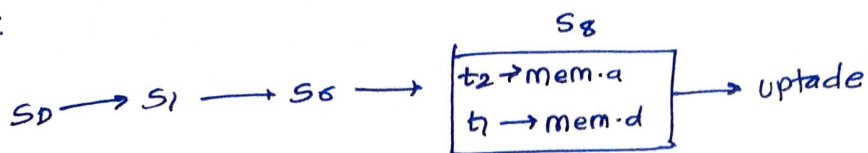
⑧ LHI:



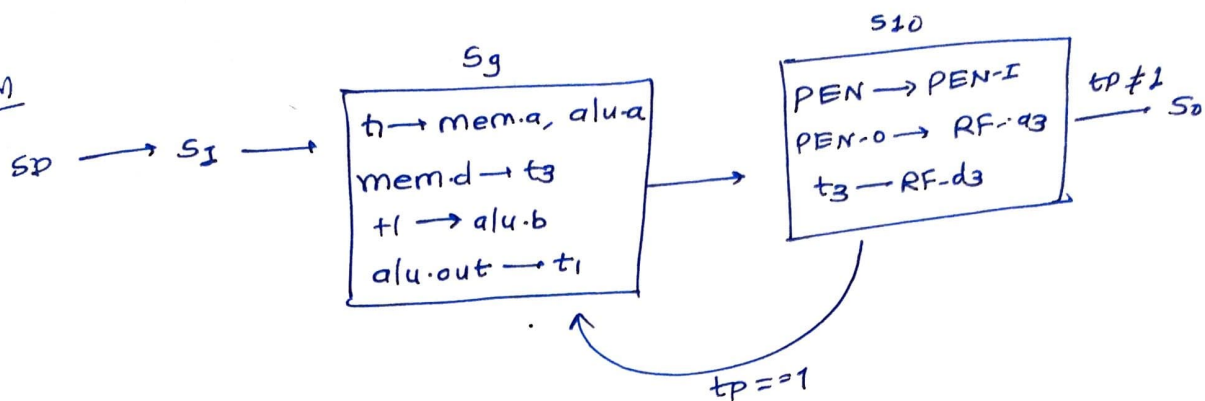
⑨ LW:



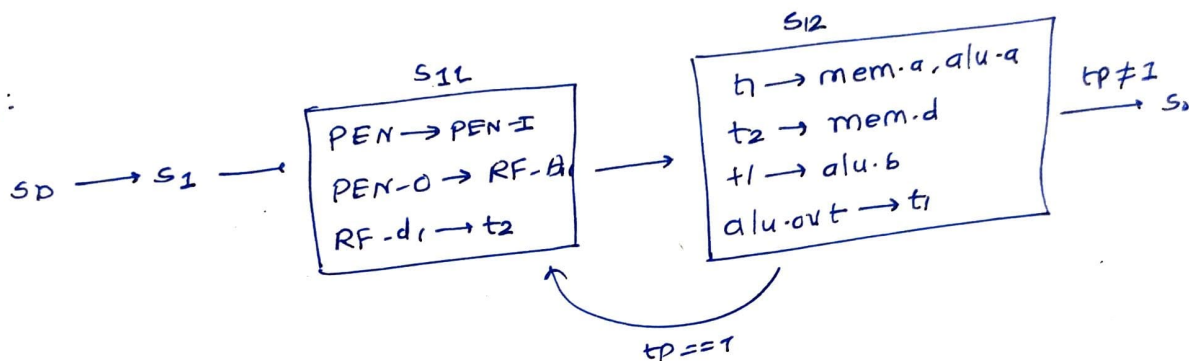
⑩ SW:



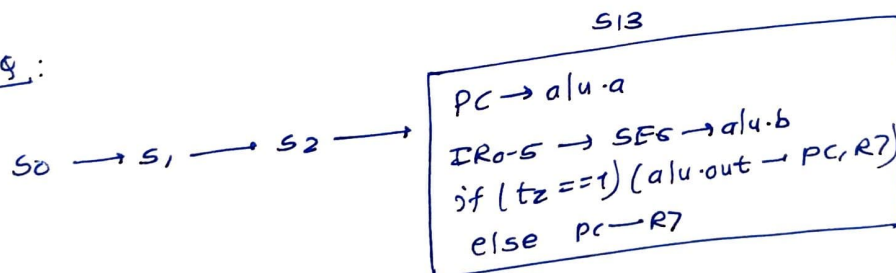
⑪ LM



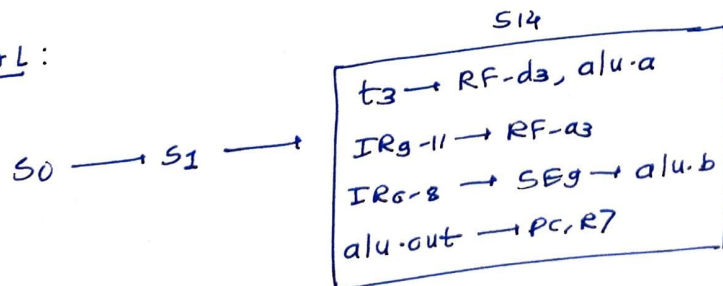
⑫ SM:



⑬ BEG:



⑭ JAL:



⑮ JLR:

