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Chapter 10. Data Storage

Course: MATH 8127-Digital Computer Fundamentals

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STUDY BY ANSWERING THESE QUESTIONS

Chapter 6. Function of Combinational Logic

True or False

1. A half-adder adds two binary bits.
2. A half-adder has a carry output only.
3. A full adder adds two bits and produces two outputs.
4. A full-adder can be realized only by using 2-input XOR gates.
5. When the input bits are both 1 and the input carry bit is 1, the sum output of a full adder is 1.
6. The output of a comparator is 0 when the two binary inputs given are equal.
7. A decoder detects the presence of a specified combination of input bits.
8. The 4-line-to-10-line decoder and the 1-of-10 decoder are two different types.
9. An encoder essentially performs a reverse decoder function.
10. A multiplexer is a logic circuit that allows digital information from a single source to be routed onto several lines.

Circle the correct answer

1. A half-adder is characterized by

   (a) two inputs and two outputs (b) three inputs and two outputs

   (c) two inputs and three outputs (d) two inputs and one output

2. A full-adder is characterized by

   (a) two inputs and two outputs (b) three inputs and two outputs

   (c) two inputs and three outputs (d) two inputs and one output

3. The inputs to a full adder are A = 1, B = 0, C_{in} = 1. The outputs are

(a) $\sum = 0, C_{out} = 1$ (b) $\sum = 1, C_{out} = 0$

(c) $\sum = 0, C_{out} = 0$ (d) $\sum = 1, C_{out} = 1$

4. A 3-bit parallel adder can add

(a) three 2-bit binary numbers (b) two 3-bit binary numbers

(c) three bits at a time (d) three bits in sequence

5. To expand a 2-bit parallel adder to a 4-bit parallel adder, you must

(a) use two 2-bit adders with no interconnections

(b) use two 2-bit adders and connect the sum outputs of one to the bit inputs of the other

(c) use four 2-bit adders with no interconnections

(d) use two 2-bit adders with the carry output of one connected to the carry input of the other

6. If a 74HC85 magnitude comparator has A = 1000 and B = 1010, the outputs are

(a) A > B = 0, A <B = 0, A = B = 0 (b) A > B = 0, A< B = 0, A = B = 1

(c) A > B = 0, A <B = 1, A = B = 0 (d) A >B = 0, A < B = 1, A = B = 1

7. If a 1-of-16 decoder with active-LOW outputs exhibits a LOW on the decimal 12 output, what are the inputs?

(a) $A_3A_2A_1A_0 = 1010$ (b) $A_3A_2A_1A_0 = 1110$

(c) $A_3A_2A_1A_0 = 1100$ (d) $A_3A_2A_1A_0 = 0100$

8. A BCD-to-7 segment decoder has 0100 on its inputs. The active outputs are

(a) a, c, f, g (b) b, c, f, g

(c) b, c, e, f (d) b, d, e, g

9. In general, a multiplexer has

(a) one data input, several data outputs, and selection inputs

(b) one data input, one data output, and one selection input

(c) several data inputs, several data outputs, and selection inputs

(d) several data inputs, one data output, and selection inputs

10. Data distributors are basically the same as

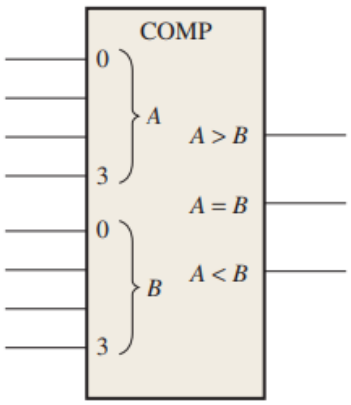
(a) decoders (b) demultiplexers

(c) multiplexers (d) encoders

Answer the following

Reference: Digital_Fundamentals_11ed_by_Thomas_L.Floyd

1. Determine the sum (∑) and the output carry (C_{out}) of a half-adder for each set of input bits:
   (a) 01 (b) 00 (c) 10 (d) 11
2. A full-adder has C_{in} = 1. What are the sum (∑) and the output carry (C_{out}) when A = 1 and B = 1?
3. What is the general logic expression of C_{out} of a Look-ahead carry adder?
4. The input bits to a full-adder are A = 1 and B = 0. Determine C_g and C_p.
5. Determine the output carry of a full-adder when C_{in} = 1, C_g = 0, and C_p = 1
6. From the truth table show how you get the logic circuit of a Full adder. Draw the logic circuit.
7. Apply each of the following sets of binary numbers to the comparator inputs that you have to draw, and determine the output by following the logic levels through the circuit.
   (a) 10 and 10 (b) 11 and 10
8. Determine the A=B, A>B, and A<B outputs for the input numbers shown on the comparator below, with A=0110 and B=0101



9. Determine the logic required to decode the binary number 1011 by producing a HIGH level on the output.
10. Draw the truth table, logic diagram and logic circuit of a 4x1 Multiplexer.
11. Draw the truth table, logic diagram and logic circuit of a 1x2 Demultiplexer.

Chapter 7. Sequential Logic

Reference: Digital_Fundamentals_11ed_by_Thomas_L.Floyd

True or False

1. A latch has one stable state.
2. A latch is considered to be in the RESET state when the Q output is low.
3. A gated D latch cannot be used to change state.
4. Flip-flops and latches are both bistable devices.
5. An edge-triggered D flip-flop changes state whenever the D input changes.
6. A clock input is necessary for an edge-triggered flip-flop.
7. When both the J and K inputs are HIGH, an edge-triggered J-K flip-flop changes state on each clock pulse.

To question below circle the correct answer

1. An active HIGH input S-R latch is formed by the cross-coupling of

   (a) two NOR gates (b) two NAND gates (c) two OR gates (d) two AND gates

2. Which of the following is not true for an active LOW input S-R latch?

   (a) S = 1, R = 1, Q = NC, Q = NC (b) S = 0, R = 1, Q = 1, Q = 0

   (c) S = 1, R = 0, Q = 1, Q = 0 (d) S = 0, R = 0, Q = 1, Q = 1

3. For what combinations of the inputs D and EN will a D latch reset?

   (a) D = LOW, EN = LOW (b) D = LOW, EN = HIGH

   (c) D = HIGH, EN = LOW (d) D = HIGH, EN = HIGH

4. A flip-flop changes its state during the

   (a) complete operational cycle

   (b) falling edge of the clock pulse

   (c) rising edge of the clock pulse

   (d) both answers (b) and (c)

5. The purpose of the clock input to a flip-flop is to

   (a) clear the device (b) set the device

   (c) always cause the output to change states

   (d) cause the output to assume a state dependent on the controlling (J-K or D) inputs.

6. For an edge-triggered D flip-flop,

   (a) a change in the state of the flip-flop can occur only at a clock pulse edge

   (b) the state that the flip-flop goes to depends on the D input

   (c) the output follows the input at each clock pulse

   (d) all of these answers

7. A feature that distinguishes the J-K flip-flop from the D flip-flop is the

   (a) toggle condition (b) preset input

   (c) type of clock (d) clear input

8. A flip-flop is SET when

   (a) J = 0, K = 0 (b) J = 0, K = 1

   (c) J = 1, K = 0 (d) J = 1, K = 1

9. A J-K flip-flop with J = 1 and K = 1 has a 10 kHz clock input. The Q output is

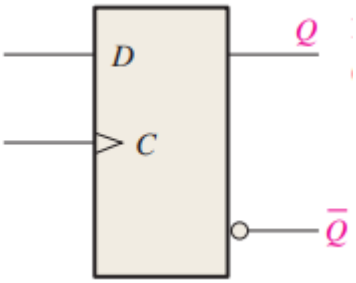
   (a) constantly HIGH (b) constantly LOW

   (c) a 10 kHz square wave (d) a 5 kHz square wave

Answer to the following questions

1. List three types of latches.
2. Define the following: (a) set-up time (b) hold time
3. How many flip-flops are required to divide a frequency by thirty-two?
4. What is the Q output of a D latch when EN = 1 and D = 1
5. Explain the function of an SR Latch active low, by the logic circuit, the behavior of cases to have its truth table.
6. Explain the function of an SR Flip-flop, by the logic circuit, the behavior of cases to have its truth table.

7. Given the below information,

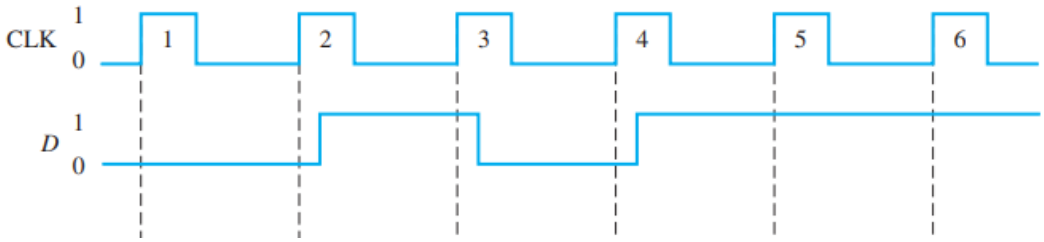


Truth table for a positive edge-triggered D flip-flop.

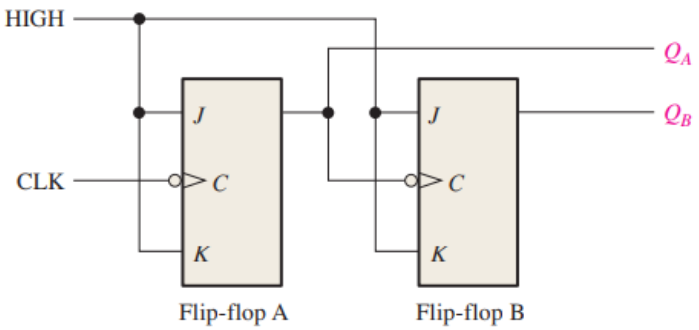
Inputs		Outputs		
D	**CLK**	***Q***	$\overline{Q}$	**Comments**
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH

Determine the Q and $\bar{Q}$ output waveforms of the flip-flop in Figure below for the D. Assume that the positive edge-triggered flip-flop is initially RESET.



8. J-K flip-flops are used to generate a binary count sequence (00, 01, 10, 11). Determine Q_A and Q_B in the figure shown below



Reference: Digital_Fundamentals_11ed_by_Thomas_L.Floyd

Chapter 8. Shift Registers

True or False

1. Shift registers consist of an arrangement of flip-flops.
2. A shift register cannot be used to store data.
3. A serial shift register accepts one bit at a time on a single line.
4. All shift registers are defined by specified sequences.
5. A shift register counter is a shift register with the serial output connected back to the serial input.
6. A shift register with four stages can store a maximum count of fifteen.
7. The Johnson counter is a special type of shift register.
8. The modulus of an 8-bit Johnson counter is eight.
9. A ring counter uses one flip-flop for each state in its sequence.
10. A shift register cannot be used as a time delay device.

Circle the correct answer

1. A register's functions include

(a) data storage (b) data movement

(c) neither (a) not (b) (d) both (a) and (b)

2. To enter a byte of data serially into an 8-bit shift register, there must be

(a) one clock pulse (b) two clock pulses

(c) four clock pulses (d) eight clock pulses

3. To parallel load a byte of data into a shift register with a synchronous load, there must be

(a) one clock pulse (b) one clock pulse for each 1 in the data

(c) eight clock pulses (d) one clock pulse for each 0 in the data

4. The group of bits 10110101 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state of 11100100. After two clock pulses, the register contains

(a) 01011110 (b) 10110101

(c) 01111001 (d) 00101101

5. With a 100 kHz clock frequency, eight bits can be serially entered into a shift register in

(a) 80 ms (b) 8 ms

(c) 80 ms (d) 10 ms

6. With a 1 MHz clock frequency, eight bits can be parallel entered into a shift register

(a) in 8 ms (b) in the propagation delay time of eight flip-flops

(c) in 1 ms (d) in the propagation delay time of one flip-flop

7. A modulus-8 Johnson counter requires

(a) eight flip-flops (b) four flip-flops

(c) five flip-flops (d) twelve flip-flops

8. A modulus-8 ring counter requires

(a) eight flip-flops (b) four flip-flops

(c) five flip-flops (d) twelve flip-flops

9. When an 8-bit serial in/serial out shift register is used for a 24 ms time delay, the clock frequency must be

(a) 41.67 kHz (b) 333 kHz

(c) 125 kHz (d) 8 MHz

10. The purpose of the ring counter in the keyboard encoding circuit of Figure 8–36 is

(a) to sequentially apply a HIGH to each row for detection of key closure

(b) to provide trigger pulses for the key code register

(c) to sequentially apply a LOW to each row for detection of key closure

(d) to sequentially reverse bias the diodes in each row

Answer to following questions

1. What determines the storage capacity of a shift register?
2. What two principal functions are performed by a shift register?
3. By a truth table show the states of the 5-bit Synchronous shift register using D flip-flops for the specified data input A=11010 and clock pulse. Assume that the register is initially cleared (all 0s).

Chapter 9. Counters

True or False

1. A state machine is a sequential circuit having a limited number of states occurring in a prescribed order.
2. Synchronous counters cannot be realized using J-K flip-flops.
3. An asynchronous counter is also known as a ripple counter.
4. A decade counter has twelve states.
5. A counter with four stages has a maximum modulus of sixteen.
6. To achieve a maximum modulus of 32, sixteen stages are required.
7. If the present state is 1000, the next state of a 4-bit up/down counter in the DOWN mode is 0111.
8. Two cascaded decade counters divide the clock frequency by 10.
9. A counter with a truncated sequence has less than its maximum number of states.
10. To achieve a modulus of 100, ten decade counters are required.

Circle the correct answer

1. A Moore state machine consists of combinational logic circuits that determine
   (a) sequences (b) memory
   (c) both (a) and (b) (d) neither (a) nor (b)
2. The output of a Mealy machine depends on its
   (a) inputs (b) next state (c) present state (d) answers (a) and (c)
3. The maximum cumulative delay of an asynchronous counter must be
   (a) more than the period of the clock waveform
   (b) less than the period of the clock waveform
   (c) equal to the period of the clock waveform
   (d) both (a) and (c)
4. A decade counter with a count of zero (0000) through nine (1001) is known as
   (a) an ASCII counter (b) a binary counter
   (c) A BCD counter (d) a decimal counter
5. The modulus of a counter is
   (a) the number of flip-flops
   (b) the actual number of states in its sequence
   (c) the number of times it recycles in a second
   (d) the maximum possible number of states

6. A 3-bit binary counter has a maximum modulus of

(a) 3 (b) 6 (c) 8 (d) 16

7. A 5-bit binary counter has a maximum modulus of

(a) 4 (b) 8 (c) 16 (d) 32

8. A modulus-12 counter must have

(a) 12 flip-flops (b) 3 flip-flops

(c) 4 flip-flops (d) synchronous clocking

9. Which one of the following is an example of a counter with a truncated modulus?

(a) Modulus 8 (b) Modulus 14

(c) Modulus 16 (d) Modulus 32

10. A BCD counter is an example of

(a) a full-modulus counter (b) a decade counter

(c) a truncated-modulus counter (d) answers (b) and (c)

11. Which of the following is a valid state in an 8421 BCD counter?

(a) 1010 (b) 1011 (c) 1111 (d) 1000

12. Three cascaded modulus-10 counters have an overall modulus of

(a) 30 (b) 100 (c) 1000 (d) 10,000

Answer the following questions

1. What does the term asynchronous mean in relation to counters?

2. How many states does a modulus-14 counter have? What is the minimum number of flip-flops required?

3. How does a synchronous counter differ from an asynchronous counter?

4. A 4-bit up/down binary counter is in the DOWN mode and in the 1010 state. On the next clock pulse, to what state does the counter go?

5. What is the terminal count of a 4-bit binary counter in the UP mode? In the DOWN mode? What is the next state after the terminal count in the DOWN mode?

6. How many decade counters are necessary to implement a divide-by-1000 (modulus-1000) counter? A divide-by-10,000?

7. Show with general block diagrams how to achieve each of the following, using a flip-flop, a decade counter, and a 4-bit binary counter, or any combination of these:

(a) Divide-by-20 counter (b) Divide-by-32 counter

(c) Divide-by-160 counter (d) Divide-by-320 counter

Chapter 10. Data Storage

True/False

1. A nibble consists of eight bits.
2. A memory cell can store a byte of data.
3. The location of a unit of data in a memory array is called its address.
4. A data bus is bidirectional in operation.
5. RAM is a random address memory.
6. Data stored in a static RAM is retained even after power is removed.
7. Cache is a type of memory used for intermediate or temporary storage of data.
8. Dynamic RAMs must be periodically refreshed to retain data.
9. ROM is a read-only memory.
10. A flash memory uses a flashing beam of light to store data.
11. Registers are at the top of a memory hierarchy.
12. Cloud storage is accessed through the Internet.

Circle the correct answer

1. The bit capacity of a memory that has 512 addresses and can store 8 bits at each address is

   (a) 512 (b) 1024 (c) 2048 (d) 4096

2. A 16-bit word consists of

   (a) 3 bytes (b) 4 nibbles (c) 4 bytes (d) 3 bytes and 1 nibble

3. Data are stored in a random-access memory (RAM) during the

   (a) read operation (b) enable operation (c) write operation (d) addressing operation

4. Data that are stored at a given address in a random-access memory (RAM) are lost when

   (a) power goes off (b) the data are read from the address

   (c) new data are written at the address (d) answers (a) and (c)

5. A ROM is a

   (a) nonvolatile memory (b) volatile memory

   (c) read/write memory (d) byte-organized memory

6. A memory with 512 addresses has

(a) 512 address lines (b) 12 address lines (c) 1 address line (d) 9 address lines

7. A byte-organized memory has

(a) 1 data output line (b) 4 data output lines (c) 8 data output lines (d) 16 data output lines

8. The storage element of a DRAM is a

(a) resistor (b) transistor (c) capacitor (d) diode

9. ADDRESS-BURST is a feature of

(a) synchronous SRAM (b) asynchronous SRAM

(c) fast page mode DRAM (d) synchronous DRAM

10. In a computer, the BIOS programs are stored in the

(a) ROM (b) RAM (c) SRAM (d) DRAM

11. SRAM, DRAM, flash, and EEPROM are all

(a) magneto-optical storage devices (b) semiconductor storage devices

(c) magnetic storage devices (d) optical storage devices

12. Optical storage devices employ

(a) ultraviolet light (b) electromagnetic fields

(c) optical couplers (d) lasers

13. Memory latency is

(a) average down time (b) time to reference a block of data

(c) processor access time (d) the hit rate

14. A facility that houses a cloud storage system is called a

(a) server (b) data center

(c) computer center (d) cloud hous

Answer the following questions

1. What is the smallest unit of data that can be stored in a memory?
2. What is the bit capacity of a memory that can store 256 bytes of data?
3. List the major types of magnetic storage.
4. Generally, how is a magnetic disk organized?
5. How are data written on and read from a magneto-optical disk?
6. List the types of optical storage.

7. Draw the Relationship of Cost, Capacity, and Access Time of memory Hierarchy.
8. State the purpose of memory hierarchy.
9. What is access time?
10. How does memory capacity affect the cost per bit?
11. Does higher level memory generally have lower capacity than lower level memory?
12. What is a hit? A miss?
13. What determines the efficiency of the memory hierarchy?
14. What is the difference between RAM and ROM?
15. Draw the ROM and RAM families.
16. What is a cloud storage system?
17. What is a server?
18. How does a user connect to a cloud storage system?
19. Name three advantages of a cloud system.
20. Draw the cloud system.
21. The figure below shows a Magnetic Hard disk, give the name of the part where the arrow points

End