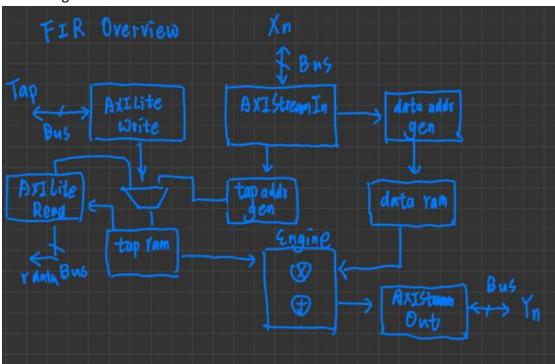
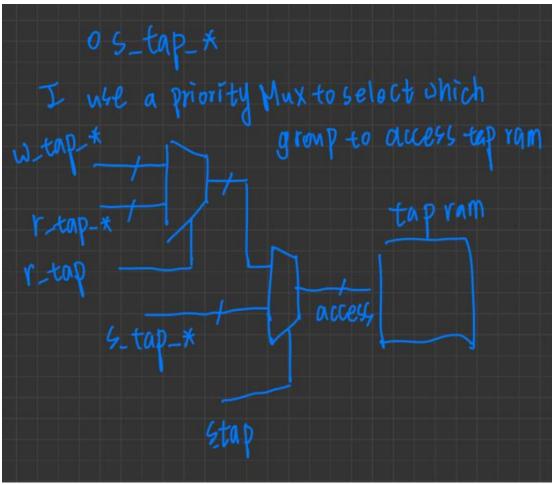
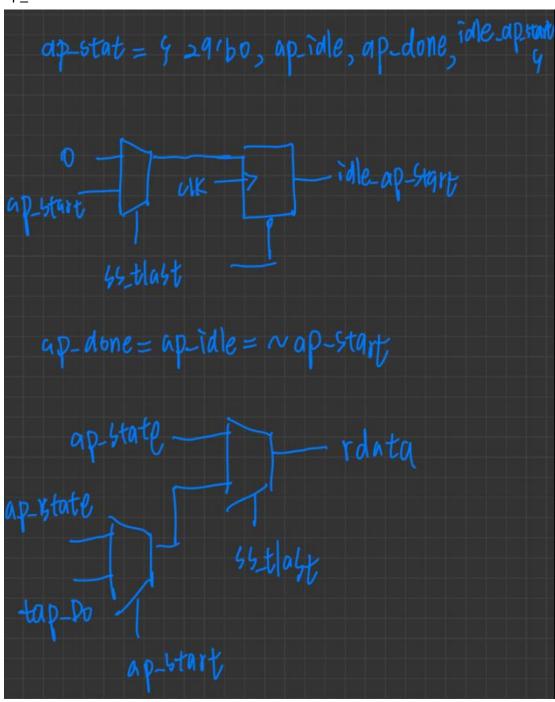
Block Diagram



SRAM Operation





Resource usage

Itilization	Post-S	Post-Synthesis Post-Implementation				
			Graph Table			
Resource	Estimation	Available	Utilization %			
LUT	403	53200	0.76			
FF	114	106400	0.11			
DSP	3	220	1.36			
10	431	125	344.80			
BUFG	4	32	12.50			

Report timing

Best: 12ns

Design Timing Summary

```
Worst Negative Slack (WNS): 1.223 ns Worst Hold Slack (WHS): 0.147 ns Worst Pulse Width Slack (WPWS): 5.500 ns Total Negative Slack (TNS): 0.000 ns Total Hold Slack (THS): 0.000 ns Total Pulse Width Negative Slack (TPWS): 0.000 ns Number of Failing Endpoints: 0 Number of Failing Endpoints: 0 Number of Failing Endpoints: 0 Total Number of Endpoints: 47 Total Number of Endpoints: 115

All user specified timing constraints are met.

***Bax Delay Paths**

Slack (MET): 1.223ns (required time - arrival time)
Source: genblk1. fir data reg[16]/C (rising edge-triggered cell FDCE clocked by axis_clk {rise@0.000ns fall@6.000ns period=12.000ns}))

Path Group: axis_clk
Path Group: axis_clk
Path Type: Setup (Max at Slow Process Corner)
Requirement: 12.000ns (axis_clk rise@12.000ns - axis_clk rise@0.000ns fall@6.000ns period=12.000ns}))

Data Path Delay: 10.672ns (logic 8.380ns (78.520%) route 2.292ns (21.480%))
Logic Levels: 9 (CARRY4=5 DSP48E1=2 LUT2=2)
Clock Path Skew: -0.145ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): 2.128ns = (14.128 - 12.000)
Source Clock Delay (SCD): 2.456ns
Clock Uncertainty: 0.035ns ((TS)2 + TIJO2)^1/2 + DJ) / 2 + PE
Total System Jitter (TJ): 0.000ns
Discrete Jitter (TS): 0.071ns (DD): 0.000ns
Phase Error (PE): 0.000ns
```

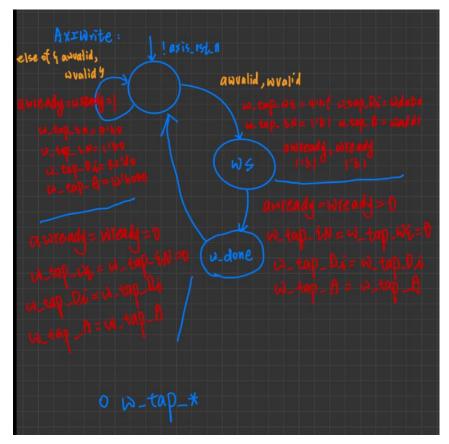
Over:10ns

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-0.777 ns	Worst Hold Slack (WHS):	0.147 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	-6.889 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	12	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	47	Total Number of Endpoints:	47	Total Number of Endpoints:	115

FSM

AXIWrite



AXIRead

```
AxI Read

L! axis_vet_n

else

avalid=veady=1

aveady=valid=0

r(tap_we=4/ho)

tap_we=0

tap_we=0
```

