波形配置界限验证

CH的波形配置参数存在问题，以下信息提供了AIOS在波形配置验证上的测试结果以及提议了新波形配置参数，供CH 参考。

为了适配活体检测应用下的检出结果CH发布了第三版的波形，如下，发布时间：6月18日

注：AIOS 到场南京第二次 Workshop 现场讨论之后

```
sensorStop
flushCfg
dfeDataOutputMode 1
channelCfg 15 6 0
adcCfg 2 1
adcbufCfg -1 0 0 1 1
profileCfg 0 60.25 10 6 80 0 0 46.5 0 128 2000 0 0 40
chirpCfg 0 0 0 0 0 0 0 2
chirpCfg 1 1 0 0 0 0 0 4
chirpCfg 2 2 0 0 0 0 0 2
chirpCfg 3 3 0 0 0 0 0 4
frameCfg 0 3 128 0 20 1 0
lowPower 0 1
sensorStart
```

AIOS进行波形配置后总结出了一些问题所在，需要与 CH 深入探讨

问题所在：

1、profileCfg中的时间设置有问题

=》CH的frameCfg中的periodicity太小

2、chirpCfg配置数量太多

=》导致内存不够，已超过L3 的size

```
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channelCfg 15 6 0
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profileCfg 0 60.25 10 6 80 0 0 46.5 0 128 2000 0 0 40
chirpCfg 0 0 0 0 0 0 0 2
chirpCfg 1 1 0 0 0 0 0 4
chirpCfg 2 2 0 0 0 0 0 2
chirpCfg 3 3 0 0 0 0 0 4
frameCfg 0 3 128 0 20 1 0
lowPower 0 1
sensorStart
```

测试验证现象：

sensorStop后，Task 堆栈使用情况

```
Data Path Stopped (last frame processing done)
Task Stack Usage (Note: CLI and sensor Management Task not reported) ==========
            Task Name         Size         Used         Free
                 Init         2048         1988           60
      Mmwave Control          3072         2368          704
          ObjDet DPM          4096         2344         1752
HWI Stack (same as System Stack) Usage ============
                             Size         Used         Free
                             2048          548         1500
```

```
Debug: Sending rlRfSetLdoBypassConfig with 0 0 0
Debug: Init Calibration Status = 0x1ffe
Error: mmWave Config failed [Error code: -3110 Subsystem: 80]
Error -1
mmwDemo:/>
mmwDemo:/>profileCfg 0 60.25 10 6 39 0 0 46.5 0 128 2000 0 0 40
Done
mmwDemo:/>
mmwDemo:/>sensorStart
[MmwDemo_CLISensorStart]sensorState:1
Error: mmWave Config failed [Error code: -3108 Subsystem: 41]
```

```
                                                    outside[100us,1.342s] */
#define RL_RET_CODE_FRAME_PERIOD_1INVAL_IN          (80U) /* Frame ON time > Frame periodicity */
#define RL_RET_CODE_FRAME_TRIG_SEL_INVAL_IN         (81U) /* Trigger select is outside[1,2] */
#define RL_RET_CODE_FRAME_TRIG_DELAY_INVAL_IN       (unsigned int)83U  er delay > 100us */
#define RL_RET_CODE_FRAME_IS_ONGOING                (83U) /* API issued when frame is ongoing */
```

AIOS 建议方案：

1、减少两个chirp

2、增加frame周期 =》frameCfg合理设置在50左右

```
sensorStop
flushCfg
dfeDataOutputMode 1
channelCfg 15 6 0
adcCfg 2 1
adcbufCfg -1 0 1 1 1
profileCfg 0 60.25 10 6 80 0 0 46.5 0 128 2000 0 0 40
chirpCfg 0 0 0 0 0 0 0 2
chirpCfg 1 1 0 0 0 0 0 4
frameCfg 0 1 128 0 52 1 0
lowPower 0 1
sensorStart
```

验证结果：

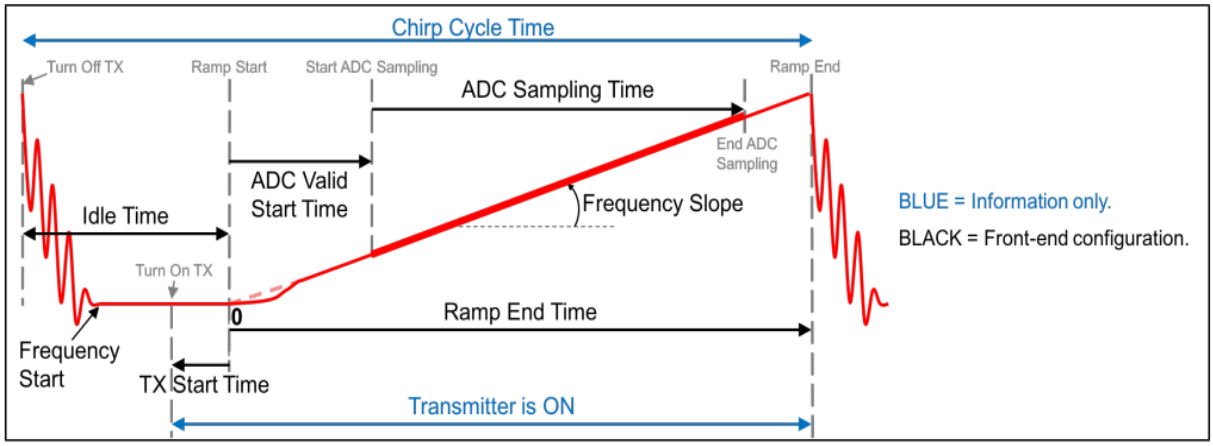
在AIOS建议方案下，尽量保留CH 原始波形配置，

1、减少2个chirp后L3 Ram的占用，512KB

rx	4
chirps	2
adc samples	128
byte per sample	4
loops	128
total size	524288

```
App: Issuing Pre-start Config IOCTL (subFrameIndx = 0)
========== Memory Stats ==========
                          Size        Used        Free     DPCUsed
System Heap(TCM)         32768       22032       10736        2048
             L3         786432      524288      262144
            TCM           4096         256        3840
```

2、frameCfg中periodicity的配置建议改为50

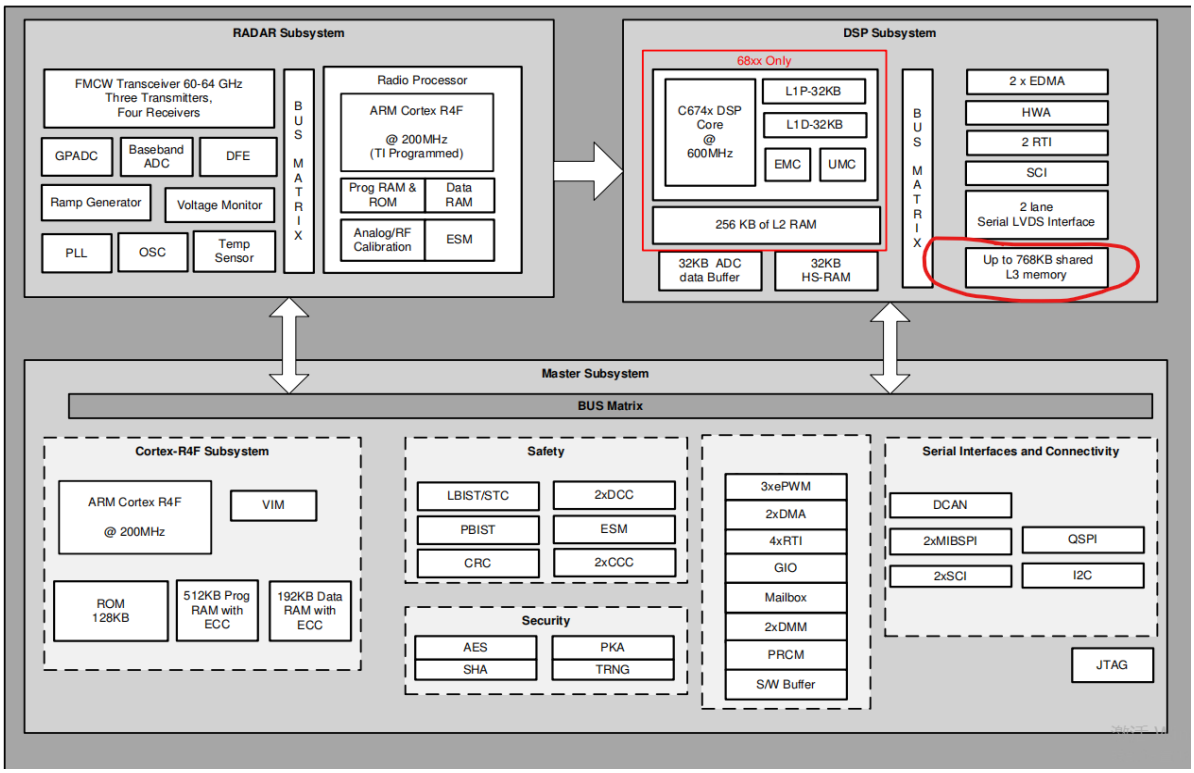


L3 Memory 限制信息，供参考

application from QSPI flash memory)

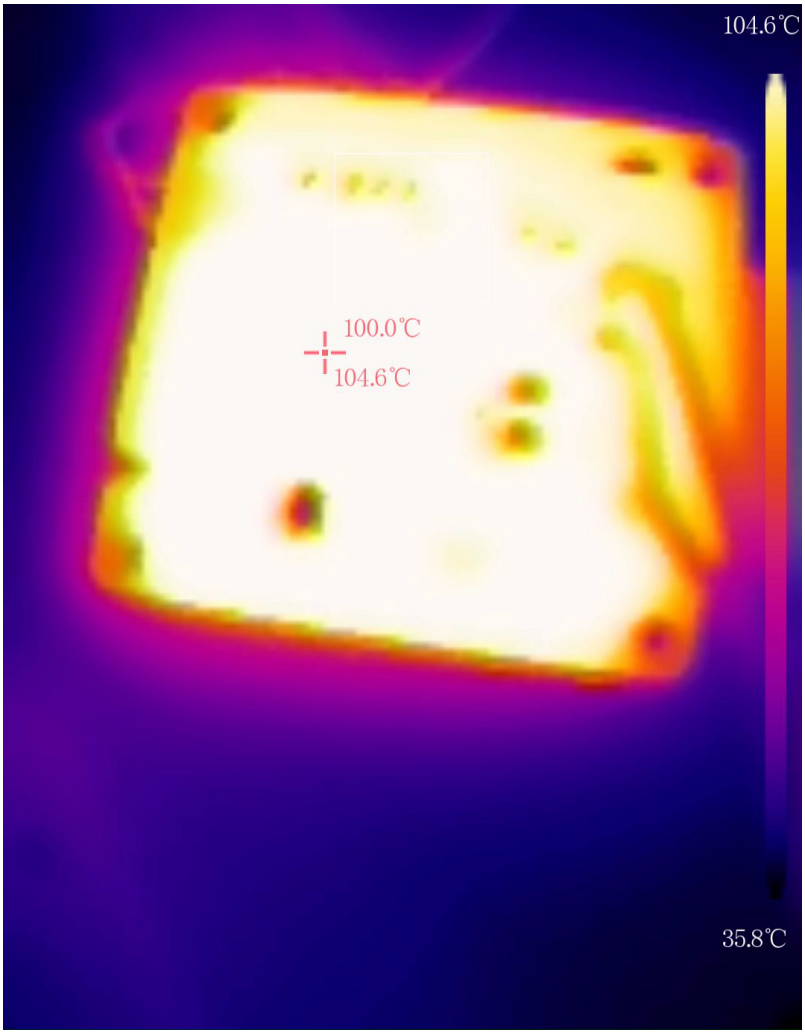
- Internal memory with ECC
  - 1.75 MB, divided into MSS program RAM (512 KB), MSS data RAM (192 KB), DSP L1 RAM (64KB) and L2 RAM (256 KB), and L3 radar data cube RAM (768 KB)

Figure 3-1. 68xx Block Diagram



其他问题：

工作温度挺高，硬件设计需考虑散热



5.1 Absolute Maximum Ratings(1)(2)

PARAMETERS		MIN	MAX	UNIT
VDDIN	1.2 V digital power supply	–0.5	1.4	V
VIN_SRAM	1.2 V power rail for internal SRAM	–0.5	1.4	V
VNWA	1.2 V power rail for SRAM array back bias	–0.5	1.4	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	–0.5	3.8	V
VIOIN_18	1.8 V supply for CMOS IO	–0.5	2	V
VIN_18CLK	1.8 V supply for clock module	–0.5	2	V
VIOIN_18DIFF	1.8 V supply for LVDS port	–0.5	2	V
VIN_13RF1	1.3 V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could be shorted on the board.	–0.5	1.45	V
VIN_13RF2				
VIN_13RF1 (1-V Internal LDO bypass mode)	Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	–0.5	1.4	V
VIN_13RF2 (1-V Internal LDO bypass mode)				
VIN_18BB	1.8-V Analog baseband power supply	–0.5	2	V
VIN_18VCO supply	1.8-V RF VCO supply	–0.5	2	V
Input and output voltage range	Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State)	–0.3V	VIOIN + 0.3	V
	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input		VIOIN + 20% up to 20% of signal period	
CLKP, CLKM	Input ports for reference crystal	–0.5	2	V
Clamp current	Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	–20	20	mA
T_J	Operating junction temperature range	–40	105	°C
T_{STG}	Storage temperature range after soldered onto PC board	–55	150	°C