User's Guide
SNVU663–June 2019

LP87524B/J/P-Q1 Technical Reference Manual

This document provides the register bit values for the one-time programmable (OTP) bits of the orderable part number, LP87524B-Q1, LP87524J-Q1 and LP87524P-Q1.

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Trademarks

1 Introduction

The LP87524B/J/P-Q1 contains four step-down DC/DC converter cores, which are configured as 4 single phase outputs. These devices power AWR1642 and AWR1243 automotive radar devices and IWR1642 industrial radar devices.

This technical reference manual can be used as a reference for the LP87524B/J/P-Q1 default register bits after OTP memory download. This technical reference manual does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the LP87524B/J/P-Q1 Four 4-MHz Buck Converters for AWR and IWR MMICs datasheet.

2 Setup

There are a few important connections to ensure the LP87524B/J/P-Q1 is configured correctly, each of which are described in this section. Good examples of how to connect the radar devices to the LP87524B/J/P-Q1 PMICs are shown in Figure 1, Figure 2 and Figure 3. LDOs are not required as the device meets noise and ripple specifications with LC filters. Refer to XWR1xxx Power Management Optimizations – Low Cost LC Filter Solution application report.

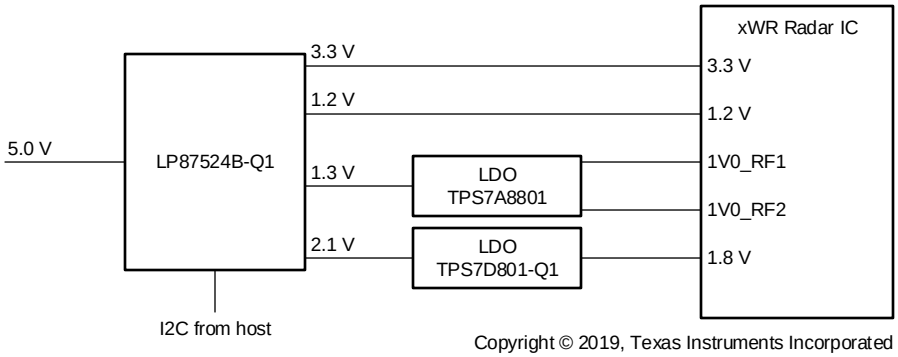

Figure 1. Typical Connection to LP87524B-Q1

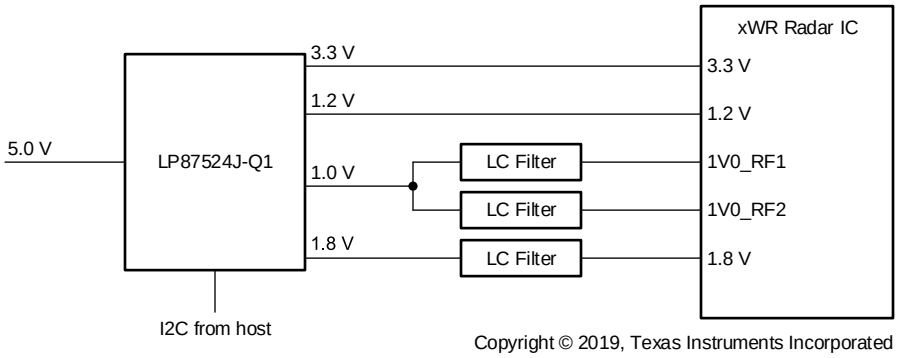

Figure 2. Typical Connection to LP87524J-Q1

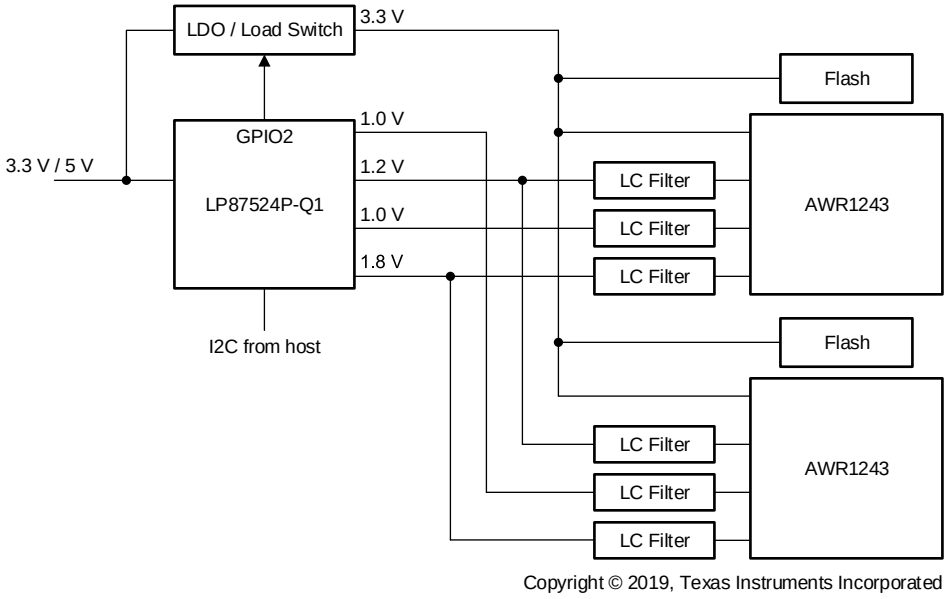

Figure 3. Typical Connection to LP87524P-Q1

2.1 SCL/SDA Pins

The SCL and SDA lines (pins 5 & 6, respectively) are used to communicate between the MCU and the LP87524B/J/P-Q1 PMIC using an I^2C compatible Interface. The I^2C compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed on the line and remain HIGH even when the bus is idle. The LP87524B/J/P-Q1 supports standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high-speed mode (3.4 MHz). For all I^2C protocol details refer to the device datasheet.

2.2 NRST Pin

The NRST pin (pin 20) is used to reset the device logic/enable device internal logic and IO interface. When the NRST voltage is below threshold level all power switches, references, controls, and bias circuitry of the LP87524B/J/P-Q1 device are turned off. When NRST is set to high level (and VANA is above UVLO level) this initiates power-on-reset (POR), OTP reading and enables the system I/O interface. The I^2C host must allow at least 1.2 ms before writing or reading data to the LP87524B/J/P-Q1. Device enters STANDBY-mode after internal startup sequence. The host can change the default register setting by I^2C if needed. The regulator(s) can be enabled/disabled by ENx pin(s) or by I^2C interface.

2.3 ENx (GPIOx) Pins

Enable pins EN1 (GPIO1), EN2 (GPIO2), EN3 (GPIO3) (pins 7, 15, 2) are I^2C configurable GPIO pins. The direction, function, and output type (open-drain or push-pull) are programmable for the GPIOs. When configured as EN pin, they can be used to start the buck converter startup sequence based on programmed timing. Shutdown times can be programmed as well. Drive these pins low to disable and high to enable when programmed as enable signal.

2.4 nINT

The nINT pin (pin 19) is an open-drain, active low output from the LP87524B/J/P-Q1 PMIC, and should be connected to a pullup resistor. After a power-on reset the LP87524B/J/P-Q1 PMIC requires a delay of 1.2 ms before there can be any communication through the I^2C interface.

3 Configuration

This section describes the default OTP settings.

3.1 Default OTP Configurations

All LP87524B/J/P-Q1 PMIC resource settings are stored in the form of volatile registers. These settings define, for example, buck output voltages, GPIO functionality, and power-up and power-down sequences. Refer to the datasheet for a full list of the setting registers.

Each device has predefined values stored in OTP which control the default configuration of the device. The tables in this section list the OTP-programmed values for each device.

Table 1 summarizes the main differences between the three OTP versions. Table 2 shows LP87524B-Q1, Table 8 shows LP87524J-Q1 and Table 14 shows LP87524P-Q1 settings for BUCK0, BUCK1, BUCK2 and BUCK3. Maximum allowed slew-rate for BUCKx depends on the output capacitance. Refer to the device datasheets for output capacitance boundary conditions.

Table 1. Differences between LP87524B/J/P-Q1 devices

Description	Bit name	LP87524B-Q1	LP87524J-Q1	LP87524P-Q1
Output voltage	BUCK0_VSET	3300 mV	3300 mV	1000 mV
	BUCK1_VSET	1200 mV	1200 mV	1200 mV
	BUCK2_VSET	1800 mV	1000 mV	1000 mV
	BUCK3_VSET	2300 mV	1800 mV	1800 mV
Peak current limit	ILIM0	2.5 A	2.5 A	4 A
	ILIM1	2.5 A	2.5 A	2.5 A
	ILIM2	5 A	5 A	4 A
	ILIM3	3.5 A	3.5 A	3.5 A
Force PWM mode or auto mode	BUCK0_FPWM	Auto	Auto	Force PWM
	BUCK1_FPWM	Auto	Auto	Force PWM
	BUCK2_FPWM	Force PWM	Force PWM	Force PWM
	BUCK3_FPWM	Force PWM	Force PWM	Force PWM
Startup and shutdown delay range	DOUBLE_DELAY, HALF_DELAY	0 ... 15 ms	0 ... 15 ms	0 ... 4.8 ms
Buck Startup Delays	BUCK0_STARTUP_DELAY	5 ms	5 ms	0.96 ms
	BUCK1_STARTUP_DELAY	5 ms	5 ms	2.24 ms
	BUCK2_STARTUP_DELAY	2 ms	2 ms	1.6 ms
	BUCK3_STARTUP_DELAY	0 ms	0 ms	0 ms
Buck Shutdown Delays	BUCK0_SHUTDOWN_DELAY	0 ms	0 ms	0.32 ms
	BUCK1_SHUTDOWN_DELAY	0 ms	0 ms	0.32 ms
	BUCK2_SHUTDOWN_DELAY	0 ms	0 ms	0.32 ms
	BUCK3_SHUTDOWN_DELAY	1 ms	1 ms	0.32 ms
GPIO2/3 Startup Delays	GPIO2_STARTUP_DELAY	5 ms	5 ms	2.88 ms
	GPIO3_STARTUP_DELAY	3 ms	3 ms	4.16 ms
GPIO2/3 Shutdown Delay	GPIO2_SHUTDOWN_DELAY	0 ms	0 ms	0.32 ms
	GPIO3_SHUTDOWN_DELAY	0 ms	0 ms	0 ms
GPIO output type	GPIO1_OD	Push-pull	Push-pull	Open drain
	GPIO2_OD	Open drain	Open drain	Open drain
	GPIO3_OD	Open drain	Open drain	Open drain
Input or output in GPIO mode	GPIO1_DIR	Input	Input	Output
	GPIO2_DIR	Output	Output	Output
	GPIO3_DIR	Output	Output	Output
Thermal warning level (125°C or 137°C)	TDIE_WARN_LEVEL	137°C	137°C	125°C

3.1.1 LP87524B-Q1 OTP Configuration

Table 2. BUCK0, BUCK1, BUCK2, BUCK3 OTP Settings

	Description	Bit Name	LP87524B-Q1	Configurable
General settings	Buck phase configuration (e.g. four single phase denoted as 1+1+1+1, four phase single output denoted as 4 ph).	N/A	1+1+1+1	No
	Switching frequency	N/A	4 MHz	No
	Spread spectrum	EN_SPREAD_SPEC	No	Yes
	Startup and shutdown delay range, 0...4.8 ms / 0... 9.6 ms / 0...15 ms / 0...30 ms	DOUBLE_DELAY, HALF_DELAY	0...15 ms	Yes
BUCK0	Output voltage	BUCK0_VSET	3300 mV	Yes
	Enable, ENx-pin or I^{2}C register	EN_BUCK0, EN_PIN_CTRL0, BUCK0_EN_PIN_SELECT	I^{2}C and EN1	Yes
	Force PWM mode or auto mode	BUCK0_FPWM	auto	Yes
	Force multiphase mode or auto mode	BUCK0_FPWM_MP	auto	Yes
	Peak current limit	ILIM0	2.5 A	Yes
	Slew rate	SLEW_RATE0	3.8 mV/µs	Yes
	Startup Delay	BUCK0_STARTUP_DELAY	5 ms	Yes
	Shutdown Delay	BUCK0_SHUTDOWN_DELAY	0 ms	Yes
BUCK1	Output voltage	BUCK1_VSET	1200 mV	Yes
	Enable, EN-pin or I^{2}C register	EN_BUCK1, EN_PIN_CTRL1, BUCK1_EN_PIN_SELECT	I^{2}C and EN1	Yes
	Force PWM mode or auto mode	BUCK1_FPWM	auto	Yes
	Peak current limit	ILIM1	2.5 A	Yes
	Slew rate	SLEW_RATE1	3.8 mV/µs	Yes
	Startup Delay	BUCK1_STARTUP_DELAY	5 ms	Yes
	Shutdown Delay	BUCK1_SHUTDOWN_DELAY	0 ms	Yes
BUCK2	Output voltage	BUCK2_VSET	1800 mV	Yes
	Enable, ENx-pin or I^{2}C register	EN_BUCK2, EN_PIN_CTRL2, BUCK2_EN_PIN_SELECT	I^{2}C and EN1	Yes
	Force PWM mode or auto mode	BUCK2_FPWM	Force PWM	Yes
	Force multiphase mode or auto mode	BUCK2_FPWM_MP	auto	Yes
	Peak current limit	ILIM2	5 A	Yes
	Slew rate	SLEW_RATE2	3.8 mV/µs	Yes
	Startup Delay	BUCK2_STARTUP_DELAY	2 ms	Yes
	Shutdown Delay	BUCK2_SHUTDOWN_DELAY	0 ms	Yes
BUCK3	Output voltage	BUCK3_VSET	2300 mV	Yes
	Enable, EN-pin or I^{2}C register	EN_BUCK3, EN_PIN_CTRL3, BUCK3_EN_PIN_SELECT	I^{2}C and EN1	Yes
	Force PWM mode or auto mode	BUCK3_FPWM	Force PWM	Yes
	Peak current limit	ILIM3	3.5 A	Yes
	Slew rate	SLEW_RATE3	3.8 mV/µs	Yes
	Startup Delay	BUCK3_STARTUP_DELAY	0 ms	Yes
	Shutdown Delay	BUCK3_SHUTDOWN_DELAY	1 ms	Yes

Table 3 lists the device settings for GPIOs.

Table 3. EN, CLKIN and GPIO Pin Settings

	Description	Bit Name	LP87524B-Q1	Configurable
EN1 (GPIO1) pin	EN1 (GPIO1) pin pulldown resistor enable or disable	EN1_PD	Enabled	Yes
EN2 (GPIO2) pin	EN2 (GPIO2) pin pulldown resistor enable or disable	EN2_PD	Disabled	Yes
EN3 (GPIO3) pin	EN3 (GPIO3) pin pulldown resistor enable or disable	EN3_PD	Disabled	Yes

Table 3. EN, CLKIN and GPIO Pin Settings (continued)

	Description	Bit Name	LP87524B-Q1	Configurable
CLKIN pin	CLKIN pin pull-down resistor enable or disable	CLKIN_PD	Enabled	Yes
	Frequency of external clock when connected to CLKIN	EXT_CLK_FREQ	2 MHz	Yes
	Mode for the internal PLL. When PLL disabled, internal RC OSC is used	PLL_MODE[1:0]	Enabled	Yes
EN1 (GPIO) control	Enable or GPIO	GPIO1_SEL	Enable	Yes
	Input or output in GPIO mode	GPIO1_DIR	Input	Yes
	Output type open drain or push-pull	GPIO1_OD	Push-pull	Yes
EN2 (GPIO) control	Enable or GPIO	GPIO2_SEL	GPIO	Yes
	Input or output in GPIO mode	GPIO2_DIR	Output	Yes
	Output type open drain or push-pull	GPIO2_OD	Open drain	Yes
	Pin control of GPIO, EN1 or EN3	EN_PIN_CTRL_GPIO2, EN_PIN_SELECT_GPIO2	EN1	Yes
	Startup Delay	GPIO2_STARTUP_DELAY	5 ms	Yes
	Shutdown Delay	GPIO2_SHUTDOWN_DELAY	0 ms	Yes
EN3 (GPIO) control	Enable or GPIO	GPIO3_SEL	GPIO	Yes
	Input or output in GPIO mode	GPIO3_DIR	Output	Yes
	Output type open drain or push-pull	GPIO3_OD	Open drain	Yes
	Pin control of GPIO, EN1 or EN2	EN_PIN_CTRL_GPIO3, EN_PIN_SELECT_GPIO3	EN1	Yes
	Startup Delay	GPIO3_ STARTUP_ DELAY	3 ms	Yes
	Shutdown Delay	GPIO3_ SHUTDOWN_ DELAY	0 ms	Yes

Table 4 shows device settings for PGOOD.

Table 4. PGOOD OTP Settings

	Description	Bit Name	LP87524B-Q1	Configurable
Signals monitored by PGOOD	BUCKx output voltage / voltage and current (master bucks)	PGx_SEL	Voltage	Yes
PGOOD mode selections	PGOOD thresholds for BUCKx (Undervoltage / Window (undervoltage and overvoltage))	PGOOD_WINDOW	Window	Yes
	PGOOD valid debounce time	PGOOD_SET_DELAY	11 ms	Yes
	PGOOD signal mode (status / latched until fault source read)	EN_PGFLT_STAT	Status	Yes
	PGOOD output mode (push-pull or open drain)	PGOOD_OD	Open drain	Yes
	PGOOD polarity (active high / active low)	PGOOD_POL	Active high (power valid)	Yes

Table 5 lists the device settings for thermal warning. Also refer to Table 7 for interrupt settings.

Table 5. Protections OTP Settings

	Description	Bit Name	LP87524B-Q1	Configurable
Protections	Thermal warning level (125°C or 137°C)	TDIE_WARN_LEVEL	137°C	Yes
	Input over-voltage protection	N/A	Enabled	No

Table 6 shows device settings for I^2C and OTP revision ID values.

Table 6. Device Identification and I^2C Settings

	Description	Bit Name	LP87524B-Q1	Configurable
I^2C slave ID (7-bit)	Slave address	N/A	0x60	No

Table 7 lists device settings for interrupts. When interrupt from an event is unmasked, an interrupt is generated to nINT pin.

Table 7. Interrupt Mask Settings

	Interrupt event	Bit Name	LP87524B-Q1	Configurable
General	Sync clock appears or disappears	SYNC_CLK_MASK	Unmasked	Yes
	Thermal warning	TDIE_WARN_MASK	Unmasked	Yes
	Load measurement ready	I_LOAD_READY_MASK	Masked	Yes
	Register reset	RESET_REG_MASK	Masked	Yes
BUCK0	Buck0 PGOOD has reached threshold level	BUCK0_PG_MASK	Masked	Yes
	Buck0 current limit triggered	BUCK0_ILIM_MASK	Masked	Yes
BUCK1	Buck1 PGOOD has reached threshold level	BUCK1_PG_MASK	Masked	Yes
	Buck1 current limit triggered	BUCK1_ILIM_MASK	Masked	Yes
BUCK2	Buck2 PGOOD has reached threshold level	BUCK2_PG_MASK	Masked	Yes
	Buck2 current limit triggered	BUCK2_ILIM_MASK	Masked	Yes
BUCK3	Buck3 PGOOD has reached threshold level	BUCK3_PG_MASK	Masked	Yes
	Buck3 current limit triggered	BUCK3_ILIM_MASK	Masked	Yes

3.1.1.1 Startup and Shutdown Sequence

Each of the bucks and GPOs on the LP87524B/J/P-Q1 can be set to startup and shutdown in a specific sequence. To configure the desired sequence the STARTUP_DELAY and SHUTDOWN_DELAY fields for each output need to be set to a value between 0x0 and 0xF. The delay time that this value corresponds to depends on the DOUBLE_DELAY bit and the HALF_DELAY bit located in the CONFIG register. A value of 0 on both of these bits will allow a delay ranging from 0 ms to 15 ms with 1 ms steps. Figure 4 shows default startup and shutdown sequence programmed to OTP, in this case with EN1 signal. Refer to the datasheet for a full description of all registers and their settings.

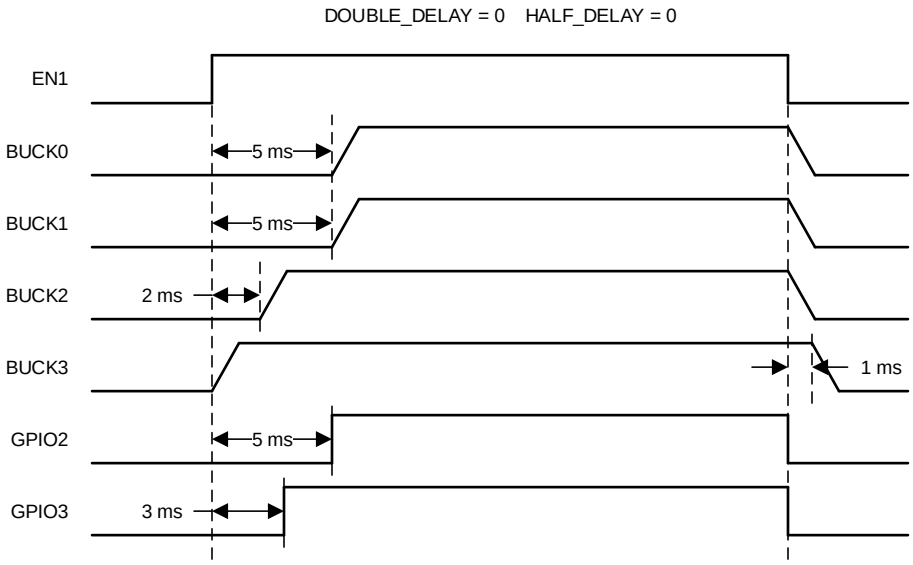

Figure 4. LP87524B-Q1 Startup and Shutdown Sequence Timing Diagram

3.1.2 LP87524J-Q1 OTP Configuration

Table 8. BUCK0, BUCK1, BUCK2, BUCK3 OTP Settings

	Description	Bit Name	LP87524J-Q1	Configurable
General settings	Buck phase configuration (e.g. four single phase denoted as 1+1+1+1, four phase single output denoted as 4 ph).	N/A	1+1+1+1	No
	Switching frequency	N/A	4 MHz	No
	Spread spectrum	EN_SPREAD_SPEC	No	Yes
	Startup and shutdown delay range, 0...4.8 ms / 0... 9.6 ms / 0...15 ms / 0...30 ms	DOUBLE_DELAY, HALF_DELAY	0...15 ms	Yes
BUCK0	Output voltage	BUCK0_VSET	3300 mV	Yes
	Enable, ENx-pin or I^2C register	EN_BUCK0, EN_PIN_CTRL0, BUCK0_EN_PIN_SELECT	I^2C and EN1	Yes
	Force PWM mode or auto mode	BUCK0_FPWM	auto	Yes
	Force multiphase mode or auto mode	BUCK0_FPWM_MP	auto	Yes
	Peak current limit	ILIM0	2.5 A	Yes
	Slew rate	SLEW_RATE0	3.8 mV/µs	Yes
	Startup Delay	BUCK0_STARTUP_DELAY	5 ms	Yes
	Shutdown Delay	BUCK0_SHUTDOWN_DELAY	0 ms	Yes
BUCK1	Output voltage	BUCK1_VSET	1200 mV	Yes
	Enable, EN-pin or I^2C register	EN_BUCK1, EN_PIN_CTRL1, BUCK1_EN_PIN_SELECT	I^2C and EN1	Yes
	Force PWM mode or auto mode	BUCK1_FPWM	auto	Yes
	Peak current limit	ILIM1	2.5 A	Yes
	Slew rate	SLEW_RATE1	3.8 mV/µs	Yes
	Startup Delay	BUCK1_STARTUP_DELAY	5 ms	Yes
	Shutdown Delay	BUCK1_SHUTDOWN_DELAY	0 ms	Yes

Table 8. BUCK0, BUCK1, BUCK2, BUCK3 OTP Settings (continued)

	Description	Bit Name	LP87524J-Q1	Configurable
BUCK2	Output voltage	BUCK2_VSET	1000 mV	Yes
	Enable, ENx-pin or I²C register	EN_BUCK2, EN_PIN_CTRL2, BUCK2_EN_PIN_SELECT	I²C and EN1	Yes
	Force PWM mode or auto mode	BUCK2_FPWM	Force PWM	Yes
	Force multiphase mode or auto mode	BUCK2_FPWM_MP	auto	Yes
	Peak current limit	ILIM2	5 A	Yes
	Slew rate	SLEW_RATE2	3.8 mV/µs	Yes
	Startup Delay	BUCK2_STARTUP_DELAY	2 ms	Yes
	Shutdown Delay	BUCK2_SHUTDOWN_DELAY	0 ms	Yes
BUCK3	Output voltage	BUCK3_VSET	1800 mV	Yes
	Enable, EN-pin or I²C register	EN_BUCK3, EN_PIN_CTRL3, BUCK3_EN_PIN_SELECT	I²C and EN1	Yes
	Force PWM mode or auto mode	BUCK3_FPWM	Force PWM	Yes
	Peak current limit	ILIM3	3.5 A	Yes
	Slew rate	SLEW_RATE3	3.8 mV/µs	Yes
	Startup Delay	BUCK3_STARTUP_DELAY	0 ms	Yes
	Shutdown Delay	BUCK3_SHUTDOWN_DELAY	1 ms	Yes

Table 9 lists the device settings for GPIOs.

Table 9. EN, CLKIN and GPIO Pin Settings

	Description	Bit Name	LP87524J-Q1	Configurable
EN1 (GPIO1) pin	EN1 (GPIO1) pin pulldown resistor enable or disable	EN1_PD	Enabled	Yes
EN2 (GPIO2) pin	EN2 (GPIO2) pin pulldown resistor enable or disable	EN2_PD	Disabled	Yes
EN3 (GPIO3) pin	EN3 (GPIO3) pin pulldown resistor enable or disable	EN3_PD	Disabled	Yes
CLKIN pin	CLKIN pin pull-down resistor enable or disable	CLKIN_PD	Enabled	Yes
	Frequency of external clock when connected to CLKIN	EXT_CLK_FREQ	2 MHz	Yes
	Mode for the internal PLL. When PLL disabled, internal RC OSC is used	PLL_MODE[1:0]	Enabled	Yes
EN1 (GPIO) control	Enable or GPIO	GPIO1_SEL	Enable	Yes
	Input or output in GPIO mode	GPIO1_DIR	Input	Yes
	Output type open drain or push-pull	GPIO1_OD	Push-pull	Yes
EN2 (GPIO) control	Enable or GPIO	GPIO2_SEL	GPIO	Yes
	Input or output in GPIO mode	GPIO2_DIR	Output	Yes
	Output type open drain or push-pull	GPIO2_OD	Open drain	Yes
	Pin control of GPIO, EN1 or EN3	EN_PIN_CTRL_GPIO2, EN_PIN_SELECT_GPIO2	EN1	Yes
	Startup Delay	GPIO2_STARTUP_DELAY	5 ms	Yes
	Shutdown Delay	GPIO2_SHUTDOWN_DELAY	0 ms	Yes
EN3 (GPIO) control	Enable or GPIO	GPIO3_SEL	GPIO	Yes
	Input or output in GPIO mode	GPIO3_DIR	Output	Yes
	Output type open drain or push-pull	GPIO3_OD	Open drain	Yes
	Pin control of GPIO, EN1 or EN2	EN_PIN_CTRL_GPIO3, EN_PIN_SELECT_GPIO3	EN1	Yes
	Startup Delay	GPIO3_ STARTUP_ DELAY	3 ms	Yes
	Shutdown Delay	GPIO3_ SHUTDOWN_ DELAY	0 ms	Yes

Table 10 shows device settings for PGOOD.

Table 10. PGOOD OTP Settings

	Description	Bit Name	LP87524J-Q1	Configurable
Signals monitored by PGOOD	BUCKx output voltage / voltage and current (master bucks)	PGx_SEL	Voltage	Yes
PGOOD mode selections	PGOOD thresholds for BUCKx (Undervoltage / Window (undervoltage and overvoltage))	PGOOD_WINDOW	Window	Yes
	PGOOD valid debounce time	PGOOD_SET_DELAY	11 ms	Yes
	PGOOD signal mode (status / latched until fault source read)	EN_PGFLT_STAT	Status	Yes
	PGOOD output mode (push-pull or open drain)	PGOOD_OD	Open drain	Yes
	PGOOD polarity (active high / active low)	PGOOD_POL	Active high (power valid)	Yes

Table 11 lists the device settings for thermal warning. Also refer to Table 13 for interrupt settings.

Table 11. Protections OTP Settings

	Description	Bit Name	LP87524J-Q1	Configurable
Protections	Thermal warning level (125°C or 137°C)	TDIE_WARN_LEVEL	137°C	Yes
	Input over-voltage protection	N/A	Enabled	No

Table 12 shows device settings for I^2C and OTP revision ID values.

Table 12. Device Identification and I^2C Settings

	Description	Bit Name	LP87524J-Q1	Configurable
I^2C slave ID (7-bit)	Slave address	N/A	0x60	No

Table 13 lists device settings for interrupts. When interrupt from an event is unmasked, an interrupt is generated to nINT pin.

Table 13. Interrupt Mask Settings

	Interrupt event	Bit Name	LP87524J-Q1	Configurable
General	Sync clock appears or disappears	SYNC_CLK_MASK	Unmasked	Yes
	Thermal warning	TDIE_WARN_MASK	Unmasked	Yes
	Load measurement ready	I_LOAD_READY_MASK	Masked	Yes
	Register reset	RESET_REG_MASK	Masked	Yes
BUCK0	Buck0 PGOOD has reached threshold level	BUCK0_PG_MASK	Masked	Yes
	Buck0 current limit triggered	BUCK0_ILIM_MASK	Masked	Yes
BUCK1	Buck1 PGOOD has reached threshold level	BUCK1_PG_MASK	Masked	Yes
	Buck1 current limit triggered	BUCK1_ILIM_MASK	Masked	Yes
BUCK2	Buck2 PGOOD has reached threshold level	BUCK2_PG_MASK	Masked	Yes
	Buck2 current limit triggered	BUCK2_ILIM_MASK	Masked	Yes
BUCK3	Buck3 PGOOD has reached threshold level	BUCK3_PG_MASK	Masked	Yes
	Buck3 current limit triggered	BUCK3_ILIM_MASK	Masked	Yes

3.1.2.1 Startup and Shutdown Sequence

Figure 5 shows default startup and shutdown sequence programmed to OTP, in this case with EN1 signal. Refer to the datasheet for a full description of all registers and their settings.

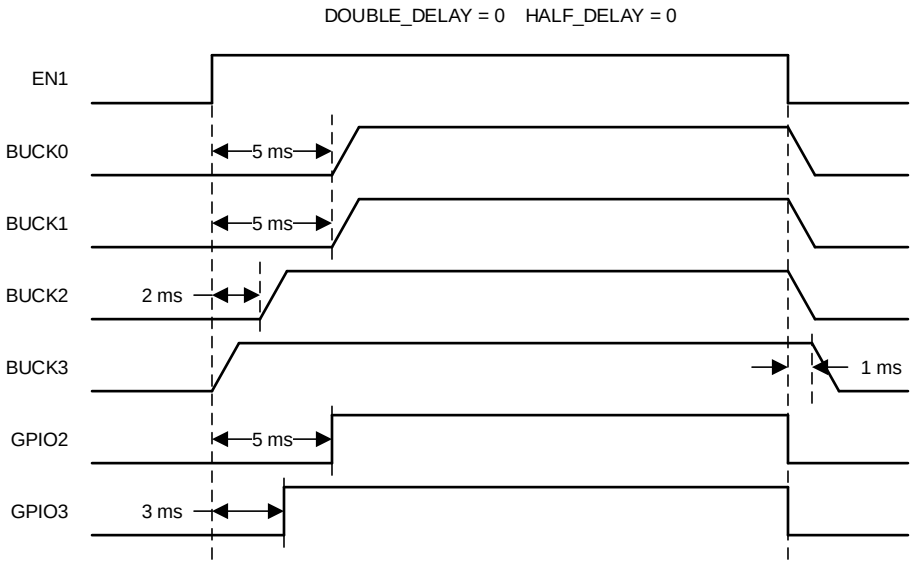

Figure 5. LP87524J-Q1 Startup and Shutdown Sequence Timing Diagram

3.1.3 LP87524P-Q1 OTP Configuration

Table 14. BUCK0, BUCK1, BUCK2, BUCK3 OTP Settings

	Description	Bit Name	LP87524P-Q1	Configurable
General settings	Buck phase configuration (e.g. four single phase denoted as 1+1+1+1, four phase single output denoted as 4 ph).	N/A	1+1+1+1	No
	Switching frequency	N/A	4 MHz	No
	Spread spectrum	EN_SPREAD_SPEC	No	Yes
	Startup and shutdown delay range, 0...4.8 ms / 0... 9.6 ms / 0...15 ms / 0...30 ms	DOUBLE_DELAY, HALF_DELAY	0...4.8 ms	Yes
BUCK0	Output voltage	BUCK0_VSET	1000 mV	Yes
	Enable, ENx-pin or I^2C register	EN_BUCK0, EN_PIN_CTRL0, BUCK0_EN_PIN_SELECT	I^2C and EN1	Yes
	Force PWM mode or auto mode	BUCK0_FPWM	Force PWM	Yes
	Force multiphase mode or auto mode	BUCK0_FPWM_MP	auto	Yes
	Peak current limit	ILIM0	4 A	Yes
	Slew rate	SLEW_RATE0	3.8 mV/µs	Yes
	Startup Delay	BUCK0_STARTUP_DELAY	0.96 ms	Yes
	Shutdown Delay	BUCK0_SHUTDOWN_DELAY	0.32 ms	Yes
BUCK1	Output voltage	BUCK1_VSET	1200 mV	Yes
	Enable, EN-pin or I^2C register	EN_BUCK1, EN_PIN_CTRL1, BUCK1_EN_PIN_SELECT	I^2C and EN1	Yes
	Force PWM mode or auto mode	BUCK1_FPWM	Force PWM	Yes
	Peak current limit	ILIM1	2.5 A	Yes
	Slew rate	SLEW_RATE1	3.8 mV/µs	Yes
	Startup Delay	BUCK1_STARTUP_DELAY	2.24 ms	Yes
	Shutdown Delay	BUCK1_SHUTDOWN_DELAY	0.32 ms	Yes

Table 14. BUCK0, BUCK1, BUCK2, BUCK3 OTP Settings (continued)

	Description	Bit Name	LP87524P-Q1	Configurable
BUCK2	Output voltage	BUCK2_VSET	1000 mV	Yes
	Enable, ENx-pin or I^{2}C register	EN_BUCK2, EN_PIN_CTRL2, BUCK2_EN_PIN_SELECT	I^{2}C and EN1	Yes
	Force PWM mode or auto mode	BUCK2_FPWM	Force PWM	Yes
	Force multiphase mode or auto mode	BUCK2_FPWM_MP	auto	Yes
	Peak current limit	ILIM2	4 A	Yes
	Slew rate	SLEW_RATE2	3.8 mV/µs	Yes
	Startup Delay	BUCK2_STARTUP_DELAY	1.6 ms	Yes
	Shutdown Delay	BUCK2_SHUTDOWN_DELAY	0.32 ms	Yes
BUCK3	Output voltage	BUCK3_VSET	1800 mV	Yes
	Enable, EN-pin or I^{2}C register	EN_BUCK3, EN_PIN_CTRL3, BUCK3_EN_PIN_SELECT	I^{2}C and EN1	Yes
	Force PWM mode or auto mode	BUCK3_FPWM	Force PWM	Yes
	Peak current limit	ILIM3	3.5 A	Yes
	Slew rate	SLEW_RATE3	3.8 mV/µs	Yes
	Startup Delay	BUCK3_STARTUP_DELAY	0 ms	Yes
	Shutdown Delay	BUCK3_SHUTDOWN_DELAY	0.32 ms	Yes

Table 15 lists the device settings for GPIOs.

Table 15. EN, CLKIN and GPIO Pin Settings

	Description	Bit Name	LP87524P-Q1	Configurable
EN1 (GPIO1) pin	EN1 (GPIO1) pin pulldown resistor enable or disable	EN1_PD	Enabled	Yes
EN2 (GPIO2) pin	EN2 (GPIO2) pin pulldown resistor enable or disable	EN2_PD	Disabled	Yes
EN3 (GPIO3) pin	EN3 (GPIO3) pin pulldown resistor enable or disable	EN3_PD	Disabled	Yes
CLKIN pin	CLKIN pin pull-down resistor enable or disable	CLKIN_PD	Enabled	Yes
	Frequency of external clock when connected to CLKIN	EXT_CLK_FREQ	2 MHz	Yes
	Mode for the internal PLL. When PLL disabled, internal RC OSC is used	PLL_MODE[1:0]	Enabled	Yes
EN1 (GPIO) control	Enable or GPIO	GPIO1_SEL	Enable	Yes
	Input or output in GPIO mode	GPIO1_DIR	Output	Yes
	Output type open drain or push-pull	GPIO1_OD	Open drain	Yes
EN2 (GPIO) control	Enable or GPIO	GPIO2_SEL	GPIO	Yes
	Input or output in GPIO mode	GPIO2_DIR	Output	Yes
	Output type open drain or push-pull	GPIO2_OD	Open drain	Yes
	Pin control of GPIO, EN1 or EN3	EN_PIN_CTRL_GPIO2, EN_PIN_SELECT_GPIO2	EN1	Yes
	Startup Delay	GPIO2_STARTUP_DELAY	2.88 ms	Yes
	Shutdown Delay	GPIO2_SHUTDOWN_DELAY	0.32 ms	Yes
EN3 (GPIO) control	Enable or GPIO	GPIO3_SEL	GPIO	Yes
	Input or output in GPIO mode	GPIO3_DIR	Output	Yes
	Output type open drain or push-pull	GPIO3_OD	Open drain	Yes
	Pin control of GPIO, EN1 or EN2	EN_PIN_CTRL_GPIO3, EN_PIN_SELECT_GPIO3	EN1	Yes
	Startup Delay	GPIO3_ STARTUP_ DELAY	4.16 ms	Yes
	Shutdown Delay	GPIO3_ SHUTDOWN_ DELAY	0 ms	Yes

Table 16 shows device settings for PGOOD.

Table 16. PGOOD OTP Settings

	Description	Bit Name	LP87524P-Q1	Configurable
Signals monitored by PGOOD	BUCKx output voltage / voltage and current (master bucks)	PGx_SEL	Voltage	Yes
PGOOD mode selections	PGOOD thresholds for BUCKx (Undervoltage / Window (undervoltage and overvoltage))	PGOOD_WINDOW	Window	Yes
	PGOOD valid debounce time	PGOOD_SET_DELAY	11 ms	Yes
	PGOOD signal mode (status / latched until fault source read)	EN_PGFLT_STAT	Status	Yes
	PGOOD output mode (push-pull or open drain)	PGOOD_OD	Open drain	Yes
	PGOOD polarity (active high / active low)	PGOOD_POL	Active high (power valid)	Yes

Table 17 lists the device settings for thermal warning. Also refer to Table 19 for interrupt settings.

Table 17. Protections OTP Settings

	Description	Bit Name	LP87524P-Q1	Configurable
Protections	Thermal warning level (125°C or 137°C)	TDIE_WARN_LEVEL	125°C	Yes
	Input over-voltage protection	N/A	Enabled	No

Table 18 shows device settings for I^2C and OTP revision ID values.

Table 18. Device Identification and I^2C Settings

	Description	Bit Name	LP87524P-Q1	Configurable
I^2C slave ID (7-bit)	Slave address	N/A	0x60	No

Table 19 lists device settings for interrupts. When interrupt from an event is unmasked, an interrupt is generated to nINT pin.

Table 19. Interrupt Mask Settings

	Interrupt event	Bit Name	LP87524P-Q1	Configurable
General	Sync clock appears or disappears	SYNC_CLK_MASK	Unmasked	Yes
	Thermal warning	TDIE_WARN_MASK	Unmasked	Yes
	Load measurement ready	I_LOAD_READY_MASK	Masked	Yes
	Register reset	RESET_REG_MASK	Masked	Yes
BUCK0	Buck0 PGOOD has reached threshold level	BUCK0_PG_MASK	Masked	Yes
	Buck0 current limit triggered	BUCK0_ILIM_MASK	Masked	Yes
BUCK1	Buck1 PGOOD has reached threshold level	BUCK1_PG_MASK	Masked	Yes
	Buck1 current limit triggered	BUCK1_ILIM_MASK	Masked	Yes
BUCK2	Buck2 PGOOD has reached threshold level	BUCK2_PG_MASK	Masked	Yes
	Buck2 current limit triggered	BUCK2_ILIM_MASK	Masked	Yes
BUCK3	Buck3 PGOOD has reached threshold level	BUCK3_PG_MASK	Masked	Yes
	Buck3 current limit triggered	BUCK3_ILIM_MASK	Masked	Yes

3.1.3.1 Startup and Shutdown Sequence

Figure 6 shows default startup and shutdown sequence programmed to OTP, in this case with EN1 signal. Refer to the datasheet for a full description of all registers and their settings.

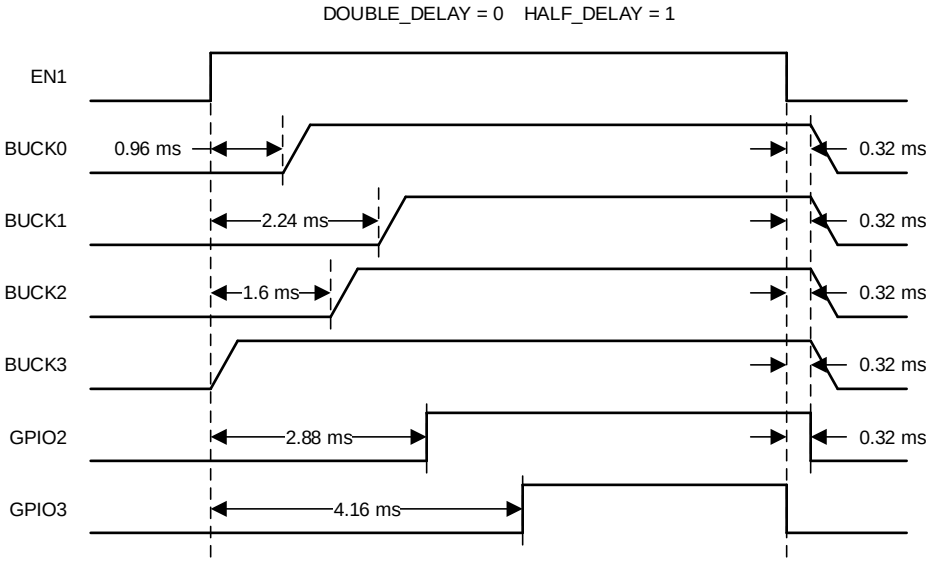

Figure 6. LP87524P-Q1 Startup and Shutdown Sequence Timing Diagram

4 References

See these references for additional information:

1. Texas Instruments, LP87524B/J/P-Q1 Four 4-MHz Buck Converters for AWR and IWR MMICs datasheet
2. Texas Instruments, XWR1xxx Power Management Optimizations – Low Cost LC Filter Solution application report

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