Errata

IWR6843, IWR6443 DeviceSilicon Errata Silicon Revisions 1.0 and 2.0

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1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (IWR6843 and IWR6443).

2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / mmWave sensor devices. Each of the Radar devices has one of the two prefixes: XIx or IWRx (for example: **XI6843**QGABL). These prefixes represent evolutionary stages of product development from engineering prototypes (XI) through fully qualified production devices (IWR).

Device development evolutionary flow:

XI — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

IWR — Production version of the silicon die that is fully qualified.

XI devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

3 Device Markings

Figure 3-1 shows an example of the IWR6843 Radar Device's package symbolization.

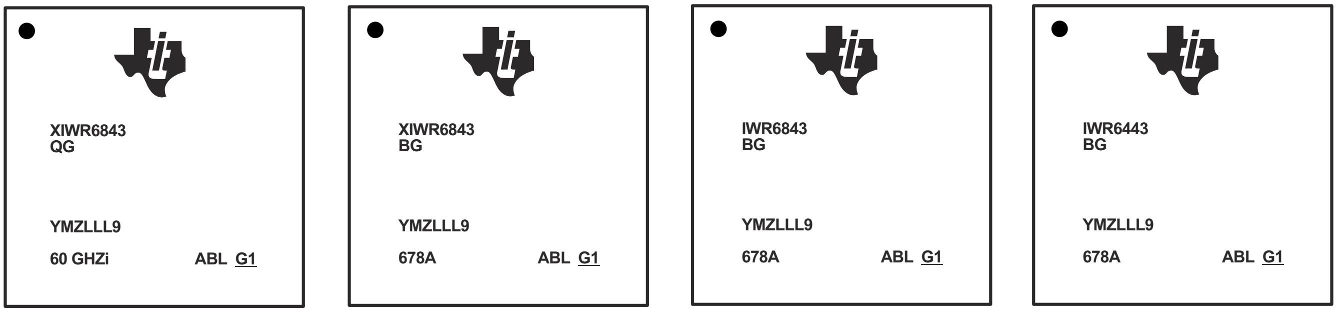

Figure 3-1. Example of Device Part Markings

This identifying number contains the following information:

- **Line 1:** Device Number
- **Line 2:** Safety Level and Security Grade
- **Line 3:** Lot Trace Code
  - YM = Year/Month Code
  - Z = Assembly Site Code
  - LLL = Assembly Lot Code
  - 9 = Primary Site Code
- **Line 4:**
  - 60 GHZi = IWR6843 (ES1.0) Identifier
  - 678A = IWR6843 (ES2.0) or IWR6443 (ES2.0) Identifier
  - ABL = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

4 Usage Notes

Usage notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These usage notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

4.1 MSS: SPI Speed in 3-Wire Mode Usage Note

The maximum SPI speed under 3-wire operation was only tested up to 33 MHz. This affects IWR6843 ES1.0 only.

5 Advisory to Silicon Variant / Revision Map

Table 5-1. Advisory to Silicon Variant / Revision Map

Advisory Number	Advisory Title	IWR6843 Only	IWR6843 / IWR6443
		ES1.0	ES2.0
	Master Subsystem		
MSS#03	Incorrect Handling of “Saturation” in FFT Hardware Accelerator’s Statistics Block	X	
MSS#10	Partial Write After a Full Data Width Write Fails to Mailbox Memory if ECC is Enabled	X	
MSS#11	Clock Monitoring Logic Core Clock Comparator (CCCB) for CPU Clock Cannot be Used	X	
MSS#12	MCAN Filter Event Interrupt not Connected to DMA	X	
MSS#13	Incorrect Read from FFT Hardware Accelerator After Complex Multiplication Operation	X	
MSS#14	Asynchronous Assertion of SoC Warm Reset may not Work Reliably When Device Operating on PLL Clock	X	
MSS#16	Delay Time, ETM Trace Clock to ETM Data Valid does not Meet Datasheet Specification	X	
MSS#17	Invalid Pre-fetch from MSS CR4 Processor (due to Speculative Read Operation from Tightly Coupled Memory Instance) Leads to Generation of MSS_ESM Group 3 Channel 7: MSS_TCMA_FATAL_ERR	X	
MSS#18 (1)	Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application	X	
MSS#19	DMA Read from Unimplemented Address Space may Result in DMA Hang Scenario	X	
MSS#20	Radar Frame Stuck due to Missing Synchronizer Logic in Hardware	X	
MSS#21	Issue with HWA Input Formatter 16 bit Real Signed Format	X	
MSS#22	CAN-FD: Message Transmitted With Wrong Arbitration and Control Fields	X	
MSS#23	HWA Read Registers Cannot be Read Reliably When the HWA is Executing a ParamSet Instruction	X	
MSS#24	Limitation With Peak Grouping Feature in Hardware Accelerator	X	
MSS#25	Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs	X	X
MSS#26	DMA Requests Lost During Suspend Mode	X	X
MSS#27	MibSPI in Slave Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1	X	X
MSS#28	A Data Length Error is Generated Repeatedly in Slave Mode When IO Loopback is Enabled	X	X
MSS#29	Spurious RX DMA REQ From a Slave Mode MibSPI	X	X
MSS#30	MibSPI RX RAM RXEMPTY Bit Does Not Get Cleared After Reading	X	X
MSS#31	CPU Abort Generated on a Write to Implemented CRC Space After a Write to Unimplemented CRC Space	X	X
MSS#32	DMMGLBCTRL BUSY Flag Not Set When DMM Starts Receiving A Packet	X	X
MSS#33	MibSPI RAM ECC is Not Read Correctly in DIAG Mode	X	X
MSS#34	HS Device Does Not Reboot Successfully on Warm Reset Getting Triggered by Watchdog Expiry	X	X
MSS#35	EDMA TPTC Generates an Incorrect Address on the Read Interface, Causing one or More Data Integrity Failures, Hangs, or Extra Reads	X	
MSS#36	DMA Read From an Unimplemented Address Space is not Reported as a BUS Error		X
MSS#37A	DCC Module Frequency Comparison can Report Erroneous Results	X	X
MSS#38	GPIO Glitch During Power-Up	X	X
MSS#39	The State of the MSS DMA is Left Pending and Uncleared on any DMA MPU Fault	X	X
MSS#40	EDMA transfer that spans ACCEL_MEM0 +ACCEL_MEM1 or ACCEL_MEM2 +ACCEL_MEM3 memories of HWA could result in data corruption	X	X
	Analog / Millimeter Wave		
ANA#11	Emissions and Interference Sensitivity During RF Calibrations	X	X

Table 5-1. Advisory to Silicon Variant / Revision Map (continued)

Advisory Number	Advisory Title	IWR6843 Only	IWR6843 / IWR6443
		ES1.0	ES2.0
ANA#12	Second Harmonic (HD2) Caused When High-Signal Level Present at Receiver Input	X	X
ANA#13A	Phase Mismatch Variation Across Temperature in TX3/TX1 and TX3/TX2 Combinations are Double That of TX2/TX1 Combination	X	X
ANA#14	Doppler Spurs Observed for Narrow Chirps	X	X
ANA#15	Excessive TX-RX Coupling or Reflection can Lead to Saturated RX Output	X	X
ANA#16	LVDS Coupling to Clock System	X	X
ANA#17	On-Board Supply Ringing Induced Spur	X	X
ANA#18	RX Digital Filtering Activity Coupling to XTAL Pins	X	X
ANA#19	Bandgap Decoupling Capacitor On-Board	X	X
ANA#20	Occasional Failures Observed During Calibration of the Radar Subsystem	X	X
ANA#21	Out of Band Radiated Spectral Emission	X	X
ANA#22	Overshoot and Undershoot During Inter-Chirp When Dynamic-Power Saving is Disabled	X	X
ANA#27A	Digital temperature sensor readings differ from analog temperature sensors.	X	X
DSP Subsystem (IWR6843 Only)			
DSS#01	Access to L3 Region Above Allocated Region may Result in Double Bit ECC Error if ECC is Enabled	X	
DSS#02	L1P Parity Error not Connected to ESM	X	
DSS#03	Different Number of Chirps in ADC Buffer's Ping and Pong Memory is not Supported	X	
DSS#04	Partial Write After Full Data Width Write Fails to HS RAM, ADC Buffer and Data Transfer Memory if ECC is Enabled for that Memory	X	
DSS#05	Byte Writes not Supported to L3 If ECC is Enabled	X	
DSS#07	Temperature Sensor Located Near DSP not Working	X	

(1) Applies to SIL Targeted devices.

6 Known Design Exceptions to Functional Specifications

MSS#03 — *Incorrect Handling of “Saturation” in FFT Hardware Accelerator’s Statistics Block*

Revision(s) Affected: IWR6843 ES1.0

Description: Statistics block always assumes that input is signed when checking for saturation, but the input can be unsigned in some cases.

Workaround(s): None.

MSS#10 — *Partial Write After a Full Data Width Write Fails to Mailbox Memory if ECC is Enabled*

Revision(s) Affected: IWR6843 ES1.0

Description: Partial data write after a full data width write would result is wrong data being written into the Mailbox memory if ECC is enabled.

Workaround(s): None. Silicon update will be provided by TI.

MSS#11 — *Clock Monitoring Logic Core Clock Comparator (CCCB) for CPU Clock Cannot be Used*

Revision(s) Affected: IWR6843 ES1.0

Description: Clock used for the Watchdog Timer (WDT) is same as the CPU clock. CCCB can be dedicated to monitor CPU clock against a reference clock like XTAL/RCOSC to generate a WDT reset if CPU clock fails. However, CCCB does not consistently generate an error if the CPU clock stops ticking

Workaround(s): None. Silicon update will be provided by TI.

MSS#12	***MCAN Filter Event Interrupt not Connected to DMA***
Revision(s) Affected:	IWR6843 ES1.0
Description:	MCAN filter event interrupt is only connected to MSS VIM and not connected to MSS DMA. If a DMA transfer operation is expected to happen on this interrupt , MSS CR4 will have to trigger the DMA
Workaround(s):	None. Silicon update will be provided by TI.

MSS#13	***Incorrect Read from FFT Hardware Accelerator After Complex Multiplication Operation***
Revision(s) Affected:	IWR6843 ES1.0
Description:	Read-back from FFT hardware accelerator slave, static configuration registers, Window RAM, Param RAM, and First stage RAM gives incorrect data if the last operation performed by the accelerator was a complex multiplication.
Workaround(s):	None.

MSS#14 *Asynchronous Assertion of SoC Warm Reset may not Work Reliably When Device Operating on PLL Clock*

Revision(s) Affected: IWR6843 ES1.0

Description: Asynchronous assertion of SoC warm reset through WARM_RESET pin, SW reset, watchdog reset, or Debug reset may not reliably work and may also result in a system hang scenario.

Workaround(s): MSS VCLK must be switched from PLL clock to REFCLK by following the prescribed software sequence before a warm reset is issued.

MSS#16 *Delay Time, ETM Trace Clock to ETM Data Valid does not Meet Datasheet Specification*

Revision(s) Affected: IWR6843 ES1.0

Description: Delay time, ETM trace clock to ETM data valid does not meet datasheet specification below:

PARAMETER	MIN	MAX	UNIT
Delay time, ETM trace clock high to ETM data valid	1	7	ns
Delay time, ETM trace clock low to ETM data valid	1	7	ns

In IWR6843 ES1.0, Delay time, ETM trace clock to ETM data timing that is being met is as given below:

PARAMETER	MIN	MAX	UNIT
Delay time, ETM trace clock high to ETM data valid	–0.5	7	ns
Delay time, ETM trace clock low to ETM data valid	–0.5	7	ns

Workaround(s): None.

MSS#17 ***Invalid Pre-fetch from MSS CR4 Processor (due to Speculative Read Operation from Tightly Coupled Memory Instance) Leads to Generation of MSS_ESM Group 3 Channel 7: MSS_TCMA_FATAL_ERR***

Revision(s) Affected: IWR6843 ES1.0

Description: The CR4 processor may perform an invalid pre-fetch access due to speculative TCM read leading to an invalid address access. This can result in a TCERROR and also a 2-bit ECC fatal error. The TCERROR is ignored by the processor since these correspond to instructions that are pre-fetched but never executed. However, the invalid MSS_TCMA_FATAL_ERR is generated on the ESM group3 channel-7.

Implication: In case of a genuine TCMA ECC fatal error, nERROR will not be generated directly through ESM.

Workaround(s): Mask Group 3 channel 7: MSS_TCMA_FATAL_ERR to ESM can be masked by writing into MSS_RCM:ESMGATE0 register. CR4F abort handler should handle the nERROR generation

OR

Disable branch prediction for MSS-CR4F

MSS#18 ***Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application***

Revision(s) Affected: IWR6843 ES1.0

Description: The CCM-R4F module compares the outputs of the two Cortex-R4F CPU cores and generates an error on any mis-compare. This ensures the lock-step operation of the two Cortex-R4F CPUs. The nERROR signal should only be set by the CCM-R4 module by a valid core mismatch. At power-on, some uninitialized circuits may cause the CCMR4-F to falsely detect a mis-compare.

Workaround(s): The anomalous nERROR toggle would need to be ignored by the external monitoring circuit (if deployed).

MSS#19 ***DMA Read from Unimplemented Address Space may Result in DMA Hang Scenario***

Revision(s) Affected: IWR6843 ES1.0

Description: The MSS DMA generates a BER (Bus Error) interrupt when the DMA detects a bus error due to a read from unimplemented address space. This interrupt is available on VIM Interrupt Channel-70 for DMA1 and VIM Interrupt Channel-51 for DMA2 .This read from unimplemented address space results in a hang condition in the DMA infrastructure bridge that connects it to the main interconnect.

Implication: A DMA read from an unimplemented address can result in a DMA hang condition. In the resulting state the DMA will not respond to any further DMA requests.

Workaround(s): The MSS CR4F processor will have to invoke a warm reset or generate an nERROR if it receives a DMA BER error.

MSS#20 ***Radar Frame Stuck due to Missing Synchronizer Logic in Hardware***

Revision(s) Affected: IWR6843 ES1.0

Description: Radar Sub System Internal Frame Clock is triggered by rlSensorStart API which starts the Radar Frame. Occasionally the rlSensorStart API does not trigger the clock due to missing synchronizer logic in hardware.

Implication: A DMA read from an unimplemented address can result in a DMA hang condition. In the resulting state the DMA will not respond to any further DMA requests.

Workaround(s): The issue is frequent if FRC clock source is changed. Ensure that FRC Clock source is not changed.

MSS#21 ***Issue with HWA Input Formatter 16 bit Real Signed Format***

Revision(s) Affected: IWR6843 ES1.0

Description: Wrong sign extension is implemented for 16 bit signed format in real only mode operation. Hence, signed 16-bit real format cannot be supported for input formatter.

Workaround(s): None. Silicon update will be provided by TI.

MSS#22	***CAN-FD: Message Transmitted With Wrong Arbitration and Control Fields***
Revision(s) Affected:	IWR6843 ES1.0 only

Description:

Under the following conditions a message with wrong ID, format, and DLC is transmitted:

- M_CAN is in state "Receiver" (PSR.ACT = "10"), no pending transmission
- A new transmission is requested before the 3rd bit of Intermission is reached
- The CAN bus is sampled dominant at the third bit of Intermission which is treated as SoF (see ISO11898-1:2015 Section 10.4.2.2)

Under the conditions listed above it may happen, that:

- The shift register is not loaded with ID, format, and DLC of the requested message
- The M_CAN will start arbitration with wrong ID, format, and DLC on the next bit
- In case the ID wins arbitration, a CAN message with valid CRC is transmitted
- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus, no error is detected by the transmitting M_CAN

The erratum is limited to the case when M_CAN is in state "Receiver" (PSR.ACT = "10") with no pending transmission and a new transmission is requested before the 3rd bit of Intermission is reached and this 3rd bit of intermission is seen dominant.

When a transmission is requested by the CPU, the Tx Message Handler performs an internal arbitration and loads the pending transmit message with the highest priority into its output buffer and then sets the transmission request for the CAN Protocol Controller. The problem occurs only when the transmission request for the CAN Protocol Controller is activated between the sample points of the 2nd and 3rd bit of Intermission and if that 3rd bit of intermission is seen dominant.

This dominant level at the 3rd bit of Intermission may result from an external disturbance or may be transmitted by another node with a significantly faster clock.

In the described case it may happen that the shift register is not loaded with arbitration and control field of the message to be transmitted. The frame is transmitted with wrong ID, format, and DLC but with the data field of the requested message. The message is transmitted in correct CAN (FD) frame format with a valid CRC.

If the message loses arbitration or is disturbed by an error, it is retransmitted with correct arbitration and control fields.

Workaround(s):

Request a new transmission only if another transmission is already pending or when the M_CAN is not in state "Receiver" (when PSR.ACT ≠ "10").

Another option would be to add a checksum to the data field covering arbitration and control fields of the message to be transmitted.

MSS#23 — *HWA Read Registers Cannot be Read Reliably When the HWA is Executing a ParamSet Instruction*

Revision(s) Affected: IWR6843 ES1.0 only

Description: Any read from the HWA configuration or status registers can be corrupted, if the read access is performed when the HWA is active. Reads from the HWA registers can be performed correctly, only after the execution of the entire ParamSet (i.e., after the ACC_DONE_INTR interrupt) or when the HWA is in IDLE mode waiting for the trigger to the start the execution of the next ParamSet instruction.

Workaround(s): Perform the following:

- Read-back of signature registers: Software needs to maintain a soft copy of the one-hot encoded signature registers and use that copy location for the EDMA programming.
- Read-back of static registers on the HWA ParamSet interrupt. There is no reliable way to read the HWA static registers, if the HWA is active.
- Read-back of Debug/status registers: The User can only read these registers when the HWA is ***not*** active.

MSS#24	***Limitation With Peak Grouping Feature in Hardware Accelerator***
Revision(s) Affected:	IWR6843 ES1.0 only
Description:	Peak is declared only if the cell under test is greater than its most immediate neighboring cells to its left and right. In the case where CFAR qualified peaks in the two adjacent cells happen to be equal in magnitude, enabling peak grouping can lead to the peak being lost.
Workaround(s):	Do not enable the peak grouping feature in the hardware accelerator.

MSS#25	***Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs***
Revision(s) Affected:	IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0
Description:	If a system reset (nRST goes low) occurs while the debugger is performing an access on the system resource using system view, a slave error should be replied to the debugger. If the access was a read, instead the response might indicate that the access completed successfully and return unpredictable data. This issue occurs under this condition: when a system reset is asserted (nRST low) on a specific cycle, while the debugger is completing an access on the system, using the system view. An example would be, when a debugger, like the CCS-IDE memory browser window, is refreshing content using the system view. This is not an issue for a CPU only reset and, this is not an issue during a power-on-reset (nPORRST) either.
Workaround(s):	Avoid performing debug reads and writes while the device might be in reset.

MSS#26 *DMA Requests Lost During Suspend Mode*

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: While the device is halted in suspend mode by the debugger, the DMA is expected to complete the remaining transfers of a block, if the DEBUG MODE bit field of the GCTRL register is configured to '01'. Instead, the DMA does not complete the remaining transfers of a block but, rather stops after two more frames of data are transferred. Subsequent DMA requests from a peripheral to trigger the remaining frames of a block can be lost.

This issue occurs only in the following conditions:

- The device is suspended by a debugger
- A peripheral continues to generate requests while the device is suspended
- The DMA is setup to continue the current block transfer during suspend mode with the DEBUG MODE bit field of the GCTRL register set to '01'
- The request transfer type TTYPE bit in the CHCTRL registers is set to frame trigger ('0')

Workaround(s): **Workaround #1:**

Use TTYPE = block transfer ('1'), when the DEBUG MODE bit field is '01' (*finish current block transfer*)

or

Workaround #2:

Use the DMA DEBUG MODE = '00' (ignore suspend), when using TTYPE = frame transfer ('0') to complete the block transfer, even after suspend/halt is asserted.

MSS#27 ***MibSPI in Slave Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1***

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: The MibSPI module, when configured in multibuffered slave mode with 3-functional pins (CLK, SIMO, SOMI) or 4-functional pins (CLK, SIMO, SOMI, nENA), could transmit incorrect data when all the following conditions are met:

- MibSPI module is configured in multibuffered mode,
- Module is configured to be a slave in the SPI communication,
- SPI communication is configured to be in 3-pin mode or 4-pin mode with nENA,
- Clock phase for SPICLK is 1, and
- SPICLK frequency is MSS_VCLK frequency / 12 or slower

Workaround(s): The issue can be avoided by setting the CSHOLD bit in the control field of the TX RAM (Multi-Buffer RAM Transmit Data Register). The nCS is not used as a functional signal in this communication; hence, setting the CSHOLD bit does not cause any other effect on the SPI communication.

MSS#28 ***A Data Length Error is Generated Repeatedly in Slave Mode When IO Loopback is Enabled***

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: When a DLEN error is created in Slave mode of the SPI using nSCS pins in IO Loopback Test mode, the SPI module re-transmits the data with the DLEN error instead of aborting the ongoing transfer and stopping. This is only an issue for an IOLPBK mode Slave in Analog Loopback configuration, when the intentional error generation feature is triggered using CTRLDLENERR (IOLPBKTSTCR.16).

Workaround(s): After the DLEN_ERR interrupt is detected in IOLPBK mode, disable the transfers by clearing the SPIEN (bit 24) in the SPIGCR1 register and then, re-enable the transfers by resetting the SPIEN bit.

MSS#29 *Spurious RX DMA REQ From a Slave Mode MibSPI*

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: A spurious DMA request could be generated even when the SPI slave is not transferring data in the following condition sequence:

- The MIBSPI is configured in standard (non-multibuffered) SPI mode, as a slave
- The DMAREQEN bit (SPIINT0.16) is set to enable DMA requests
- The Chip Select (nSCS) pin is in an active state, but no transfers are active
- The SPI is disabled by clearing the SPIEN (SPIGCR1.24) bit from '1' to '0'

The above sequence triggers a false request pulse on the Receive DMA Request as soon as the SPIEN bit is cleared from '1' to '0'.

Workaround(s): Whenever disabling the SPI, by clearing the SPIEN bit (SPIGCR1.24), first clear the DMAREQEN bit (SPIINT0.16) to '0', and then, clear the SPIEN bit.

MSS#30 ***MibSPI RX RAM RXEMPTY bit Does Not Get Cleared After Reading***

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: The RXEMPTY flag may not be auto-cleared after a CPU or DMA read when the following conditions are met:

- The TXFULL flag of the latest buffer that the sequencer read out of transmit RAM for the currently active transfer group is 0,
- A higher-priority transfer group interrupts the current transfer group and the sequencer starts to read the first buffer of the new transfer group from the transmit RAM, and
- Simultaneously, the Host (CPU/DMA) is reading out a receive RAM location that contains valid received data from the previous transfers.

Workaround(s): If at all possible, avoid transfer groups interrupting one another.

If dummy buffers are used in lower-priority transfer groups, select the appropriate "BUFMODE" for them (like, SKIP/DISABLED) unless, there is a specific need to use the "SUSPEND" mode.

MSS#31 ***CPU Abort Generated on a Write to Implemented CRC Space After a Write to Unimplemented CRC Space***

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: An abort could be generated on a write to a legal address in the address offset region (0x0000–0x01FF) of the CRC register space when a normal mode write to an unimplemented address region (0x0200–0xFFFF) of the CRC register space is followed by a write to a legal address region (0x0000–0x01FF) of the CRC register space.

Workaround(s): None.

MSS#32 — *DMMGLBCTRL BUSY Flag Not Set When DMM Starts Receiving A Packet*

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: The BUSY flag in the DMMGLBCTRL register should be set when the DMM starts receiving a packet or has data in its internal buffers. However, the BUSY flag (DMMGLBCTRL.24) may not get set when the DMM starts receiving a packet under the following condition:

- The BUSY bit is set only after the packet has been received, de-serialized, and written to the internal buffers. It stays active while data is still in the DMM internal buffers. If the internal buffers are empty (meaning that no data needs to be written to the destination memory) then, the BUSY bit will be cleared.

Workaround(s): Wait for a number of DMMCLK cycles (for example, 95 DMMCLK cycles) beyond the longest reception and deserialization time needed for a given packet size and DMM port configuration, before checking the status of the BUSY flag, and after the DMM ON/OFF bit field (DMMGLBCTRL.[3:0]) has been programmed to OFF.

MSS#33 ***MibSPI RAM ECC is Not Read Correctly in DIAG Mode***

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: A Read operation to the ECC address space of the MibSPI RAM in DIAG mode, does not return the correct ECC value for the first 128 buffers, if the Extended Buffer support is implemented but, the Extended Mode is disabled for the particular MibSPI instance.

Workaround(s): None.

MSS#34	***HS Device Does Not Reboot Successfully on Warm Reset Getting Triggered or With Internal Software Reset***
Revision(s) Affected:	IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0
Description:	A warm reset triggered by a watchdog expiry (MSS Wdog) , a software register write (SOFTSYSRST), or an external warm reset pin does not ensure a successful reboot of the device in a secure device (HS device).
Workaround(s):	A warm reset should not be triggered externally or internally by a watchdog expiry, a software write, or other trigger mechanisms. To initiate a reset cycle, external circuitry should be used on the sensor design. The external circuitry uses the watchdog, nERROR OUT monitoring, or other kinds of GPIO signaling to trigger a reset using the nRST pin of the device.

MSS#35 EDMA TPTC Generates an Incorrect Address on the Read Interface, Causing one or More Data Integrity Failures, Hangs, or Extra Reads

Revision(s) Affected: IWR6843 ES1.0 only

Description: Certain scenarios could lead to an incorrect read, hang, or data integrity issues in the EDMA TPTC block. Table 6-1 shows the various scenarios and the resulting effects of each scenario.

A scenario happens, if *ALL* conditions listed for that scenario are satisfied (true); that is, "AND" of all conditions.

A “hang” outcome means that one or more attempts of the hang causing scenarios can progressively lead to not receiving a "transfer completion" indication from the TPTC. The last transfer attempt which does not receive the completion indication can be any transfer – any scenario transfer within this advisory or even outside of this advisory.

Table 6-1. EDMA TPTC Scenario IDs and Condition Results

SCENARIO ID	CONDITIONS	DATA INTEGRITY FAILURES	HANGS	EXTRA READS
1	AB-sync BCNT > 1 ACNT not in [2,4,8,16,32] (ACNT < 64) OR ((ACNT = 64) AND (SRCBIDX != ACNT)) Source Addressing crossing 4-KB boundary for any of the BCNT number of ACNT transfers. condition [1]	Yes (see Figure 6-4)	Possible	Possible
2	AB-sync with BCNT=1 or A-sync ACNT not in [2..24, 32] ACNT <= 64 Source Addressing crossing 4-KB boundary for any of the BCNT number of ACNT transfers. condition [1]	No	Possible	Yes
3	AB-sync with BCNT=1 or A-sync ACNT in [2..24, 32] Source Addressing crossing 4-KB boundary for any of the BCNT number of ACNT transfers. condition [1]	No	No	Yes (see Figure 6-1)
4	AB-sync BCNT > 1 ACNT in [2,4,8,16,32] SRCBIDX = ACNT ACNT * BCNT <=64 Source Addressing crossing 4-KB boundary for any of the BCNT number of ACNT transfers. condition [1]	No	No	Yes (see Figure 6-2)
5	AB-sync BCNT > 1 ACNT in [2,4,8,16,32] SRCBIDX = ACNT ACNT * BCNT <=64 Source Addressing *does NOT* cross 4-KB boundary for any of the BCNT number of ACNT transfers; that is, NOT of condition [1] Source Addressing crosses 4-KB boundary for merged source array of size ACNT * BCNT. condition [2]	No	No	Yes (see Figure 6-3)

Source Addressing crossing 4-KB boundary cross **condition [1]** in Table 6-1 is defined as follows:
[X(i) = LSB_12bits(SRC_ADDR + i * SRC_BIDX)] + ACNT > 0x1000
where 0 <= i < BCNT

Source Addressing crossing 4-KB boundary cross **condition [2]** in Table 6-1 is defined as follows:
LSB_12bits(SRC_ADDR) + (ACNT * BCNT) > 0x1000

For the condition [1] and condition [2] expressions above, note that the SRC_ADDR is candidate source address considering the C-dimension. If CCNT > 1, then, the SRC_ADDR would be every candidate source address for all CCNTs depending on the type of transfer and the SRCCIDX.

For each extra read in SCENARIO ID #3 for which condition [1] is applicable, each index i above that satisfies the condition results in extra read from starting address SRC_ADDR + (i + 1) * SRCBIDX and of length equal to the distance from the start address to the boundary [that is, 0x1000 – X(i)]. Note: length < ACNT.

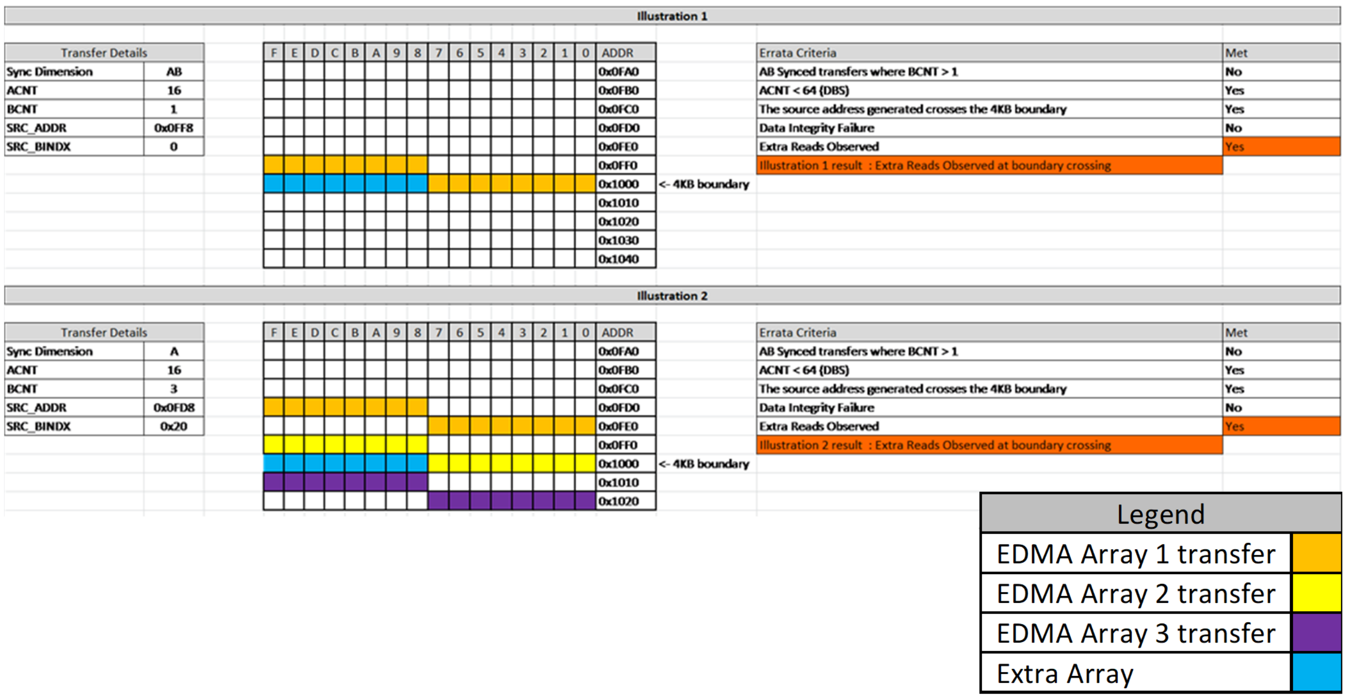

Figure 6-1. Scenario ID #3 – Extra Reads

For each extra read in SCENARIO ID #4 for which condition [1] is applicable, there is an extra read from starting address SRC + BCNT * ACNT (=SRCBIDX) of length equal to the distance of the start address to the boundary [that is, length is 0x1000 – X(i)], where i is the index of one and only 4-KB boundary crossing condition. Note: length < ACNT.

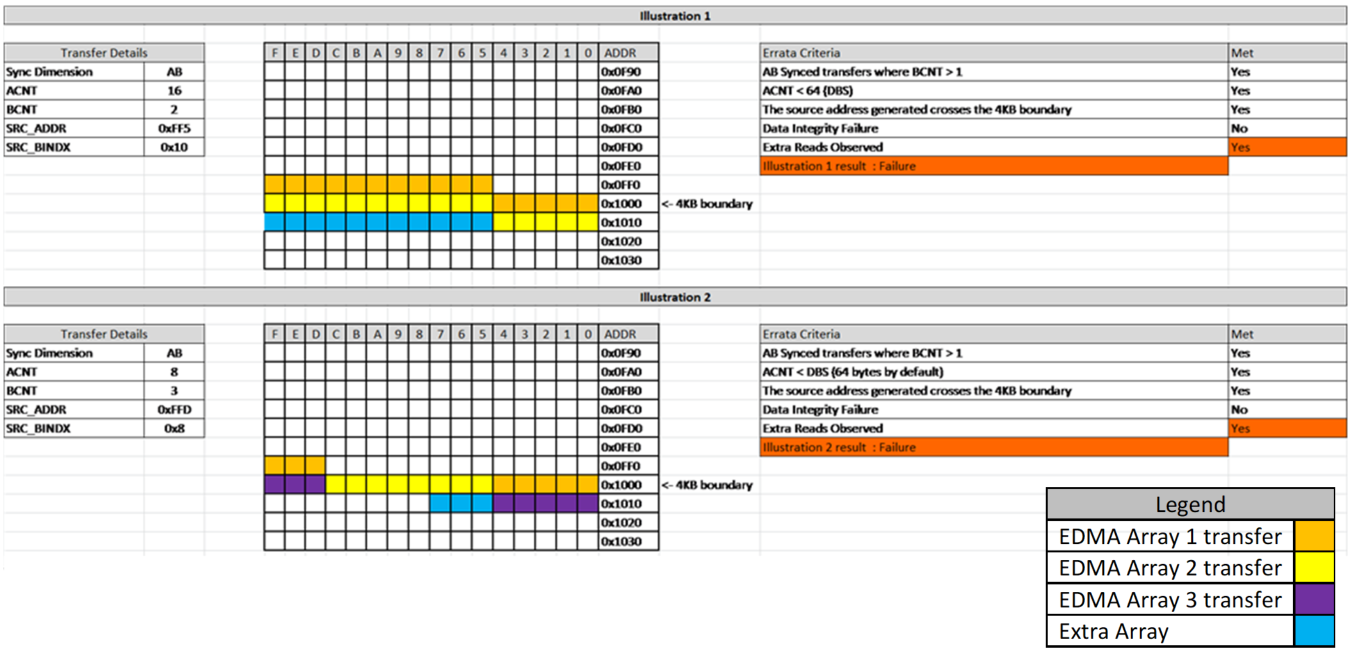

Figure 6-2. Scenario ID #4 – Extra Reads

For the extra read in SCENARIO ID #5 for which condition [2] is applicable, there is an extra read from starting address SRC + BCNT * ACNT (=SRCBIDX) of length equal to the distance of the start address and is of length ACNT.

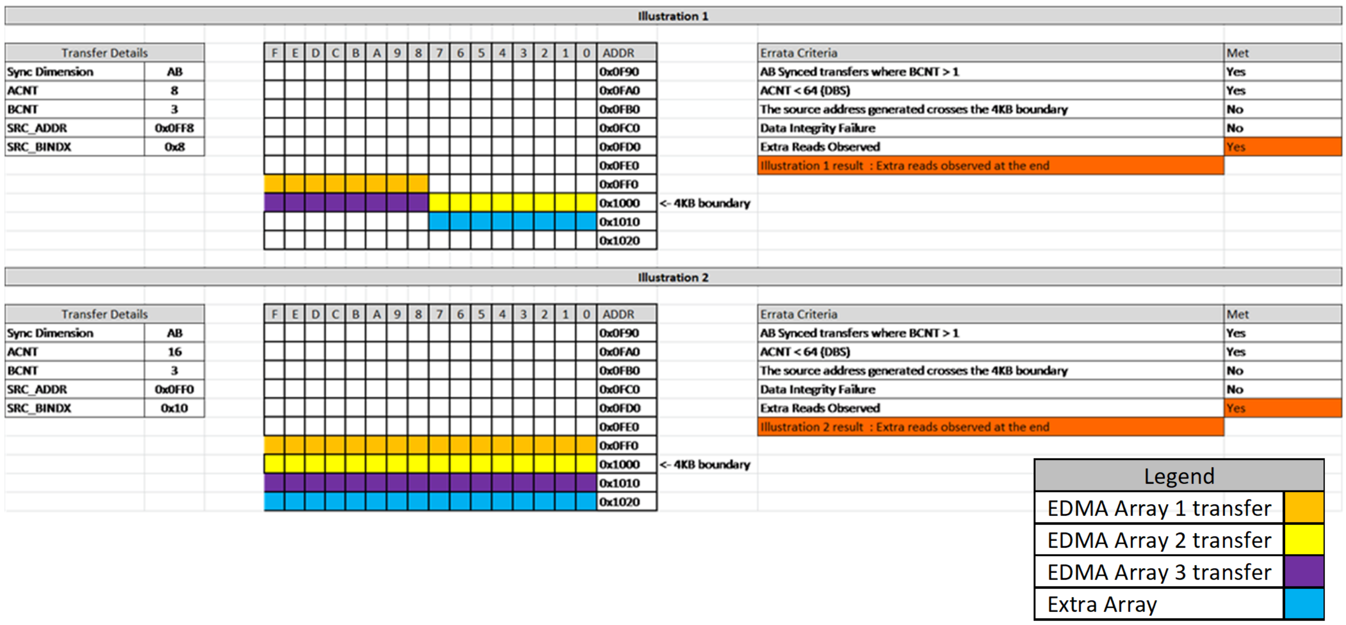

Figure 6-3. Scenario ID #5 – Extra Reads

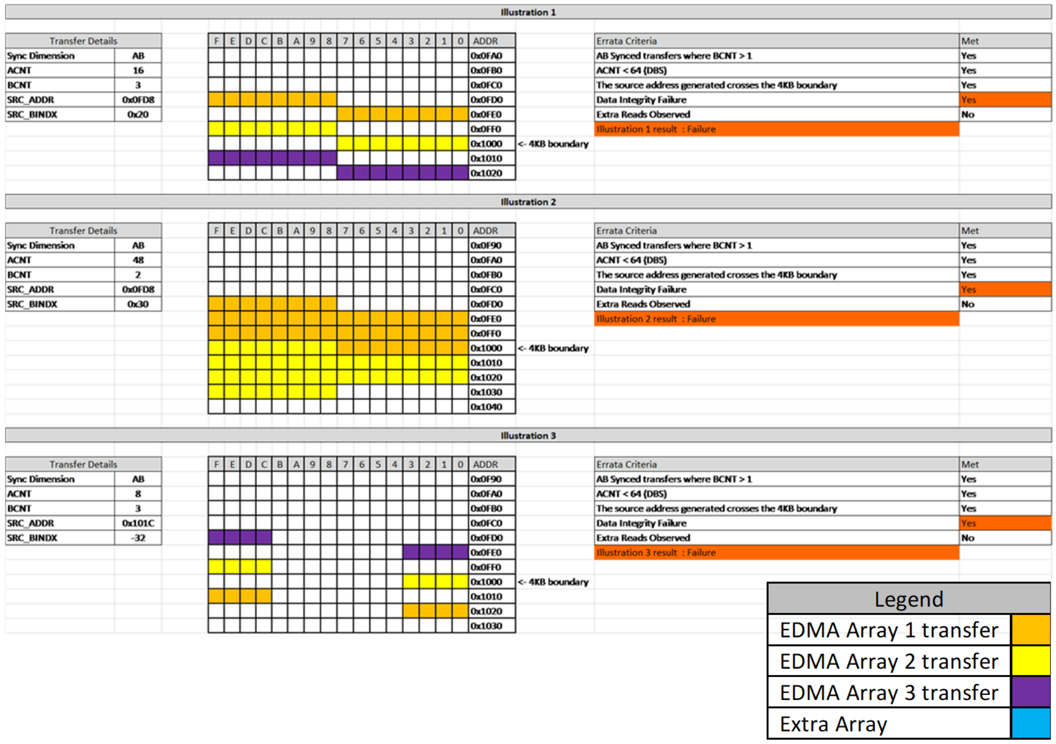

Figure 6-4. Scenario ID #1 – Data Integrity Failure

Workaround(s):

Workaround #1 - ALL SCENARIO IDs (see Table 6-1)

Prevent one or more of the conditions necessary for the problematic scenarios to happen.

Workaround #2 - SCENARIO ID #3, SCENARIO ID #4, and SCENARIO ID #5 – EXTRA READS

For SCENARIO ID #3, SCENARIO ID #4, and SCENARIO ID #5 – EXTRA READS, another workaround besides avoiding the 4-KB boundary cross conditions, is to ensure that buffers involved in this kind of transfer are positioned so that extra reads stay within the physical memory boundaries. If the extra reads go to Reserved space *or* space blocked by the Memory Protection Unit (MPU), the TPTC generates a bus error interrupt to the processor.

MSS#36 ***DMA Read From an Unimplemented Address Space is not Reported as a BUS Error***

Revision(s) Affected: IWR6843 ES2.0 only; IWR6443 ES2.0

Description: The MSS DMA should generate a Bus Error (BER) interrupt when the DMA detects an error due to a read from an unimplemented address location. This interrupt is not available on any of the VIM Interrupt Channels for DMA1 and DMA2.

Implication: A DMA read from an unimplemented address can go undetected.

Workaround(s): The DMA MPU has to be engaged with valid address range to ensure no occurrence of any read from an invalid address location happens.

DMA transfers have to be covered with end-to-end CRC from source to destination.

MSS#37A	***DCC Module Frequency Comparison can Report Erroneous Results***
Revision(s) Affected:	IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0
Description:	The Dual-clock Comparator module, which is used to monitor a clock frequency while comparing with a known clock reference, could stop earlier than expected, and, thus, indicating the measured clock frequency to be lower. This is due to a clock domain crossing issue causing a preset to the error detection logic to get triggered.
Workaround(s):	Applicable for devices with monitoring support. Multiple measurements can be taken for the same clock pairs, and for the average, or majority of the frequencies reported. Application code, where possible, could compare the clocks using an alternate clock comparator module (CCC).

MSS#38 ***GPIO Glitch During Power-Up***

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: During the 3.3-V supply ramp, the GPIO outputs could possibly see a short glitch (*rising above the 0 V for a short duration*). This GPIO glitch cannot be avoided by just a pulldown resistor. If the GPIO glitch during boot-up is high enough, it could be falsely detected as a “high”.

Workaround(s): Any GPIO used for such critical controls where glitch cannot be tolerated, should be gated by the nRESET signal of the xWR device.

Using a tri-state buffer (for example: SN74LVC1G126-Q1) externally to isolate the GPIO output from the system until the nRESET of xWR device is released. At this point, all the supplies are expected to be stable.

MSS#39 ***The State of the MSS DMA is Left Pending and Uncleared on any DMA MPU Fault***

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: The state of the MSS DMA is left pending and uncleared on any DMA MPU fault. The transfer that caused this MPU fault is left pending inside the DMA IP.

Any trigger on DMA REQ lines (could be caused by any module/IP that is hooked up to DMA in h/w) can re-trigger DMA to start executing the above pending transfer irrespective of whether that trigger is actually valid/enabled in DMA or that module/IP.

Workaround For devices where the Boot ROM is executing the MSS DMA MPU Self tests. As part of application initialization, if the MSS DMA will be used, the following register field should be used to reset the MSS DMA IP so that the uncleared transfer is reset:

1. Write MSS_RCM:SOFTRST1[31:24] 0xAD
2. Write MSS_RCM:SOFTRST1[31:24] 0x0

It is not recommended to use this configuration at any another instance other than that recommended here in this Errata.

On an actual Real time MPU Error, this error should be treated as a non-recoverable error and a warm reset should be issued to recover.

MSS#40	***Any EDMA Transfer That Spans ACCEL_MEM1 +ACCEL_MEM2 Memories of Hardware Accelerator May Result In Data Corruption Without Any Notification Of Error From The SoC***
Revision(s) Affected:	IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0
Description:	As per TPTC IP Spec, a Transfer request (TR) is supposed to access a single slave end point. ACCEL_MEM0/ACCEL_MEM1 memory banks of HWA are available via single slave point and ACCEL_MEM2/ ACCEL_MEM3 memory banks of HWA are available as another slave point (different from that of ACCEL_MEM0/ ACCEL_MEM1). Hence if a single TR is used to access a buffer spanning ACCEL_MEM1 and ACCEL_MEM2 memories of the HWA (i.e. a single buffer spanning 2 different slave points), the spec is not being adhered to. This errata is explicitly highlighting this spec requirement
Workaround(s):	Split the access into 2 TRs so that a single TR does not span ACCEL_MEM1 +ACCEL_MEM2. The 2 TRs can be chained.

ANA#11 ***Emissions and Interference Sensitivity During RF Calibrations***

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: External interference present on the RX or TX pins with level >-10 dBm can lead to degraded accuracy or errors in RF calibrations. This applies to boot-time PD, TX power, RX IQMM and gain calibrations, as well as run-time TX output power calibrations.

Also, a few boot cals will violate -10dBm peak power FCC spec applicable in the non-ISM band. This includes Tx power boot cal, Phase shifter boot cal and Rx IQMM boot cal.

Workaround(s): At customer factory, perform the RF INIT calibration in interference-free environment, and use the device's calibration save APIs to save the calibration results. These results can be restored later in the field. Use this sequence in the field: Skip the above RF calibrations using the “RF init calibration conf” API, restore the calibration file that was saved in factory, and then, issue the RF INIT API.

The workaround for runtime Tx output calibration is to use the “OLPC only” option in “Run time calibration conf and trigger” API. However, this can cause degradation in the Tx power accuracy.

ANA#12 ***Second Harmonic (HD2) is Present When Receiver is Tested Standalone Using CW Input***

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: There is a finite isolation between the RF pins/package and the FMCW synthesizer. This can create spurious tones at the synthesizer output and lead to appearance of 2nd order harmonics and inter-modulations of expected IF frequencies at RX ADC output. The amplitude of the 2nd harmonic could be as high as -55 dBc, referenced to the power level of the intended tone at the LNA input.

Workaround(s): No workaround available at this time. However, in many typical radar use-cases the HD2 does not affect the system performance due to two reasons:

1. Since the HD2 comes from a coupling to the LO signal, there is an inherent suppression of the HD2 level due to the self-mixing effect (that is, phase noise and phase spur suppression effect at the mixer).
2. In real-life scenarios there is often a double-bounce effect of the radar signal reflected from the target, which leads to a ghost object at twice the distance of the actual object. This effect is often indistinguishable from the effect of HD2 itself.

ANA#13A	***Phase Mismatch Variation Across Temperature in TX3/TX1 and TX3/TX2 Combinations are Double That of TX2/TX1 Combination***
Revision(s) Affected:	IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0
Description:	TX3/TX1 combination exhibits a phase mismatch variation across the complete recommended operating temperature range per the data manual whereas, TX2/TX1 and TX3/TX2 combinations exhibit a lower degree of variation over the same temperature range.
Workaround(s):	In applications requiring high phase accuracy across TX channels, a background angle calibration can be used to control phase variation over temperature

ANA#14	***Doppler Spurs Observed for Narrow Chirps***
Revision(s) Affected:	IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0
Description:	There is a non-linearity of the synthesizer when crossing certain frequencies: 60.3-, 60.75-, 61.2-, 61.56-, 62.1-, 62.64-, 63-, and 63.45-GHz. Implication: There will be a spur in the non-zero Doppler bin when the synthesizer crosses any of these frequencies during a chirp. The exact Doppler bin depends on the slope and ramp timings. The spur will be spread across multiple range bins.
Workaround(s):	Avoid narrow bandwidth ramps around frequencies with high-spur levels.

ANA#15 — *Excessive TX-RX Coupling or Reflection can Lead to Saturated RX Output*

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: If there is excessing TX-RX coupling or chassis reflection, it can lead to a saturated RX output. This situation can occur if the RX input is stronger than -10dBm.

Workaround(s): Improve TX-to-RX antenna isolation on PCB. Radome/chassis should give low reflection amplitude and should be as close as possible to the sensor, to reduce the IF frequency.

ANA#16	***LVDS Coupling to Clock System***
Revision(s) Affected:	IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0
Description:	The digital activity in the High-Speed Serial Interfaces (HSI) state machine can couple to the clock system/FMCW synthesizer and can cause spurs in its clock output. The spur frequency is HSI rate dependent (for example, for a 600-MHz HSI clock rate, 6.25-MHz and 12.5-MHz spurs can be observed on TX/RX output, and for a 900-MHz HSI clock rate, 7-MHz and 14-MHz spurs can be observed on the TX/RX output). The spur levels are low (*near or below -65 dBc*).
Workaround(s):	The spur will not be present, when the LVDS is not used.

ANA#17 ***On-Board Supply Ringing Induced Spur***

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: Turning OFF and ON front-end modules can cause on-board supply ringing and slow the settling of the power supply. This supply ringing can manifest as a spur in the FMCW synthesizer output spectrum.

Workaround(s): **Workaround #1:**

Disable inter-chirp duty cycling of the RX.

or

Workaround #2:

Design the power supply to damp out the ringing on the rails to the device.

ANA#18	***RX Digital Filtering Activity Coupling to XTAL Pins***
Revision(s) Affected:	IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0
Description:	The Digital filtering activity can potentially couple to XTAL pins and lead to spurs in the RX ADC output. The spur frequencies depend on the sampling rate (Fs) and DFE modes. Specifically, these spurs have been observed when Fs is close to 10- and 20-Msps within ±1.5 MHz. In these cases, an IF spur can appear at about 2Fs-40 MHz, 4Fs-40 MHz. The spur amplitudes vary with the frequency of the spur and are in the -35dBc range (for spur IF frequency of 200 kHz) to -75dBc range (for a spur IF frequency of 1.5 MHz) at the FMCW synthesizer output spectrum.
Workaround(s):	Avoid sampling rates of 10 ±1.5 Msps and 20 ±1.5 Msps. Exact 10-Msps and 20-Msps sampling rates are allowed, as they will not cause a spur.

ANA#19	***Bandgap Decoupling Capacitor On-Board***
Revision(s) Affected:	IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0
Description:	A 47-nF capacitor is needed on the bandgap pin. Not having correct capacitor on this pin, can cause boot up issues, especially, at negative temperatures. This requirement is being Included in the errata, as it is a recent change which may not be updated in older reference designs.
Workaround(s):	Use the recommended 47-nF capacitor. For example: part - GRM155R71E473KA88 (see the device-specific EVM and Reference Design files for updated part).

ANA#20	***Occasional Failures Observed During Calibration of the Radar Subsystem***
Revision(s) Affected:	IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0
Description:	Rare occurrences of failures have been observed in the Dual-Clock Comparator (DCC) module, as a result the APLL or Synthesizer may report a failure.
Workaround(s):	**Workaround #1:** Any APLL calibration failure needs to be responded with a reset cycle. ***or*** **Workaround #2:** Any SYNTH calibration failure reported by the BSS will require an RFinit.

ANA#21	***Out of Band Radiated Spectral Emission***
Revision(s) Affected:	IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0
Description:	Out-of-band radiated spectral emissions are observed at 14.4-GHz and 28.8-GHz.
Workaround(s):	To help in reducing the spur, shield around the device (*excluding Antenna region*). Microwave absorbers are available and can be attached to the top of the device.

ANA#22 ***Overshoot and Undershoot During Inter-Chirp When Dynamic-Power Saving is Disabled***

Revision(s) Affected: IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: This issue applies when Dynamic-Power Saving is disabled for Transmitters.

Overshoot and Undershoot conditions cause narrower RF sweeping bandwidth. For a 500-MHz chirp bandwidth, there is MAX Overshoot of ~100 MHz, and a MAX Undershoot of ~100 MHz.

This would lead to a significant reduction in effective chirp bandwidth for bandwidth-limited cases (for example, ISM band).

For example:

For an FMCW RF positive Ramp Chirp example, programmed for Fstart MHz to be (Fstart + 500) MHz, the effective observed transmission may span from (Fstart - 160) MHz to (Fstart + 500) MHz. Which would be an undershoot of 160 MHz. In order to compensate for such an undershoot, the programmed Chirps would have to be (Fstart + 160) MHz to (Fstart + 500) MHz.

The net result is, the programmed Chirp would have to be for a reduced Bandwidth (that is, 340 MHz).

Workaround(s): **Workaround #1:**

A firmware resolution of 400 MHz is implemented in the accompanied SDK release (SDK version 3.4 or later). This allows the user to program up to 400 MHz of the available 500-MHz ISM band of 61 GHz to 61.5 GHz applications.

or

Workaround #2:

To ensure the TX power amplifier is OFF during chirp idle time and not causing "on-air" emissions during the undershoot/overshoot period, keep the inter-chirp power savings ON.

ANA#27A ***Digital Temperature Sensor Readings Differ From Analog Temperature Sensors***

Revisions Affected IWR6843 ES1.0 and IWR6843 ES2.0; IWR6443 ES2.0

Description: The local heating in the digital circuitry can cause the readings from digital temperature sensor to differ from that of the analog temperature sensors (Tx, Rx, and PM).

Implication: The temperature monitor API computes the maximum temperature difference across different sensors and compares against the programmed threshold (TEMP_DIFF_THRESH). Higher difference between analog and digital temperature sensors can cause the monitor to fail.

Workaround(s): In temperature monitor configuration API (AWR_MONITOR_TEMPERATURE_CONF_SB), if the thresholds for the digital temperature sensors (DIG_TEMP_THRESH_MIN and DIG_TEMP_THRESH_MAX) are both set to zero, the BSS will ignore the digital sensor while computing the temperature difference across sensors to compare against the programmed threshold value (TEMP_DIFF_THRESH).

The digital temperature values (verbose output) from the API need to be validated externally by the processor.

DSS#01 *Access to L3 Region Above Allocated Region may Result in Double Bit ECC Error if ECC is Enabled*

Revision(s) Affected: IWR6843 ES1.0

Description: Access to L3 region above allocated region may result in a Double Bit ECC error in addition to the data abort if ECC is enabled.

Workaround(s): None. Silicon update will be provided by TI.

DSS#02 *L1P Parity Error not Connected to ESM*

Revision(s) Affected: IWR6843 ES1.0

Description: L1P parity error is only connected to DSP and not connected to MSS ESM.

Workaround(s): None. Silicon update will be provided by TI.

DSS#03 *Different Number of Chirps in ADC Buffer's Ping and Pong Memory is not Supported*

Revision(s) Affected: IWR6843 ES1.0

Description: Different number of chirps in ADC buffer's ping and pong memory is not supported. They need to be programmed to a same value and the configuration for number of chirps in Ping and Pong can only be changed at Sub-Frame boundary.

Workaround(s): None. Silicon update will be provided by TI.

DSS#04 *Partial Write After Full Data Width Write Fails to HS RAM, ADC Buffer and Data Transfer Memory if ECC is Enabled for that Memory*

Revision(s) Affected: IWR6843 ES1.0 only

Description: Partial data write after a full data width write would result is wrong data being written into HS RAM , ADC buffer and Data Transfer memory if ECC is enabled for that memory.

Workaround(s): None. Silicon update will be provided by TI.

DSS#05 — *Byte Writes not Supported to L3 If ECC is Enabled*

Revision(s) Affected: IWR6843 ES1.0

Description: Byte writes are not supported to L3 memory when ECC is enabled. ECC invalidation does not work correctly in this scenario.

Workaround(s): None. Silicon update will be provided by TI.

DSS#07 — *Temperature Sensor Located Near DSP not Working*

Revision(s) Affected: IWR6843 ES1.0

Description: The temperature sensor that is located near the DSP is not working in IWR6843 ES1.0. This is a known bug that will be fixed in ES2.0. There are eight temperature sensors located throughout the analog, all of which are working and accessible via an API call.

Workaround(s): None. Silicon update will be provided by TI.

7 Trademarks

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Revision History

Changes from June 1, 2020 to September 30, 2020 (from Revision B (June 2020) to Revision C (September 2020)) Page

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