2022 Digital IC Design Homework 2

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Functional Simulation Result

Stage 1	Pass	Stage 2	Pass	Stage 3	Pass

Stage 1

```
# --stage1 simulation--
#
# Setting1: PASS
#
# Setting2: PASS
#
# Setting3: PASS
#
# Setting4: PASS
#
# Setting5: PASS
#
# Setting6: PASS
#
# Setting7: PASS
#
# Setting8: PASS
#
# Setting9: PASS
#
# Setting10: PASS
#
```

Stage 2

```
# --stage2 simulation--
#
# Setting11: PASS
#
# Setting12: PASS
#
# Setting13: PASS
#
# Setting14: PASS
#
# Setting15: PASS
#
# Setting16: PASS
#
# Setting17: PASS
#
# Setting18: PASS
#
# Setting19: PASS
#
# Setting20: PASS
```

Stage 3

```
# --stage3 simulation--
#
# Setting21: PASS
#
# Setting22: PASS
#
# Setting23: PASS
#
# Setting24: PASS
#
# Setting25: PASS
#
# Setting26: PASS
#
# Setting27: PASS
#
# Setting28: PASS
#
# Setting29: PASS
#
# Setting30: PASS
```

Description of your design

主要分為: controller 模組和 data path 模組，

其中 data path 模組又分為 counter 模組、compare 模組。

- Controller : 以兩個 combinational circuit 和一個 Sequential circuit 組成

燈號順序為: 綠、黃、紅、綠….

Sequential circuit: state register

If Set = 1 or reset = 1: current state = green light

If Jump = 1: current state = red light

If Stop = 1: current state = current state

Else current state = next state

1st combinational circuit: next state logic

根據 current state:

If recount = 1 => next state 為下一個燈號順序，否則保持原燈號。

2nd combinational circuit: output logic

根據 current state 決定 control signal

- Counter: 一個 Sequential circuit 組成

If (rst | Jump | Set | Recount_counter) => count out = 1

If Stop => count out = count out

Else count out = count out + 1

- Compare: 以一個 combinational circuit 和一個 Sequential circuit 組成

Sequential circuit: 儲存各燈號秒數

If Set = 1 => 將 Rin, Yin, Gin 存入 register

Sequential circuit: 比較 counter 是否等於對應燈號秒數，如果等於，將 recount 設為 1，否則 recount = 0