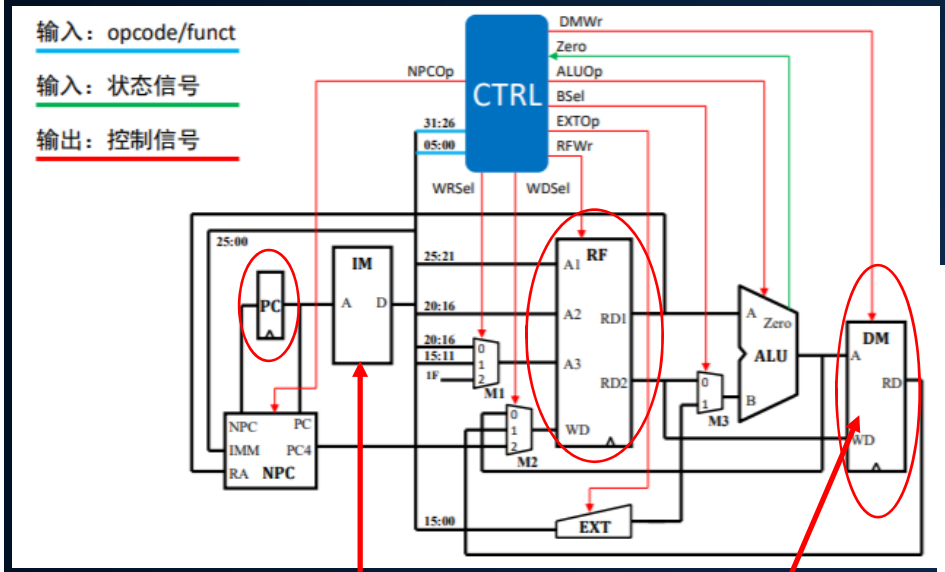
单周期CPU设计与实现

薛睿、仇洁婷、郑海刚

关于时序-实现方式1



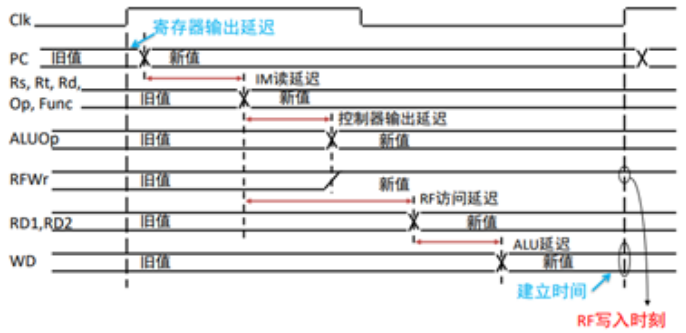
Distributed Memory IP（LUT-based）
实现IM、DM

组合逻辑部件

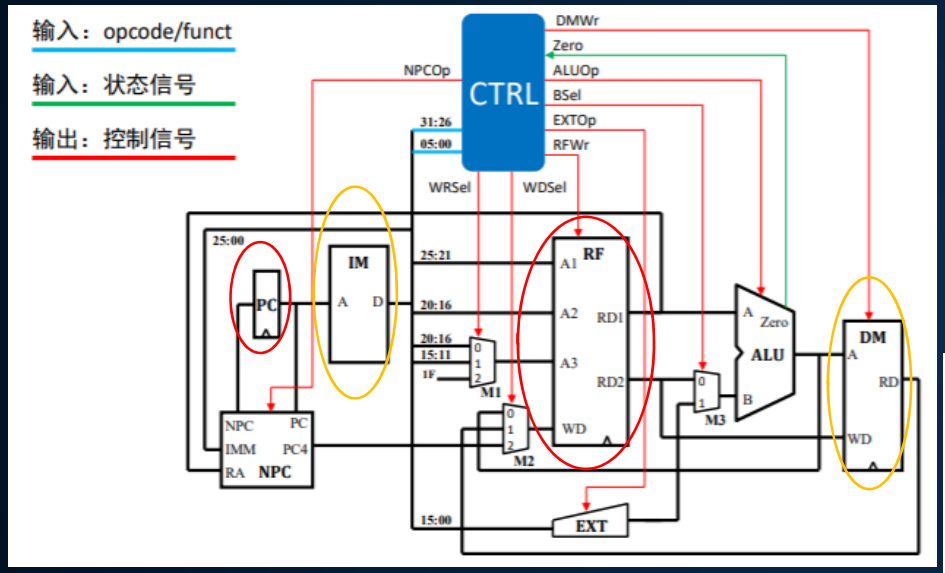
时序逻辑部件

Add指令执行延迟分析

- 执行延迟包括：PC输出延迟、IM读延迟、控制器输出延迟、ALU运算延迟、寄存器建立延迟



关于时序-实现方式2



Block Memory实现IM、DM