Schematics Only for RK3576 EVB1

RK_EVB1_RK3576_LP4XD200P132SD6_V12

Main Functions Introduction

1) PMIC: 1 x RK806S-5 + DiscretePower
2) RAM: 1 x LPDDR4X 32bit(Option 1 x LPDDR4 32bit)
3) ROM: 1 x eMMC5.1 + 1 x UFS2.0 (Option SPI Nand Falsh)
4) Support: 1 x Micro SD Card3.0
5) Support: 1 x USB TYPEC + 1 x USB3.2 Gen1x1 HOST1
6) Support: 1 x PCIe Slot (Option)
7) Support: 1 x 4Lanes MIPI DCPHY RX Camera(Need Ext Board)
8) Support: 2 x 4Lanes or 4 x 2Lanes MIPI DPHY RX Camera(Need Ext Board)
9) Support: 1 x 4Lanes MIPI DSI TX with Touch Connector
10) Support: 1 x HDMI2.1 TX (Up to 4Kx2K@120Hz)
11) Support: 1 x a/b/g/n/ac/ax 2T2R PCIe WIFI6 + UART/PCM BT
12) Support: 2 x 10/100/1000M Ethernet
13) Support: 1 x Headphone + 2 x SPK + 1 x Analog MIC
14) Support: 1 x Array MIC Connector(Ext PDM MicArray Board)
15) Support: 1 x IR Receiver
16) Support: 1 x G-Sensor
17) Support: Array Key(MENU,VOL+,VOL-,ESC)
18) Support: 7 x SARADC + 1 x SARADC only for boot
19) Support: 1 x Debug UART to USB connector and 1 x JTAG Connector
20) Support: 1 x CAN(Option)
21) Support: 3 x LED

Note:

The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic.
If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	00.Cover Page		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang / Reviewed by:	Sheet:	1 of 49

Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. NC stands for component not mounted temporarily
2. If Value or option is NC, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

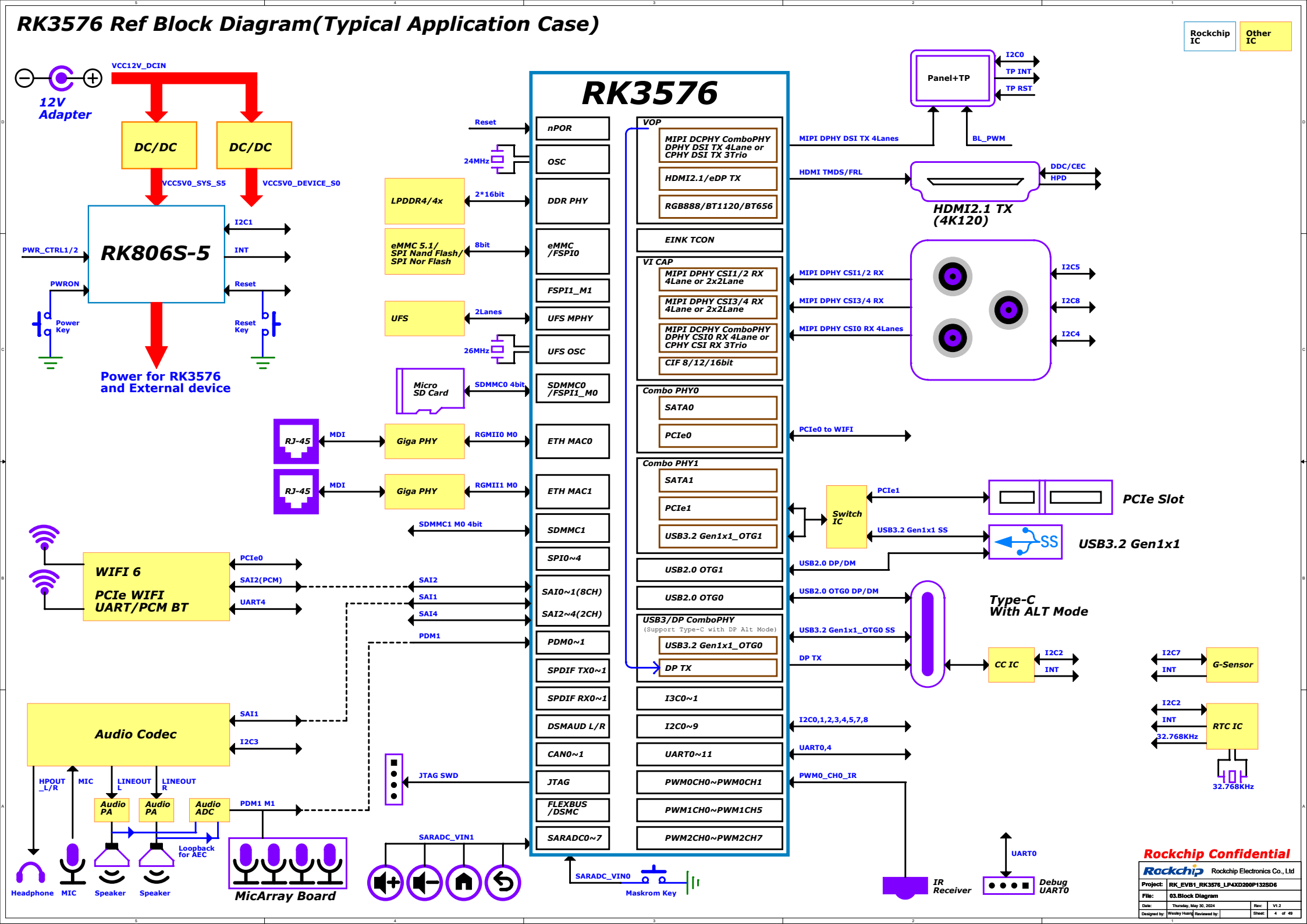
Rockchip Electronics Co., Ltd					
Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	01.Index and Notes				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:		Sheet:	2 of 49

Revision History

Version	Date	By	Change Dsecription	Approved
V0.1	2023-11-17	Wesley Huang	1: Draft version;	
V0.2	2023-11-27	Wesley Huang	1. Ordinary GPIO can be used to implement the PCIE21_PERSTN_Mx function, so remove the PCIE21_PERSTN_Mx function name from IOMUX; 2. Adjusting the usage of some GPIO; 3. Replace the level conversion circuit; 4. Renaming Pin names of RK3576 related to PCIE and SATA; 5. PMIC PWR CTRL control strategy adjustment: Modify the scheme to only require 2 PWR_CTRL control signals; 6. Modification of filtering capacitors for DDR and analog PHY power supply: VDDQ_DDR_S0: C1202 changed to 1uF-0201, C1205 changed to 22uF; VDD_DDR_S0: Change C1202, C1209 and C1211 to 1uF, 10uF-0402, and 22uF; UFS: C1303 and C1306 changed to 1uF; MIPI DCPHY: C1505 changed to 1uF; MIPI CSI1/2: C1501 changed to 1uF; MIPI CSI3/3: C1508 changed to 1uF; 7. Some detailed adjustments.	
V1.0	2023-12-11	Wesley Huang	1. Modify the circuit of peripheral devices, such as fans and IR. 2. Modifying the timing of RK806S-5	
V1.01	2024-03-21	Wesley Huang	Modification of BOM: 1. NPU: C1038 changed to 22uF-0603; add C1040-47uF-0805; C2318/C2319/C2323 change to NC; R2309 change to NC; 2. GPU: C1031 changed to 22uF-0603; add C1039-22uF-0603; C2304/C2305/C2306 change to NC; R2303 change to NC; 3. BOOT MODE CONFIG change to Config8: R1102 change to 43K; R1103 change to 100K;	
V1.1	2024-04-15	Wesley Huang	1. 8bit FSPI change to 4bit FSPI 2. Some detailed adjustments.	
V1.2	2024-05-30	Wesley Huang	1. SARADC_AVDD1V8 pin of RK3576 is changed to use the PLDO2 power supply of RK806S-5; The timing of the PLDO2 power supply is changed from 3 to 5. 2. The PCB package of RK3576 is modified to BGA698_16R1X17R2X1R08. 3. EN control signal of VCC1V2_UFS_VCCQ_S0' DCDC is changed. 3. Some detailed adjustments.	

RK3576 Ref Block Diagram(Typical Application Case)

Rockchip IC | Other IC



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Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_EVB1_RK3576_LP4XD200P132SD6
File:	03.Block Diagram
Date:	Thursday, May 30, 2024
Rev:	V1.2
Designed by:	Wesley Huang
Reviewed by:	
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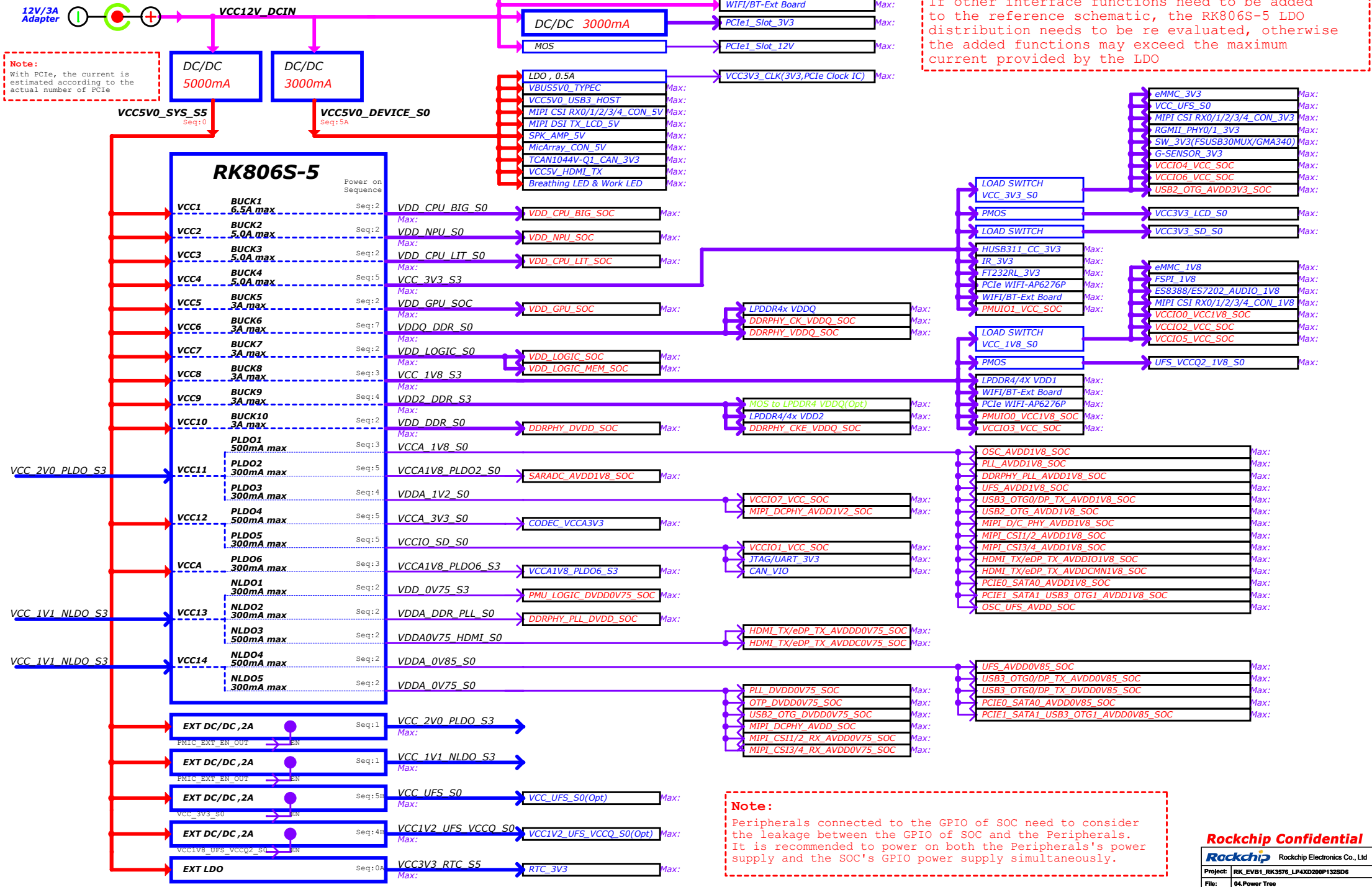
Power Tree



Note:
The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic. If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Note:
Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_EVB1_RK3576_LP4XD200P132SD6
File:	04.Power Tree
Date:	Thursday, May 30, 2024
Rev:	V1.2
Designed by:	Wesley Huang
Reviewed by:	
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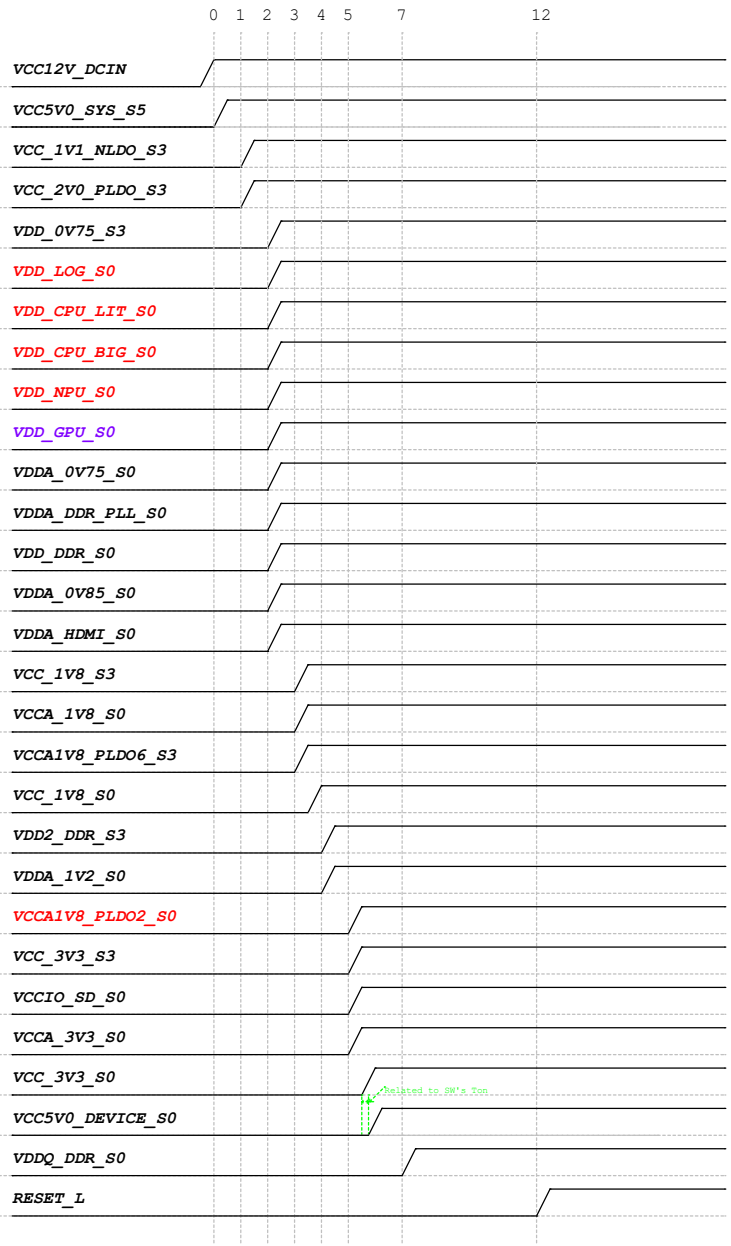
Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:5	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	5A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCC_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Note:

The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

Note:

Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

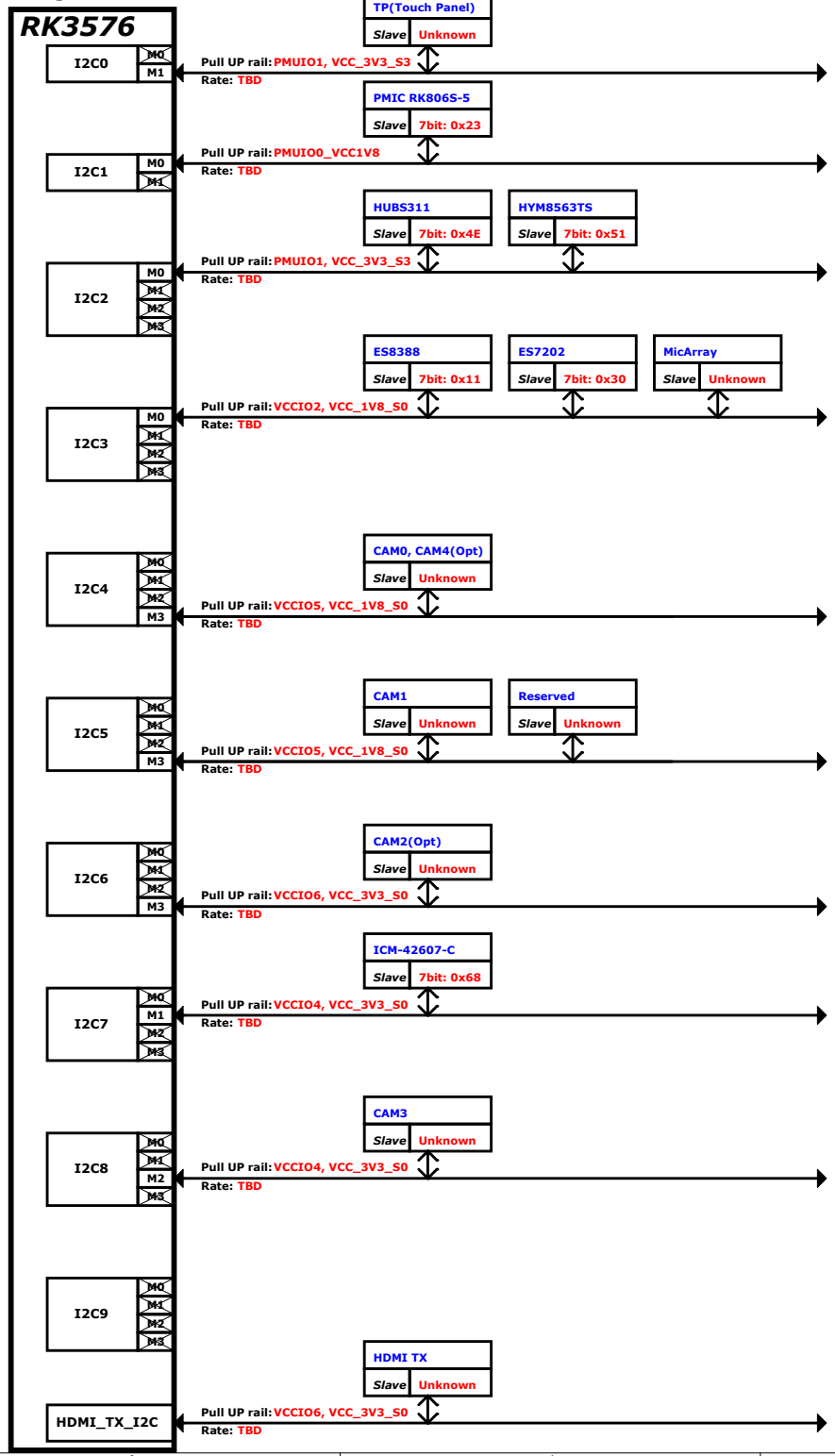
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

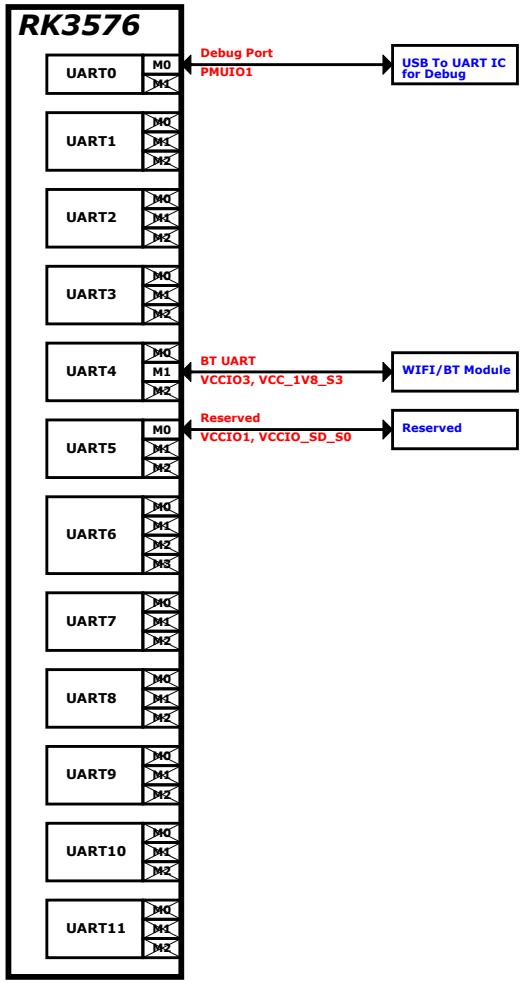
IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	05.Power Sequence and Map				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:		Sheet:	6 of 49

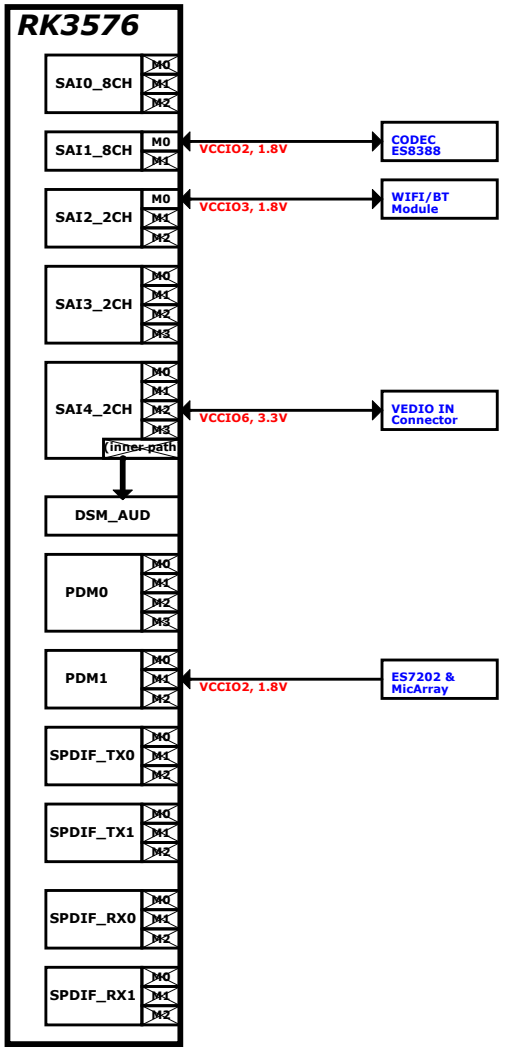
I2C MAP



UART MAP



Audio MAP



Note:

M0 Unselected IOmux path

M1 IOmux path in use

At the same time, only one path can be selected.

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_EVB1_RK3576_LP4XD200P132SD6
File:	05.Lower-Speed Bus Map
Date:	Thursday, May 30, 2024
Rev:	V1.2
Designed by:	Wesley Huang
Reviewed by:	
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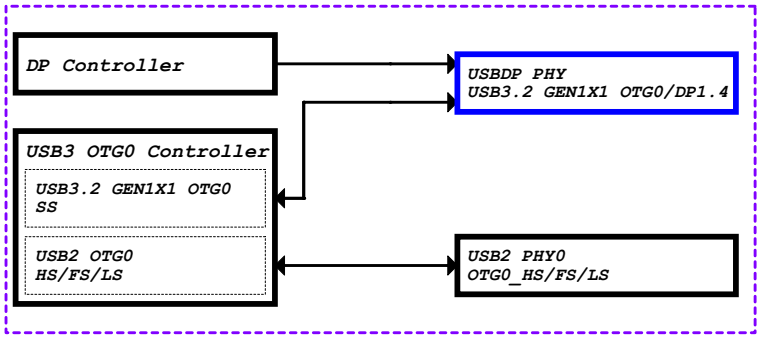
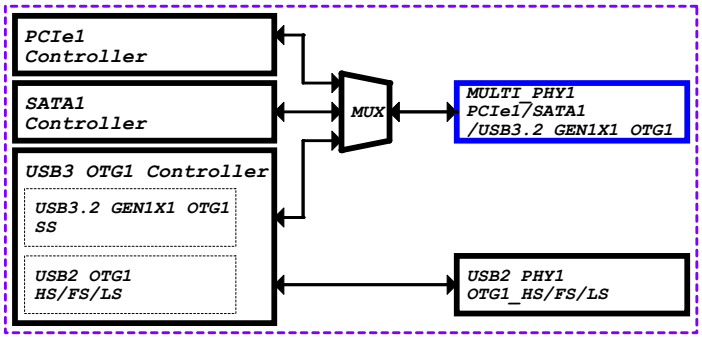
MULTI_PHY Path Map

USBDP PHY--USB3.2 GEN1X1 OTG0/DP1.4



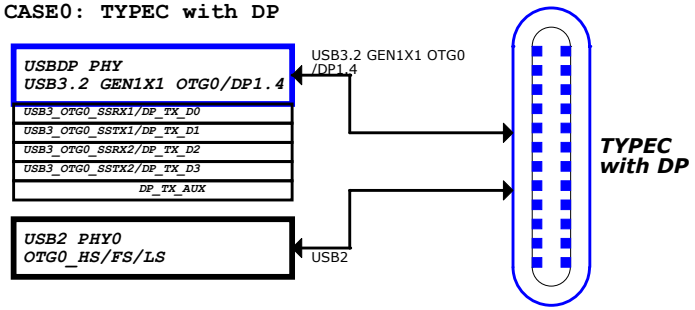
PCIe Combo PHY1--
PCIe1/SATA1/USB3.2 GEN1X1 OTG1



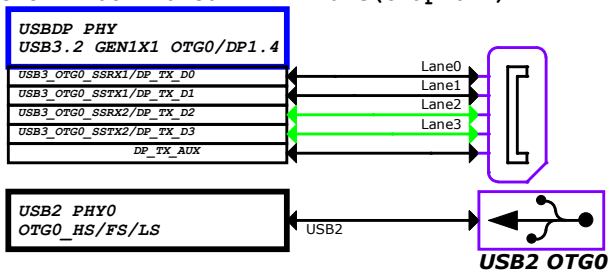
Note:
USB2 PHY1 can only be used when PCIE1/SATA1 is not in use!!!

USB OTG0/DP Application

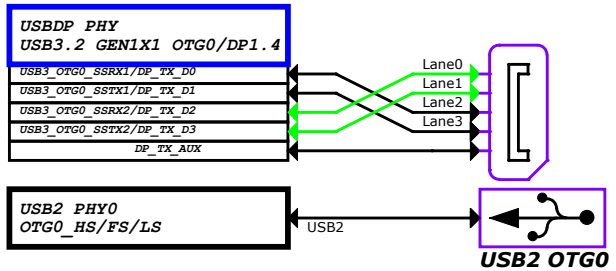
CASE0: TYPEC with DP



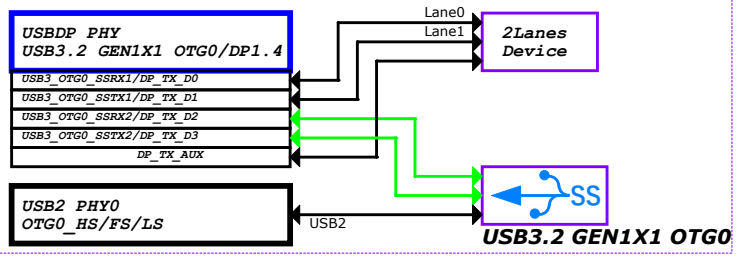
CASE1: USB2 OTG0 + DP 4Lane(Swap OFF)



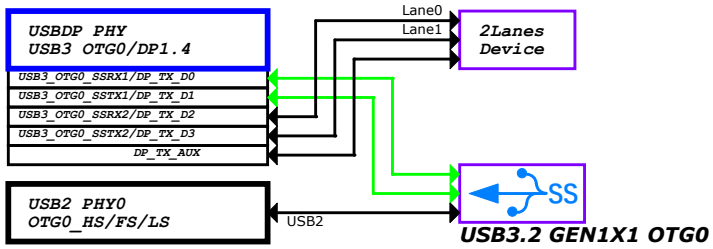
CASE2: USB2 OTG0 + DP 4Lane(Swap ON)



CASE3: USB3.2 GEN1X1 OTG0 + DP 2Lane(Swap OFF)



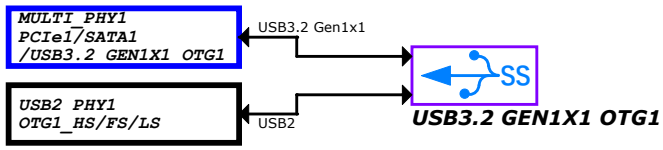
CASE4: USB3.2 GEN1X1 OTG0 + DP 2Lane(Swap ON)



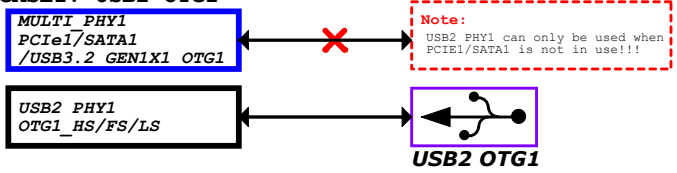
Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

USB OTG1 Application

CASE0: USB3.2 GEN1X1 OTG1

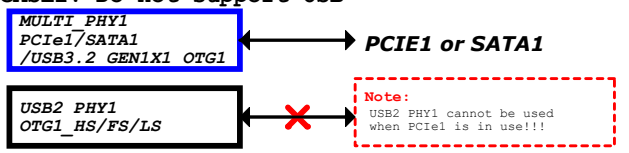


CASE1: USB2 OTG1



Note:
USB2 PHY1 can only be used when PCIE1/SATA1 is not in use!!!

CASE2: Do not support USB



Note:
USB2 PHY1 cannot be used when PCIe1 is in use!!!

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_EVB1_RK3576_LP4XD200P132SD6
File:	07.USB/DP Configure Map
Date:	Thursday, May 30, 2024
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Designed by:	Wesley Huang
Reviewed by:	
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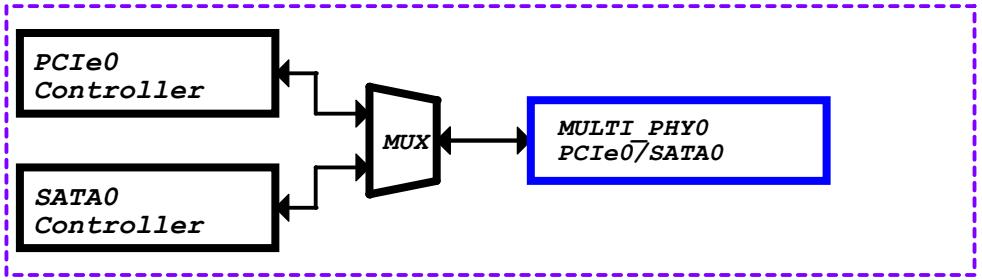
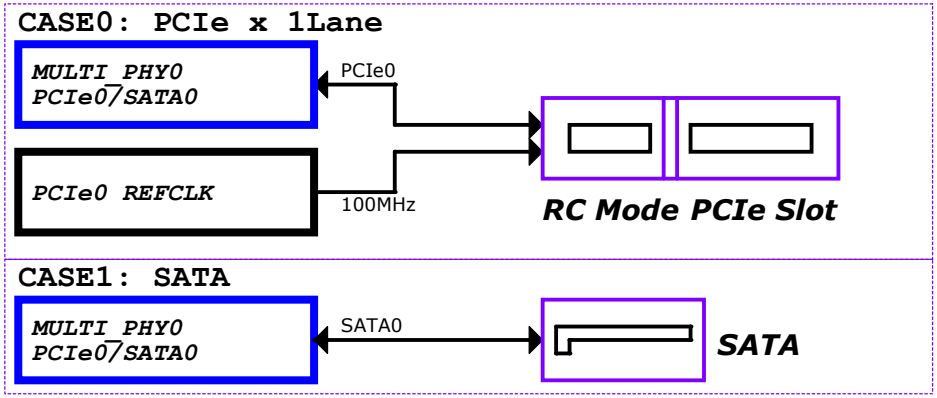
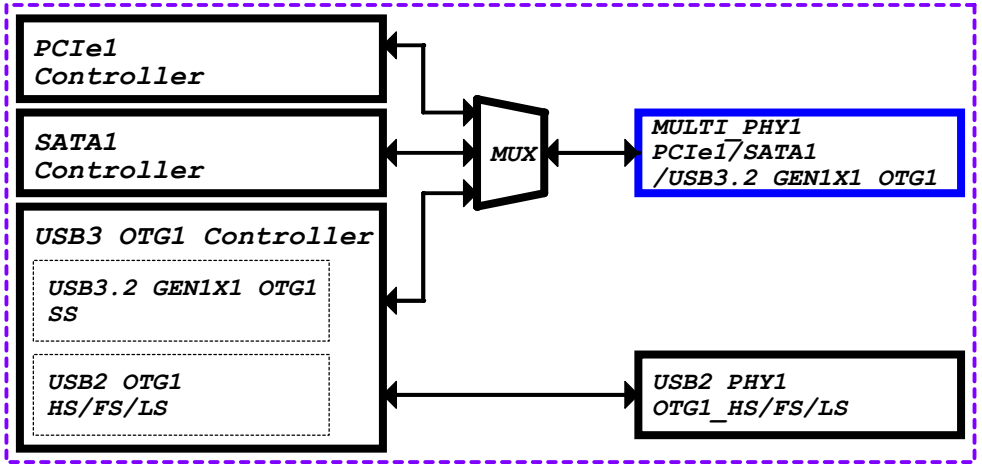
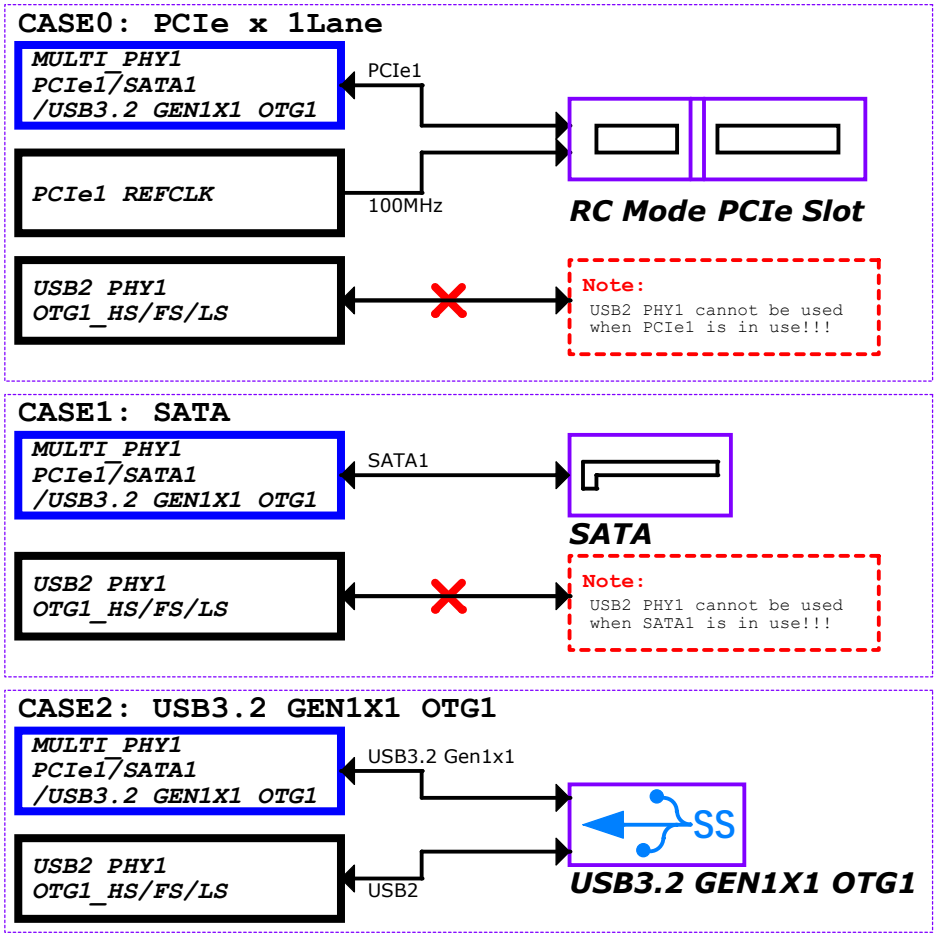
PCIe Combo PHY0--PCIe0/SATA0





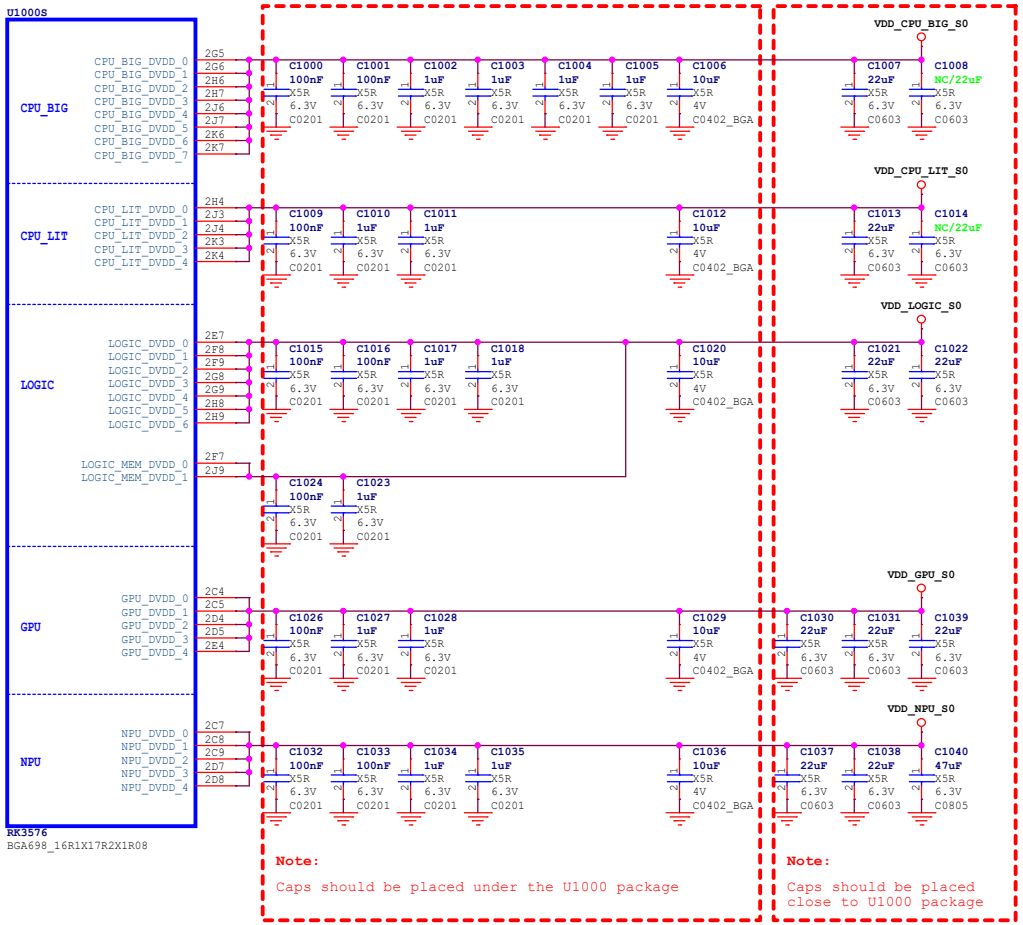
PCIe Combo PHY1--
PCIe1/SATA1/USB3.2 GEN1X1 OTG1



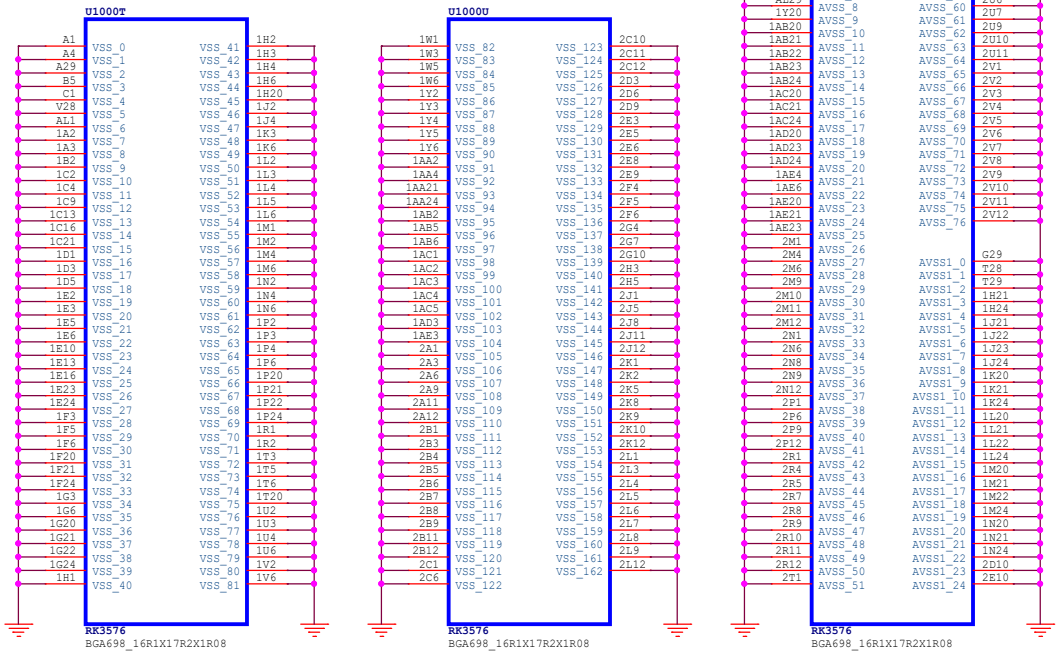


Rockchip Electronics Co., Ltd					
Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	08.PCIe Combo PHY Configure Map				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:		Sheet:	9 of 49

RK3576_S (Power)



RK3576_T/U/V (GND)



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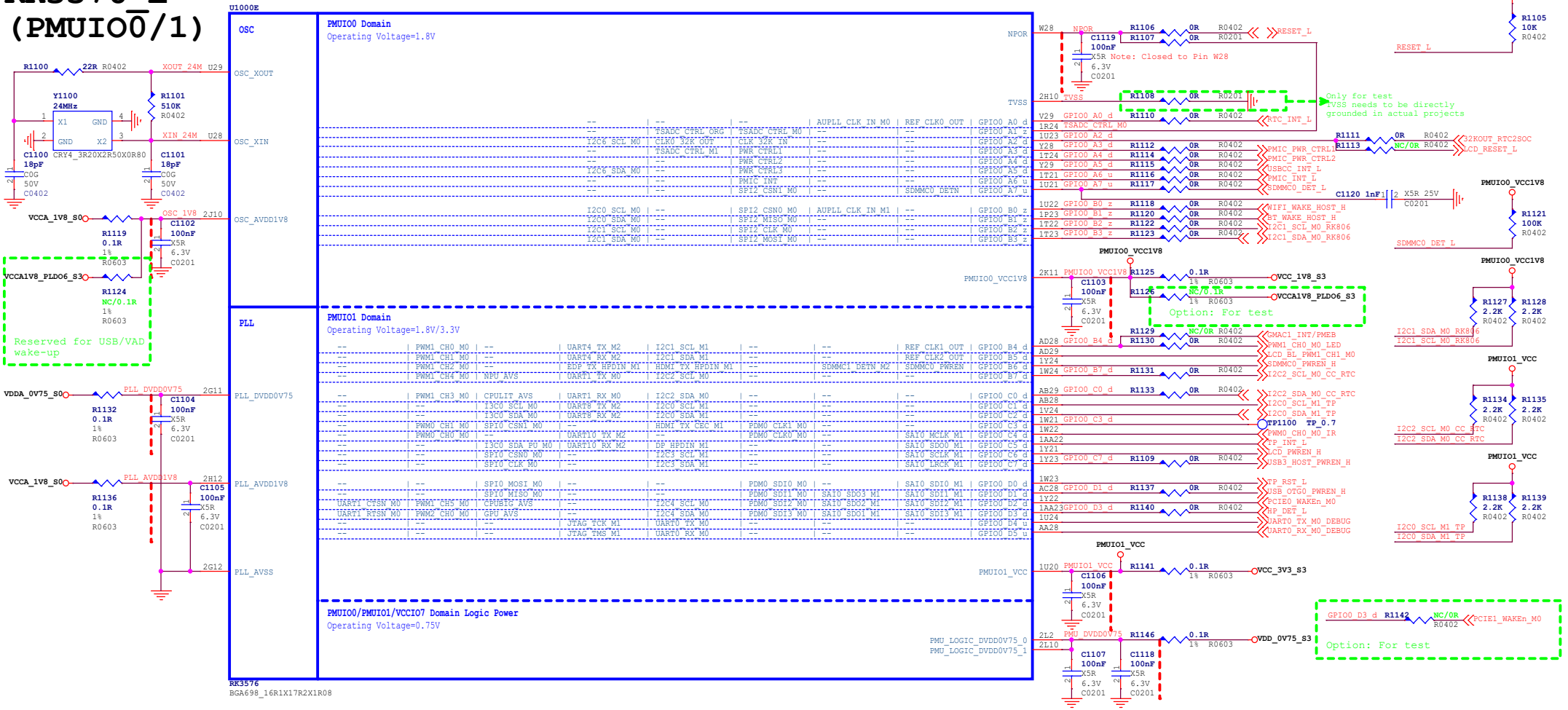
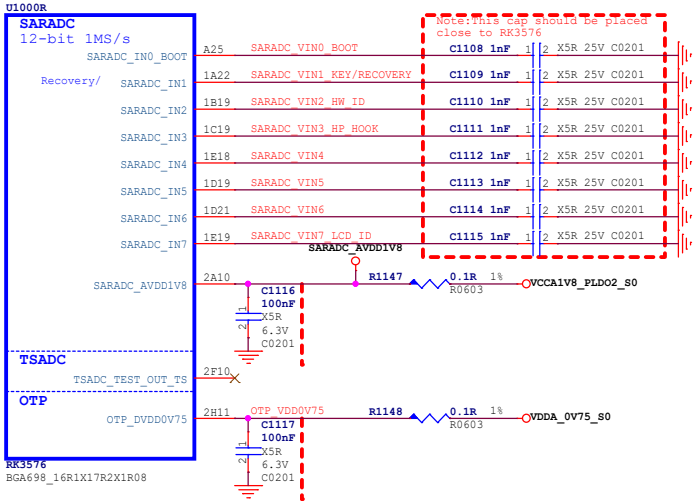
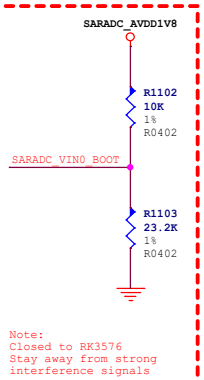
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	10.RK3576-Power/GND				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:		Sheet:	10 of 49

RK3576_E (PMUIO0/1)



RK3576_R (SARADC)



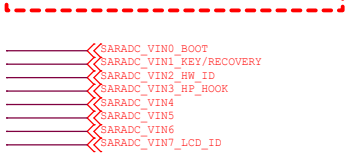


BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

Item	Rup	Rdown	ADC Value	Boot Mode
Config1	NC	10K	0	USB (Maskrom mode)
Config2	10K	1.13K	416	FSPI0->USB
Config3	10K	2.49K	816	FSPI1_M0->EMMC->USB
Config4	10K	4.3K	1231	FSPI1_M1->EMMC->USB
Config5	10K	6.8K	1658	FSPI0->UFS->USB
Config6	10K	10K	2048	FSPI1_M0->UFS->USB
Config7	10K	14.7K	2437	UFS->USB
Config8	10K	23.2K	2862	UFS->SDMMC0->USB
Config9	10K	40.2K	3279	RFU
Config10	10K	88.7K	3680	EMMC->SDMMC0->USB
Config11	10K	NC	4095	EMMC->USB

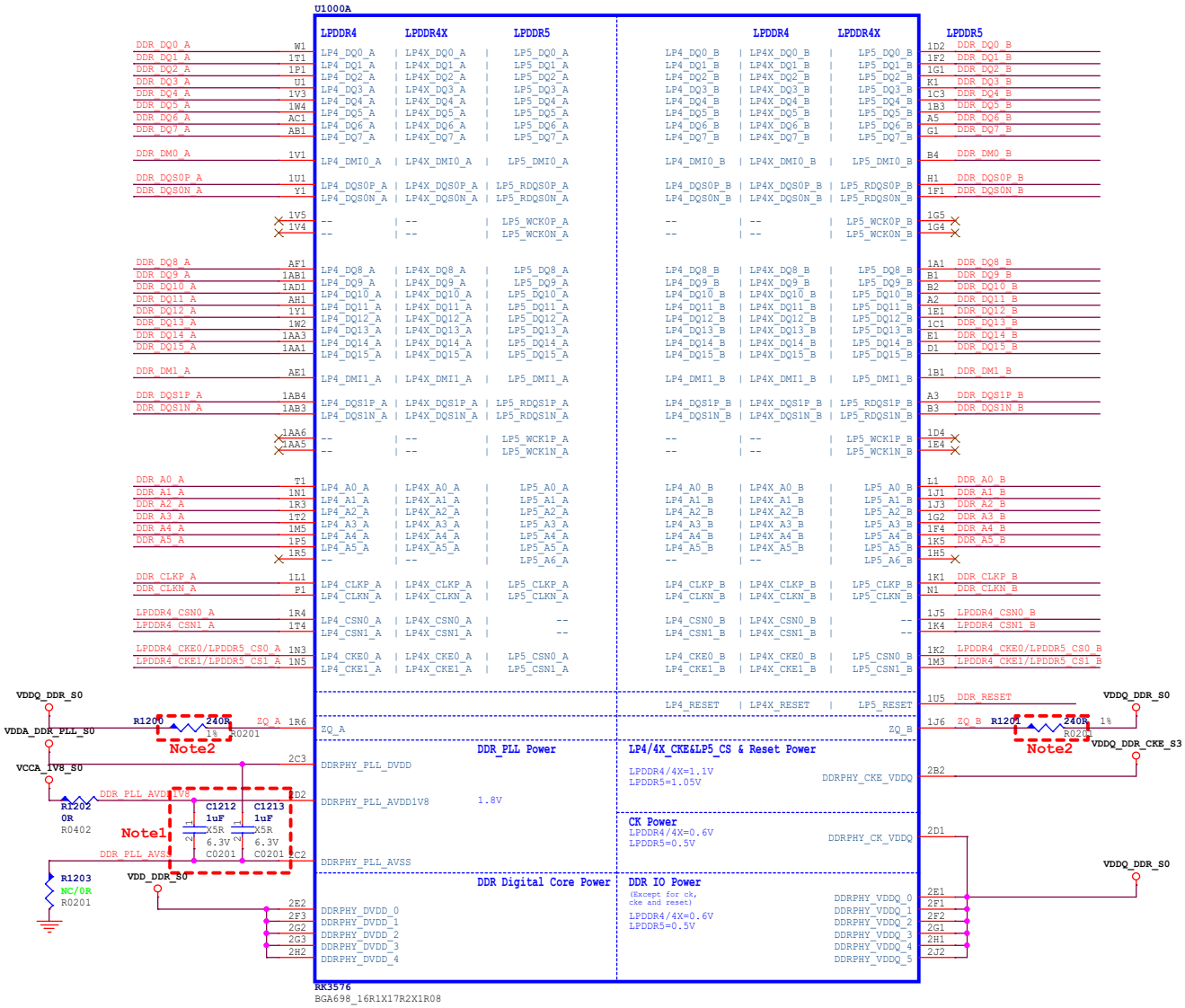
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



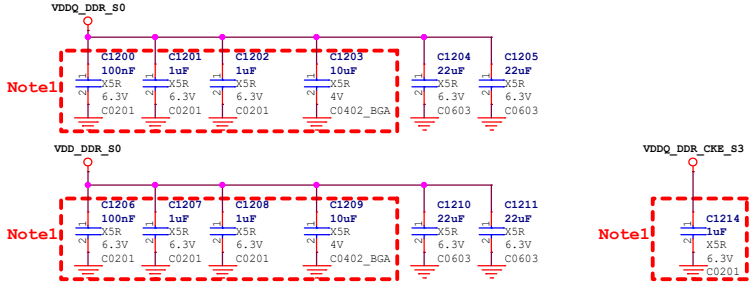
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_EVB1_RK3576_LP4XD200P132SD6
File:	11.RK3576-OSC/PLL/PMUIO/SARADC
Date:	Thursday, May 30, 2024
Rev:	V1.2
Designed by:	Wesley Huang
Reviewed by:	
Sheet:	11 of 49

RK3576_A(DDRPHY)



DDR FILTER

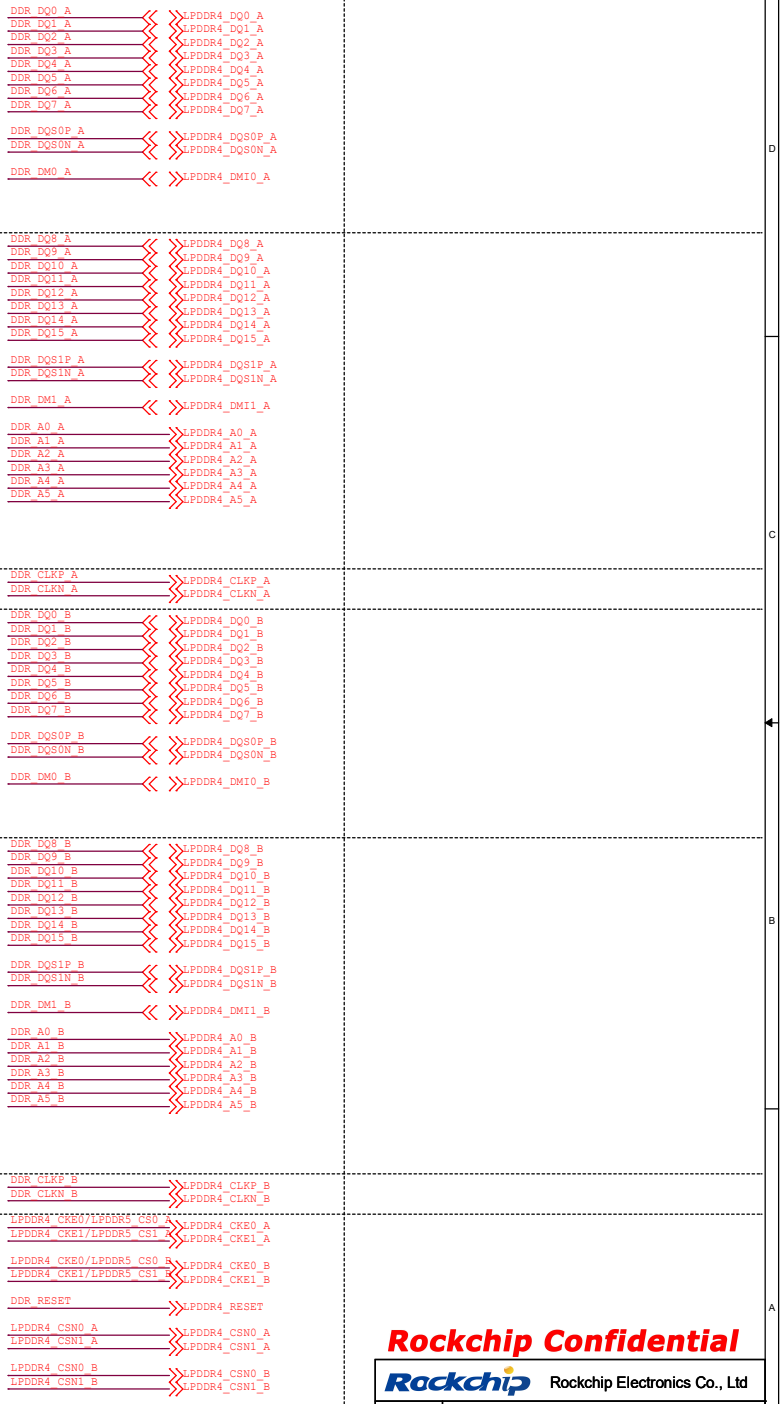


Note:
(1) Power Sequence: VDD-VDDQ_CKE-VDDQ
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

Note1:
Caps in the red line dotted box should be placed under the U1000 package

Note2:
Resistors in the red line dotted box should be placed under the U1000 package

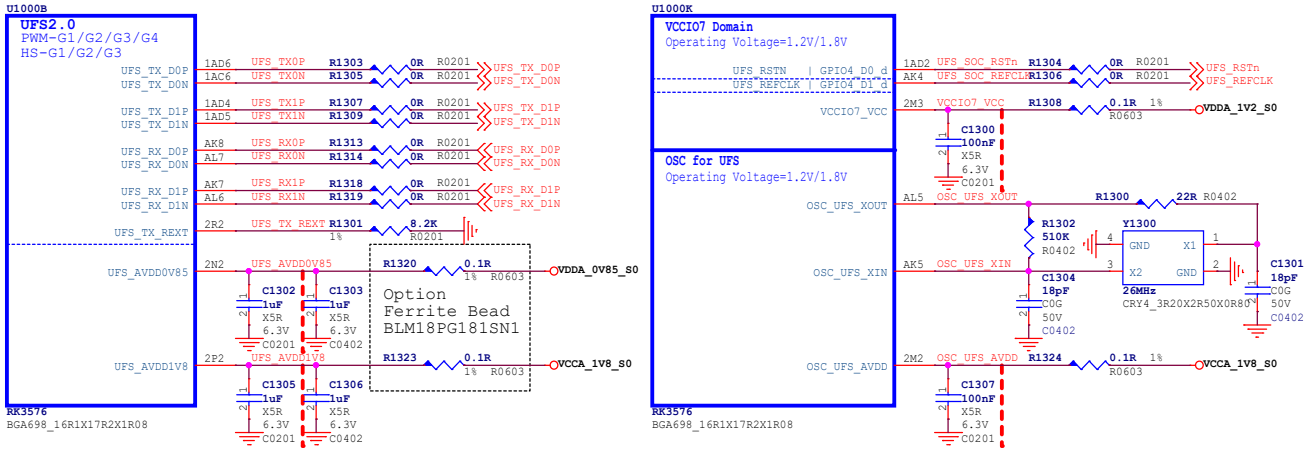
LPDDR4 Signal



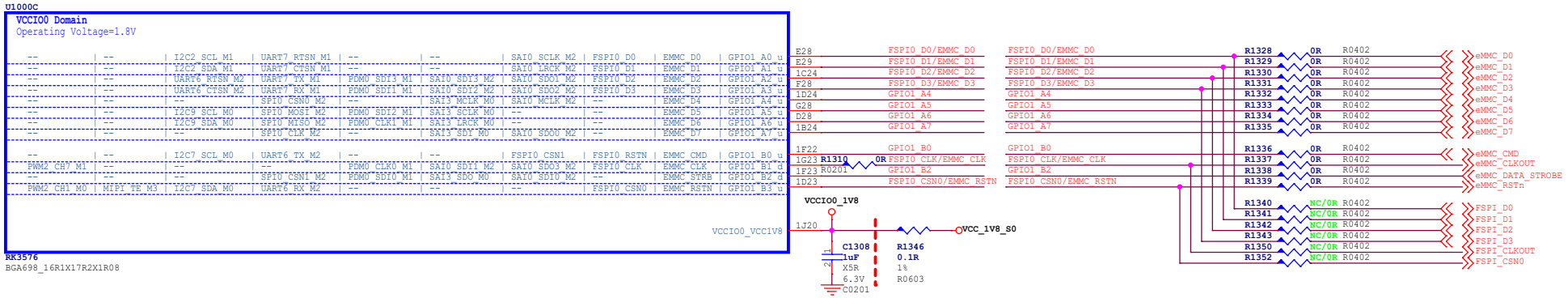
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	12.RK3576-DDR PHY				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:		Sheet:	12 of 49

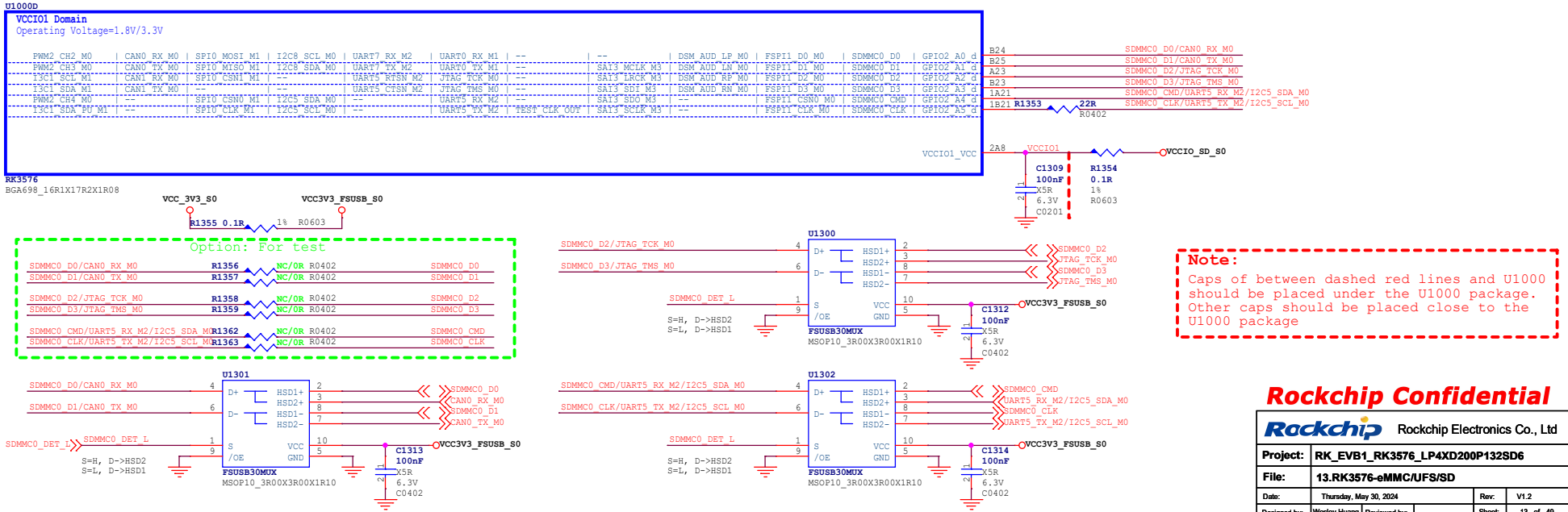
RK3576_B (UFS2.0)



RK3576_C (VCCIO0)



RK3576_D (VCCIO1)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	13.RK3576-eMMC/UFS/SD		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet: 13 of 49

RK3576_L (USB3/DP)

U1000L

USB3 OTG0/DP1.4 Alt
USB:USB3.2 Gen1x1 OTG0
DP :RBR/HBR/HBR2/HBR3

--	DP_TX_AUXP
--	DP_TX_AUXN
USB3_OTG0_SSRX1P	DP_TX_D0P
USB3_OTG0_SSRX1N	DP_TX_D0N
USB3_OTG0_SSTX1P	DP_TX_D1P
USB3_OTG0_SSTX1N	DP_TX_D1N
USB3_OTG0_SSRX2P	DP_TX_D2P
USB3_OTG0_SSRX2N	DP_TX_D2N
USB3_OTG0_SSTX2P	DP_TX_D3P
USB3_OTG0_SSTX2N	DP_TX_D3N
USB3_OTG0_REXT	DP_TX_REXT
USB3_OTG0_DP_TX_AVDD0V85	
USB3_OTG0_DP_TX_DVDD0V85	
USB3_OTG0_DP_TX_AVDD1V8	

RK3576
BGA698_16R1X17R2X1R08

Support:
Type-C With Displayport Alternate Mode

2T2 DP_TX_AUXP
2T3 DP_TX_AUXN
AK10 USB3_OTG0_SSRX1P/DP_TX_D0P
AL10 USB3_OTG0_SSRX1N/DP_TX_D0N
AL11 USB3_OTG0_SSTX1P/DP_TX_D1P
AK11 USB3_OTG0_SSTX1N/DP_TX_D1N
AK12 USB3_OTG0_SSRX2P/DP_TX_D2P
AL12 USB3_OTG0_SSRX2N/DP_TX_D2N
AL13 USB3_OTG0_SSTX2P/DP_TX_D3P
AK13 USB3_OTG0_SSTX2N/DP_TX_D3N
2T7 USB3_OTG0_DP_TX_REXT R1400 8.2K 1% R0201
2M5 USB3_OTG0/DP_TX_AVDD0V85 VDDA_0V85_S0
2N5
C1400 1uF X5R 6.3V C0201
C1401 NC/1uF X5R 6.3V C0402
R1403 0.1R 1% R0603
2N4 USB3_OTG0/DP_TX_AVDD1V8 VCCA_1V8_S0
C1402 1uF X5R 6.3V C0201
C1403 NC/1uF X5R 6.3V C0402
R1404 0.1R 1% R0603

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_M (USB2)

U1000M

USB2 OTG0
OTG/HOST/DEVICE
HS/FS/LS
Download Port

USB2_OTG0_DP	
USB2_OTG0_DM	
USB2_OTG0_ID	
USB2_OTG0_VBUSDET	
USB2_OTG0_REXT	

USB2 OTG1
OTG/HOST/DEVICE
HS/FS/LS

USB2_OTG1_DP	
USB2_OTG1_DM	
USB2_OTG1_ID	
USB2_OTG1_VBUSDET	
USB2_OTG1_REXT	
USB2_OTG_DVDD0V75	
USB2_OTG_AVDD1V8	
USB2_OTG_AVDD3V3	

RK3576
BGA698_16R1X17R2X1R08

Note!!!
The USB2 PHY1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected

AK9 USB2_OTG0_DP
AL9 USB2_OTG0_DM
2R6 USB2_OTG0_ID Note: There is an internal pull-up resistor connected to 1.8V
TP1400 TP_0.7
2P3 USB2_OTG0_VBUSDET
C1404 100nF X5R 10V C0402
2R3 USB2_OTG0_REXT R1401 200R 1% R0201
2T4 USB2_HOST1_DP
2T5 USB2_HOST1_DM
2T9 USB2_OTG1_ID
TP1401 TP_0.7
VCC5V0_USB3_HOST1
2T10 USB2_OTG1_VBUSDET
2U8 USB2_OTG1_REXT R1402 200R 1% R0201
C1409 100nF X5R 10V C0201
R1406 20K R0402
R1405 10K R0402
Option: For test
2P5 USB2_OTG_DVDD0V75 R1407 0.1R 1% R0603 VDDA_0V75_S0
C1405 100nF X5R 6.3V C0201
R1408 NC/0.1R 1% R0603 VDD_0V75_S3
2P4 USB2_OTG_AVDD1V8 R1409 0.1R 1% R0603 VCCA_1V8_S0
C1406 100nF X5R 6.3V C0201
C1407 NC/1uF X5R 6.3V C0402
R1410 NC/0.1R 1% R0603 VCC_1V8_S3
2P7 USB2_OTG_AVDD3V3 R1412 0.1R 1% R0603 VCC_3V3_S0
C1408 100nF X5R 6.3V C0201
R1411 NC/0.1R 1% R0603 VCC_3V3_S3

Reserved for test
USB wakes up SOC

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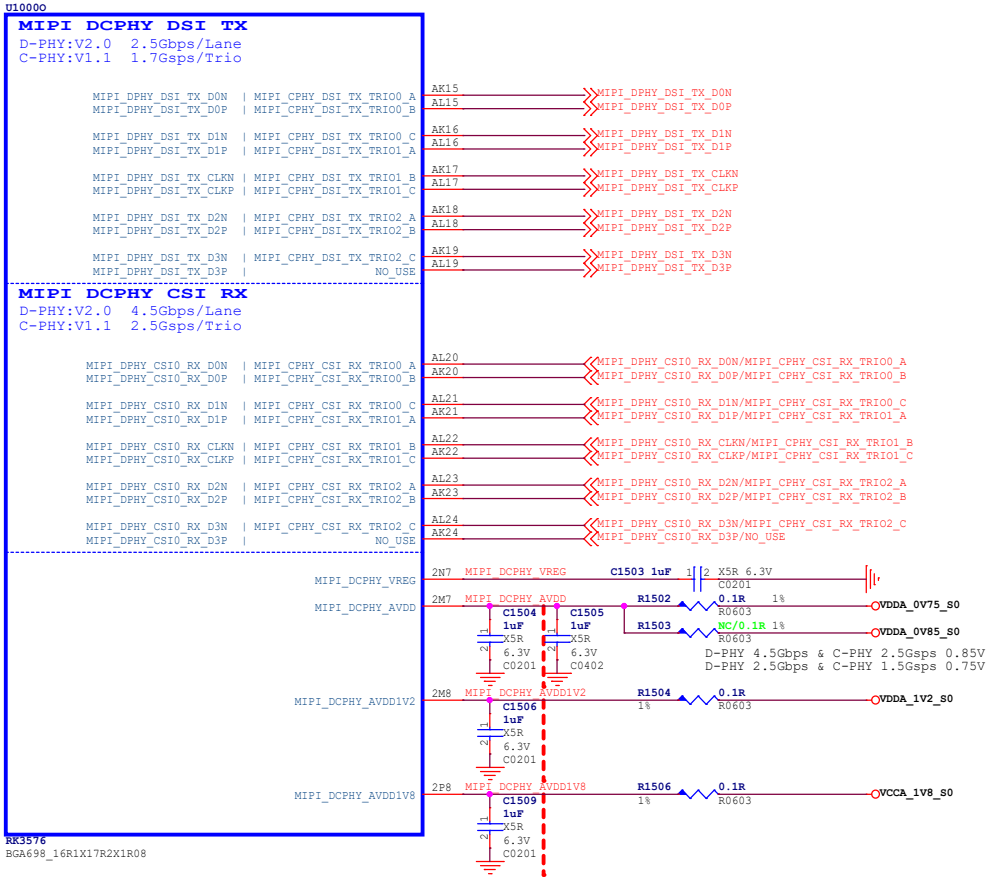
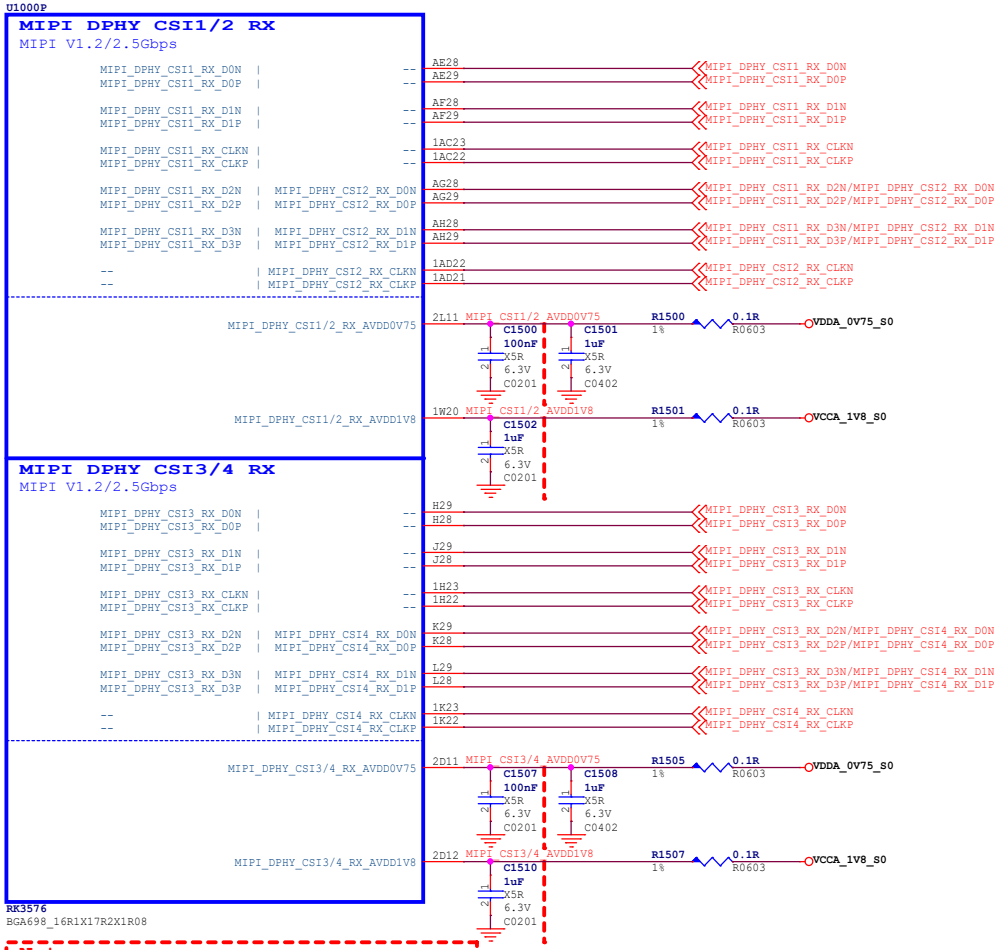
Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	14.RK3576-TypeC/USB		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by: Wesley Huang	Reviewed by:	Sheet:	14 of 49

RK3576_O(MIPI DCPHY)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_P(MIPI DPHY CSI RX)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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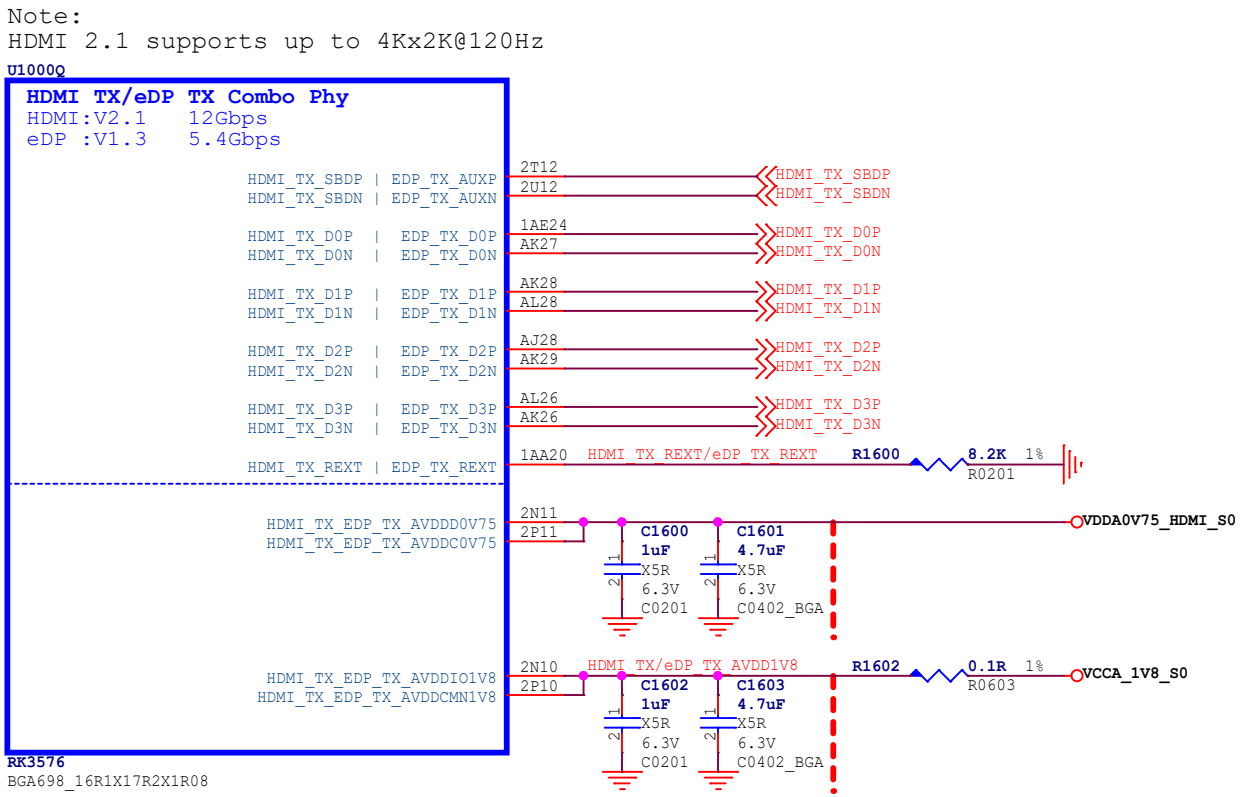
Rockchip Electronics Co., Ltd					
Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	15.RK3576-MIPI DSI/CSI				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:		Sheet:	15 of 49

RK3576_Q(HDMI/eDP)

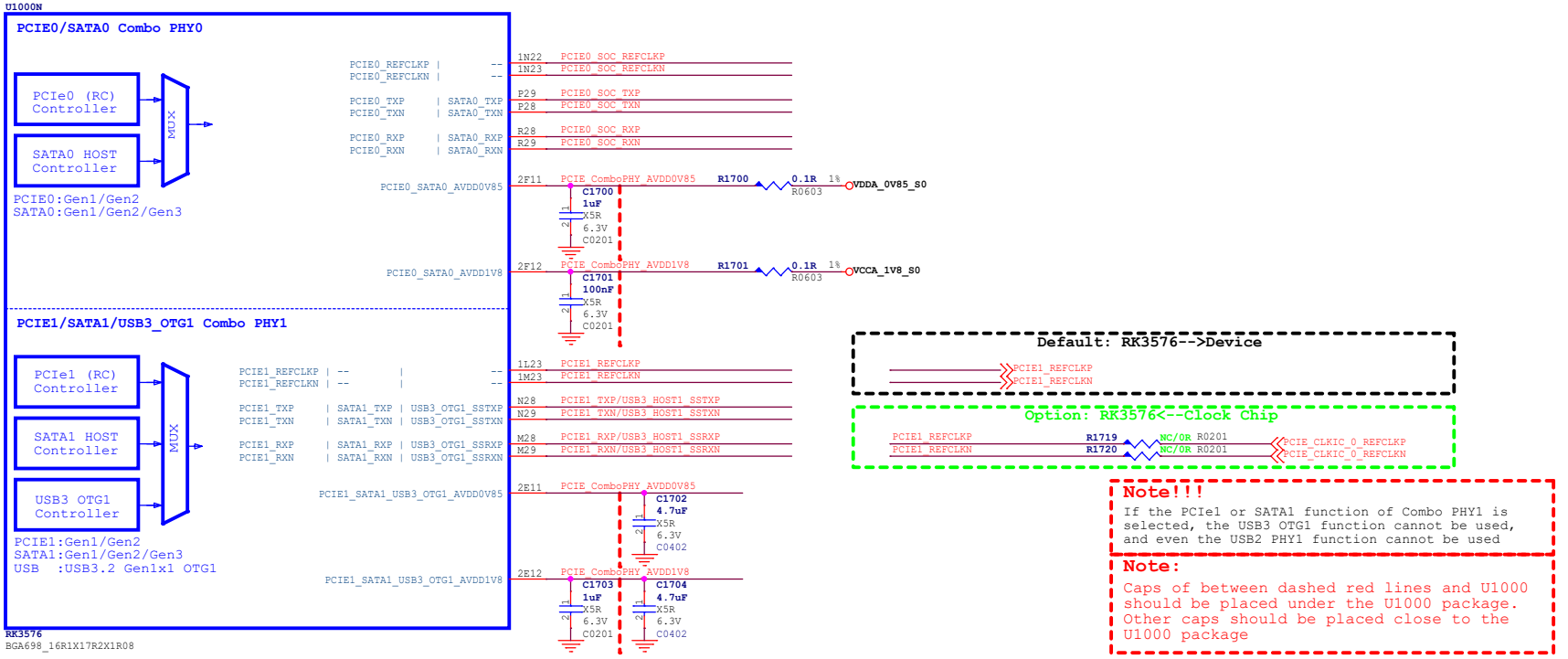


Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

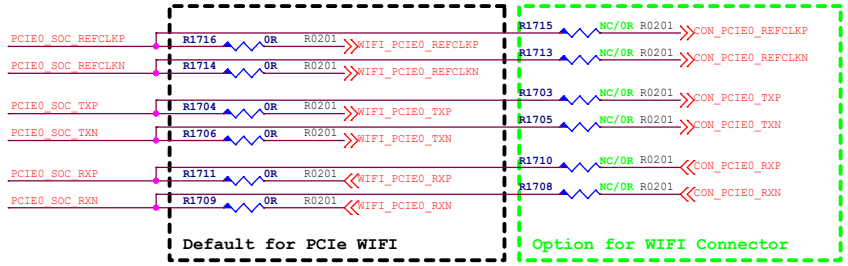
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	16.RK3576-HDMI/eDP				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:		Sheet:	16 of 49

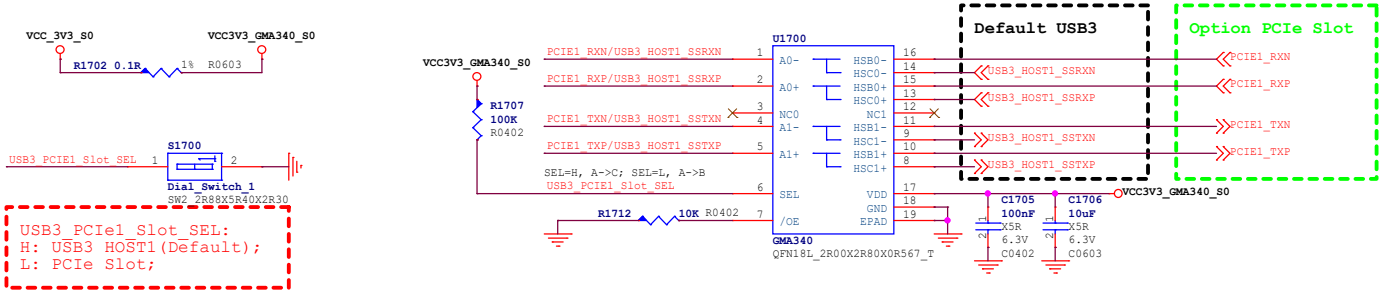
RK3576_N(PCIe/SATA/USB3)



PCIe Port0



PCIe Port1



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	17.RK3576-PCIe/SATA/USB3				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:		Sheet:	17 of 49

RK3576_F(VCCIO2)

U1000F

VCCIO2 Domain
Operating Voltage=1.8V/3.3V

PWM2_CH5_M0	--	--	--	--	AUPLL_CLK_IN_M2	SAI4_MCLK_M0	SAI1_MCLK_M0	GPIO4_A2_d
PWM2_CH4_M1	--	I2C2_SCL_M2	UART5_RTSN_M1	SPI3_CSN0_M2	FLEXBUS1_CSN_M4	--	--	SAI1_SCLK_M0	GPIO4_A3_d
CAN0_TX_M2	--	I2C4_SCL_M1	UART6_TX_M0	SPI3_MOSI_M2	FLEXBUS0_D13_M1	PDM1_SDI3_M1	SAI4_SCLK_M0	--	GPIO4_A4_d
--	PCIE1_CLKREQN_M2	I2C2_SDA_M2	UART5_CTSN_M1	SPI4_CSN1_M2	FLEXBUS1_D12_M1	--	--	SAI1_LRCK_M0	GPIO4_A5_d
CAN0_RX_M2	--	I2C4_SDA_M1	UART6_RX_M0	SPI3_MISO_M2	FLEXBUS0_D14_M1	PDM1_CLK0_M1	SAI4_LRCK_M0	--	GPIO4_A6_d
PWM2_CH6_M0	--	--	--	SPI3_CLK_M2	--	--	SAI4_SDI_M0	SAI1_SDO0_M0	GPIO4_A7_d
--	UART2_RTSN_M1	UART6_RTSN_M0	UART5_TX_M1	SPI4_CLK_M2	FLEXBUS1_D13_M1	PDM1_CLK1_M1	SAI1_SDI3_M0	SAI1_SDO1_M0	GPIO4_B0_d
--	UART2_CTSN_M1	UART6_CTSN_M0	UART5_RX_M1	SPI4_MOSI_M2	FLEXBUS1_D14_M1	PDM1_SDI2_M1	SAI1_SDI2_M0	SAI1_SDO2_M0	GPIO4_B1_d
--	--	MIPI_TE_M0	--	SPI4_MISO_M2	FLEXBUS1_D15_M1	PDM1_SDI1_M1	SAI1_SDI1_M0	SAI1_SDO3_M0	GPIO4_B2_d
PWM2_CH7_M0	--	--	--	SPI3_CSN1_M2	SPI4_CSN0_M2	--	PDM1_SDI0_M1	SAI4_SDO_M0	SAI1_SDI0_M0	GPIO4_B3_d
CAN1_RX_M2	--	I2C3_SDA_M0	UART2_RX_M1	--	FLEXBUS0_CSN_M4	--	--	SPDIF_RX0_M0	SAI1_SDO0_M0	GPIO4_B4_d
CAN1_TX_M2	PCIE0_CLKREQN_M2	I2C3_SCL_M0	UART2_TX_M1	--	FLEXBUS0_D15_M1	--	--	SPDIF_TX0_M0	SAI1_SDO0_M0	GPIO4_B5_d

RK3576
BGA698_16R1X17R2X1R08

1D6 GPIO4_A2_d R1802 0R R0402 SAI1_MCLK_M0
1C6 GPIO4_A3_d R1803 0R R0402 SAI1_SCLK_M0
1C5 GPIO4_A4_d R1804 0R R0402 PDM1_SDI3_M1_LOOPBACK
1B6 GPIO4_A5_d R1806 0R R0402 SAI1_LRCK_M0
1B5 GPIO4_A6_d R1807 0R R0402 PDM1_CLK0_M1_LOOPBACK
A7 GPIO4_A7_d R1808 0R R0402 SAI1_SDO0_M0

1A5 PDM1_CLK1_M1
B7 PDM1_SDI2_M1
B6 PDM1_SDI1_M1
1A6 GPIO4_B3_d R1810 0R R0402 SAI1_SDI0_M0
B8 I2C3_SDA_M0_Audio
1A4 I2C3_SCL_M0_Audio

VCCIO2
2A2 VCCIO2_VCC
C1800 100nF X5R 6.3V C0201
R1812 0.1R 1% R0603 VCCIO_AUDIO

VCCIO2
R1800 2.2K R0402
R1801 2.2K R0402
I2C3_SDA_M0_Audio
I2C3_SCL_M0_Audio

GPIO4_A4_d R1805 NC/0R R0402 PDM1_SDI3_M1
GPIO4_A6_d R1809 NC/0R R0402 PDM1_CLK0_M1
GPIO4_B3_d R1811 NC/0R R0402 PDM1_SDI0_M1

Option
Reserved for MIC Array Interface

RK3576_G(VCCIO3)

U1000G

VCCIO3 Domain
Operating Voltage=1.8V/3.3V

PWM1_CH0_M1	PCIE1_CLKREQN_M1	SPI1_CLK_M0	I2C9_SDA_M1	--	--	--	SAI3_SCLK_M1	--	SDMMC1_D0_M0	ETH1_RXD2_M1	GPIO1_B4_d
PWM1_CH1_M1	--	SPI1_MOSI_M0	I2C9_SCL_M1	--	--	--	SAI3_LRCK_M1	--	SDMMC1_D1_M0	ETH1_RXD3_M1	GPIO1_B5_d
--	PCIE0_CLKREQN_M1	SPI1_MISO_M0	--	UART3_CTSN_M2	--	--	SAI3_SDO_M1	--	SDMMC1_D2_M0	ETH1_RXCLK_M1	GPIO1_B6_d
--	--	SPI1_CSN0_M0	--	UART3_RTSN_M2	--	--	SAI3_SDI_M1	--	SDMMC1_D3_M0	ETH1_TXD2_M1	GPIO1_B7_d
PWM0_CH0_M1	--	SPI1_CSN1_M0	--	UART3_TX_M2	--	PDM0_SDI2_M2	--	--	SDMMC1_CMD_M0	ETH1_TXD3_M1	GPIO1_C0_d
--	--	--	--	UART3_RX_M2	--	PDM0_CLK0_M2	SAI3_MCLK_M1	--	SDMMC1_CLK_M0	ETH1_RXCLK_M1	GPIO1_C1_d
PWM1_CH2_M1	--	SPI2_CSN1_M1	I2C8_SCL_M1	UART4_RTSN_M1	--	--	FSPI1_CSN1_M1	FSPI1_RSTN_M1	SDMMC1_PWREN_M0	ETH1_RXSCLK_M1	GPIO1_C2_d
--	--	SPI2_CSN0_M1	I2C8_SDA_M1	UART4_CTSN_M1	--	--	--	FSPI1_CSN0_M1	SDMMC1_DETN_M0	ETH1_RXSTRB_M1	GPIO1_C3_d
--	PCIE0_BUTTONRSTN	SPI2_MOSI_M1	UART2_RTSN_M0	UART4_TX_M1	--	--	--	FSPI1_D0_M1	--	ETH1_TXD0_M1	GPIO1_C4_d
--	PCIE1_BUTTONRSTN	SPI2_MISO_M1	UART2_CTSN_M0	UART4_RX_M1	--	--	--	FSPI1_D1_M1	--	ETH1_TXD1_M1	GPIO1_C5_d
--	SATA_CPPOD	--	I2C8_SCL_M1	UART2_TX_M0	--	PDM0_SDI0_M2	--	FSPI1_D2_M1	--	ETH1_TXCTL_M1	GPIO1_C6_d
--	SATA_CPDET	--	I2C8_SDA_M1	UART2_RX_M0	--	PDM0_SDI1_M2	--	FSPI1_D3_M1	--	ETH1_RXD0_M1	GPIO1_C7_d
--	--	--	--	UART10_TX_M1	--	--	SAI2_SDO_M0	--	--	ETH1_RXD1_M1	GPIO1_D0_d
--	--	--	I3C0_SDA_PU_M1	UART10_RX_M1	--	--	SAI2_SCLK_M0	--	--	ETH1_RXCTL_M1	GPIO1_D1_d
PWM1_CH3_M1	--	--	I3C0_SCL_M1	--	--	--	SAI2_LRCK_M0	--	--	ETH1_MDC_M1	GPIO1_D2_d
PWM1_CH4_M1	--	--	I3C0_SDA_M1	--	--	--	SAI2_SDI_M0	--	--	ETH1_MDIO_M1	GPIO1_D3_d
--	--	--	I2C5_SCL_M1	UART10_RTSN_M1	SPDIF_RX1_M2	PDM0_SDI3_M2	SAI2_MCLK_M0	--	--	ETH1_MCLK_M1	GPIO1_D4_d
CLK1_32K_OUT	SATA_MPSWIT	SPI2_CLK_M1	I2C5_SDA_M1	UART10_CTSN_M1	SPDIF_TX1_M2	PDM0_CLK1_M2	--	FSPI1_CLK_M1	--	ETH_CLK1_25M_OUT_M1	GPIO1_D5_d

RK3576
BGA698_16R1X17R2X1R08

A28 SDMMC1_D0_M0
B27 SDMMC1_D1_M0
1A23 SDMMC1_D2_M0
A27 SDMMC1_D3_M0

B26 SDMMC1_CMD_M0
1B22 GPIO1_C1_d R1813 0R R0402 SDMMC1_CLK_M0
B29 GPIO1_C2_u R1814 0R R0402 UART4_RTSN_M1
1C23 GPIO1_C3_u R1815 0R R0402 UART4_CTSN_M1
1B23 GPIO1_C4_d R1816 0R R0402 UART4_TX_M1 For BT
B28 GPIO1_C5_d R1817 0R R0402 UART4_RX_M1
A26 GPIO1_C6_d R1818 0R R0402 WIFI_REG_ON_H
1C22 GPIO1_C7_d R1819 0R R0402 BT_REG_ON_H

C29 GPIO1_D0_d R1820 0R R0402 SAI2_SDO_M0
1D22 GPIO1_D1_d R1821 0R R0402 SAI2_SCLK_M0
1A24 GPIO1_D2_d R1822 0R R0402 SAI2_LRCK_M0 For BT
C28 GPIO1_D3_d R1842 0R R0402 SAI2_SDI_M0
1E21 GPIO1_D4_d R1823 0R R0402 HOST_WAKE_BT_H
1E22 GPIO1_D5_d R1824 0R R0402 SSENSOR_INT_L
R1825 NC/0R R0402 CLK1_32K_OUT_WIFI

VCCIO3
2B10 VCCIO3_VCC
C1801 100nF X5R 6.3V C0201
R1826 0.1R 1% R0603 VCCIO_WL

GPIO1_D0_d R1853 NC/0R R0402 SAI2_SDO_M0_CON
GPIO1_D1_d R1854 NC/0R R0402 SAI2_SCLK_M0_CON
GPIO1_D2_d R1855 NC/0R R0402 SAI2_LRCK_M0_CON
GPIO1_D3_d R1856 NC/0R R0402 SAI2_SDI_M0_CON

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_J(VCCIO6)

U1000J

VCCIO6 Domain
Operating Voltage=1.8V/3.3V

PWM1_CH5_M1	UART11_TX_M2	SPI4_CSN1_M0	I2C7_SCL_M3	--	HDMI_TX_CEC_M0	--	SAI4_MCLK_M2	DSM_AUD_LP_M1	GPIO4_C0_d
PWM0_CH1_M1	UART11_RX_M2	ETP_TX_HPDIN_M0	I2C7_SDA_M3	PCIE1_CLKREQN_M3	HDMI_TX_HPDIN_M0	--	--	DSM_AUD_LN_M1	GPIO4_C1_d
PWM2_CH0_M1	UART9_TX_M2	CAN0_TX_M1	I2C2_SCL_M3	--	HDMI_TX_SCL	--	--	DSM_AUD_RP_M1	GPIO4_C2_d
PWM2_CH1_M1	UART9_RX_M2	CAN0_RX_M1	I2C2_SDA_M3	--	HDMI_TX_SDA	--	--	DSM_AUD_RN_M1	GPIO4_C3_d
PWM2_CH6_M1	UART6_TX_M3	SPI4_CSN0_M0	I2C3_SCL_M3	DP_HPDIN_M0	--	--	SAI4_LRCK_M2	ISP_PRELIGHT_TRIG_M1	GPIO4_C4_d
PWM2_CH5_M1	UART6_RX_M3	SPI4_MOSI_M0	I2C3_SDA_M3	SATA1_ACTLED_M1	--	VP0_SYNC_OUT	SAI4_SDO_M2	ISP_FLASH_TRIGOUT_M1	GPIO4_C5_d
PWM2_CH2_M1	CAN1_TX_M1	SPI4_MISO_M0	I2C6_SCL_M3	SATA0_ACTLED_M1	PCIE0_CLKREQN_M3	VP1_SYNC_OUT	SAI4_SDI_M2	--	GPIO4_C6_d
PWM2_CH3_M1	CAN1_RX_M1	SPI4_CLK_M0	I2C6_SDA_M3	--	--	VP2_SYNC_OUT	SAI4_SCLK_M2	--	GPIO4_C7_d

RK3576
BGA698_16R1X17R2X1R08

AK3 GPIO4_C0_d
AK2 HDMI_TX_HPDIN_M0
AL2 GPIO4_C2_d
1AE2 GPIO4_C3_d
AL3 GPIO4_C4_d
AK1 GPIO4_C5_d
1AE1 GPIO4_C6_d
AJ1 GPIO4_C7_d

VCCIO6
2N3 VCCIO6_VCC
C1802 100nF X5R 6.3V C0201
R1836 0.1R 1% R0603 VCC_3V3_S0
R1837 NC/0.1R 1% R0603 VCC_1V8_S0
R1838 NC/0.1R 1% R0603 VCC_3V3_S3
Option: For test
Option: For test

GPIO4_C0_d R1827 0R R0402 HDMI_TX_CEC_M0
R1828 NC/0R R0402 SAI4_MCLK_M2_DCPHY
R1829 NC/0R R0402 SAI4_MCLK_M2
GPIO4_C2_d R1830 0R R0402 HDMI_TX_SCL
R1831 NC/0R R0402 MIPI_DPHY_CSI1_PWM
GPIO4_C3_d R1832 0R R0402 HDMI_TX_SDA
R1833 NC/0R R0402 MIPI_DPHY_CSI2_PWM
GPIO4_C5_d R1834 0R R0402 PWM2_CH5_M1_FAN
R1835 NC/0R R0402 MIPI_DPHY_CSI4_PWM

Default Function
Option: For test

Default turn off
Option: For test

SW1800
GPIO4_C4_d 1
GPIO4_C6_d 2
GPIO4_C7_d 3
4
8 R1839 NC/0R R0402 MIPI_DPHY_CSI3_PWM
7 R1843 NC/0R R0402 I2C6_SCL_M3_MIPI_CSI2
6 R1849 NC/0R R0402 I2C6_SDA_M3_MIPI_CSI2
5
Dial_Switch_4
SW8_5R68X5R40X2R30

Option: MIPI CAM

R1840 NC/0R R0402 SAI4_LRCK_M2
R1841 0R R0402
R1844 NC/0R R0402 SAI4_SDI_M2
R1847 0R R0402
R1850 NC/0R R0402 SAI4_SCLK_M2
R1852 0R R0402

Audio for MIPI DPHY HDMI RX

Option: Audio for MIPI DCPHY HDMI RX
SAI4_LRCK_M2_DCPHY
SAI4_SDI_M2_DCPHY
SAI4_SCLK_M2_DCPHY

Default Turn on

SW1801
GPIO4_C4_d 1
GPIO4_C6_d 2
GPIO4_C7_d 3
4
8 PCIE1_PERSTn
7
6 IRC_AIN
5 IRC_BIN
Dial_Switch_4
SW8_5R68X5R40X2R30

VCCIO6
R1845 2.2K R0402 I2C6_SCL_M3_MIPI_CSI2
R1846 2.2K R0402 I2C6_SDA_M3_MIPI_CSI2

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Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	18.RK3576-GPIO VCCIO2/3/6		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	
		Sheet:	18 of 49

RK3576_H(VCCIO4)

U1000H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

--	--	I2C4_SCL_M2	SPI4_CSN1_M3	UART8_TX_M1	--	SAI0_SDO0_M0	ETH0_RXD0_M1	SDMMC1_D0_M1	VI_CIF_D15	GPIO2_A6_d
--	--	I2C4_SDA_M2	--	UART8_RX_M1	--	SAI0_SDO1_M0	ETH0_TXCTL_M1	SDMMC1_D1_M1	VI_CIF_D14	GPIO2_A7_d
--	--	--	--	UART1_TX_M1	PDM0_SDI3_M3	SAI0_SDI0_M0	ETH0_TXD1_M1	SDMMC1_D2_M1	VI_CIF_D13	GPIO2_B0_d
--	--	--	--	UART1_RX_M1	PDM0_SDI2_M3	SAI0_SDI1_M0	ETH0_TXD0_M1	SDMMC1_D3_M1	VI_CIF_D12	GPIO2_B1_d
--	--	PCIE0_CLKREQn_M0	SPI4_CSN0_M3	UART1_CTSN_M1	PDM0_SDI1_M3	SAI0_SDI2_M0	ETH0_TXD3_M1	SDMMC1_CMD_M1	VI_CIF_D11	GPIO2_B2_d
--	--	PCIE1_CLKREQn_M0	SPI4_CLK_M3	UART1_RTSN_M1	PDM0_CLK1_M3	SAI0_SDO2_M0	ETH0_TXCLK_M1	SDMMC1_CLK_M1	VI_CIF_D10	GPIO2_B3_d
--	SATA0_ACTLED_M0	--	SPI4_MOSI_M3	UART7_CTSN_M0	PDM0_SDI0_M3	SAI0_SDI3_M0	ETH0_TXD2_M1	SDMMC1_PWREN_M1	VI_CIF_D9	GPIO2_B4_d
--	SATA1_ACTLED_M0	--	SPI4_MISO_M3	UART7_RTSN_M0	PDM0_CLK0_M3	SAI0_MCLK_M0	ETH0_RXCLK_M1	SDMMC1_DETN_M1	VI_CIF_D8	GPIO2_B5_d
--	--	I2C8_SCL_M2	UART8_RTSN_M1	UART7_TX_M0	--	SAI0_SCLK_M0	ETH0_RXD3_M1	ETH1_PTP_REFCLK_M1	VI_CIF_D7	GPIO2_B6_d
--	--	I2C8_SDA_M2	UART8_CTSN_M1	UART7_RX_M0	--	SAI0_LRCK_M0	ETH0_RXD2_M1	--	VI_CIF_D6	GPIO2_B7_d
PWM1_CH0_M2	--	--	--	UART9_RX_M0	PDM1_SDI1_M0	--	ETH0_PTP_REFCLK_M1	ETH1_RXD2_M0	VI_CIF_D5	GPIO2_C0_d
PWM1_CH1_M2	--	--	SPI1_CSN1_M1	UART9_TX_M0	PDM1_CLK1_M0	SAI2_MCLK_M1	ETH0_PPSCLK_M1	ETH1_RXD3_M0	VI_CIF_D4	GPIO2_C1_d
PWM1_CH2_M2	--	--	SPI1_MOSI_M1	UART11_CTSN_M1	PDM1_SDI2_M0	SAI2_SCLK_M1	ETH0_PPSTRIG_M1	ETH1_RXCLK_M0	VI_CIF_D3	GPIO2_C2_d
PWM0_CH0_M2	--	--	SPI1_MISO_M1	UART11_RTSN_M1	PDM1_SDI3_M0	SAI2_LRCK_M1	--	ETH1_RXD2_M0	VI_CIF_D2	GPIO2_C3_d
PWM1_CH3_M2	--	--	SPI1_CSN0_M1	UART11_TX_M1	PDM1_SDI0_M0	SAI2_SDO_M1	--	ETH1_RXD3_M0	VI_CIF_D1	GPIO2_C4_d
PWM0_CH3_M2	--	--	SPI1_CLK_M1	UART11_RX_M1	PDM1_CLK0_M0	SAI2_SDI_M1	--	ETH1_RXCLK_M0	VI_CIF_D0	GPIO2_C5_d
PWM1_CH4_M2	--	I2C5_SCL_M2	--	UART4_CTSN_M0	--	SAI4_SCLK_M3	--	ETH1_TXD0_M0	--	GPIO2_C6_d
PWM0_CH1_M2	--	I2C5_SDA_M2	--	UART4_RTSN_M0	--	SAI4_LRCK_M3	--	ETH1_TXD1_M0	--	GPIO2_C7_d
PWM2_CH0_M2	--	I2C6_SCL_M2	--	UART4_TX_M0	--	SAI4_SDI_M3	--	ETH1_TXCTL_M0	--	GPIO2_D0_d
PWM2_CH1_M2	--	I2C6_SDA_M2	--	UART4_RX_M0	--	SAI4_SDO_M3	--	ETH1_RXD0_M0	--	GPIO2_D1_d
PWM2_CH2_M2	I3C1_SCL_M0	--	--	UART6_TX_M1	--	SAI4_MCLK_M3	--	ETH1_RXD1_M0	CAM_CLKU_OUT_M1	GPIO2_D2_d
PWM2_CH3_M2	I3C1_SDA_M0	--	--	UART6_RX_M1	--	--	--	ETH1_RXCTL_M0	--	GPIO2_D3_d
PWM2_CH4_M2	--	I2C9_SDA_M2	--	UART6_RTSN_M1	--	--	--	ETH1_MDC_M0	ISP_PRELIGHT_TRIG_M0	GPIO2_D4_d
PWM2_CH5_M2	--	I2C9_SCL_M2	--	UART6_CTSN_M1	--	--	--	ETH1_MDIO_M0	ISP_FLASH_TRIGOUT_M0	GPIO2_D5_d
PWM2_CH6_M2	I3C1_SDA_PU_M0	--	--	UART9_RTSN_M0	SPDIF_RX0_M2	SAI3_MCLK_M2	ETH0_MCLK_M1	ETH_CLK1_25M_OUT_M0	CAM_CLKL_OUT_M1	GPIO2_D6_d
PWM2_CH7_M2	--	--	SPI3_CSN1_M0	UART9_CTSN_M0	SPDIF_TX0_M2	SAI3_SDO3_M0	ETH_CLKO_25M_OUT_M1	ETH1_MCLK_M0	CAM_CLKZ_OUT_M1	GPIO2_D7_d
--	--	I2C7_SCL_M1	SPI3_CLK_M0	UART3_TX_M0	--	SAI3_SCLK_M2	ETH0_MDIO_M1	--	VI_CIF_HREF	GPIO3_A0_d
--	--	I2C7_SDA_M1	SPI3_MOSI_M0	UART3_RX_M0	--	SAI3_LRCK_M2	ETH0_MDC_M1	ETH1_PPSTRIG_M0	VI_CIF_VSYNC	GPIO3_A1_d
--	MIPI_TE_M1	CAN1_TX_M3	SPI3_MISO_M0	UART3_CTSN_M0	SPDIF_RX1_M1	SAI3_SDO_M2	ETH0_RXCTL_M1	ETH1_PPSCLK_M0	VI_CIF_CLKO	GPIO3_A2_d
--	--	CAN1_RX_M3	SPI3_CSN0_M0	UART3_RTSN_M0	SPDIF_TX1_M1	SAI3_SDI_M2	ETH0_RXD1_M1	ETH1_PTP_REFCLK_M0	VI_CIF_CLKI	GPIO3_A3_d

VCCIO4_VCC

RK3576

BGA698_16R1X17R2X1R08

Option: For test

GPIO2_D6_d R1901 NC/0R R0402 MIPI_DPHY_CSI2_CAM_CLKOUT

GPIO2_D7_d R1903 NC/0R R0402 GMAC1_MCLKINOUT_M0

GPIO3_A2_d R1905 NC/0R R0402 MIPI_DPHY_CSI4_CAM_CLKOUT

R1906 NC/0R R0402 SPDIF_RX1_M1_DPHY

R1948 NC/0R R0402 SPDIF_RX1_M1_DCPHY

R1950 NC/0R R0402 PCIE1_PRSNT_L

B22 TYPEC_DPTX_AUX_PUPDCTL1

B20 TYPEC_DPTX_AUX_PUPDCTL2

B19 GPIO2_B0_d R1907 0R R0402 HDMI_TX_ON_H

1A18 GPIO2_B1_d R1908 0R R0402 SPK_CTL_H

1A17 PCIE0_CLKREQn_M0

1B16 PCIE1_CLKREQn_M0

A19 PCIE0_PERSTn

1C18 GMAC0_RSTn

A21 I2C8_SCL_M2_MIPI_CSI3

B21 I2C8_SDA_M2_MIPI_CSI3

VCCIO4

R1909 4.7K R0402 I2C8_SCL_M2_MIPI_CSI3

R1910 4.7K R0402 I2C8_SDA_M2_MIPI_CSI3

A17 GMAC1_RXD2_M0

1A15 GMAC1_RXD3_M0

1D15 GMAC1_RXCLK_M0

A15 GPIO2_C3_d R1912 0R R0402 GMAC1_TXD2_M0

1A13 GPIO2_C4_d R1913 0R R0402 GMAC1_TXD3_M0

1C15 GPIO2_C5_d R1914 0R R0402 GMAC1_TXCLK_M0

1A14 GPIO2_C6_d R1915 0R R0402 GMAC1_TXD0_M0

B15 GPIO2_C7_d R1918 0R R0402 GMAC1_TXD1_M0

VCCIO4

R1916 2.2K R0402 I2C7_SCL_M1_Sensor

R1917 2.2K R0402 I2C7_SDA_M1_Sensor

B16 GPIO2_D0_d R1919 0R R0402 GMAC1_TXCTL_M0

1A16 GMAC1_RXD0_M0

B17 GMAC1_RXD1_M0

B18 GMAC1_RXCTL_M0

1B13 GPIO2_D4_d R1920 0R R0402 GMAC1_MDC_M0

1B15 GPIO2_D5_d R1921 0R R0402 GMAC1_MDIO_M0

1D18 R1911 0R R0402 GPIO2_D6_d R1900 0R R0402 ETH_CLK1_25M_OUT_M0

1E15 R1949 0R R0402 GPIO2_D7_d R1902 0R R0402 MIPI_DPHY_CSI2_CAM_CLKOUT

1D16 I2C7_SCL_M1_Sensor

1B18 I2C7_SDA_M1_Sensor

1A20 GPIO3_A2_d R1904 0R R0402 MIPI_TE_M1_GPIO3_A2

1A19 GMAC1_RSTn

VCCIO4

2A7

C1900 NC/100nF X5R 6.3V C0201

C1901 1uF X5R 6.3V C0201

R1922 0.1R 1% R0603 VCC_3V3_S0

R1923 NC/0.1R 1% R0603 VCC_1V8_S0

Option: For test

RK3576_I(VCCIO5)

U1000I

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH0_M3	--	SPI2_CLK_M2	UART1_CTSN_M2	FLEXBUS0_CSN_M0	--	FLEXBUS1_D11	DSMC_RDYN	SAI4_SDI_M1	ETH_CLK0_25M_OUT_M0	VO_EBC_SDSHR	VO_LCDC_D23	GPIO3_A4_d
PWM1_CH1_M3	--	SPI2_CSN1_M2	UART1_RTSN_M2	--	--	FLEXBUS0_D7	DSMC_DATA15	PDM1_SDI3_M2	ETH0_MDIO_M0	VO_EBC_GDSF	VO_LCDC_D22	GPIO3_A5_d
PWM1_CH2_M3	--	UART10_CTSN_M0	UART1_RX_M2	--	--	FLEXBUS0_D6	DSMC_DATA14	PDM1_SDI2_M2	ETH0_MDC_M0	VO_EBC_GDOE	VO_LCDC_D21	GPIO3_A6_d
--	--	UART10_RTSN_M0	UART1_TX_M2	--	--	FLEXBUS0_D5	DSMC_DATA13	PDM1_CLK1_M2	ETH0_RXCTL_M0	VO_EBC_VCOM	VO_LCDC_D20	GPIO3_A7_d
PWM0_CH0_M3	--	SPI2_MOSI_M2	UART10_RX_M0	--	--	FLEXBUS0_D8	DSMC_CSN1	SAI4_MCLK_M1	ETH0_MCLK_M0	VO_EBC_SDCE3	VO_LCDC_D19	GPIO3_B0_d
PWM1_CH3_M3	--	SPI4_CSN0_M1	UART10_TX_M0	--	--	FLEXBUS0_D4	DSMC_DATA12	PDM1_CLK0_M2	ETH0_RXD1_M0	VO_EBC_SDCE2	VO_LCDC_D18	GPIO3_B1_d
--	I2C8_SDA_M3	--	UART9_RX_M1	--	--	FLEXBUS0_D3	DSMC_DATA11	PDM1_SDI1_M2	ETH0_RXD0_M0	VO_EBC_SDCE1	VO_LCDC_D17	GPIO3_B2_d
--	I2C8_SCL_M3	--	UART9_TX_M1	--	--	FLEXBUS0_D2	DSMC_DATA10	PDM1_SDI0_M2	ETH0_TXCTL_M0	VO_EBC_SDCE0	VO_LCDC_D16	GPIO3_B3_d
PWM1_CH4_M3	--	--	UART9_RTSN_M1	--	--	FLEXBUS0_D1	DSMC_DATA9	SPDIF_RX1_M0	ETH0_TXD1_M0	VO_EBC_SDDO15	VO_LCDC_D15	GPIO3_B4_d
PWM1_CH5_M3	--	--	UART9_CTSN_M1	--	--	FLEXBUS0_D0	DSMC_DATA8	SPDIF_TX1_M0	ETH0_TXD0_M0	VO_EBC_SDDO14	VO_LCDC_D14	GPIO3_B5_d
PWM0_CH1_M3	--	SPI3_CSN0_M1	--	--	--	FLEXBUS0_CLK	DSMC_DQS1	--	ETH0_TXCLK_M0	VO_EBC_SDDO13	VO_LCDC_D13	GPIO3_B6_d
--	I2C4_SDA_M3	UART3_CTSN_M1	UART2_RX_M2	FLEXBUS1_CSN_M0	--	FLEXBUS1_D10	DSMC_DQS0	SAI1_SDI0_M1	ETH0_PPSTRIG_M0	VO_EBC_SDDO12	VO_LCDC_D12	GPIO3_B7_d
--	I2C4_SCL_M3	UART3_RTSN_M1	UART2_TX_M2	--	--	FLEXBUS1_D9	DSMC_DATA7	SAI1_SDO3_M1	ETH0_PPSCLK_M0	VO_EBC_SDDO11	VO_LCDC_D11	GPIO3_C0_d
CAN0_RX_M3	I2C5_SDA_M3	SPI2_MISO_M2	UART11_RX_M0	--	--	FLEXBUS1_D8	DSMC_DATA6	SAI1_SDO1_M1	ETH0_PTP_REFCLK_M0	VO_EBC_SDDO10	VO_LCDC_D10	GPIO3_C1_d
PWM2_CH0_M3	I2C9_SCL_M3	SPI4_MISO_M1	UART11_RTSN_M0	--	--	FLEXBUS1_D9	DSMC_INT1	SAI2_SCLK_M2	ETH0_RXD3_M0	VO_EBC_SDDO9	VO_LCDC_D9	GPIO3_C2_d
PWM2_CH1_M3	I2C9_SDA_M3	SPI4_MOSI_M1	UART11_CTSN_M0	FLEXBUS0_CSN_M2	--	FLEXBUS1_D10	DSMC_INT3	SAI2_LRCK_M2	ETH0_TXD2_M0	VO_EBC_SDDO8	VO_LCDC_D8	GPIO3_C3_d
CAN0_TX_M3	I2C5_SCL_M3	SPI2_CSN0_M2	UART11_TX_M0	--	--	FLEXBUS1_D7	DSMC_DATA5	SAI1_SDO1_M1	--	VO_EBC_SDDO7	VO_LCDC_D7	GPIO3_C4_d
PWM2_CH2_M3	--	SPI1_MISO_M2	UART8_RX_M0	--	--	FLEXBUS1_D6	DSMC_DATA4	SAI1_SDO0_M1	--	VO_EBC_SDDO6	VO_LCDC_D6	GPIO3_C5_d
--	--	SPI1_MOSI_M2	UART8_TX_M0	--	--	FLEXBUS1_D5	DSMC_DATA3	SAI1_LRCK_M1	--	VO_EBC_SDDO5	VO_LCDC_D5	GPIO3_C6_d
--	--	SPI1_CLK_M2	UART8_RTSN_M0	--	--	FLEXBUS1_D4	DSMC_DATA2	SAI1_SCLK_M1	--	VO_EBC_SDDO4	VO_LCDC_D4	GPIO3_C7_d
PWM2_CH3_M3	--	SPI1_CSN0_M2	UART8_CTSN_M0	--	--	FLEXBUS1_D3	DSMC_DATA1	SAI1_MCLK_M1	--	VO_EBC_SDDO3	VO_LCDC_D3	GPIO3_D0_d
--	I3C1_SDA_PU_M2	SPI4_CLK_M1	--	FLEXBUS1_CSN_M2	--	FLEXBUS1_D2	DSMC_CSN2	SAI2_MCLK_M2	ETH0_RXCLK_M0	VO_EBC_SDDO2	VO_LCDC_D2	GPIO3_D1_d
PWM2_CH4_M3	I3C1_SDA_M2	SPI4_CSN1_M1	UART2_RTSN_M2	FLEXBUS0_CSN_M3	FLEXBUS1_D15_M0	FLEXBUS1_D12	DSMC_CSN3	SAI2_SDI_M2	ETH0_RXD3_M0	VO_EBC_SDDO1	VO_LCDC_D1	GPIO3_D2_d
PWM2_CH5_M3	I3C1_SCL_M2	--	UART2_CTSN_M2	--	--	FLEXBUS1_D2	DSMC_CSN0	SAI2_SDO_M2	ETH0_RXD2_M0	VO_EBC_SDDO0	VO_LCDC_D0	GPIO3_D3_d
--	I2C3_SCL_M2	SPI3_CLK_M1	UART5_RX_M0	--	--	FLEXBUS1_D1	DSMC_DATA0	SAI1_SDI1_M1	--	VO_EBC_SDLE	VO_LCDC_DEN	GPIO3_D4_d
--	I2C3_SDA_M2	SPI3_MISO_M1	UART5_TX_M0	--	--	FLEXBUS1_D0	DSMC_CLKF	SAI1_SDI2_M1	--	VO_EBC_GDCLK	VO_LCDC_HSYNC	GPIO3_D5_d
PWM2_CH6_M3	--	SPI3_MOSI_M1	UART5_CTSN_M0	--	--	FLEXBUS1_CLK	DSMC_CLKN	SAI1_SDI3_M1	--	VO_EBC_SDCLK	VO_LCDC_VSYNC	GPIO3_D6_d
PWM2_CH7_M3	--	SPI3_CSN1_M1	UART5_RTSN_M0	FLEXBUS1_CSN_M1	FLEXBUS1_D12_M0	FLEXBUS1_D15_M0	DSMC_RESETN	SAI4_SCLK_M1	CAM_CLK0_OUT_M0	VO_EBC_SDOE	VO_LCDC_CLK	GPIO3_D7_d
MIPI_TE_M2	I2C7_SCL_M2	SPI1_CSN1_M2	UART3_TX_M1	FLEXBUS1_CSN_M3	FLEXBUS1_D14_M0	FLEXBUS0_D13_M0	DSMC_INT0	SAI4_LRCK_M1	CAM_CLK1_OUT_M0	SPDIF_RX0_M1	--	GPIO4_A0_d
--	I2C7_SDA_M2	--	UART3_RX_M1	FLEXBUS0_CSN_M1	FLEXBUS1_D13_M0	FLEXBUS0_D14_M0	DSMC_INT2	SAI4_SDO_M1	CAM_CLK2_OUT_M0	SPDIF_TX0_M1	VO_POST_EMPTY	GPIO4_A1_d

RK3576

BGA698_16R1X17R2X1R08

Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

1D13 GPIO3_A4_d

A9 GPIO3_A5_d R1924 0R R0402 GMAC0_MDIO_M0

1A7 GPIO3_A6_d R1925 0R R0402 GMAC0_MDC_M0

B13 GMAC0_RXCTL_M0

VCCIO5

R1926 2.2K R0402 I2C4_SDA_M3_MIPI_CSI0

R1927 2.2K R0402 I2C4_SCL_M3_MIPI_CSI0

B14 GPIO3_B0_d

1A11 GMAC0_RXD1_M0

A13 GMAC0_RXD0_M0

A11 GPIO3_B3_d R1928 0R R0402 GMAC0_TXCTL_M0

B10 GPIO3_B4_d R1929 0R R0402 GMAC0_TXD1_M0

1A9 GPIO3_B5_d R1930 0R R0402 GMAC0_TXD0_M0

B11 GPIO3_B6_d R1931 0R R0402 GMAC0_TXCLK_M0

1D12 I2C4_SDA_M3_MIPI_CSI0

1E9 I2C4_SCL_M3_MIPI_CSI0

1B10 I2C5_SDA_M3_MIPI_CSI1

B9 GPIO3_C2_d R1932 0R R0402 GMAC0_TXD3_M0

1A8 GPIO3_C3_d R1933 0R R0402 GMAC0_TXD2_M0

1D9 I2C5_SCL_M3_MIPI_CSI1

1B9 GPIO3_C5_d

1D7 MIPI_DPHY_CSI0_PWREN_H

1C7 MIPI_DPHY_CSI0_PDN_H

VCCIO5

R1934 2.2K R0402 I2C5_SDA_M3_MIPI_CSI1

R1935 2.2K R0402 I2C5_SCL_M3_MIPI_CSI1

1C12 MIPI_DPHY_CSI1_PDN_H

1A12 GMAC0_RXCLK_M0

1A10 GMAC0_RXD3_M0

B12 GMAC0_RXD2_M0

1E12 GPIO3_D4_d

1D10 MIPI_DPHY_CSI3_PDN_H

1C10 GPIO3_D6_d

1E7 R1951 0R R0402 MIPI_DPHY_CSI0_CAM_CLKOUT

1B12 R1952 0R R0402 MIPI_DPHY_CSI1_CAM_CLKOUT

1B7 R1953 0R R0402 MIPI_DPHY_CSI3_CAM_CLKOUT

VCCIO5_VCC_0

VCCIO5_VCC_1

VCCIO5

2A4

2A5

C1902 NC/100nF X5R 6.3V C0201

C1903 1uF X5R 6.3V C0201

R1936 NC/0.1R 1% R0603 VCC_3V3_S0

R1937 0.1R 1% R0603 VCC_1V8_S0

Option: For test

GPIO3_A4_d R1938 0R R0402 NC/0R R0402 R1940

GPIO3_B0_d R1942 0R R0402 NC/0R R0402 R1944

GPIO3_C5_d R1946 0R R0402 NC/0R R0402 R1947

Default Function

ETH_CLK0_25M_OUT_M0

MIPI_DPHY_CSI1/2_PWREN_H

MIPI_DPHY_CSI3/4_PWREN_H

Option: For test

MIPI_DPHY_CSI1/2_PWREN_H

MIPI_DPHY_CSI0_PWM

Option: For test

GMAC0_MCLKINOUT_M0

GPIO3_D4_d R1939 0R R0402 NC/0R R0402 R1941

GPIO3_D6_d R1943 0R R0402 NC/0R R0402 R1945

Default Function

PCIE1_PWREN_H

HP_CTL_H

Option: For test

MIPI_DPHY_CSI2_PDN_H

MIPI_DPHY_CSI4_PDN_H

Option: For test

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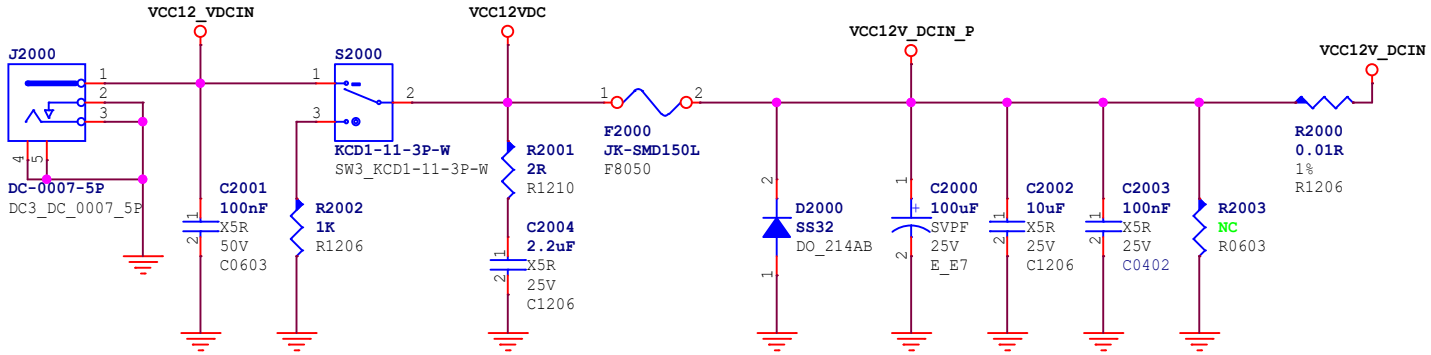
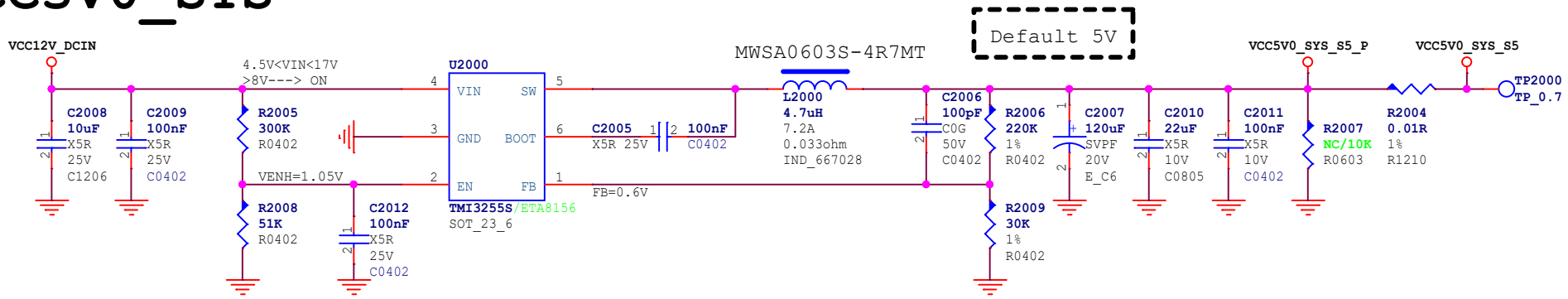
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	19.RK3576-GPIO VCCIO4/5		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	
		Sheet:	19 of 49

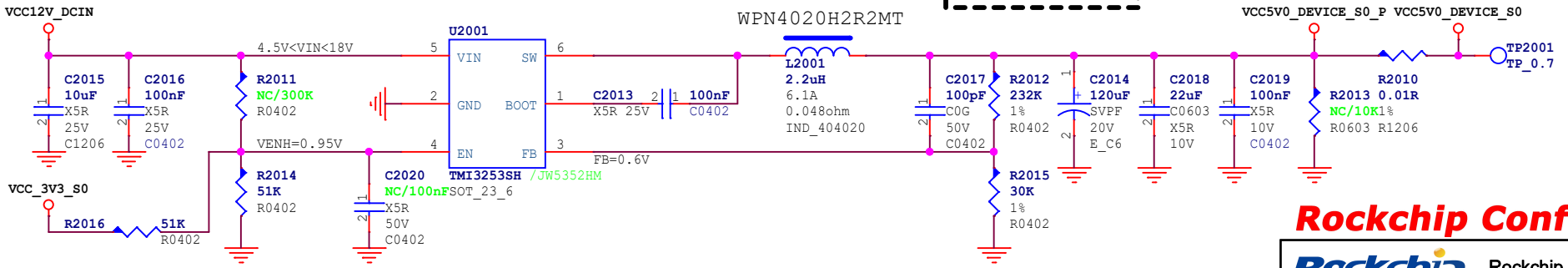
12V/3A DCIN



VCC5V0_SYS

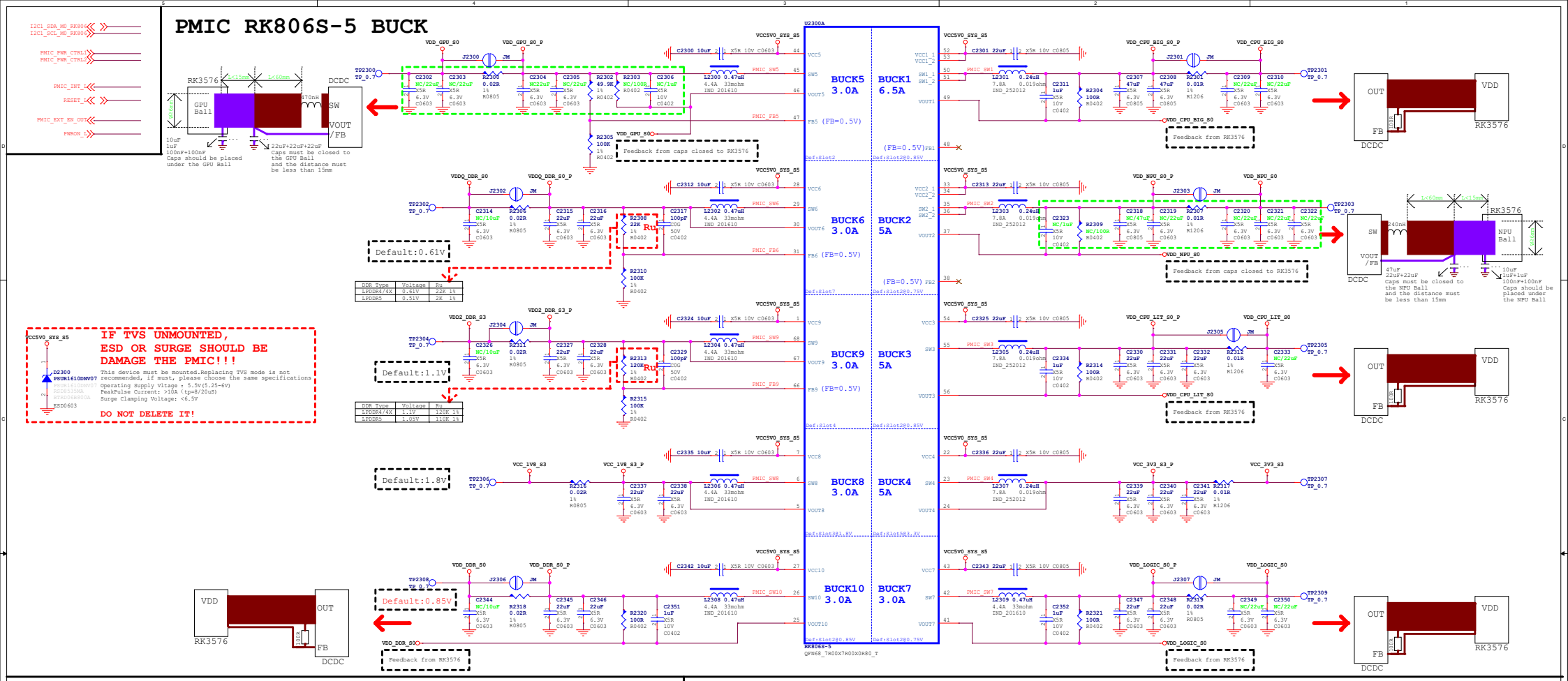


VCC5V0_DEVICE



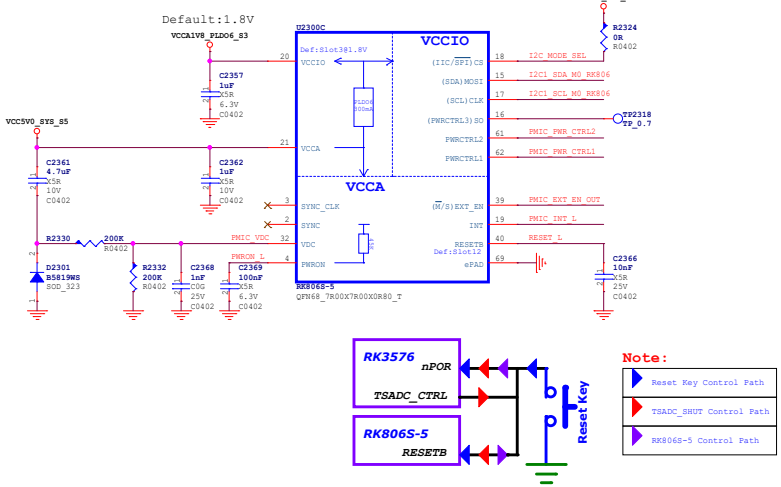
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	20.Power-DC IN		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang / Reviewed by:	Sheet:	20 of 49

PMIC RK806S-5 BUCK

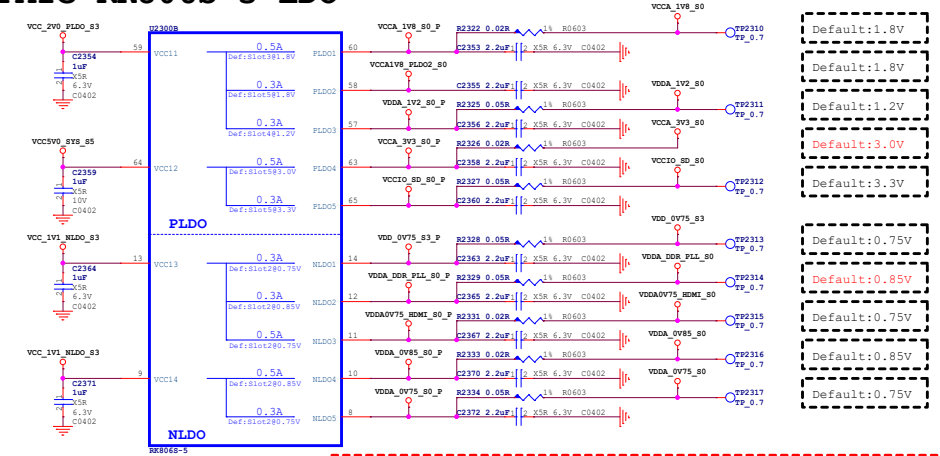


PMIC RK806S-5 Managerment

Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND



PMIC RK806S-5 LDO



Note:
The RK806 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

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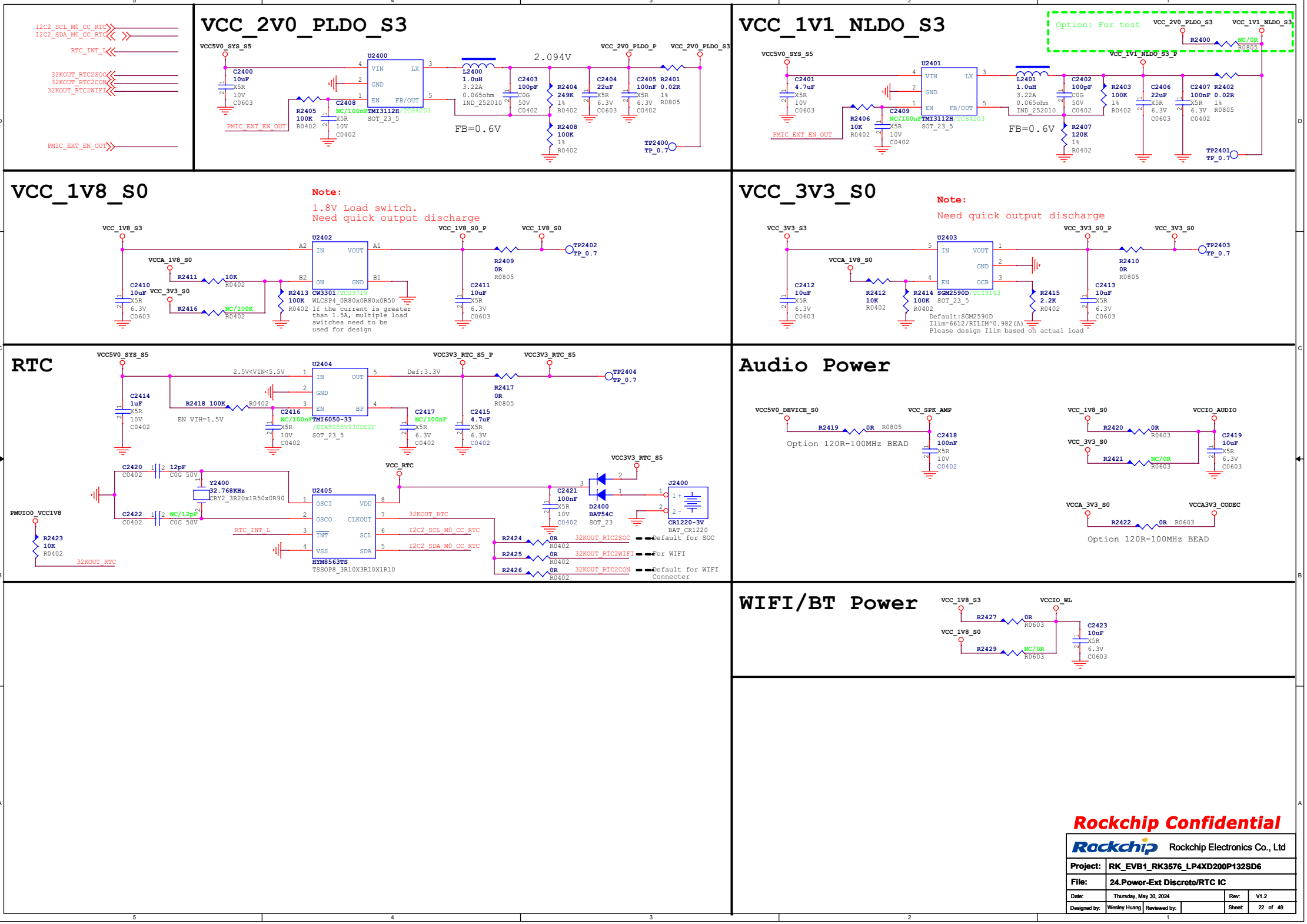
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	23.Power-PMIC RK806S-5		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by: Wesley Huang	Reviewed by:	Sheet:	21 of 49


I2C2_SCL_M0_CC_RTC
I2C2_SDA_M0_CC_RTC
RTC_INT_L
32KOUT_RTC2SOC
32KOUT_RTC2CON
32KOUT_RTC2WIFI
PMIC_EXT_EN_OUT
VCC_2V0_PLDO_S3
VCC5V0_SYS_S5
U2400
VIN
LX
GND
EN
FB/OUT
C2400 10uF X5R 10V C0603
C2408 NC/100nF X5R 10V C0402
R2405 100K R0402
TMI3112H/TCS4203
SOT_23_5
L2400 1.0uH 3.22A 0.065ohm IND_252010
2.094V
C2403 100pF C0G 50V C0402
R2404 249K 1% R0402
C2404 22uF X5R 6.3V C0603
C2405 100nF X5R 6.3V C0402
R2401 0.02R 1% R0805
R2408 100K 1% R0402
FB=0.6V
VCC_2V0_PLDO_P
VCC_2V0_PLDO_S3
TP2400 TP_0.7
VCC_1V1_NLDO_S3
Option: For test
R2400 NC/0R R0805
VCC_1V1_NLDO_S3_P
U2401
C2401 4.7uF X5R 10V C0603
C2409 NC/100nF X5R 10V C0402
R2406 10K R0402
TMI3112H/TCS4203
SOT_23_5
L2401 1.0uH 3.22A 0.065ohm IND_252010
C2402 100pF C0G 50V C0402
R2403 100K 1% R0402
C2406 22uF X5R 6.3V C0603
C2407 100nF X5R 6.3V C0402
R2402 0.02R 1% R0805
R2407 120K 1% R0402
FB=0.6V
TP2401 TP_0.7
VCC_1V8_S0
Note:
1.8V Load switch.
Need quick output discharge
VCC_1V8_S3
U2402
VCCA_1V8_S0
R2411 10K R0402
C2410 10uF X5R 6.3V C0603
VCC_3V3_S0
R2416 NC/100K R0402
R2413 100K R0402
CW3301/TCS9719
WLCSP4_0R80x0R80x0R50
If the current is greater than 1.5A, multiple load switches need to be used for design
VCC_1V8_S0_P
VCC_1V8_S0
R2409 0R R0805
C2411 10uF X5R 6.3V C0603
TP2402 TP_0.7
VCC_3V3_S0
Note:
Need quick output discharge
VCC_3V3_S3
U2403
VCCA_1V8_S0
C2412 10uF X5R 6.3V C0603
R2412 10K R0402
R2414 100K R0402
SGM2590D/TCS9163
SOT_23_5
Default:SGM2590D
Ilim=6612/RILIM^0.982(A)
Please design Ilim based on actual load
R2415 2.2K R0402
VCC_3V3_S0_P
VCC_3V3_S0
R2410 0R R0805
C2413 10uF X5R 6.3V C0603
TP2403 TP_0.7
RTC
VCC5V0_SYS_S5
U2404
2.5V<VIN<5.5V
C2414 1uF X5R 10V C0402
R2418 100K R0402
EN VIH=1.5V
C2416 NC/100nF X5R 10V C0402
TMI6050-33
/ETA5055V330DS2F
SOT_23_5
Def:3.3V
C2417 NC/100nF X5R 6.3V C0402
C2415 4.7uF X5R 6.3V C0402
VCC3V3_RTC_S5_P
VCC3V3_RTC_S5
R2417 0R R0805
TP2404 TP_0.7
VCC_RTC
VCC3V3_RTC_S5
C2420 12pF C0G 50V C0402
C2422 NC/12pF C0G 50V C0402
Y2400 32.768KHz CRY2_3R20x1R50x0R90
U2405
OSCI
OSCO
INT
VDD
CLKOUT
SCL
SDA
VSS
HYM8563TS
TSSOP8_3R10X3R10X1R10
C2421 100nF X5R 10V C0402
D2400 BAT54C SOT_23
J2400
CR1220-3V
BAT_CR1220
PMUIO0_VCC1V8
R2423 10K R0402
32KOUT_RTC
RTC_INT_L
I2C2_SCL_M0_CC_RTC
I2C2_SDA_M0_CC_RTC
R2424 0R R0402 32KOUT_RTC2SOC Default for SOC
R2425 0R R0402 32KOUT_RTC2WIFI For WIFI
R2426 0R R0402 32KOUT_RTC2CON Default for WIFI Connecter
Audio Power
VCC5V0_DEVICE_S0
R2419 0R R0805
Option 120R-100MHz BEAD
VCC_SPK_AMP
C2418 100nF X5R 10V C0402
VCC_1V8_S0
VCCIO_AUDIO
R2420 0R R0603
C2419 10uF X5R 6.3V C0603
VCC_3V3_S0
R2421 NC/0R R0603
VCCA_3V3_S0
VCCA3V3_CODEC
R2422 0R R0603
Option 120R-100MHz BEAD
WIFI/BT Power
VCC_1V8_S3
VCCIO_WL
R2427 0R R0603
VCC_1V8_S0
R2429 NC/0R R0603
C2423 10uF X5R 6.3V C0603
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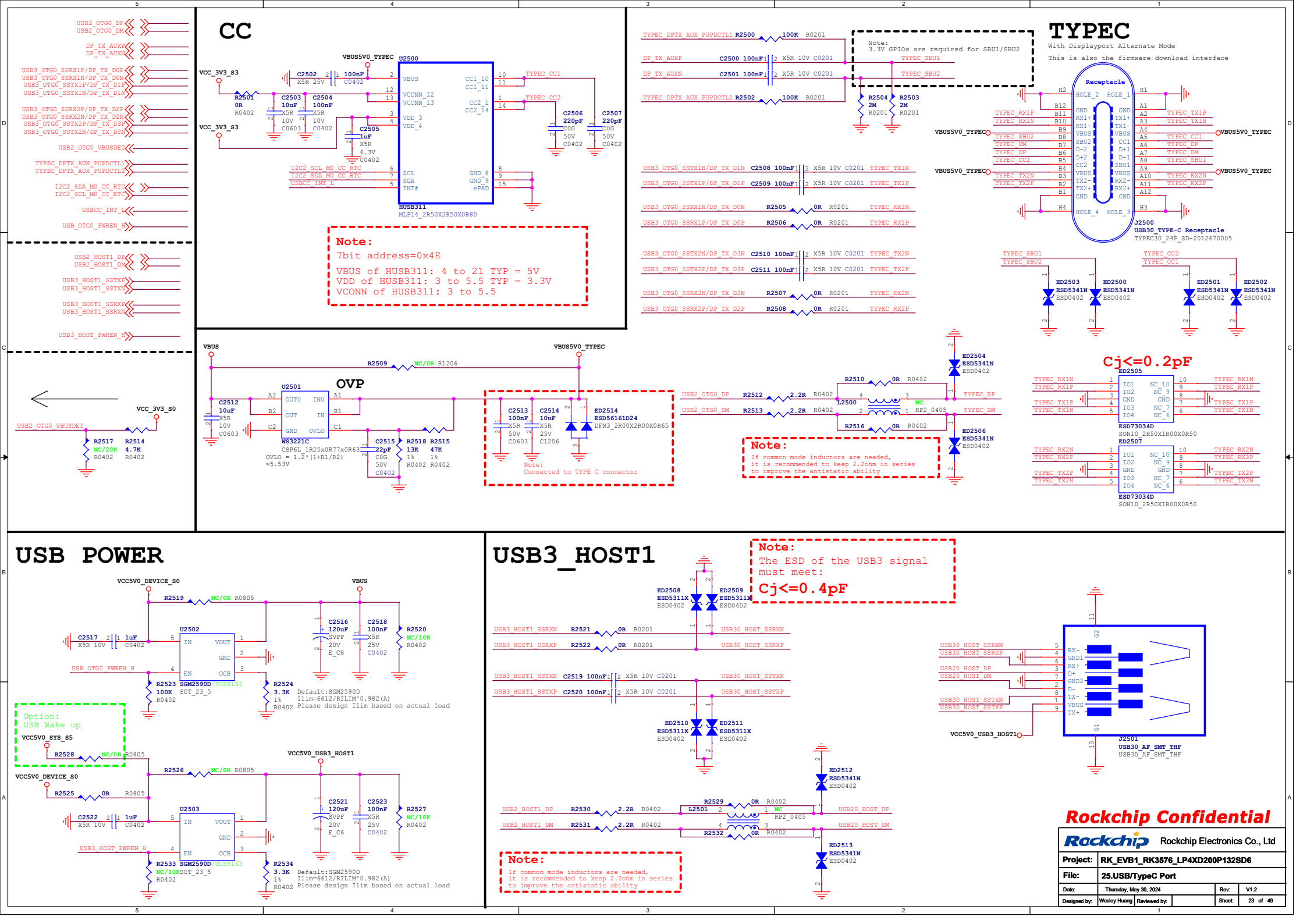
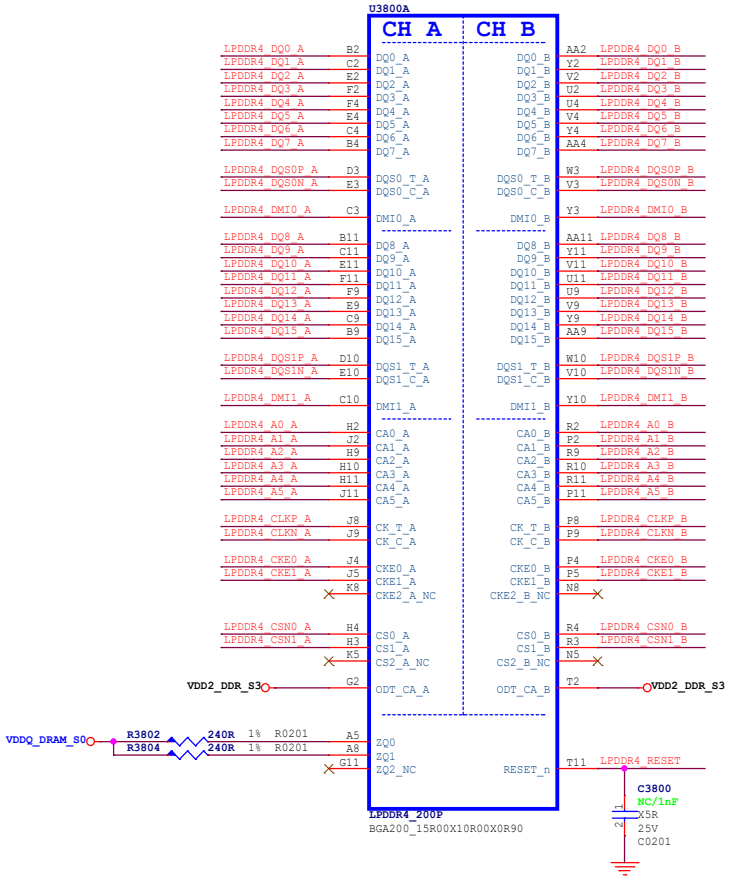
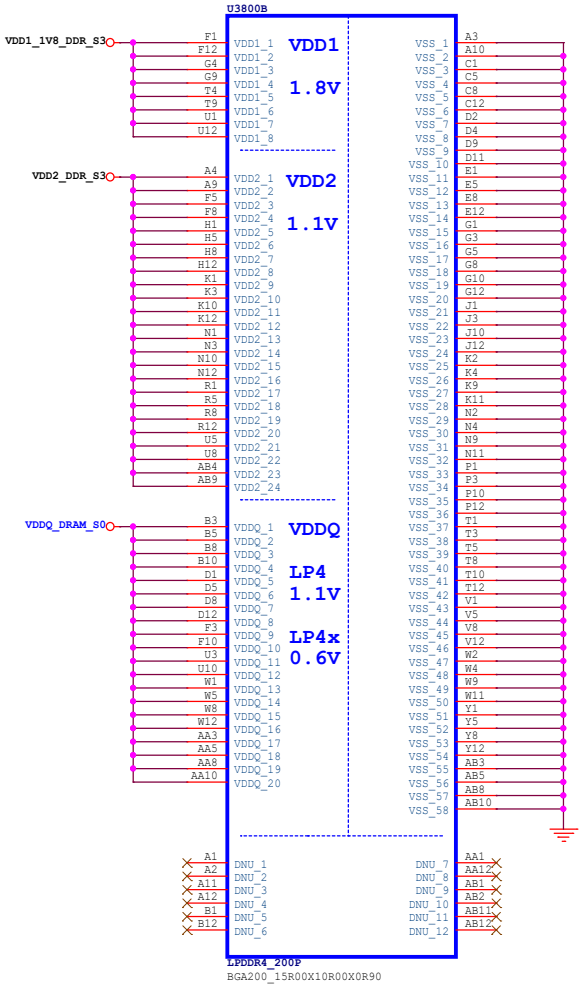
Rockchip Electronics Co., Ltd
Project: RK_EVB1_RK3576_LP4XD200P132SD6
File: 24.Power-Ext Discrete/RTC IC
Date: Thursday, May 30, 2024
Rev: V1.2
Designed by: Wesley Huang
Reviewed by:
Sheet: 22 of 49


CC
TYPEC
With Displayport Alternate Mode
This is also the firmware download interface
Note:
7bit address=0x4E
VBUS of HUSB311: 4 to 21 TYP = 5V
VDD of HUSB311: 3 to 5.5 TYP = 3.3V
VCONN of HUSB311: 3 to 5.5
Note:
3.3V GPIOs are required for SBU1/SBU2
OVP
Cj<=0.2pF
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
Note:
Connected to TYPE C connector
USB_POWER
USB3_HOST1
Note:
The ESD of the USB3 signal
must meet:
Cj<=0.4pF
Option:
USB Wake up
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK_EVB1_RK3576_LP4XD200P132SD6
File: 25.USB/TypeC Port
Date: Thursday, May 30, 2024
Rev: V1.2
Designed by: Wesley Huang
Reviewed by:
Sheet: 23 of 49

LPDDR4/4X





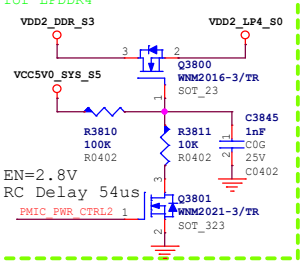
Note:

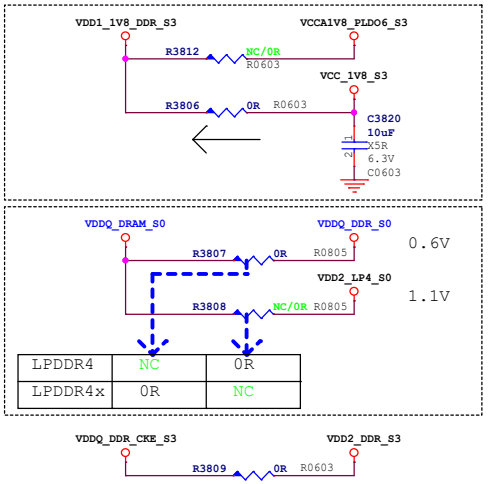
Sequence:VDD1-VDD2-VDDQ

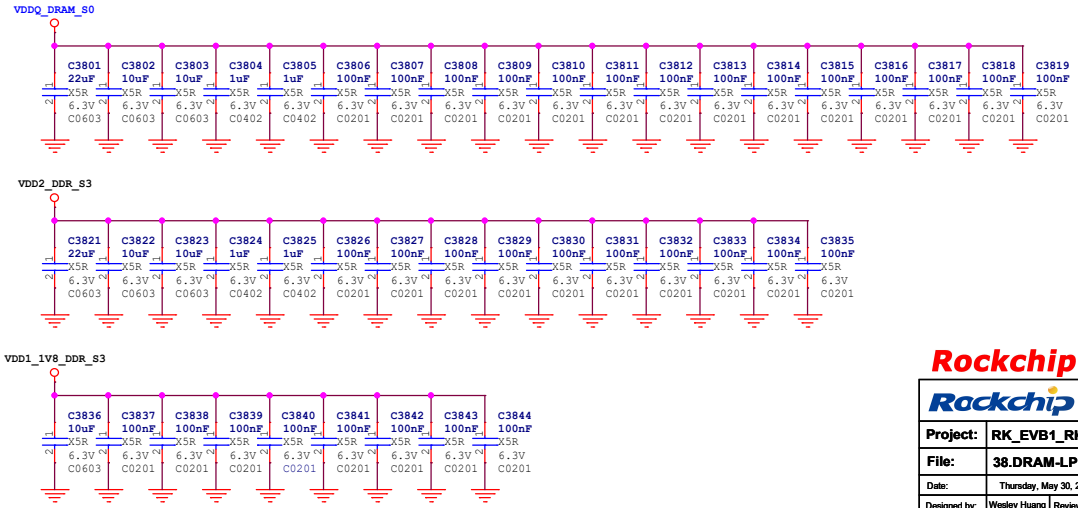
	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65

Option

Power down VDDQ during standby for LPDDR4







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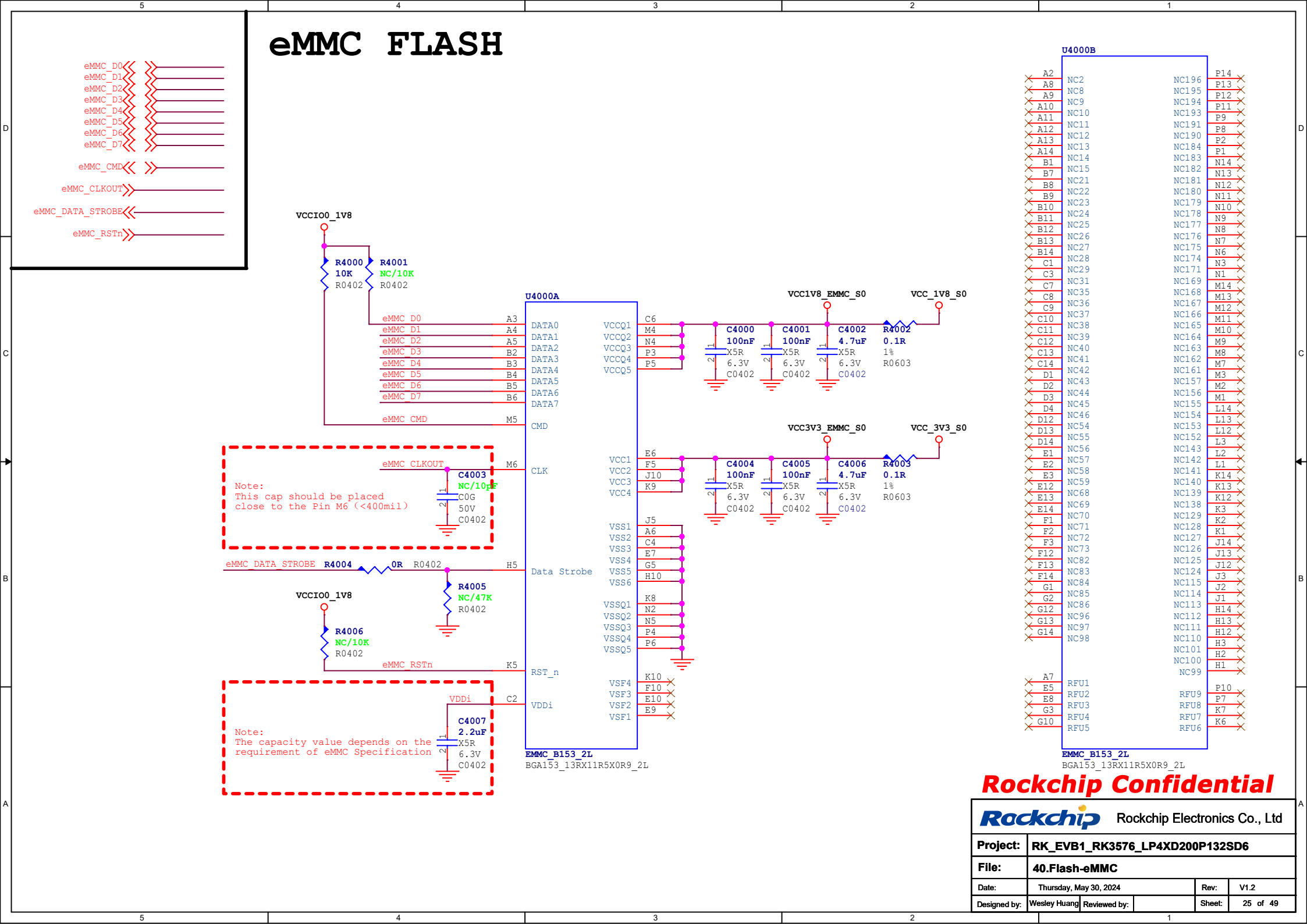
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_EVB1_RK3576_LP4XD200P132SD6
File:	38.DRAM-LPDDR4X_1X32bit_200P
Date:	Thursday, May 30, 2024
Rev:	V1.2
Designed by:	Wesley Huang
Reviewed by:	
Sheet:	24 of 49

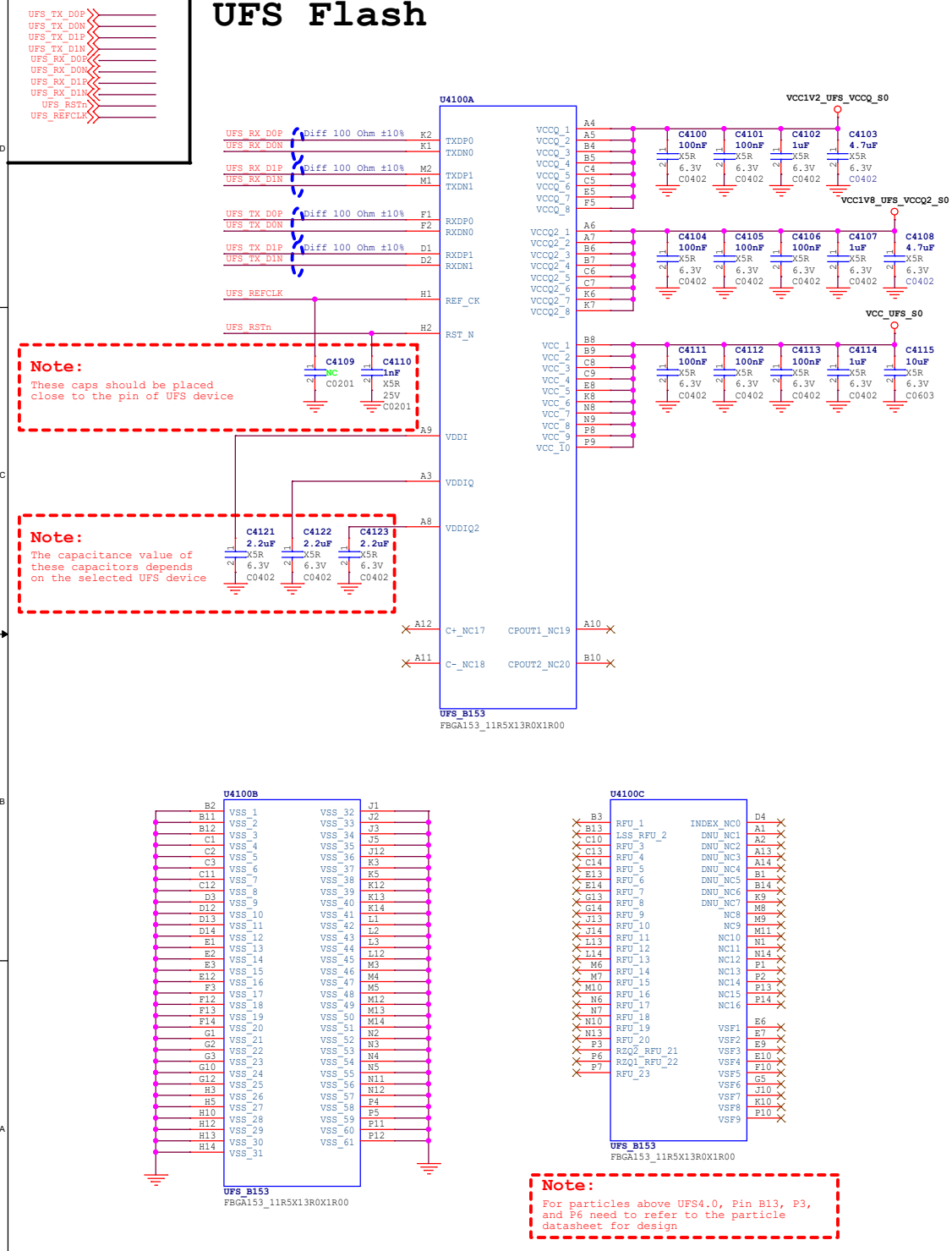
eMMC FLASH



Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	40.Flash-eMMC		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by: Wesley Huang	Reviewed by:	Sheet:	25 of 49

UFS Flash



Note:
These caps should be placed close to the pin of UFS device

Note:
The capacitance value of these capacitors depends on the selected UFS device

Note:
For particles above UFS4.0, Pin B13, P3, and P6 need to refer to the particle datasheet for design

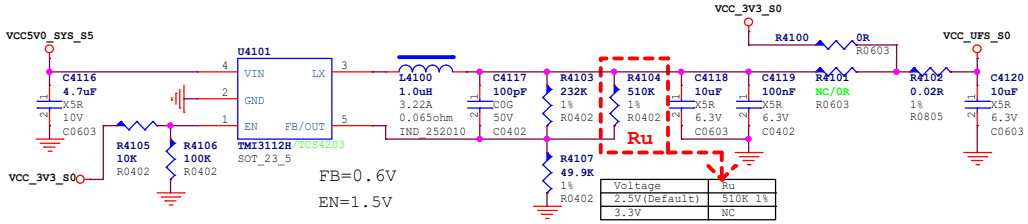
UFS POWER

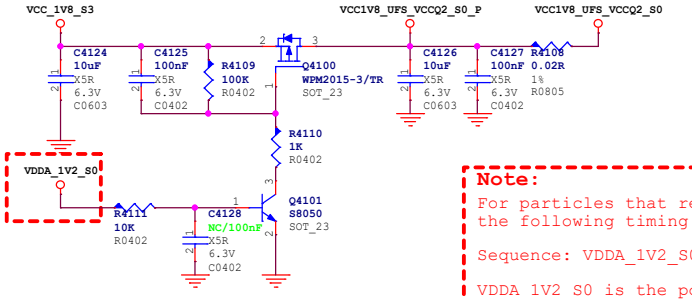
Supported Particles	VCCQ	VCCQ2	VCC	
UFS2.0	1.2V	1.8V	3.3V	Default UFS device: UFS2.2
UFS2.1	No Connect	1.8V	3.3V	
UFS2.2	No Connect	1.8V	3.3V	
UFS3.0	1.2V	No Connect	2.5V/3.3V	
UFS3.1	1.2V	No Connect	2.5V/3.3V	

Do not support UFS4.0 Device!

Sequence:VCCQ2->VCCQ, VCC is independent

Note:
The power ball that is not used at the particle must be kept floating.

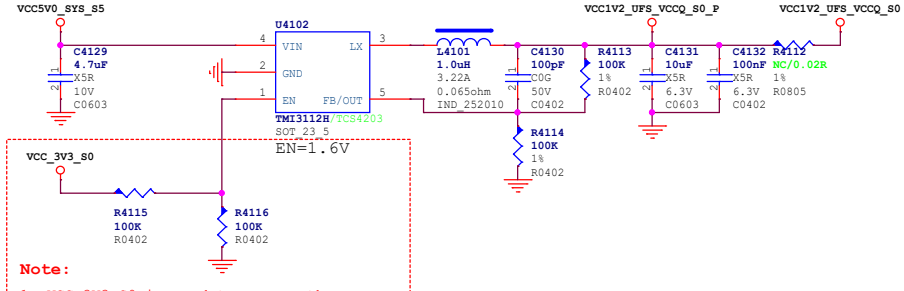




Note:
For particles that require VCCQ and VCCQ2, the following timing needs to be met:

Sequence: VDDA_1V2_S0->VCCQ2->VCCQ

VDDA_1V2_S0 is the power of REF_CK & RST_N in RK SOC, which needs to be powered on before UFS particles



Note:
1. VCC_3V3_S0 is used to ensure the power supply timing of the UFS chip;
2. The resistance voltage division value needs to be designed based on the EN pin threshold of DCDC.

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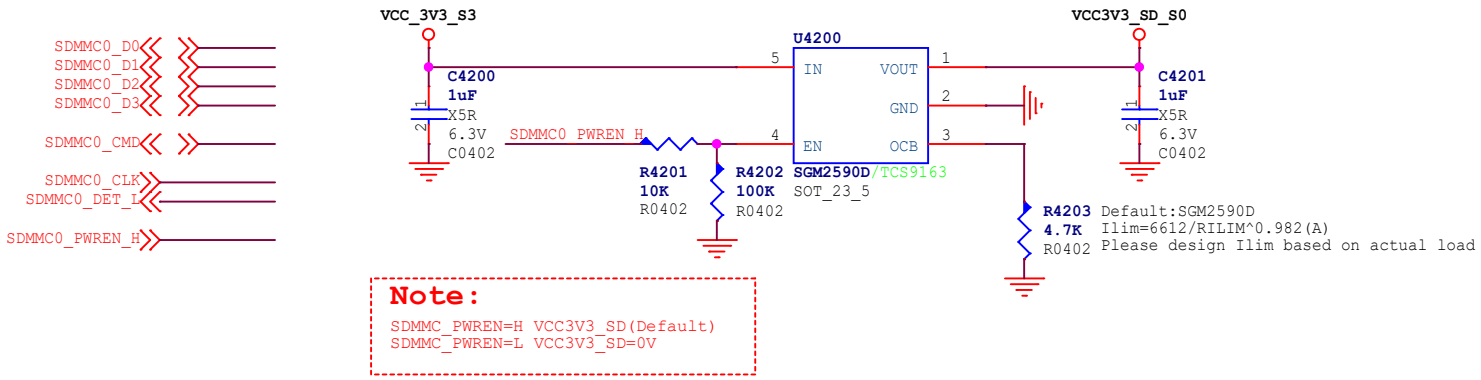
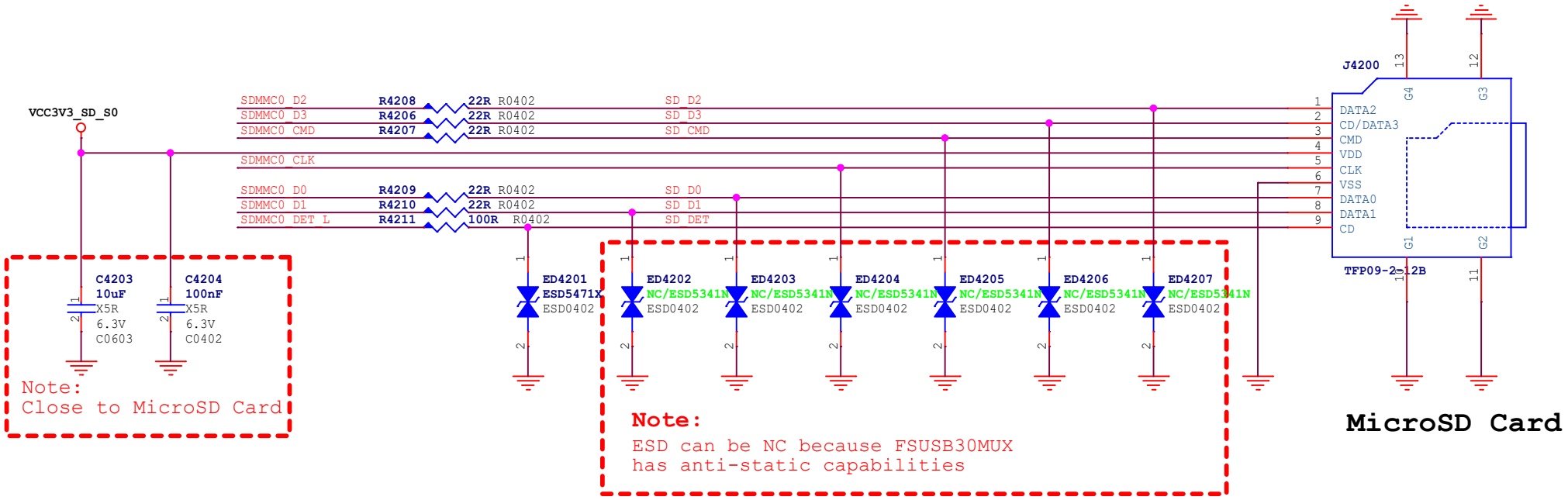
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	41.Flash-UFS		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet: 26 of 49

TF CARD



Note:
SDMMC_PWREN=H VCC3V3_SD(Default)
SDMMC_PWREN=L VCC3V3_SD=0V



Note:
Close to MicroSD Card

Note:
ESD can be NC because FSUSB30MUX
has anti-static capabilities

MicroSD Card

Note:
SDMMC_DET_L:
SDCARD PLUG: Pull-down to GND
SDCARD UNPLUG: Pull-up to PMUIO0_VCC1V8.

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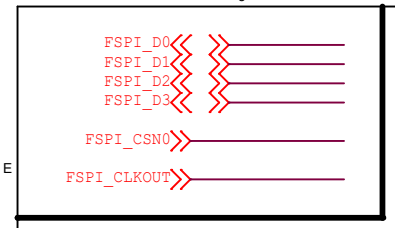
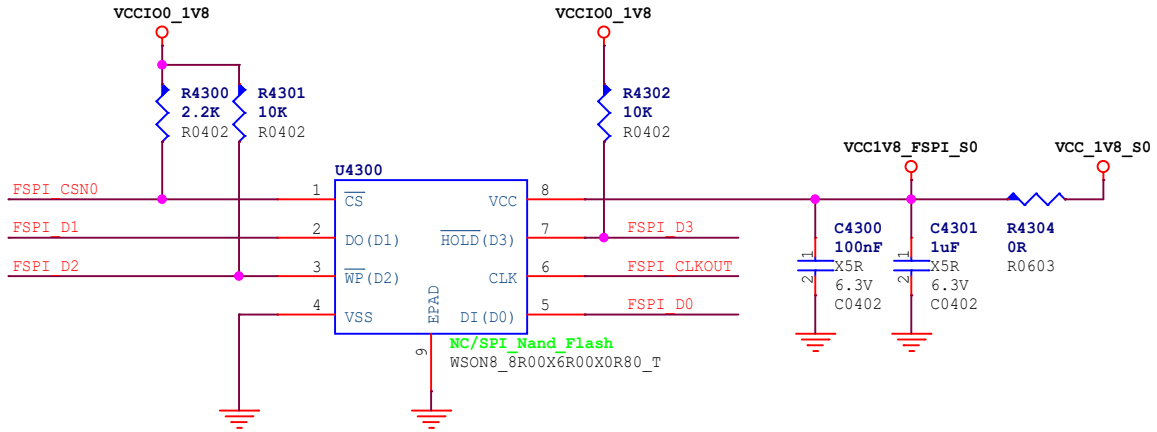
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	42.Flash-MicroSD Card		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by: Wesley Huang	Reviewed by:	Sheet:	27 of 49

SPI NOR OR NAND Flash





Note:
These caps should be placed close to the pin of FLASH device

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Project:	RK_EVB1_RK3576_LP4XD200P132SD6			
File:	43.Flash-SPI Flash(opt)			
Date:	Thursday, May 30, 2024		Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet:	28 of 49

MIPI_DPHY_CSI0_RX_CLKP/MIPI_CPHY_CSI_RX_TRIO1_C
MIPI_DPHY_CSI0_RX_CLKN/MIPI_CPHY_CSI_RX_TRIO1_B
MIPI_DPHY_CSI0_RX_D0N/MIPI_CPHY_CSI_RX_TRIO0_A
MIPI_DPHY_CSI0_RX_D0P/MIPI_CPHY_CSI_RX_TRIO0_B
MIPI_DPHY_CSI0_RX_D1N/MIPI_CPHY_CSI_RX_TRIO0_C
MIPI_DPHY_CSI0_RX_D1P/MIPI_CPHY_CSI_RX_TRIO1_A
MIPI_DPHY_CSI0_RX_D2N/MIPI_CPHY_CSI_RX_TRIO2_A
MIPI_DPHY_CSI0_RX_D2P/MIPI_CPHY_CSI_RX_TRIO2_B
MIPI_DPHY_CSI0_RX_D3N/MIPI_CPHY_CSI_RX_TRIO2_C
MIPI_DPHY_CSI0_RX_D3P/NO_USE
MIPI_DPHY_CSI0_CAM_CLKOUT
I2C4_SDA_M3_MIPI_CSI0
I2C4_SCL_M3_MIPI_CSI0
MIPI_DPHY_CSI0_PDN_H
MIPI_DPHY_CSI0_PWM
MIPI_DPHY_CSI0_PWREN_H
MIPI_DPHY_FSYNC
MIPI_DPHY_HSYNC
IRC_AIN
IRC_BIN
SAI4_MCLK_M2_DCPHY
SAI4_LRCK_M2_DCPHY
SAI4_SCLK_M2_DCPHY
SAI4_SDI_M2_DCPHY
VIDEOIN_RESERVE_IO0
VIDEOIN_RESERVE_IO1
SPDIF_RX1_M1_DCPHY

MIPI-CSI0_RX

CON4600

1	GND1	GND19	2
3	MIPI_RX0_D0N	MIPI_RX1_D0N	4
5	MIPI_RX0_D0P	MIPI_RX1_D0P	6
7	GND2	GND18	8
9	MIPI_RX0_D1N	MIPI_RX1_D1N	10
11	MIPI_RX0_D1P	MIPI_RX1_D1P	12
13	GND3	GND17	14
15	MIPI_RX0_CLK0N	MIPI_RX1_CLK0N	16
17	MIPI_RX0_CLK0P	MIPI_RX1_CLK0P	18
19	GND4	GND16	20
21	MIPI_RX0_D2N	MIPI_RX1_D2N	22
23	MIPI_RX0_D2P	MIPI_RX1_D2P	24
25	GND5	GND15	26
27	MIPI_RX0_D3N	MIPI_RX1_D3N	28
29	MIPI_RX0_D3P	MIPI_RX1_D3P	30
31	GND6	GND14	32
33	MIPI_RX0_CLK1N	MIPI_RX1_CLK1N	34
35	MIPI_RX0_CLK1P	MIPI_RX1_CLK1P	36
37	GND7	GND13	38
39	MIPI_RX0_MCLK0	MIPI_RX1_MCLK0	40
41	MIPI_RX0_MCLK1	MIPI_RX1_MCLK1	42
43	GND8	GND12	44
45	MIPI_RX0_I2C_SDA/SPI0_MOSI	MIPI_RX0_I2C_SDA/SPI1_MOSI	46
47	MIPI_RX0_I2C_SCL/SPI0_SCLK	MIPI_RX0_I2C_SCL/SPI1_SCLK	48
49	MIPI_RX0_RST0/MIPI_RX_RST	MIPI_RX1_RST0	50
51	MIPI_RX0_PDN0/MIPI_RX_INT	MIPI_RX1_PDN0	52
53	MIPI_RX0_RST1/MIPI_RX_PWM	MIPI_RX1_RST1	54
55	MIPI_RX0_PDN1/HOTPLUG_DET	MIPI_RX1_PDN1	56
57	MIPI_RX0_XVS/FSIN/SPI0_CSN	MIPI_RX1_XVS/FSIN/SPI1_CSN/IRCUT_A1	58
59	MIPI_RX0_XHS/VSYNC/SPI0_MISO	MIPI_RX1_XHS/VSYNC/SPI1_MISO/IRCUT_B1	60
	1.8V		
63	IR_PWREN	LIGHT_PWREN	64
65	MIPI_RX0_PWREN	MIPI_RX1_PWREN	66
	1.8V/3.3V		
67	IRCUT_A0/SAI_SDI2	SPDIF_TX/SAI_SDI3	68
69	IRCUT_B0/SAI_SDI1	SAI_MCLK	70
71	AF_SPI_SCLK/SAI_SDO	AF_SPI_CSN/SAI_SCLK	72
73	AF_SPI_MOSI/SAI_LRCK	AF_SPI_MISO/SAI_SDI0/SPDIF_RX	74
	3.3V		
61	1.8V	3.3V	62
75	GND9	GND11	76
77	5V_0	GND10	78
79	5V_1	12V	80
	POWER		

MIPI_DPHY_CSI0_RX_D0N/MIPI_CPHY_CSI_RX_TRIO0_A
MIPI_DPHY_CSI0_RX_D0P/MIPI_CPHY_CSI_RX_TRIO0_B
MIPI_DPHY_CSI0_RX_D1N/MIPI_CPHY_CSI_RX_TRIO0_C
MIPI_DPHY_CSI0_RX_D1P/MIPI_CPHY_CSI_RX_TRIO1_A
MIPI_DPHY_CSI0_RX_CLKN/MIPI_CPHY_CSI_RX_TRIO1_B
MIPI_DPHY_CSI0_RX_CLKP/MIPI_CPHY_CSI_RX_TRIO1_C
MIPI_DPHY_CSI0_RX_D2N/MIPI_CPHY_CSI_RX_TRIO2_A
MIPI_DPHY_CSI0_RX_D2P/MIPI_CPHY_CSI_RX_TRIO2_B
MIPI_DPHY_CSI0_RX_D3N/MIPI_CPHY_CSI_RX_TRIO2_C
MIPI_DPHY_CSI0_RX_D3P/NO_USE
MIPI_DPHY_CSI0_CAM_CLKOUT

I2C4_SDA_M3_MIPI_CSI0 — R4611 0R R0402
I2C4_SCL_M3_MIPI_CSI0 — R4612 0R R0402
MIPI_DPHY_CSI0_PDN_H — R4613 0R R0402
MIPI_DPHY_FSYNC — R4614 0R R0402
MIPI_DPHY_CSI0_PWM — R4615 NC/0R R0402
MIPI_DPHY_HSYNC — R4616 0R R0402
MIPI_DPHY_CSI0_PWREN_H — R4617 0R R0402
IRC_AIN — R4618 0R R0402
IRC_BIN — R4619 0R R0402
SAI4_LRCK_M2_DCPHY — R4622 0R R0402

VIDEOIN_RESERVE_IO0
VIDEOIN_RESERVE_IO1

TP4600 TP_0.7
R4620 0R R0402 SAI4_MCLK_M2_DCPHY
R4621 0R R0402 SAI4_SCLK_M2_DCPHY
R4623 0R R0402 SAI4_SDI_M2_DCPHY
R4628 NC/0R R0402 SPDIF_RX1_M1_DCPHY

VCC_1V8_S0 — R4624 0R R0603
VCC5V0_DEVICE_S0 — R4626 0R R0603

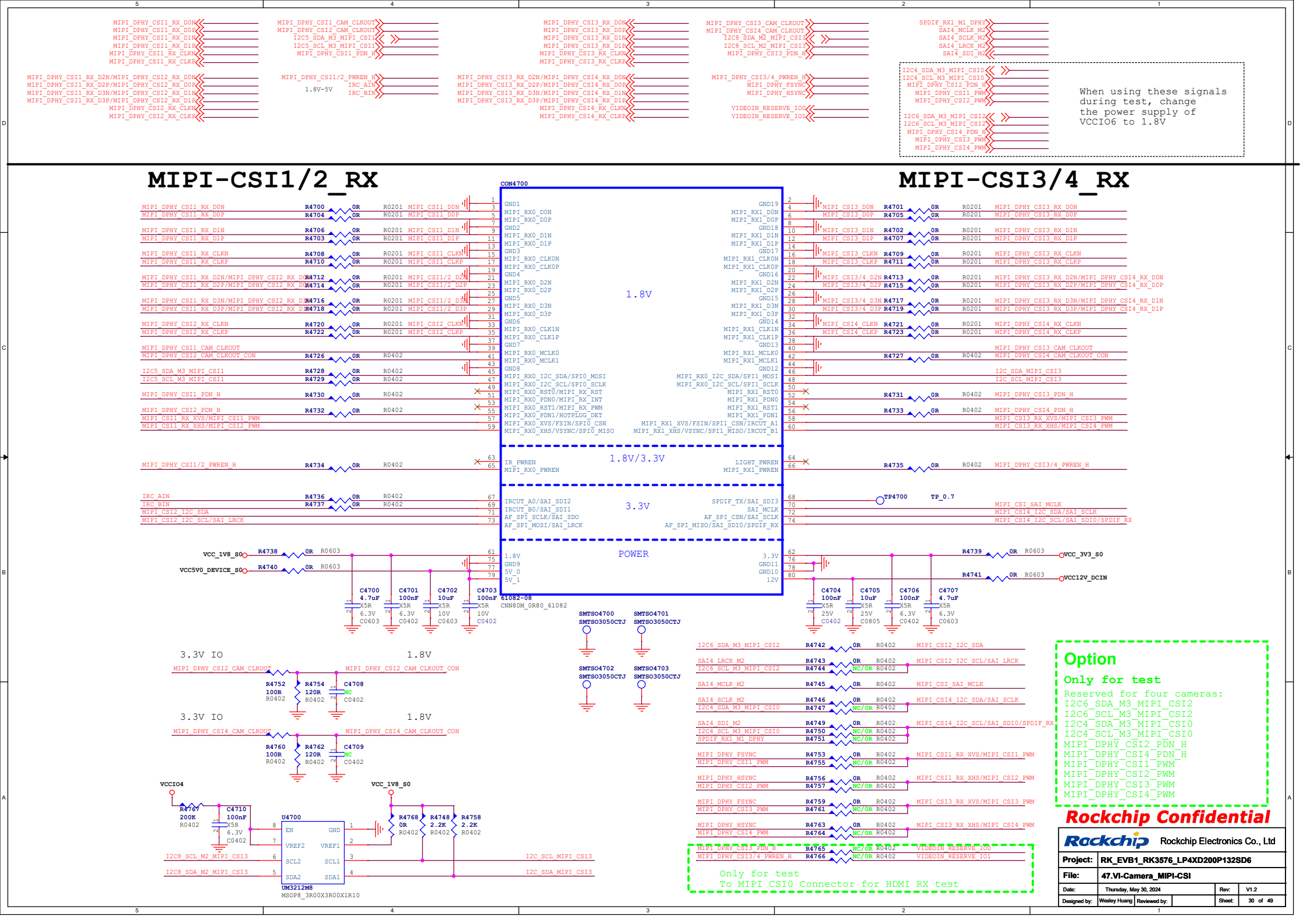
C4600 4.7uF X5R 6.3V C0603
C4601 100nF X5R 6.3V C0402
C4602 10uF X5R 10V C0603
C4603 100nF X5R 10V C0402
61082-08 CNN80M_0R80_61082

R4625 0R R0603 VCC_3V3_S0
R4627 0R R0603 VCC12V_DCIN

C4604 100nF X5R 25V C0402
C4605 10uF X5R 25V C0805
C4606 100nF X5R 6.3V C0402
C4607 4.7uF X5R 6.3V C0603

SMTSO4600 SMTSO3050CTJ
SMTSO4601 SMTSO3050CTJ
SMTSO4602 SMTSO3050CTJ
SMTSO4603 SMTSO3050CTJ

Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	46.VI-Camera_MIPI-DCPHY		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet: 29 of 49


MIPI_DPHY_CSI1_RX_D0N
MIPI_DPHY_CSI1_RX_D0P
MIPI_DPHY_CSI1_RX_D1N
MIPI_DPHY_CSI1_RX_D1P
MIPI_DPHY_CSI1_RX_CLKN
MIPI_DPHY_CSI1_RX_CLKP
MIPI_DPHY_CSI1_RX_D2N/MIPI_DPHY_CSI2_RX_D0N
MIPI_DPHY_CSI1_RX_D2P/MIPI_DPHY_CSI2_RX_D0P
MIPI_DPHY_CSI1_RX_D3N/MIPI_DPHY_CSI2_RX_D1N
MIPI_DPHY_CSI1_RX_D3P/MIPI_DPHY_CSI2_RX_D1P
MIPI_DPHY_CSI2_RX_CLKN
MIPI_DPHY_CSI2_RX_CLKP
MIPI_DPHY_CSI1_CAM_CLKOUT
MIPI_DPHY_CSI2_CAM_CLKOUT
I2C5_SDA_M3_MIPI_CSI1
I2C5_SCL_M3_MIPI_CSI1
MIPI_DPHY_CSI1_PDN_H
MIPI_DPHY_CSI1/2_PWREN_H
1.8V~5V
IRC_AIN
IRC_BIN
MIPI_DPHY_CSI3_RX_D0N
MIPI_DPHY_CSI3_RX_D0P
MIPI_DPHY_CSI3_RX_D1N
MIPI_DPHY_CSI3_RX_D1P
MIPI_DPHY_CSI3_RX_CLKN
MIPI_DPHY_CSI3_RX_CLKP
MIPI_DPHY_CSI3_RX_D2N/MIPI_DPHY_CSI4_RX_D0N
MIPI_DPHY_CSI3_RX_D2P/MIPI_DPHY_CSI4_RX_D0P
MIPI_DPHY_CSI3_RX_D3N/MIPI_DPHY_CSI4_RX_D1N
MIPI_DPHY_CSI3_RX_D3P/MIPI_DPHY_CSI4_RX_D1P
MIPI_DPHY_CSI4_RX_CLKN
MIPI_DPHY_CSI4_RX_CLKP
MIPI_DPHY_CSI3_CAM_CLKOUT
MIPI_DPHY_CSI4_CAM_CLKOUT
I2C8_SDA_M2_MIPI_CSI3
I2C8_SCL_M2_MIPI_CSI3
MIPI_DPHY_CSI3_PDN_H
MIPI_DPHY_CSI3/4_PWREN_H
MIPI_DPHY_FSYNC
MIPI_DPHY_HSYNC
VIDEOIN_RESERVE_IO0
VIDEOIN_RESERVE_IO1
SPDIF_RX1_M1_DPHY
SAI4_MCLK_M2
SAI4_SCLK_M2
SAI4_LRCK_M2
SAI4_SDI_M2
I2C4_SDA_M3_MIPI_CSI0
I2C4_SCL_M3_MIPI_CSI0
MIPI_DPHY_CSI2_PDN_H
MIPI_DPHY_CSI1_PWM
MIPI_DPHY_CSI2_PWM
I2C6_SDA_M3_MIPI_CSI2
I2C6_SCL_M3_MIPI_CSI2
MIPI_DPHY_CSI4_PDN_H
MIPI_DPHY_CSI3_PWM
MIPI_DPHY_CSI4_PWM
When using these signals during test, change the power supply of VCCIO6 to 1.8V
MIPI-CSI1/2_RX
MIPI-CSI3/4_RX
CON4700
1.8V
1.8V/3.3V
3.3V
POWER
R4700 0R R0201 MIPI_CSI1_D0N
R4704 0R R0201 MIPI_CSI1_D0P
R4706 0R R0201 MIPI_CSI1_D1N
R4703 0R R0201 MIPI_CSI1_D1P
R4708 0R R0201 MIPI_CSI1_CLKN
R4710 0R R0201 MIPI_CSI1_CLKP
R4712 0R R0201 MIPI_CSI1/2_D2N
R4714 0R R0201 MIPI_CSI1/2_D2P
R4716 0R R0201 MIPI_CSI1/2_D3N
R4718 0R R0201 MIPI_CSI1/2_D3P
R4720 0R R0201 MIPI_CSI2_CLKN
R4722 0R R0201 MIPI_CSI2_CLKP
R4726 0R R0402
R4728 0R R0402
R4729 0R R0402
R4730 0R R0402
R4732 0R R0402
R4734 0R R0402
R4736 0R R0402
R4737 0R R0402
R4738 0R R0603 VCC_1V8_S0
R4740 0R R0603 VCC5V0_DEVICE_S0
R4701 0R R0201 MIPI_CSI3_D0N
R4705 0R R0201 MIPI_CSI3_D0P
R4702 0R R0201 MIPI_CSI3_D1N
R4707 0R R0201 MIPI_CSI3_D1P
R4709 0R R0201 MIPI_CSI3_CLKN
R4711 0R R0201 MIPI_CSI3_CLKP
R4713 0R R0201 MIPI_CSI3/4_D2N
R4715 0R R0201 MIPI_CSI3/4_D2P
R4717 0R R0201 MIPI_CSI3/4_D3N
R4719 0R R0201 MIPI_CSI3/4_D3P
R4721 0R R0201 MIPI_CSI4_CLKN
R4723 0R R0201 MIPI_CSI4_CLKP
R4727 0R R0402
R4731 0R R0402
R4733 0R R0402
R4735 0R R0402
R4739 0R R0603 VCC_3V3_S0
R4741 0R R0603 VCC12V_DCIN
TP4700 TP_0.7
C4700 4.7uF X5R 6.3V C0603
C4701 100nF X5R 6.3V C0402
C4702 10uF X5R 10V C0603
C4703 100nF X5R 10V C0402
C4704 100nF X5R 25V C0402
C4705 10uF X5R 25V C0805
C4706 100nF X5R 6.3V C0402
C4707 4.7uF X5R 6.3V C0603
61082-08 CNN80M_0R80_61082
SMTSO4700 SMTSO3050CTJ
SMTSO4701 SMTSO3050CTJ
SMTSO4702 SMTSO3050CTJ
SMTSO4703 SMTSO3050CTJ
3.3V IO
1.8V
R4752 100R R0402
R4754 120R R0402
C4708 NC C0402
R4760 100R R0402
R4762 120R R0402
C4709 NC C0402
VCCIO4
VCC_1V8_S0
R4767 200K R0402
C4710 100nF X5R 6.3V C0402
U4700
UM3212M8
MSOP8_3R00X3R00X1R10
R4768 0R R0402
R4748 2.2K R0402
R4758 2.2K R0402
I2C8_SCL_M2_MIPI_CSI3
I2C8_SDA_M2_MIPI_CSI3
I2C_SCL_MIPI_CSI3
I2C_SDA_MIPI_CSI3
R4742 0R R0402 MIPI_CSI2_I2C_SDA
R4743 0R R0402 MIPI_CSI2_I2C_SCL/SAI_LRCK
R4744 NC/0R R0402
R4745 0R R0402 MIPI_CSI_SAI_MCLK
R4746 0R R0402 MIPI_CSI4_I2C_SDA/SAI_SCLK
R4747 NC/0R R0402
R4749 0R R0402 MIPI_CSI4_I2C_SCL/SAI_SDI0/SPDIF_RX
R4750 NC/0R R0402
R4751 NC/0R R0402
R4753 0R R0402 MIPI_CSI1_RX_XVS/MIPI_CSI1_PWM
R4755 NC/0R R0402
R4756 0R R0402 MIPI_CSI1_RX_XHS/MIPI_CSI2_PWM
R4757 NC/0R R0402
R4759 0R R0402 MIPI_CSI3_RX_XVS/MIPI_CSI3_PWM
R4761 NC/0R R0402
R4763 0R R0402 MIPI_CSI3_RX_XHS/MIPI_CSI4_PWM
R4764 NC/0R R0402
R4765 NC/0R R0402 VIDEOIN_RESERVE_IO0
R4766 NC/0R R0402 VIDEOIN_RESERVE_IO1
Only for test
To MIPI CSI0 Connector for HDMI RX test
Option
Only for test
Reserved for four cameras:
I2C6_SDA_M3_MIPI_CSI2
I2C6_SCL_M3_MIPI_CSI2
I2C4_SDA_M3_MIPI_CSI0
I2C4_SCL_M3_MIPI_CSI0
MIPI_DPHY_CSI2_PDN_H
MIPI_DPHY_CSI4_PDN_H
MIPI_DPHY_CSI1_PWM
MIPI_DPHY_CSI2_PWM
MIPI_DPHY_CSI3_PWM
MIPI_DPHY_CSI4_PWM
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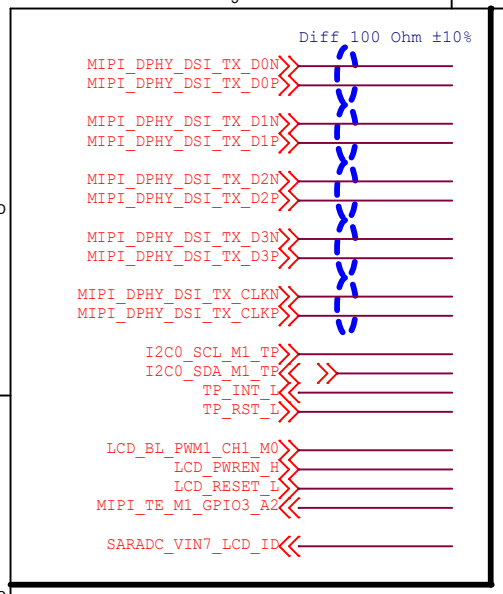
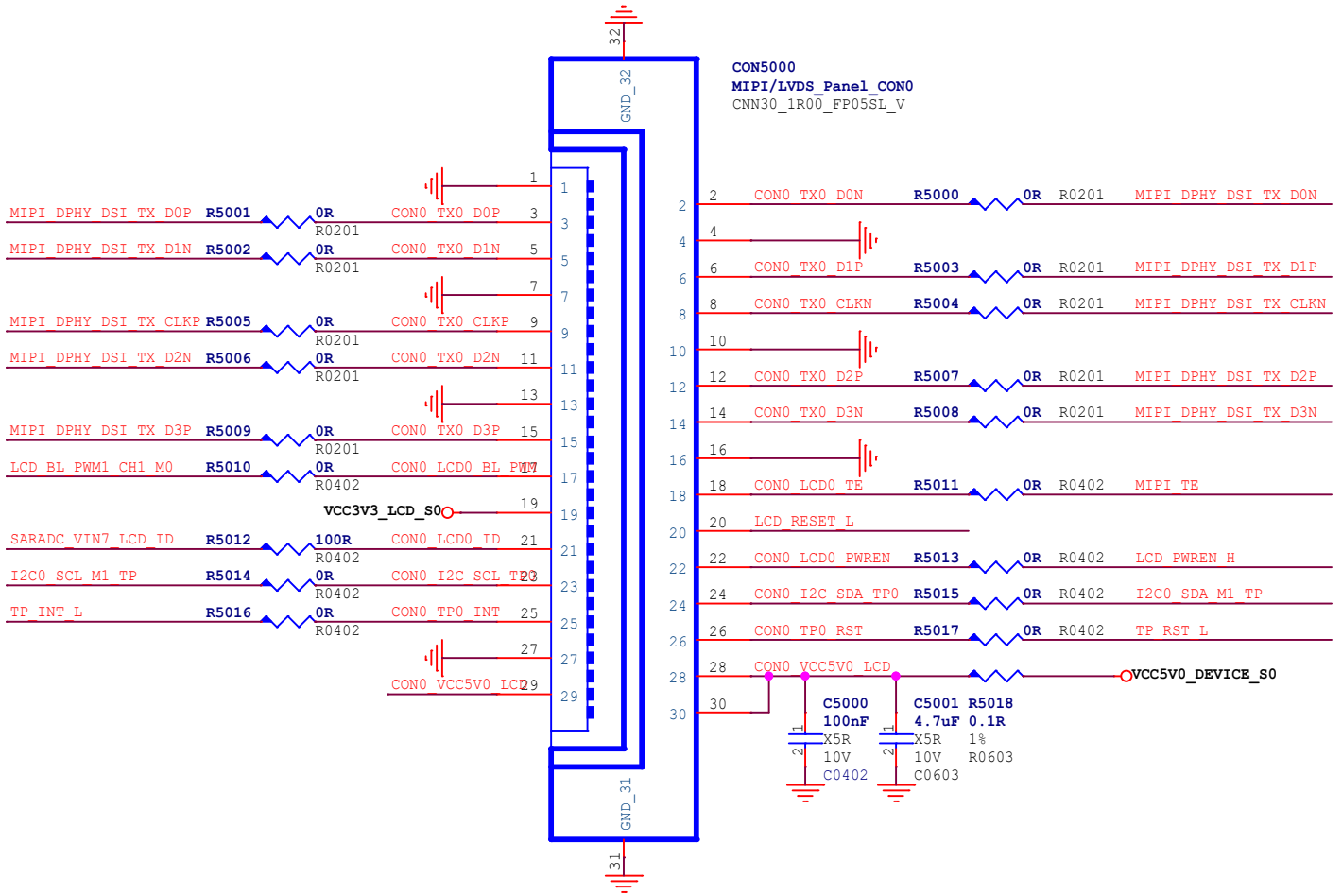
Rockchip Electronics Co., Ltd
Project: RK_EVB1_RK3576_LP4XD200P132SD6
File: 47.VI-Camera_MIPI-CSI
Date: Thursday, May 30, 2024
Rev: V1.2
Designed by: Wesley Huang
Reviewed by:
Sheet: 30 of 49

Single-MIPI LCM



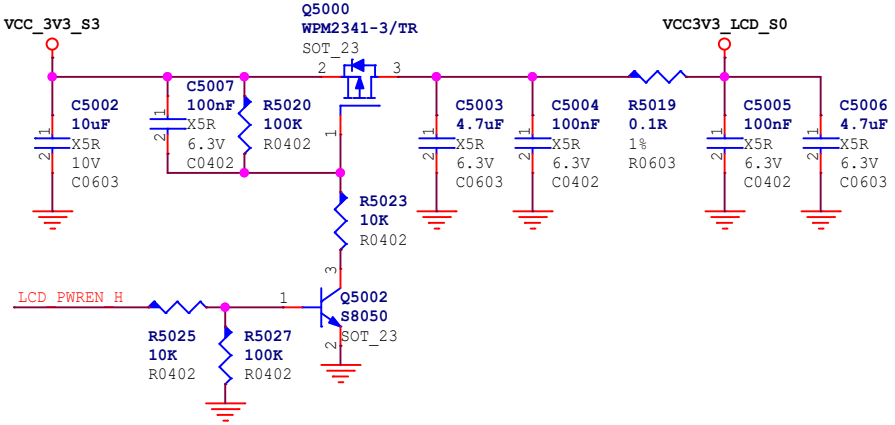


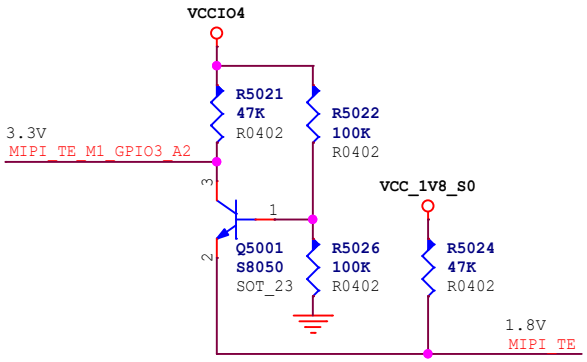
FPC Pin List

Pin1	GND
Pin2	D0N
Pin3	D0P
Pin4	GND
Pin5	D1N
Pin6	D1P
Pin7	GND
Pin8	CLKN/AUXN
Pin9	CLKP/AUXP
Pin10	GND
Pin11	D2N
Pin12	D2P
Pin13	GND
Pin14	D3N
Pin15	D3P
Pin16	GND
Pin17	LCD_PWM_BL
Pin18	LCD_TE
Pin19	VCC3V3_LCD
Pin20	LCD_RST
Pin21	LCD_ID
Pin22	LCD_PWREN
Pin23	TP_I2C_SCL
Pin24	TP_I2C_SDA
Pin25	TP_INT
Pin26	TP_RST
Pin27	GND
Pin28	5V0
Pin29	5V0
Pin30	5V0

Note:

Signal	IO Level
I2C_SCL_TP	3.3V
I2C_SDA_TP	3.3V
TP_INT_L	3.3V
TP_RST_L	1080P:3.3V 720P:1.8V
LCD_BL_PWM	3.3V
LCD_PWREN_H	1.8V/3.3V
LCD_RST_L	1.8V
MIPI_TE	1.8V
SARADC_VIN7_LCD_ID	1.8V





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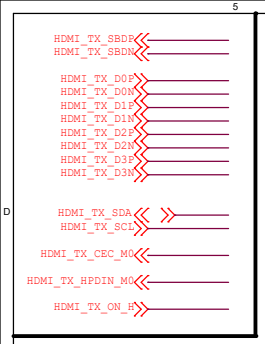
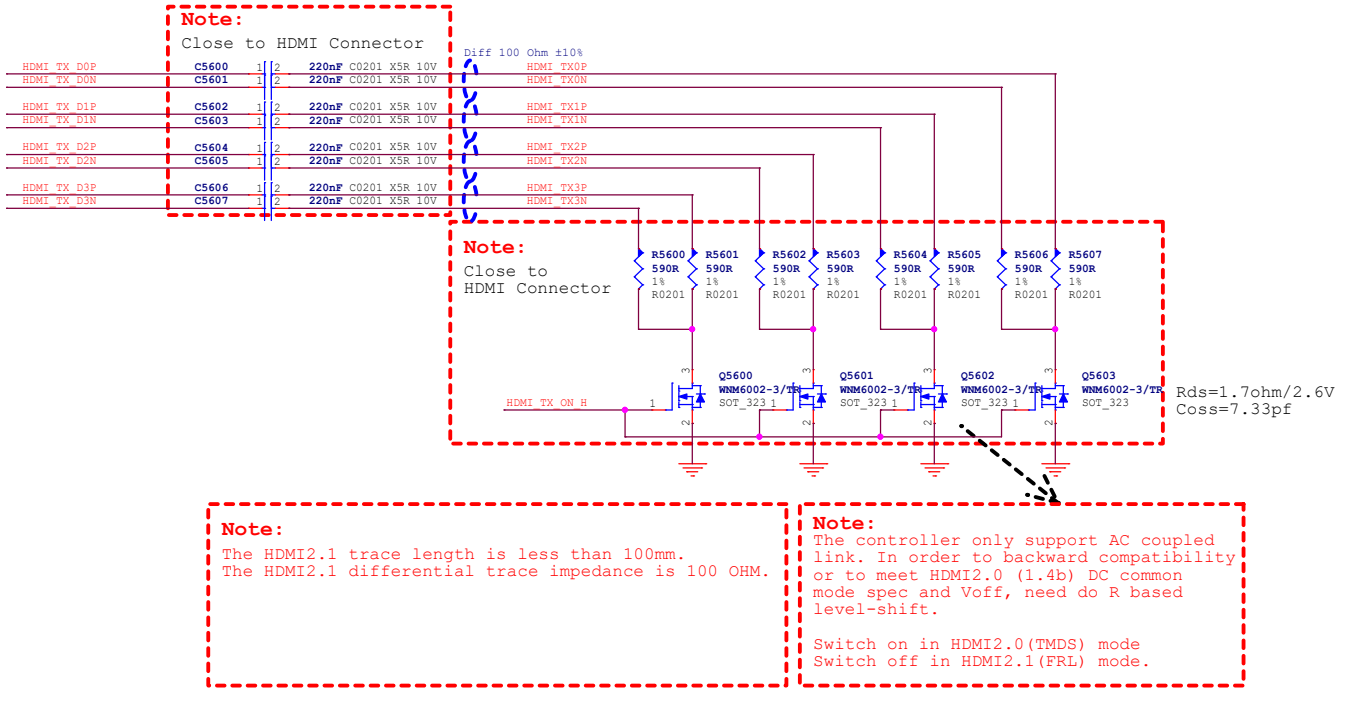
Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	50.VO-LCM MIPI DPHY TX		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by: Wesley Huang	Reviewed by:	Sheet:	31 of 49

HDMI 2.1

Support video output up to 4Kx2K@120Hz

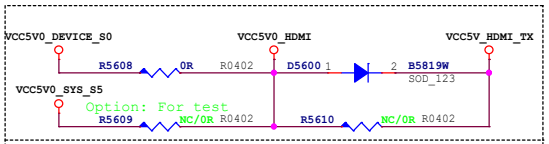




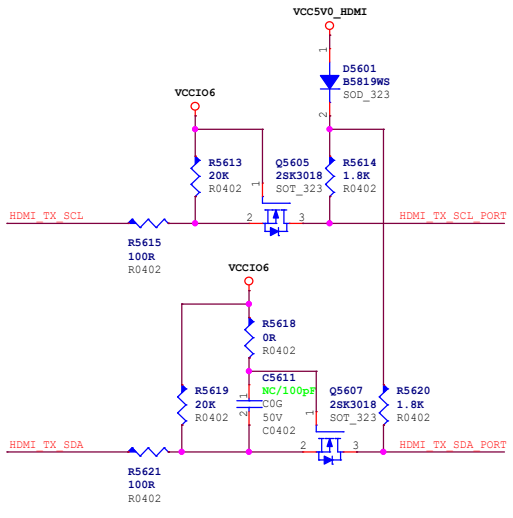
Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

Note:
The controller only support AC coupled link. In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

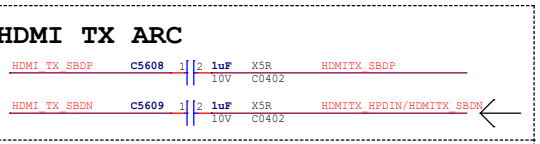
Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.



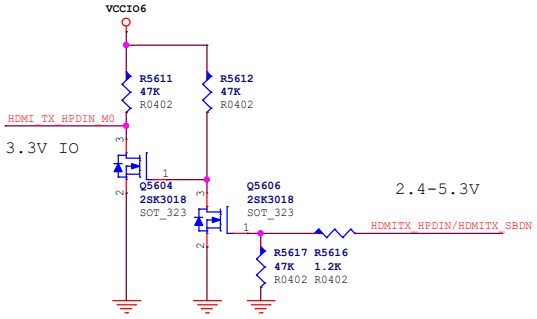
HDMI TX DDC



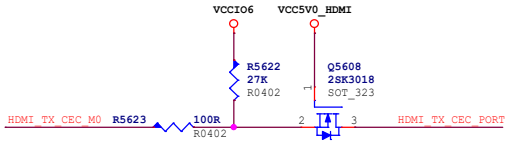
HDMI TX ARC



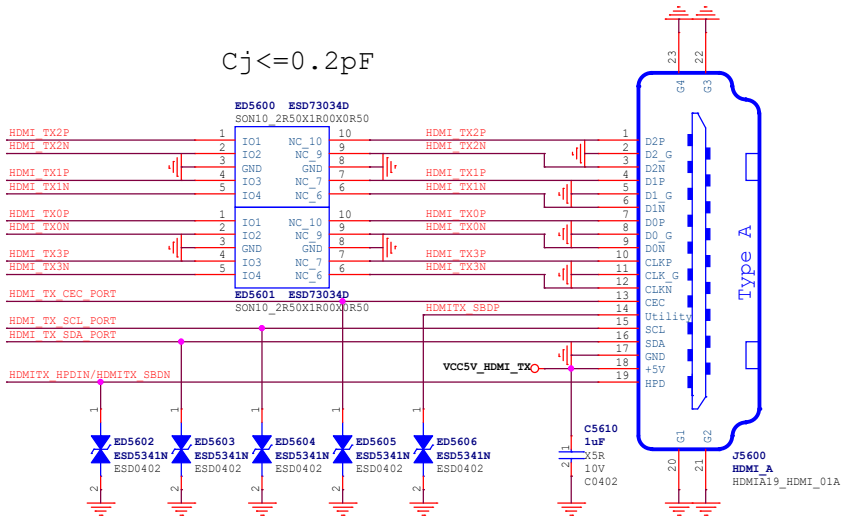
HDMI TX HPD



HDMI TX CEC



Cj<=0.2pF



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	56.VO-HDMI TX				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:		Sheet:	32 of 49

PCIe WIFI6/BT Module-2T2R

WIFI_PCIE0_REFCLKP
WIFI_PCIE0_REFCLKN
WIFI_PCIE0_TXP
WIFI_PCIE0_TXN
WIFI_PCIE0_RXP
WIFI_PCIE0_RXN
PCIE0_CLKREQn_M0
PCIE0_WAKEn_M0
PCIE0_PERSTn
32KOUT_RTC2WIFI

SAI2_SCLK_M0
SAI2_LRCK_M0
SAI2_SDO_M0
SAI2_SDI_M0
UART4_TX_M1
UART4_RX_M1
UART4_RTSN_M1
UART4_CTSN_M1
BT_REG_ON_H
BT_WAKE_HOST_H
HOST_WAKE_BT_H
WIFI_REG_ON_H
WIFI_WAKE_HOST_H

ANT6400 夹板式
SMA-J-P-H-RA-TH1
ANT5_SMA_ST_EM1
ANT6401
SMA-J-P-H-RA-TH1
ANT5_SMA_ST_EM1
ANT6402
ANT_JACK
ANT_JACK

C6400 NC C0402
C6402 10pF C0G 50V C0402
C6403 10pF C0G 50V C0402
C6401 NC C0402
C6405 NC C0402
C6410 NC C0402
C6406 NC/10pF C0G 50V C0402
C6404 NC C0402
C6407 NC C0402

50 Ohm RF trace

This standalone BT-ANT is reserved for AP6275PR3.
Leave PIN48 float for AP6275P, of which BT-ANT is mux with WIFI.

U6400
AP6275P
MD55_WIFI_AP6276P

Pins for AP6276P
GND_55 GND_54 GND_53 GPIO_52 GPIO_51

NOTE:
Adjust the load capacitor according to the crystal spec.

Y6400
37.4MHz
CRY4_3R20X2R50X0R8
C6408 12pF C0G 50V C0402
C6409 12pF C0G 50V C0402
R6400 0R R0402
XIN_WIFI
XOUT_WIFI

R6401 0R R0402
C6415 4.7uF X5R 6.3V C0402

PCIE0_PERSTn_1V8
XIN_WIFI
XOUT_WIFI
WIFI_REG_ON_H
WIFI_WAKE_HOST_H
SAI2_SDI_M0
SAI2_SDO_M0
SAI2_LRCK_M0
SAI2_SCLK_M0
PCIE0_WAKEn_1V8

PCIE_PERST_L
XTAL_IN
XTAL_OUT
WL_REG_ON
WL_HOST_WAKE
GPIO_17
GPIO_18
BT_PCM_OUT
BT_PCM_IN
BT_PCM_SYNC
BT_PCM_CLK
GND_23
PCIE_PME_L
CBUCK_0P9

BT_HOST_WAKE
BT_WAKE
BT_ANT
PCIE_TX_P
PCIE_TX_N
PCIE_RX_P
PCIE_RX_N
BT_UART_CTS_N
BT_UART_RTS_N
BT_UART_RXD
BT_UART_TXD
GND_39
BT_REG_ON
PCIE_CLKREQ_L

BT_WAKE_HOST_H
HOST_WAKE_BT_H
AP627xP_PCIE_TXP
AP627xP_PCIE_TXN
AP627xP_PCIE_RXP
AP627xP_PCIE_RXN
UART4_RTSN_M1
UART4_CTSN_M1
UART4_TX_M1
UART4_RX_M1
BT_REG_ON_H
PCIE0_CLKREQn_1V8

C6411 100nF X5R 10V C0201 WIFI_PCIE0_RXP
C6412 100nF X5R 10V C0201 WIFI_PCIE0_RXN
C6413 100nF X5R 10V C0201 WIFI_PCIE0_TXP
C6414 100nF X5R 10V C0201 WIFI_PCIE0_TXN

NOTE:
The packaging of AP6276P is compatible with AP6275P

AP627xP_REFCLKP
AP627xP_REFCLKN
C6416 100pF X5R 25V C0201 WIFI_PCIE0_REFCLKP
C6417 100pF X5R 25V C0201 WIFI_PCIE0_REFCLKN

L6400 2.2uH IND_303015 1A_DCR<=80mohm
L6401 2.2uH IND_303015 1A_DCR<=80mohm

VCC_3V3_S3
VCC3V3_PCIEWL_VBAT
R6402 0.02R R0805 1%
VCC_3V3_S0
R6404 NC/0.02R R0805 1%

VBAT:(3.1-3.8V)/1.2A
VDDIO:(1.68-1.98V)/300mA.

32.768KHZ:
+/-25ppm/30-70%/1.8V

Y6401
32.768KHz
CRY4_3R20X2R50X1R20
C6424 100nF X5R 6.3V C0402
R6407 470K R0402
32KOUT_CRY
32KOUT_RTC2WIFI
R6403 NC/0R R0402
R6405 22R R0402
WIFIBT_32KIN_2T2R
R6406 NC R0402
C6421 NC C0402

C6420 4.7uF X5R 6.3V C0402
C6418 100nF X5R 6.3V C0402
C6419 22uF X5R 6.3V C0603
C6422 100nF X5R 6.3V C0402
C6423 4.7uF X5R 6.3V C0402

VCC3V3_PCIEWL_VBAT
VCCIO_WL

PCIE0_PERSTn
PCIE0_PERSTn_1V8
R6410 10K R0402
R6413 12K R0402

VCCIO4
3.3V
PCIE0_CLKREQn_M0
R6408 47K R0402
R6411 100K R0402
Q6400 S8050 SOT_23
R6416 100K R0402
R6414 47K R0402
VCC_1V8_S0
VCCIO_WL
R6418 NC/47K R0402
OD
PCIE0_CLKREQn_1V8
Option: For test

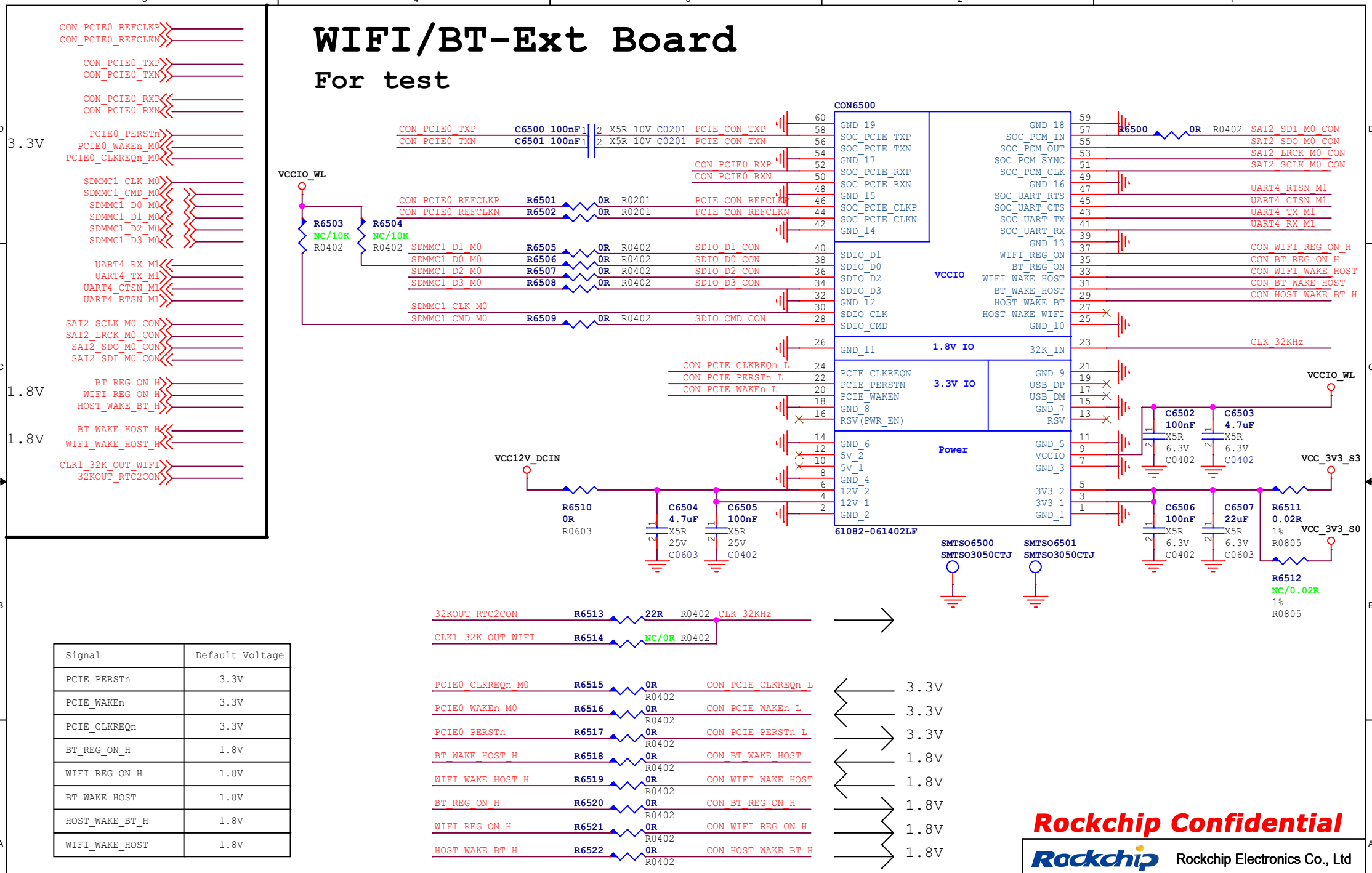
PMUIO1_VCC
3.3V
PCIE0_WAKEn_M0
R6409 47K R0402
R6412 100K R0402
Q6401 S8050 SOT_23
R6417 100K R0402
R6415 47K R0402
VCC_1V8_S0
VCCIO_WL
R6419 NC/47K R0402
OD
PCIE0_WAKEn_1V8
Option: For test

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	64.WIFI6/BT-PCIe+UART_2T2R		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet: 33 of 49

WIFI/BT-Ext Board

For test

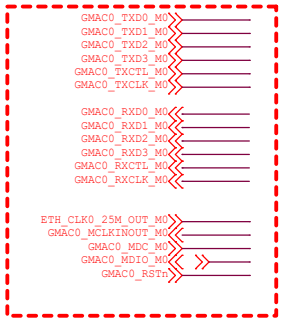


Signal	Default Voltage
PCIE_PERSTn	3.3V
PCIE_WAKEn	3.3V
PCIE_CLKREQn	3.3V
BT_REG_ON_H	1.8V
WIFI_REG_ON_H	1.8V
BT_WAKE_HOST	1.8V
HOST_WAKE_BT_H	1.8V
WIFI_WAKE_HOST	1.8V

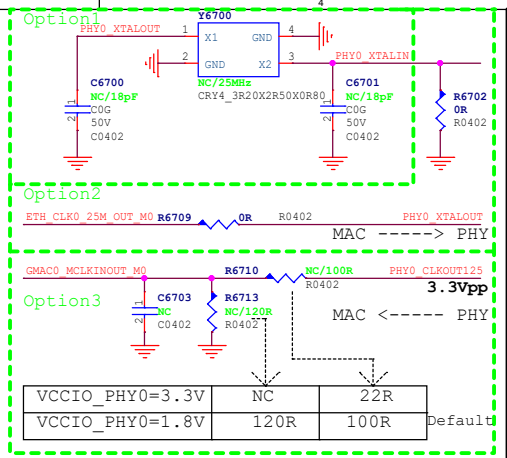
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	65.WIFI/BT-RK WIFI Connector		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet: 34 of 49

RGMII0_M0

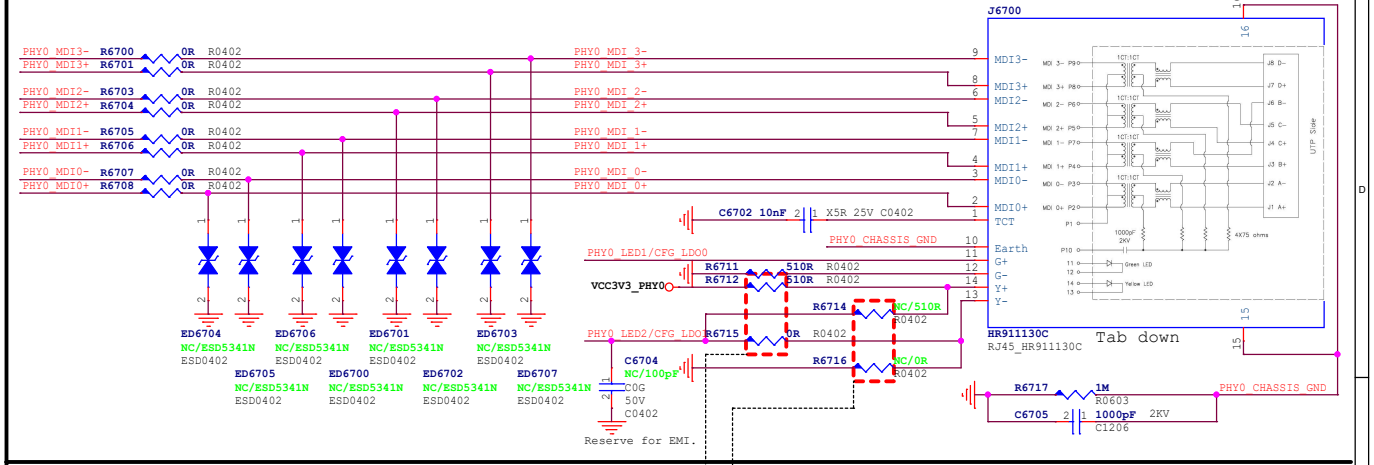


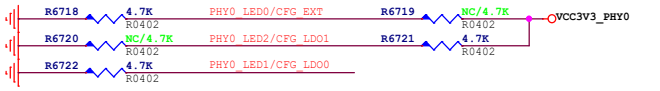
RK SOC clock mode recommended	
RK3576	mode1,mode2



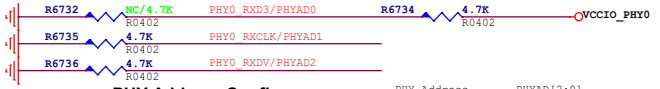
VCCIO_PHY0=3.3V	NC	22R	
VCCIO_PHY0=1.8V	120R	100R	Default

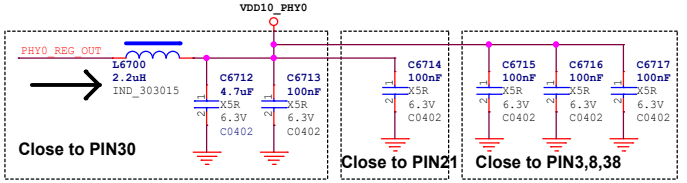
Giga PHY clock mode selected			
Clock mode	Option1	Option2	Option3
mode1	No	Yes	No
mode2	Yes	No	No
mode3	Yes	No	Yes

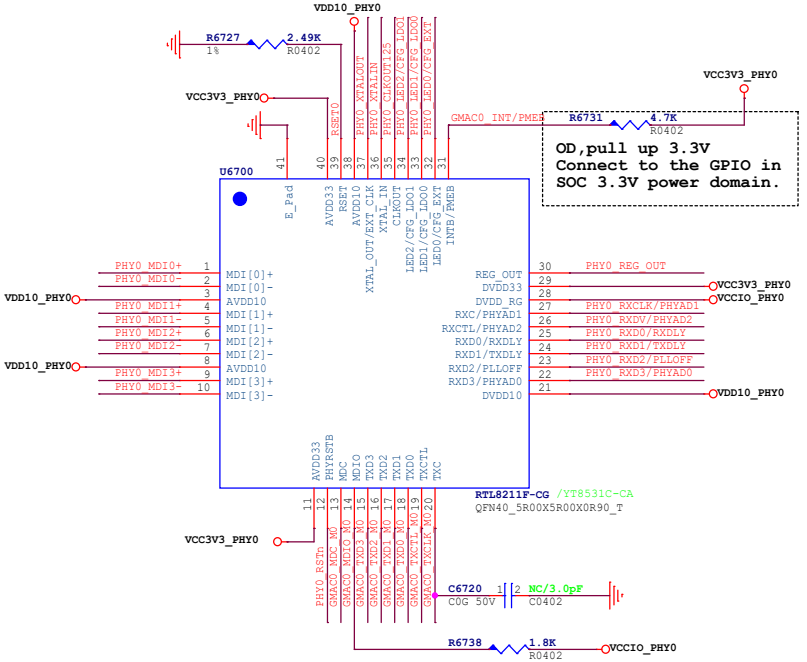




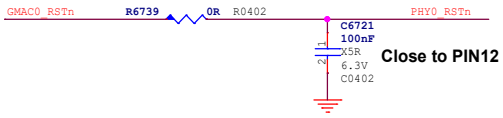
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	PHY0_LED2
External 3.3V	1'b1	2'b00	String 510R to GND
External 1.8V	1'b1	2'b10	String 510R to VCC3V3_PHY
Internal 1.8V (default)	1'b0	2'b10	String 510R to VCC3V3_PHY

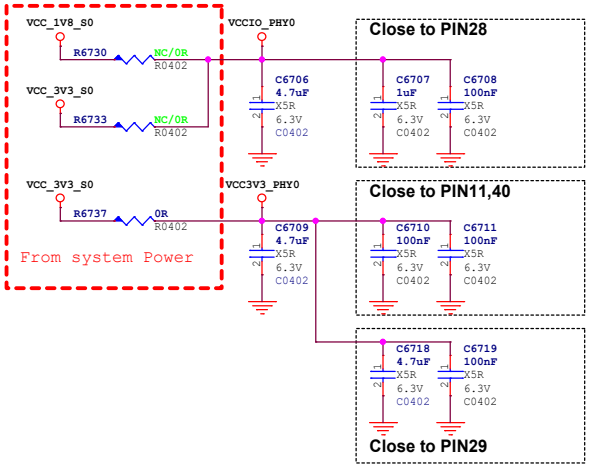


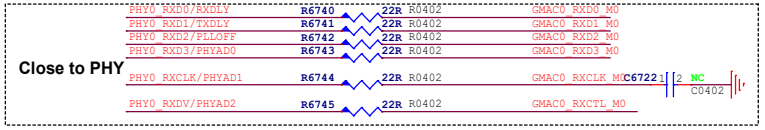




PHYRSTB is 3.3V IO







Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	67.Ethernet-GEPHY_RGMII0		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet: 35 of 49

RGMII1_M0

RK SOC clock mode recommended	
RK3576	mode1,mode2

Giga PHY clock mode selected			
Clock mode	Option1	Option2	Option3
mode1	No	Yes	No
mode2	Yes	No	No
mode3	Yes	No	Yes

Option1

Option2

Option3

VCCIO_PHY0=3.3V	NC	22R	
VCCIO_PHY0=1.8V	120R	100R	Default

VCC_PHY0_IO Voltage Config

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	PHY1_LED2
External 3.3V (default)	1'b1	2'b00	String 510R to GND
External 1.8V	1'b1	2'b10	String 510R to VCC3V3_PHY
Internal 1.8V	1'b0	2'b10	String 510R to VCC3V3_PHY

Pull-up to disable PLL @ ALDPS mode(Low power mode)

Pull-up for additional 2ns delay to RXC for data latching

Pull-up for additional 2ns delay to TXC for data latching

PHY Address Config

PHY Address	PHYAD[2:0]
1 (default)	3'b001

OD,pull up 3.3V
Connect to the GPIO in
SOC 3.3V power domain.

PHYRSTB is 3.3V IO

Close to PHY

Close to PIN28

Close to PIN11,40

Close to PIN29

Close to PIN30

Close to PIN21

Close to PIN3,8,38

Close to PIN12

From system Power

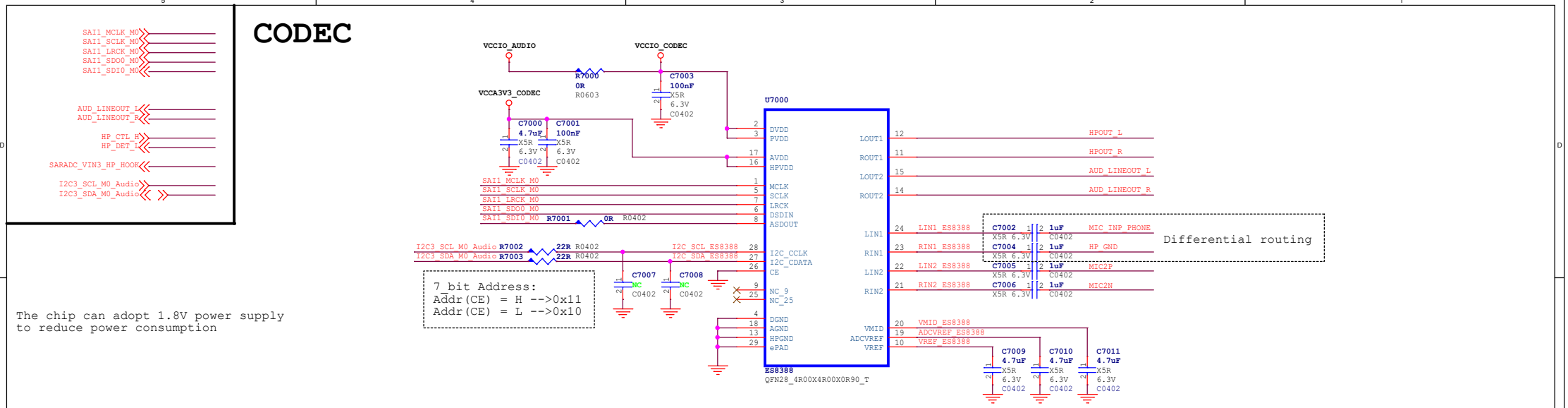
Tab down

Reserve for EMI.

Rockchip Confidential

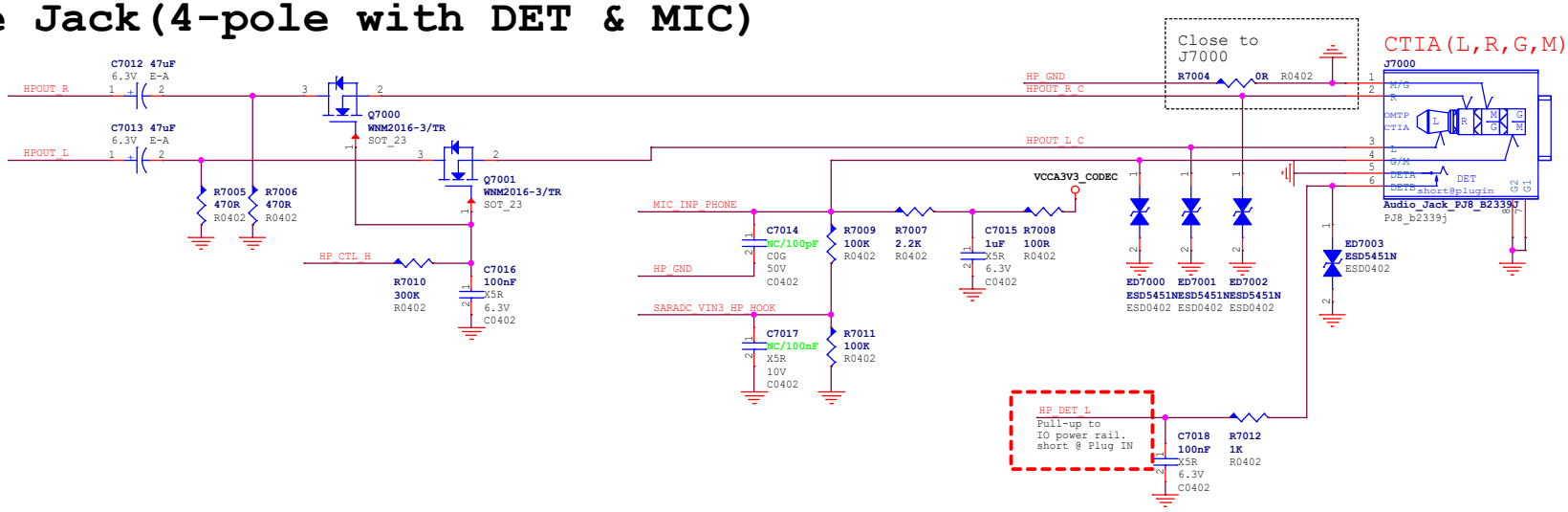
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	68.Ethernet-GEPHY_RGMII1		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet: 36 of 49

CODEC

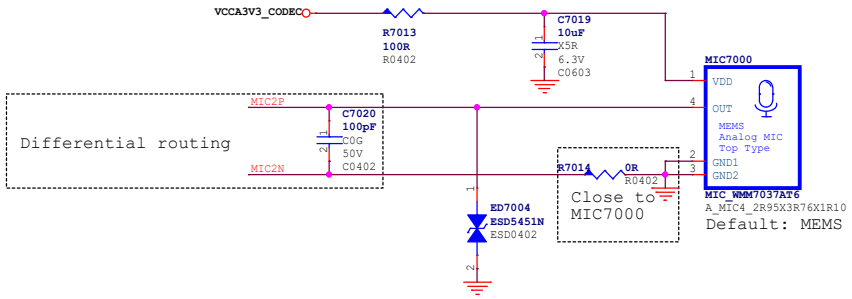


The chip can adopt 1.8V power supply to reduce power consumption

Headphone Jack(4-pole with DET & MIC)



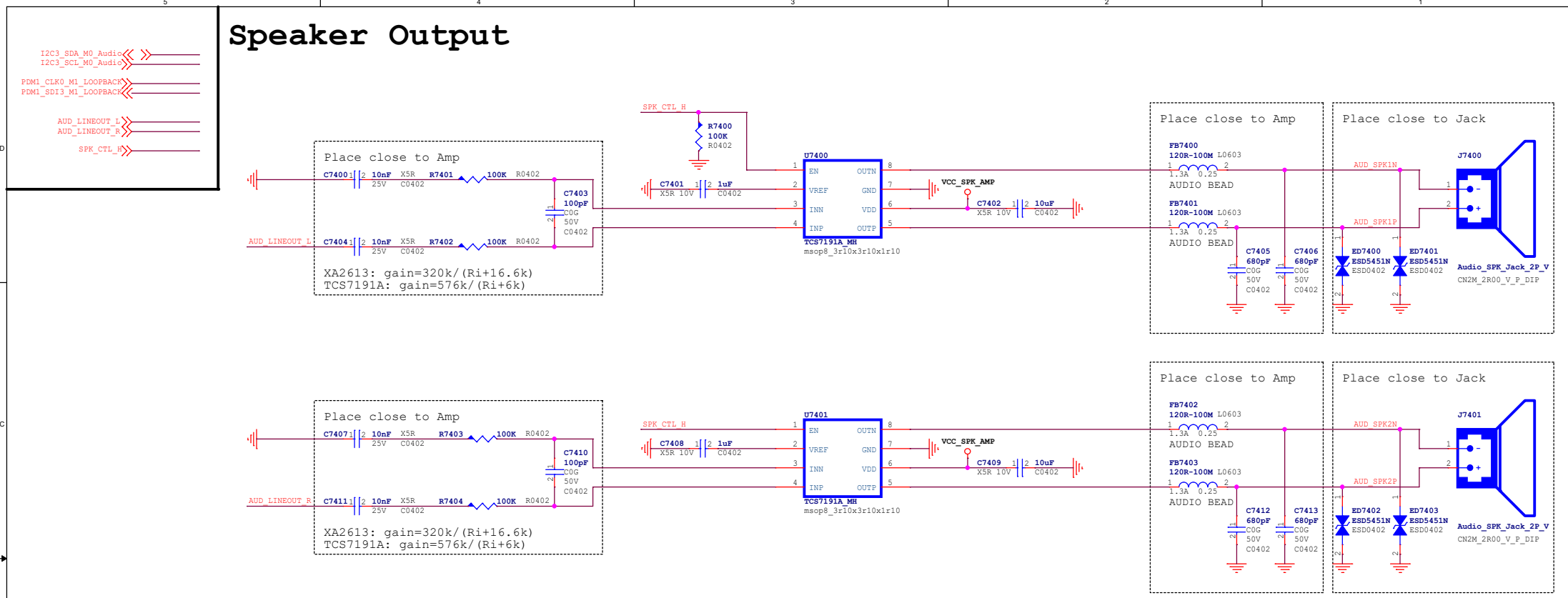
MIC



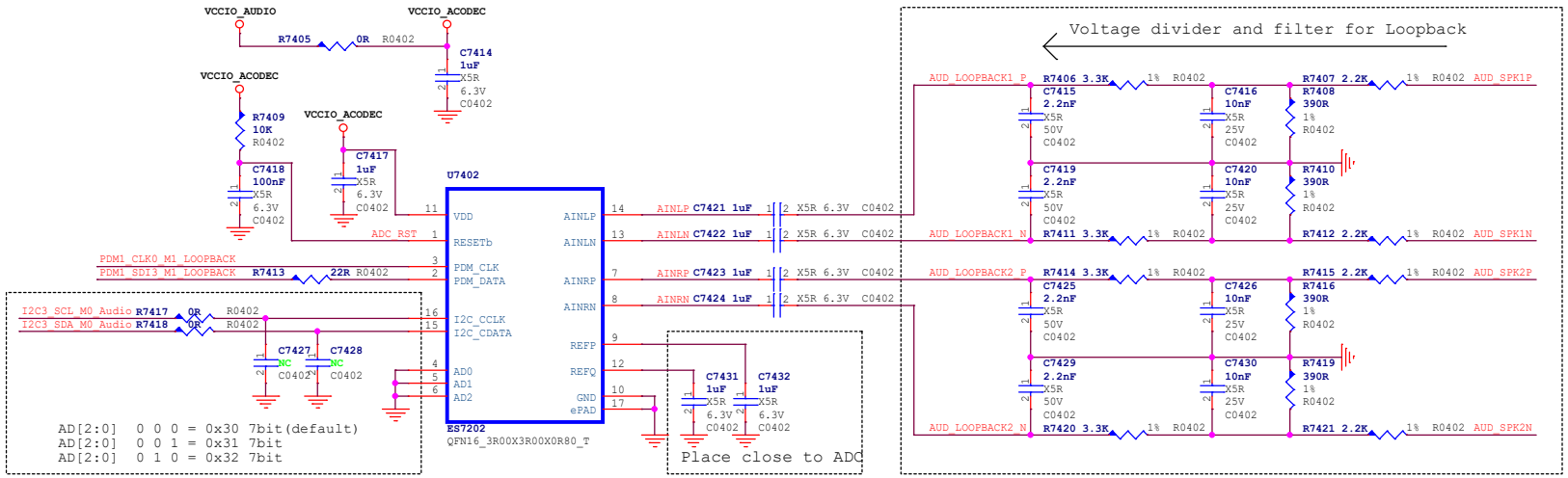
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	70.Audio-CODEC(ES8388)				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:		Sheet:	37 of 49

Speaker Output



Loopback for Dual Speakers

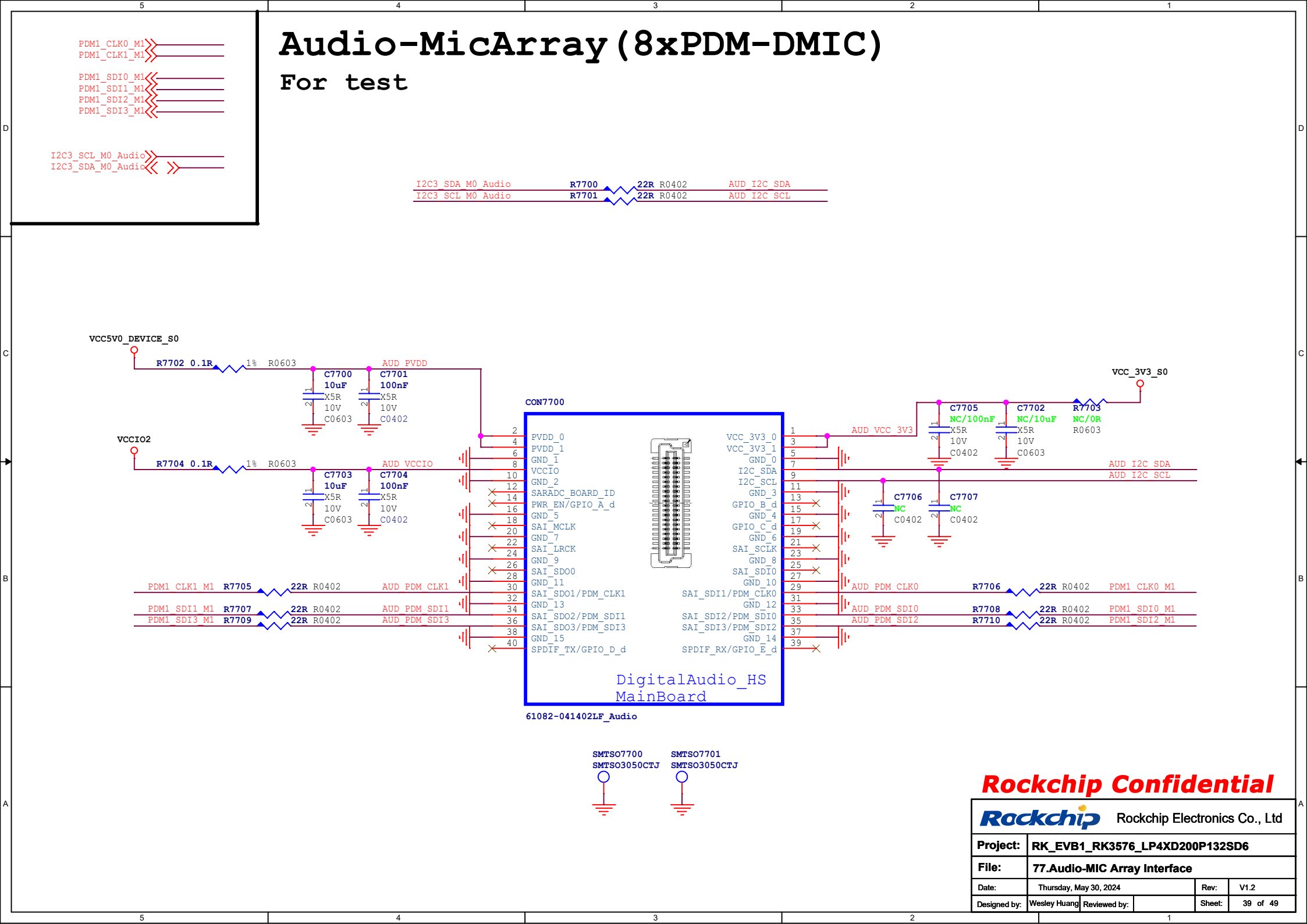


Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	74.Audio-SPK LoopBack		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang / Reviewed by:	Sheet:	38 of 49

Audio-MicArray(8xPDM-DMIC)

For test



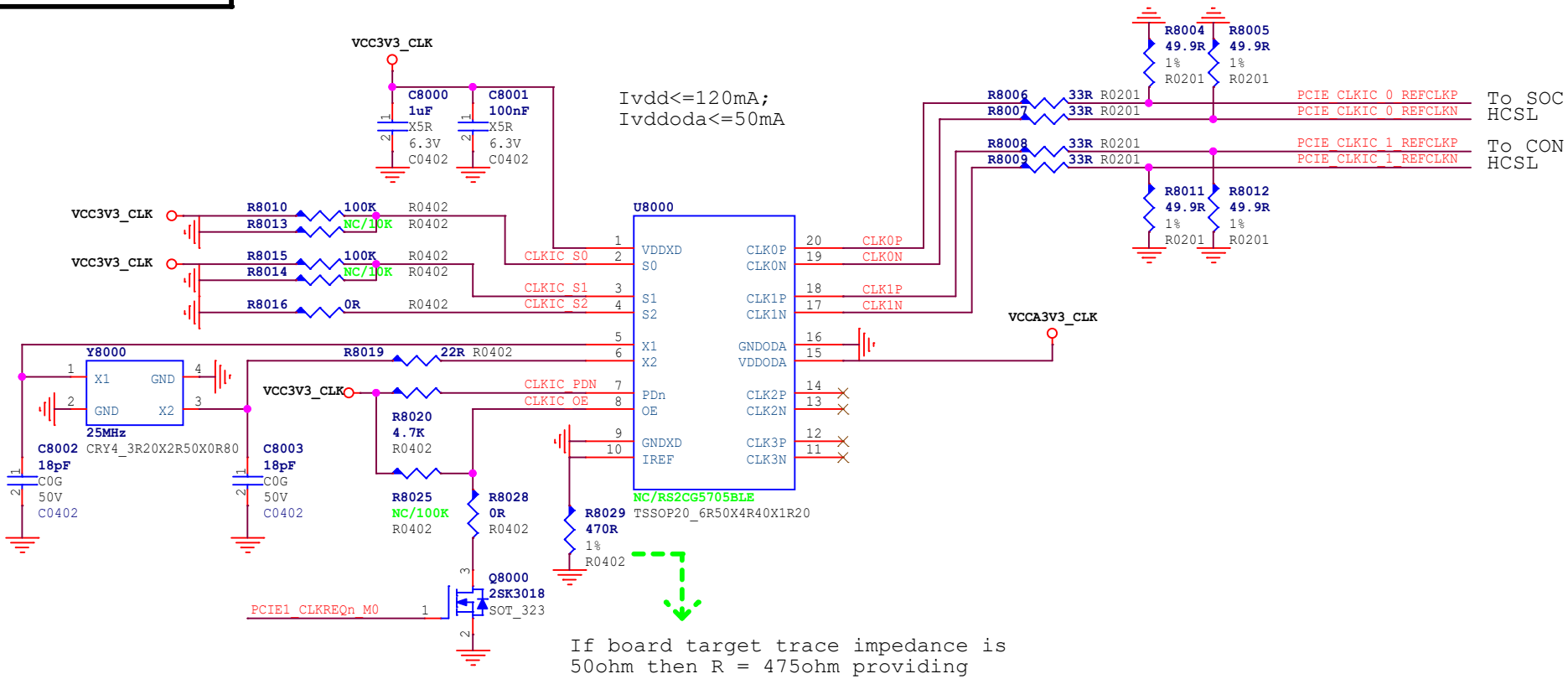
Rockchip Confidential

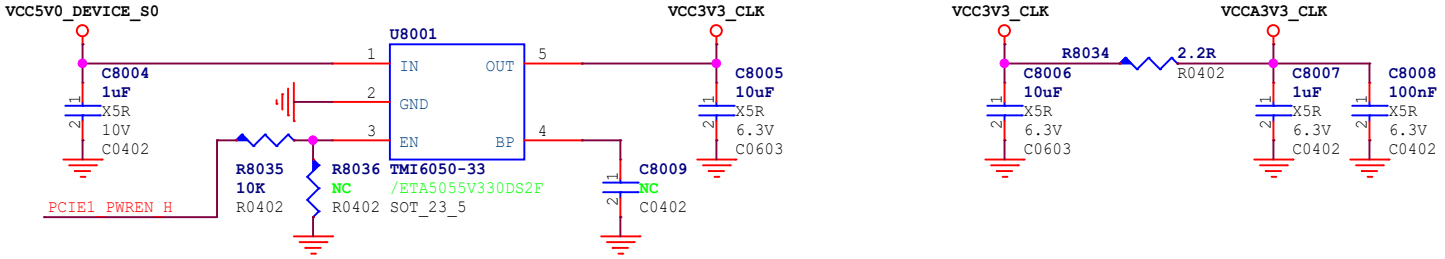
Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	77.Audio-MIC Array Interface		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by: Wesley Huang	Reviewed by:	Sheet:	39 of 49

PCIe Clock Generator

For test

PCIE_CLKIC_0_REFCLKP
PCIE_CLKIC_0_REFCLKN
PCIE_CLKIC_1_REFCLKP
PCIE_CLKIC_1_REFCLKN
PCIE1_CLKREQn_M0
PCIE1_PWREN_H



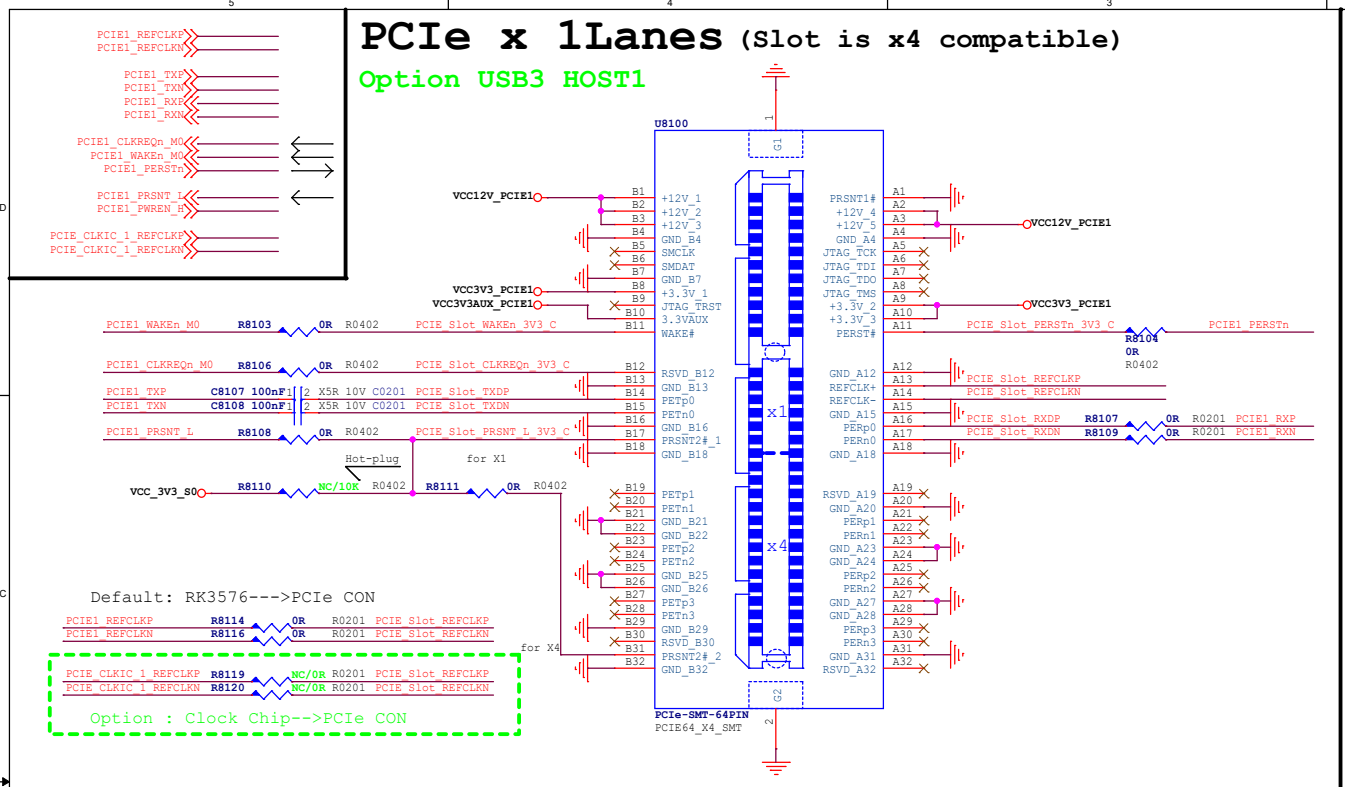


Rockchip Confidential

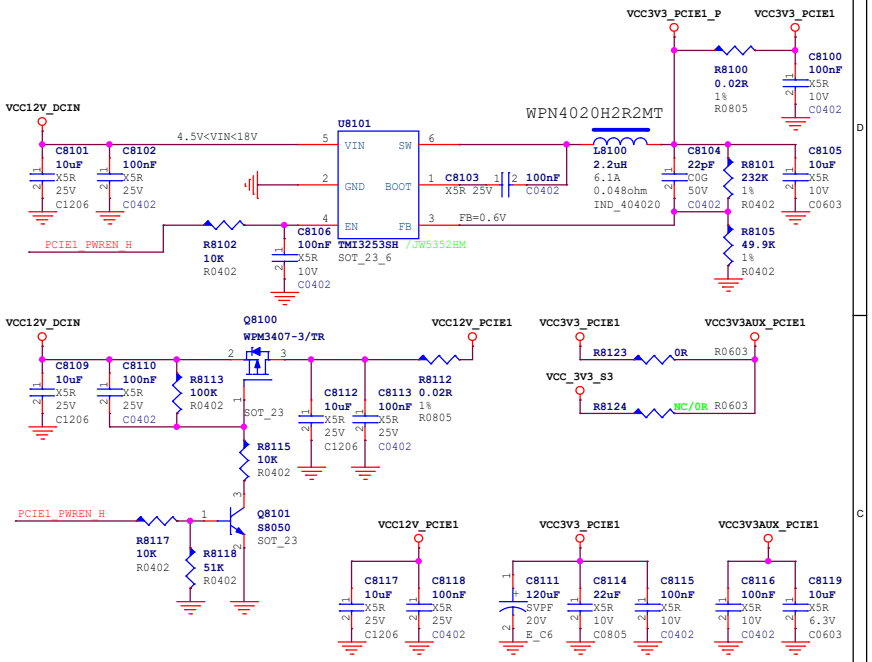
Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	80.PCIe-PCIe Clock Generator		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by: Wesley Huang	Reviewed by:	Sheet:	40 of 49

PCIe x 1Lanes (Slot is x4 compatible)

Option USB3 HOST1



(12V DC Power Supply is required)



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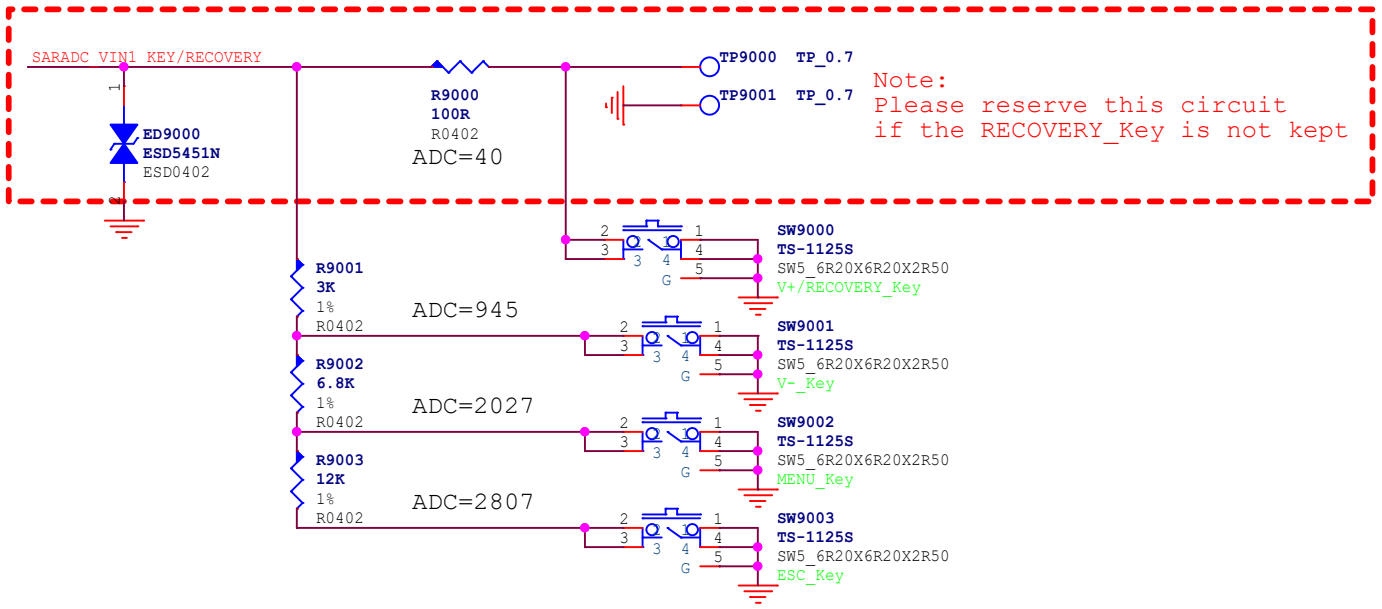
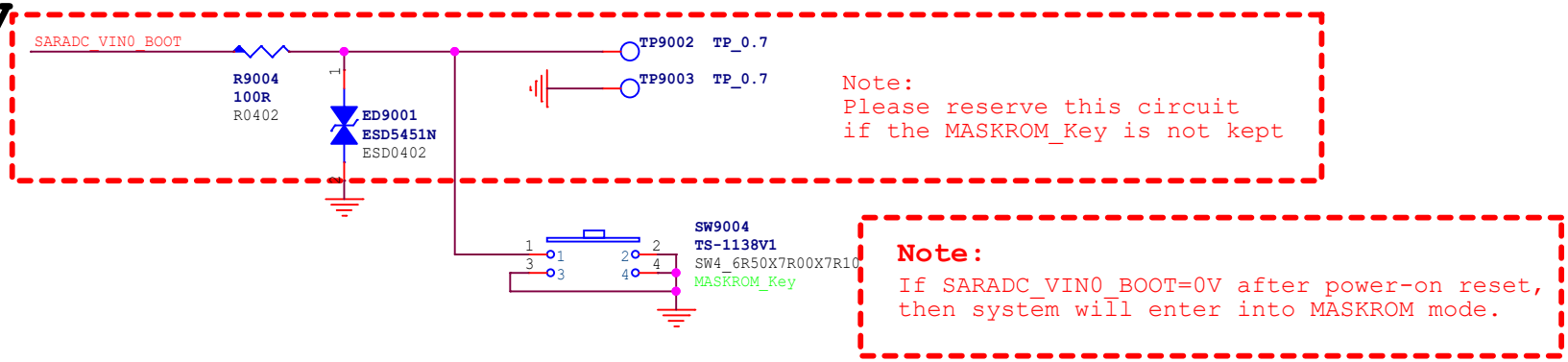
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	81.PCIe-PCIe Slot_1x1Lane_64P				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:		Sheet:	41 of 49

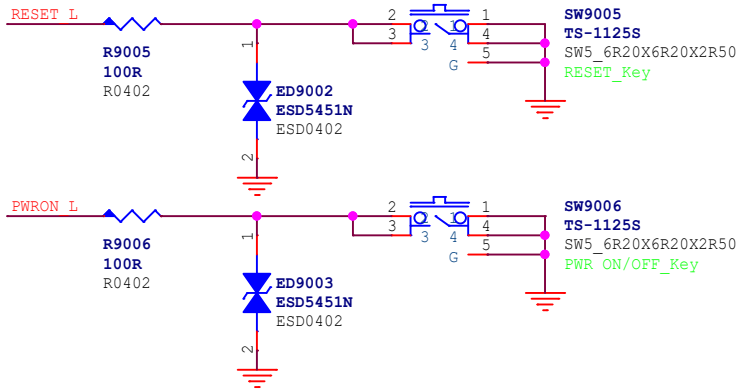
SARADC_VIN1_KEY/RECOVERY
RESET_L
PWRON_L
SARADC_VIN0_BOOT

KEY



MASKROM Key





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Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	90.Key-PowerON/Reset/V+/V-/etc		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by: Wesley Huang	Reviewed by:	Sheet:	42 of 49

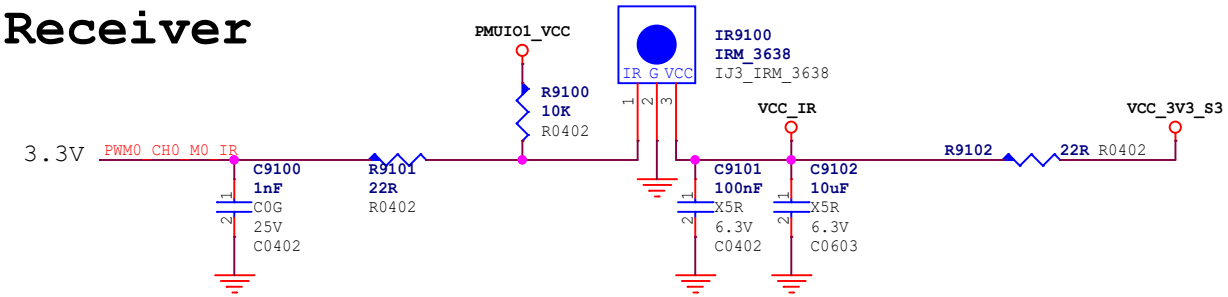
PWM0_CH0_M0_IR

I2C7_SCL_M1_Sensor

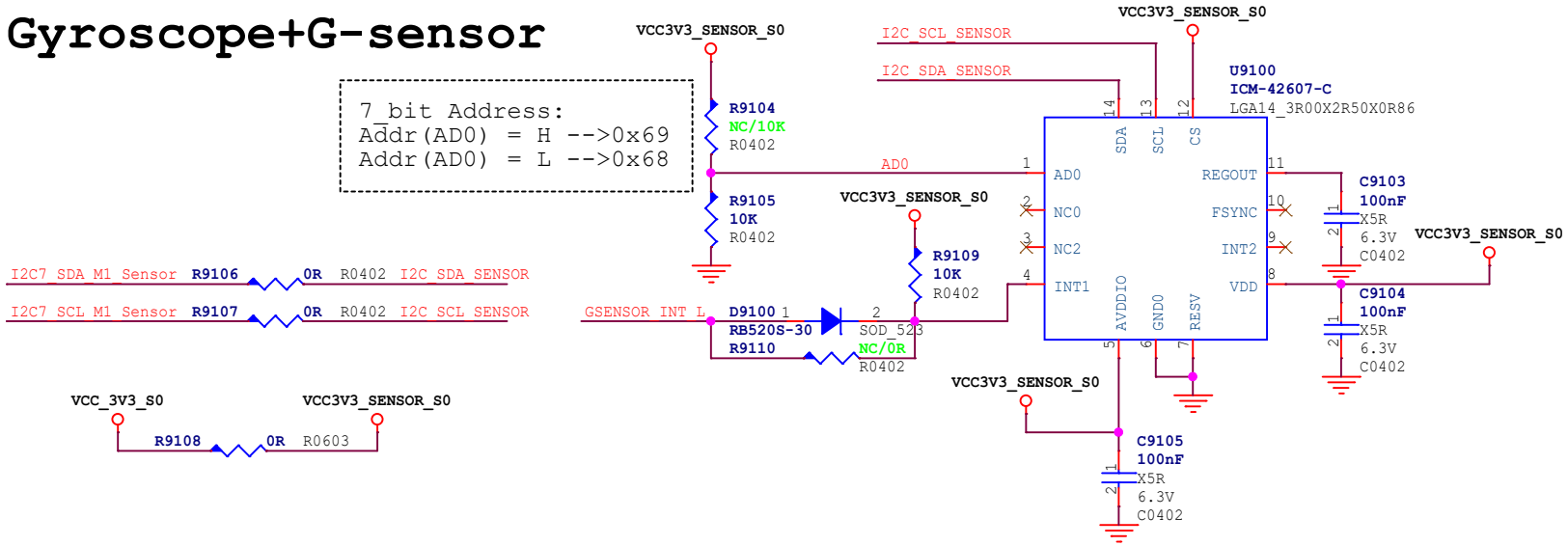
I2C7_SDA_M1_Sensor

GSENSOR_INT_L

IR Receiver



Gyroscope+G-sensor



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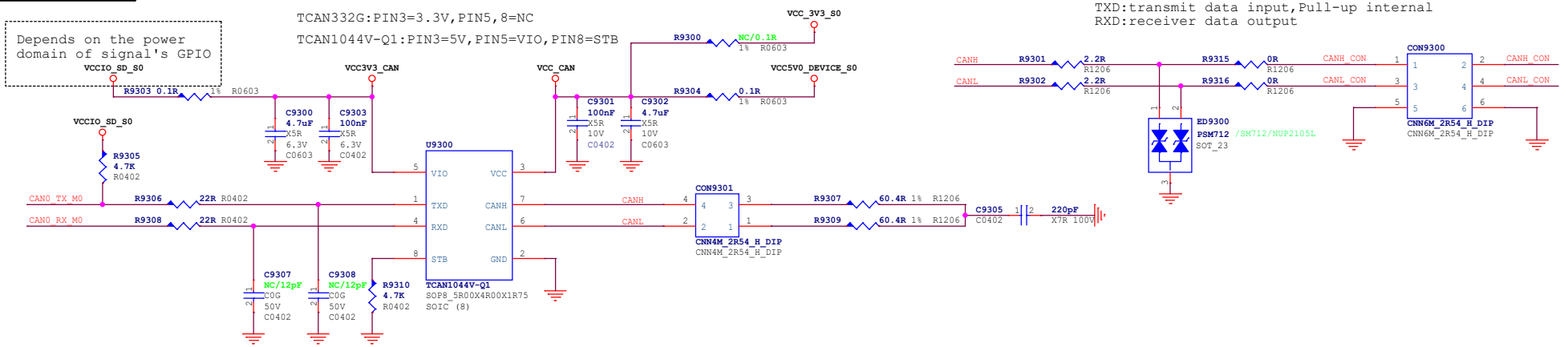
Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3576_LP4XD200P132SD6			
File:	91.Sensors/IR Receiver			
Date:	Thursday, May 30, 2024		Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet:	43 of 49

CAN

Functions only supported when there is
no MicroSD card function



TCAN1044V:
Vio:Support 1.8V,2.5V,3.3V,5V
Receiver common mode input
voltage:+/-12V;
Support of classical CAN and optimized
CAN FD performance at 2,5,and 8 Mbps.
Temperature grade:-40 to 125

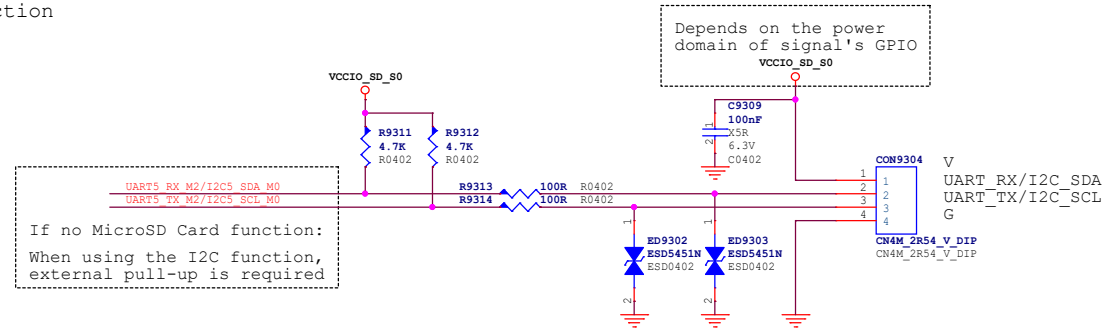
STB(Standby)
The STB pin is an input pin used for mode control of the transcervier.The STB pin can be supplied from either the system processor or from a static system voltage source,If normal mode is the only intended mode of operation than the STB pin can be tired directly to GND.

Table 5. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received See section 8.3.3.1
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

UART/I2C

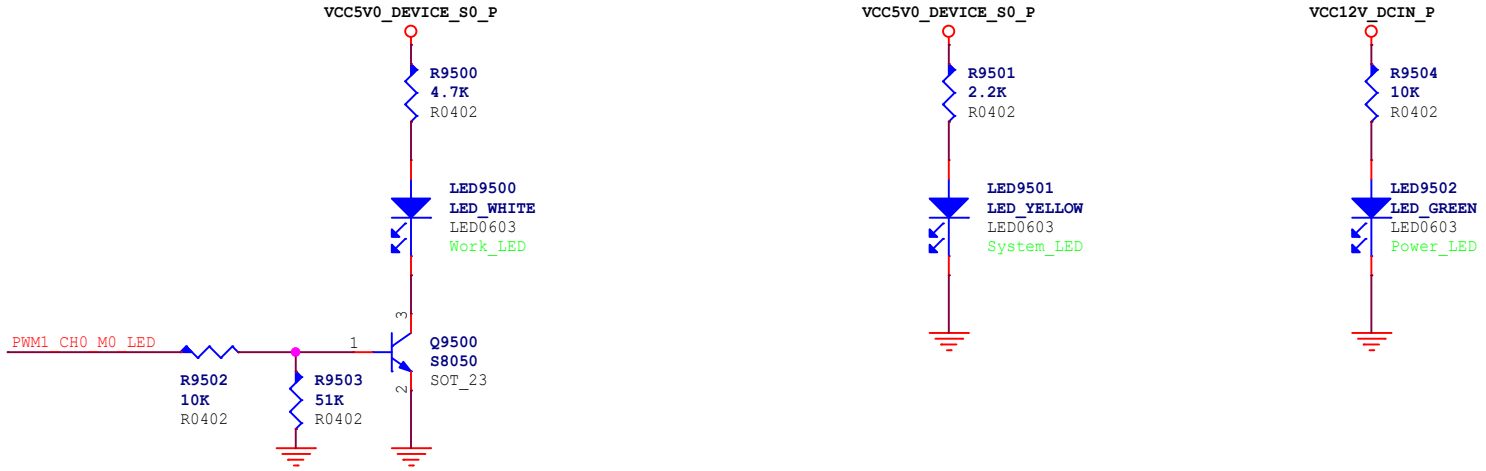
Functions only supported when there is
no MicroSD card function



Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	93.UART/CAN Port				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:		Sheet:	44 of 49

PWM1_CH0_M0_LED

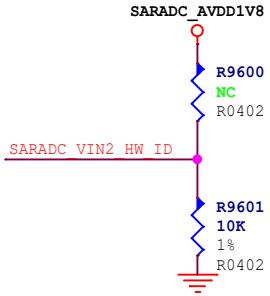
Work_LED



Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	95.LED		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by: Wesley Huang	Reviewed by:	Sheet:	45 of 49

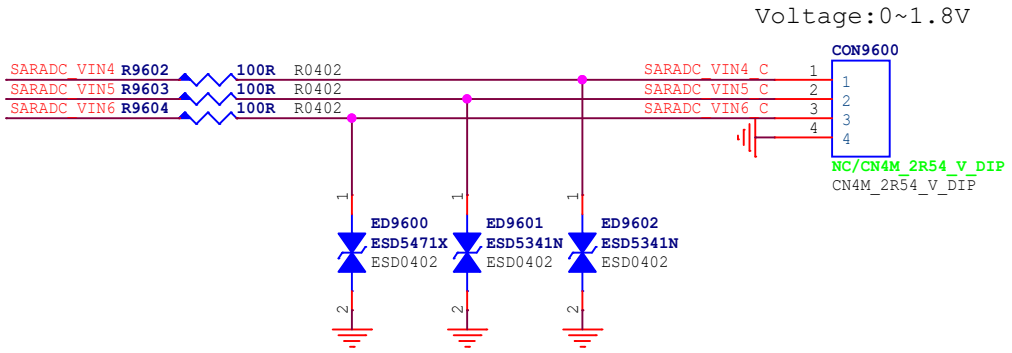
SARADC_VIN2_HW_ID
SARADC_VIN4
SARADC_VIN5
SARADC_VIN6

HW_ID



Config Table for SARADC_VIN2_HW_ID				
Item	**Rup**	**Rdown**	**ADC Value**	**VERSION**
HW_ID1	NC	10K	0	RK3576 EVB1 V12
HW_ID2	10K	1.13K	416	RESERVE
HW_ID3	10K	2.49K	816	RESERVE
HW_ID4	10K	4.3K	1231	RESERVE
HW_ID5	10K	6.8K	1658	RESERVE
HW_ID6	10K	10K	2048	RESERVE
HW_ID7	10K	14.7K	2437	RESERVE
HW_ID8	10K	23.2K	2862	RESERVE
HW_ID9	10K	40.2K	3279	RESERVE
HW_ID10	10K	88.7K	3680	RESERVE
HW_ID11	10K	NC	4095	RESERVE

SARADC PIN



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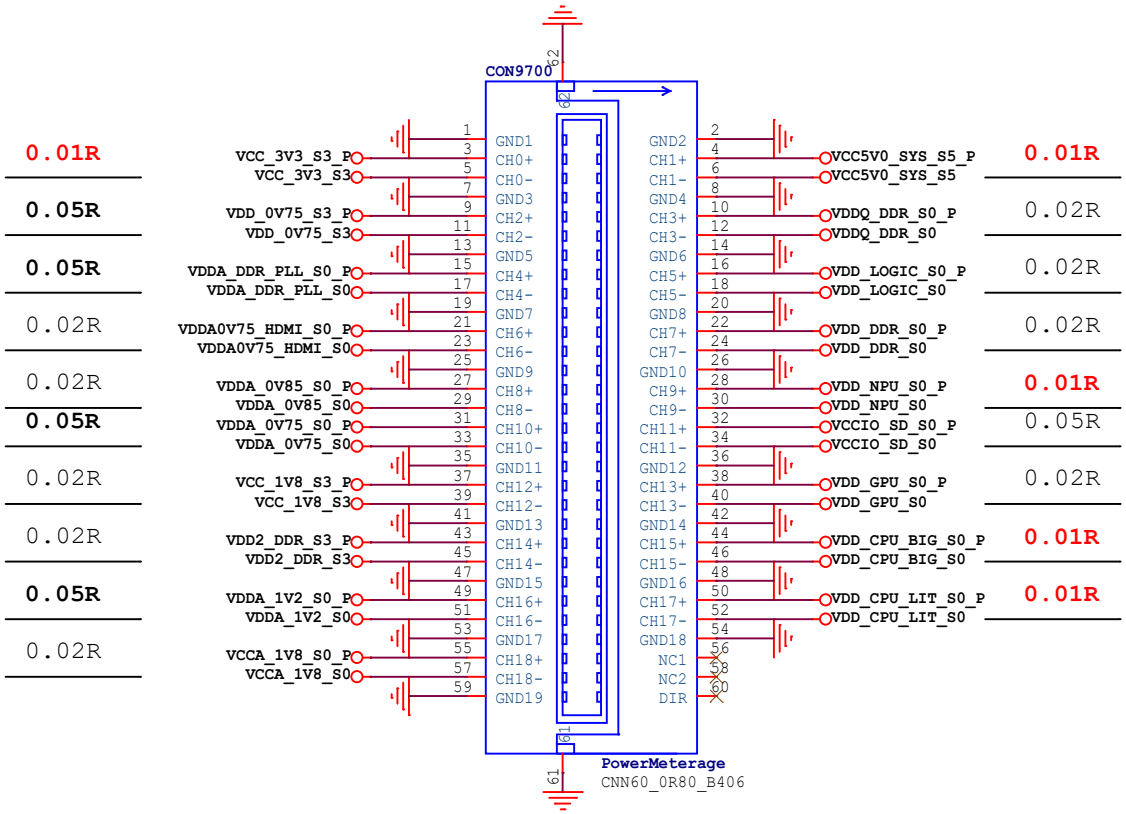
Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	96.HW_ID/BOM_ID		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang / Reviewed by:	Sheet:	46 of 49

Power-test

For test



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Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3576_LP4XD200P132SD6			
File:	97.Power Test			
Date:	Thursday, May 30, 2024		Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet:	47 of 49

Debug UART_M0

UART0_RX_M0_DEBUG
UART0_TX_M0_DEBUG
JTAG_TCK_M0
JTAG_TMS_M0

Option1

VCCIO_FT232
TP9800TP_0.7
R9800 10K R0402
UART0_RX_M0_DEBUG R9801 22R R0402
UART0_TX_M0_DEBUG D9800 RB520S-30 SOD_523
VCC_3V3_S3_P
VCCIO_FT232
TP9801TP_0.7
R9802 0.1R 1% R0603
C9800 1uF X5R 6.3V C0402
C9801 100nF X5R 6.3V C0402

U9800
FT232RL
SSOP28_10R20X5R30X2R00

LED9800 LED_BLUE R9803 2.2K R0402 LED0603
VCC5V_FT232_DEBUG
C9802 10uF X5R 10V C0603
C9803 100nF X5R 10V C0402
VCC3V3_FT232_DEBUG
C9804 100nF X5R 6.3V C0402

DEBUG_USBDM R9804 22R R0402 DEBUG_USBDM_C
DEBUG_USBDP R9805 22R R0402 DEBUG_USBDP_C

ED9800 ESD5341N ESD0402
ED9801 ESD5341N ESD0402

R9806 5.1K R0402
R9807 5.1K R0402

J9800
USB20_TYPE_C_NEW
TYPEC20_16P_U20401

Option2

It is recommended to reserve this circuit for debug of actual products

VCC_3V3_S3_P
C9850 100nF X5R 6.3V C0402
J9850
UART0_RX_M0_DEBUG R9950 100 R0402
UART0_TX_M0_DEBUG R9951 100 R0402
ED9850 ESD5451N ESD0402
ED9850 ESD5451N ESD0402
V RX TX G
CN4M_2R54_V
CN4M_2R54_V_P_DIP

JTAG_4pin_SWD

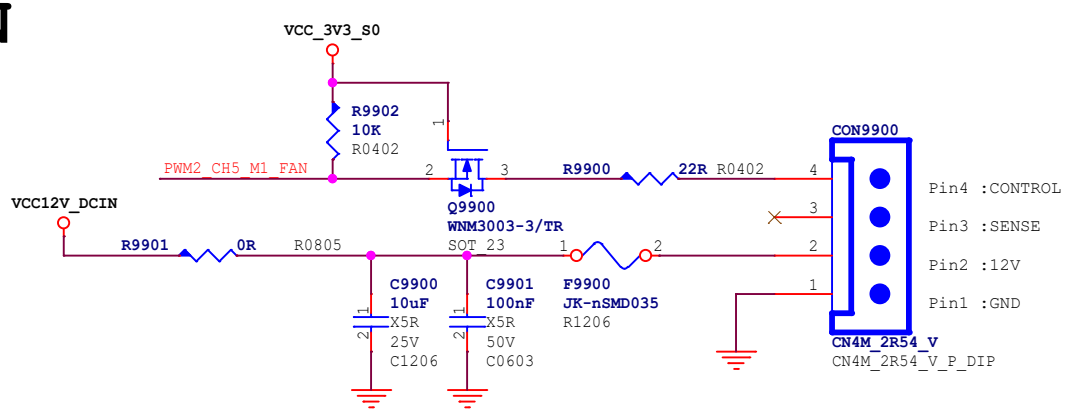
VCCIO_SD_S0
VCC_JTAG
R9808 0R R0402
VCCIO_SD_S0
VCC_3V3_S0
R9809 NC/0R R0402
C9805 100nF X5R 6.3V C0402
R9810 10K R0402
J9801
JTAG_TMS_M0
JTAG_TCK_M0
V TMS TCK G
CN4M_2R54_V_DIP
R9811 10K R0402
ED9802 ESD5451N ESD0402
ED9803 ESD5451N ESD0402

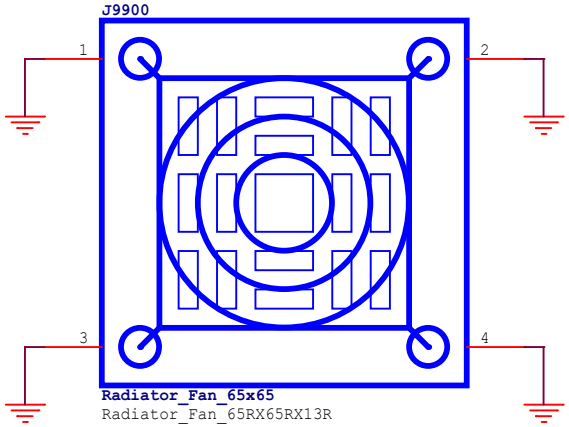
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	98.Debug UART/JTAG		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by: Wesley Huang	Reviewed by:	Sheet:	48 of 49

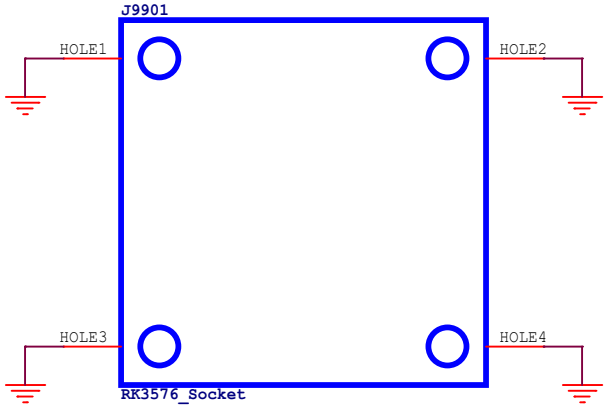
PWM2_CH5_M1_FAN

FAN

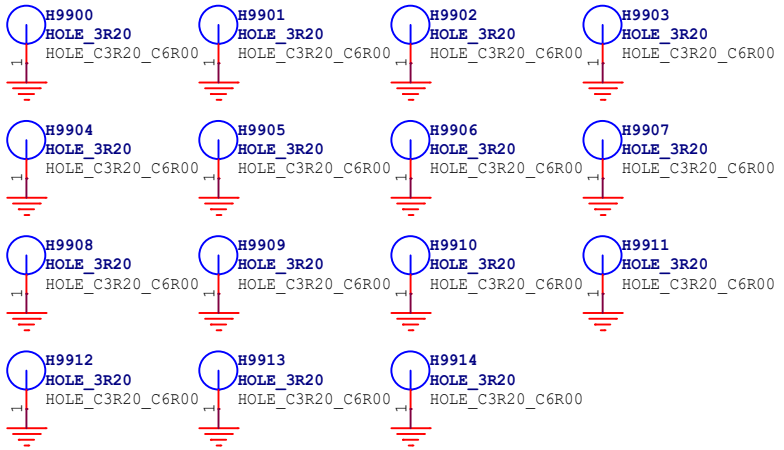




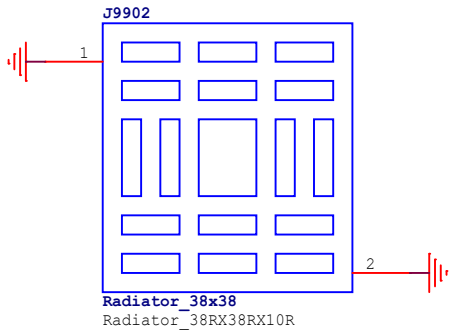
Socket



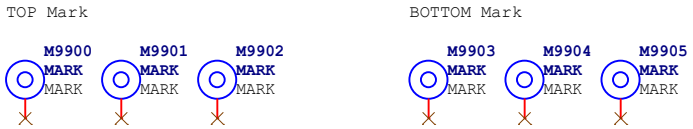
Hole



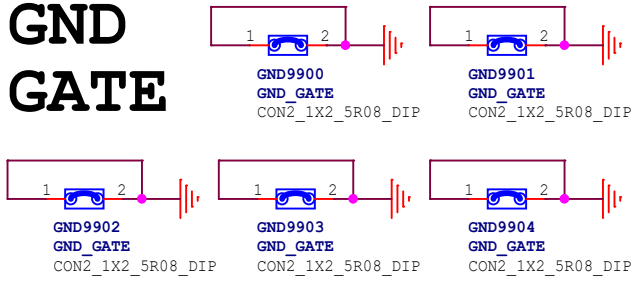
Heatsink



Mark



GND GATE



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Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	99.Mark/Hole/Heatsink		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet: 49 of 49