Rockchip RK628F Datasheet

Revision History

Date	Revision	Description
2024-07-02	1.1	Update the parameters in 3.1 Absolute Maximum Ratings and 3.2 Recommended Operating Condition
2023-12-26	1.0	Initial release

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Chapter 1 Introduction

RK628F is a high-integration interface chip, which can support HDMI/parallel RGB/BT.1120 as input and dual MIPI/dual LVDS/GVI(general video interface)/parallel RGB/BT.1120 as output with featured scaler inside. The key application scenario is extension of display output port for original application processor such as RK3288/RK3399/RK3588, or HDMI in interface providing.

1.1 Features
1.1.1 Video input interface
- HDMI RX interface
  - Compliant with HDMI 1.4/HDMI 2.0
  - Supports HDCP 1.4
  - Supports 8/10bit per component video format
  - Supports rgb888/yuv444/yuv422/yuv420
  - Supports Max resolution 4096x2160@60fps
  - Supports data rates up to 600Mhz, with PHY bit rate 6Gbps per lane
  - Supports DDC Bus I2C master interface at 3.3/5V
  - Supports EDID and CEC function
  - Supports DVI
- Parallel IN interface
  - Supports Max resolution 1080p@60fps
  - Supports 16bits BT.1120 in
  - Supports 24bits parallel RGB in

Table 1-1 RK628F video input interface

Interface	Resolution	Data rate	Bit rate per lane
HDMI	4096x2160@60	NA	6Gbps
BT.1120	1080p@60fps	148.5M	NA
RGB	1080p@60fps	148.5M	NA

1.1.2 Video output interface
- HDMI TX interface
  - Supports all DTV resolutions including 480p/720p /1080p
  - Supports data rate from 25MHz to 148.5MHZ
  - TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
  - DDC Bus I2C master interface at 3.3/5V
  - The EDID and CEC function are also supported by HDMI Transmitter Controller
- MIPI TX interface
  - DSI
    - ◆ Compliant with MIPI DPHY V1.2
    - ◆ Support the DPI interface color coding mappings into 24-bit Interface
    - ◆ Up to 4 D-PHY Data Lanes per channel
    - ◆ Supports data rate up to 1.3Gbps
    - ◆ Supports dual channel DSI
  - CSI
    - ◆ Compliant with MIPI DPHY V1.2
    - ◆ Support format: YUV422
    - ◆ Up to 4 D-PHY Data Lanes
    - ◆ Supports data rate up to 1.3Gbps
    - ◆ Supports dual channel CSI
- GVI TX interface
  - Supports RGB666/RGB888/RGB101010/YUV422-8bit/YUV422-10bit format
  - Supports Max resolution 4096x2160@60fps
  - Supports up to 3.75Gbps data rate (effective data rate 3Gbps)
  - Supports 1/2/4/8 lanes

- ■ Supports output lanes flexible mapping
- ■ Supports 1/2 section mode
- ● LVDS TX interface
  - ■ Compliant with the Standard TIA/EIA-644-A LVDS standard
  - ■ Supports data rate up to 1Gbps
  - ■ Support 8bit format-1, format-2, format-3 display mode, Support 6bit display mode.
  - ■ Supports dual channel LVDS
- ● Parallel Video Out interface
  - ■ Supports Max resolution 1080p@60fps
  - ■ Supports 16bits BT.1120 out
  - ■ Supports 24bits parallel RGB out

Table 1-2 RK628F video output interface

Interface	Resolution	Data rate	Bit rate per lane
GVI	4096x2160@60fps	NA	3.75Gbps
Dual MIPI DSI	2560x1600@60fps	NA	1.3Gbps
MIPI DSI	1080p@60fps	NA	1.3Gbps
Dual MIPI CSI	3840x2160@60fps	NA	1.3Gbps
MIPI CSI	3840x2160@30fps	NA	1.3Gbps
Dual LVDS	1080p@60fps	NA	1 Gbps
LVDS	720p@60fps	NA	1 Gbps
BT.1120	1080p@60fps	148.5M	NA
RGB	1080p@60fps	148.5M	NA
HDMI	1080p@60fps	148.5M	NA

1.1.3 TX/RX adapter
- ● Interaction of HDP signal between HDMI TX and HDMI RX
- ● Support HDMI TX CEC function
- ● Support RX HDCP1.4 inside-key memory. It is readable and writable
- ● Support HDMI RX/TX
- ● Support on-chip EDID memory. It is readable and writable
1.1.4 Post process
- ● CSC
  - ■ RGB2YUV
  - ■ YUV2RGB
  - ■ YUV2VYU
  - ■ CSC matrix
- ● Display interface
  - ■ Parallel display Interface: 30-bit(RGB/YUV)
  - ■ Asynchronous output pixel clock (PLL required)
  - ■ Flexible display timing setting
  - ■ Configurable border black area
- ● Scaling down
  - ■ Max input resolution: 4096x2160
  - ■ Arbitrary non-integer scaling ratio
  - ■ Support two mode: bilinear and average
  - ■ Max 1/4 scaling ratio for bilinear scaling down
  - ■ Max 1/6 scaling ratio for average scaling down
- ● Scaling up
  - ■ Max output resolution: 4096x2160
  - ■ Arbitrary non-integer scaling ratio
  - ■ Support four scaling up mode for different effect
  - ■ Max 6 scaling ratio
- ● Split
  - ■ Left-right mode
  - ■ Odd-even mode

1.1.5 Others

- Audio
  - Support HDMI RX I2S interface, up to 192kHz sample rate, 8 channel
  - Support I/O I2S interface, 8 channel
  - Support HDMI TX I2S interface, 8 channel
  - Support the connection of RX and TX's I2S
- PWM
  - Single channel PWM output supported
- Package Type
  - FBGA144L (body:8mm x 8mm ;ball size: 0.3mm ;ball pitch: 0.65)

1.2 Block Diagram

The following figure shows the basic block diagram of RK628F.

Fig. 1-1 RK628F Block Diagram

Chapter 2 Package Information

2.1 Order Information

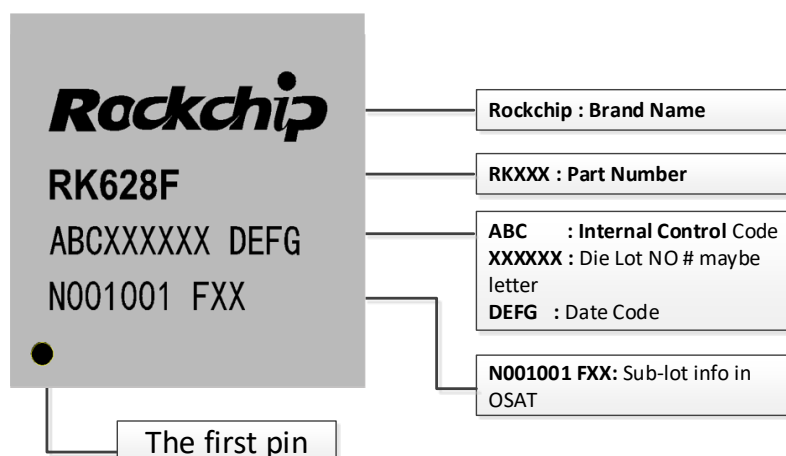| Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK628F	RoHS	FBGA144L	3480PCS	High speed interface bridge chip

2.2 Top Marking

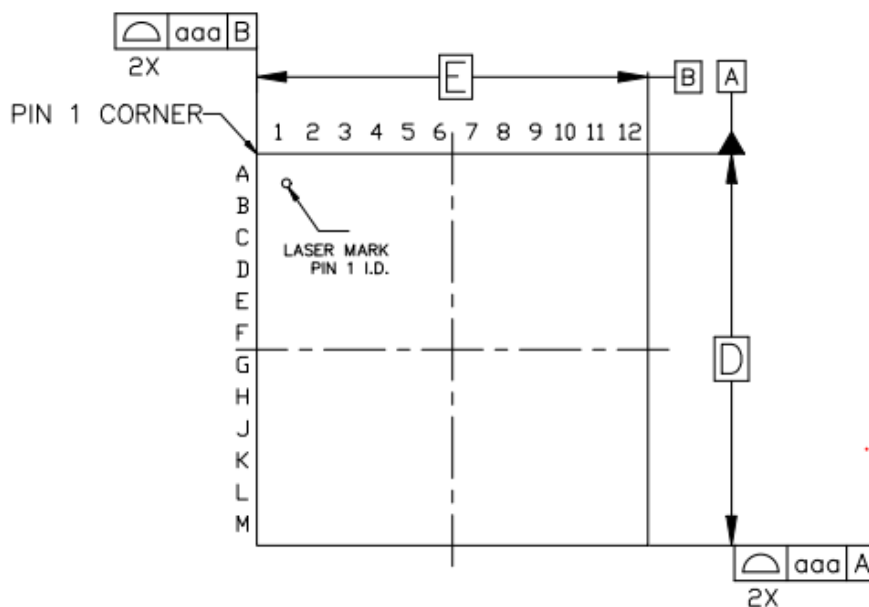Fig. 2-1 RK628F Package Definition

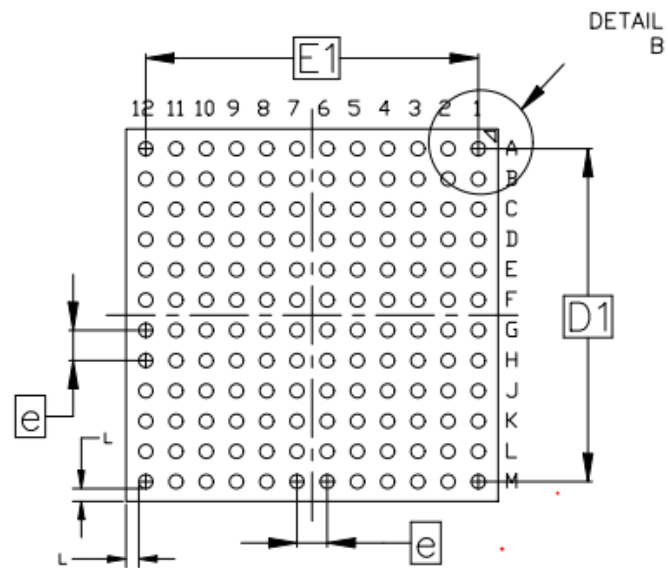## 2.3 Package Dimension

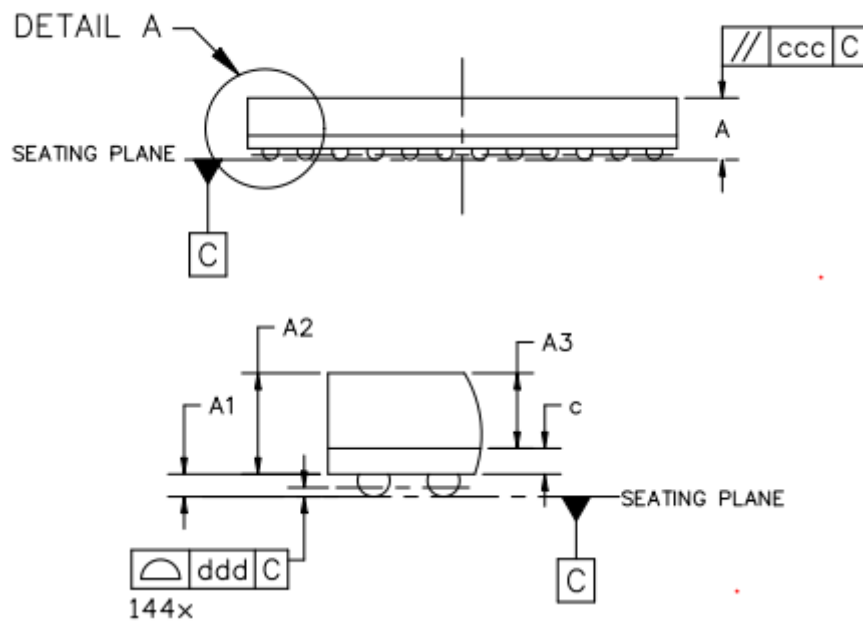Fig. 2-2 RK628F Package Top View

Fig. 2-3 RK628F Package Bottom View

Fig. 2-4 RK628F Package Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	––	1.15	1.23
A1	0.16	0.21	0.26
A2	0.89	0.94	0.99
A3	0.70 BASIC		
c	0.20	0.24	0.28
D	7.90	8.00	8.10
D1	7.15 BASIC		
E	7.90	8.00	8.10
E1	7.15 BASIC		
e	0.65 BASIC		
b	0.25	0.30	0.35
L	0.275 REF		
aaa	0.15		
ccc	0.08		
ddd	0.08		
eee	0.15		
fff	0.08		

Fig. 2-5 RK628F Package Dimension

2.4 MSL Information

Moisture sensitivity Level ：MSL3

2.5 Lead Finish/Ball Material Information

Lead Finish/Ball material ：SnAgCu

2.6 Pin Number Order

Table 2-1 RK628F WBBGA144 Pin Number Order Information

Pin Number	Pin Name	Pin Number	Pin Name
A1	VSS_1	G1	GVI/LVDS/MIPI_TX0N
A2	GVI/LVDS/MIPI_TX5P	G2	GVI/LVDS/MIPI_TX0P
A3	GVI/LVDS/MIPI_TX6P	G3	VSS_25
A4	GVI/LVDS/MIPI_TX7P	G4	VSS_19
A5	GVI/LVDS/MIPI_TX8P	G5	VSS_9
A6	GVI/LVDS/MIPI_TX9P	G6	VSS_13
A7	GPIO3_B1/GVI_HPD	G7	VSS_16
A8	GPIO3_A1/VOP_HSYNC	G8	VSS_20
A9	VOP_DCLK	G9	HDMIRX_EXTR
A10	GPIO2_C4/VOP_D20/JTAGTDI	G10	GPIO2_A0/VOP_D0
A11	GPIO2_C1/VOP_D17/XIPSFCMISO	G11	GPIO2_A1/VOP_D1
A12	VSS_2	G12	GPIO2_A2/VOP_D2
B1	GVI/LVDS/MIPI_REXT	H1	GPIO0_A7/I2S_D3_M0/UARTTRTSN
B2	GVI/LVDS/MIPI_TX5N	H2	GPIO0_A6/I2S_D2_M0/UARTCTSN
B3	GVI/LVDS/MIPI_TX6N	H3	GPIO0_A5/I2S_D1_M0/UARTRX
B4	GVI/LVDS/MIPI_TX7N	H4	RESETN
B5	GVI/LVDS/MIPI_TX8N	H5	VCCIO1
B6	GVI/LVDS/MIPI_TX9N	H6	VSS_29
B7	GPIO3_B2/GVI_LOCK	H7	GPIO1_A0/TEST_CLKO

Pin Number	Pin Name	Pin Number	Pin Name
B8	GPIO3_A3/VOP_VSYNC	H8	GPIO1_A1/SFC_CSLK
B9	GPIO3_A0/VOP_DEN	H9	HDMIRX_DVDD_1V1_1
B10	GPIO2_C3/VOP_D19/JTAGTDO	H10	VSS_18
B11	GPIO2_C0/VOP_D16/XIPSFCCSN	H11	HDMIRX_D2N
B12	GPIO2_B7/VOP_D15	H12	HDMIRX_D2P
C1	GVI/LVDS/MIPI_TX4N	J1	GPIO0_A3/I2S_LRCK_M0
C2	GVI/LVDS/MIPI_TX4P	J2	GPIO0_A2/I2S_SCK_M0
C3	GVI/LVDS/MIPI_PLL_AVDD_3V3	J3	INT/SPIBOOT
C4	VSS_26	J4	HDMITX_DVDD_1V1_2
C5	GVI/LVDS/MIPI_AVDD_1V1_3	J5	HDMITX_DVDD_1V1_3
C6	VSS_27	J6	HDMITX_DVDD_1V1_1
C7	I2C_ADDR	J7	PLL_AVDD_1V1
C8	GPIO2_C7/VOP_D23/JTAGTRSN	J8	GND30
C9	GPIO2_C6/VOP_D22/JTAGTCK	J9	HDMIRX_DVDD_1V1_2
C10	GPIO2_C2/VOP_D18/XIPSFCMOSI	J10	HDMIRX_AVDD_3V3_1
C11	GPIO2_B4/VOP_D12	J11	HDMIRX_D1N
C12	GPIO2_B6/VOP_D14	J12	HDMIRX_D1P
D1	GVI/LVDS/MIPI_TX3N	K1	GPIO0_B1/HDMITX_SDA
D2	GVI/LVDS/MIPI_TX3P	K2	GPIO0_A4/I2S_D0_M0/UARTTX
D3	VSS_5	K3	I2C_SDA
D4	GVI/LVDS/MIPI_AVDD_1V1_1	K4	HDMITX_AVDD_3V3
D5	GVI/LVDS/MIPI_AVDD_3V3_1	K5	VSS_7
D6	VSS_24	K6	VSS_22
D7	TEST	K7	VSS_10
D8	DVDD_2	K8	GPIO1_B0/HDMIRX_HPD_M0
D9	GPIO2_C5/VOP_D21/JTAGTMS	K9	GPIO1_B3/HDMIRX_CEC_M0
D10	GPIO2_B2/VOP_D10	K10	VSS_23
D11	GPIO2_B3/VOP_D11	K11	HDMIRX_D0N
D12	GPIO2_B5/VOP_D13	K12	HDMIRX_D0P
E1	GVI/LVDS/MIPI_TX2N	L1	GPIO0_B2/HDMITX_SCL
E2	GVI/LVDS/MIPI_TX2P	L2	GPIO0_B0/HDMITX_HPD
E3	GVI/LVDS/MIPI_AVDD_1V1_2	L3	I2C_SCL
E4	GVI/LVDS/MIPI_AVDD_3V3_2	L4	HDMITX_CLKN
E5	VSS_11	L5	HDMITX_D0N
E6	VSS_14	L6	HDMITX_D1N
E7	VSS_28	L7	HDMITX_D2N
E8	VCCIO2_1	L8	GPIO1_B2/HDMIRX_SCL_M0
E9	DVDD_1	L9	OSC_OUT
E10	GPIO2_A7/VOP_D7	L10	VSS_28
E11	GPIO2_B1/VOP_D9	L11	HDMIRX_CLKN
E12	GPIO2_B0/VOP_D8	L12	HDMIRX_CLKP
F1	GVI/LVDS/MIPI_TX1N	M1	VSS_4
F2	GVI/LVDS/MIPI_TX1P	M2	GPIO0_B3/HDMITX_CEC
F3	GVI/LVDS/MIPI_AVDD_1V1_4	M3	HDMITX_EXTR
F4	VSS_6	M4	HDMITX_CLKP
F5	VSS_8	M5	HDMITX_D0P
F6	VSS_12	M6	HDMITX_D1P
F7	VSS_15	M7	HDMITX_D2P
F8	VCCIO2_2	M8	GPIO1_B1/HDMIRX_SDA_M0
F9	GPIO2_A3/VOP_D3	M9	OSC_IN
F10	GPIO2_A6/VOP_D6	M10	PLL_AVDD
F11	GPIO2_A5/VOP_D5	M11	VSS_29
F12	GPIO2_A4/VOP_D4	M12	VSS_3

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 RK628F Absolute Maximum Ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for internal digital logic@1.1v	DVDD_1,DVDD_2	1.32	V
DC supply voltage for digital GPIO@1.8V mode	VCCIO2_1 VCCIO2_2	1.98 1.98	V
DC supply voltage for digital GPIO@3.3V mode	VCCIO1 VCCIO2_1 VCCIO2_2	3.63 3.63 3.63	V
DC supply voltage for HDMI RX	HDMIRX_AVDD_3V3 HDMIRX_DVDD_1V1	3.63 1.32	V
DC supply voltage for GVI/LVDS/MIPI TX	GVI/LVDS/MIPI_PLL_AVDD_3V3 GVI/LVDS/MIPI_AVDD_3V3 GVI/LVDS/MIPI_AVDD_1V1	3.63 3.63 1.32	V
DC supply voltage for HDMI TX	HDMITX_DVDD_1V1 HDMITX_AVDD_3V3	1.32 3.63	V
DC supply voltage for PLL	PLL_AVDD_1V1 PLL_AVDD_3V3	1.32 3.63	V
Storage Temperature	Tstg	125	℃
Max Conjunction Temperature	Tj	125	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

The following table describes the recommended operating conditions.

Table 3-2 RK628F Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
DC supply voltage for internal digital logic@1.1v	DVDD_1,DVDD_2	0.99	1.1	1.21	V
DC supply voltage for digital GPIO@1.8V mode	VCCIO2_1 VCCIO2_2	1.71 1.71	1.8 1.8	1.89 1.89	V
DC supply voltage for digital GPIO@3.3V mode	VCCIO1 VCCIO2_1 VCCIO2_2	3.135 3.135 3.135	3.3 3.3 3.3	3.465 3.465 3.465	V
DC supply voltage for HDMI RX	HDMIRX_AVDD_3V3 HDMIRX_DVDD_1V1	3.135 0.99	3.3 1.1	3.465 1.21	V
DC supply voltage for GVI/LVDS/MIPI TX	GVI/LVDS/MIPI_PLL_AVDD_3V3 GVI/LVDS/MIPI_AVDD_3V3 GVI/LVDS/MIPI_AVDD_1V1	3.135 3.135 0.99	3.3 3.3 1.1	3.465 3.465 1.21	V
DC supply voltage for HDMI TX	HDMITX_AVDD_3V3 HDMITX_DVDD_1V1	3.135 0.99	3.3 1.1	3.465 1.21	V
DC supply voltage for PLL	PLL_AVDD_3V3 PLL_AVDD_1V1	3.135 0.99	3.3 1.1	3.465 1.21	V
PLL input clock frequency		N/A	24	N/A	MHz
Operating Temperature		-20	25	80	℃

3.3 DC Characteristics

Table 3-3 RK628F DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V for GPIO0/1/2/3	Input Low Voltage	Vil	-0.3	0	0.8	V
	Input High Voltage	Vih	2.0	3.3	3.465	V
	Output Low Voltage	Vol	NA	0	0.4	V
	Output High Voltage	Voh	2.4	3.3	NA	V
	Threshold Point	Vtr+	1	1.16	1.34	V

	Parameters	Symbol	Min	Typ	Max	Units
		Vtr-	1.02	1.19	1.39	V
	Pullup Resistor	Rpu	26	46	71	Kohm
	Pulldown Resistor	Rpd	27	48	102	Kohm
Digital GPIO @1.8V for GPIO0/1/2/3	Input Low Voltage	Vil	-0.3	0	0.58	V
	Input High Voltage	Vih	1.27	1.8	3.15	V
	Output Low Voltage	Vol	NA	0	0.45	V
	Output High Voltage	Voh	1.40	1.8	NA	V
	Threshold Point	Vtr+	0.9	0.95	1.01	V
		Vtr-	0.91	0.97	1.03	V
	Pullup Resistor	Rpu	/	50	/	Kohm
	Pulldown Resistor	Rpd	/	50	/	Kohm

3.4 Recommended Operating Frequency

Table 3-4 RK628F Recommended Operating Frequency

Parameter	Condition	Symbol	Min	Typ	Max	Unit
CPLL	1.1V , 25 ℃	cpll	270	1188	1600	MHz
	1.21V , -40 ℃		270	1188	1600	
	0.99V , 125 ℃		270	1188	1600	
GPLL	1.1V , 25 ℃	gpll	270	984	1600	MHz
	1.21V , -40 ℃		270	984	1600	
	0.99V , 125 ℃		270	984	1600	
APLL	1.1V , 25 ℃	apll	270	984	1600	MHz
	1.21V , -40 ℃		270	984	1600	
	0.99V , 125 ℃		270	984	1600	
HDMI RX CTRL	1.1V , 25 ℃	dclk_rx	13.5	594	600	MHz
	1.21V , -40 ℃		13.5	594	600	
	0.99V , 125 ℃		13.5	594	600	
Process	1.1V , 25 ℃	Sclk	13.5	594	600	MHz
	1.21V , -40 ℃		13.5	594	600	
	0.99V , 125 ℃		13.5	594	600	

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	θ_{JA}	42.36	(℃/W)
Junction-to-board thermal resistance	θ_{JB}	18.52	(℃/W)
Junction-to-case thermal resistance	θ_{JB}	20.51	(℃/W)

Note: The testing PCB is 4 layers, 114.3mmx101.6mm, *1.6mm thickness, Ambient temperature is 25℃.*