

RK3576_AIOT_REF_SCH_V11

Modify_Notes_CN

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更新记录

修订记录累积了每次文档更新的说明，最新版本的文档包含以前所有文档版本的更新内容。

版本	修改人	修改日期	修改说明	备注
V1.0	Wesley Huang	2024.03.22	First edition for RK3576	
V1.1	Wesley Huang	2024.05.30	具体修改记录请见下面内容。	

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1 原理图版本说明

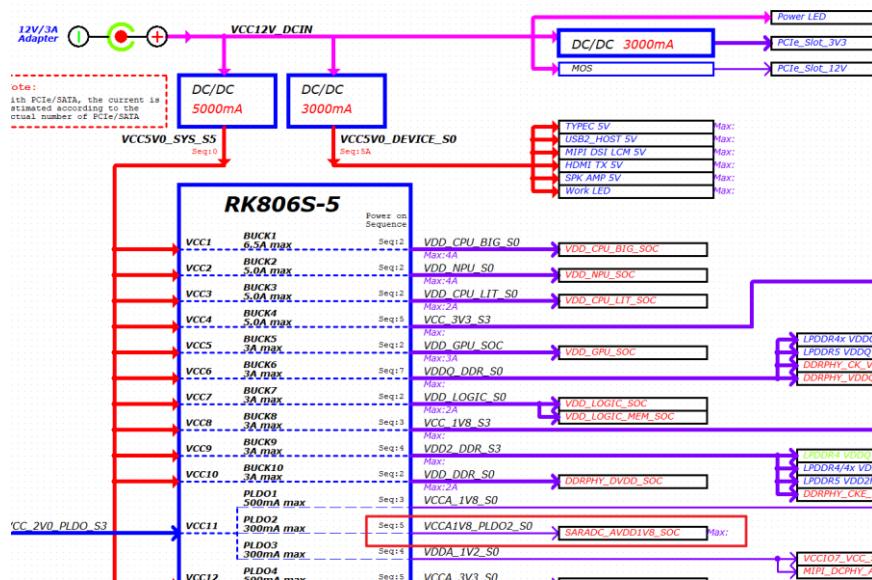
基于《RK3576_AIOT_REF_SCH_V10_20240322.DSN》版本上更新修改。
最新版本为《RK3576_AIOT_REF_SCH_V10_20240530.DSN》

2 最新V1.1版本原理图及PCB修改内容说明

2.1 Page 5--04.Power Tree

根据 SOC 的时序要求, PMIC 的 PLDO2 时序修改为 5, 用于给 SARADC_AVDD1V8 供电, **请务必更新。**

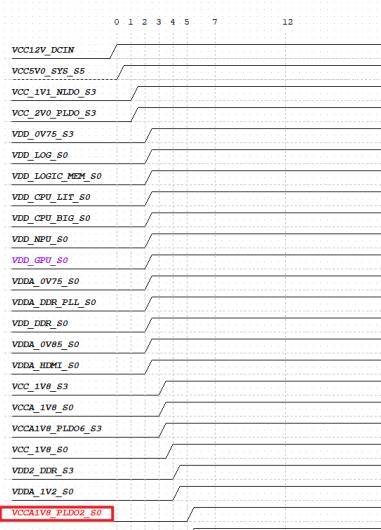
Default Power Tree



2.2 Page 6-- 05.Power Sequence and Map

根据 SOC 的时序要求, PMIC 的 PLDO2 时序修改为 5, **请务必更新。**

Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Name	Power Shot	Time	Default Voltage	Default On/Off	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot#2	0.85V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	RK806_BUCK2	3A	VDD_NPU_S0	Slot#2	0.85V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	RK806_BUCK3	5.0A	VDD_CPU_LIT_S0	Slot#2	0.85V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot#3	3.3V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot#4	1.8V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQD_DDR_S0	Slot#4	1.8V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDDQD_DDR_S0	Slot#4	1.8V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot#3	1.8V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot#4	1.8V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot#4	1.8V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	RK806_PLDO1	0.5A	VCCA1V8_PLDO2_S0	Slot#5	1.8V	ON	DVS	TBD	TBD	
VCC12V_PLDO_S3	RK806_PLDO2	0.3A	VDDA1V2_S0	Slot#5	1.8V	ON	DVS	TBD	TBD	
VCC12V_PLDO_S3	RK806_PLDO3	0.3A	VDDA1V2_S0	Slot#5	1.8V	ON	DVS	TBD	TBD	
VCC12V_PLDO_S3	RK806_PLDO4	0.3A	VCC1V8_SD_S0	Slot#5	3.0V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot#3	1.8V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	RK806_NLD01	0.3A	VDD_0V75_S3	Slot#2	0.75V	ON	DVS	TBD	TBD	
VCC1V8_NLU_S3	RK806_NLD02	0.3A	VDDA1V2_NLU_S0	Slot#2	0.85V	ON	DVS	TBD	TBD	
VCC1V8_NLU_S3	RK806_NLD04	0.3A	VDDA1V2_NLU_S0	Slot#2	0.85V	ON	DVS	TBD	TBD	
VCC1V8_NLU_S3	RK806_NLD05	0.3A	VDDA1V2_NLU_S0	Slot#2	0.75V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	EXT_BUCK	2A	VDD2_0V9_DOR_S3	Slot#5A	0.9V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	EXT_BUCK	2A	VCC_2V0_PLDO_S3	Slot#2	2.1V	ON	DVS	TBD	TBD	
VCC5V0_SYS_S5	EXT_BUCK	2A	VCC_1V8_NLU_S3	Slot#2	1.1V	ON	DVS	TBD	TBD	
VCC12V_OCN	EXT_BUCK	5A	VCC5V0_SYS_S5	Slot#5A	5.0V	ON	DVS	TBD	TBD	
VCC12V_OCN	EXT_BUCK	5A	VCC5V0_DEVICE_S0	Slot#5A	5.2V	ON	DVS	TBD	TBD	
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot#3A	3.3V	ON	DVS	TBD	TBD	
VCC_1V8_S0	SWITCH	2A	VCC_1V8_S0	Slot#3A	1.8V	ON	DVS	TBD	TBD	

Note:
The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

Peripherals:
Peripherals connected to the GPIO of SOC need to be powered on during sleeping.
It is recommended to power on both the Peripherals and the SOC's GPIO power supply simultaneously.

IO Power Domain Map

ID	Domain	Pin Num	Support IO Voltage	Supply Pin Name	Power Source	Operating Voltage
PMU009	Pin 2K11	1	1.8V Only	PW100L_VCC1V8	VCC_1V8	1.8V
PMU010	Pin 1020	1	1.8V or 2.3V	PW101L_VCC	VCC_1V8	2.3V
VCC100	Pin 1200	1	1.8V Only	VCC100_VCC1V8	VCC_1V8	1.8V
VCC101	Pin 2A#	1	1.8V or 2.3V	VCC101_VCC	VCC_1V8	1.8V/2.3V
VCC102	Pin 2A#	2	1.8V or 2.3V	VCC102_VCC	VCC_1V8	2.3V
VCC103	Pin 2B#	1	1.8V or 2.3V	VCC103_VCC	VCC_1V8	1.8V
VCC104	Pin 2A#	1	1.8V or 2.3V	VCC104_VCC	VCC_1V8	2.3V
VCC105	Pin 2A#	2	1.8V or 2.3V	VCC105_VCC	VCC_1V8	1.8V
VCC106	Pin 2M#	1	1.8V or 2.3V	VCC106_VCC	VCC_1V8	2.3V
VCC107	Pin 2H3	1	1.8V or 2.3V	VCC107_VCC	VCC_1V8	1.8V



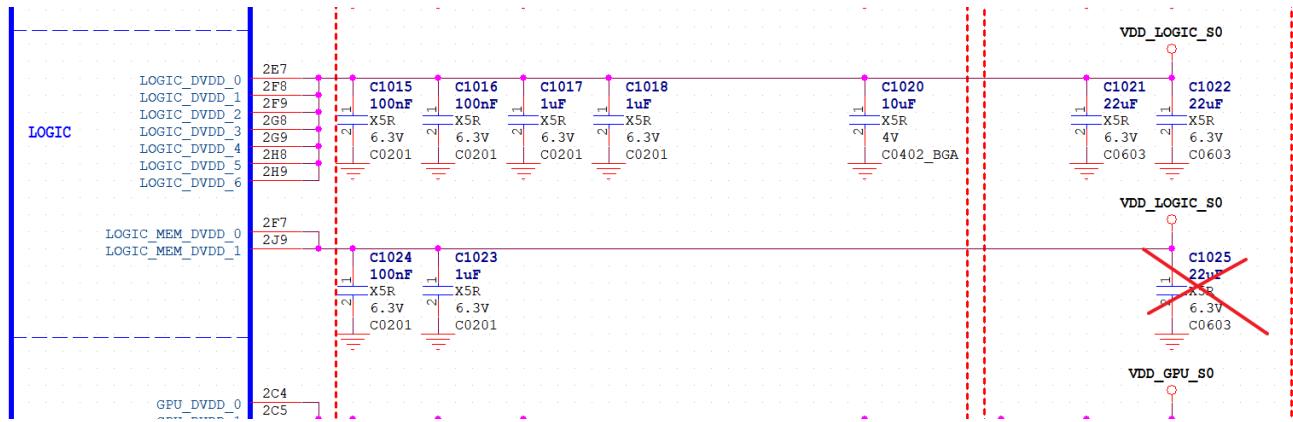
2.3 Page 10~Page 19

RK3576 量产芯片的厚度变薄 0.1mm，相应 PCB 封装名修改为 BGA698_16R1X17R2X1R08

	Name	Number	Option	Optional	OriginalSymbolOrigin	Part Reference	Part Type	Part Number	PARTS	Pc	PCB Footprint	Pd
1	RK_EVB1_RK3576_LP	IN50202990				MIC700	IC				A_MCU_128PQFN28V1R10	
2	RK_EVB1_RK3576_LP	IN502037949				AM76400	RF Jack				ANT_SMA_ST_EMI	
3	RK_EVB1_RK3576_LP	IN502037771				AM76401	RF Jack				ANT_SMA_ST_EMI	
4	RK_EVB1_RK3576_LP	IN50222381				AM76402	ANT				ANT_JACK	
5	RK_EVB1_RK3576_LP	IN51204631				J2400					BAT_CRI220	
6	RK_EVB1_RK3576_LP	IN53068541				U4000B	NAND_FLASH				BGA153_16R1X17R2X1R08_2L	
7	RK_EVB1_RK3576_LP	IN530685478				U4000A	NAND_FLASH				BGA153_16R1X17R2X1R08_2L	
8	RK_EVB1_RK3576_LP	IN53125692				U2800B					BGA200_16R0X16R0X20R0	
9	RK_EVB1_RK3576_LP	IN53125674				U2800A					BGA200_16R0X16R0X20R0	
10	RK_EVB1_RK3576_LP	IN531224157				U1000Q	SOC				BGA698_16R1X17R2X1R08	
11	RK_EVB1_RK3576_LP	IN531224450				U1000N	SOC				BGA698_16R1X17R2X1R08	
12	RK_EVB1_RK3576_LP	IN531236239				U1000R	SOC				BGA698_16R1X17R2X1R08	
13	RK_EVB1_RK3576_LP	IN531236492				U1000F	SOC				BGA698_16R1X17R2X1R08	
14	RK_EVB1_RK3576_LP	IN531245910				U1000G	SOC				BGA698_16R1X17R2X1R08	
15	RK_EVB1_RK3576_LP	IN531245728				U1000J	SOC				BGA698_16R1X17R2X1R08	
16	RK_EVB1_RK3576_LP	IN531247180				U1000O	SOC				BGA698_16R1X17R2X1R08	
17	RK_EVB1_RK3576_LP	IN531247014				U1000I	SOC				BGA698_16R1X17R2X1R08	
18	RK_EVB1_RK3576_LP	IN531236779				U1000E	SOC				BGA698_16R1X17R2X1R08	
19	RK_EVB1_RK3576_LP	IN531234806				U1000S	SOC				BGA698_16R1X17R2X1R08	
20	RK_EVB1_RK3576_LP	IN531241147				U1000D	SOC				BGA698_16R1X17R2X1R08	
21	RK_EVB1_RK3576_LP	IN531234595				U1000V	SOC				BGA698_16R1X17R2X1R08	
22	RK_EVB1_RK3576_LP	IN531234604				U1000T	SOC				BGA698_16R1X17R2X1R08	
23	RK_EVB1_RK3576_LP	IN531233793				U1000U	SOC				BGA698_16R1X17R2X1R08	
24	RK_EVB1_RK3576_LP	IN531243320				U1000P	SOC				BGA698_16R1X17R2X1R08	
25	RK_EVB1_RK3576_LP	IN531242537				U1000L	SOC				BGA698_16R1X17R2X1R08	
26	RK_EVB1_RK3576_LP	IN531238478				U1000A	SOC				BGA698_16R1X17R2X1R08	
27	RK_EVB1_RK3576_LP	IN531242491				U1000B	SOC				BGA698_16R1X17R2X1R08	
28	RK_EVB1_RK3576_LP	IN531240611				U1000K	SOC				BGA698_16R1X17R2X1R08	
29	RK_EVB1_RK3576_LP	IN531242247				U1000M	SOC				BGA698_16R1X17R2X1R08	
30	RK_EVB1_RK3576_LP	IN531247109				U1000H	SOC				BGA698_16R1X17R2X1R08	
31	RK_EVB1_RK3576_LP	IN531240832				U1000C	SOC				BGA698_16R1X17R2X1R08	
32	RK_EVB1_RK3576_LP	IN531257802				C3833	-一般用片封装陶瓷音				C0201	
33	RK_EVB1_RK3576_LP	IN531257894				C3837	-一般用片封装陶瓷音				C0201	
34	RK_EVB1_RK3576_LP	IN531257390				C3826	-一般用片封装陶瓷音				C0201	

2.4 Page 11-- 10.RK3576-Power/GND

删除 C1025

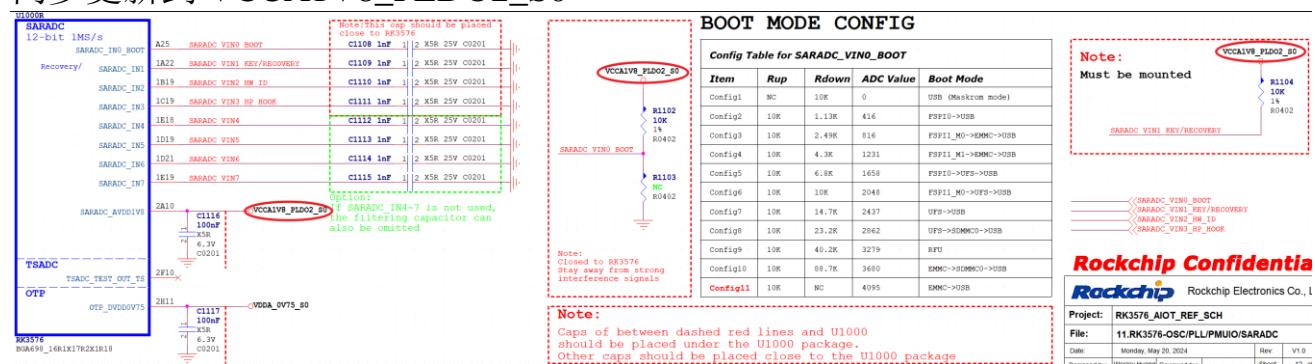


2.5 Page 12--11.RK3576-OSC/PLL/PMUIO/SARADC

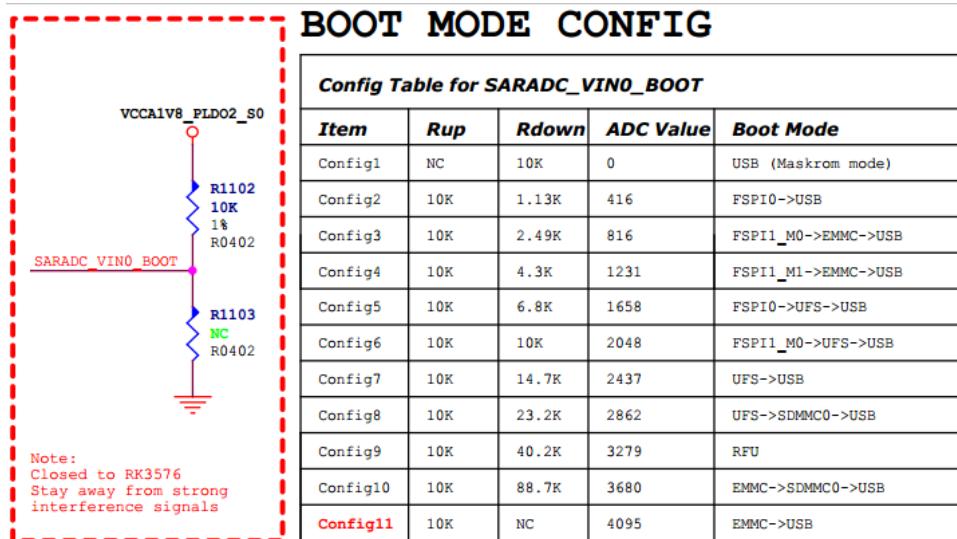
(1) SARADC/OTP 修改

根据 SOC 的时序要求，SARADC/OTP 的供电时序需要改为 5，因此

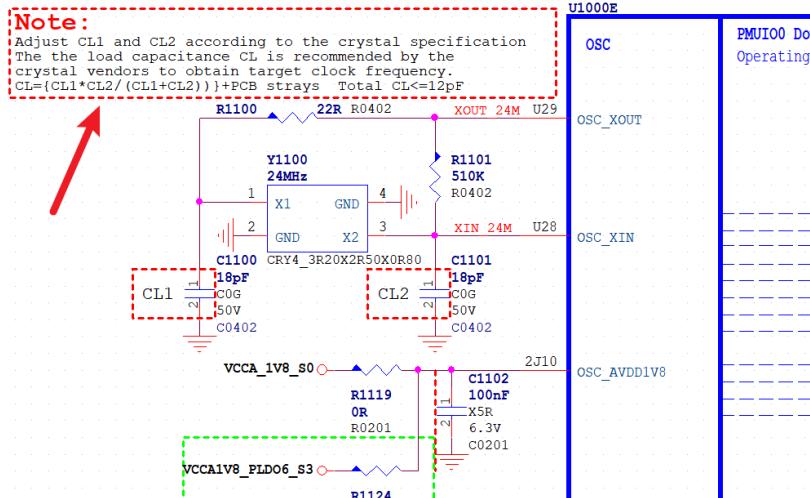
SARADC/OTP 的供电引脚 SARADC_AVDD1V8 改用 RK806S-5 的 PLDO2 电源 VCCA1V8_PLDO2_S0(时序改为 5)来单独供电，SARADC 的相关上拉电源需要同步更新到 VCCA1V8_PLDO2_S0



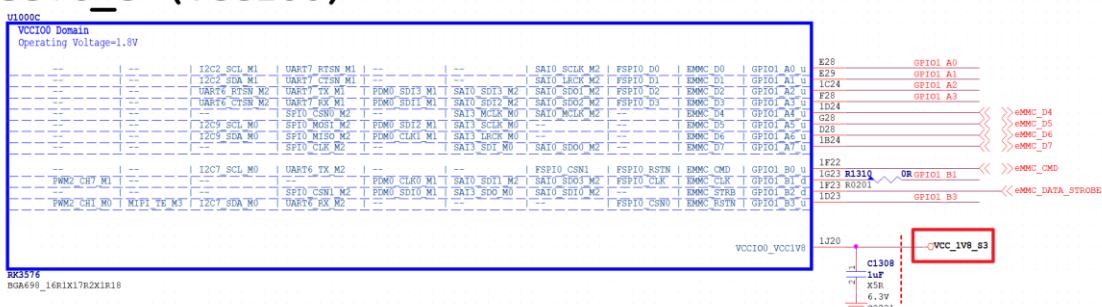
(2) SARADC_VIN0_BOOT 配置的电阻阻值等比例缩小，以增强抗干扰能力



(3) 增加系统OSC的负载电容要求文字说明：

RK3576_E (PMUIO0/1)**2.6 Page 14--13.RK3576-eMMC/UFS/SD**

针对待机功耗要求不高的项目，可以将EMMC的VCCIO0电源域供电改为待机常供电VCC_1V8_S3，也就是EMMC待机常供电，此时系统的VCC_1V8_S0供电可不需要采用带放电电阻的load switch(详见2.7 Page 23--24.Power-Ext Discrete/RTC IC)。如果待机功耗要求较高，比如带电池的产品—平板和电子书等，建议EMMC待机时下电来减少功耗，此时需要采用带放电电阻的load switch。

RK3576_C (VCCIO0)

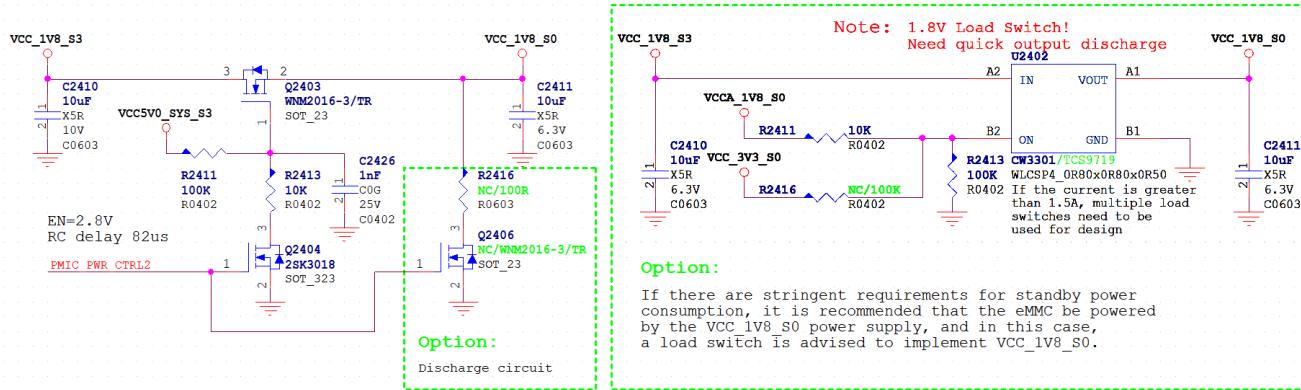
2.7 Page 23--24.Power-Ext Discrete/RTC IC

1.8V的带放电电阻的load switch成本较高。

针对待机功耗要求不高时，EMMC待机时可不下电，此时对系统的VCC_1V8_S0供电要求不高，VCC_1V8_S0供电修改为采用MOS管的方案，如下图左侧图所示，其中放电电路为option电路。

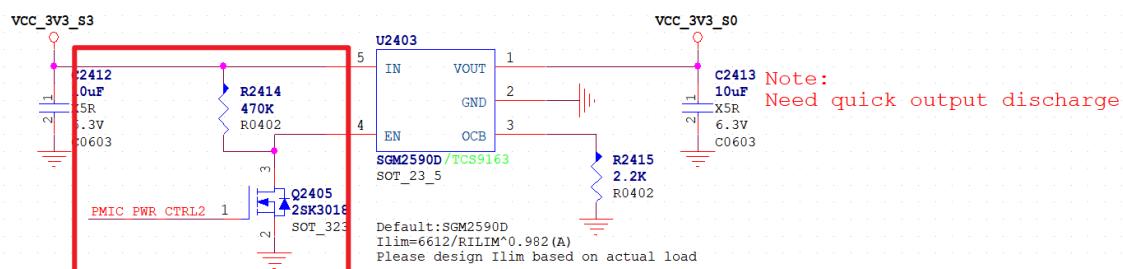
如果待机功耗要求较高，比如带电池的产品—平板和电子书等，建议EMMC待机时下电来减少功耗，此时需要采用带放电电阻的load switch，如下图右侧的绿色虚框方案。

VCC_1V8_S0



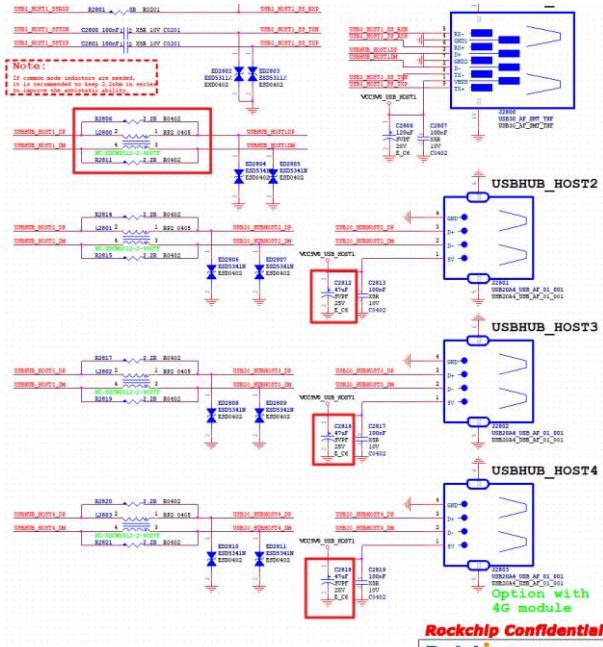
VCC_3V3_S0的使能改用PMIC_PWR_CTRL2和NMOS管来控制，以保证VCC_3V3_S0待机时和VCCA_1V8_S0的压差不大于2V(以满足USB的下电要求)

VCC_3V3_S0



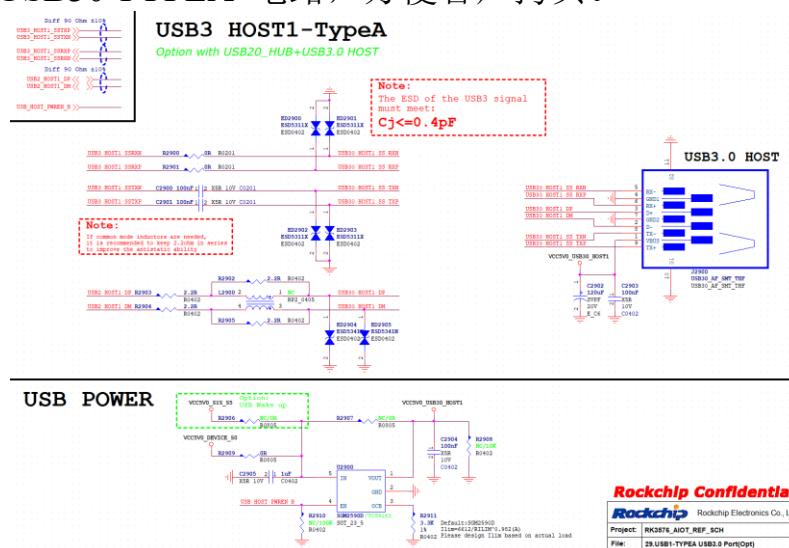
2.8 Page 27-- 28.USB1-USB20_HUB+USB3.0 HOST

由于HUB出来的4个USB公用一路5V供电，为避免总电容太大，上电瞬间把电源拉下来，将USB20接口的供电电源电容从120uF改为47uF。



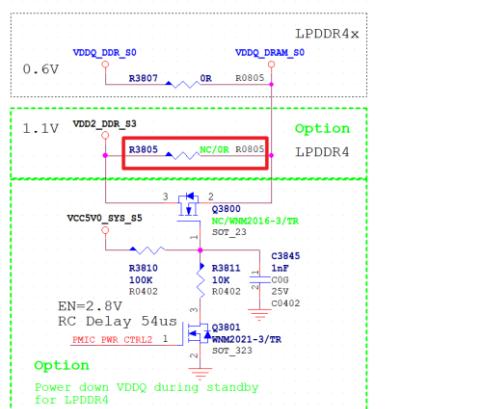
2.9 Page 28-- 29.USB1-TYPEA USB3.0 Port(Opt) (新增)

增加USB1原生USB3.0 TYPEA 电路，方便客户拷贝。



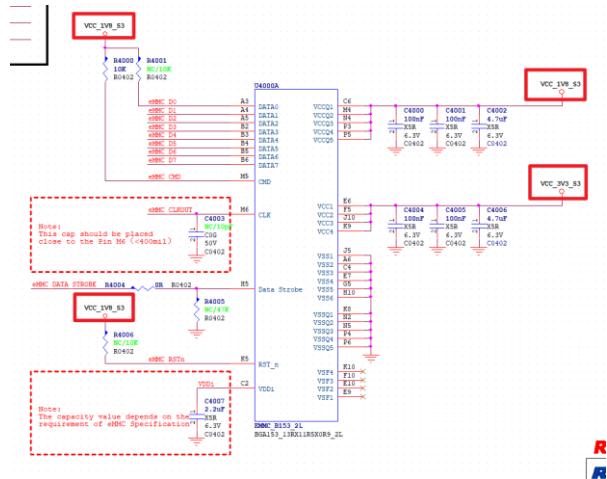
2.10 Page 29--38.DRAM-LPDDR4X_1X32bit_200P

LPDDR4颗粒的VDDQ_DRAM_S0供电增加VDD2_DDR_S3直通电阻方案，针对待机功耗要求不高时，可以选用VDD2_DDR_S3供电，减少器件数量。



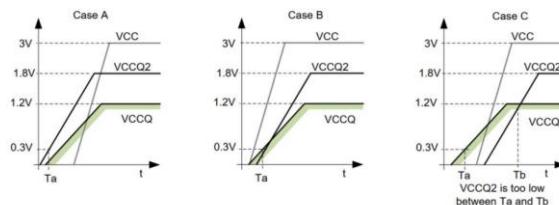
2.11 Page 31--40.Flash-eMMC

针对待机功耗要求不高的项目，可以将eMMC的颗粒供电改为待机常供电VCC_1V8_S3，也就是eMMC待机常供电，此时系统的VCC_1V8_S0供电可不需要采用带放电电阻的load switch(详见2.7 Page 23--24.Power-Ext Discrete/RTC IC)。如果待机功耗要求较高，比如带电池的产品—平板和电子书等，建议eMMC待机时下电来减少功耗，此时需要采用带放电电阻的load switch。



2.12 Page 32--41.Flash-UFS

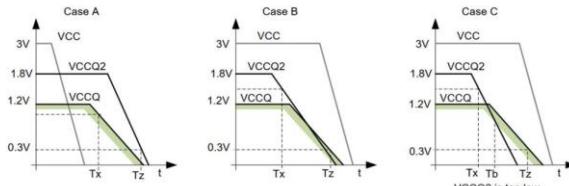
UFS 的时序要求如下：



NOTE 1 The green band represents the voltage range between VCCQ-200 mV and VCCQ.

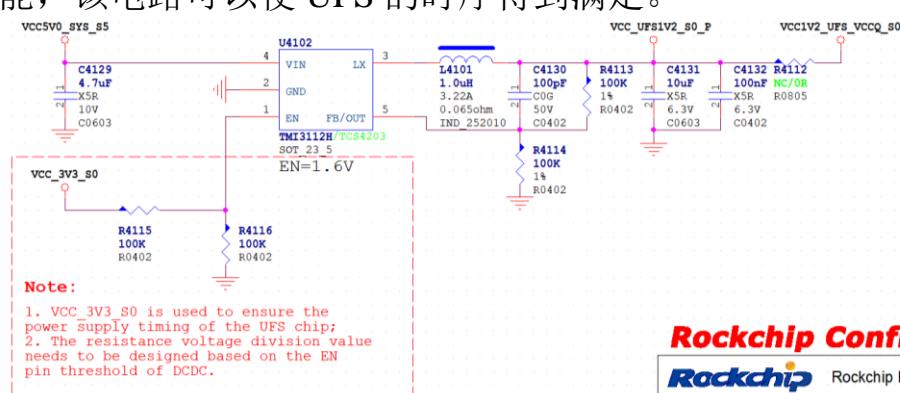
Figure 7.6 — Power up ramps

Figure 7.7 shows three power down ramp examples: case A and case B meet the requirement, while case C violates it in the time interval from Tb to Tz.



NOTE 1 The green band represents the voltage range between VCCQ-200 mV and VCCQ.

调整 UFS 的 VCC1V2_UFS_VCCQ_S0 供电的使能电路，改为用 VCC_3V3_S0 分压后来使能，该电路可以使 UFS 的时序得到满足。

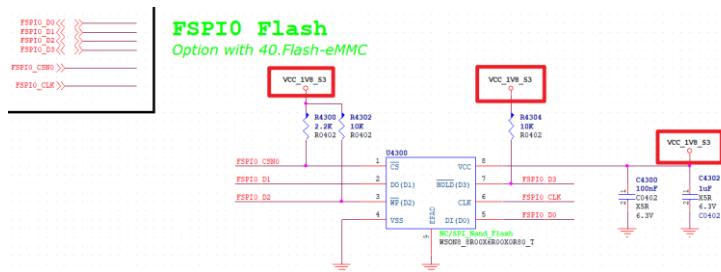


Rockchip Confidential

Rockchip Rockchip Elec

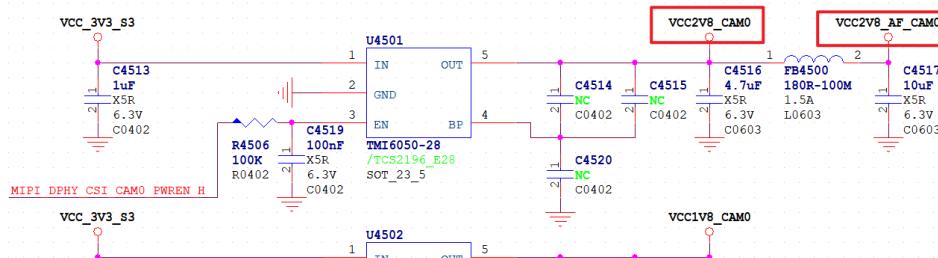
2.13 Page 34--43.Flash-SPI Flash(opt)

由于VCCIO0电源域的供电改为S3供电，FSPIO的颗粒供电也跟着改为S3电源



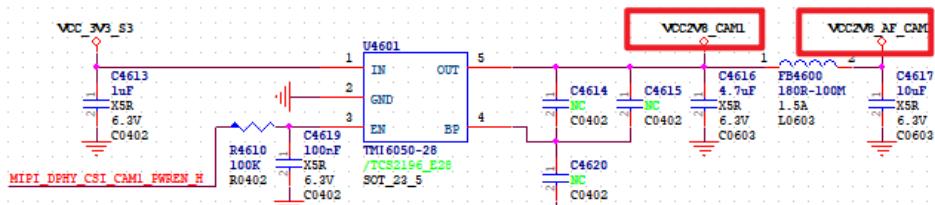
2.14 Page 35--45.VI-CAM MIPI DPHY CSI0 RX

VCC2V8_CAM0 调整到磁珠前，VCC2V8_AF_CAM0 调整到磁珠后



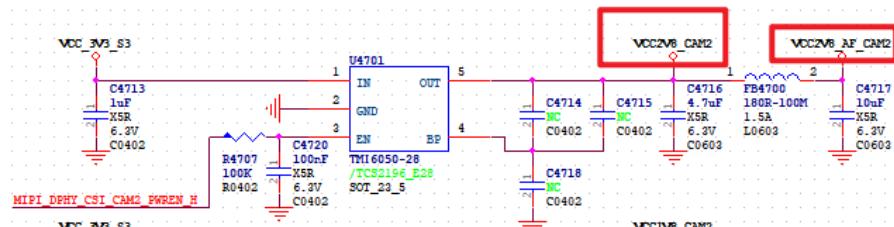
2.15 Page 36--46.VI-CAM MIPI DPHY CSI1/2 RX

VCC2V8_CAM1 调整到磁珠前，VCC2V8_AF_CAM1 调整到磁珠后



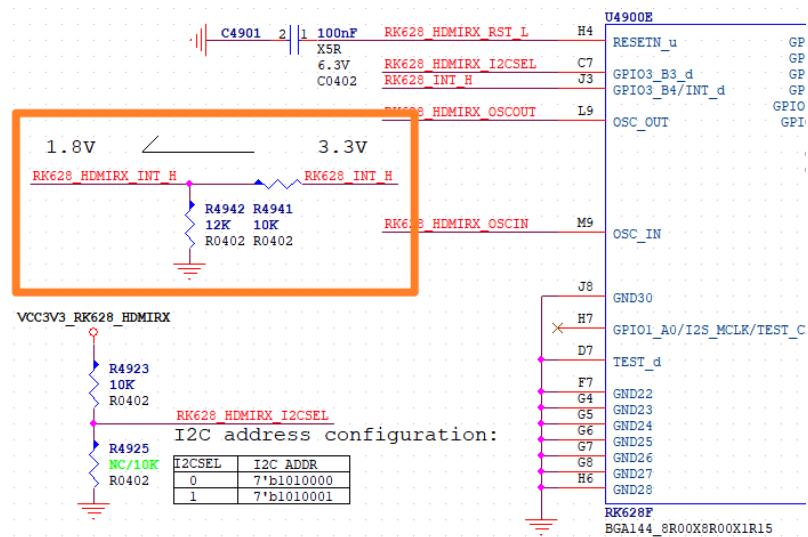
2.16 Page 37--47.VI-CAM MIPI DPHY CSI3/4 RX

VCC2V8_CAM2 调整到磁珠前，VCC2V8_AF_CAM2 调整到磁珠后

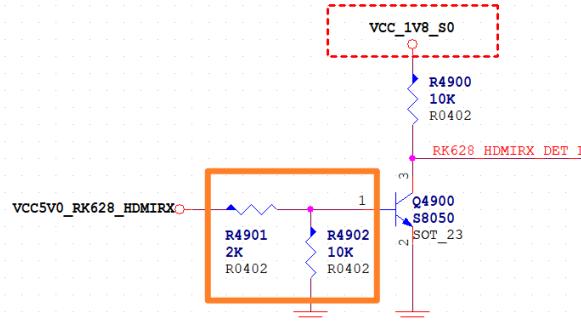


2.17 Page 38-- 49.VI-HDMI20 RX to MIPI RX(Opt)

RK628F 的 RK628_INT_H 信号是 3.3V 电平，且是高电平有效，RK3576 由于参考图中选择的 GPIO 是 1.8V 的，需要加电阻分压



分压电阻改小，加快放电速度

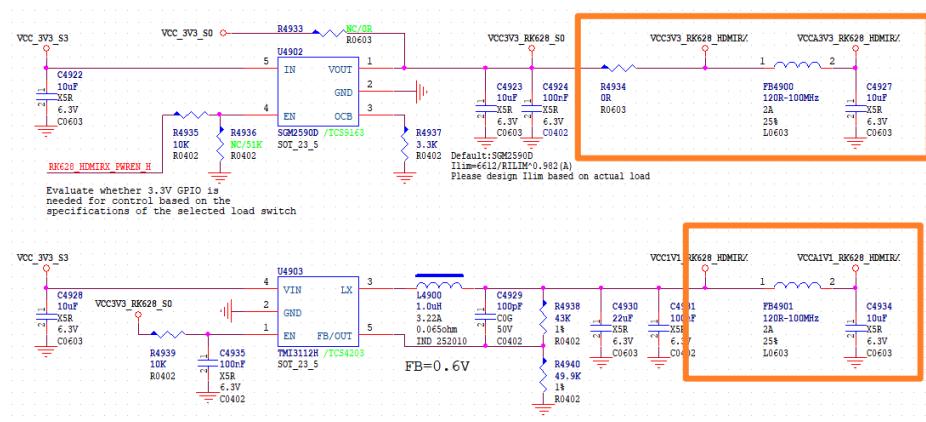


电容删减一些

RK628 Power

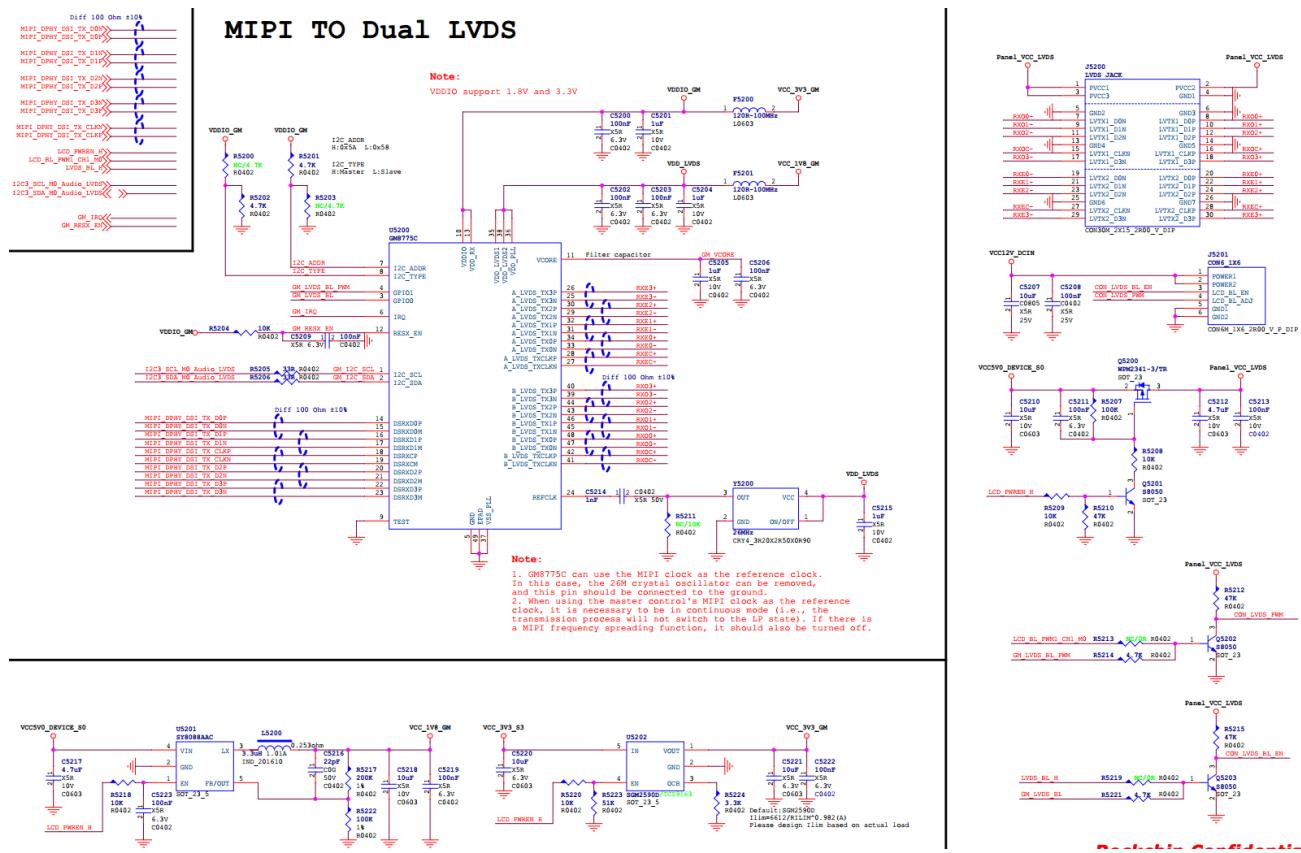
Power-on Sequence:

3V3 --> 1V1



2.18 Page 40--52.VO-MIPI to LVDS_GM8775C(新增)

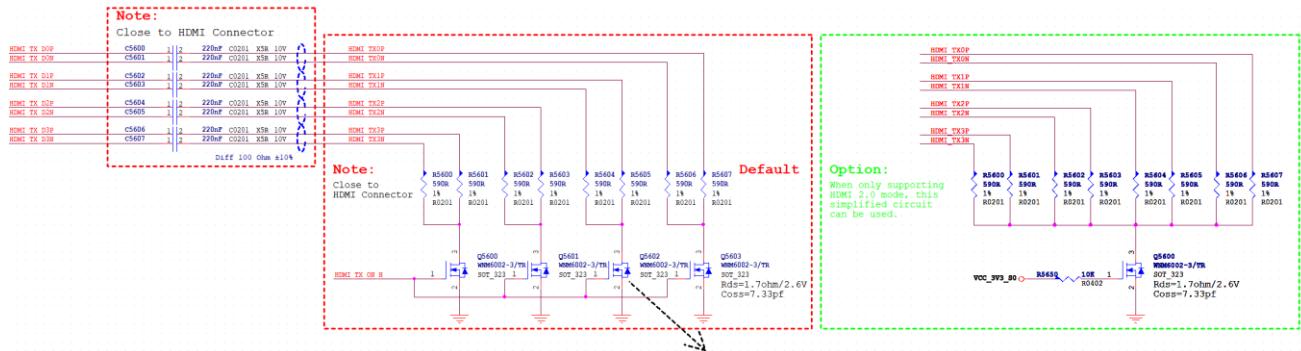
新增 MIPI 转双 LVDS 电路



2.19 Page 43--56.VO-HDMI TX

增加仅支持HDMI2.0时的MOS管简化方案，如下图绿色虚框所示。

HDMI 2.1 Support video output up to 4Kx2K@120Hz

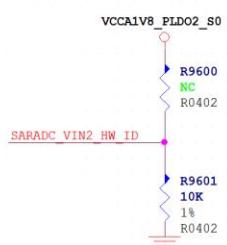


2.20 Page 63-- 96.HW_ID

SARADC上拉电源改为VCCA1V8 PLDO2 S0。

将HW ID的电阻配置等比例降低阻值，提高抗干扰能力。

HW_ID



Config Table for SARADC_VIN2_HW_ID				
Item	Rup	Rdown	ADC Value	VERSION
HW_ID1	NC	10K	0	HW_ID0
HW_ID2	10K	1.13K	416	RESERVE
HW_ID3	10K	2.49K	816	RESERVE
HW_ID4	10K	4.3K	1231	RESERVE
HW_ID5	10K	6.8K	1658	RESERVE
HW_ID6	10K	10K	2048	RESERVE
HW_ID7	10K	14.7K	2437	RESERVE
HW_ID8	10K	23.2K	2862	RESERVE
HW_ID9	10K	40.2K	3279	RESERVE
HW_ID10	10K	88.7K	3680	RESERVE
HW_ID11	10K	NC	4095	RESERVE