REF Schematic for RK3576

Main Functions Introduction

1) PMIC: 1 x RK806S-5 + DiscretePower
2) RAM: 1 x LPDDR4X 32bit
   Option: 1 x LPDDR4 32bit
   Option: 1 x LPDDR5 32bit
3) ROM: 1 x eMMC5.1 + 1 x UFS
   Option: 1 x SPI Flash(FSPI0)
4) Support: 1 x Micro SD Card3.0
   Option: 1 x SPI Flash(FSPI1)
5) Support: 1 x USB TYPEC with Displayport Alt Mode
   Option: 1 x USB2.0
   Option: 1 x USB3.2 Gen1x1 HOST
6) Support: 3 x USB2.0 HOST(USB2.0 HUB) + 1 x USB3.2 Gen1x1 HOST(USB2.0 from HUB)
   Option: 1 x USB3.2 Gen1x1 HOST
7) Support: 1 x a/b/g/n/ac/ax 2T2R SDIO WIFI6 + UART/PCM BT
   Option: 1 x a/b/g/n/ac/ax 2T2R PCIe WIFI6 + UART/PCM BT
   Option: 1 x a/b/g/n/ac/ax 2T2R SDIO WIFI + UART/PCM BT
   Option: 1 x a/b/g/n/ac 1T1R SDIO WIFI + UART/PCM BT
8) Support: 1 x PCIe Slot_36P
   Option: 1 x a/b/g/n/ac/ax 2T2R PCIe WIFI6 + UART/PCM BT
   Option: 1 x MiniPCIe Slot_with 4G
   Option: 1 x SATA Slot
9) Support: 3 x CAM MIPI CSI RX
   Option: 1 x 4Lanes MIPI DPHY RX Camera + 1 x HDMI RX to MIPI CSI
10) Support: 1 x LCM MIPI DSI TX
   Option: 1 x MIPI to LVDS
11) Support: 1 x HDMI2.1 TX (Up to 4Kx2K@120Hz)
   Option: 1 x LCM eDP TX
12) Support: 2 x 10/100/1000M Ethernet
   Option: 1 x 10/100M Ethernet + 1 x 10/100/1000M Ethernet
13) Support: 1 x Headphone + 2 x SPK + 1 x Analog MIC
   Option: 4 x PDM-DMIC
14) Support: 1 x SPDIF TX + 1 x SPDIF RX
15) Support: 1 x IR Receiver
16) Support: 1 x G-Sensor
17) Support: Array Key(MENU,VOL+,VOL-,ESC)
18) Support: 7 x SARADC + 1 x SARADC only for boot
19) Support: 1 x Debug UART Connector

Note:

The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic.
If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	00.Cover Page				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	1 of 65

Table of Content

Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. NC stands for component not mounted temporarily
2. If Value or option is NC, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

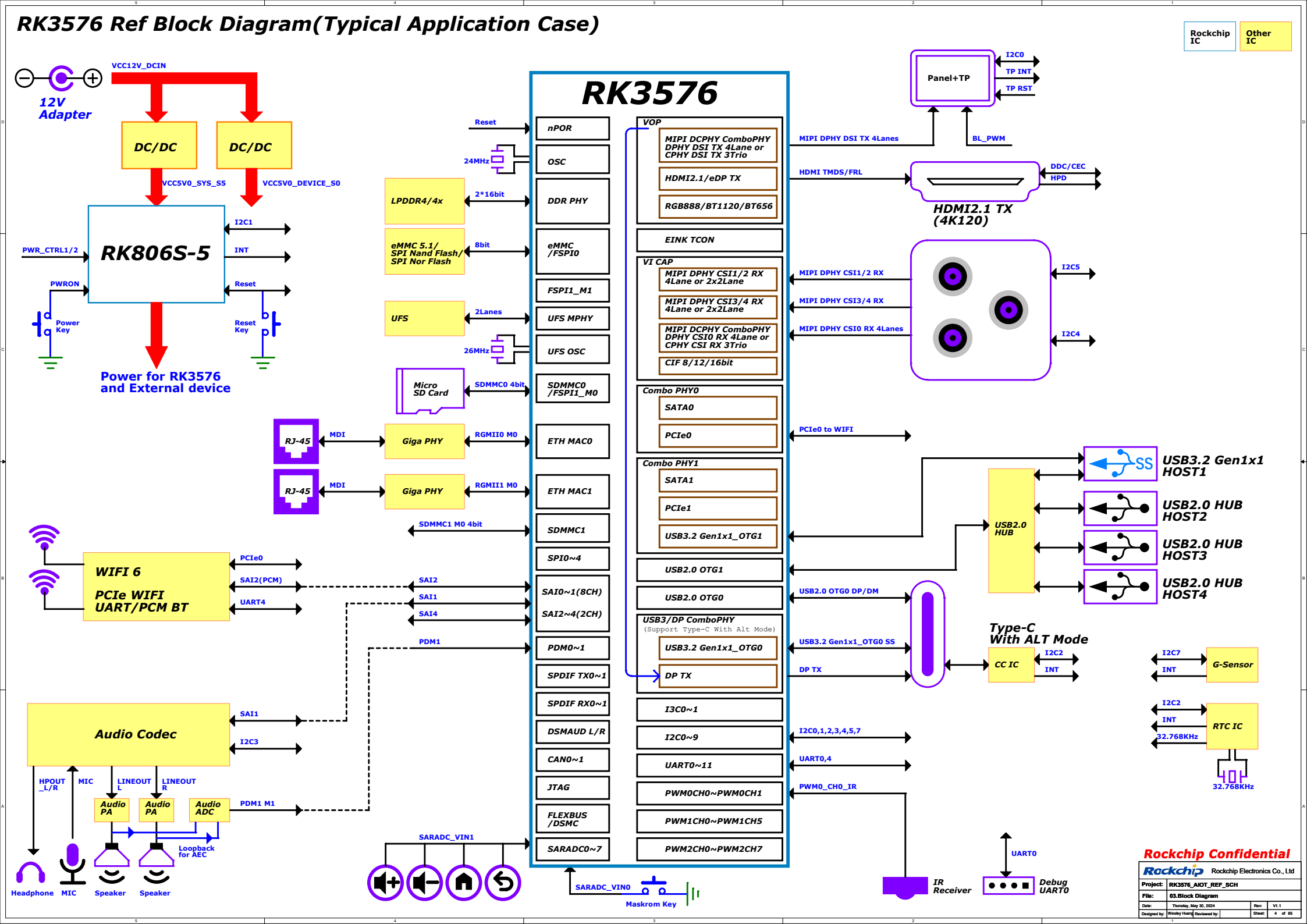
Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	01.Index and Notes				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	2 of 65

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2024-03-22	Wesley Huang	1. First version;	
V1.1	2024-05-30	Wesley Huang	1. SARADC_AVDD1V8 pin of RK3576 is changed to use the PLDO2 power supply of RK806S-5; The timing of the PLDO2 power supply is changed from 3 to 5. 2. Added a new MIPI to dual LVDS circuit; 3. The VCC_1V8_S0 power supply has been modified to use a MOSFET-based solution, and the enable control for VCC_3V3_S0 has been modified to be controlled by PMIC_PWR_CTRL2 and an NMOS transistor; 4. The power supply for EMMC has been changed to a VCC_1V8_S3 during standby; 5. Add 29.USB1-TYPEA USB3.0 Port(Opt) 6. The PCB package of RK3576 is modified to BGA698_16R1X17R2X1R08. 7. EN control signal of VCC1V2_UFS_VCCQ_S0' DCDC is changed. 8. Add voltage dividing resistors to the int signal of RK628F 9. Make some minor modifications.	

RK3576 Ref Block Diagram(Typical Application Case)

Rockchip IC | Other IC



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Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3576_AIOT_REF_SCH
File:	03.Block Diagram
Date:	Thursday, May 30, 2024
Rev:	V1.1
Designed by:	Wesley Huang
Reviewed by:	
Sheet:	4 of 65

Default Power Tree

Note: Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

12V/3A Adapter

VCC12V_DCIN

Note: With PCIe/SATA, the current is estimated according to the actual number of PCIe/SATA

DC/DC 5000mA

DC/DC 3000mA

DC/DC 3000mA
- Power LED Max:
- PCIe_Slot_3V3 Max:
- MOS
  - PCIe_Slot_12V Max:

VCC5V0_SYS_S5 Seq:0

VCC5V0_DEVICE_S0 Seq:5A
- TYPEC 5V Max:
- USB2_HOST 5V Max:
- MIPI DSI LCM 5V Max:
- HDMI TX 5V Max:
- SPK AMP 5V Max:
- Work LED Max:

RK806S-5

Power on Sequence

VCC1	BUCK1 6.5A max	Seq:2	VDD_CPU_BIG_S0 Max:4A	VDD_CPU_BIG_SOC
VCC2	BUCK2 5.0A max	Seq:2	VDD_NPU_S0 Max:4A	VDD_NPU_SOC
VCC3	BUCK3 5.0A max	Seq:2	VDD_CPU_LIT_S0 Max:2A	VDD_CPU_LIT_SOC
VCC4	BUCK4 5.0A max	Seq:5	VCC_3V3_S3 Max:	LOAD SWITCH VCC_3V3_S0
VCC5	BUCK5 3A max	Seq:2	VDD_GPU_SOC Max:3A	VDD_GPU_SOC
VCC6	BUCK6 3A max	Seq:7	VDDQ_DDR_S0 Max:	LPDDR4x VDDQ Max: LPDDR5 VDDQ Max: DDRPHY_CK_VDDQ_SOC Max: DDRPHY_VDDQ_SOC Max:
VCC7	BUCK7 3A max	Seq:2	VDD_LOGIC_S0 Max:2A	VDD_LOGIC_SOC VDD_LOGIC_MEM_SOC
VCC8	BUCK8 3A max	Seq:3	VCC_1V8_S3 Max:	LOAD SWITCH 3 x LDO 3 x LDO 3 x LDO LOAD SWITCH CC IC 3V3 Max: eMMC_3V3 Max: TP 3V3 Max: WIFI BAT Max: IR 3V3 Max: Debug Uart 3V3 Max: PMUIO1_VCC_SOC Max:
VCC9	BUCK9 3A max	Seq:4	VDD2_DDR_S3 Max:	LPDDR4 VDDQ Max: LPDDR4/4x VDD2 Max: LPDDR5 VDD2H Max: DDRPHY_CKE_VDDQ_SOC Max:
VCC10	BUCK10 3A max	Seq:2	VDD_DDR_S0 Max:2A	DDRPHY_DVDD_SOC
VCC_2V0_PLDO_S3	PLDO1 500mA max	Seq:3	VCCA_1V8_S0	OSC_AVDD1V8_SOC Max: PLL_AVDD1V8_SOC Max: DDRPHY_PLL_AVDD1V8_SOC Max: UFS_AVDD1V8_SOC Max: OSC_UFS_AVDD_SOC Max: USB3_OTG0/DP_TX_AVDD1V8_SOC Max: USB2_OTG_AVDD1V8_SOC Max: MIPI_D/C_PHY_AVDD1V8_SOC Max: MIPI_CSI1/2_AVDD1V8_SOC Max: MIPI_CSI3/4_AVDD1V8_SOC Max: HDMI_TX/eDP_TX_AVDDIO1V8_SOC Max: HDMI_TX/eDP_TX_AVDDCMN1V8_SOC Max: PCIE0_SATA0_AVDD1V8_SOC Max: PCIE1_SATA1_USB3_OTG1_AVDD1V8_SOC Max:
VCC11	PLDO2 300mA max	Seq:5	VCCA1V8_PLDO2_S0	SARADC_AVDD1V8_SOC Max:
	PLDO3 300mA max	Seq:4	VDDA_1V2_S0	VCCIO7_VCC_SOC Max: MIPI_DCPHY_AVDD1V2_SOC Max:
VCC12	PLDO4 500mA max	Seq:5	VCCA_3V3_S0	CODEC VCCA3V3 Max:
	PLDO5 300mA max	Seq:5	VCCIO_SD_S0	VCCIO1_VCC_SOC Max:
VCCA	PLDO6 300mA max	Seq:3	VCCA1V8_PLDO6_S3	VCCA1V8_PLDO6_S3 Max:
	NLDO1 300mA max	Seq:2	VDD_0V75_S3	PMU_LOGIC_DVDD0V75_SOC Max:
VCC_1V1_NLDO_S3	NLDO2 300mA max	Seq:2	VDDA_DDR_PLL_S0	DDRPHY_PLL_DVDD_SOC Max:
	NLDO3 500mA max	Seq:2	VDDA_HDMI_S0	HDMI_TX/eDP_TX_AVDDD0V75_SOC Max: HDMI_TX/eDP_TX_AVDDC0V75_SOC Max:
VCC_1V1_NLDO_S3	NLDO4 500mA max	Seq:2	VDDA_0V85_S0	UFS_AVDD0V85_SOC Max: USB3_OTG0/DP_TX_AVDD0V85_SOC Max: USB3_OTG0/DP_TX_DVDD0V85_SOC Max: PCIE0_SATA0_AVDD0V85_SOC Max: PCIE1_SATA1_USB3_OTG1_AVDD0V85_SOC Max:
	NLDO5 300mA max	Seq:2	VDDA_0V75_S0	PLL_DVDD0V75_SOC Max: OTP_DVDD0V75_SOC Max: USB2_OTG_DVDD0V75_SOC Max: MIPI_DCPHY_AVDD_SOC Max: MIPI_CSI1/2_RX_AVDD0V75_SOC Max: MIPI_CSI3/4_RX_AVDD0V75_SOC Max:
	EXT DC/DC ,2A (VCC_3V3_S3 → EN)	Seq:1	VDD2L_0V9_DDR_S3 Max:	LPDDR5 VDD2L Max:
	EXT DC/DC ,2A (PMIC_EXT_EN_OUT → EN)	Seq:1	VCC_2V0_PLDO_S3 Max:	
	EXT DC/DC ,2A (PMIC_EXT_EN_OUT → EN)	Seq:1	VCC_1V1_NLDO_S3 Max:	
	EXT DC/DC ,2A (VCC_3V3_S0 → EN)	Seq:5B	VCC_UFS_S0 Max:	VCC_UFS_S0(Opt) Max:
	EXT DC/DC ,2A (VCC1V8_UFS_VCCQ2_S0 → EN)	Seq:4B	VCC1V2_UFS_VCCQ_S0 Max:	VCC1V2_UFS_VCCQ_S0(Opt) Max:
	EXT LDO	Seq:0A	VCC3V3_RTC_S5 Max:	RTC_3V3 Max:

- Audio ADC ES7202 3V3 Max:
- CODEC ES8388 3V3 Max:
- USB2 HUB Max:
- VCC_UFS_S0 Max:
- RGMII PHY0/1 3V3 Max:
- RGMII PHY1 VCCIO Max:
- SPDIF TX/RX Max:
- G-Sensor 3V3 Max:
- VCCIO2_VCC_SOC Max:
- VCCIO4_VCC_SOC Max:
- VCCIO6_VCC_SOC Max:
- USB2_OTG_AVDD3V3_SOC Max:

LOAD SWITCH VCC_3V3_S0
- SD Card 3V3 Max:
- CAM 1V2 Max:
- CAM 2V8 Max:
- CAM 1V8 Max:
- LCD 3V3 Max:

NMOS VCC_1V8_S0
- VCCIO5_VCC_SOC Max:

eMMC_1V8 PMOS
- UFS_VCCQ2_1V8_S0 Max:

Note: The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic. If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3576_AIOT_REF_SCH
File:	04.Power Tree
Date:	Thursday, May 30, 2024
Rev:	V1.1
Designed by:	Wesley Huang
Reviewed by:	
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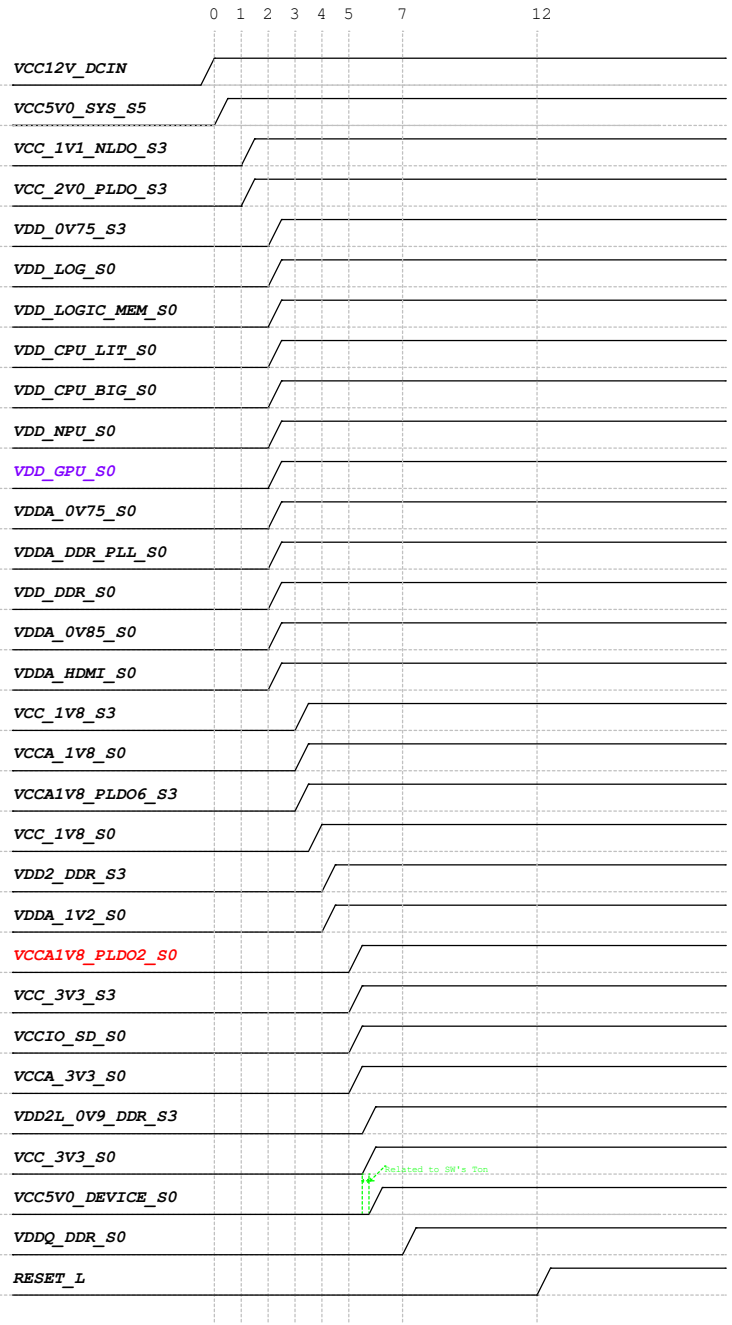
Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:5	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC5V0_SYS_S5	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5A	0.9V	ON	0.9V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	5A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCC_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Note:

The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

Note:

Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3576_AIOT_REF_SCH
File:	05.Power Sequence and Map
Date:	Thursday, May 30, 2024
Rev:	V1.1
Designed by:	Wesley Huang
Reviewed by:	
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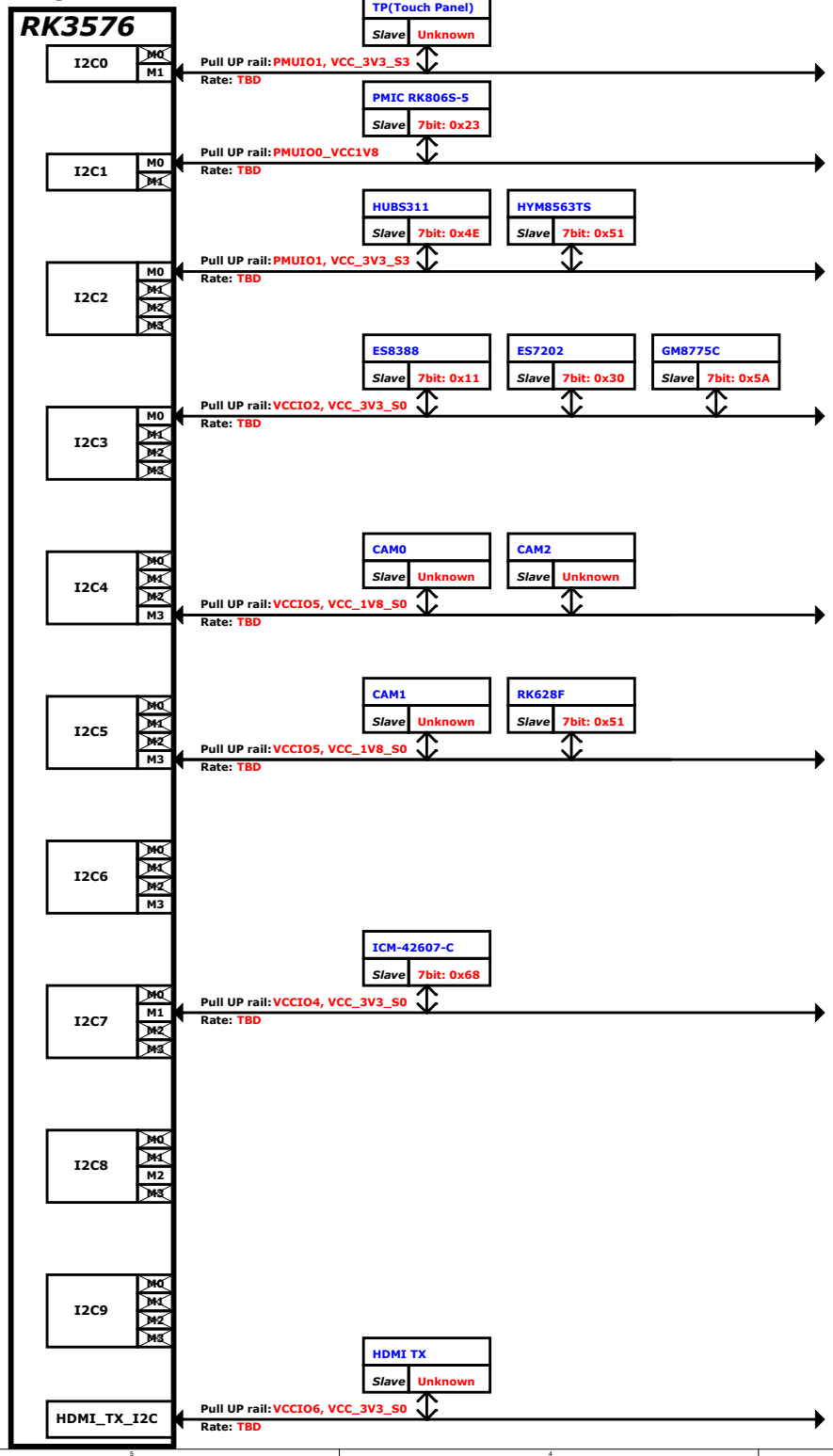
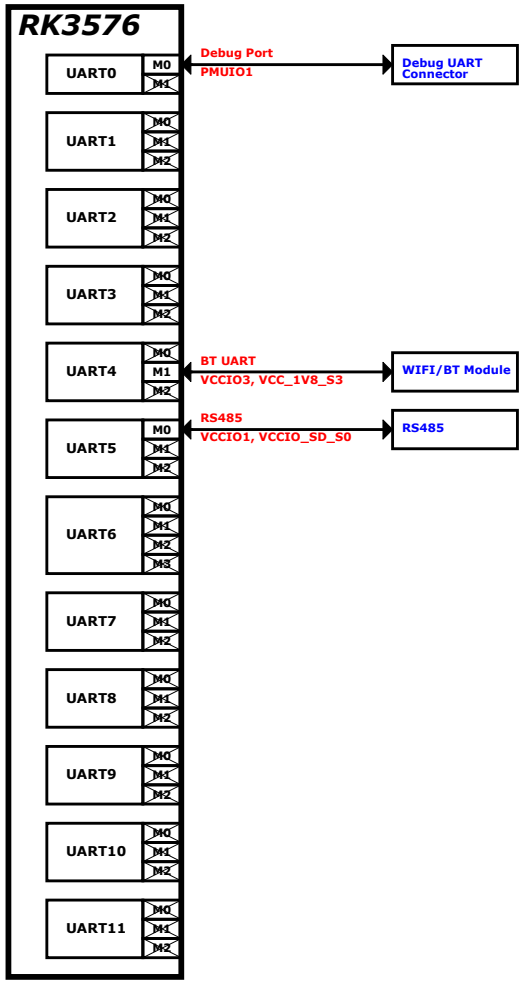
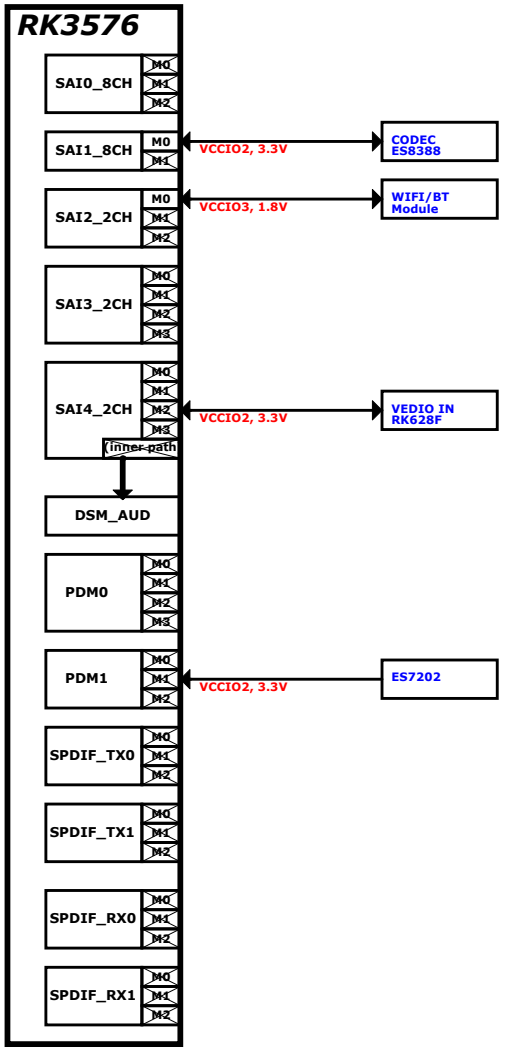
I2C MAP



UART MAP



Audio MAP



Note:

M0 Unselected IOmux path

M1 IOmux path in use

At the same time, only one path can be selected.

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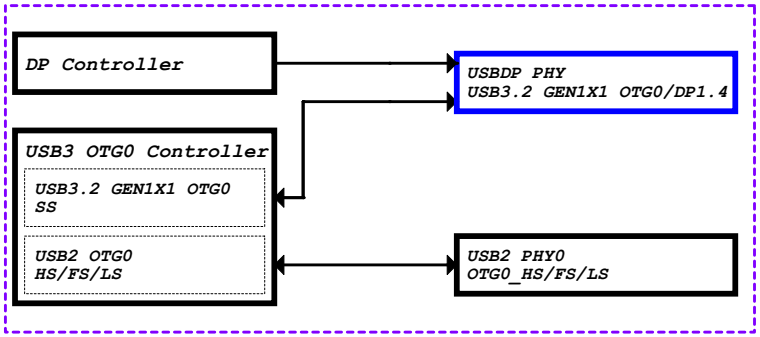
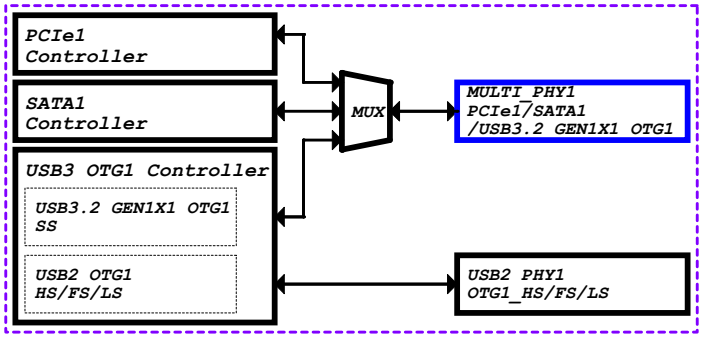
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	05.Lower-Speed Bus Map		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by: Wesley Huang	Reviewed by:	Sheet:	7 of 65

MULTI_PHY Path Map

USBDP PHY--USB3.2 GEN1X1 OTG0/DP1.4



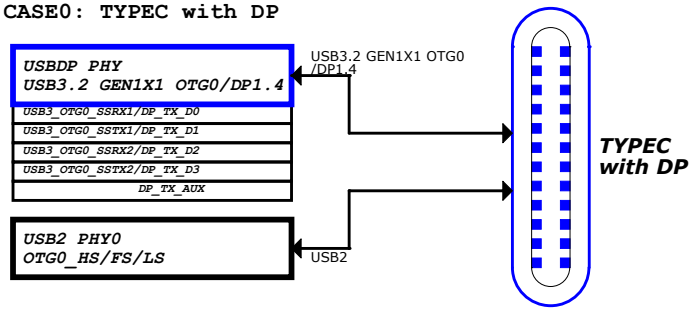
PCIe Combo PHY1--
PCIe1/SATA1/USB3.2 GEN1X1 OTG1



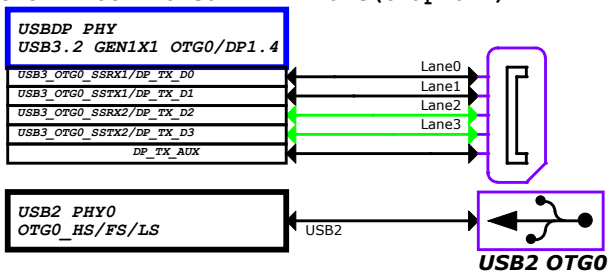
Note:
USB2 PHY1 can only be used when PCIE1/SATA1 is not in use!!!

USB OTG0/DP Application

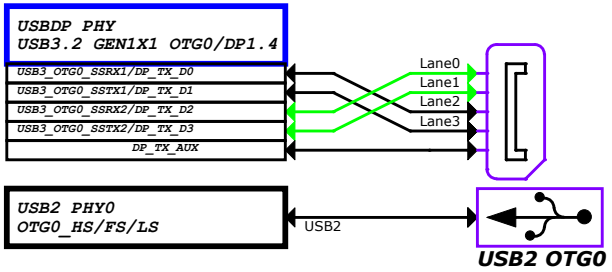
CASE0: TYPEC with DP



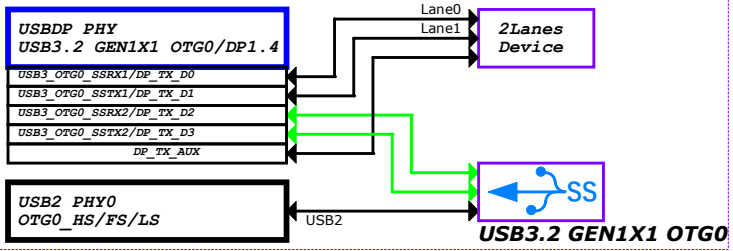
CASE1: USB2 OTG0 + DP 4Lane(Swap OFF)



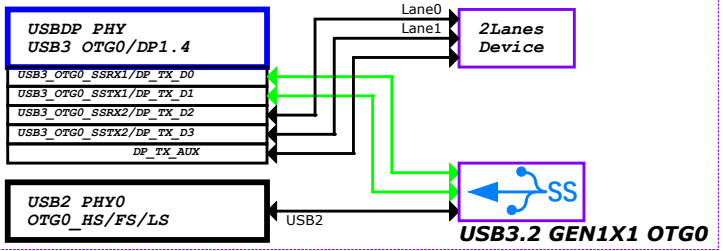
CASE2: USB2 OTG0 + DP 4Lane(Swap ON)



CASE3: USB3.2 GEN1X1 OTG0 + DP 2Lane(Swap OFF)



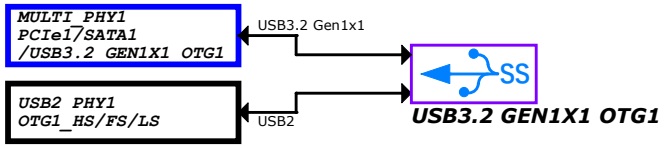
CASE4: USB3.2 GEN1X1 OTG0 + DP 2Lane(Swap ON)



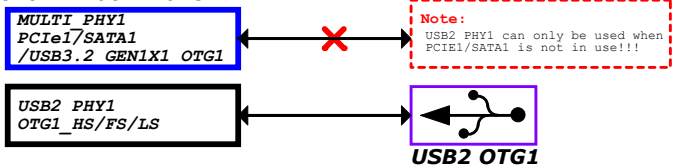
Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

USB OTG1 Application

CASE0: USB3.2 GEN1X1 OTG1

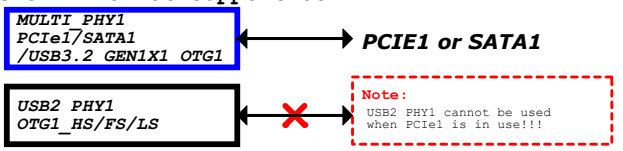


CASE1: USB2 OTG1



Note:
USB2 PHY1 can only be used when PCIE1/SATA1 is not in use!!!

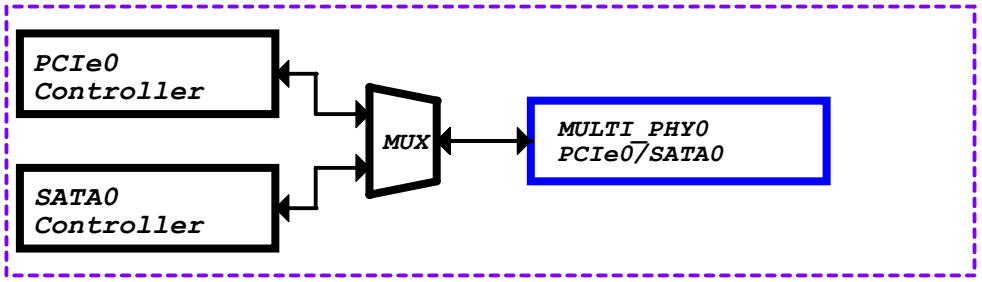
CASE2: Do not support USB

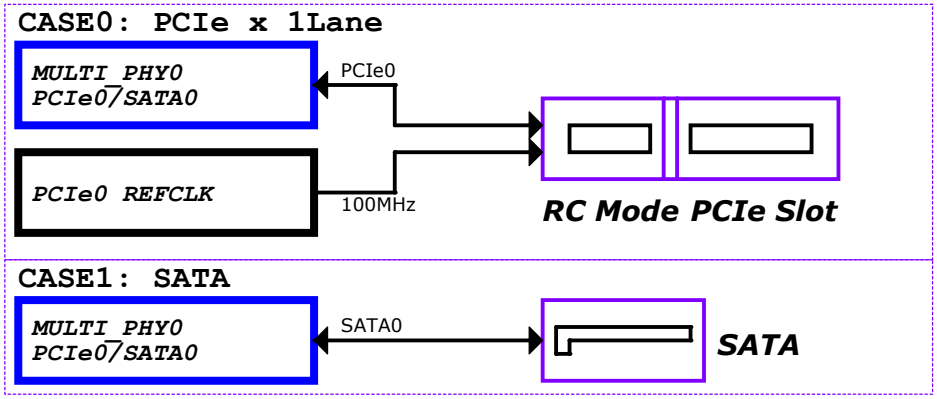


Note:
USB2 PHY1 cannot be used when PCIe1 is in use!!!

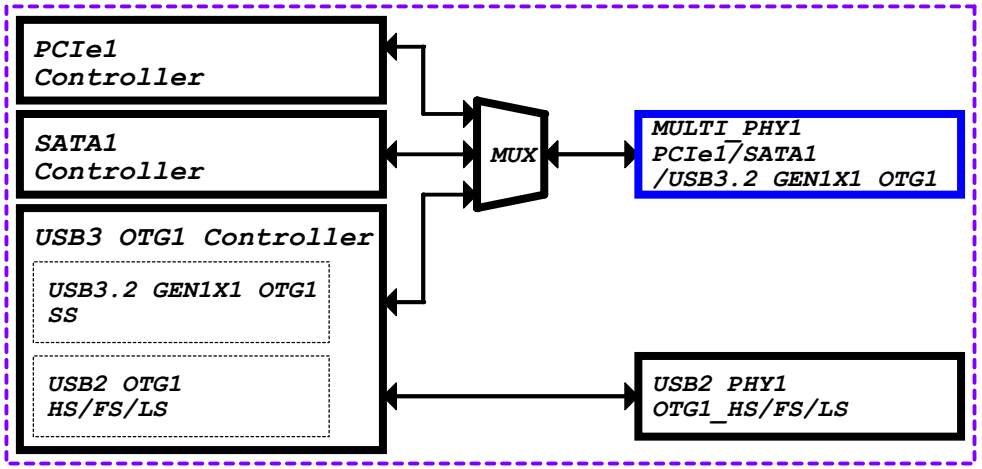
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3576_AIOT_REF_SCH
File:	07.USB/DP Configure Map
Date:	Thursday, May 30, 2024
Rev:	V1.1
Designed by:	Wesley Huang
Reviewed by:	
Sheet:	8 of 65

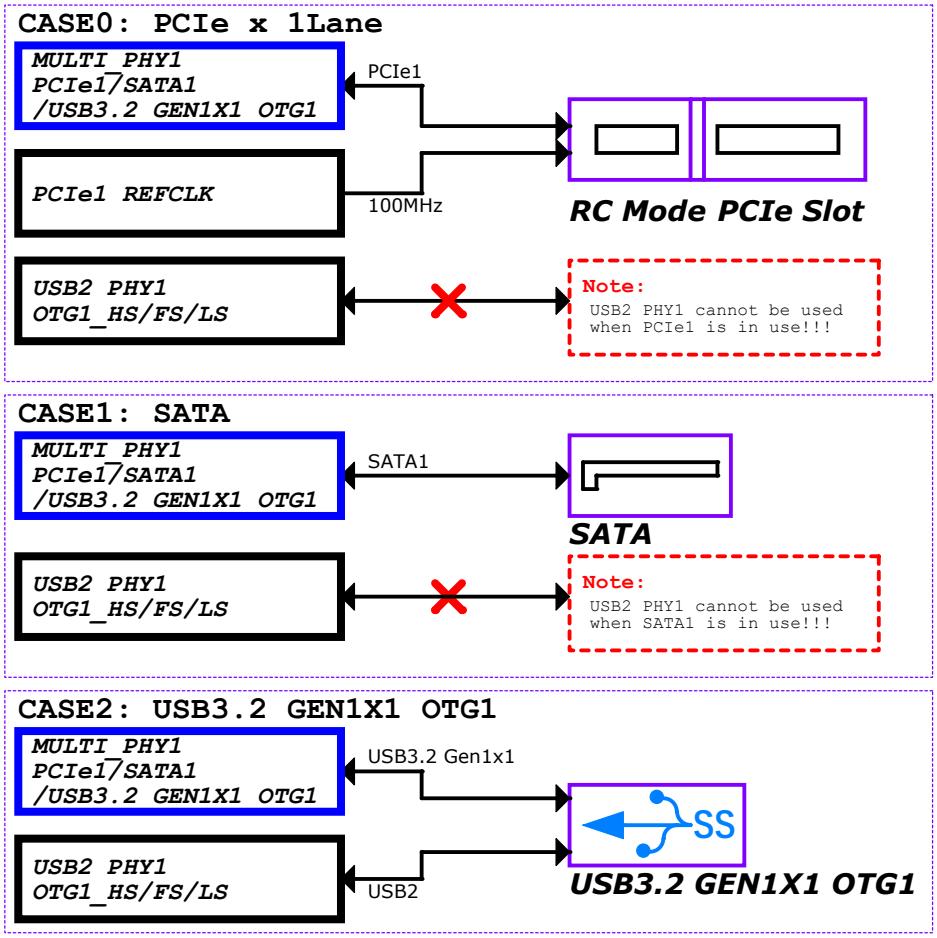
PCIe Combo PHY0--PCIe0/SATA0





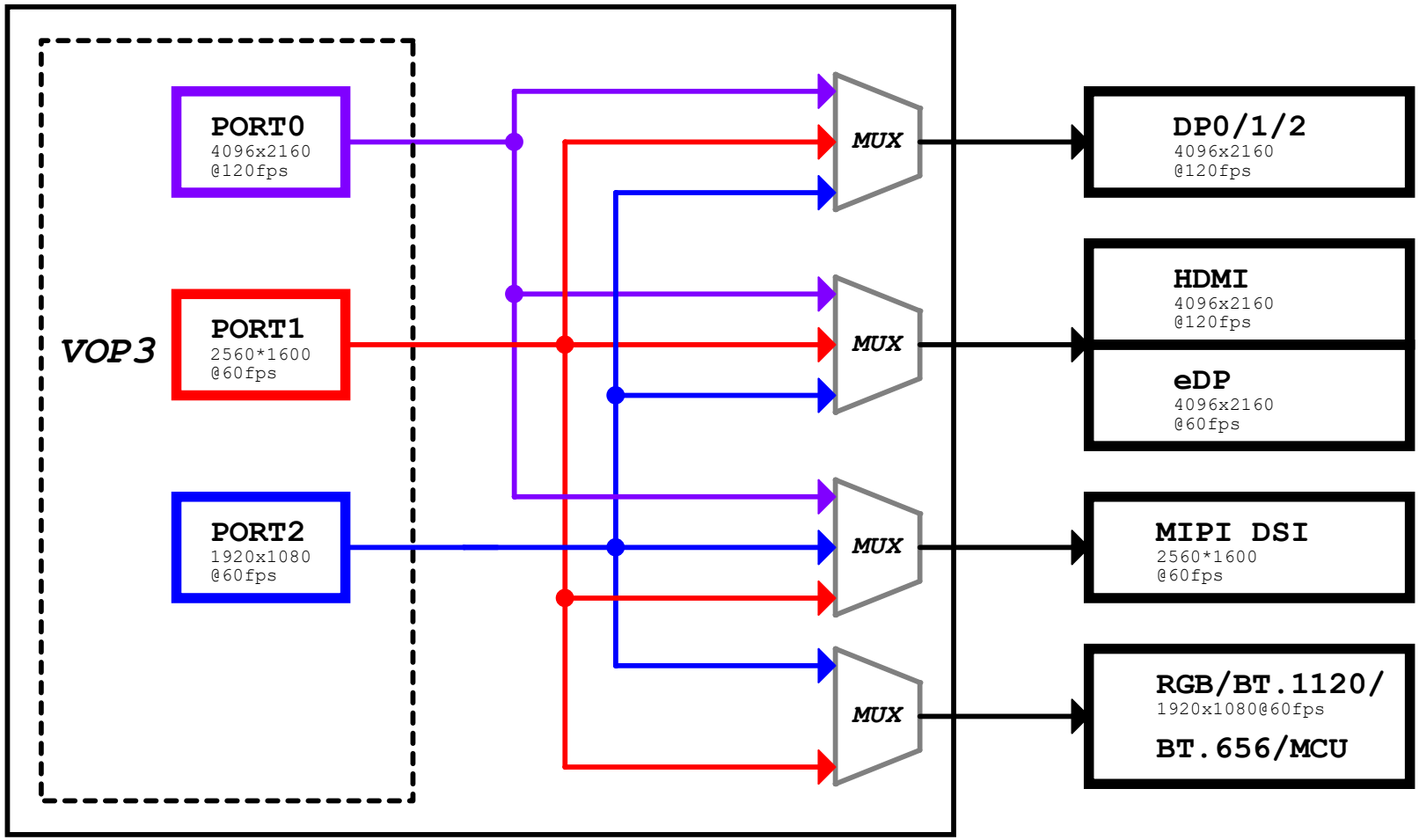
PCIe Combo PHY1--
PCIe1/SATA1/USB3.2 GEN1X1 OTG1





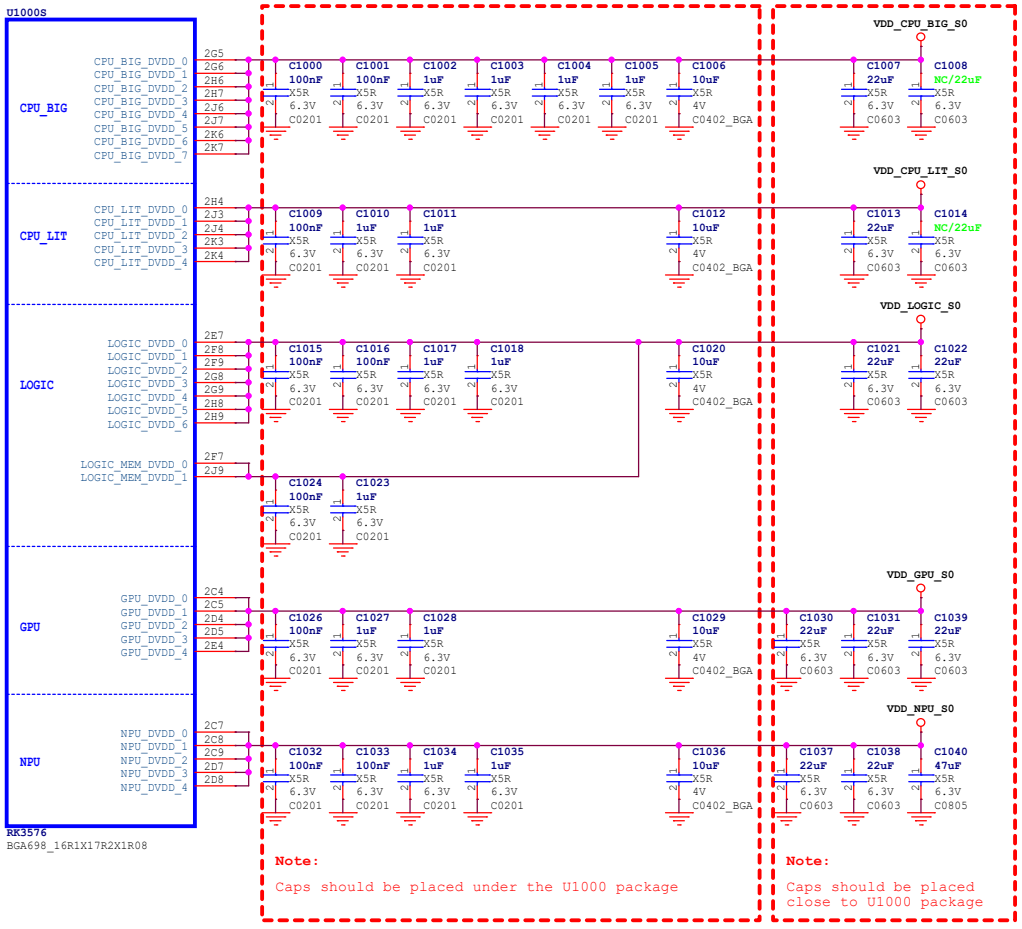
Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	08.PCIe Combo PHY Configure Map				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	9 of 65

VO MAP

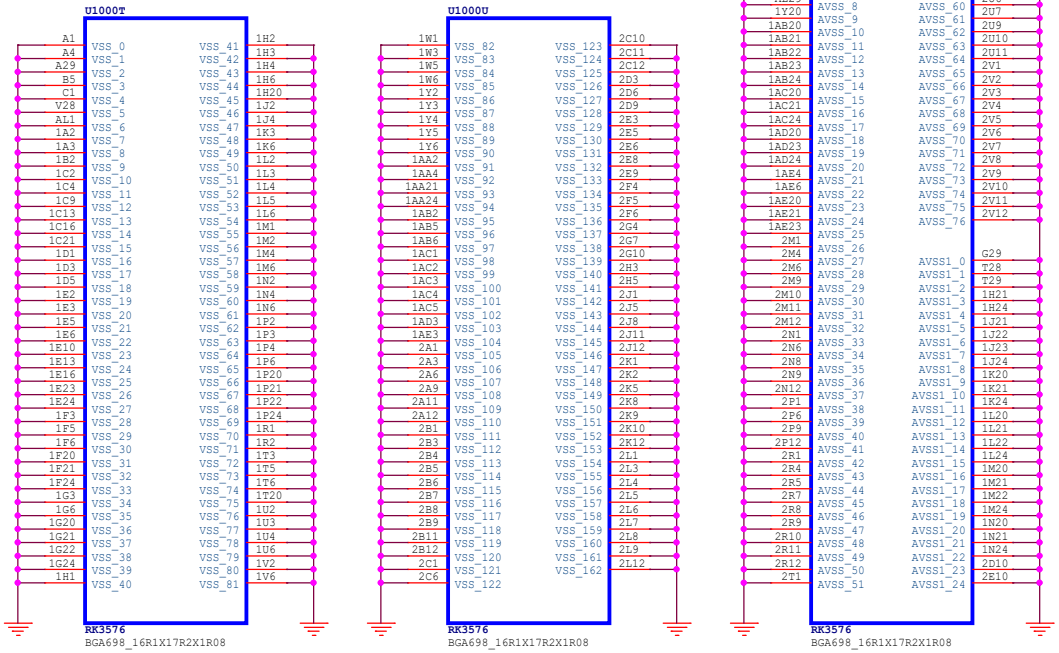


Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	09.VOP Map		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang / Reviewed by:	Sheet:	10 of 65

RK3576_S (Power)



RK3576_T/U/V (GND)



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Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	10.RK3576-Power/GND				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	11 of 65

RK3576_E (PMUIO0/1)

Note:
Adjust CL1 and CL2 according to the crystal specification
The the load capacitance CL is recommended by the crystal vendors to obtain target clock frequency.
CL=(CL1*CL2/(CL1+CL2))+PCB strays Total CL<=12pF

U1000E

OSC
PMUIO0 Domain
Operating Voltage=1.8V

PLL
PMUIO1 Domain
Operating Voltage=1.8V/3.3V

PMUIO0/PMUIO1/VCCIO7 Domain Logic Power
Operating Voltage=0.75V

RK3576
BGA698_16R1X17R2X1R08

RK3576_R (SARADC)

U1000R

SARADC
12-bit 1MS/s
TSADC
OTP

RK3576
BGA698_16R1X17R2X1R08

Note:This cap should be placed close to RK3576

Option:
If SARADC_IN4~7 is not used, the filtering capacitor can also be omitted

Note:
Closed to RK3576
Stay away from strong interference signals

BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

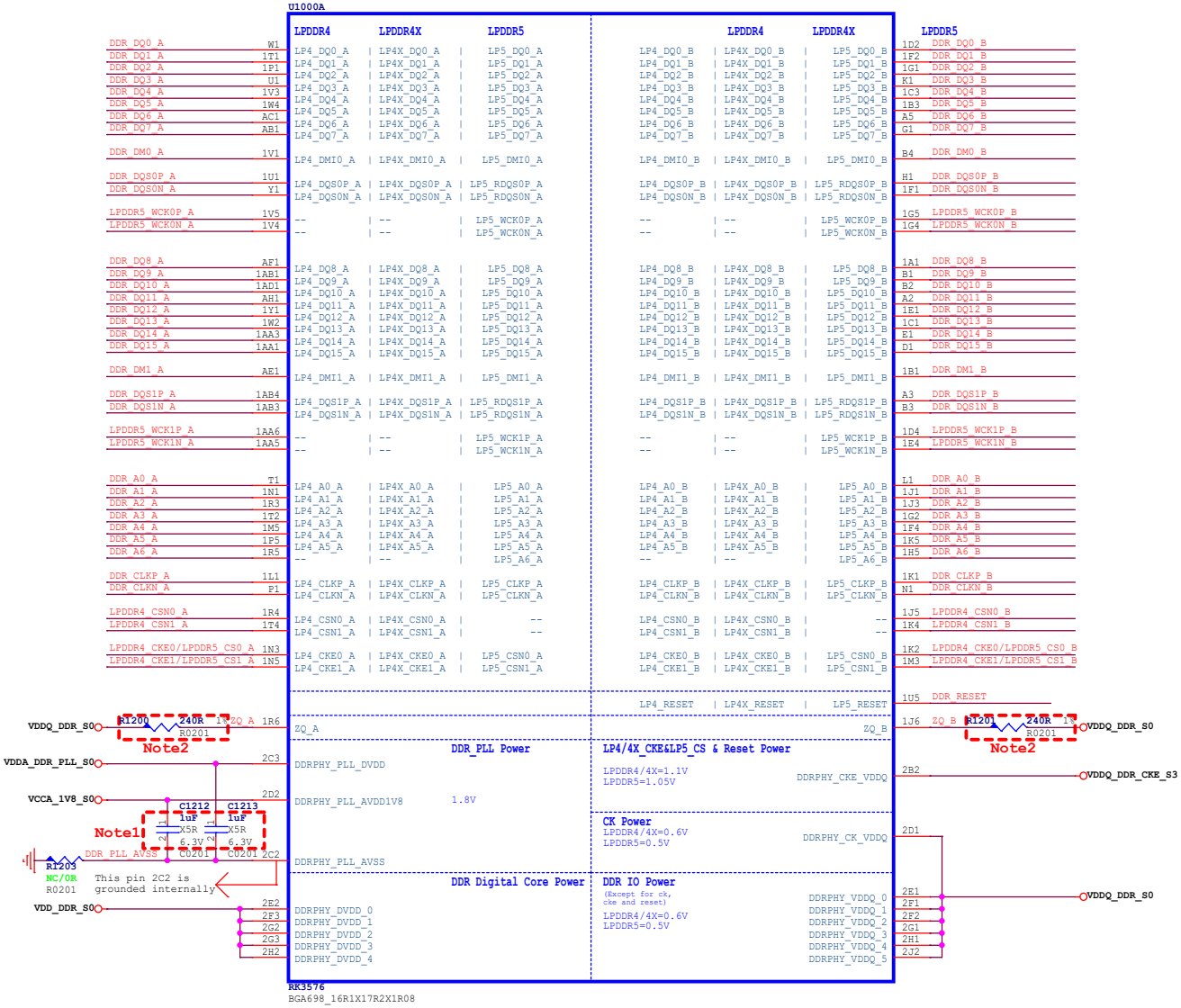
Item	Rup	Rdown	ADC Value	Boot Mode
Config1	NC	10K	0	USB (Maskrom mode)
Config2	10K	1.13K	416	FSPI0->USB
Config3	10K	2.49K	816	FSPI1_M0->EMMC->USB
Config4	10K	4.3K	1231	FSPI1_M1->EMMC->USB
Config5	10K	6.8K	1658	FSPI0->UFS->USB
Config6	10K	10K	2048	FSPI1_M0->UFS->USB
Config7	10K	14.7K	2437	UFS->USB
Config8	10K	23.2K	2862	UFS->SDMMC0->USB
Config9	10K	40.2K	3279	RFU
Config10	10K	88.7K	3680	EMMC->SDMMC0->USB
Config11	10K	NC	4095	EMMC->USB

Note:
Must be mounted

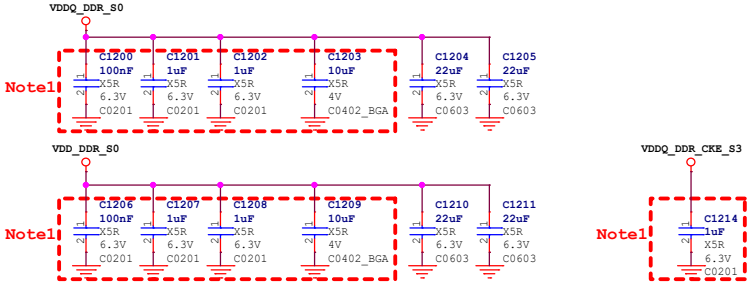
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3576_AIOT_REF_SCH
File:	11.RK3576-OSC/PLL/PMUIO/SARADC
Date:	Thursday, May 30, 2024
Rev:	V1.1
Designed by:	Wesley Huang
Reviewed by:	
Sheet:	12 of 65

RK3576_A(DDRPHY)



DDR FILTER

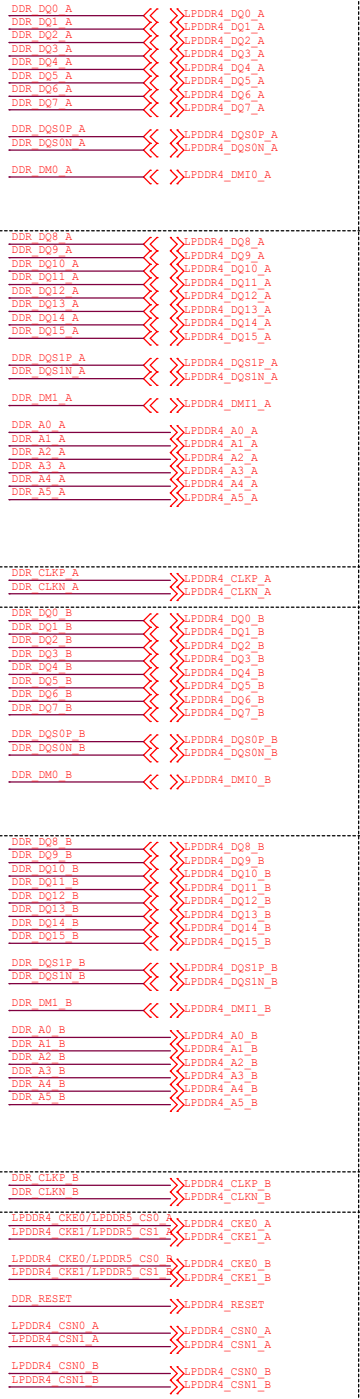


Note:
(1) Power Sequence: VDD-VDDQ_CKE-VDDQ
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

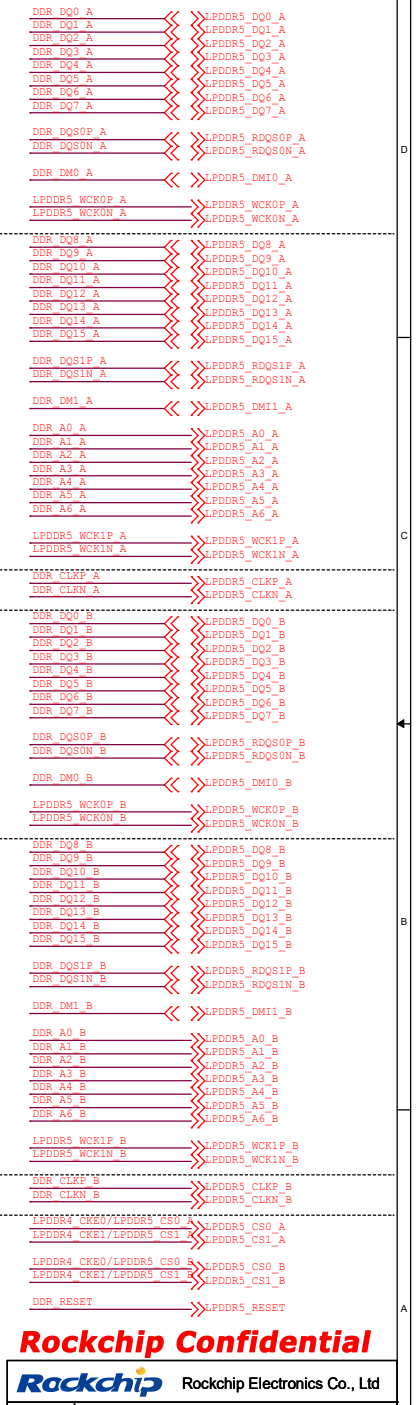
Note1:
Caps in the red line dotted box should be placed under the U1000 package

Note2:
Resistors in the red line dotted box should be placed under the U1000 package

LPDDR4/4X



LPDDR5



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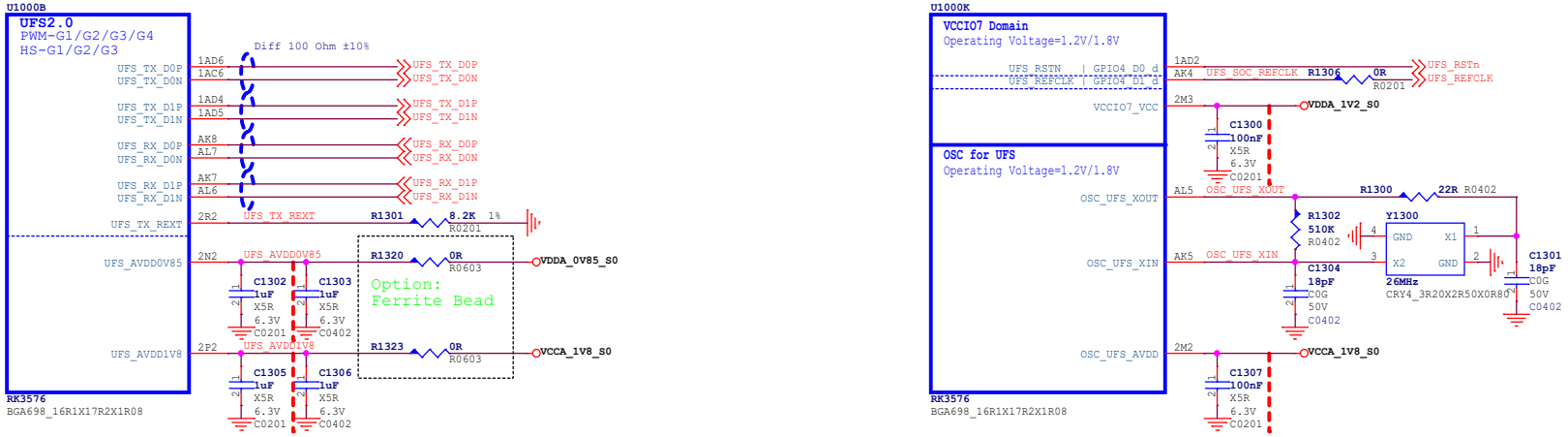
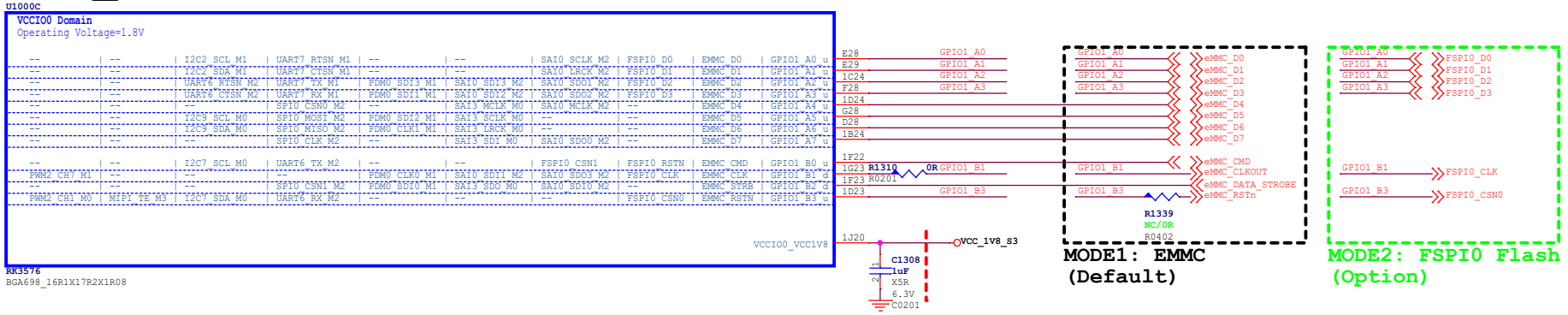
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	12.RK3576-DDR PHY		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:	Sheet: 13 of 65

RK3576_B (UFS2.0)



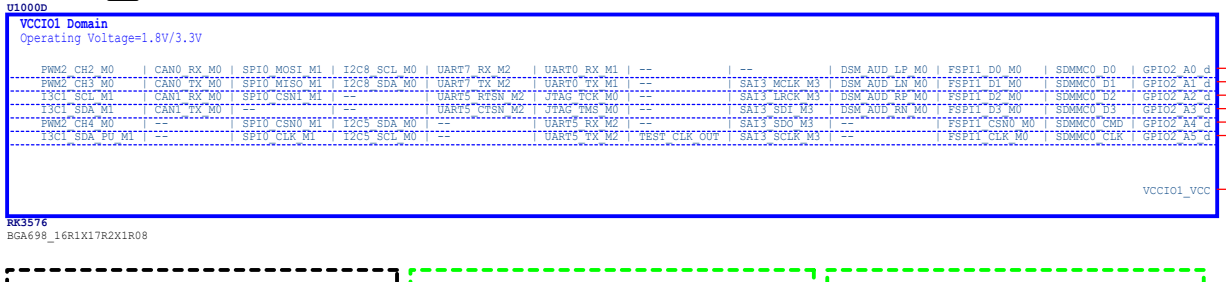
RK3576_C (VCCIO0)

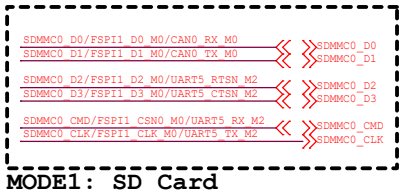


MODE1: EMMC (Default)

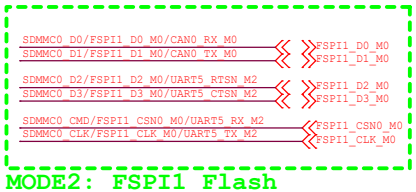
MODE2: FSPI0 Flash (Option)

RK3576_D (VCCIO1)

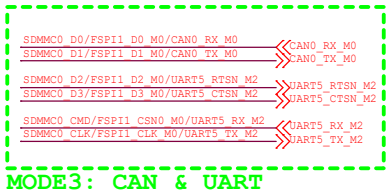




MODE1: SD Card (Default)



MODE2: FSPI1 Flash (Option)



MODE3: CAN & UART (Option)

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	13.RK3576-eMMC/UFS/SD				
Date:	Thursday, May 30, 2024		Rev:	V1.1	
Designed by:	Wesley Huang	Reviewed by:		Sheet:	14 of 65

RK3576_L (USB3/DP)

U1000L

USB3 OTG0/DP1.4 Alt
USB:USB3.2 Gen1x1 OTG0
DP :RBR/HBR/HBR2/HBR3

--	DP_TX_AUXP
--	DP_TX_AUXN
USB3_OTG0_SSRX1P	DP_TX_D0P
USB3_OTG0_SSRX1N	DP_TX_D0N
USB3_OTG0_SSTX1P	DP_TX_D1P
USB3_OTG0_SSTX1N	DP_TX_D1N
USB3_OTG0_SSRX2P	DP_TX_D2P
USB3_OTG0_SSRX2N	DP_TX_D2N
USB3_OTG0_SSTX2P	DP_TX_D3P
USB3_OTG0_SSTX2N	DP_TX_D3N
USB3_OTG0_REXT	DP_TX_REXT
USB3_OTG0_DP_TX_AVDD0V85	
USB3_OTG0_DP_TX_DVDD0V85	
USB3_OTG0_DP_TX_AVDD1V8	

RK3576
BGA698_16R1X17R2X1R08

Support: Type-C With Displayport Alternate Mode

Diff 100 Ohm ±10%
2T2 DP_TX_AUXP
2T3 DP_TX_AUXN
AK10 USB3_OTG0_SSRX1P/DP_TX_D0P
AL10 USB3_OTG0_SSRX1N/DP_TX_D0N
AL11 USB3_OTG0_SSTX1P/DP_TX_D1P
AK11 USB3_OTG0_SSTX1N/DP_TX_D1N
AK12 USB3_OTG0_SSRX2P/DP_TX_D2P
AL12 USB3_OTG0_SSRX2N/DP_TX_D2N
AL13 USB3_OTG0_SSTX2P/DP_TX_D3P
AK13 USB3_OTG0_SSTX2N/DP_TX_D3N
2T7 USB3_OTG0_DP_TX_REXT — R1400 8.2K 1% R0201
2M5, 2N5 — VDDA_0V85_S0
C1400 1uF X5R 6.3V C0201
C1401 NC/1uF X5R 6.3V C0402
2N4 — VCCA_1V8_S0
C1402 1uF X5R 6.3V C0201
C1403 NC/1uF X5R 6.3V C0402

Diff 95 Ohm ±10%
USB3_OTG0_SSRX1P/DP_TX_D0P → USB3_OTG0_SSRX1P
USB3_OTG0_SSRX1N/DP_TX_D0N → USB3_OTG0_SSRX1N
USB3_OTG0_SSTX1P/DP_TX_D1P → USB3_OTG0_SSTX1P
USB3_OTG0_SSTX1N/DP_TX_D1N → USB3_OTG0_SSTX1N
USB3_OTG0_SSRX2P/DP_TX_D2P → USB3_OTG0_SSRX2P
USB3_OTG0_SSRX2N/DP_TX_D2N → USB3_OTG0_SSRX2N
USB3_OTG0_SSTX2P/DP_TX_D3P → USB3_OTG0_SSTX2P
USB3_OTG0_SSTX2N/DP_TX_D3N → USB3_OTG0_SSTX2N

MODE1: TypeC with ALT (Default)

Diff 90 Ohm ±10%
USB3_OTG0_SSRX1P/DP_TX_D0P → USB3_OTG0_SSRX1P
USB3_OTG0_SSRX1N/DP_TX_D0N → USB3_OTG0_SSRX1N
USB3_OTG0_SSTX1P/DP_TX_D1P → USB3_OTG0_SSTX1P
USB3_OTG0_SSTX1N/DP_TX_D1N → USB3_OTG0_SSTX1N

MODE2: USB30 + DP 2Lane (Option)

Diff 100 Ohm ±10%
USB3_OTG0_SSRX2P/DP_TX_D2P → DPTX_SWAPON_D0P
USB3_OTG0_SSRX2N/DP_TX_D2N → DPTX_SWAPON_D0N
USB3_OTG0_SSTX2P/DP_TX_D3P → DPTX_SWAPON_D1P
USB3_OTG0_SSTX2N/DP_TX_D3N → DPTX_SWAPON_D1N

Diff 100 Ohm ±10%
USB3_OTG0_SSRX1P/DP_TX_D0P → DP_TX_D0P
USB3_OTG0_SSRX1N/DP_TX_D0N → DP_TX_D0N
USB3_OTG0_SSTX1P/DP_TX_D1P → DP_TX_D1P
USB3_OTG0_SSTX1N/DP_TX_D1N → DP_TX_D1N
USB3_OTG0_SSRX2P/DP_TX_D2P → DP_TX_D2P
USB3_OTG0_SSRX2N/DP_TX_D2N → DP_TX_D2N
USB3_OTG0_SSTX2P/DP_TX_D3P → DP_TX_D3P
USB3_OTG0_SSTX2N/DP_TX_D3N → DP_TX_D3N

MODE3: DP (Option)

Support 1/2/4Lane

Note: If using the DP interface to light up the eDP screen, there may be compatibility issues. Please consult RK for detail.

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_M (USB2)

U1000M

USB2 OTG0
OTG/HOST/DEVICE
HS/FS/LS
Download Port

USB2_OTG0_DP	
USB2_OTG0_DM	
USB2_OTG0_ID	
USB2_OTG0_VBUSDET	
USB2_OTG0_REXT	

USB2 OTG1
OTG/HOST/DEVICE
HS/FS/LS

USB2_OTG1_DP	
USB2_OTG1_DM	
USB2_OTG1_ID	
USB2_OTG1_VBUSDET	
USB2_OTG1_REXT	
USB2_OTG_DVDD0V75	
USB2_OTG_AVDD1V8	
USB2_OTG_AVDD3V3	

40K
40K

RK3576
BGA698_16R1X17R2X1R08

Diff 90 Ohm ±10%
AK9 USB2_OTG0_DP
AL9 USB2_OTG0_DM
2R6 Note: There is an internal pull-up resistor connected to 1.8V — USB2_OTG0_ID
2P3 — USB2_OTG0_VBUSDET
2R3 USB2_OTG0_REXT — R1401 200R 1% R0201
C1404 100nF X5R 10V C0402

Diff 90 Ohm ±10%
2T4 USB2_HOST1_DP
2T5 USB2_HOST1_DM
2T9
2T10

Note!!!
The USB2 PHY1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected

2U8 USB2_OTG1_REXT — R1402 200R 1% R0201

2P5 USB2_OTG_DVDD0V75
C1405 100nF X5R 6.3V C0201
R1407 0R R0201 — VDDA_0V75_S0
R1408 NC/0R R0201 — VDD_0V75_S3

2P4 USB2_OTG_AVDD1V8
C1406 100nF X5R 6.3V C0201
C1407 NC/1uF X5R 6.3V C0402
R1409 0R R0201 — VCCA_1V8_S0
R1410 NC/0R R0201 — VCC_1V8_S3

2P7 USB2_OTG_AVDD3V3
C1408 100nF X5R 6.3V C0201
R1412 0R R0201 — VCC_3V3_S0
R1411 NC/0R R0201 — VCC_3V3_S3

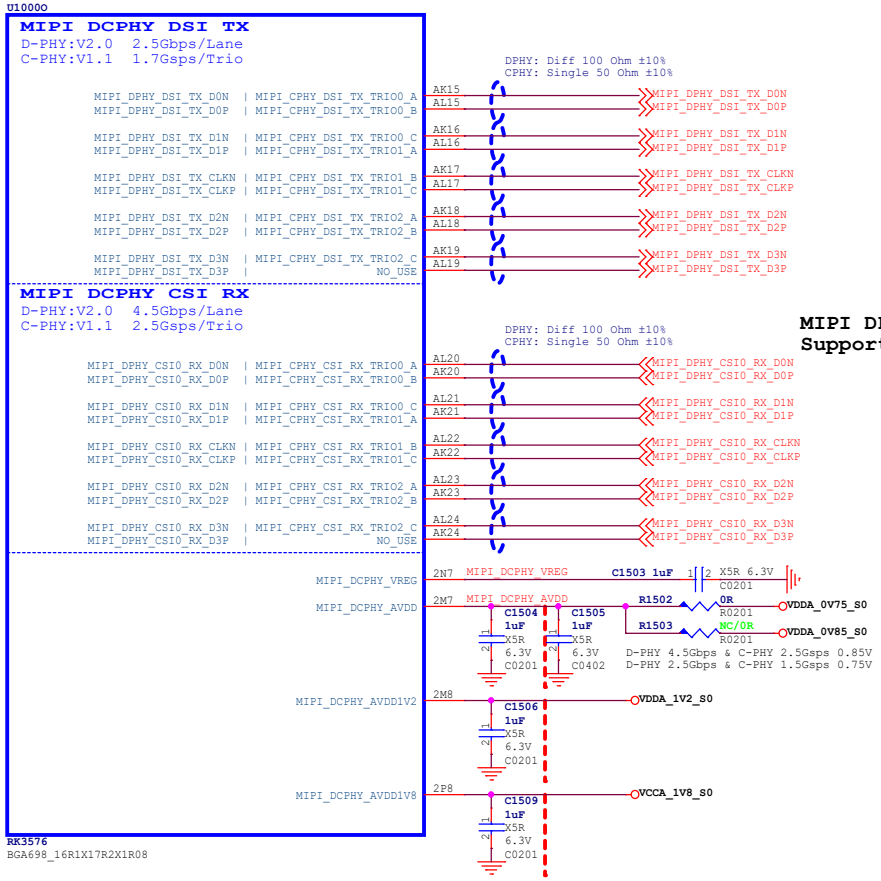
Option:
USB Wake up

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	14.RK3576-TypeC/USB		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by: Wesley Huang	Reviewed by:	Sheet:	15 of 65

RK3576_O(MIPI DCPHY)

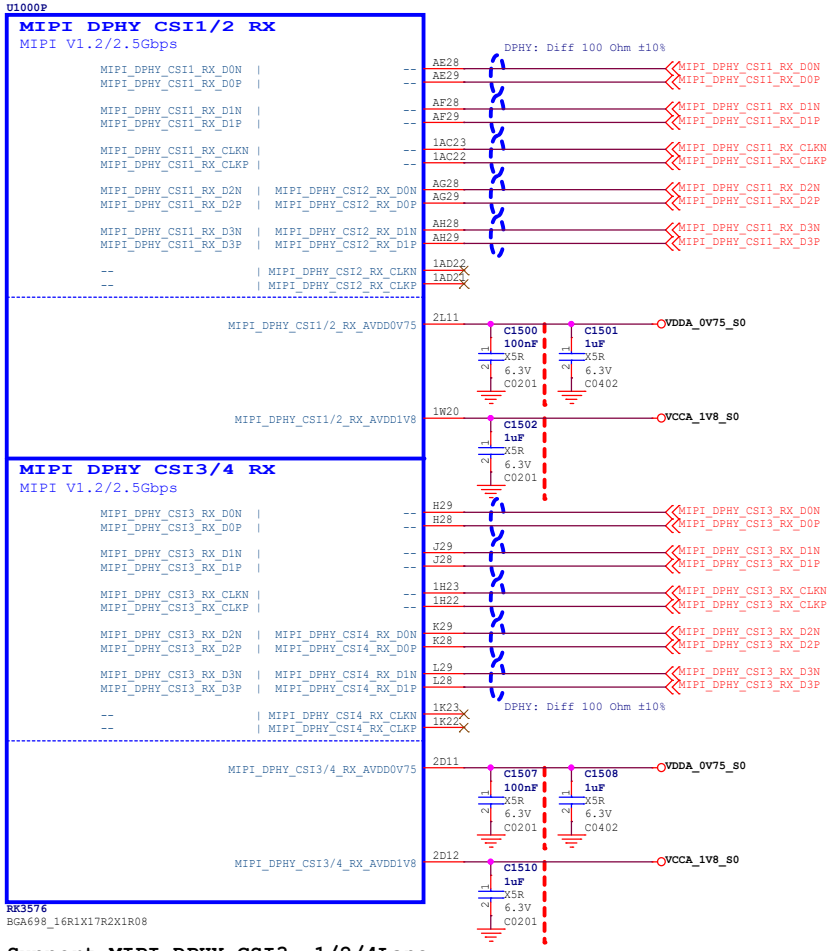


MIPI DPHY CSI0:
Support 1/2/4Lane

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_P(MIPI DPHY CSI RX)

Support MIPI DPHY CSI1: 1/2/4Lane
Support MIPI DPHY CSI2: 1/2Lane
Support: MIPI DPHY CSI1 2Lane + MIPI DPHY CSI2 2Lane



Support MIPI DPHY CSI3: 1/2/4Lane
Support MIPI DPHY CSI4: 1/2Lane
Support MIPI DPHY CSI3 2Lane + MIPI DPHY CSI4 2Lane

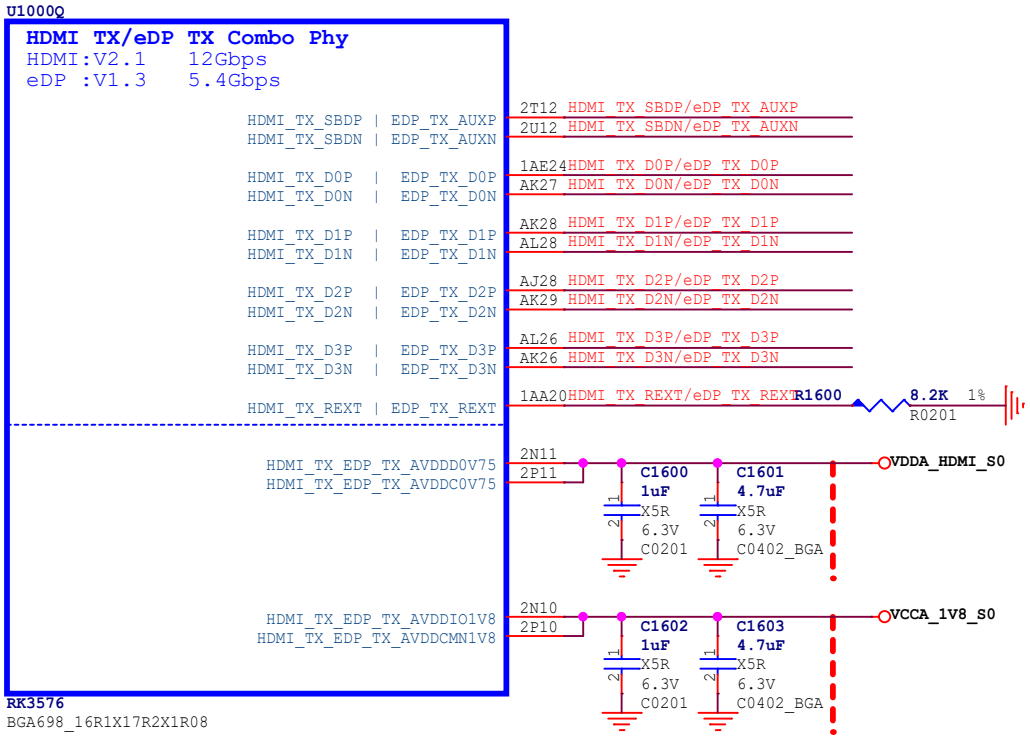
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

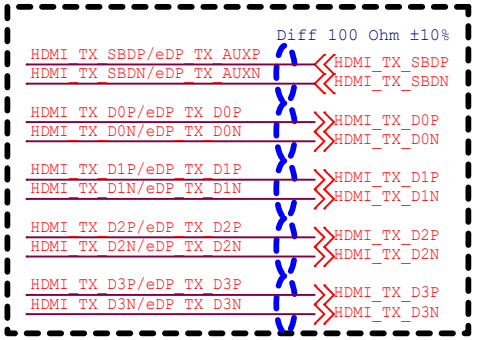
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	15.RK3576-MIPI DSI/CSI				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	16 of 65

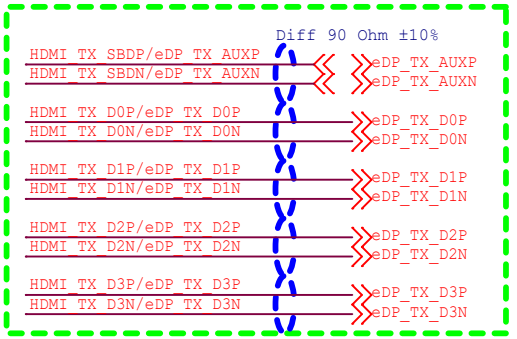
RK3576_Q(HDMI/eDP)

Note:
HDMI 2.1 supports up to 4Kx2K@120Hz





MODE1: HDMI
(Default)



MODE2: eDP
(Option)

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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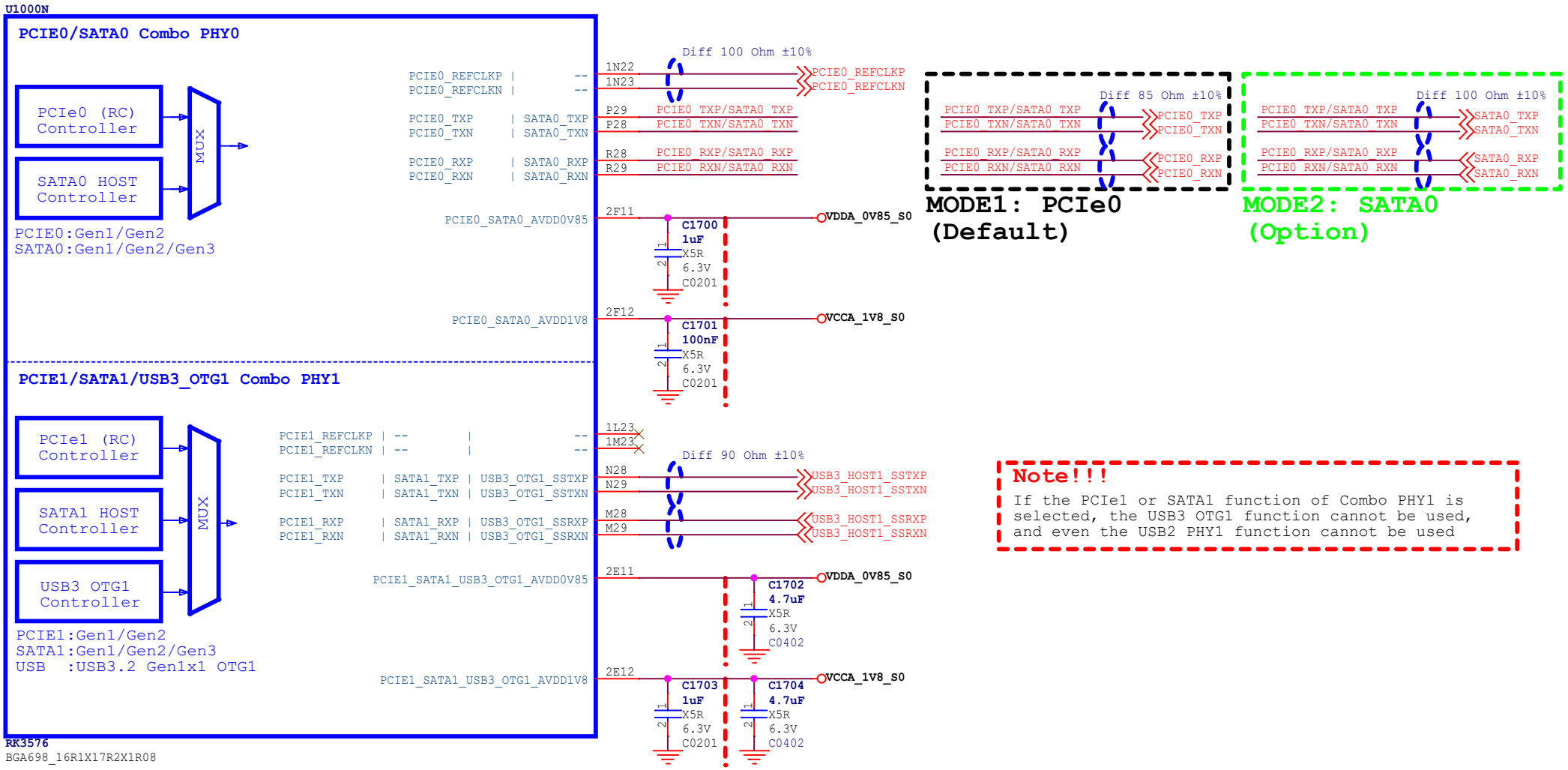
Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	16.RK3576-HDMI/eDP		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by: Wesley Huang	Reviewed by:	Sheet:	17 of 65

RK3576_N(PCIe/SATA/USB3)



Note!!!

If the PCIe1 or SATA1 function of Combo PHY1 is selected, the USB3 OTG1 function cannot be used, and even the USB2 PHY1 function cannot be used

Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	17.RK3576-PCIe/SATA/USB3		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by: Wesley Huang	Reviewed by:	Sheet:	18 of 65

RK3576_F(VCCIO2)

U1000F

VCCIO2 Domain
Operating Voltage=1.8V/3.3V

PWM2_CH5_M0	--	--	--	--	AUPLL_CLK_IN_M2	SAI4_MCLK_M0	SAI1_MCLK_M0	GPIO4_A2_d
PWM2_CH4_M1	--	I2C2_SCL_M2	UART5_RTSN_M1	SPI3_CSN0_M2	FLEXBUS1_CSN_M4	--	SAI1_SCLK_M0	GPIO4_A3_d
CAN0_TX_M2	--	I2C4_SCL_M1	UART6_TX_M0	SPI3_MOSI_M2	FLEXBUS0_D13_M1	PDM1_SDI3_M1	SAI4_SCLK_M0	GPIO4_A4_d
--	PCIE1_CLKREQN_M2	I2C2_SDA_M2	UART5_CTSN_M1	SPI4_CSN1_M2	FLEXBUS1_D12_M1	--	SAI1_LRCK_M0	GPIO4_A5_d
CAN0_RX_M2	--	I2C4_SDA_M1	UART6_RX_M0	SPI3_MISO_M2	FLEXBUS0_D14_M1	PDM1_CLK0_M1	SAI4_LRCK_M0	GPIO4_A6_d
PWM2_CH6_M0	--	--	--	SPI3_CLK_M2	--	--	SAI4_SDI_M0	GPIO4_A7_d
--	UART2_RTSN_M1	UART6_RTSN_M0	UART5_TX_M1	SPI4_CLK_M2	FLEXBUS1_D13_M1	PDM1_CLK1_M1	SAI1_SDI3_M0	SAI1_SDO1_M0	GPIO4_B0_d
--	UART2_CTSN_M1	UART6_CTSN_M0	UART5_RX_M1	SPI4_MOSI_M2	FLEXBUS1_D14_M1	PDM1_SDI2_M1	SAI1_SDI2_M0	SAI1_SDO2_M0	GPIO4_B1_d
--	--	MIPI_TE_M0	--	SPI4_MISO_M2	FLEXBUS1_D15_M1	PDM1_SDI1_M1	SAI1_SDI1_M0	SAI1_SDO3_M0	GPIO4_B2_d
PWM2_CH7_M0	--	--	SPI3_CSN1_M2	SPI4_CSN0_M2	--	PDM1_SDI0_M1	SAI4_SDO_M0	SAI1_SDI0_M0	GPIO4_B3_d
CAN1_RX_M2	--	I2C3_SDA_M0	UART2_RX_M1	--	FLEXBUS0_CSN_M4	--	--	SPDIF_RX0_M0	GPIO4_B4_d
CAN1_TX_M2	PCIE0_CLKREQN_M2	I2C3_SCL_M0	UART2_TX_M1	--	FLEXBUS0_D15_M1	--	--	SPDIF_TX0_M0	GPIO4_B5_d

RK3576
BGA698_16R1X17R2X1R08

1D6 GPIO4_A2 R1802 0R R0402 SAI1_MCLK_M0
1C6 GPIO4_A3 R1803 0R R0402 SAI1_SCLK_M0
1C5 GPIO4_A4
1B6 SAI1_LRCK_M0
1B5 GPIO4_A6
A7 GPIO4_A7
1A5 PDM1_CLK1_M1_Loopback
B7 SAI1_SDO2_M0
B6 PDM1_SDI1_M1_Loopback
1A6 SAI1_SDI0_M0
B8 I2C3_SDA_M0_Audio_LVDS
1A4 I2C3_SCL_M0_Audio_LVDS

VCCIO2_VCC 2A2 C1800 100nF X5R 6.3V C0201 VCC_3V3_S0

VCC_3V3_S0
R1800 2.2K R0402
R1801 2.2K R0402
I2C3_SDA_M0_Audio_LVDS
I2C3_SCL_M0_Audio_LVDS

GPIO4_A4 SAI4_SCLK_M0
GPIO4_A6 SAI4_LRCK_M0
GPIO4_A7 SAI4_SDI_M0

MODE1: HDMI RX Audio (Default)

GPIO4_A7 R1804 100R R0402 R1805 120R R0402 PWM2_CH6_M0_CAM

MODE2: MIPI RX Control Signal (Option)

RK3576_G(VCCIO3)

U1000G

VCCIO3 Domain
Operating Voltage=1.8V/3.3V

PWM1_CH0_M1	PCIE1_CLKREQN_M1	SPI1_CLK_M0	I2C9_SDA_M1	--	--	--	SAI3_SCLK_M1	--	SDMMC1_D0_M0	ETH1_RXD2_M1	GPIO1_B4_d
PWM1_CH1_M1	--	SPI1_MOSI_M0	I2C9_SCL_M1	--	--	--	SAI3_LRCK_M1	--	SDMMC1_D1_M0	ETH1_RXD3_M1	GPIO1_B5_d
--	PCIE0_CLKREQN_M1	SPI1_MISO_M0	--	UART3_CTSN_M2	--	--	SAI3_SDO_M1	--	SDMMC1_D2_M0	ETH1_RXCLK_M1	GPIO1_B6_d
--	--	SPI1_CSN0_M0	--	UART3_RTSN_M2	--	--	SAI3_SDI_M1	--	SDMMC1_D3_M0	ETH1_TXD2_M1	GPIO1_B7_d
PWM0_CH0_M1	--	SPI1_CSN1_M0	--	UART3_TX_M2	--	PDM0_SDI2_M2	--	--	SDMMC1_CMD_M0	ETH1_TXD3_M1	GPIO1_C0_d
--	--	--	--	UART3_RX_M2	--	PDM0_CLK0_M2	SAI3_MCLK_M1	--	SDMMC1_CLK_M0	ETH1_TXCLK_M1	GPIO1_C1_d
PWM1_CH4_M1	--	SPI2_CSN1_M1	I2C8_SCL_M1	UART4_RTSN_M1	--	--	--	FSPI1_CSN1_M1	SDMMC1_PWREN_M0	ETH1_PPSCLK_M1	GPIO1_C2_d
--	--	SPI2_CSN0_M1	I2C8_SDA_M1	UART4_CTSN_M1	--	--	--	FSPI1_CSN0_M1	SDMMC1_DETN_M0	ETH1_PPSTRIG_M1	GPIO1_C3_d
--	PCIE0_BUTTONRSTN	SPI2_MOSI_M1	UART2_RTSN_M0	UART4_TX_M1	--	--	--	FSPI1_D0_M1	--	ETH1_RXD0_M1	GPIO1_C4_d
--	PCIE1_BUTTONRSTN	SPI2_MISO_M1	UART2_CTSN_M0	UART4_RX_M1	--	--	--	FSPI1_D1_M1	--	ETH1_RXD1_M1	GPIO1_C5_d
--	SATA_CPPOD	--	I2C8_SCL_M1	UART2_TX_M0	--	PDM0_SDI0_M2	--	FSPI1_D2_M1	--	ETH1_RXCTL_M1	GPIO1_C6_d
--	SATA_CPDET	--	I2C8_SDA_M1	UART2_RX_M0	--	PDM0_SDI1_M2	--	FSPI1_D3_M1	--	ETH1_RXD0_M1	GPIO1_C7_d
--	--	--	--	UART10_TX_M1	--	--	SAI2_SDO_M0	--	--	ETH1_RXD1_M1	GPIO1_D0_d
--	--	--	I3C0_SDA_PU_M1	UART10_RX_M1	--	--	SAI2_SCLK_M0	--	--	ETH1_RXCTL_M1	GPIO1_D1_d
PWM1_CH3_M1	--	--	I3C0_SCL_M1	--	--	--	SAI2_LRCK_M0	--	--	ETH1_MDC_M1	GPIO1_D2_d
PWM1_CH4_M1	--	--	I3C0_SDA_M1	--	--	--	SAI2_SDI_M0	--	--	ETH1_MDIO_M1	GPIO1_D3_d
--	--	--	I2C5_SCL_M1	UART10_RTSN_M1	SPDIF_RX1_M2	PDM0_SDI3_M2	SAI2_MCLK_M0	--	--	ETH1_MCLK_M1	GPIO1_D4_d
CLK1_32K_OUT	SATA_MPSWITCH	SPI2_CLK_M1	I2C5_SDA_M1	UART10_CTSN_M1	SPDIF_TX1_M2	PDM0_CLK1_M2	--	FSPI1_CLK_M1	--	ETH_CLK1_25M_OUT_M1	GPIO1_D5_d

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BGA698_16R1X17R2X1R08

GPIO1_B4 SDMMC1_D0_M0
GPIO1_B5 SDMMC1_D1_M0
GPIO1_B6 SDMMC1_D2_M0
GPIO1_B7 SDMMC1_D3_M0
GPIO1_C0 SDMMC1_CMD_M0
GPIO1_C1 SDMMC1_CLK_M0

MODE1: SDIO WI-FI (Default)

GPIO1_B6 PCIE0_CLKREQn_M1_WIFI
GPIO1_B7 PCIE0_PERSTn_WIFI

MODE2: PCIe WI-FI (Option)

A28 GPIO1_B4
B27 GPIO1_B5
1A23 GPIO1_B6
A27 GPIO1_B7
B26 GPIO1_C0
1B22 R1813 0R R0402 GPIO1_C1
B29 UART4_RTSN_M1
1C23 UART4_CTSN_M1
1B23 UART4_TX_M1
B28 UART4_RX_M1
A26 WIFI_REG_ON_H
1C22 BT_REG_ON_H
C29 SAI2_SDO_M0
1D22 SAI2_SCLK_M0
1A24 SAI2_LRCK_M0
C28 SAI2_SDI_M0
1E21 HOST_WAKE_BT_H
1E22 CLK1_32K_OUT_WIFI

VCCIO3_VCC 2B10 C1801 100nF X5R 6.3V C0201 VCCIO_WL

RK3576_J(VCCIO6)

U1000J

VCCIO6 Domain
Operating Voltage=1.8V/3.3V

PWM1_CH5_M1	UART11_TX_M2	SPI4_CSN1_M0	I2C7_SCL_M3	--	HDMI_TX_CEC_M0	--	SAI4_MCLK_M2	DSM_AUD_LP_M1	GPIO4_C0_d
PWM0_CH1_M1	UART11_RX_M2	ESPI_TX_HPDIN_M0	I2C7_SDA_M3	PCIE1_CLKREQN_M3	HDMI_TX_HPDIN_M0	--	--	DSM_AUD_LN_M1	GPIO4_C1_d
PWM2_CH0_M1	UART9_TX_M2	CAN0_TX_M1	I2C2_SCL_M3	--	HDMI_TX_SCL	--	--	DSM_AUD_RF_M1	GPIO4_C2_d
PWM2_CH1_M1	UART9_RX_M2	CAN0_RX_M1	I2C2_SDA_M3	--	HDMI_TX_SDA	--	--	DSM_AUD_RN_M1	GPIO4_C3_d
PWM2_CH6_M1	UART6_TX_M3	SPI4_CSN0_M0	I2C3_SCL_M3	DP_HPDIN_M0	--	--	SAI4_LRCK_M2	ISP_PRELIGHT_TRIG_M1	GPIO4_C4_d
PWM2_CH5_M1	UART6_RX_M3	SPI4_MOSI_M0	I2C3_SDA_M3	SATA1_ACTLED_M1	--	VP0_SYNC_OUT	SAI4_SDO_M2	ISP_FLASH_TRIGOUT_M1	GPIO4_C5_d
PWM2_CH2_M1	CAN1_TX_M1	SPI4_MISO_M0	I2C6_SCL_M3	SATA0_ACTLED_M1	PCIE0_CLKREQN_M3	VP1_SYNC_OUT	SAI4_SDI_M2	--	GPIO4_C6_d
PWM2_CH3_M1	CAN1_RX_M1	SPI4_CLK_M0	I2C6_SDA_M3	--	--	VP2_SYNC_OUT	SAI4_SCLK_M2	--	GPIO4_C7_d

RK3576
BGA698_16R1X17R2X1R08

C1803 1nF X5R 25V C0201
AK3 HDMI_TX_CEC_M0
AK2 HDMI_TX_HPDIN_M0
AL2 HDMI_TX_SCL
1AE2 HDMI_TX_SDA
AL3 GPIO4_C4
AK1 GPIO4_C5
1AE1 HDMI_TX_ON_H
AJ1 4G_DISABLE

VCCIO6_VCC 2N3 C1802 100nF X5R 6.3V C0201 VCC_3V3_S0

GPIO4_C4 TYPEC_DPTX_AUX_PUPDCTL1
GPIO4_C5 TYPEC_DPTX_AUX_PUPDCTL2

MODE1: TYPEC Control Signal (Default)

GPIO4_C4 DP_HPDIN
GPIO4_C5 DP_PWREN_H
C1804 1nF X5R 25V C0201

MODE2: DP Control Signal (Option)

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	18.RK3576-GPIO VCCIO2/3/6		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:	Sheet: 19 of 65

RK3576_H(VCCIO4)

U1000H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

--	--	I2C4_SCL_M2	SPI4_CSN1_M3	UART8_TX_M1	--	SAI0_SDO0_M0	ETH0_RXD0_M1	SDMMC1_D0_M1	VI_CIF_D15	GPIO2_A6_d
--	--	I2C4_SDA_M2	--	UART8_RX_M1	--	SAI0_SDO1_M0	ETH0_TXCTL_M1	SDMMC1_D1_M1	VI_CIF_D14	GPIO2_A7_d
--	--	--	--	UART1_TX_M1	PDM0_SDI3_M3	SAI0_SDI0_M0	ETH0_TXD1_M1	SDMMC1_D2_M1	VI_CIF_D13	GPIO2_B0_d
--	--	--	--	UART1_RX_M1	PDM0_SDI2_M3	SAI0_SDI1_M0	ETH0_TXD0_M1	SDMMC1_D3_M1	VI_CIF_D12	GPIO2_B1_d
--	--	PCIE0_CLKREQn_M0	SPI4_CSN0_M3	UART1_CTSN_M1	PDM0_SDI1_M3	SAI0_SDI2_M0	ETH0_TXD3_M1	SDMMC1_CMD_M1	VI_CIF_D11	GPIO2_B2_d
--	--	PCIE1_CLKREQn_M0	SPI4_CLK_M3	UART1_RTSN_M1	PDM0_CLK1_M3	SAI0_SDO2_M0	ETH0_TXCLK_M1	SDMMC1_CLK_M1	VI_CIF_D10	GPIO2_B3_d
--	SATA0_ACTLED_M0	--	SPI4_MOSI_M3	UART7_CTSN_M0	PDM0_SDI0_M3	SAI0_SDI3_M0	ETH0_TXD2_M1	SDMMC1_PWREN_M1	VI_CIF_D9	GPIO2_B4_d
--	SATA1_ACTLED_M0	--	SPI4_MISO_M3	UART7_RTSN_M0	PDM0_CLK0_M3	SAI0_MCLK_M0	ETH0_RXCLK_M1	SDMMC1_DETN_M1	VI_CIF_D8	GPIO2_B5_d
--	--	I2C8_SCL_M2	UART8_RTSN_M1	UART7_TX_M0	--	SAI0_SCLK_M0	ETH0_RXD3_M1	ETH1_PTP_REFCLK_M1	VI_CIF_D7	GPIO2_B6_d
--	--	I2C8_SDA_M2	UART8_CTSN_M1	UART7_RX_M0	--	SAI0_LRCK_M0	ETH0_RXD2_M1	--	VI_CIF_D6	GPIO2_B7_d
PWM1_CH0_M2	--	--	--	UART9_RX_M0	PDM1_SDI1_M0	--	ETH0_PTP_REFCLK_M1	ETH1_RXD2_M0	VI_CIF_D5	GPIO2_C0_d
PWM1_CH1_M2	--	--	SPI1_CSN1_M1	UART9_TX_M0	PDM1_CLK1_M0	SAI2_MCLK_M1	ETH0_PPSCLK_M1	ETH1_RXD3_M0	VI_CIF_D4	GPIO2_C1_d
PWM1_CH2_M2	--	--	SPI1_MOSI_M1	UART11_CTSN_M1	PDM1_SDI2_M0	SAI2_SCLK_M1	ETH0_PPSTRIG_M1	ETH1_RXCLK_M0	VI_CIF_D3	GPIO2_C2_d
PWM0_CH0_M2	--	--	SPI1_MISO_M1	UART11_RTSN_M1	PDM1_SDI3_M0	SAI2_LRCK_M1	--	ETH1_RXD2_M0	VI_CIF_D2	GPIO2_C3_d
PWM1_CH3_M2	--	--	SPI1_CSN0_M1	UART11_TX_M1	PDM1_SDO_M0	SAI2_SDO_M1	--	ETH1_RXD3_M0	VI_CIF_D1	GPIO2_C4_d
PWM0_CH3_M2	--	--	SPI1_CLK_M1	UART11_RX_M1	PDM1_CLK0_M0	SAI2_SDI_M1	--	ETH1_RXCLK_M0	VI_CIF_D0	GPIO2_C5_d
PWM1_CH4_M2	--	I2C5_SCL_M2	--	UART4_CTSN_M0	--	SAI4_SCLK_M3	--	ETH1_TXD0_M0	--	GPIO2_C6_d
PWM0_CH4_M2	--	I2C5_SDA_M2	--	UART4_RTSN_M0	--	SAI4_LRCK_M3	--	ETH1_TXD1_M0	--	GPIO2_C7_d
PWM2_CH0_M2	--	I2C6_SCL_M2	--	UART4_TX_M0	--	SAI4_SDI_M3	--	ETH1_TXCTL_M0	--	GPIO2_D0_d
PWM2_CH1_M2	--	I2C6_SDA_M2	--	UART4_RX_M0	--	SAI4_SDO_M3	--	ETH1_RXD0_M0	--	GPIO2_D1_d
PWM2_CH2_M2	I3C1_SCL_M0	--	--	UART6_TX_M1	--	SAI4_MCLK_M3	--	ETH1_RXD1_M0	CAM_CLKU_OUT_M1	GPIO2_D2_d
PWM2_CH3_M2	I3C1_SDA_M0	--	--	UART6_RX_M1	--	--	--	ETH1_RXCTL_M0	--	GPIO2_D3_d
PWM2_CH4_M2	--	I2C9_SDA_M2	--	UART6_RTSN_M1	--	--	--	ETH1_MDC_M0	ISP_PRELIGHT_TRIG_M0	GPIO2_D4_d
PWM2_CH5_M2	--	I2C9_SCL_M2	--	UART6_CTSN_M1	--	--	--	ETH1_MDIO_M0	ISP_FLASH_TRIGOUT_M0	GPIO2_D5_d
PWM2_CH6_M2	I3C1_SDA_PU_M0	--	--	UART9_RTSN_M0	SPDIF_RX0_M2	SAI3_MCLK_M2	ETH0_MCLK_M1	ETH_CLK1_25M_OUT_M0	CAM_CLKL_OUT_M1	GPIO2_D6_d
PWM2_CH7_M2	--	--	SPI3_CSN1_M0	UART9_CTSN_M0	SPDIF_TX0_M2	SAI3_SDO3_M0	ETH_CLK0_25M_OUT_M1	ETH1_MCLK_M0	CAM_CLKZ_OUT_M1	GPIO2_D7_d
--	--	I2C7_SCL_M1	SPI3_CLK_M0	UART3_TX_M0	--	SAI3_SCLK_M2	ETH0_MDIO_M1	--	VI_CIF_HREF	GPIO3_A0_d
--	--	I2C7_SDA_M1	SPI3_MOSI_M0	UART3_RX_M0	--	SAI3_LRCK_M2	ETH0_MDC_M1	ETH1_PPSTRIG_M0	VI_CIF_VSYNC	GPIO3_A1_d
--	MIPI_TE_M1	CAN1_TX_M3	SPI3_MISO_M0	UART3_CTSN_M0	SPDIF_RX1_M1	SAI3_SDO_M2	ETH0_RXCTL_M1	ETH1_PPSCLK_M0	VI_CIF_CLKO	GPIO3_A2_d
--	--	CAN1_RX_M3	SPI3_CSN0_M0	UART3_RTSN_M0	SPDIF_TX1_M1	SAI3_SDI_M2	ETH0_RXD1_M1	ETH1_PTP_REFCLK_M0	VI_CIF_CLKI	GPIO3_A3_d

RK3576

BGA698_16R1X17R2X1R08

VCCIO4_VCC

2A7

C1900 NC/100nF X5R 6.3V C0201

C1901 1uF X5R 6.3V C0201

VCC_3V3_S0

MODE1: HP Control(Default)

GPIO2_A6 → HP_CTL_H

MODE2: LVDS Fun(Option)

GPIO2_A6 → GM_RESX_EN

B22 GPIO2_A6 → SPK_CTL_H

B19 → GSENSOR_INT_L

1A18 → PCIE0_PERSTn

1A17 → PCIE0_CLKREQn_M0

1B16 → GMAC0_RSTn

A19 → GMAC1_RSTn

1C18 GPIO2_B5

A21 → USB_OTG0_PWREN_H

B21 GPIO2_B7

A17 → GMAC1_RXD2_M0

1A15 → GMAC1_RXD3_M0

1D15 → GMAC1_RXCLK_M0

A15 GPIO2_C3

1A13 GPIO2_C4

1C15 GPIO2_C5

1A14 GPIO2_C6 R1915 0R R0402 → GMAC1_TXD0_M0

B15 GPIO2_C7 R1918 0R R0402 → GMAC1_TXD1_M0

B16 GPIO2_D0 R1919 0R R0402 → GMAC1_TXCTL_M0

1A16 → GMAC1_RXD0_M0

B17 → GMAC1_RXD1_M0

B18 → GMAC1_RXCTL_M0

1B13 GPIO2_D4 R1920 0R R0402 → GMAC1_MDC_M0

1B15 → GMAC1_MDIO_M0

1D18 GPIO2_D6 R1911 0R R0402 → ETH_CLK1_25M_OUT_M0

1E15 GPIO2_D7 R1949 0R R0402 → GMAC1_MCLKINOUT_M0

1D16 → I2C7_SCL_M1_Sensor

1B18 → I2C7_SDA_M1_Sensor

1A20 GPIO3_A2

1A19 → SPDIF_TX1_M1

VCC_3V3_S0

R1916 2.2K R0402 I2C7_SCL_M1_Sensor

R1917 2.2K R0402 I2C7_SDA_M1_Sensor

MODE1: CAM RX Signal(Default)

GPIO2_B5 → MIPI_DPHY_CSI_CAM1_RST_H

MODE2: HDMI RX(Option)

GPIO2_B5 → RK628_HDMIRX_RST_L

MODE1: HP Control(Default)

GPIO2_B7 → HP_DET_L

MODE2: LVDS Fun(Option)

GPIO2_B7 → GM_IRQ

MODE1: RGMII1(Default)

GPIO2_C3 R1912 0R R0402 → GMAC1_TXD2_M0

GPIO2_C4 R1913 0R R0402 → GMAC1_TXD3_M0

GPIO2_C5 R1914 0R R0402 → GMAC1_TXCLK_M0

MODE2: MIC Array(Option)

GPIO2_C3 → PDM1_SDI3_M0

GPIO2_C4 → PDM1_SDI0_M0

GPIO2_C5 → PDM1_CLK0_M0

MODE1: SPDIF RX

GPIO3_A2 → SPDIF_RX1_M1

MODE2: MIPI LCD TE Fun(Option)

GPIO3_A2 → MIPI_TE_M1

MODE3: LVDS Fun(Option)

GPIO3_A2 → LVDS_BL_H

RK3576_I(VCCIO5)

U1000I

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH0_M3	--	SPI2_CLK_M2	UART1_CTSN_M2	FLEXBUS0_CSN_M0	--	FLEXBUS1_D11	DSMC_RDYN	SAI4_SDI_M1	ETH_CLK0_25M_OUT_M0	VO_EBC_SDSHR	VO_LCDC_D23	GPIO3_A4_d
PWM1_CH1_M3	--	SPI2_CSN1_M2	UART1_RTSN_M2	--	--	FLEXBUS0_D7	DSMC_DATA15	PDM1_SDI3_M2	ETH0_MDIO_M0	VO_EBC_GDSF	VO_LCDC_D22	GPIO3_A5_d
PWM1_CH2_M3	--	UART10_CTSN_M0	UART1_RX_M2	--	--	FLEXBUS0_D6	DSMC_DATA14	PDM1_SDI2_M2	ETH0_MDC_M0	VO_EBC_GDOE	VO_LCDC_D21	GPIO3_A6_d
--	--	UART10_RTSN_M0	UART1_TX_M2	--	--	FLEXBUS0_D5	DSMC_DATA13	PDM1_CLK1_M2	ETH0_RXCTL_M0	VO_EBC_VCOM	VO_LCDC_D20	GPIO3_A7_d
PWM0_CH0_M3	--	SPI2_MOSI_M2	UART10_RX_M0	--	--	FLEXBUS0_D8	DSMC_CSN1	SAI4_MCLK_M1	ETH0_MCLK_M0	VO_EBC_SDCE3	VO_LCDC_D19	GPIO3_B0_d
PWM1_CH3_M3	--	SPI4_CSN0_M1	UART10_TX_M0	--	--	FLEXBUS0_D4	DSMC_DATA12	PDM1_CLK0_M2	ETH0_RXD1_M0	VO_EBC_SDCE2	VO_LCDC_D18	GPIO3_B1_d
--	I2C8_SDA_M3	--	UART9_RX_M1	--	--	FLEXBUS0_D3	DSMC_DATA11	PDM1_SDI1_M2	ETH0_RXD0_M0	VO_EBC_SDCE1	VO_LCDC_D17	GPIO3_B2_d
--	I2C8_SCL_M3	--	UART9_TX_M1	--	--	FLEXBUS0_D2	DSMC_DATA10	PDM1_SDI0_M2	ETH0_TXCTL_M0	VO_EBC_SDCE0	VO_LCDC_D16	GPIO3_B3_d
PWM1_CH4_M3	--	--	UART9_RTSN_M1	--	--	FLEXBUS0_D1	DSMC_DATA9	SPDIF_RX1_M0	ETH0_TXD1_M0	VO_EBC_SDDO15	VO_LCDC_D15	GPIO3_B4_d
PWM1_CH5_M3	--	--	UART9_CTSN_M1	--	--	FLEXBUS0_D0	DSMC_DATA8	SPDIF_TX1_M0	ETH0_TXD0_M0	VO_EBC_SDDO14	VO_LCDC_D14	GPIO3_B5_d
PWM0_CH1_M3	--	SPI3_CSN0_M1	--	--	--	FLEXBUS0_CLK	DSMC_DQS1	--	ETH0_TXCLK_M0	VO_EBC_SDDO13	VO_LCDC_D13	GPIO3_B6_d
--	I2C4_SDA_M3	UART3_CTSN_M1	UART2_RX_M2	FLEXBUS1_CSN_M0	--	FLEXBUS1_D10	DSMC_DQS0	SAI1_SDI0_M1	ETH0_PPSTRIG_M0	VO_EBC_SDDO12	VO_LCDC_D12	GPIO3_B7_d
--	I2C4_SCL_M3	UART3_RTSN_M1	UART2_TX_M2	--	--	FLEXBUS1_D9	DSMC_DATA7	SAI1_SDO3_M1	ETH0_PPSCLK_M0	VO_EBC_SDDO11	VO_LCDC_D11	GPIO3_C0_d
CAN0_RX_M3	I2C5_SDA_M3	SPI2_MISO_M2	UART11_RX_M0	--	--	FLEXBUS1_D8	DSMC_DATA6	SAI1_SDO1_M1	ETH1_PTP_REFCLK_M0	VO_EBC_SDDO10	VO_LCDC_D10	GPIO3_C1_d
CAN0_TX_M3	I2C9_SCL_M3	SPI4_MISO_M1	UART11_RTSN_M0	--	--	FLEXBUS1_D9	DSMC_INT1	SAI2_SCLK_M2	ETH0_RXD3_M0	VO_EBC_SDDO9	VO_LCDC_D9	GPIO3_C2_d
PWM2_CH1_M3	I2C9_SDA_M3	SPI4_MOSI_M1	UART11_CTSN_M0	FLEXBUS0_CSN_M2	--	FLEXBUS1_D10	DSMC_INT3	SAI2_LRCK_M2	ETH0_TXD2_M0	VO_EBC_SDDO8	VO_LCDC_D8	GPIO3_C3_d
CAN0_TX_M3	I2C5_SCL_M3	SPI2_CSN0_M2	UART11_TX_M0	--	--	FLEXBUS1_D7	DSMC_DATA5	SAI1_SDO1_M1	--	VO_EBC_SDDO7	VO_LCDC_D7	GPIO3_C4_d
PWM2_CH2_M3	--	SPI1_MISO_M2	UART8_RX_M0	--	--	FLEXBUS1_D6	DSMC_DATA4	SAI1_SDO0_M1	--	VO_EBC_SDDO6	VO_LCDC_D6	GPIO3_C5_d
--	--	SPI1_MOSI_M2	UART8_TX_M0	--	--	FLEXBUS1_D5	DSMC_DATA3	SAI1_LRCK_M1	--	VO_EBC_SDDO5	VO_LCDC_D5	GPIO3_C6_d
--	--	SPI1_CLK_M2	UART8_RTSN_M0	--	--	FLEXBUS1_D4	DSMC_DATA2	SAI1_SCLK_M1	--	VO_EBC_SDDO4	VO_LCDC_D4	GPIO3_C7_d
PWM2_CH3_M3	--	SPI1_CSN0_M2	UART8_CTSN_M0	--	--	FLEXBUS1_D3	DSMC_DATA1	SAI1_MCLK_M1	--	VO_EBC_SDDO3	VO_LCDC_D3	GPIO3_D0_d
--	I3C1_SDA_PU_M2	SPI4_CLK_M1	--	FLEXBUS1_CSN_M2	--	FLEXBUS1_D11	DSMC_CSN2	SAI2_MCLK_M2	ETH0_RXCLK_M0	VO_EBC_SDDO2	VO_LCDC_D2	GPIO3_D1_d
PWM2_CH4_M3	I3C1_SDA_M2	SPI4_CSN1_M1	UART12_RTSN_M2	FLEXBUS0_CSN_M3	FLEXBUS1_D15_M0	FLEXBUS0_D12	DSMC_CSN3	SAI2_SDI_M2	ETH0_RXD3_M0	VO_EBC_SDDO1	VO_LCDC_D1	GPIO3_D2_d
PWM2_CH5_M3	I3C1_SCL_M2	--	UART12_CTSN_M2	--	--	FLEXBUS1_D2	DSMC_CSN0	SAI2_SDO_M2	ETH0_RXD2_M0	VO_EBC_SDDO0	VO_LCDC_D0	GPIO3_D3_d
--	I2C3_SCL_M2	SPI3_CLK_M1	UART5_RX_M0	--	--	FLEXBUS1_D1	DSMC_DATA0	SAI1_SDI1_M1	--	VO_EBC_SDLE	VO_LCDC_DEN	GPIO3_D4_d
--	I2C3_SDA_M2	SPI3_MISO_M1	UART5_TX_M0	--	--	FLEXBUS1_D0	DSMC_CLKF	SAI1_SDI2_M1	--	VO_EBC_GDCLK	VO_LCDC_HSYNC	GPIO3_D5_d
PWM2_CH6_M3	--	SPI3_MOSI_M1	UART5_CTSN_M0	--	--	FLEXBUS1_CLK	DSMC_CLKN	SAI1_SDI3_M1	--	VO_EBC_SDCLK	VO_LCDC_VSYNC	GPIO3_D6_d
PWM2_CH7_M3	--	SPI3_CSN1_M1	UART5_RTSN_M0	FLEXBUS1_CSN_M1	FLEXBUS1_D12_M0	FLEXBUS1_D15_M0	DSMC_RESETN	SAI4_SCLK_M1	CAM_CLK1_OUT_M0	VO_EBC_SDOE	VO_LCDC_CLK	GPIO3_D7_d
MIPI_TE_M2	I2C7_SCL_M2	SPI1_CSN1_M2	UART3_TX_M1	FLEXBUS1_CSN_M3	FLEXBUS1_D14_M0	FLEXBUS0_D13_M0	DSMC_INT0	SAI4_LRCK_M1	CAM_CLK2_OUT_M0	SPDIF_RX0_M1	--	GPIO4_A0_d
--	I2C7_SDA_M2	--	UART3_RX_M1	FLEXBUS0_CSN_M1	FLEXBUS1_D13_M0	FLEXBUS0_D14_M0	DSMC_INT2	SAI4_SDO_M1	CAM_CLK2_OUT_M0	SPDIF_TX0_M1	VO_POST_EMPTY	GPIO4_A1_d

RK3576

BGA698_16R1X17R2X1R08

VCCIO5_VCC_0

VCCIO5_VCC_1

2A4

2A5

C1902 NC/100nF X5R 6.3V C0201

C1903 1uF X5R 6.3V C0201

VCC_1V8_S0

1D13 GPIO3_A4 R1923 0R R0402 → ETH_CLK0_25M_OUT_M0

A9 → GMAC0_MDIO_M0

1A7 GPIO3_A6 R1925 0R R0402 → GMAC0_MDC_M0

B13 → GMAC0_RXCTL_M0

B14 GPIO3_B0 → MIPI_DPHY_CSI_CAM1_PDN_H

1A11 → GMAC0_RXD1_M0

A13 → GMAC0_RXD0_M0

A11 GPIO3_B3 R1928 0R R0402 → GMAC0_TXCTL_M0

B10 GPIO3_B4 R1929 0R R0402 → GMAC0_TXD1_M0

1A9 GPIO3_B5 R1930 0R R0402 → GMAC0_TXD0_M0

B11 GPIO3_B6 R1931 0R R0402 → GMAC0_TXCLK_M0

1D12 → I2C4_SDA_M3_MIPI_CAM0/2

GPIO3_B0 → RK628_HDMIRX_DET_L

Option: HDMI RX

1E9 → I2C4_SCL_M3_MIPI_CAM0/2

1B10 → I2C5_SDA_M3_MIPI_CAM1/HDMI_RX

B9 GPIO3_C2 R1932 0R R0402 → GMAC0_TXD3_M0

1A8 GPIO3_C3 R1933 0R R0402 → GMAC0_TXD2_M0

1D9 → I2C5_SCL_M3_MIPI_CAM1/HDMI_RX

1B9 GPIO3_C5 → MIPI_DPHY_CSI_CAM1_PWREN_H

1D7 → MIPI_DPHY_CSI_CAM2_PWREN_H

1C7 → MIPI_DCPHY_CSI_CAM0_PDN_H

GPIO3_C5 → RK628_HDMIRX_PWREN_H

Option: HDMI RX

1C12 → MIPI_DPHY_CSI_CAM0_PWREN_H

1A12 → GMAC0_RXCLK_M0

1A10 → GMAC0_RXD3_M0

B12 → GMAC0_RXD2_M0

1E12 → MIPI_DPHY_CSI_CAM2_PDN_H

1D10 → MIPI_DCPHY_CSI_CAM0_RST_H

1C10 → MIPI_DPHY_CSI_CAM2_RST_H

1E7 GPIO3_D7 R1951 0R R0402 → MIPI_DCPHY_CSI_CAM0_CLKOUT

1B12 GPIO4_A0 R1952 0R R0402 → MIPI_DPHY_CSI_CAM1_CLKOUT

1B7 GPIO4_A1 R1953 0R R0402 → MIPI_DPHY_CSI_CAM2_CLKOUT

GPIO4_A0 → RK628_HDMIRX_INT_H

Option: HDMI RX

VCC_1V8_S0

R1926 2.2K R0402 I2C4_SDA_M3_MIPI_CAM0/2

R1927 2.2K R0402 I2C4_SCL_M3_MIPI_CAM0/2

VCC_1V8_S0

R1934 2.2K R0402 I2C5_SDA_M3_MIPI_CAM1/HDMI_RX

R1935 2.2K R0402 I2C5_SCL_M3_MIPI_CAM1/HDMI_RX

Note:

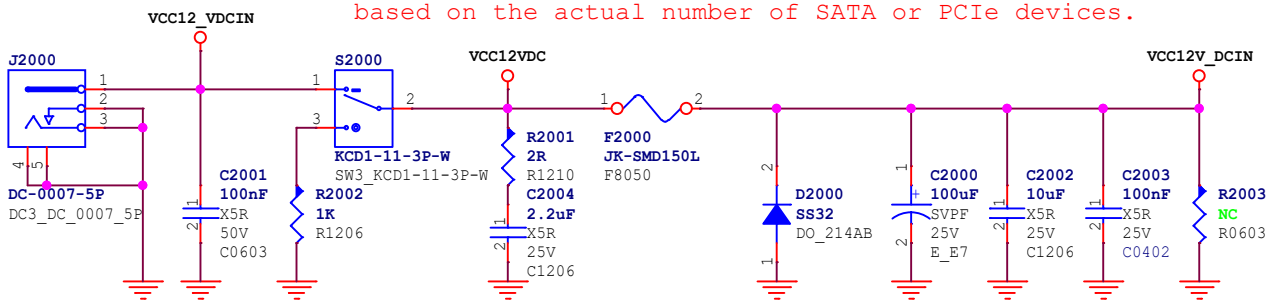
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Rockchip Confidential

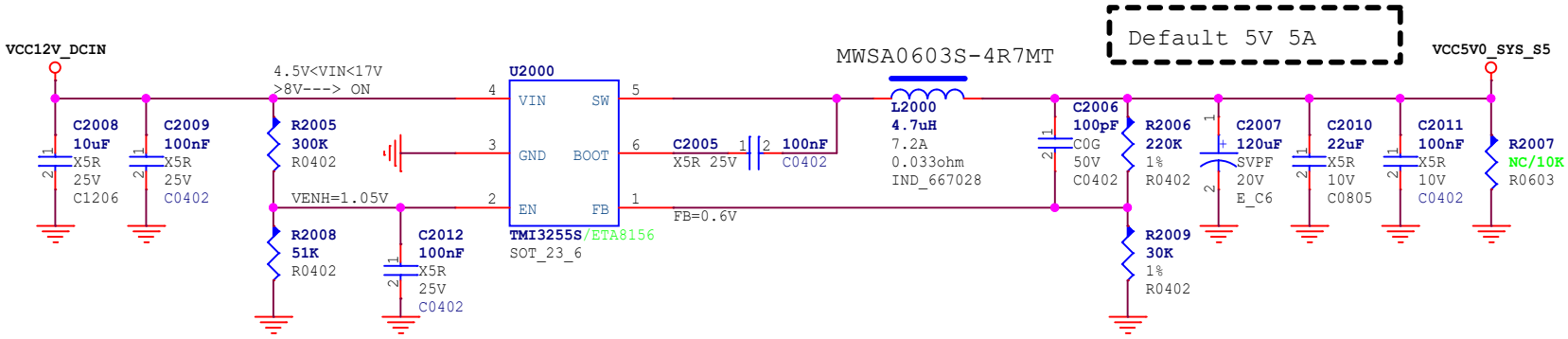
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	19.RK3576-GPIO VCCIO4/5		
Date:	Tuesday, June 04, 2024	Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:	
Sheet:	20 of 65		

12V/3A DCIN

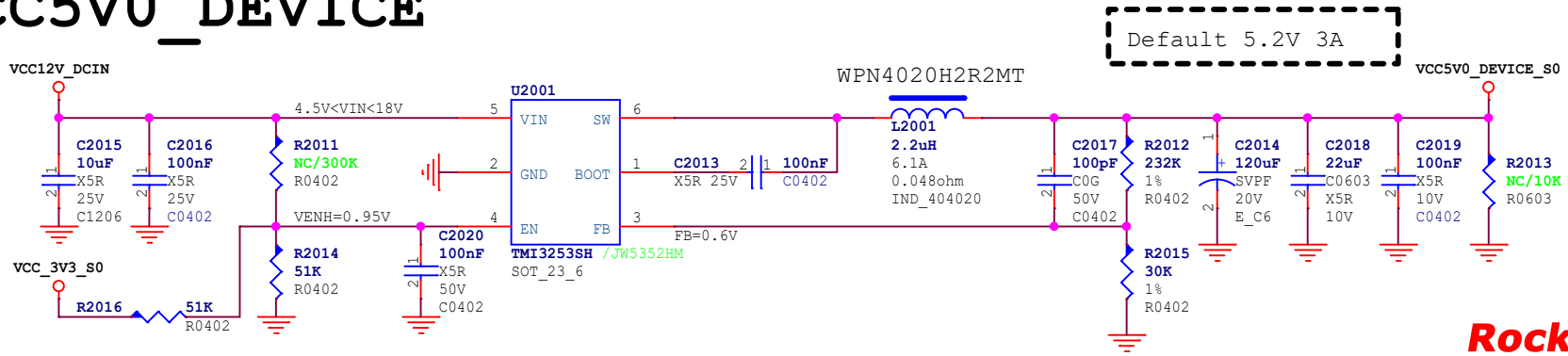
Note:
When supporting multiple SATA or PCIe devices, the current must be designed based on the actual number of SATA or PCIe devices.



VCC5V0_SYS



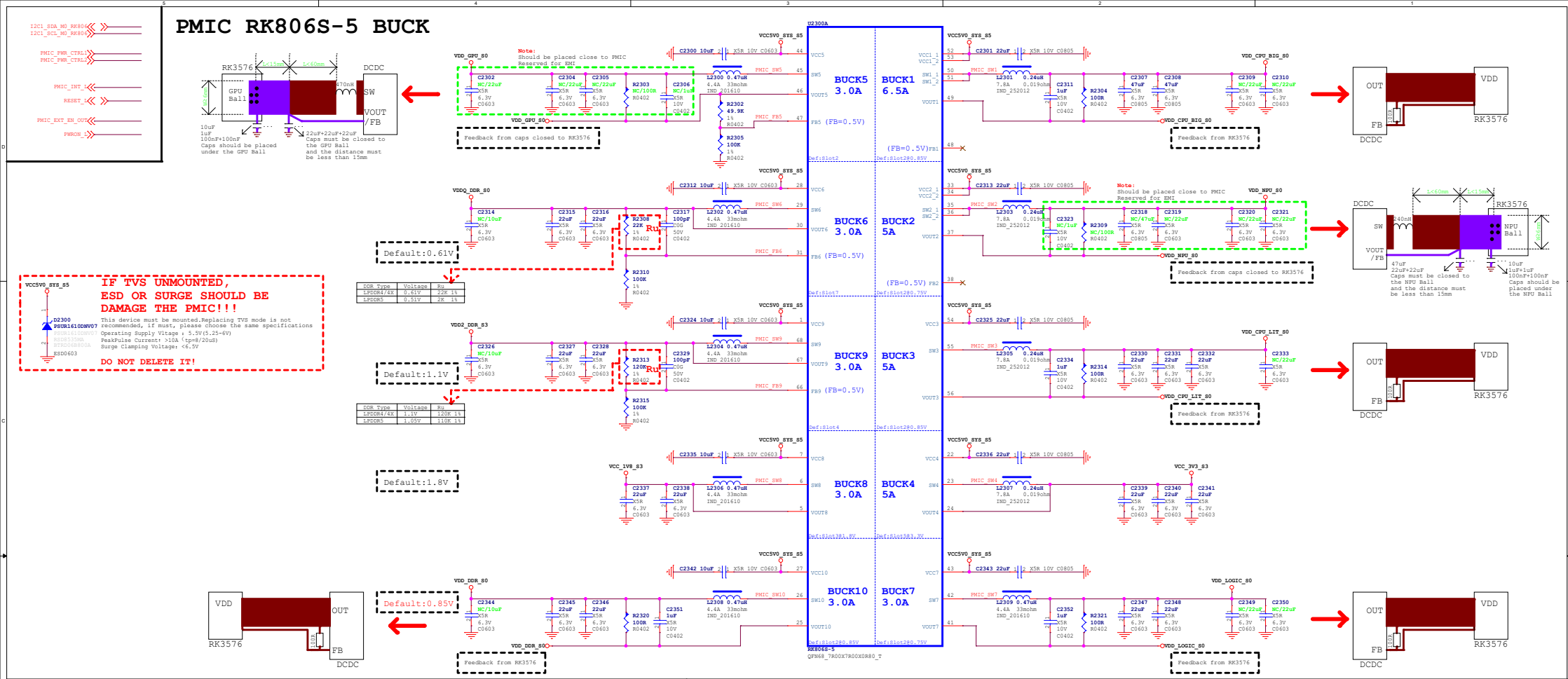
VCC5V0_DEVICE



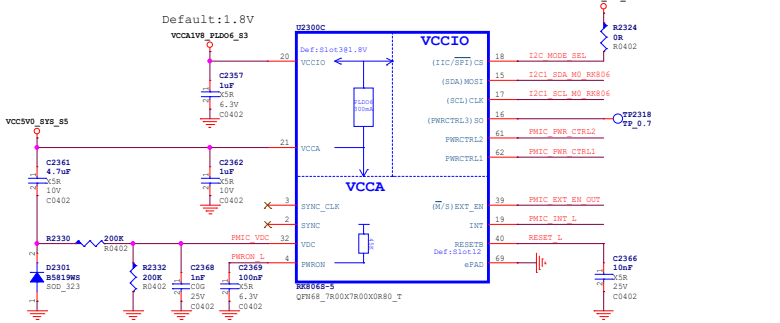
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	20.Power-DC IN		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by: Wesley Huang	Reviewed by:	Sheet:	21 of 65

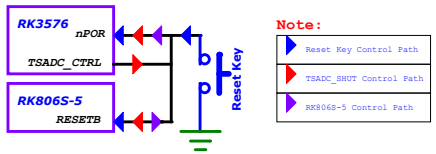
PMIC RK806S-5 BUCK



PMIC RK806S-5 Managerment

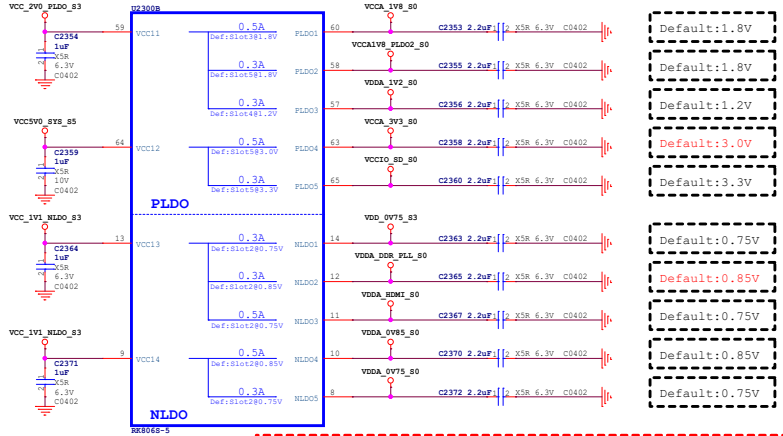


Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND



Note:
- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806S-5 Control Path

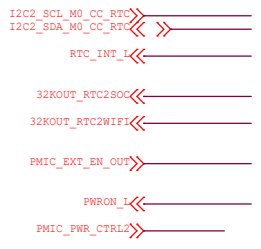
PMIC RK806S-5 LDO



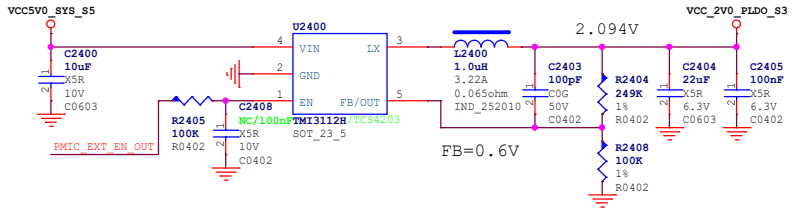
Note:
The RK806S-5 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Rockchip Confidential

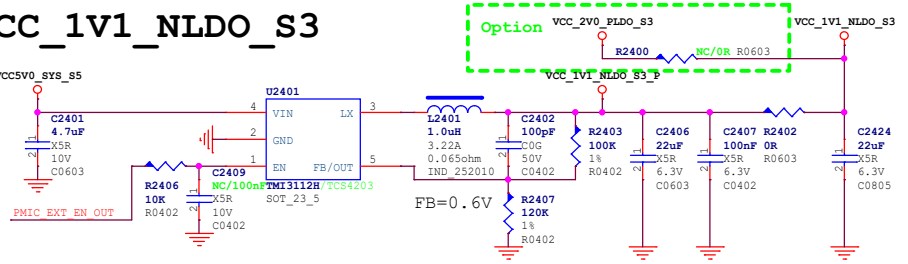
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3576_AIOT_REF_SCH
File:	23.Power-PMIC RK806S-5
Date:	Thursday, May 30, 2024
Rev:	V1.1
Designed by:	Wesley Huang
Reviewed by:	
Sheet:	22 of 65



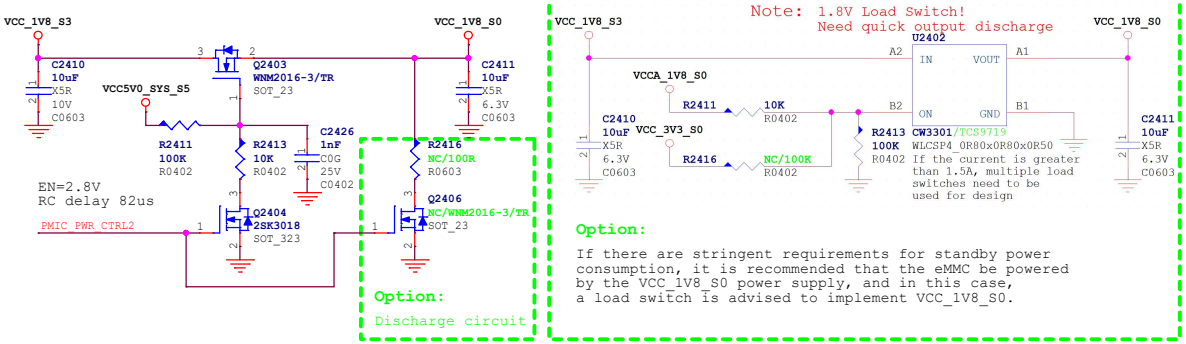
VCC_2V0_PLDO_S3



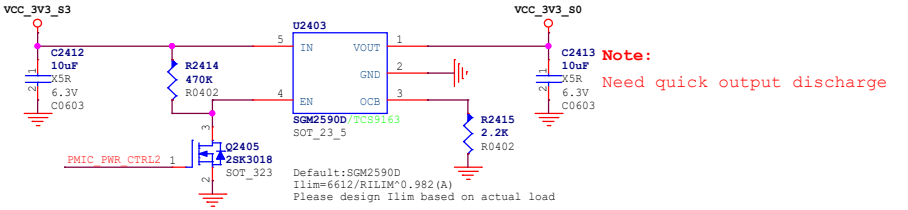
VCC_1V1_NLDO_S3



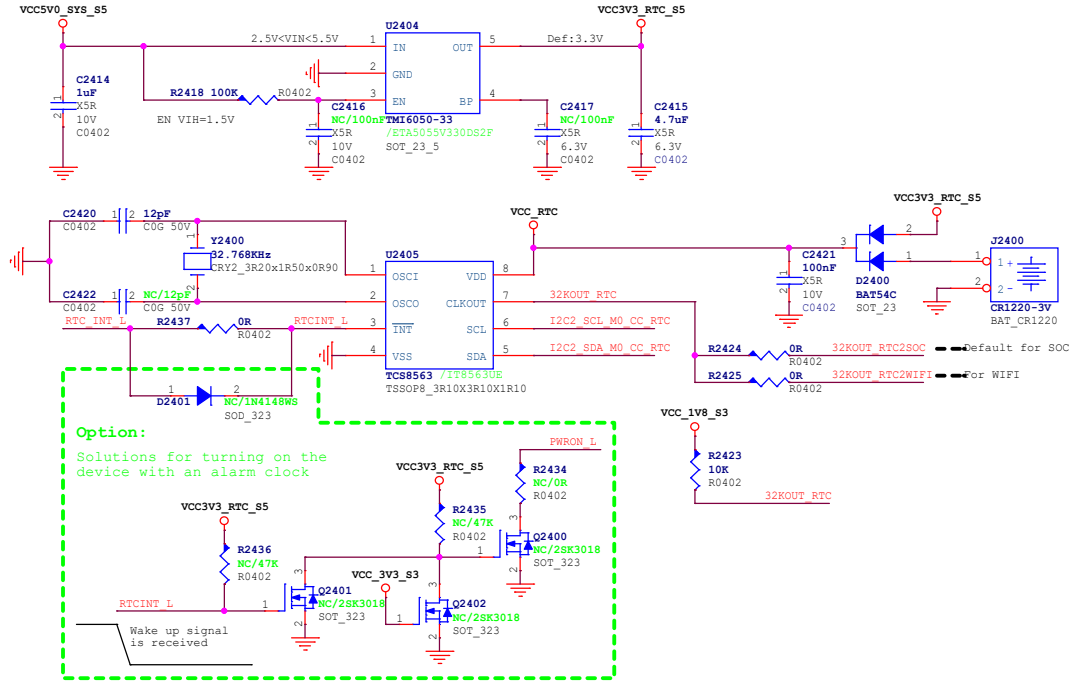
VCC_1V8_S0



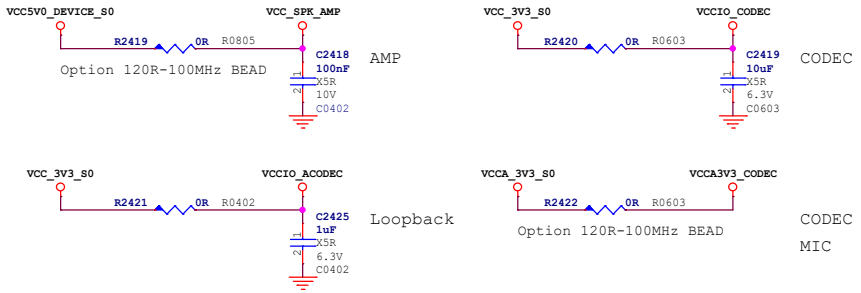
VCC_3V3_S0



RTC



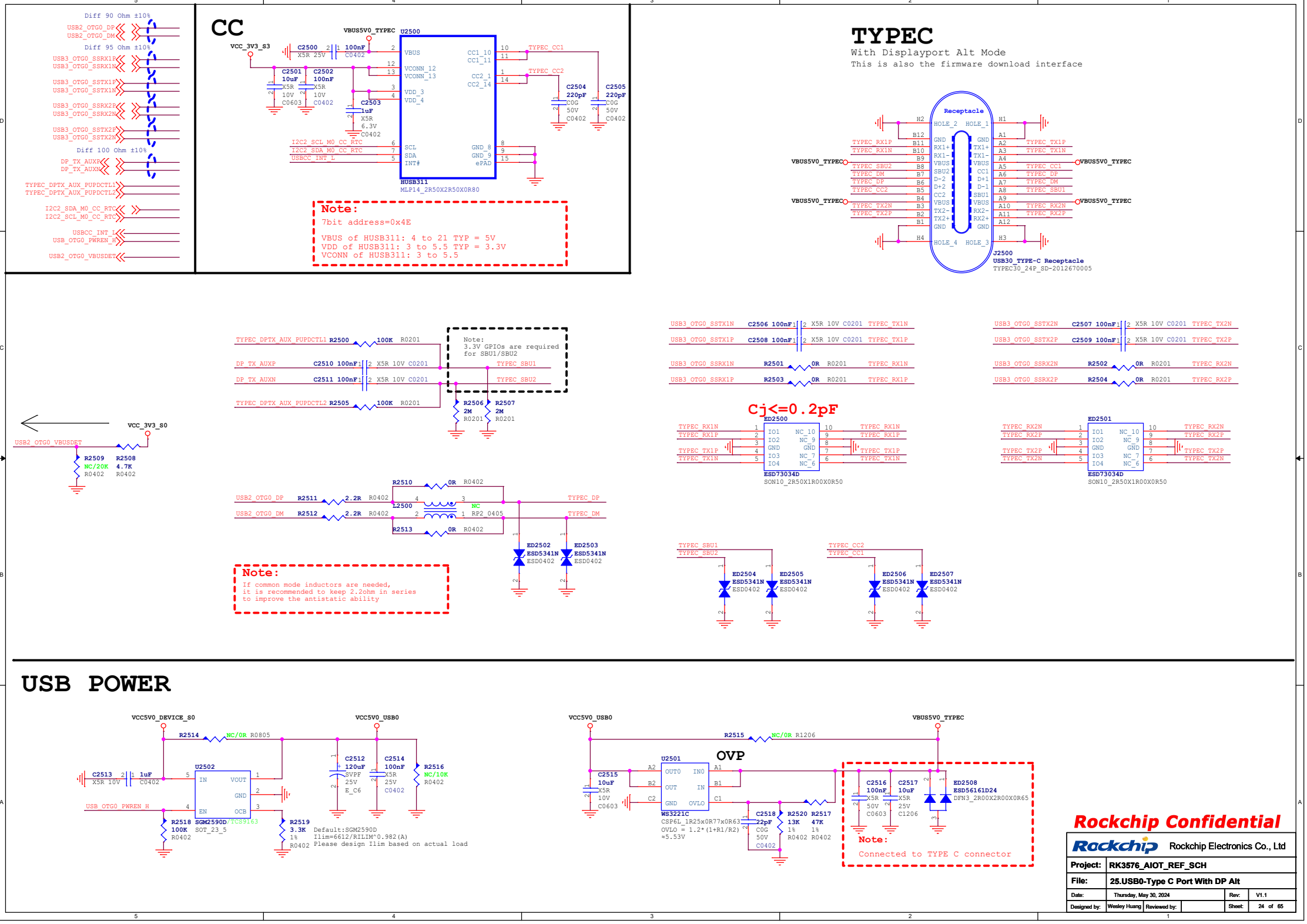
Audio Power



WIFI/BT Power

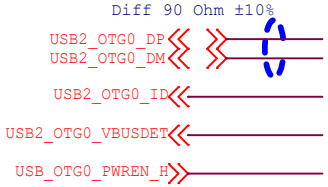
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	24.Power-Ext Discrete/RTC IC				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	23 of 65

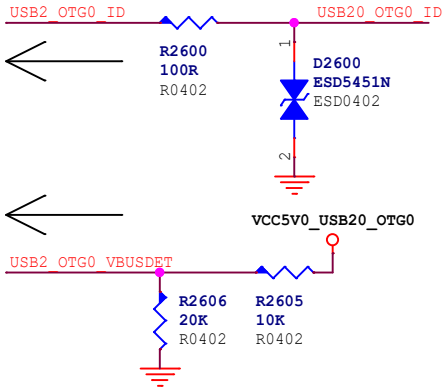

Diff 90 Ohm ±10%
USB2_OTG0_DP
USB2_OTG0_DM
Diff 95 Ohm ±10%
USB3_OTG0_SSRX1P
USB3_OTG0_SSRX1N
USB3_OTG0_SSTX1P
USB3_OTG0_SSTX1N
USB3_OTG0_SSRX2P
USB3_OTG0_SSRX2N
USB3_OTG0_SSTX2P
USB3_OTG0_SSTX2N
Diff 100 Ohm ±10%
DP_TX_AUXP
DP_TX_AUXN
TYPEC_DPTX_AUX_PUPDCTL1
TYPEC_DPTX_AUX_PUPDCTL2
I2C2_SDA_M0_CC_RTC
I2C2_SCL_M0_CC_RTC
USBCC_INT_L
USB_OTG0_PWREN_H
USB2_OTG0_VBUSDET
CC
VCC_3V3_S3
VBUS5V0_TYPEC
U2500
C2500 X5R 25V 100nF C0402
C2501 10uF X5R 10V C0603
C2502 100nF X5R 10V C0402
C2503 1uF X5R 6.3V C0402
C2504 220pF C0G 50V C0402
C2505 220pF C0G 50V C0402
VBUS
VCONN_12
VCONN_13
VDD_3
VDD_4
SCL
SDA
INT#
CC1_10
CC1_11
CC2_1
CC2_14
GND_8
GND_9
ePAD
TYPEC_CC1
TYPEC_CC2
I2C2_SCL_M0_CC_RTC
I2C2_SDA_M0_CC_RTC
USBCC_INT_L
HUSB311
MLP14_2R50X2R50X0R80
Note:
7bit address=0x4E
VBUS of HUSB311: 4 to 21 TYP = 5V
VDD of HUSB311: 3 to 5.5 TYP = 3.3V
VCONN of HUSB311: 3 to 5.5
TYPEC
With Displayport Alt Mode
This is also the firmware download interface
Receptacle
HOLE_1
HOLE_2
HOLE_3
HOLE_4
GND
TX1+
TX1-
VBUS
CC1
D+1
D-1
SBU1
RX2-
RX2+
TYPEC_TX1P
TYPEC_TX1N
TYPEC_CC1
TYPEC_DP
TYPEC_DM
TYPEC_SBU1
TYPEC_RX2N
TYPEC_RX2P
RX1+
RX1-
D-2
D+2
CC2
TX2-
TX2+
TYPEC_RX1P
TYPEC_RX1N
TYPEC_SBU2
TYPEC_DM
TYPEC_DP
TYPEC_CC2
TYPEC_TX2N
TYPEC_TX2P
J2500
USB30_TYPE-C Receptacle
TYPEC30_24P_SD-2012670005
TYPEC_DPTX_AUX_PUPDCTL1 R2500 100K R0201
DP_TX_AUXP C2510 100nF X5R 10V C0201
DP_TX_AUXN C2511 100nF X5R 10V C0201
TYPEC_DPTX_AUX_PUPDCTL2 R2505 100K R0201
Note:
3.3V GPIOs are required
for SBU1/SBU2
TYPEC_SBU1
TYPEC_SBU2
R2506 2M R0201
R2507 2M R0201
VCC_3V3_S0
USB2_OTG0_VBUSDET
R2509 NC/20K R0402
R2508 4.7K R0402
USB3_OTG0_SSTX1N C2506 100nF X5R 10V C0201 TYPEC_TX1N
USB3_OTG0_SSTX1P C2508 100nF X5R 10V C0201 TYPEC_TX1P
USB3_OTG0_SSRX1N R2501 0R R0201 TYPEC_RX1N
USB3_OTG0_SSRX1P R2503 0R R0201 TYPEC_RX1P
Cj<=0.2pF
ED2500
ESD73034D
SON10_2R50X1R00X0R50
USB3_OTG0_SSTX2N C2507 100nF X5R 10V C0201 TYPEC_TX2N
USB3_OTG0_SSTX2P C2509 100nF X5R 10V C0201 TYPEC_TX2P
USB3_OTG0_SSRX2N R2502 0R R0201 TYPEC_RX2N
USB3_OTG0_SSRX2P R2504 0R R0201 TYPEC_RX2P
ED2501
ESD73034D
SON10_2R50X1R00X0R50
USB2_OTG0_DP R2511 2.2R R0402
USB2_OTG0_DM R2512 2.2R R0402
R2510 0R R0402
R2513 0R R0402
L2500 NC RP2_0405
TYPEC_DP
TYPEC_DM
ED2502 ESD5341N ESD0402
ED2503 ESD5341N ESD0402
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
TYPEC_SBU1
TYPEC_SBU2
ED2504 ESD5341N ESD0402
ED2505 ESD5341N ESD0402
TYPEC_CC2
TYPEC_CC1
ED2506 ESD5341N ESD0402
ED2507 ESD5341N ESD0402
USB POWER
VCC5V0_DEVICE_S0
VCC5V0_USB0
R2514 NC/0R R0805
C2513 X5R 10V 1uF C0402
U2502
IN
VOUT
GND
EN
OCB
USB_OTG0_PWREN_H
R2518 100K R0402
SGM2590D/TCS9163
SOT_23_5
R2519 3.3K 1% R0402
C2512 120uF SVPF 25V E_C6
C2514 100nF X5R 25V C0402
R2516 NC/10K R0402
Default:SGM2590D
Ilim=6612/RILIM^0.982(A)
Please design Ilim based on actual load
VCC5V0_USB0
VBUS5V0_TYPEC
R2515 NC/0R R1206
OVP
U2501
OUT0
IN0
OUT
IN
GND
OVLO
WS3221C
CSP6L_1R25x0R77x0R63
OVLO = 1.2*(1+R1/R2)
≈5.53V
C2515 10uF X5R 10V C0603
C2518 22pF C0G 50V C0402
R2520 13K 1% R0402
R2517 47K 1% R0402
C2516 100nF X5R 50V C0603
C2517 10uF X5R 25V C1206
ED2508 ESD56161D24 DFN3_2R00X2R00X0R65
Note:
Connected to TYPE C connector
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK3576_AIOT_REF_SCH
File: 25.USB0-Type C Port With DP Alt
Date: Thursday, May 30, 2024
Rev: V1.1
Designed by:
Wesley Huang
Reviewed by:
Sheet: 24 of 65

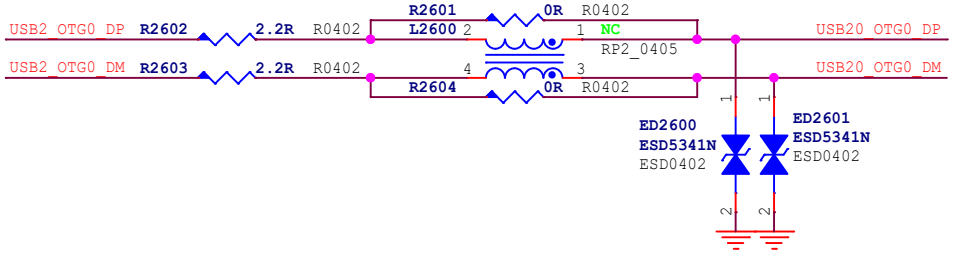
USB2.0 OTG0-Mirco Port (Together with DP 4Lanes)

Option with 25.USB0-Type C Port

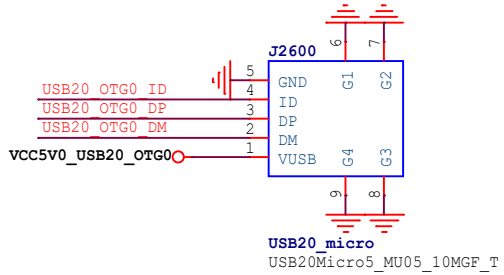


Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability

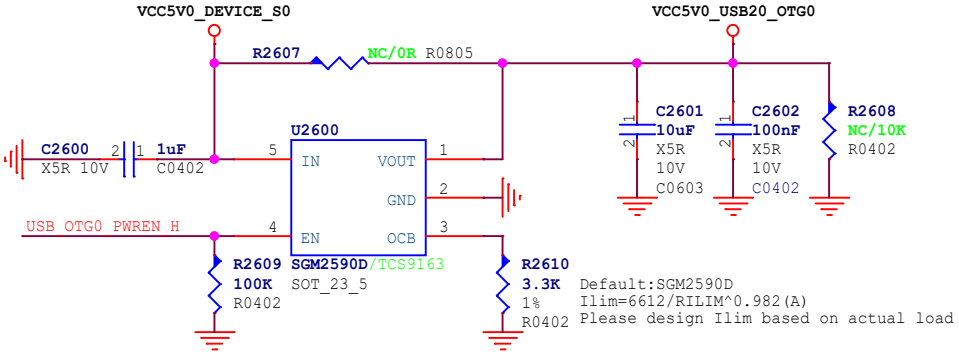




This is the firmware download interface



USB POWER

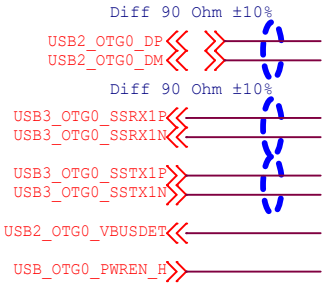


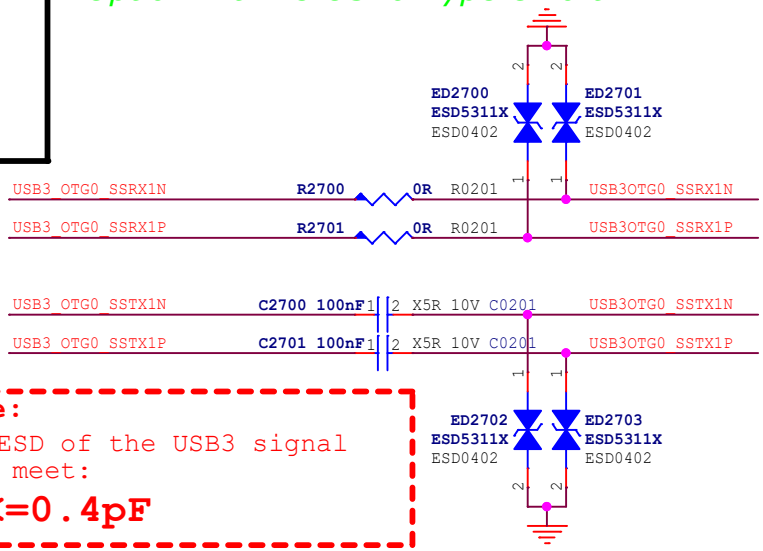
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	26.USB0-Mirco USB2.0 Port(Opt)		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by: Wesley Huang	Reviewed by:	Sheet:	25 of 65

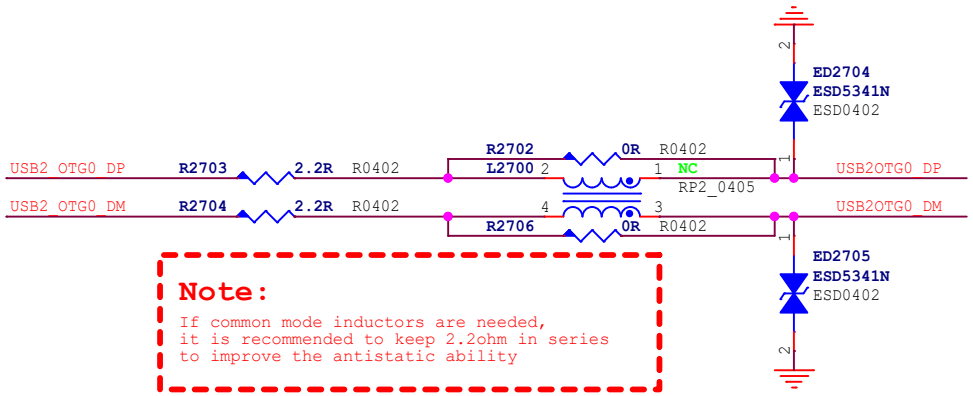
USB3 OTG0-TypeA (Together with DP 2Lanes)

Option with 25.USB0-Type C Port



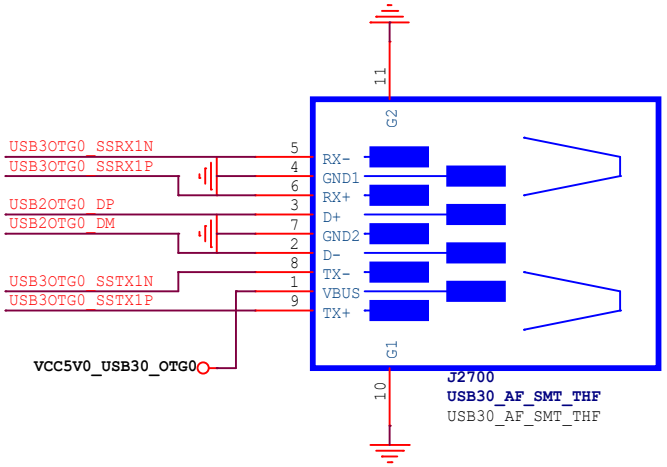


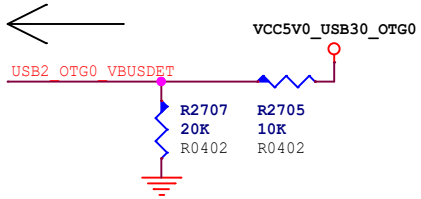
Note:
The ESD of the USB3 signal must meet:
Cj<=0.4pF



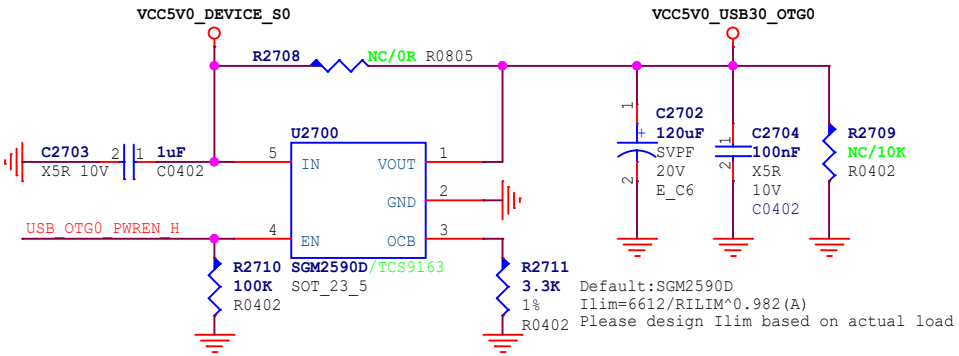
Note:
If common mode inductors are needed, it is recommended to keep 2.2ohm in series to improve the antistatic ability

This is the firmware download interface





USB POWER



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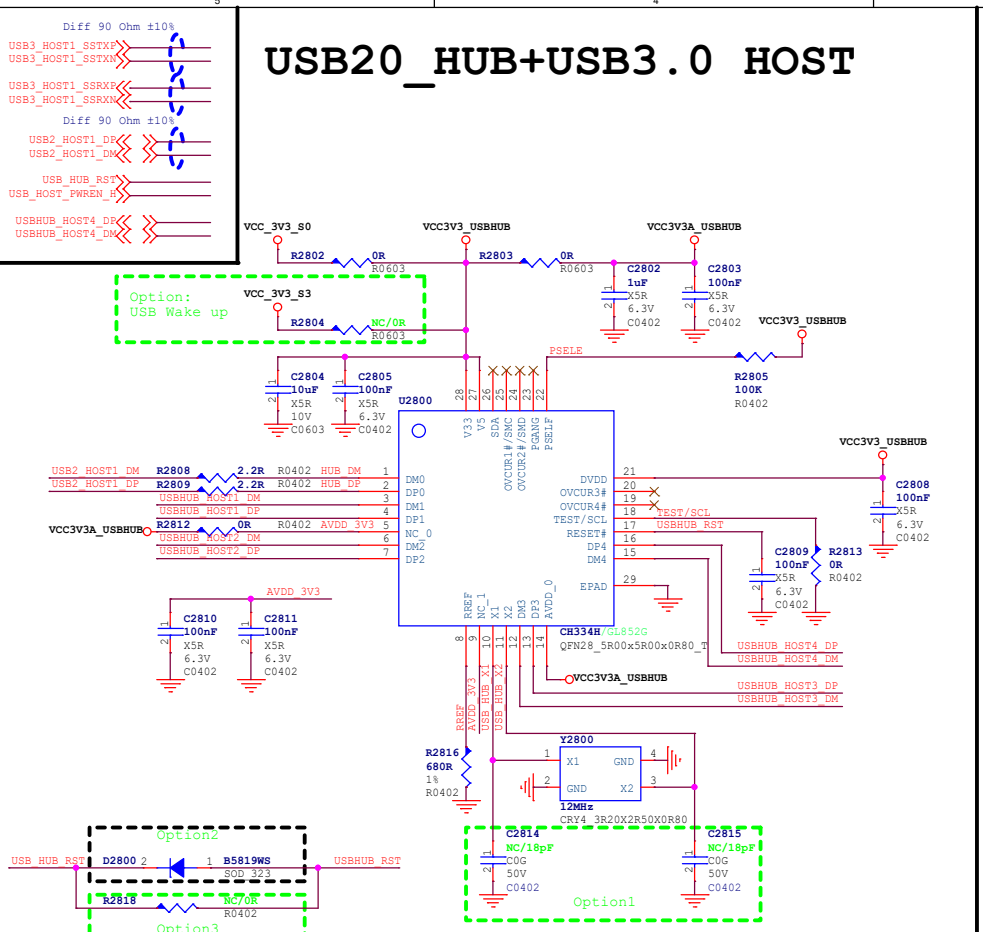
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	27.USB0-TypeA USB3.0 Port(Opt)		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:	Sheet: 26 of 65

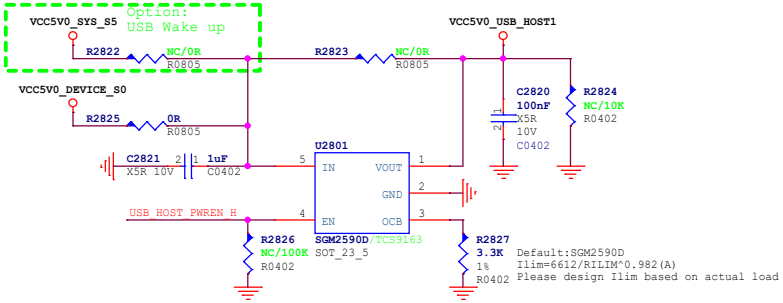
USB20_HUB+USB3.0 HOST



Note:
Yes: option circuit be mounted
No: option circuit not be mounted

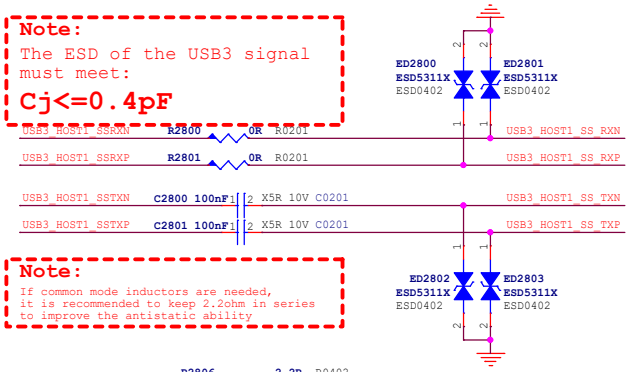
OPTION	Option1	Option2	Option3
CH334H	NO	Yes	NO
GL852G	Yes	NO	Yes

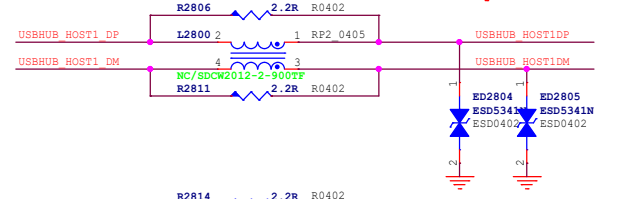
USB POWER

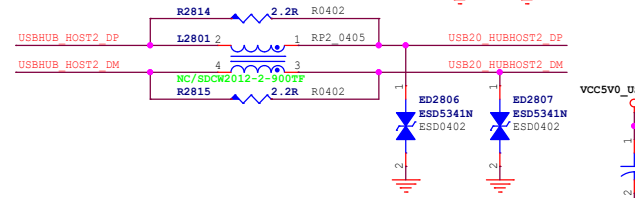


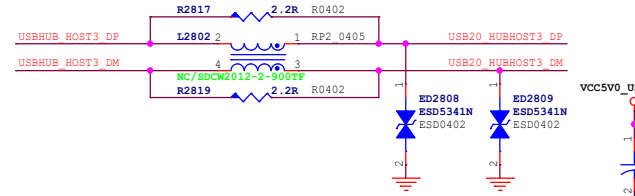
Note:
The ESD of the USB3 signal must meet:
Cj<=0.4pF

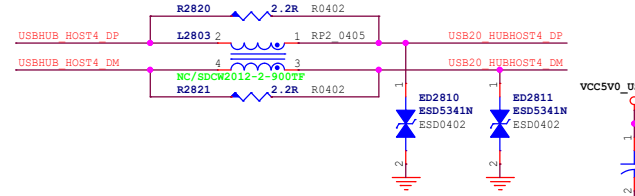
Note:
If common mode inductors are needed, it is recommended to keep 2.2ohm in series to improve the antistatic ability



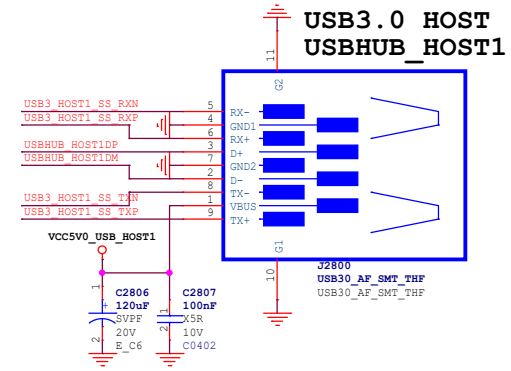




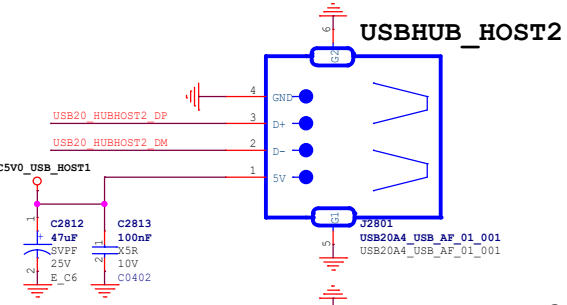




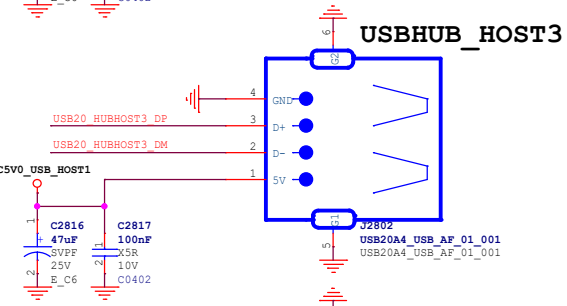
USB3.0 HOST
USBHUB_HOST1



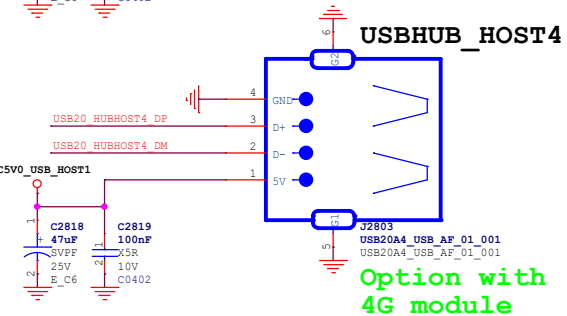
USBHUB_HOST2



USBHUB_HOST3



USBHUB_HOST4

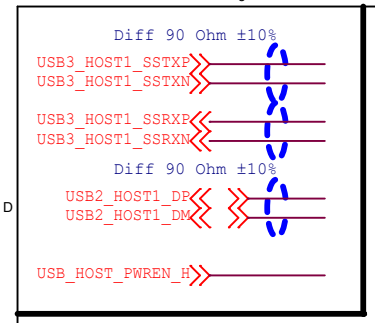


Option with 4G module

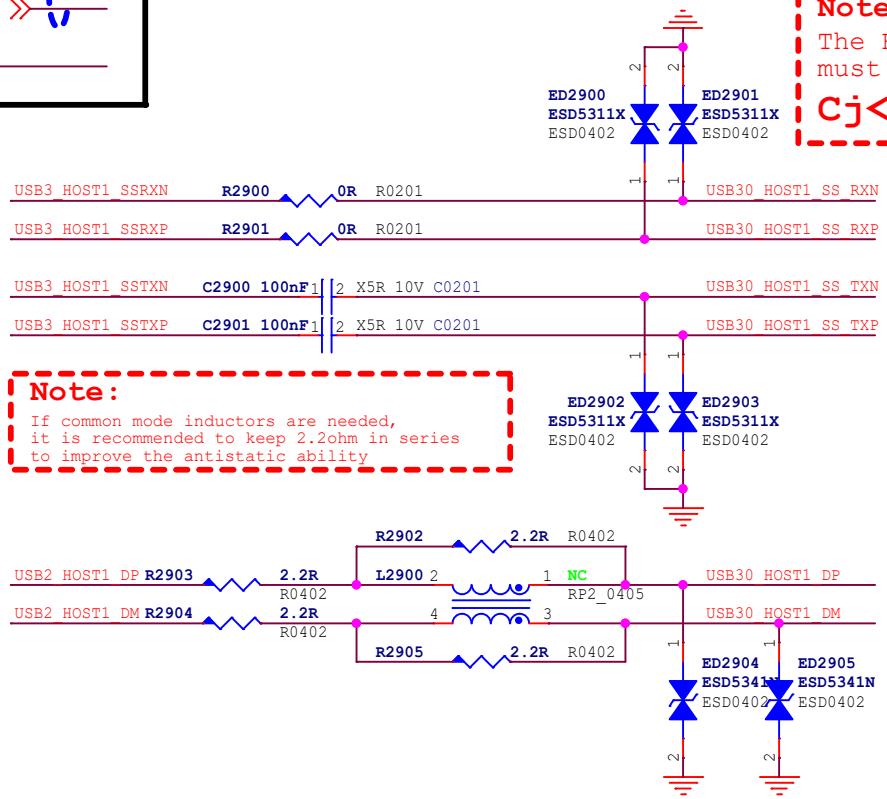
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	28.USB1-USB20_HUB+USB3.0 HOST		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang / Reviewed by:	Sheet:	27 of 65

USB3 HOST1-TypeA

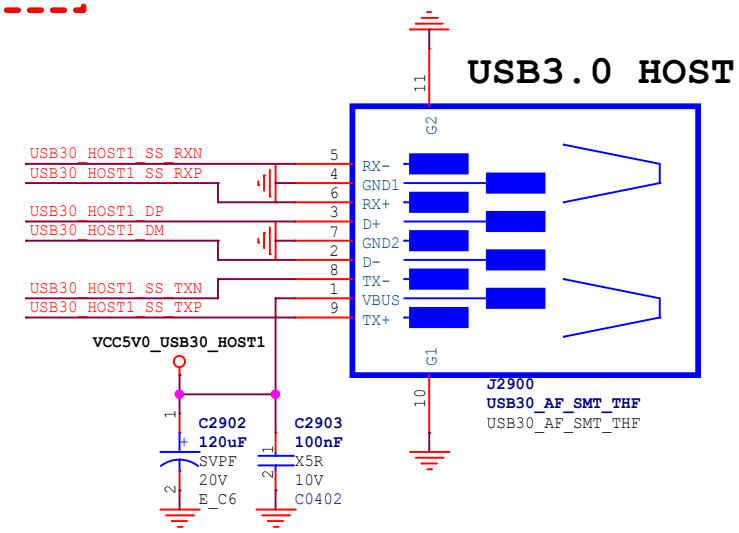
Option with 28.USB1-USB20_HUB+USB3.0 HOST



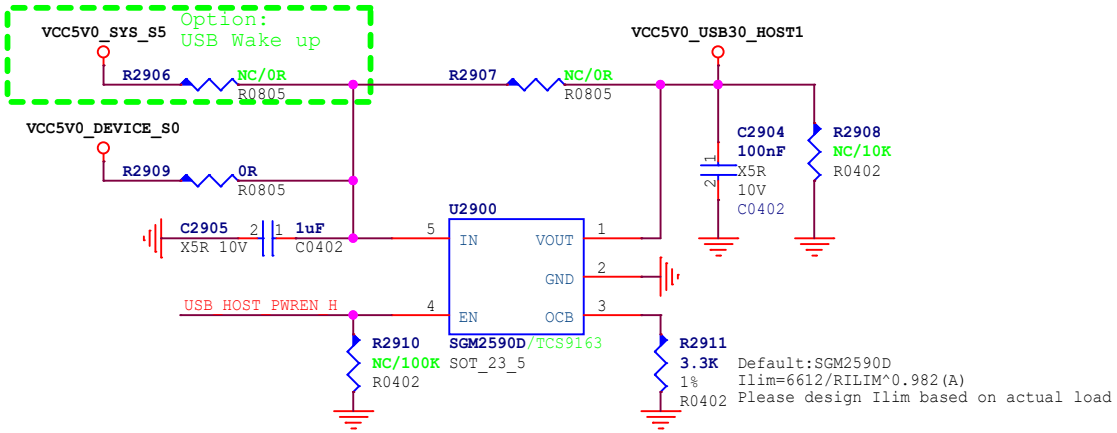
Note:
The ESD of the USB3 signal must meet:
Cj<=0.4pF



Note:
If common mode inductors are needed, it is recommended to keep 2.2ohm in series to improve the antistatic ability



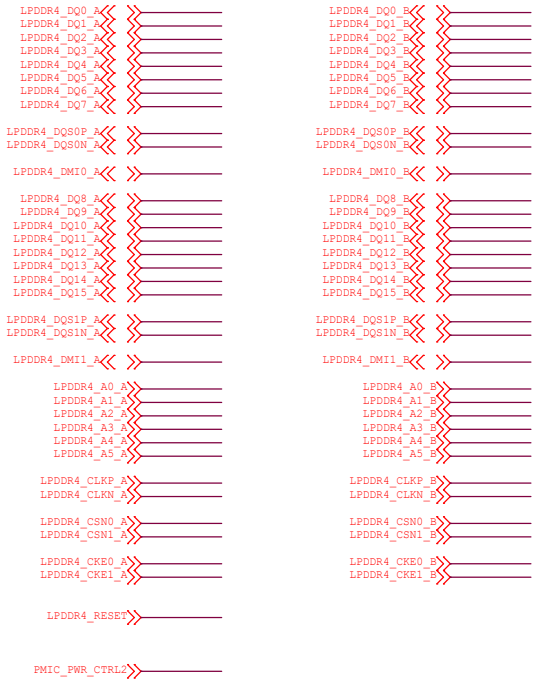
USB POWER

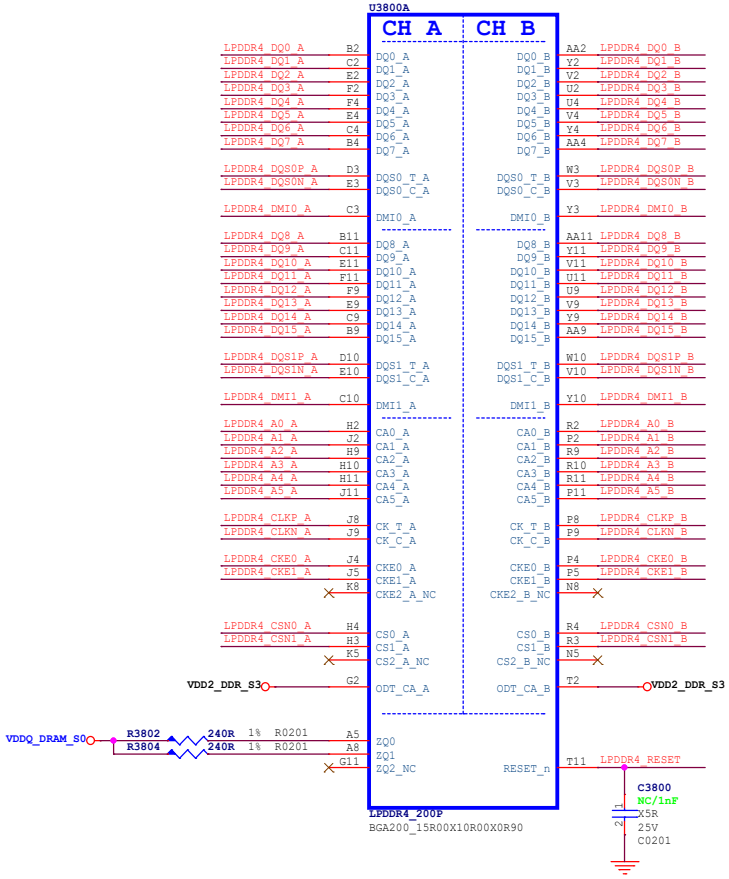


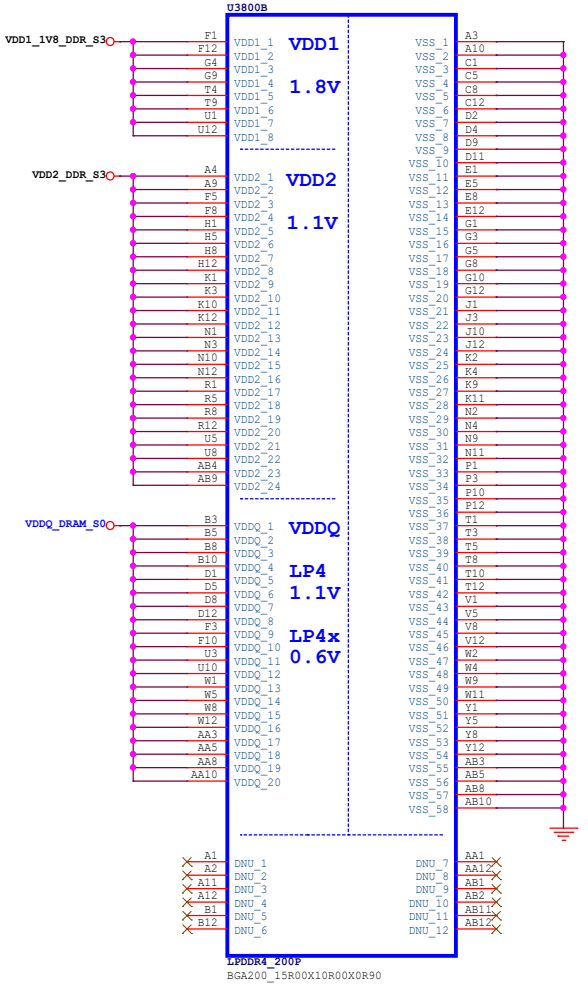
Rockchip Confidential

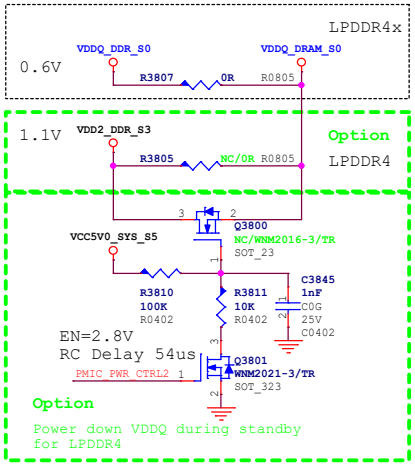
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	29.USB1-TYPEA USB3.0 Port(Opt)		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang / Reviewed by:	Sheet:	28 of 65

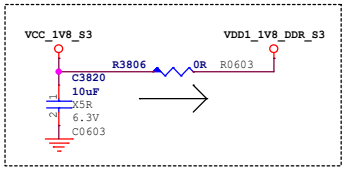
LPDDR4/4X

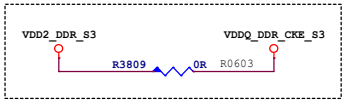








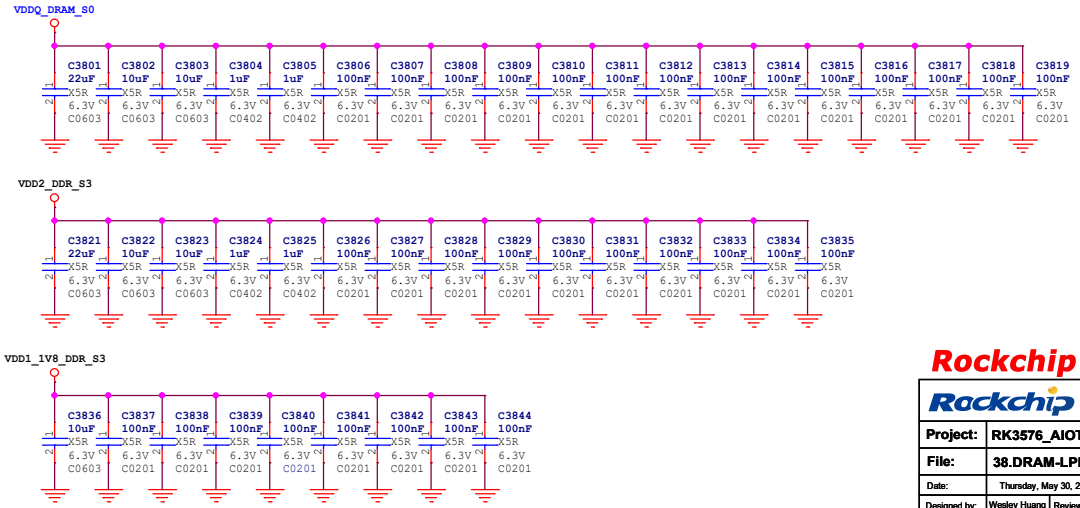




Note:

Sequence:VDD1-VDD2-VDDQ

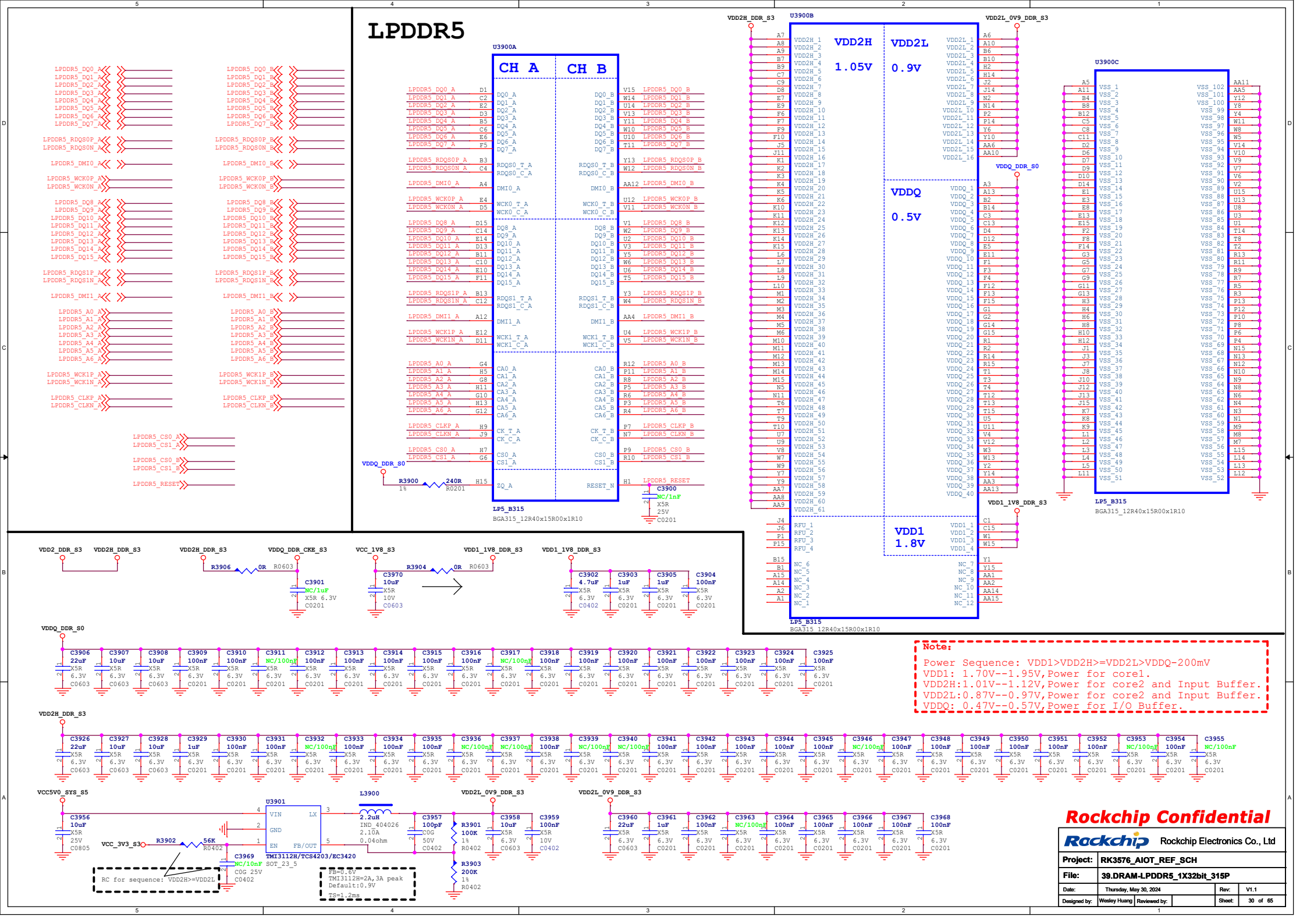
	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	38.DRAM-LPDDR4X_1X32bit_200P		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang / Reviewed by:	Sheet:	29 of 65

LPDDR5



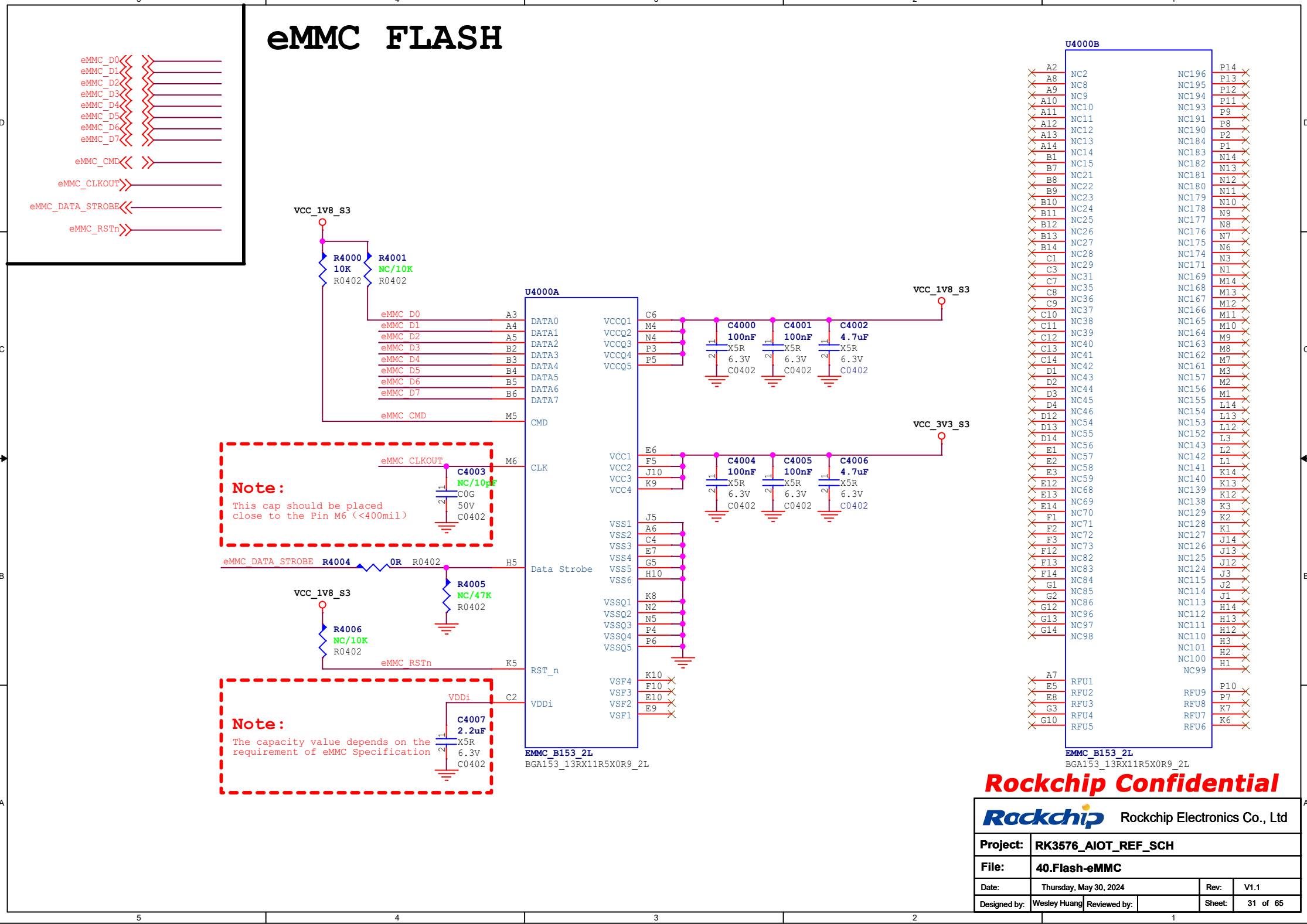
Note:

Power Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV
VDD1: 1.70V--1.95V,Power for core1.
VDD2H:1.01V--1.12V,Power for core2 and Input Buffer.
VDD2L:0.87V--0.97V,Power for core2 and Input Buffer.
VDDQ: 0.47V--0.57V,Power for I/O Buffer.

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	39.DRAM-LPDDR5_1X32bit_315P		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:	Sheet: 30 of 65

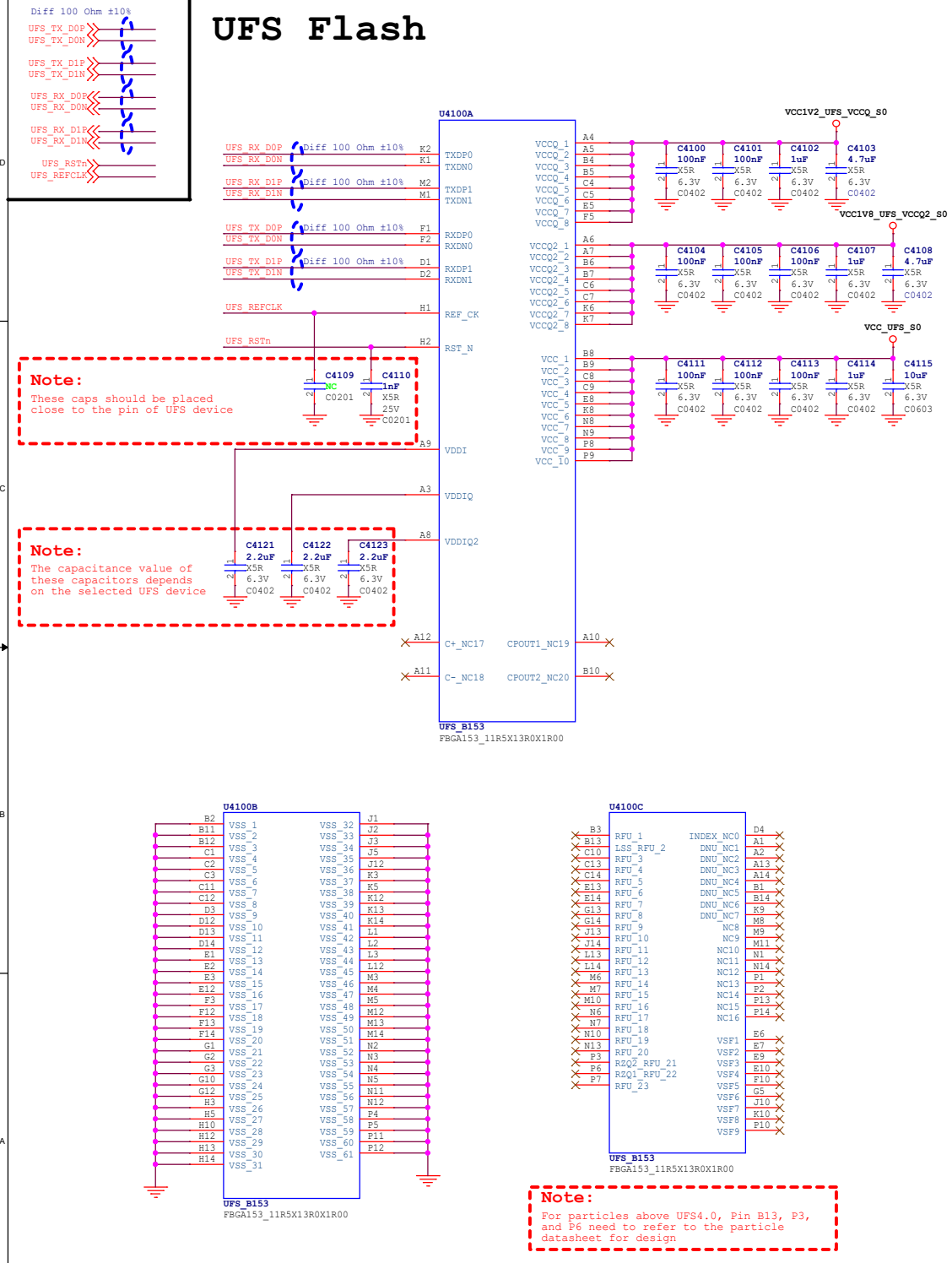
eMMC FLASH



Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	40.Flash-eMMC		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by: Wesley Huang	Reviewed by:	Sheet:	31 of 65

UFS Flash



Note:
These caps should be placed close to the pin of UFS device

Note:
The capacitance value of these capacitors depends on the selected UFS device

Note:
For particles above UFS4.0, Pin B13, P3, and P6 need to refer to the particle datasheet for design

UFS POWER

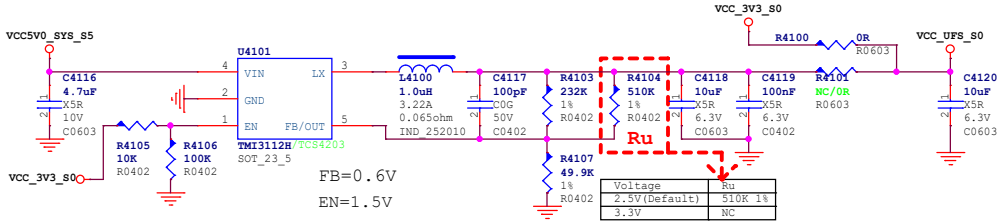
Supported Particles	VCCQ	VCCQ2	VCC
UFS2.0	1.2V	1.8V	3.3V
UFS2.1	No Connect	1.8V	3.3V
UFS2.2	No Connect	1.8V	3.3V
UFS3.0	1.2V	No Connect	2.5V/3.3V
UFS3.1	1.2V	No Connect	2.5V/3.3V

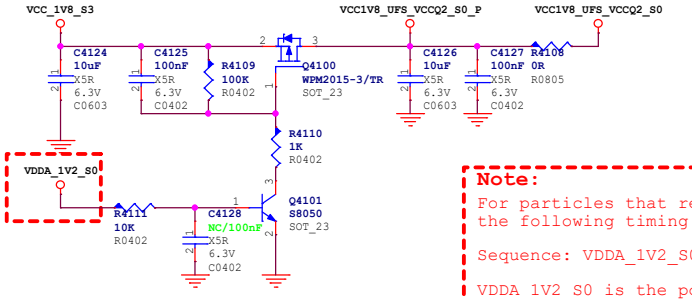
Default UFS device: UFS2.2

Do not support UFS4.0 Device!

Sequence:VCCQ2->VCCQ, VCC is independent

Note:
The power ball that is not used at the particle must be kept floating.

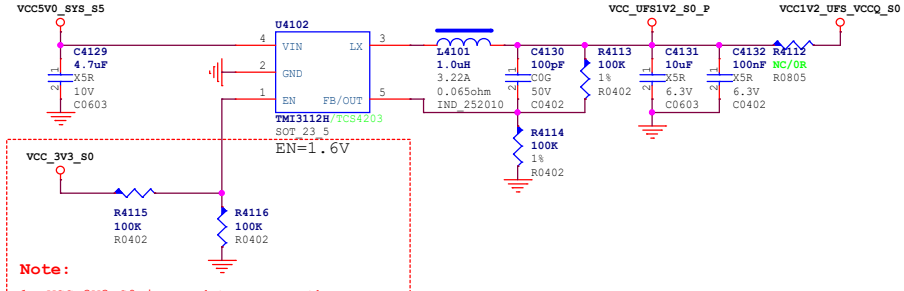




Note:
For particles that require VCCQ and VCCQ2, the following timing needs to be met:

Sequence: VDDA_1V2_S0->VCCQ2->VCCQ

VDDA_1V2_S0 is the power of REF_CK & RST_N in RK SOC, which needs to be powered on before UFS particles

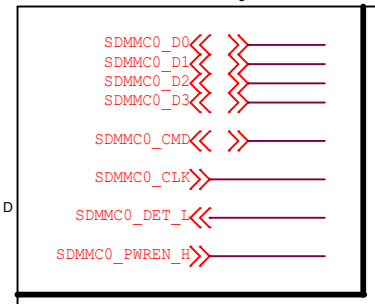


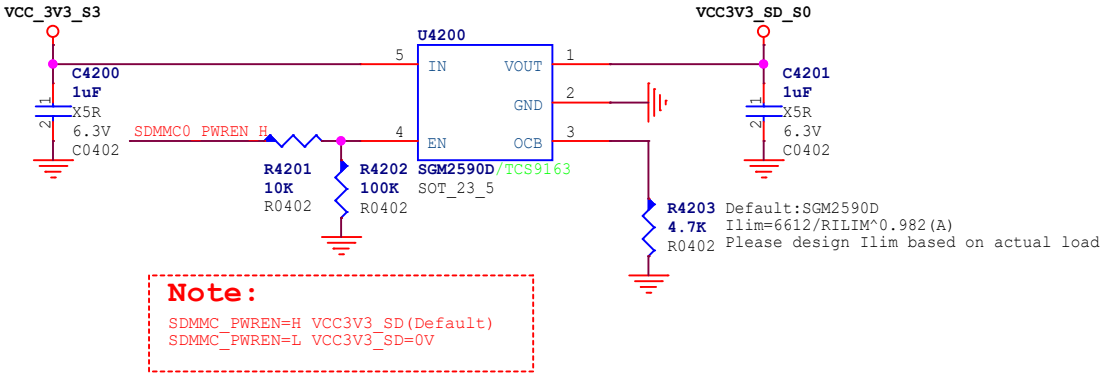
Note:
1. VCC_3V3_S0 is used to ensure the power supply timing of the UFS chip;
2. The resistance voltage division value needs to be designed based on the EN pin threshold of DCDC.

Rockchip Confidential

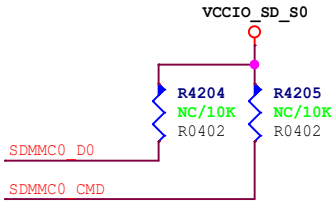
Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	41.Flash-UFS		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:	Sheet: 32 of 65

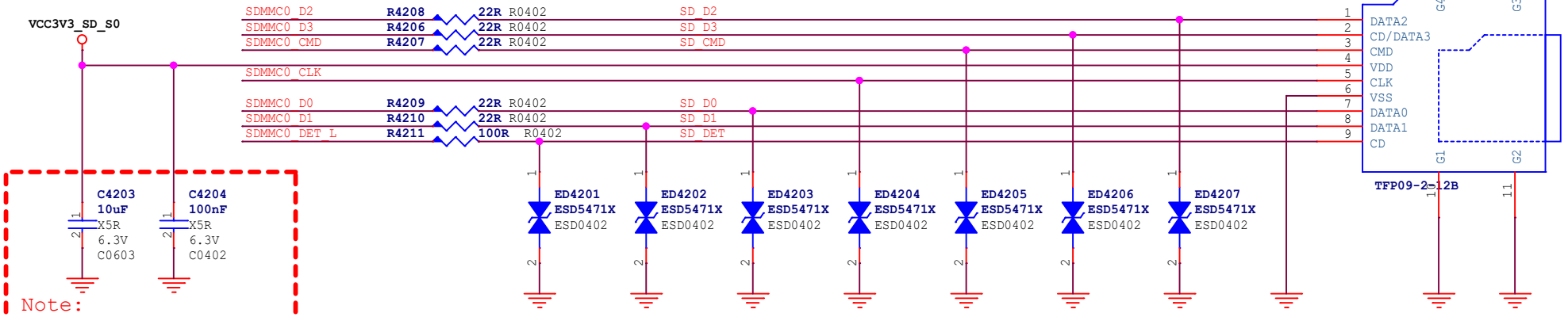
TF CARD





Note:
SDMMC_PWREN=H VCC3V3_SD(Default)
SDMMC_PWREN=L VCC3V3_SD=0V





Note:
Close to MicroSD Card

MicroSD Card

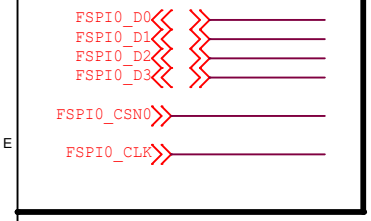
Note:
SDMMC_DET_L:
SDCARD PLUG: Pull-down to GND
SDCARD UNPLUG: Pull-up to PMUIO0_VCC1V8.

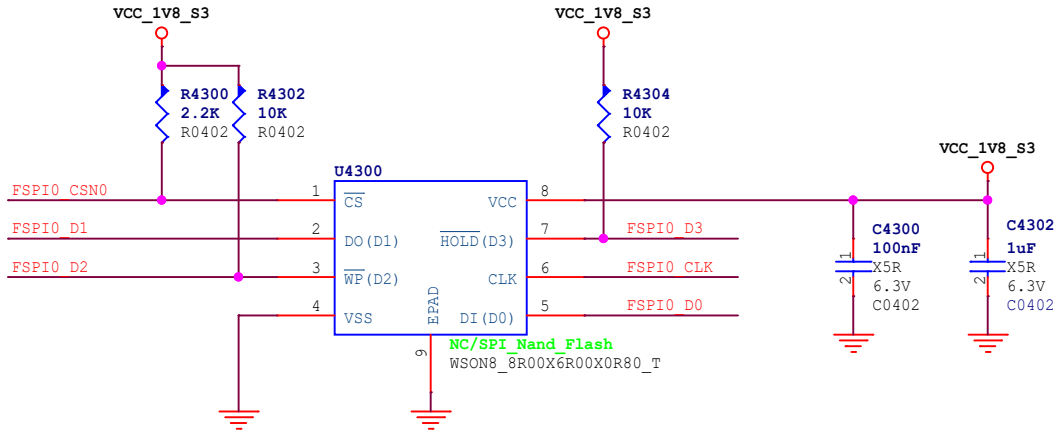
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	42.Flash-MicroSD Card		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by: Wesley Huang	Reviewed by:	Sheet:	33 of 65

FSPI0 Flash

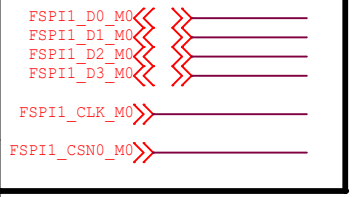
Option with 40.Flash-eMMC

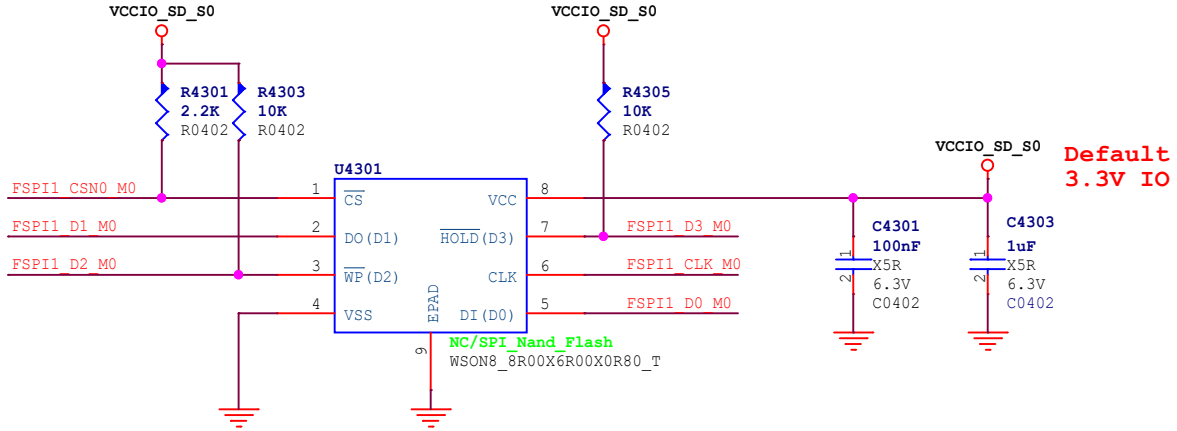




FSPI1 Flash

Option with 42.Flash-MicroSD Card

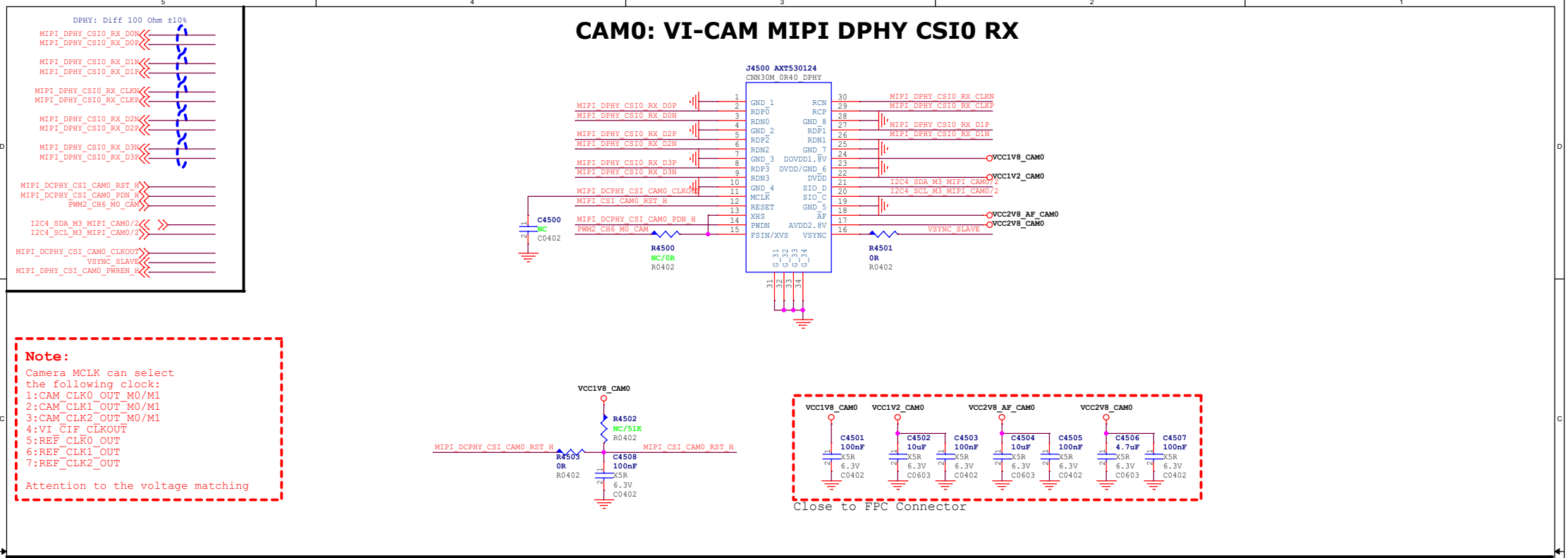




Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	43.Flash-SPI Flash(opt)		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by: Wesley Huang	Reviewed by:	Sheet:	34 of 65

CAM0: VI-CAM MIPI DPHY CSI0 RX



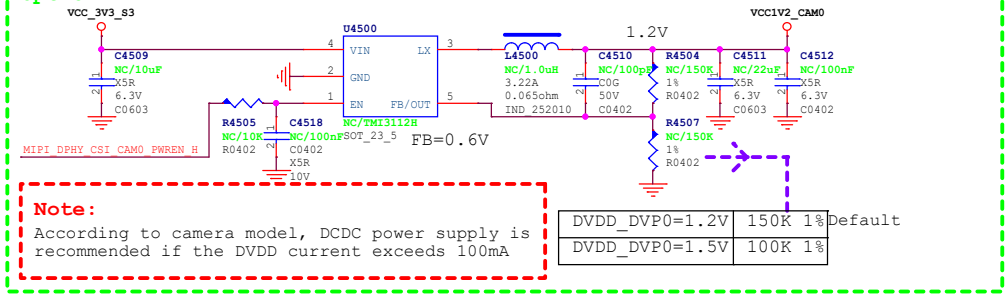
Note:
Camera MCLK can select the following clock:
1:CAM_CLK0_OUT_M0/M1
2:CAM_CLK1_OUT_M0/M1
3:CAM_CLK2_OUT_M0/M1
4:VI_CIF_CLKOUT
5:REF_CLK0_OUT
6:REF_CLK1_OUT
7:REF_CLK2_OUT

Attention to the voltage matching

Close to FPC Connector

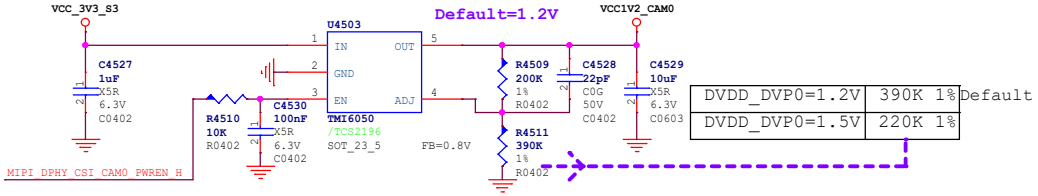
CAM0_POWER

Option



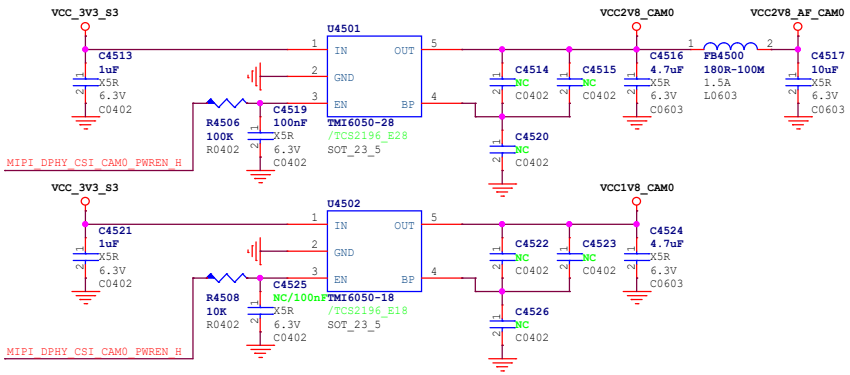
DVDD_DVP0=1.2V	150K 1%	Default
DVDD_DVP0=1.5V	100K 1%	

Note:
According to camera model, DCDC power supply is recommended if the DVDD current exceeds 100mA



DVDD_DVP0=1.2V	390K 1%	Default
DVDD_DVP0=1.5V	220K 1%	

Note:
When the binocular camera is used, If separate control is required, separate power supply is recommended

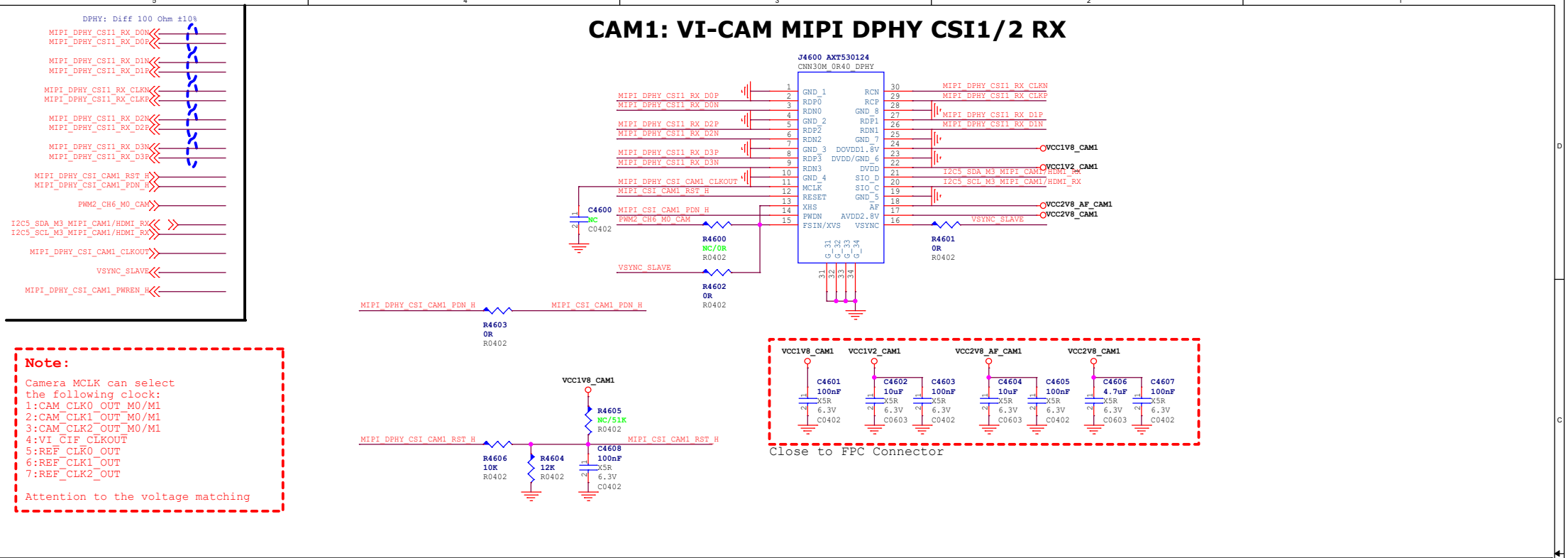


Note:
Adjust the power on sequence according to the camera model
eg:GC8034
Power on Sequence
1.8V-->1.2V-->2.8V--->MCLK-->PWDN--->RST

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	45.VI-CAM MIPI DPHY CSI0 RX				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	35 of 65

CAM1: VI-CAM MIPI DPHY CSI1/2 RX

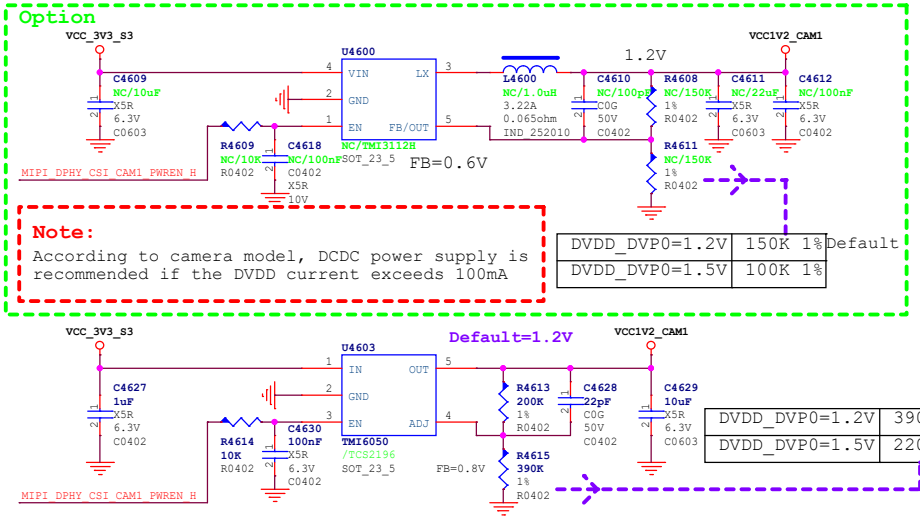


Note:

Camera MCLK can select the following clock:
1:CAM_CLK0_OUT_M0/M1
2:CAM_CLK1_OUT_M0/M1
3:CAM_CLK2_OUT_M0/M1
4:VI_CIF_CLKOUT
5:REF_CLK0_OUT
6:REF_CLK1_OUT
7:REF_CLK2_OUT

Attention to the voltage matching

CAM1_POWER

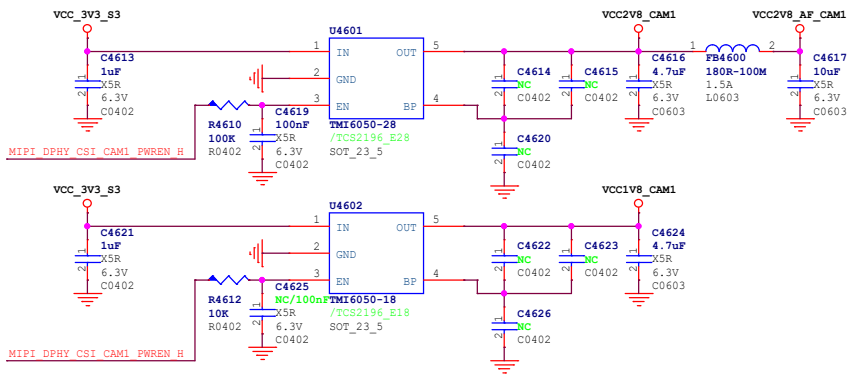


Note:

According to camera model, DCDC power supply is recommended if the DVDD current exceeds 100mA

Note:

When the binocular camera is used, If separate control is required, separate power supply is recommended



Note:

Adjust the power on sequence according to the camera model

eg:GC8034

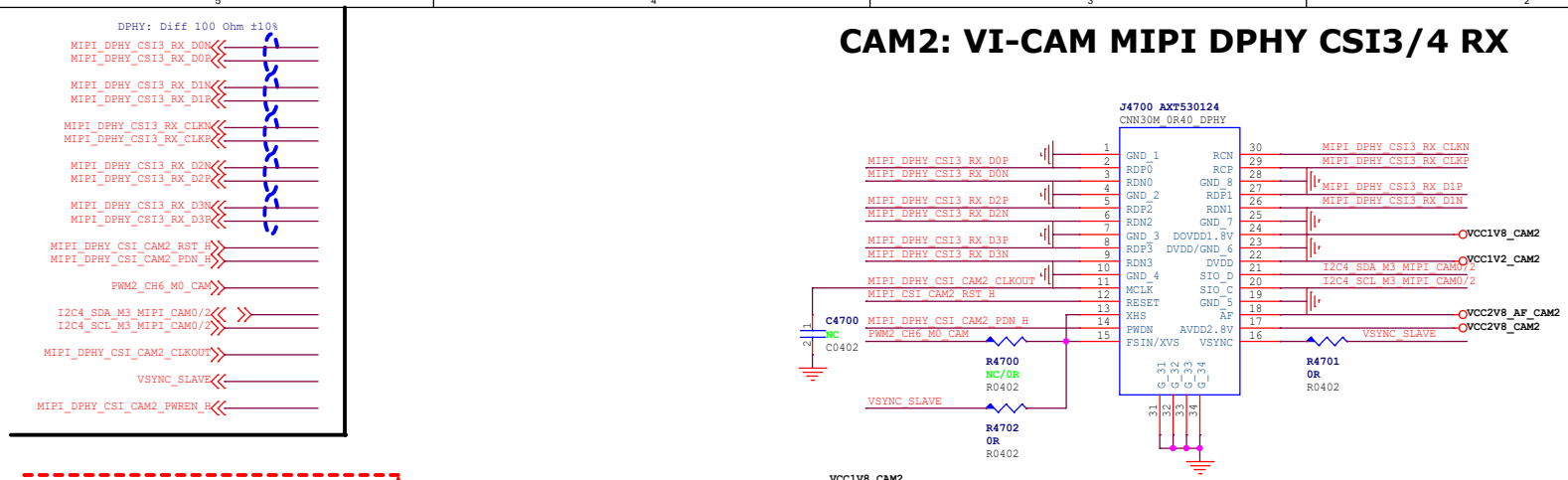
Power on Sequence

1.8V-->1.2V-->2.8V--->MCLK-->PWDN--->RST

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	46.VI-CAM MIPI DPHY CSI1/2 RX				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	36 of 65

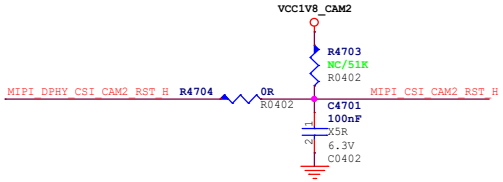
CAM2: VI-CAM MIPI DPHY CSI3/4 RX

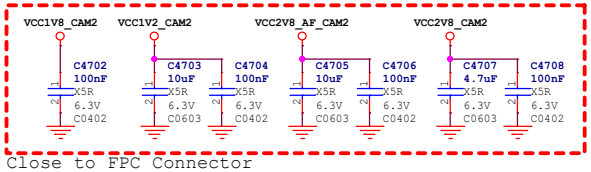


Note:

Camera MCLK can select the following clock:
1:CAM_CLK0_OUT_M0/M1
2:CAM_CLK1_OUT_M0/M1
3:CAM_CLK2_OUT_M0/M1
4:VI_CIF_CLKOUT
5:REF_CLK0_OUT
6:REF_CLK1_OUT
7:REF_CLK2_OUT

Attention to the voltage matching

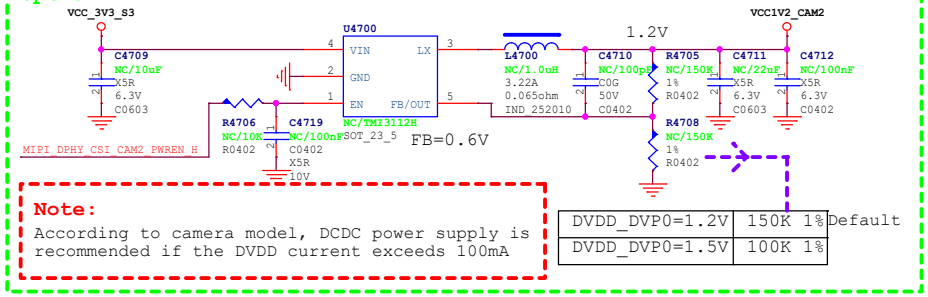




Close to FPC Connector

CAM2_POWER

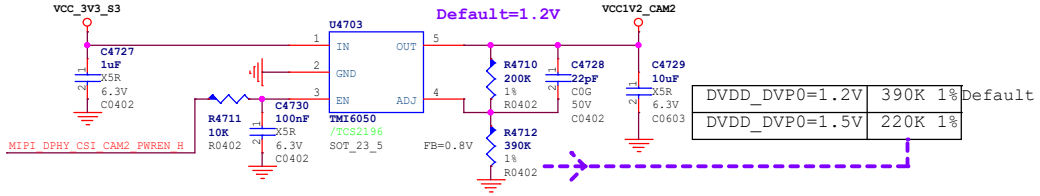
Option



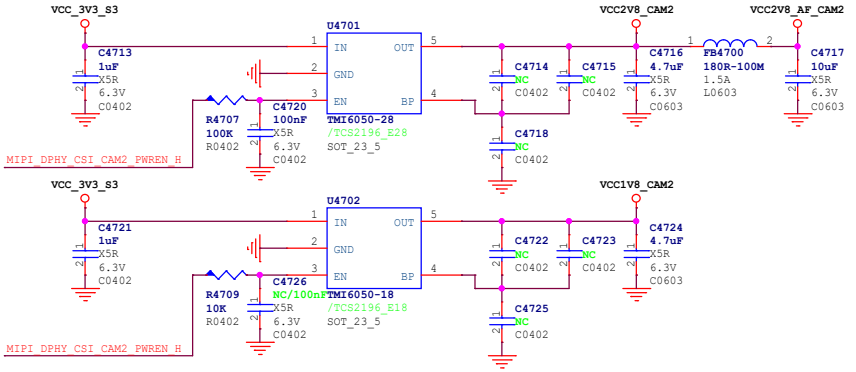
Note:

According to camera model, DCDC power supply is recommended if the DVDD current exceeds 100mA

DVDD_DVP0=1.2V	150K 1%	Default
DVDD_DVP0=1.5V	100K 1%	



DVDD_DVP0=1.2V	390K 1%	Default
DVDD_DVP0=1.5V	220K 1%	



Note:

When the binocular camera is used, If separate control is required, separate power supply is recommended

Note:

Adjust the power on sequence according to the camera model

eg:GC8034

Power on Sequence

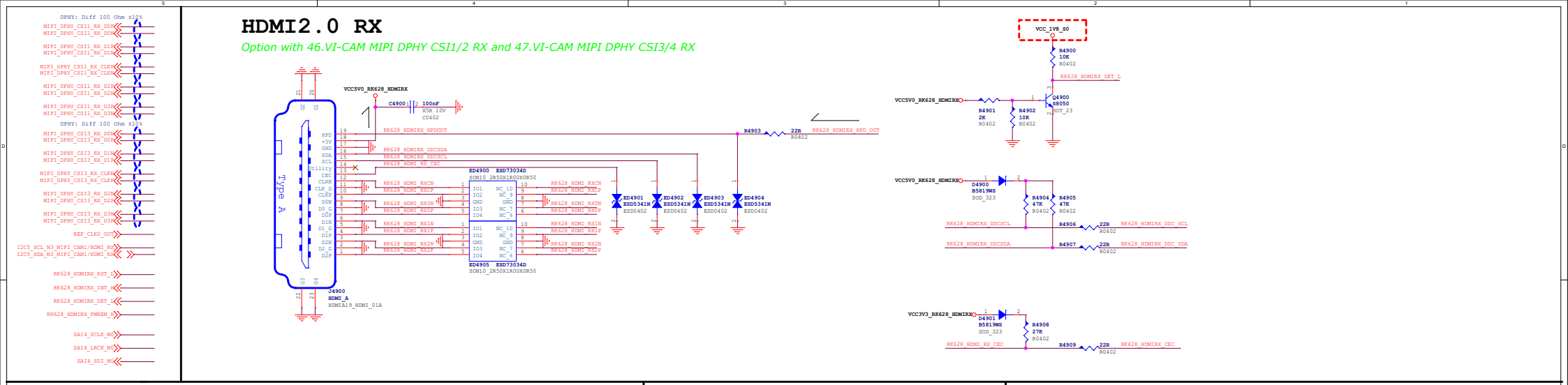
1.8V-->1.2V-->2.8V--->MCLK-->PWDN--->RST

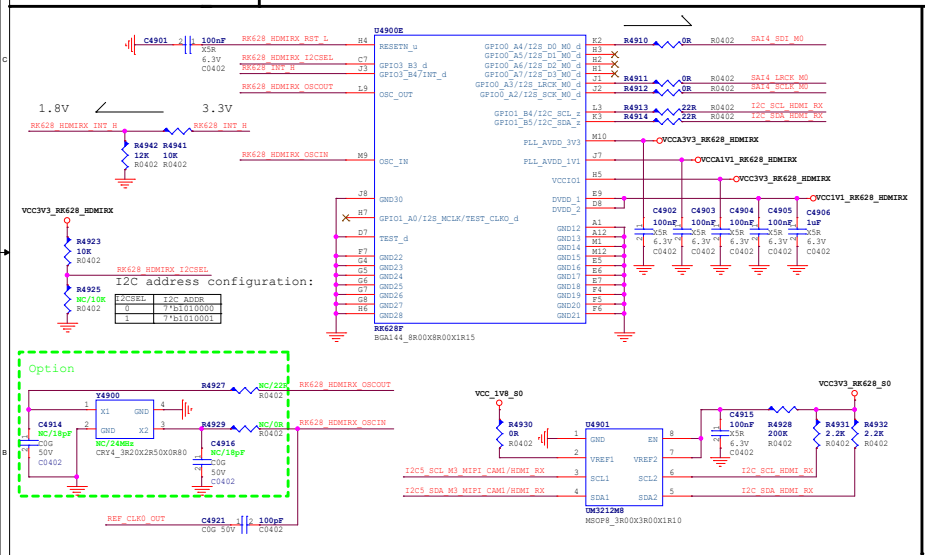
Rockchip Confidential

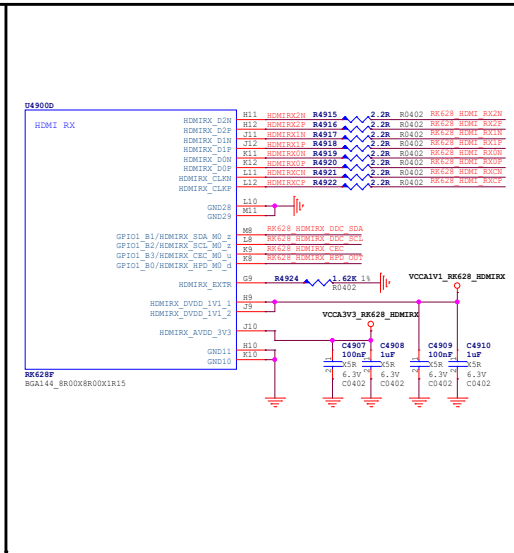
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	47.VI-CAM MIPI DPHY CSI3/4 RX				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	37 of 65

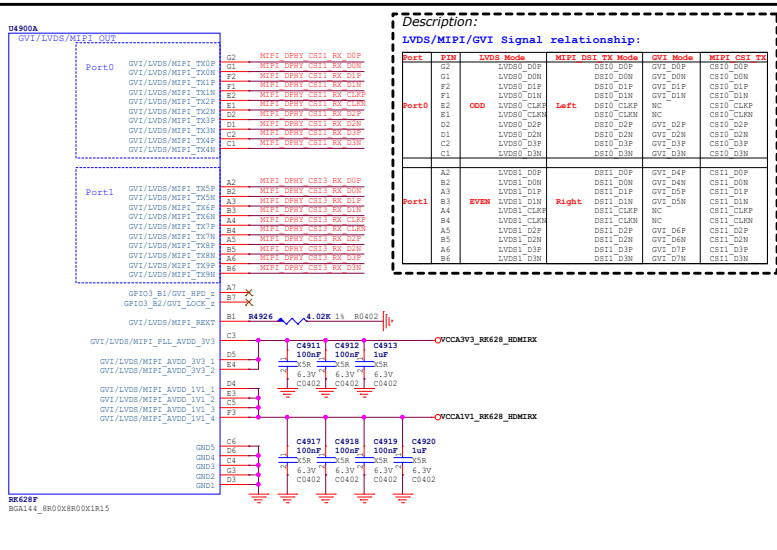
HDMI2.0 RX

Option with 46.VI-CAM MIPI DPHY CSI1/2 RX and 47.VI-CAM MIPI DPHY CSI3/4 RX









Description:

LVDS/MIPI/GVI Signal relationship:

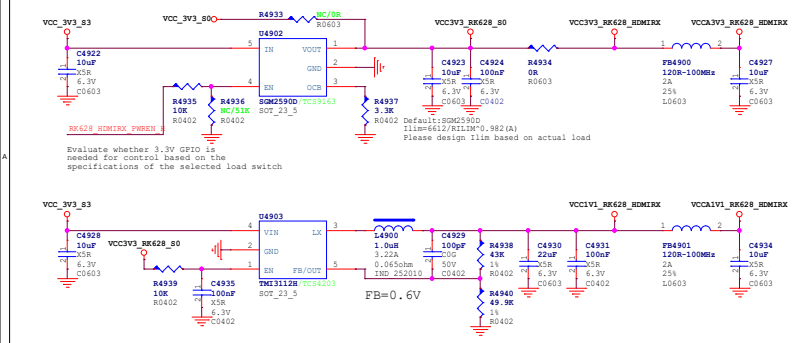
Port	PIN	LVDS Mode	MIPI_DSI TX Mode	GVI Mode	MIPI_CSI TX
Port0	G2	LVDS0_D0P	DSI0_D0P	GVI_D0P	CSI0_D0P
	G1	LVDS0_D0N	DSI0_D0N	GVI_D0N	CSI0_D0N
	F2	LVDS0_D1P	DSI0_D1P	GVI_D1P	CSI0_D1P
	F1	LVDS0_D1N	DSI0_D1N	GVI_D1N	CSI0_D1N
	E2	LVDS0_CLKP	DSI0_CLKP	NC	CSI0_CLKP
	E1	LVDS0_CLKN	DSI0_CLKN	NC	CSI0_CLKN
	D2	LVDS0_D2P	DSI0_D2P	GVI_D2P	CSI0_D2P
	D1	LVDS0_D2N	DSI0_D2N	GVI_D2N	CSI0_D2N
	C2	LVDS0_D3P	DSI0_D3P	GVI_D3P	CSI0_D3P
	C1	LVDS0_D3N	DSI0_D3N	GVI_D3N	CSI0_D3N
Port1	A2	LVDS1_D0P	DSI1_D0P	GVI_D4P	CSI1_D0P
	B2	LVDS1_D0N	DSI1_D0N	GVI_D4N	CSI1_D0N
	A3	LVDS1_D1P	DSI1_D1P	GVI_D5P	CSI1_D1P
	B3	LVDS1_D1N	DSI1_D1N	GVI_D5N	CSI1_D1N
	A4	LVDS1_CLKP	DSI1_CLKP	NC	CSI1_CLKP
	B4	LVDS1_CLKN	DSI1_CLKN	NC	CSI1_CLKN
	A5	LVDS1_D2P	DSI1_D2P	GVI_D6P	CSI1_D2P
	B5	LVDS1_D2N	DSI1_D2N	GVI_D6N	CSI1_D2N
	A6	LVDS1_D3P	DSI1_D3P	GVI_D7P	CSI1_D3P
	B6	LVDS1_D3N	DSI1_D3N	GVI_D7N	CSI1_D3N

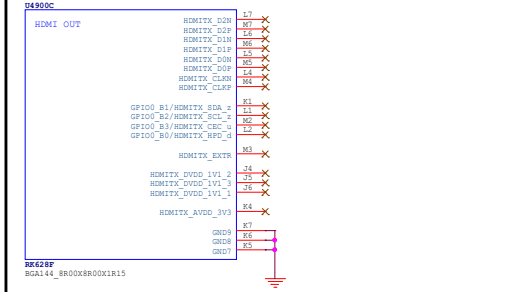
Port0: ODD, Left — Port1: EVEN, Right

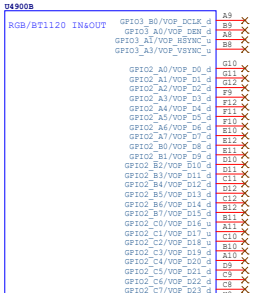
RK628 Power

Power-on Sequence:

3V3 --> 1V1



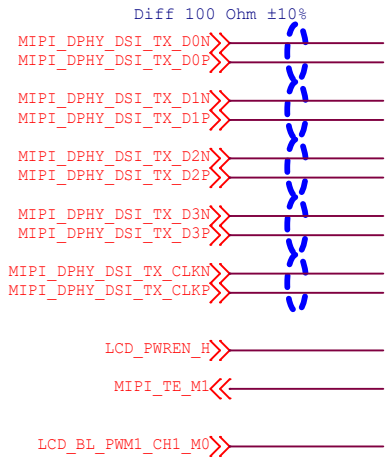


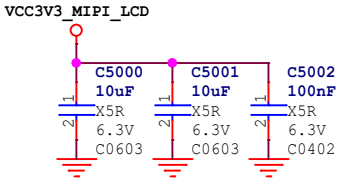


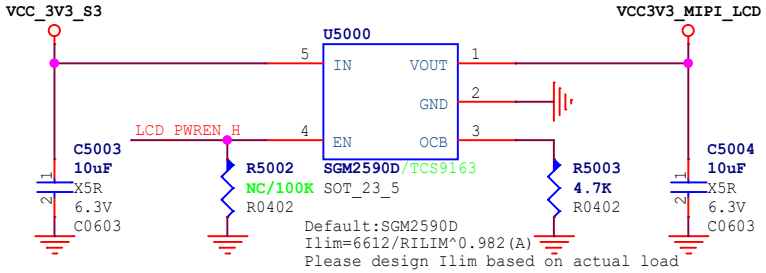
Rockchip Confidential

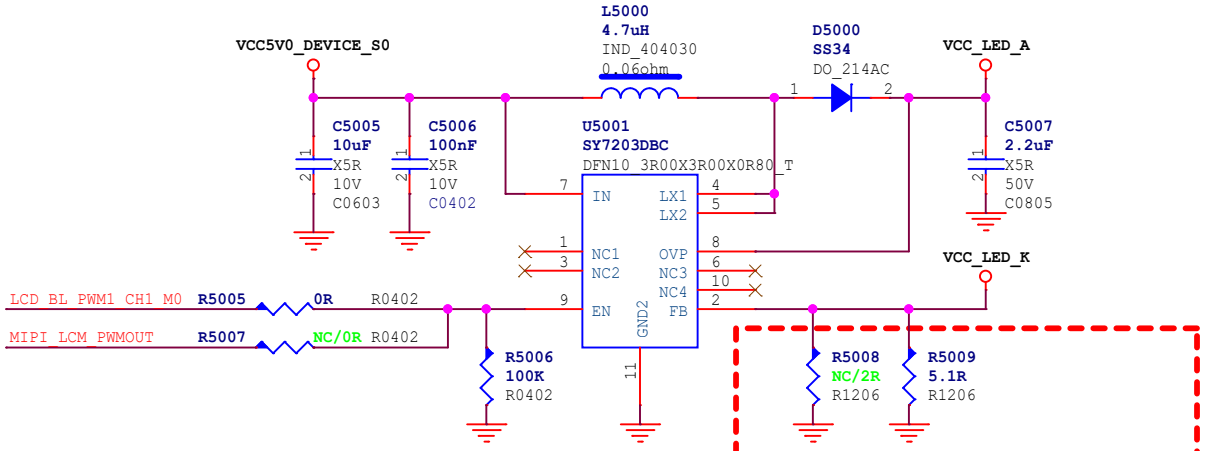
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3576_AIOT_REF_SCH
File:	49.VI-HDMI20 RX to MIPI RX(Opt)
Date:	Tuesday, June 04, 2024
Rev:	V1.1
Designed by:	Wesley Huang
Reviewed by:	
Sheet:	38 of 65

MIPI LCM

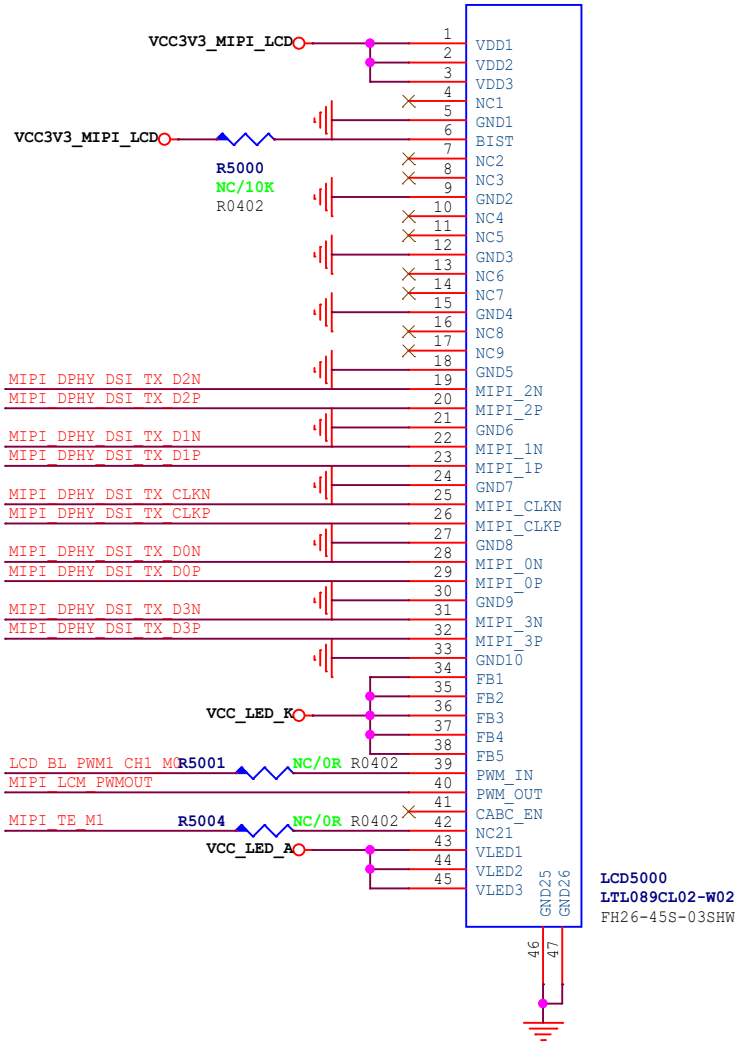








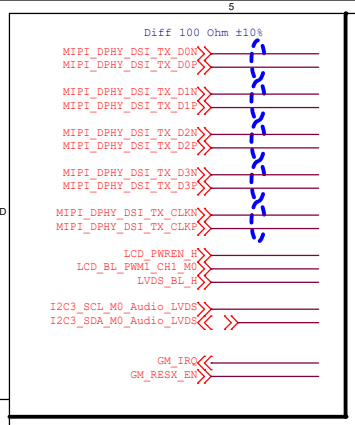
Note:
Adjust the value of resistor according to used LCD.



Rockchip Confidential

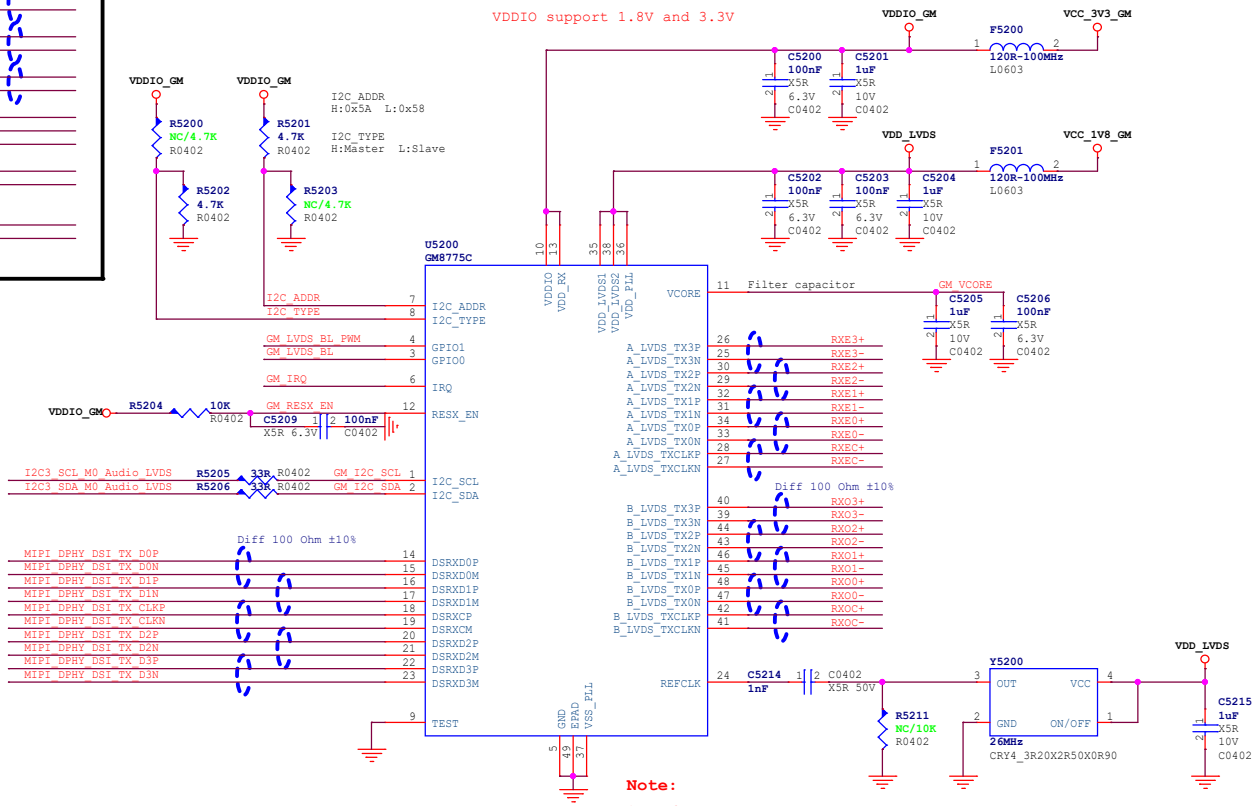
Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	50.VO-LCM MIPI DPHY TX		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by: Wesley Huang	Reviewed by:	Sheet:	39 of 65

MIPI TO Dual LVDS



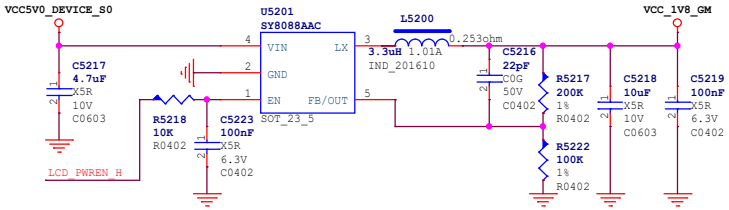
Note:

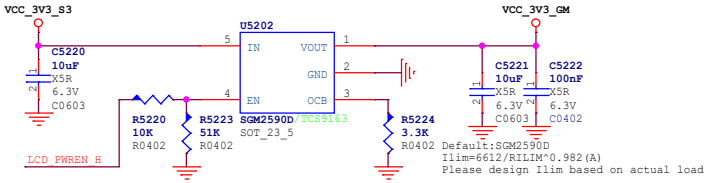
VDDIO support 1.8V and 3.3V

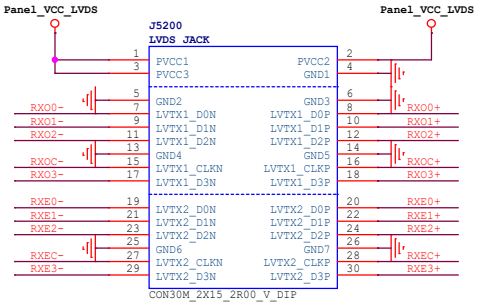


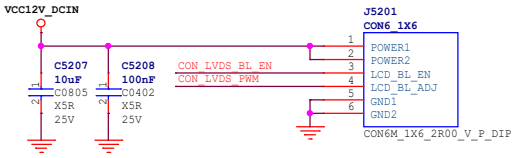
Note:

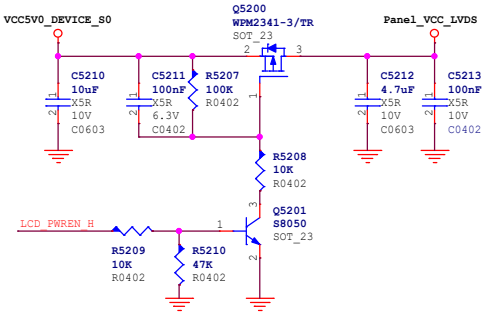
1. GM8775C can use the MIPI clock as the reference clock. In this case, the 26M crystal oscillator can be removed, and this pin should be connected to the ground.
2. When using the master control's MIPI clock as the reference clock, it is necessary to be in continuous mode (i.e., the transmission process will not switch to the LP state). If there is a MIPI frequency spreading function, it should also be turned off.

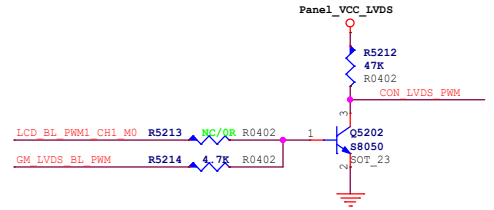


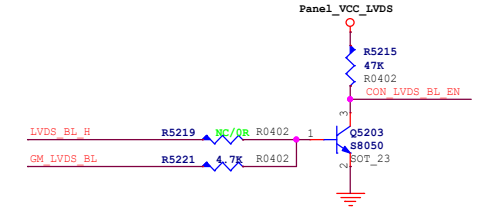










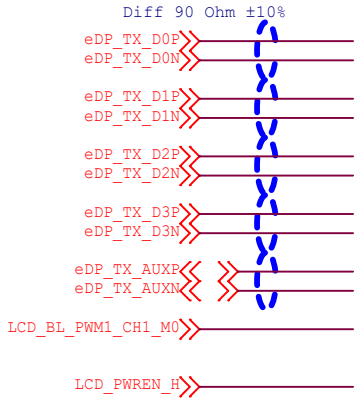


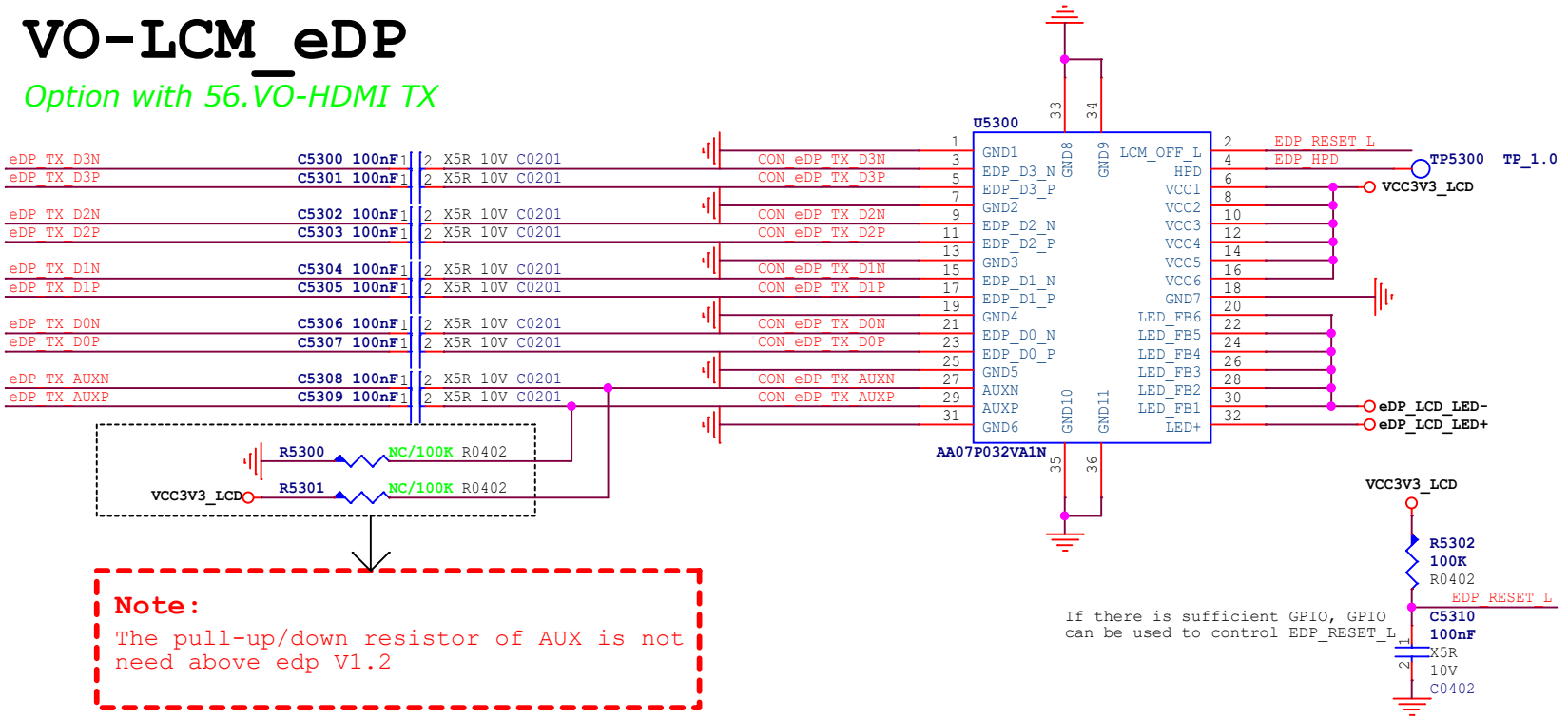
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	52.VO-MIPI to LVDS_GM8775C				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	40 of 65

VO-LCM_eDP

Option with 56.VO-HDMI TX

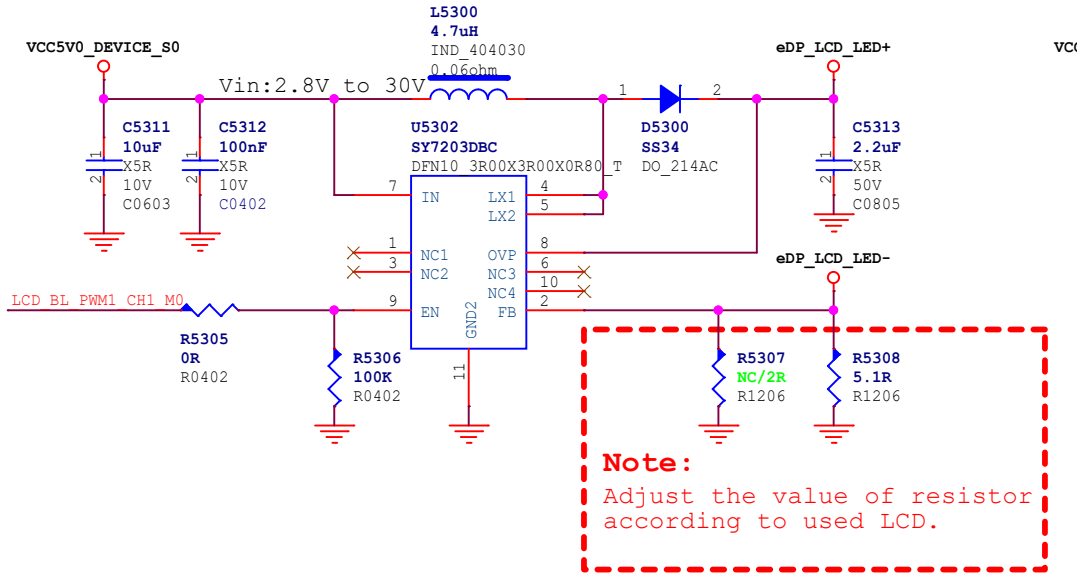




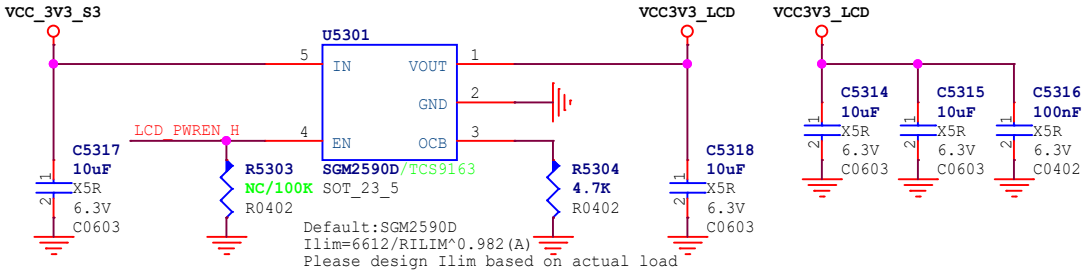
Note:

Signal	IO Level
LCD0_PWREN_H	1.8V/3.3V
LCD0_BL_PWM	3.3V
LCD0_RST_L	3.3V

Note:
The pull-up/down resistor of AUX is not need above edp V1.2



Note:
Adjust the value of resistor according to used LCD.

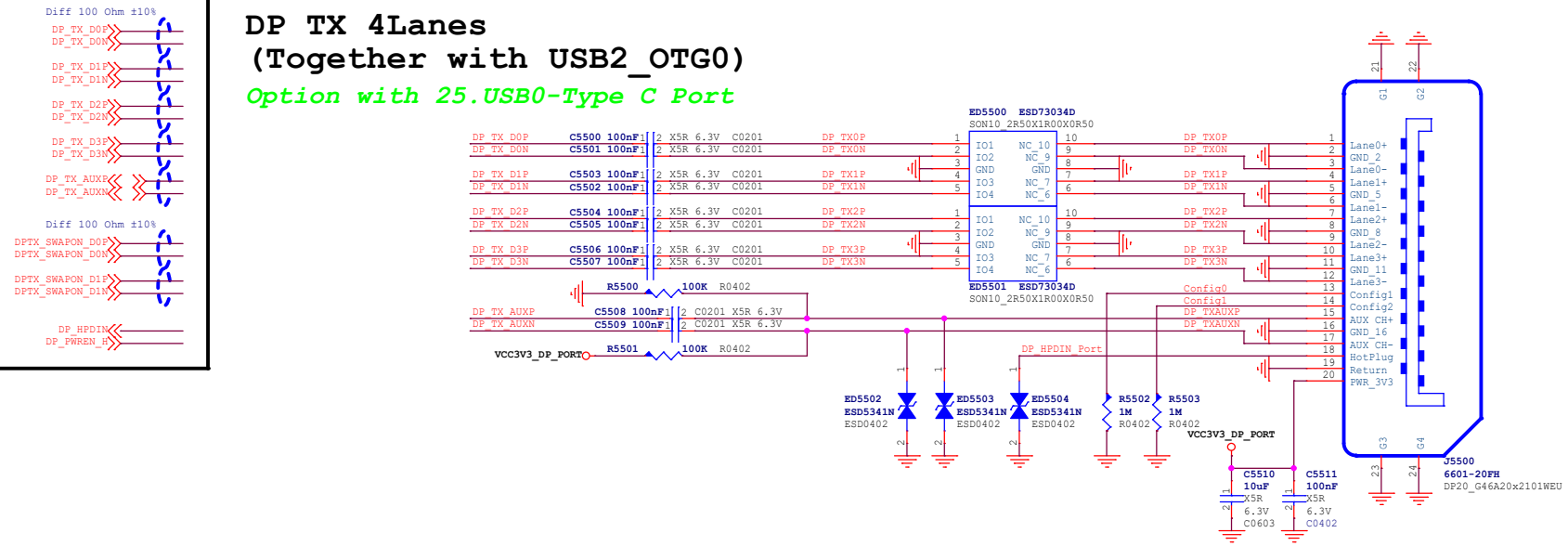


Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	53.VO-LCM eDP TX		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:	Sheet: 41 of 65

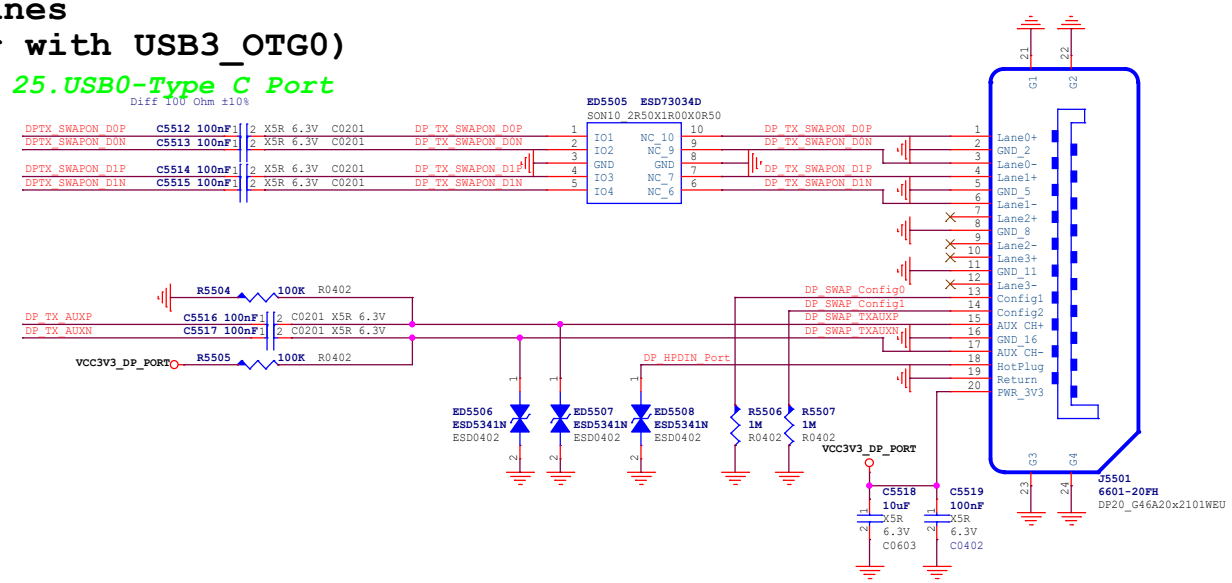
DP TX 4Lanes
(Together with USB2_OTG0)

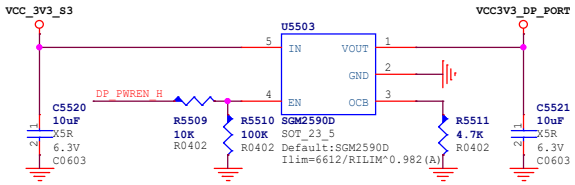
Option with 25.USB0-Type C Port

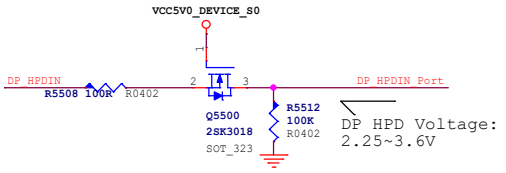


DP TX 2Lanes
(Together with USB3_OTG0)

Option with 25.USB0-Type C Port





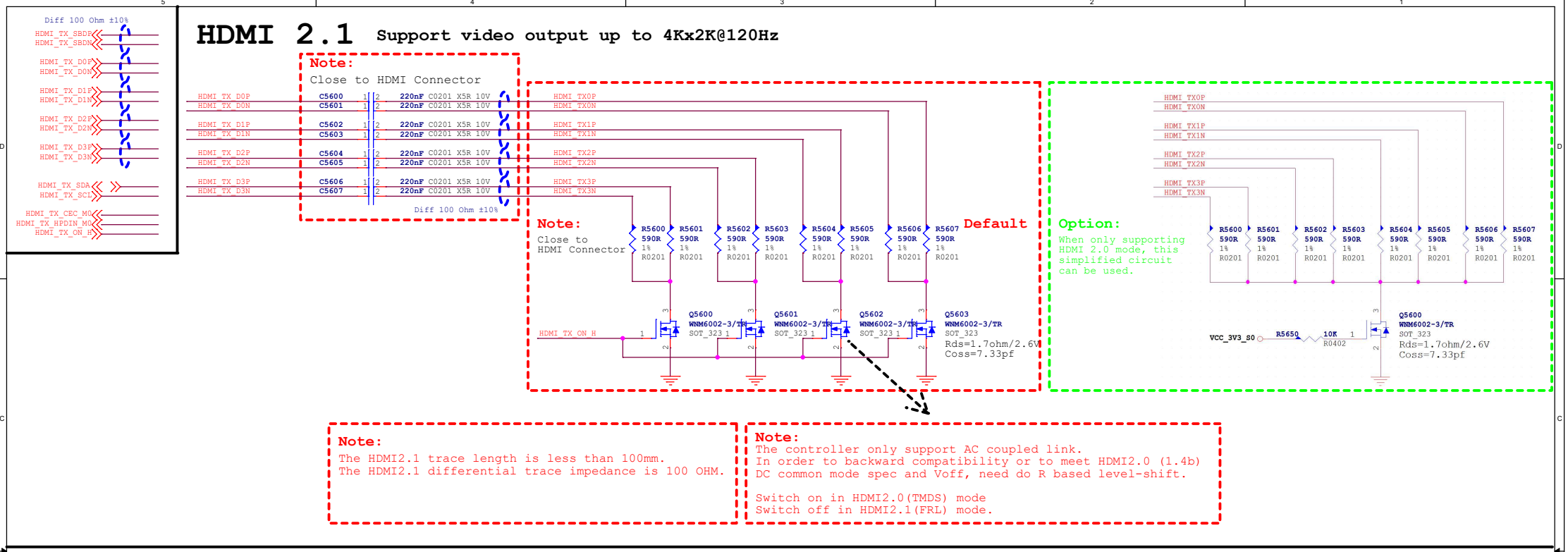


Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH			
File:	58.VO-DP TX			
Date:	Thursday, May 30, 2024		Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:	Sheet:	42 of 65

HDMI 2.1

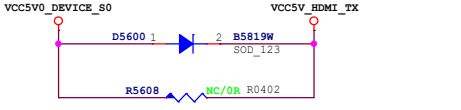
Support video output up to 4Kx2K@120Hz



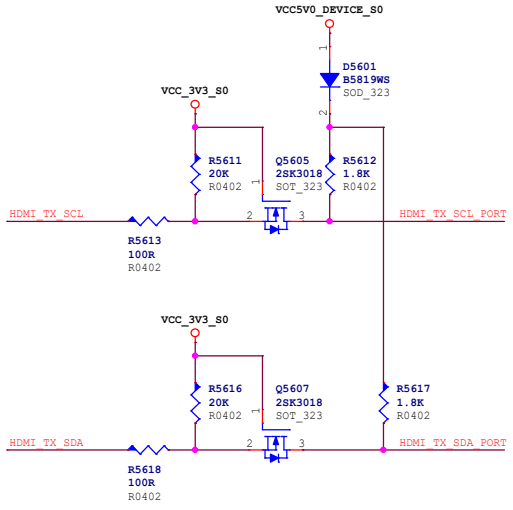
Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

Note:
The controller only support AC coupled link.
In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

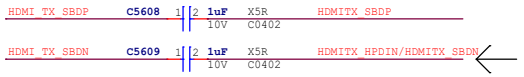
Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.



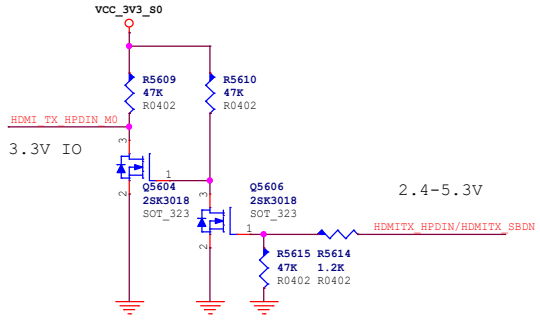
HDMI TX DDC



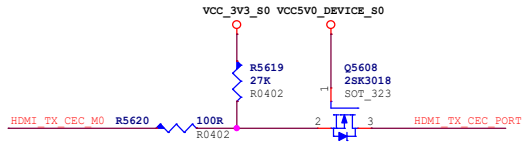
HDMI TX ARC

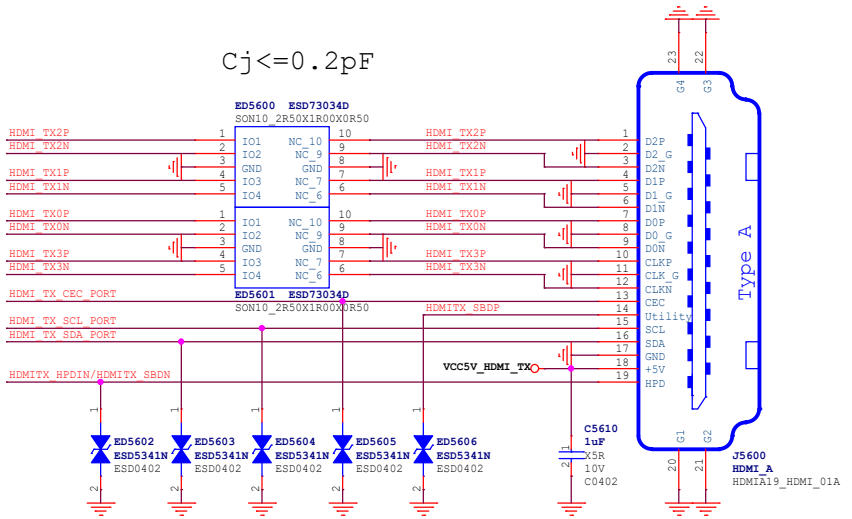


HDMI TX HPD



HDMI TX CEC



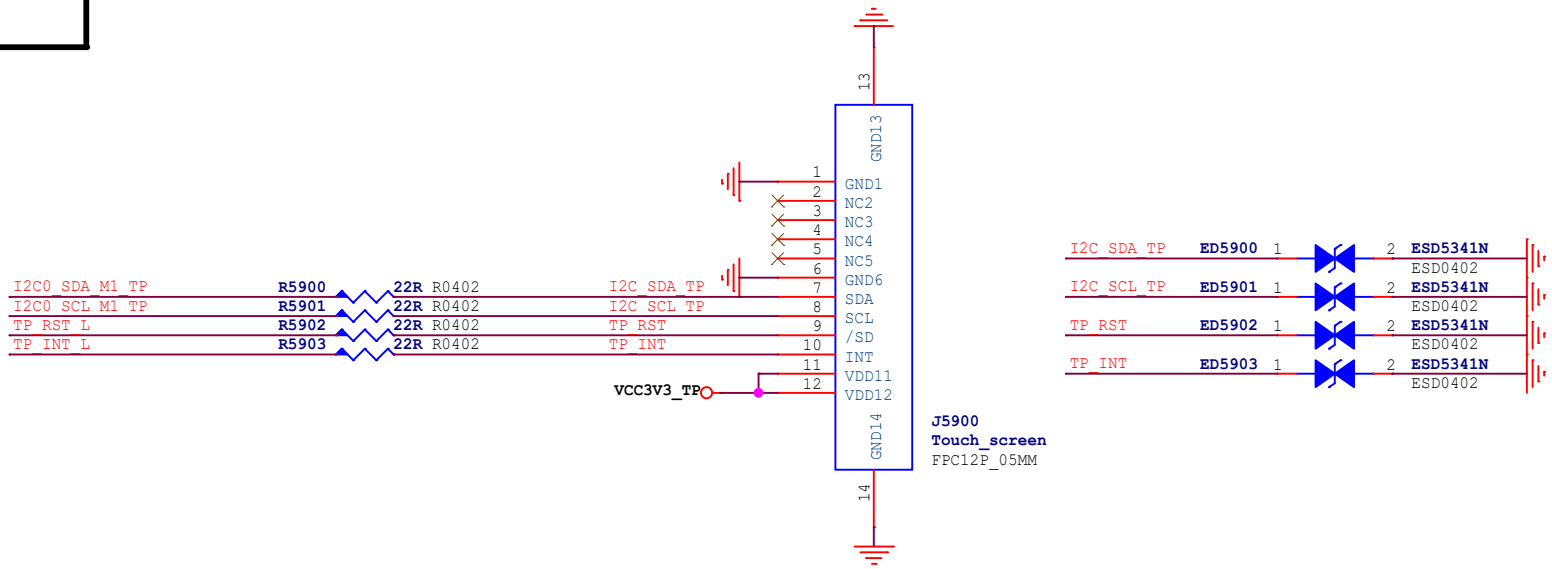


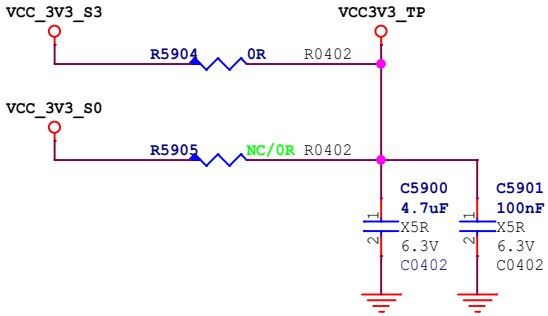
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	56.VO-HDMI TX		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:	Sheet: 43 of 65

Touch Panel connector

I2C0_SCL_M1_TP
I2C0_SDA_M1_TP
TP_RST_L
TP_INT_L





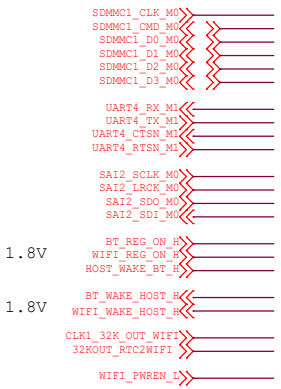
Support touch to wake-up under sleep mode.
Please note that in this usage, the TP module will increase the standby current.
If touch wake-up is not needed, you can move this circuits to the power domain of VCC_3V3_S0

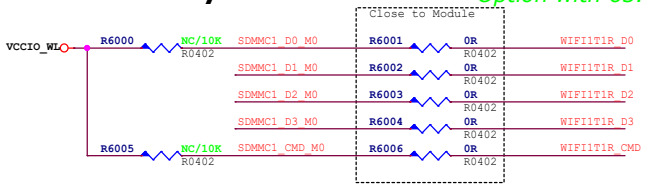
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	59.TP Connector_COF		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by: Wesley Huang	Reviewed by:	Sheet:	44 of 65

SDIO WIFI/BT MODULE

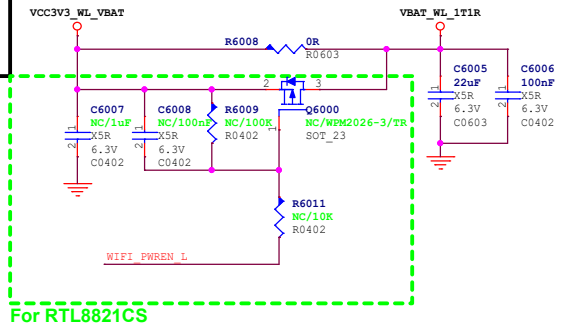
Option with 63.WIFI6/BT-SDIO+UART_2T2R

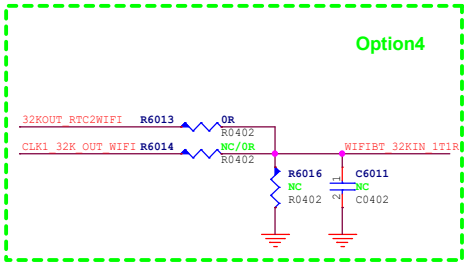


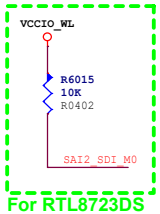


Note:

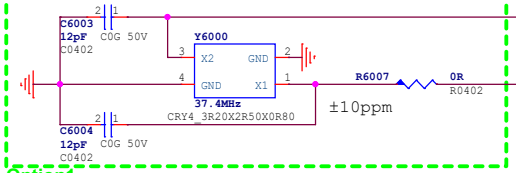
The maximum peak current is 600mA
Close to WIFI module



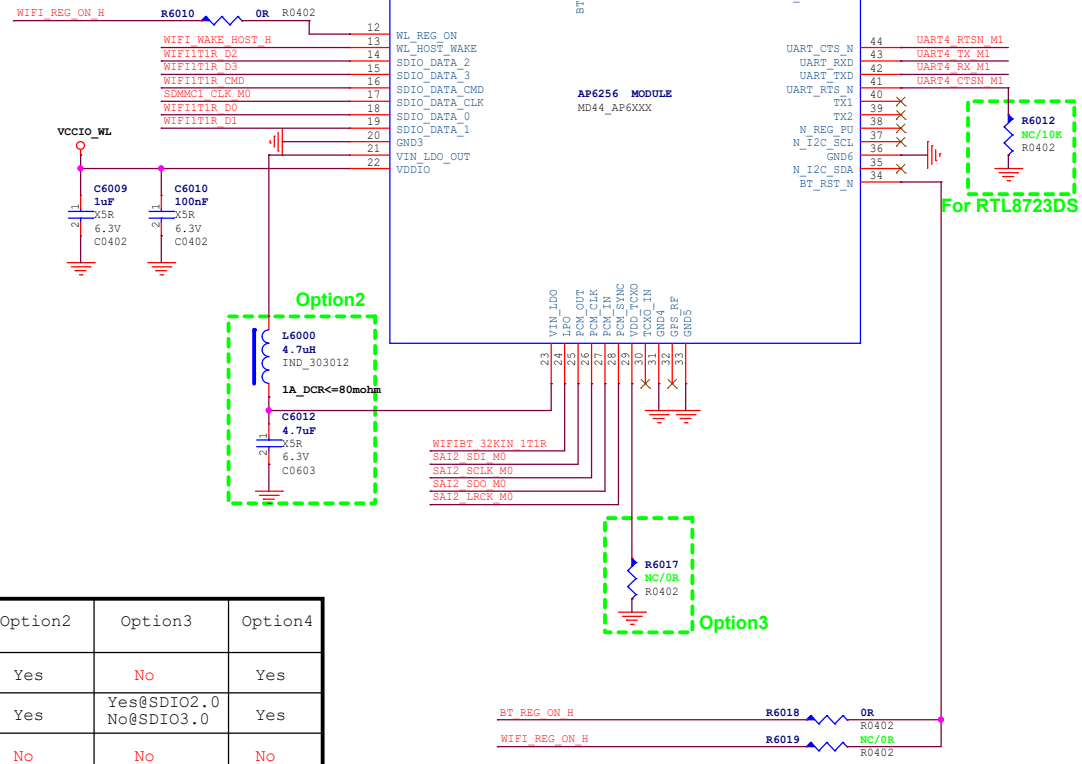




Note:
Adjusted the load capacitance according to the crystal specification.



Using RTL8189ETV/FTV modules,
please notice
WIFI REG ON is on pin12 or pin34,
choose
according to the actual condition.



Using RTL8189ETV/FTV modules, please notice
WIFI REG ON is on pin12 or pin34, choose
according to the actual condition.

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

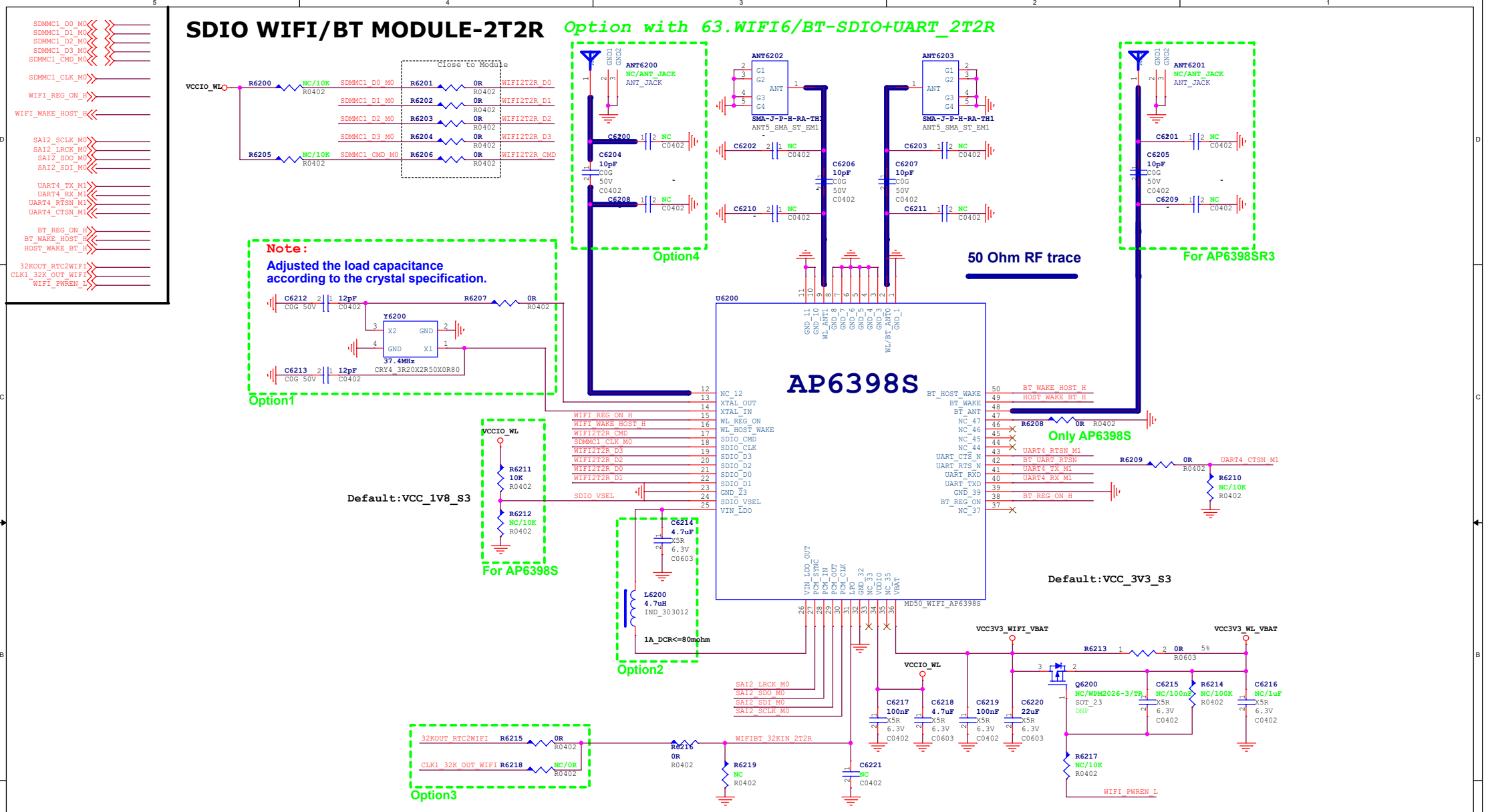
OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	60.WIFI/BT-SDIO+UART_1T1R(Opt)		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang / Reviewed by:	Sheet:	45 of 65

SDIO WIFI/BT MODULE-2T2R

Option with 63.WIFI6/BT-SDIO+UART_2T2R



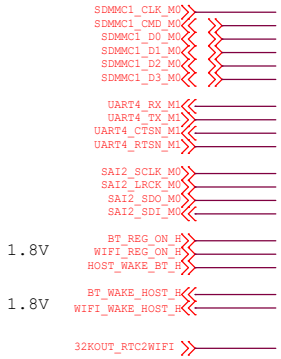
Note:
Yes: option circuit be mounted
No: option circuit not be mounted

OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AP6398S	Yes	Yes	Yes	Yes	5.0	37.4MHz	1.8V/3.3V	Yes	Yes	Yes	No
RTL8822CS Module	Yes	Yes	Yes	Yes	5.0	/	1.8V/3.3V	No	No	No	Yes
UWE5621DS Module	Yes	Yes	Yes	Yes	5.1	/	1.8V/3.3V	No	No	No	Yes

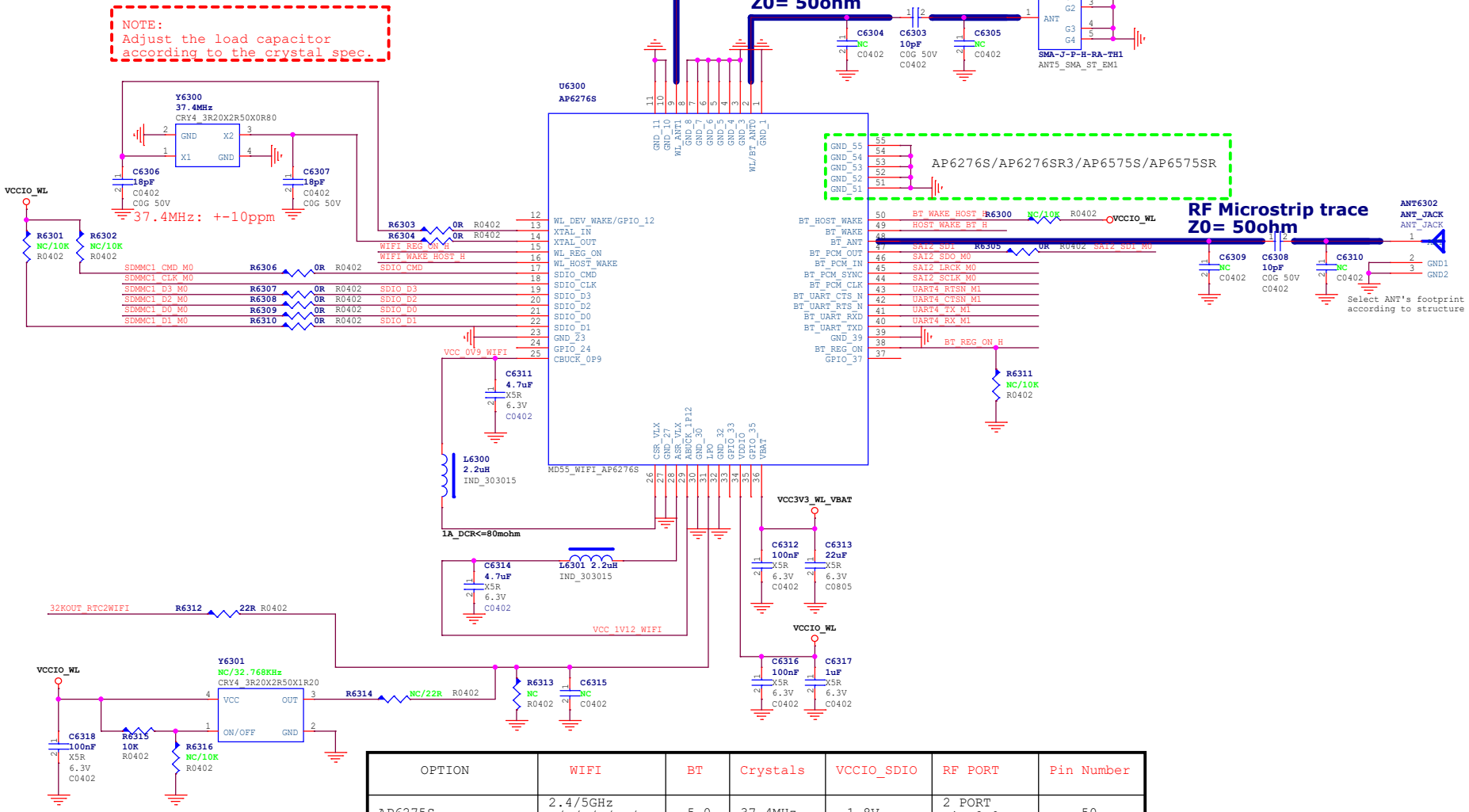
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	62.WIFI/BT-SDIO+UART_2T2R(Opt)		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang / Reviewed by:	Sheet:	46 of 65

WIFI6/BT-SDIO+UART 2T2R



Signal	Default Voltage
BT_REG_ON_H	1.8V
WIFI_REG_ON_H	1.8V
BT_WAKE_HOST	1.8V
HOST_WAKE_BT_H	1.8V
WIFI_WAKE_HOST	1.8V



OPTION	WIFI	BT	Crystals	VCCIO_SDIO	RF PORT	Pin Number
AP6275S	2.4/5GHz A/B/G/N/AC/AX	5.0	37.4MHz	1.8V	2 PORT pin 2,9	50
AP6275SR3	2.4/5GHz A/B/G/N/AC/AX	5.0	37.4MHz	1.8V	3 PORT pin 2,9,48	50
AP6276S	2.4/5GHz A/B/G/N/AC/AX	5.3	37.4MHz	1.8V	2 PORT pin 2,9	55
AP6276SR3	2.4/5GHz A/B/G/N/AC/AX	5.3	37.4MHz	1.8V	3 PORT pin 2,9,48	55

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	63.WIFI6/BT-SDIO+UART_2T2R				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	47 of 65

PCIe WIFI6/BT Module-2T2R

Option with 63.WIFI6/BT-SDIO+UART_2T2R and 81.PCIe-PCIe Slot_36P

Diff 100 Ohm ±10%
PCIE0_REFCLKP
PCIE0_REFCLKN
Diff 85 Ohm ±10%
PCIE0_TXP
PCIE0_TXN
PCIE0_RXP
PCIE0_RXN
PCIE0_WAKEn_M0
PCIE0_CLKREQn_M1_WIFI
PCIE0_PERSTn_WIFI
32KOUT_RTC2WIFI
SAI2_SCLK_M0
SAI2_LRCK_M0
SAI2_SDO_M0
SAI2_SDI_M0
UART4_TX_M1
UART4_RX_M1
UART4_RTSN_M1
UART4_CTSN_M1
BT_REG_ON_H
BT_WAKE_HOST_H
HOST_WAKE_BT_H
WIFI_REG_ON_H
WIFI_WAKE_HOST_H

ANT6400
SMA-J-P-H-RA-TH1
ANT5_SMA_ST_EM1
ANT6401
SMA-J-P-H-RA-TH1
ANT5_SMA_ST_EM1
ANT6402
ANT_JACK
ANT_JACK
C6400 NC C0402
C6401 NC C0402
C6402 10pF C0G 50V C0402
C6403 10pF C0G 50V C0402
C6404 NC C0402
C6405 NC C0402
C6406 NC C0402
C6407 NC/10pF C0G 50V C0402
C6408 NC C0402

50 Ohm RF trace

This standalone BT-ANT is reserved for AP6275PR3.
Leave PIN48 float for AP6275P, of which BT-ANT is mux with WIFI.

U6400
AP6275P
MD55_WIFI_AP6276P

Pins for AP6276P
GND_55
GND_54
GND_53
GPIO_52
GPIO_51

NOTE:
Adjust the load capacitor according to the crystal spec.
Y6400
XIN_WIFI
XOUT_WIFI
C6413 12pF C0G 50V C0402
37.4MHz CRY4_3R20X2R50X0R8
C6414 12pF C0G 50V C0402
R6400 0R R0402

PCIE0_PERSTn_1V8
XIN_WIFI
XOUT_WIFI
WIFI_REG_ON_H
WIFI_WAKE_HOST_H
SAI2_SDI_M0
SAI2_SDO_M0
SAI2_LRCK_M0
SAI2_SCLK_M0
PCIE0_WAKEn_1V8
R6401 0R R0402
C6415 4.7uF X5R 6.3V C0402
PCIE_PERST_L
XTAL_IN
XTAL_OUT
WL_REG_ON
WL_HOST_WAKE
GPIO_17
GPIO_18
BT_PCM_OUT
BT_PCM_IN
BT_PCM_SYNC
BT_PCM_CLK
GND_23
PCIE_PME_L
CBUCK_0P9
BT_HOST_WAKE
BT_WAKE
BT_ANT
PCIE_TX_P
PCIE_TX_N
PCIE_RX_P
PCIE_RX_N
BT_UART_CTS_N
BT_UART_RTS_N
BT_UART_RXD
BT_UART_TXD
GND_39
BT_REG_ON
PCIE_CLKREQ_L
BT_WAKE_HOST_H
HOST_WAKE_BT_H
AP627xP_PCIE_TXP
AP627xP_PCIE_TXN
AP627xP_PCIE_RXP
AP627xP_PCIE_RXN
UART4_RTSN_M1
UART4_CTSN_M1
UART4_TX_M1
UART4_RX_M1
BT_REG_ON_H
PCIE0_CLKREQn_1V8
C6409 100nF X5R 10V C0201 PCIE0_RXP
C6410 100nF X5R 10V C0201 PCIE0_RXN
C6411 100nF X5R 10V C0201 PCIE0_TXP
C6412 100nF X5R 10V C0201 PCIE0_TXN
CSR_VLX
GND_27
ASR_VLX
ABUCK_1P12
GND_30
LPO
GND_32
PCIE_RCLK_N
VDDIO
PCIE_RCLK_P
VBAT

NOTE:
The packaging of AP6276P is compatible with AP6275P

AP627xP_REFCLKP
AP627xP_REFCLKN
C6416 100pF X5R 25V C0201 PCIE0_REFCLKP
C6417 100pF X5R 25V C0201 PCIE0_REFCLKN

L6400 2.2uH IND_303015 1A_DCR<=80mohm
L6401 2.2uH IND_303015 1A_DCR<=80mohm
C6418 4.7uF X5R 6.3V C0402
VCC3V3_WL_VBAT
C6419 100nF X5R 6.3V C0402
C6420 22uF X5R 6.3V C0603
VCCIO_WL
C6423 100nF X5R 6.3V C0402
C6424 4.7uF X5R 6.3V C0402

VBAT:(3.1-3.8V)/1.2A
VDDIO:(1.68-1.98V)/300mA.

32.768KHZ:
+/-25ppm/30-70%/1.8V
Y6401
NC/32.768KHz
CRY4_3R20X2R50X1R20
VCCIO_WL
C6421 NC/100nF X5R 6.3V C0402
R6405 NC/470K R0402
VCC
OUT
ON/OFF
GND
32KOUT_CRY
32KOUT_RTC2WIFI
R6402 NC/0R R0402
R6403 22R R0402
WIFIBT_32KIN
R6404 NC R0402
C6422 NC C0402

PCIE0_PERSTn_WIFI
R6408 0R R0402
PCIE0_PERSTn_1V8
OD
PCIE0_CLKREQn_M1_WIFI
R6411 0R R0402
PCIE0_CLKREQn_1V8

VCC_3V3_S3
3.3V
PCIE0_WAKEn_M0
R6406 47K R0402
R6407 100K R0402
VCC_1V8_S0
Q6400 S8050 SOT_23
R6409 100K R0402
R6410 47K R0402
VCCIO_WL
R6412 NC/47K R0402
OD
PCIE0_WAKEn_1V8
Option

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Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	64.WIFI6/BT-PCIe+UART_2T2R(Opt)				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	48 of 65

RMII

Option with 67.Ethernet-GEPHY_RGMII1

GMAC1_TXD0_M0
GMAC1_TXD1_M0
GMAC1_TXCTL_M0
GMAC1_RXD0_M0
GMAC1_RXD1_M0
GMAC1_RXCTL_M0
GMAC1_MCLKINOUT_M0
GMAC1_MDC_M0
GMAC1_MDIO_M0
ETH_CLK1_25M_OUT_M0
GMAC1_RSTn

Option

FEPHY0_CKXTAL1_I 1 — Y6500 (X1, GND, GND, X2; 4, 2, 3) — FEPHY0_CKXTAL2_O/I

C6500 NC/18pF C0G 50V C0402

NC/25MHz CRY4_3R20X2R50X0R80

C6501 NC/18pF C0G 50V C0402

Default

ETH_CLK1_25M_OUT_M0 — R6503 0R R0402 — FEPHY0_CKXTAL1_I

R6505 NC/0R R0402 — FEPHY0_CKXTAL2_O/I

R6506 NC/0R R0402 — FEPHY0_CKXTAL1_I

Default: Refclk:MAC output,PHY input

GMAC1_MCLKINOUT_M0 — R6512 0R R0402 — FEPHY0_TXC

C6506 NC C0402

High-tension area

FEPHY0_MDI0P — R6500 0R R0402 — ED6500 NC/UDD32C03L01 SOD_323

FEPHY0_MDI0N — R6501 0R R0402

FEPHY0_MDI1P — R6502 0R R0402 — ED6501 NC/UDD32C03L01 SOD_323

FEPHY0_MDI1N — R6504 0R R0402

U6500 UTH16C01 SOIC16_12R70X9R40X6R27

1 FEPHY0_A+
2 FEPHY0_MCT1
3 FEPHY0_A-
4
5
6 FEPHY0_B+
7 FEPHY0_MCT2
8 FEPHY0_B-

C6502 10nF X5R 25V C0402

C6503 10nF X5R 25V C0402

FEPHY0_MCT1
FEPHY0_MCT2

D6500 NC/BS3500NCF SMB_F

D6501 NC/BS3500NCF SMB_F

J6500 RJ45_1008RGF_11B RJ45_1008RGF_11B

Tab down

FEPHY0_B-
FEPHY0_B+
FEPHY0_A-
FEPHY0_A+

GLED+ GLED- YLED+ YLED-

9 FEPHY0_LED1/PHYAD1
10 FEPHY0_LED1-
11 FEPHY0_LED0+
12 FEPHY0_LED0/PHYAD0/PMEB

NC1 NC2 G1 G2

R6507 75R R0805 — R6508 75R R0805 — R6509 75R R0805 — R6510 75R R0805

C6504 1000pF 2KV C1206L — LAN_CHASSIS_GND

R6511 1M R1206L — C6505 1000pF 2KV C1206L

Note:

YT8512C/RTL8201F only support 3.3V IO
VCCIO4 must be changed to 3.3V power supply

VCC_3V3_S0 — R6517 0R R0402 — VCCA3V3_FEPHY0

Close to PIN7,30

C6507 4.7uF X5R 6.3V C0402

C6508 100nF X5R 6.3V C0402

C6509 100nF X5R 6.3V C0402

VCC3V3_FEPHY0 — R6520 0R R0402

Close to PIN14

C6511 4.7uF X5R 6.3V C0402

C6512 100nF X5R 6.3V C0402

R6513 NC/4.7K R0402 — FEPHY0_RXD3/CLK_CTL — R6514 4.7K R0402 — VCC3V3_FEPHY0

YT8512C/RTL8201F:
Pull Low for RMII REF_CLK Output mode
Pull High for RMII REF_CLK Input mode(default)

FEPHY0_RXDV — R6518 4.7K R0402 — VCC3V3_FEPHY0

Pull High for RMII mode(default)

R6519 4.7K R0402 — FEPHY0_RXER/FXEN

Pull Low for UTP Mode(default)
Pull High for Fiber Mode

R6523 4.7K R0402 — FEPHY0_RXD1 — R6524 NC/4.7K R0402 — VCC3V3_FEPHY0

Pull Low for LED0 Mode(default)
Pull High for WOL Mode WOL:Wake-on-LAN

Default:LED

VCC3V3_FEPHY0

FEPHY0_LED0+ — R6516 510R R0402

FEPHY0_LED0/PHYAD0/PMEB — R6515 4.7K R0402

C6510 NC/100pF C0G 50V C0402 Reserve for EMI.

R6521 510R R0402 — FEPHY0_LED1-

R6522 4.7K R0402 — FEPHY0_LED1/PHYAD1

C6513 NC/100pF C0G 50V C0402 Reserve for EMI.

PHY Address Config

PHY Address	PHYAD[1:0]
1 (default)	2'b01

VCC3V3_FEPHY0

FEPHY0_TXC
GMAC1_TXD0_M0
GMAC1_TXD1_M0
FEPHY0_RXD3/CLK_CTL
FEPHY0_RXD2/INT
FEPHY0_RXD1
FEPHY0_RXD0

R6525 10K R0402 — VCC3V3_FEPHY0

R6526 22R R0402 — GMAC1_RXD1_M0

R6527 22R R0402 — GMAC1_RXD0_M0

U6501 YT8512C /RTL8201F QFN32_5R00X5R00X1R00_T

TXD0 TXC DVDD33 RXC RXD3/CLK_CTL RXD2/INTB RXD1 RXD0

TXD1 TXD2 TXD3 TXEN PHYRSTB MDC MDIO LED0/PHYAD0/PMEB

RXDV AVDD33_1 MDI1- MDI1+ MDI0- MDI0+ AVDD100OUT RSET

LED1/PHYAD1 CRS/CRS_DV COL RXER/FXEN DVDD100OUT AVDD33_2 CKXTAL1_I CKXTAL2/O/EXT_I E-Pad

VCC3V3_FEPHY0 — R6528 NC/10K R0402 — FEPHY0_TXD3

GMAC1_RSTn — R6529 0R R0402 — FEPHY0_RSTn

PHYRSTB is 3.3V IO

VCC3V3_FEPHY0 — R6530 NC/10K R0402

C6514 100nF X5R 6.3V C0402

VCC3V3_FEPHY0 — R6532 1.8K R0402 — GMAC1_MDC_M0 — GMAC1_MDIO_M0

GMAC1_RXCTL_M0 — R6533 22R R0402 — FEPHY0_CRS_DV — FEPHY0_RXER/FXEN

FEPHY0_LED0/PHYAD0/PMEB
FEPHY0_LED1/PHYAD1

FEPHY0_MDI1N
FEPHY0_MDI1P
FEPHY0_MDI0N
FEPHY0_MDI0P
FEPHY0_AVDD100OUT
FEPHY0_RSEL

VCCA3V3_FEPHY0

R6531 2.49K 1% R0402

C6515 100nF X5R 6.3V C0402

C6516 NC/1uF X5R 6.3V C0402

FEPHY0_CKXTAL2_O/I
FEPHY0_CKXTAL1_I

FEPHY0_DVDD100OUT

R6534 4.7K R0402

C6517 100nF X5R 6.3V C0402

C6518 NC/1uF X5R 6.3V C0402

VCCA3V3_FEPHY0

Note: For YT8512C

If GMAC1_RXCTL_M0 has pull-up resistance by default, then 4.7K pull-down resistance is required

Default

Refclk:MAC output,PHY input		Refclk:MAC input,PHY output	
GMACx_TXD0	→ PHY_TXD0	GMACx_TXD0	→ PHY_TXD0
GMACx_TXD1	→ PHY_TXD1	GMACx_TXD1	→ PHY_TXD1
GMACx_TXD2		GMACx_TXD2	
GMACx_TXD3		GMACx_TXD3	
GMACx_TXEN	→ PHY_TXEN	GMACx_TXEN	→ PHY_TXEN
GMACx_TXCLK		GMACx_TXCLK	
GMACx_RXD0	← PHY_RXD0	GMACx_RXD0	← PHY_RXD0
GMACx_RXD1	← PHY_RXD1	GMACx_RXD1	← PHY_RXD1
GMACx_RXD2		GMACx_RXD2	
GMACx_RXD3		GMACx_RXD3	
GMACx_RXDV	← PHY_CRS_DV	GMACx_RXDV	← PHY_CRS_DV
GMACx_RXCLK		GMACx_RXCLK	
GMACx_RXER	← PHY_RXER	GMACx_RXER	← PHY_RXER
GMACx_MDC	→ PHY_MDC	GMACx_MDC	→ PHY_MDC
GMACx_MDIO	↔ PHY_MDIO	GMACx_MDIO	↔ PHY_MDIO
GMACx_MCLKINOUT	→ PHY_TXC	GMACx_MCLKINOUT	← PHY_TXC
ETHx_REFCLKO_25M	→ PHY OSC	ETHx_REFCLKO_25M	→ PHY OSC

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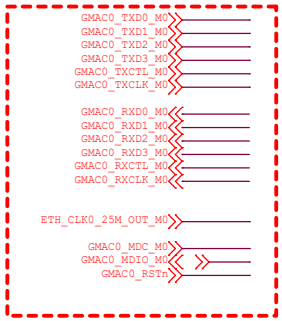
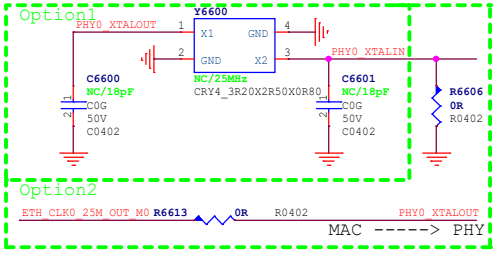
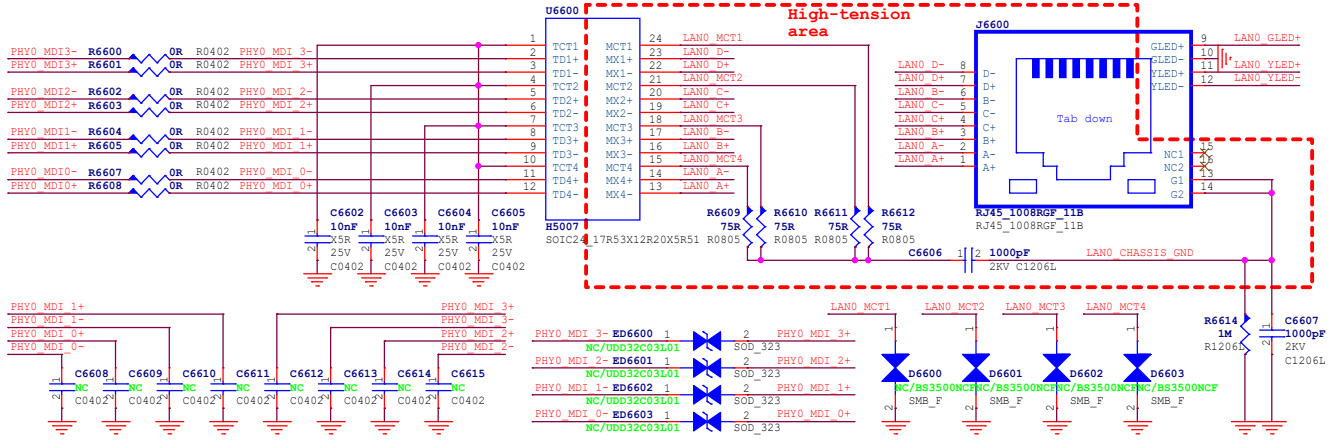
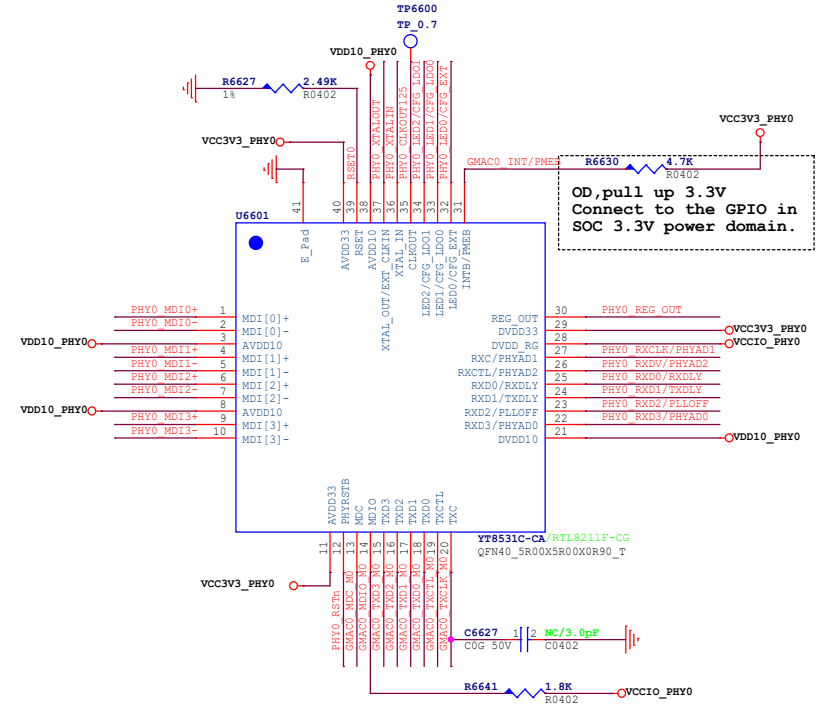
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	65.Ethernet-FEPHY_RMII1(Opt)		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:	Sheet: 49 of 65

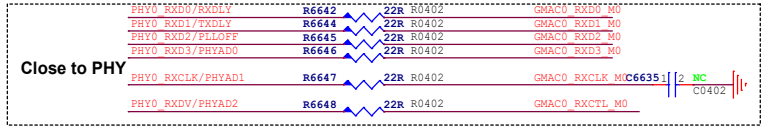
RGMII0_M0



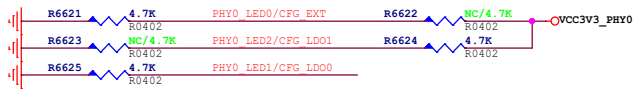








RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	PHY0_LED2
External 3.3V	1'b1	2'b00	String 510R to GND
External 1.8V	1'b1	2'b10	String 510R to VCC3V3_PHY
Internal 1.8V (default)	1'b0	2'b10	String 510R to VCC3V3_PHY

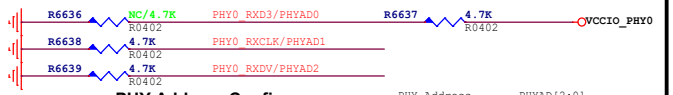


VCC_PHY0_IO Voltage Config

Pull-up to disable PLL @ ALDPS mode(Low power mode)

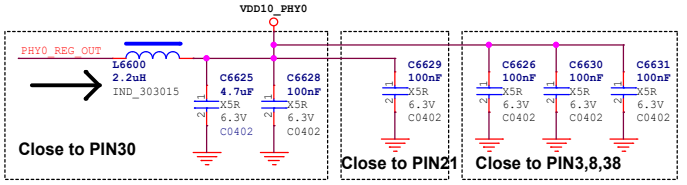
Pull-up for additional 2ns delay to RXC for data latching

Pull-up for additional 2ns delay to TXC for data latching

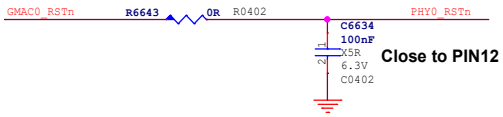


PHY Address Config

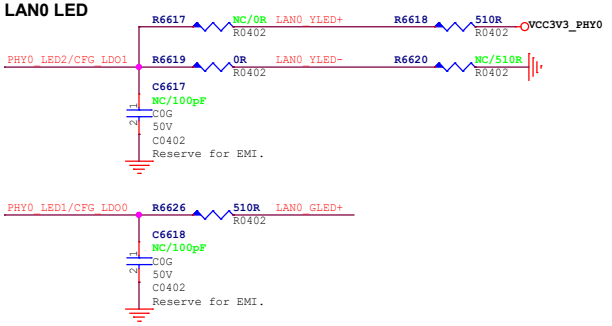
PHY Address	PHYAD[2:0]
1 (default)	3'b001

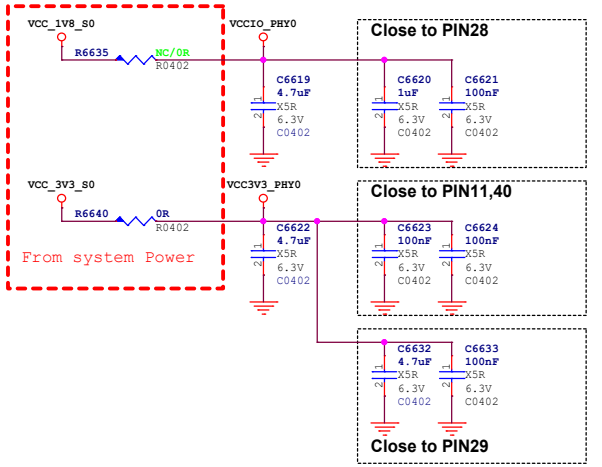


PHYRSTB is 3.3V IO



LAN0 LED





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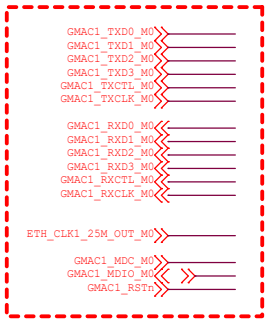
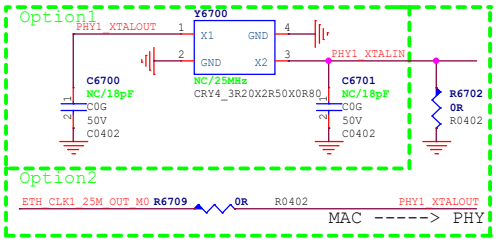
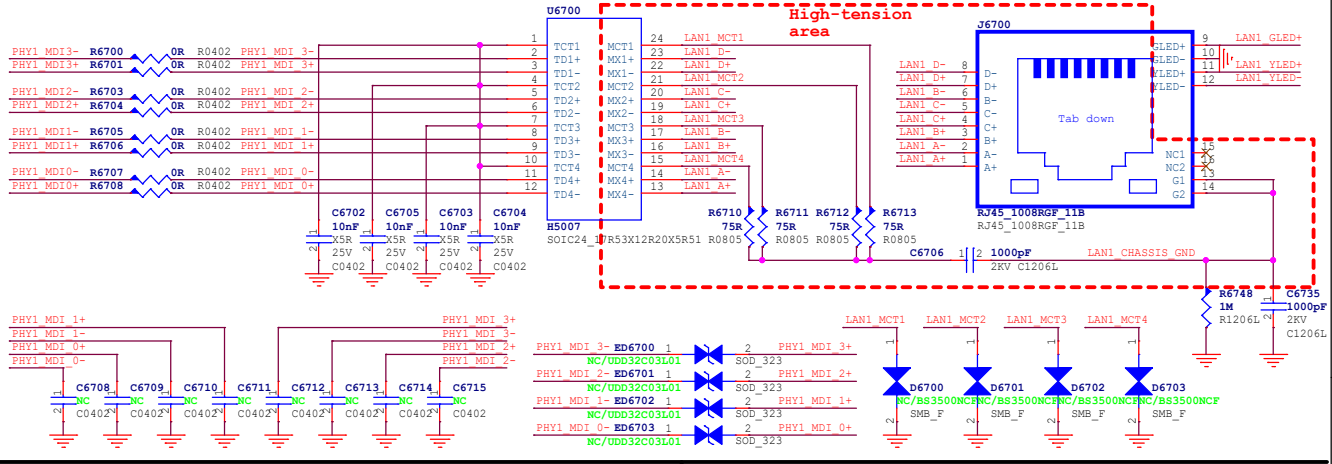
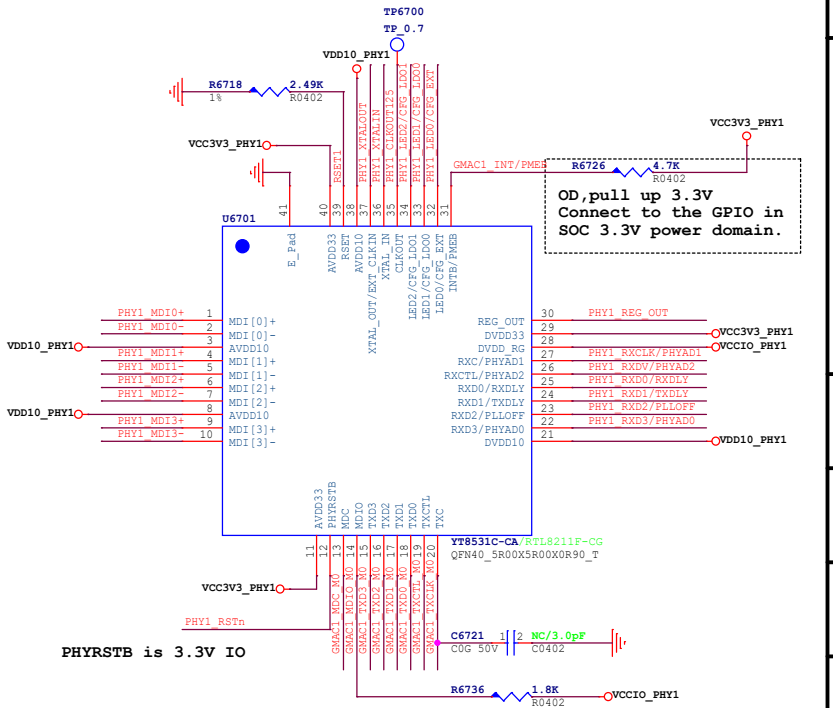
Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	66.Ethernet-GEPHY_RGMII0				
Date:	Thursday, May 30, 2024		Rev:	V1.1	
Designed by:	Wesley Huang	Reviewed by:		Sheet:	50 of 65

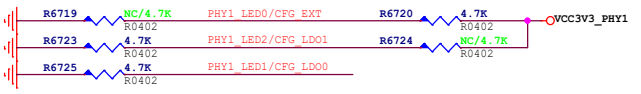
RGMII1_M0











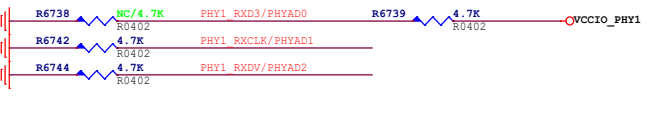
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	PHY1_LED2
External 3.3V (default)	1'b1	2'b00	String 510R to GND
External 1.8V	1'b1	2'b10	String 510R to VCC3V3_PHY
Internal 1.8V	1'b0	2'b10	String 510R to VCC3V3_PHY

VCC_PHY0_IO Voltage Config

Pull-up to disable PLL @ ALDPS mode(Low power mode)

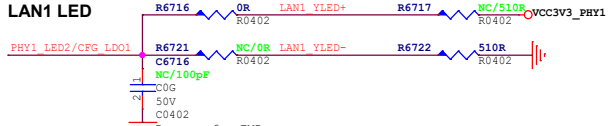
Pull-up for additional 2ns delay to RXC for data latching

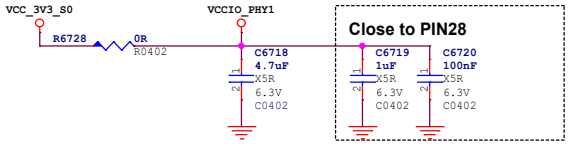
Pull-up for additional 2ns delay to TXC for data latching

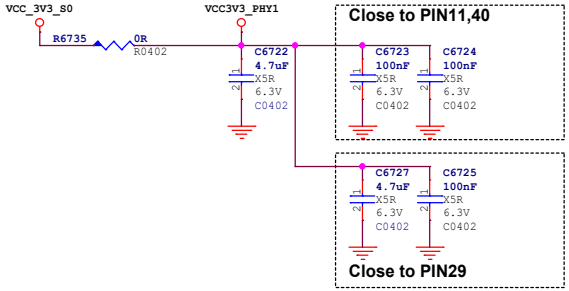


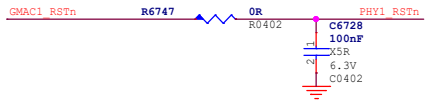
PHY Address	PHYAD[2:0]
1 (default)	3'b001

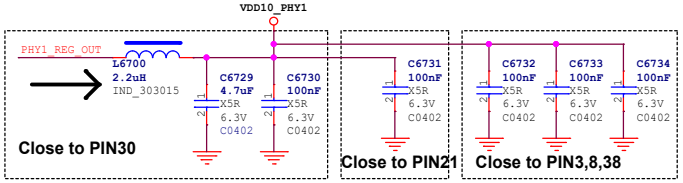
PHY Address Config











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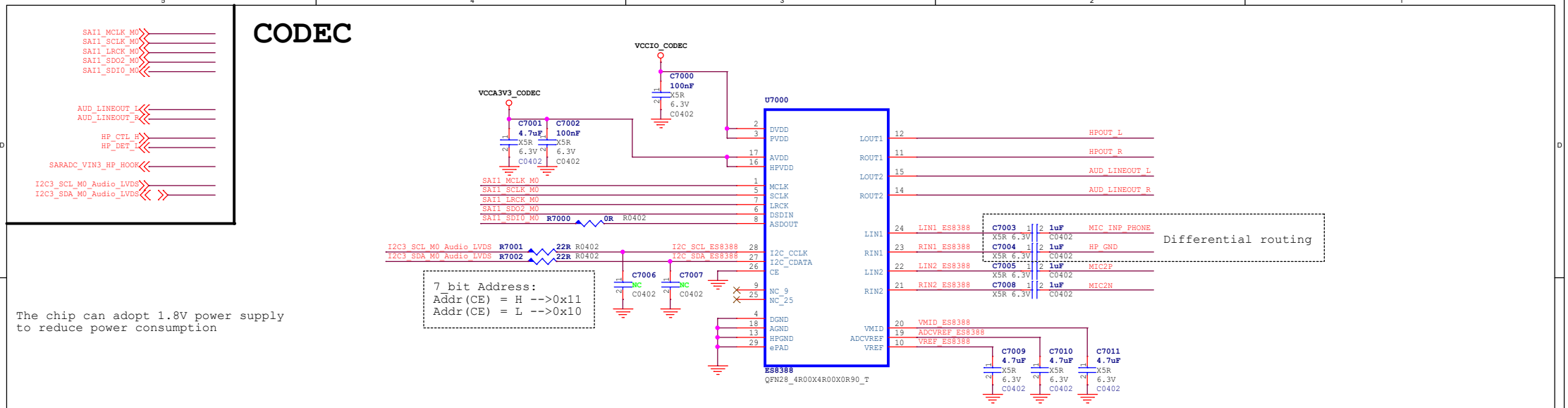
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	67.Ethernet-GEPHY_RGMII1		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:	Sheet: 51 of 65

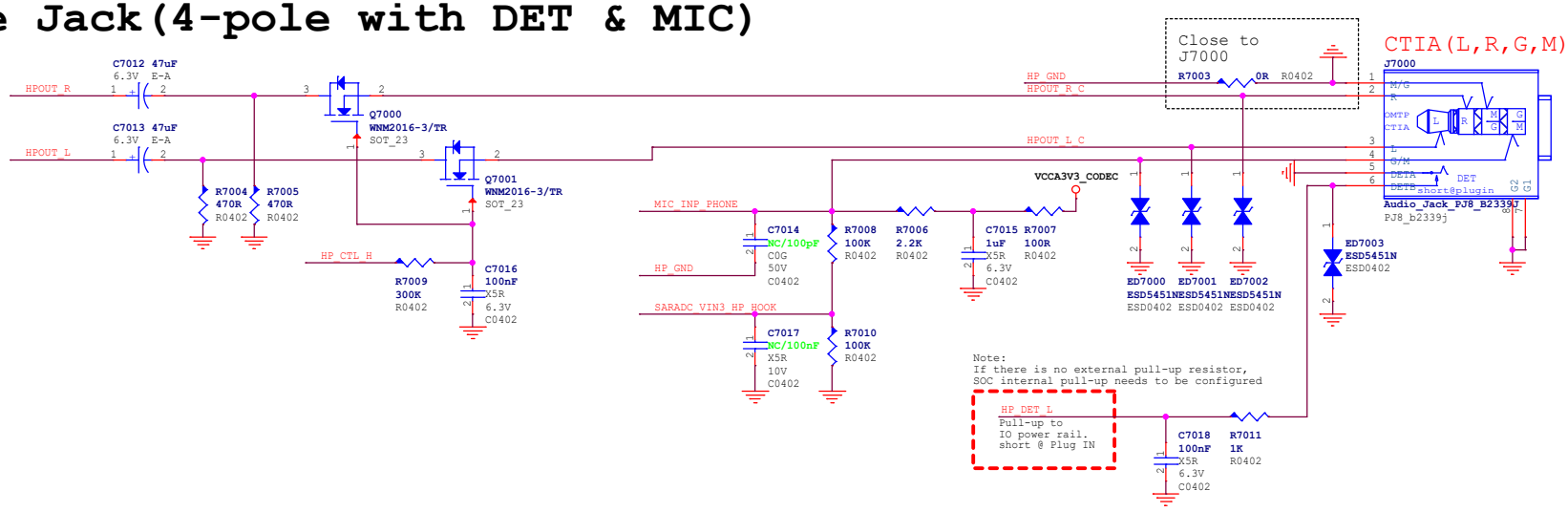
CODEC



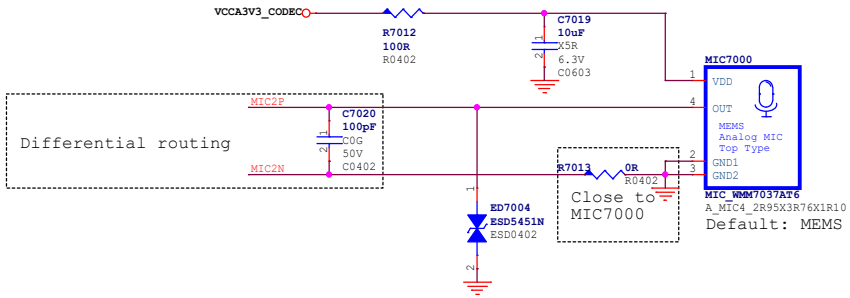
7_bit Address:
Addr(CE) = H -->0x11
Addr(CE) = L -->0x10

The chip can adopt 1.8V power supply
to reduce power consumption

Headphone Jack(4-pole with DET & MIC)



MIC



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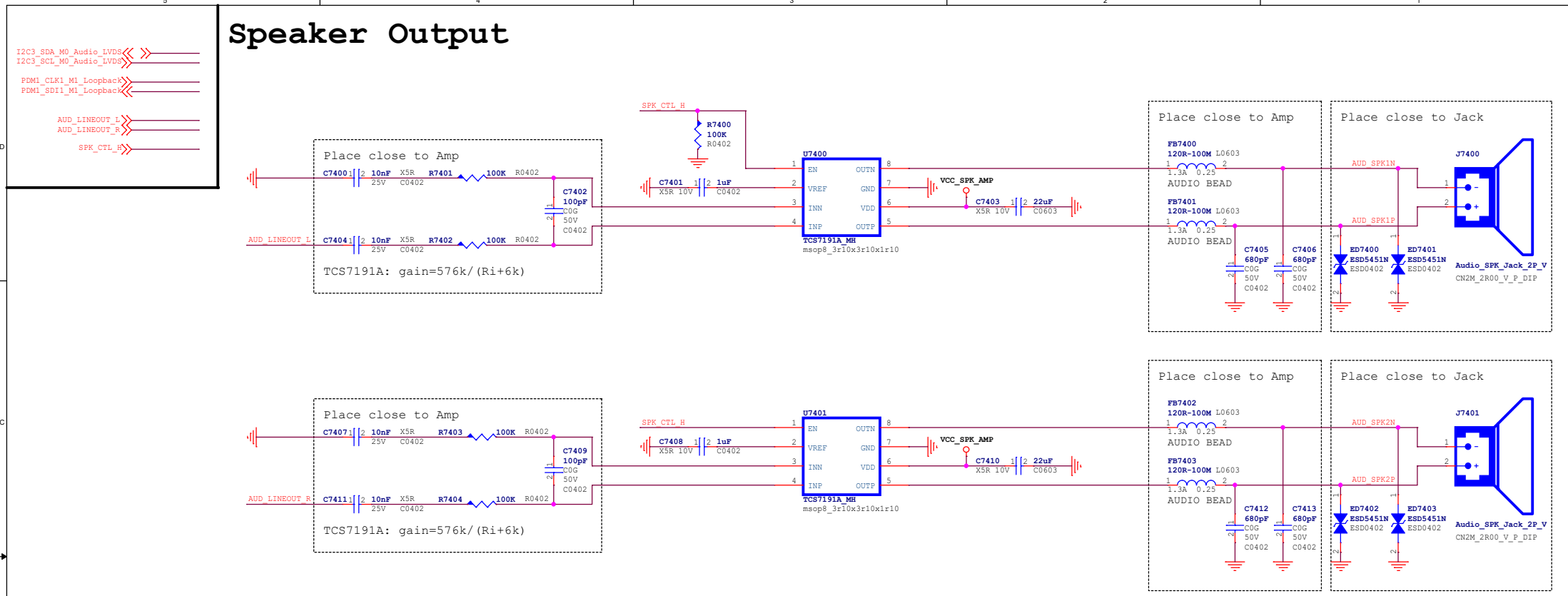
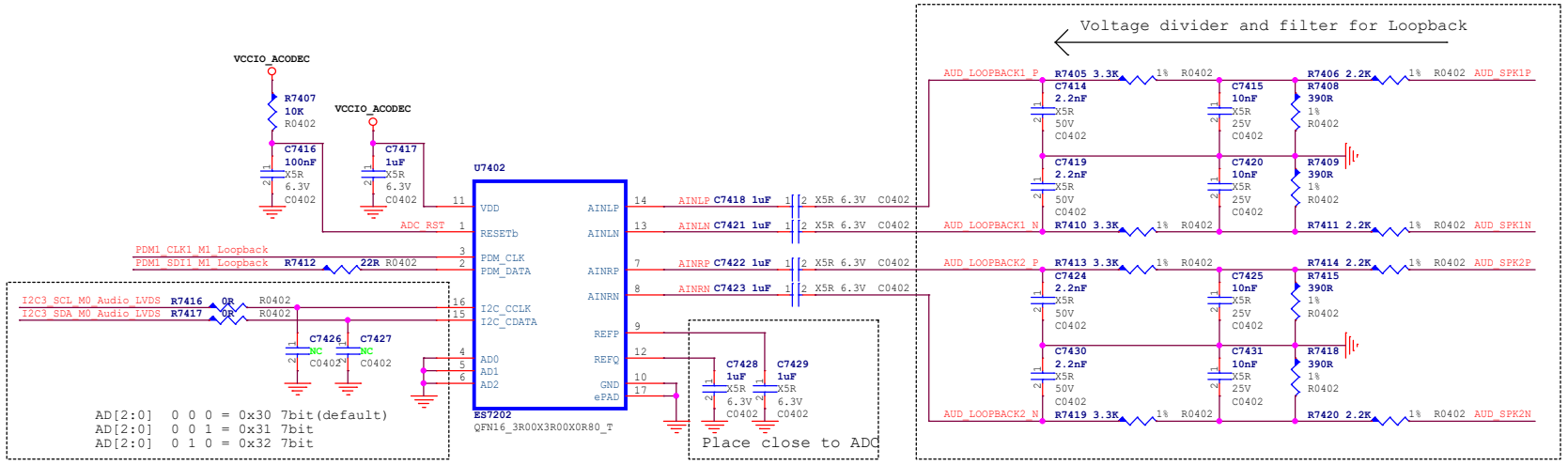
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	70.Audio-CODEC(ES8388)				
Date:	Thursday, May 30, 2024		Rev:	V1.1	
Designed by:	Wesley Huang	Reviewed by:		Sheet:	52 of 65

Speaker Output



Loopback for Dual Speakers



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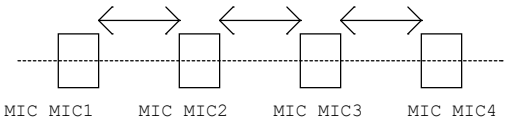
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	74.Audio-SPK LoopBack		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang / Reviewed by:	Sheet:	53 of 65

Audio-MIC Array(4xPDM-DMIC)

Option with 67.Ethernet-GEPHY_RGMII1

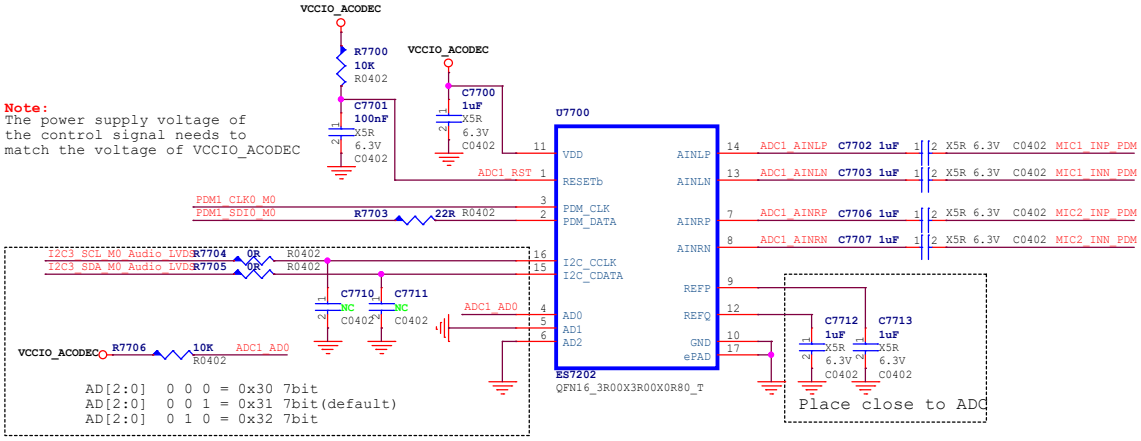
PDM1_CLK0_M0
PDM1_SDI0_M0
PDM1_SDI3_M0
I2C3_SCL_M0_Audio_LVDS
I2C3_SDA_M0_Audio_LVDS

Equal spacing arrangement; according to mic algorithm

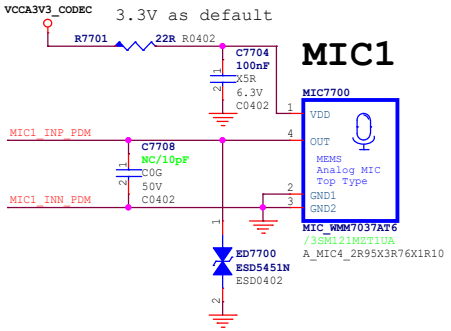


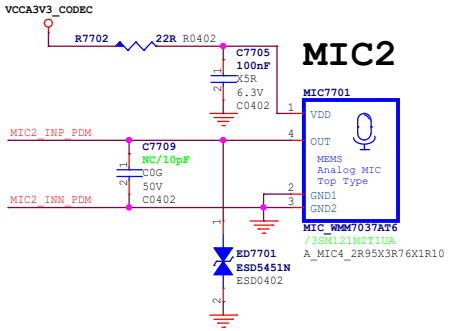
For 4MIC Array Applications

Note:
The power supply voltage of the control signal needs to match the voltage of VCCIO_ACODEC

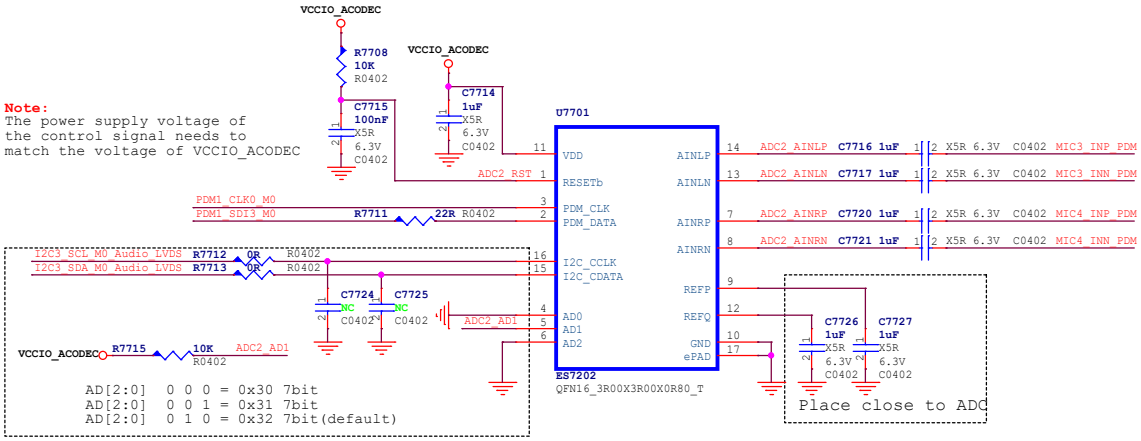


AD[2:0] 0 0 0 = 0x30 7bit
AD[2:0] 0 0 1 = 0x31 7bit(default)
AD[2:0] 0 1 0 = 0x32 7bit

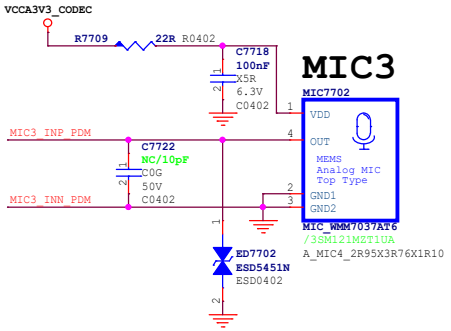


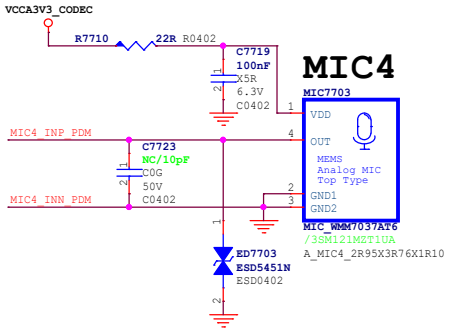


Note:
The power supply voltage of the control signal needs to match the voltage of VCCIO_ACODEC



AD[2:0] 0 0 0 = 0x30 7bit
AD[2:0] 0 0 1 = 0x31 7bit
AD[2:0] 0 1 0 = 0x32 7bit(default)





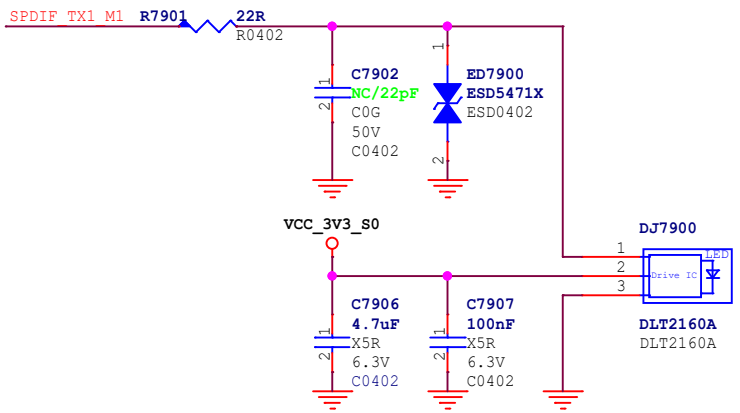
Rockchip Confidential

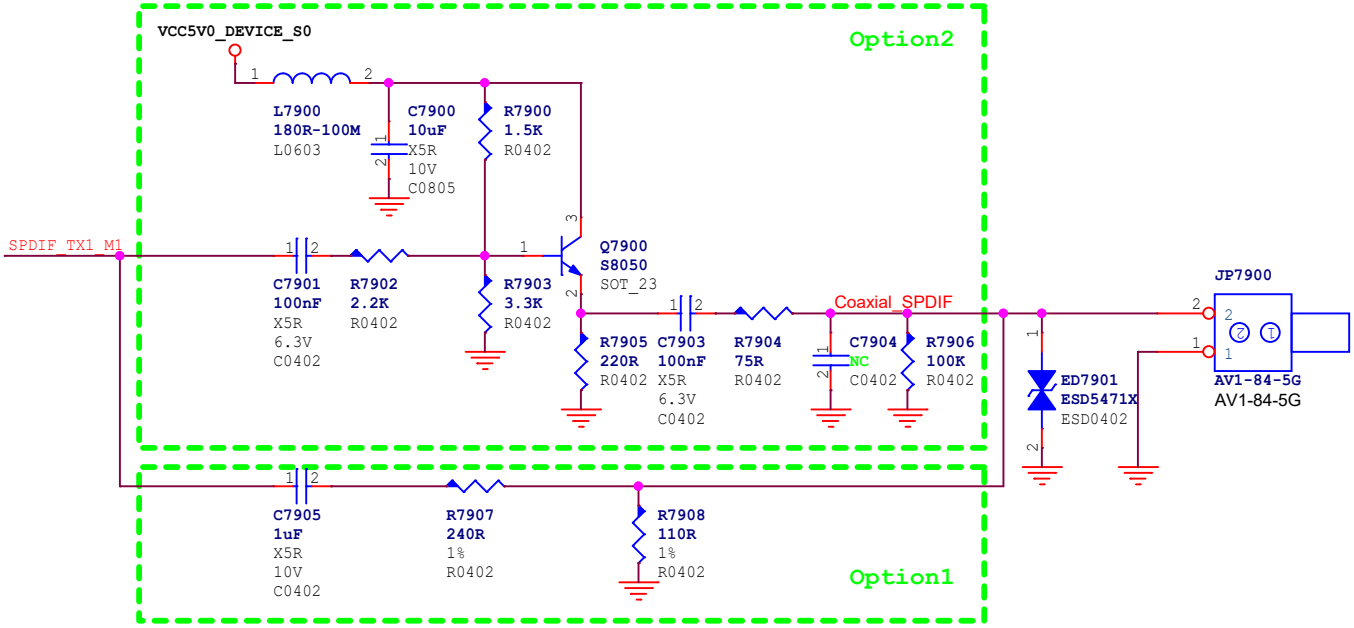
Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	77.Audio-MIC Array(Opt)				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	54 of 65

SPDIF_TX1_M1

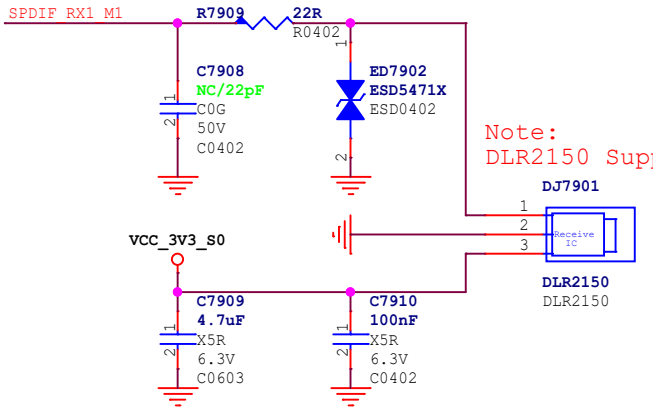
SPDIF_RX1_M1

S/PDIF_TX





S/PDIF_RX



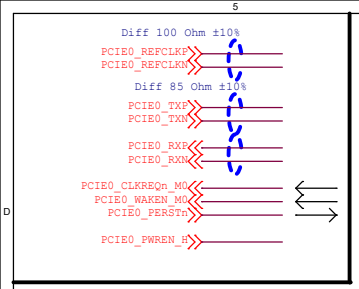
Note:
DLR2150 Support 25Mbps

Rockchip Confidential

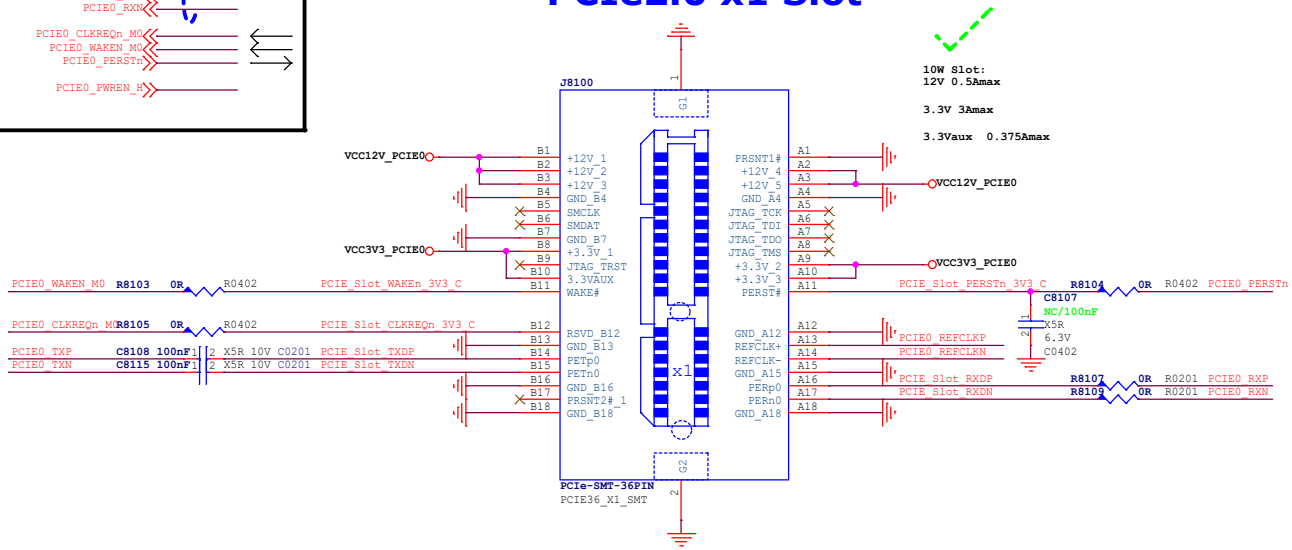
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	79.Audio-S/PDIF TX & S/PDIF RX		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:	Sheet: 55 of 65

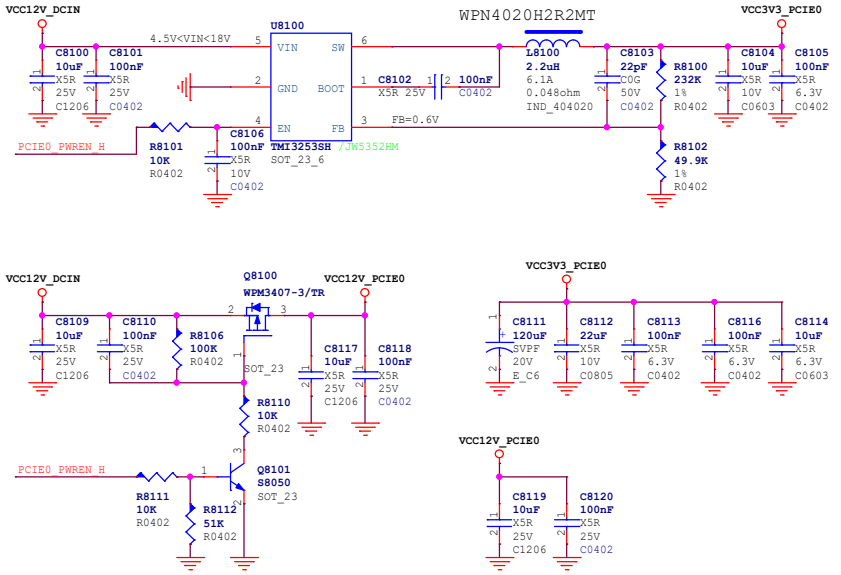
PCIe x 1Lanes (Slot is x1 compatible)

(12V DC Power Supply is required)



PCIe2.0 x1 Slot





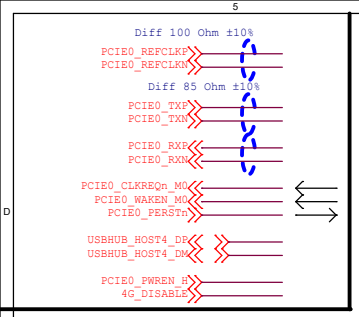
Rockchip Confidential

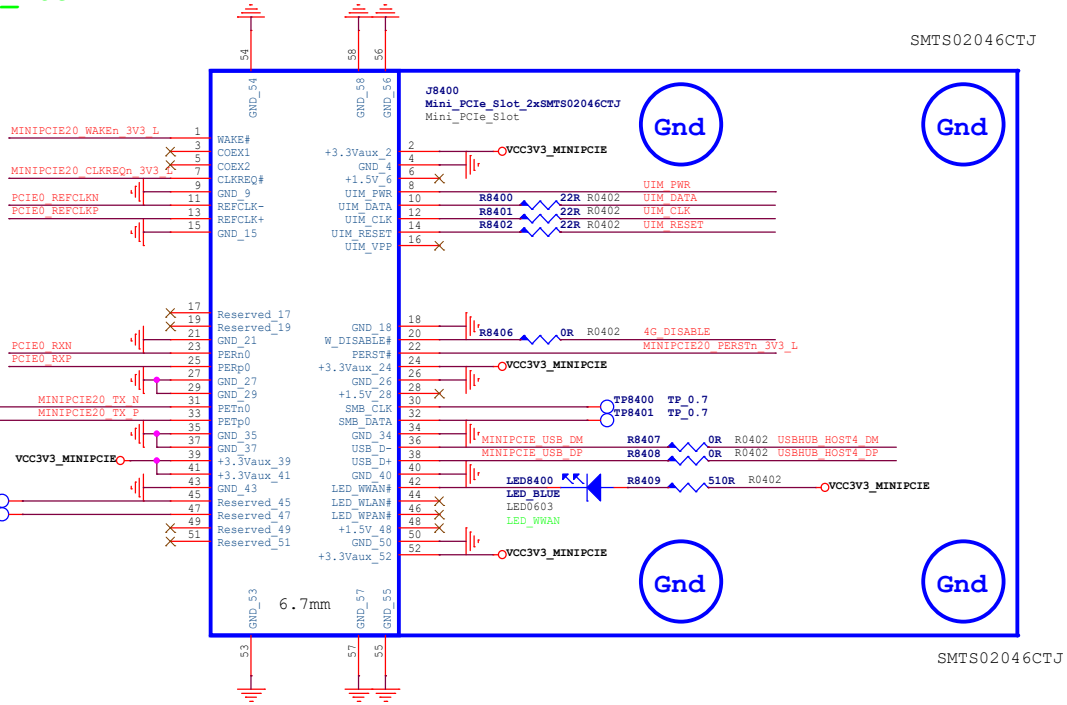
Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	81.PCIe-PCIe Slot_36P				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	56 of 65

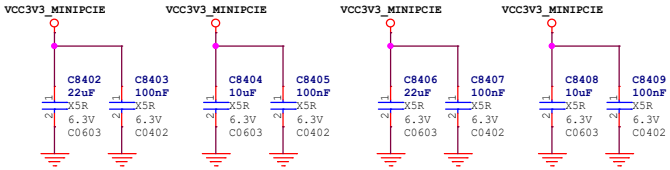
MiniPCIe Slot with 4G Function

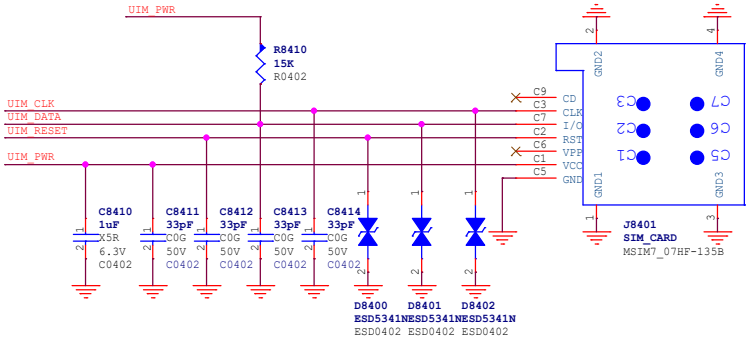
(12V DC Power Supply is required)

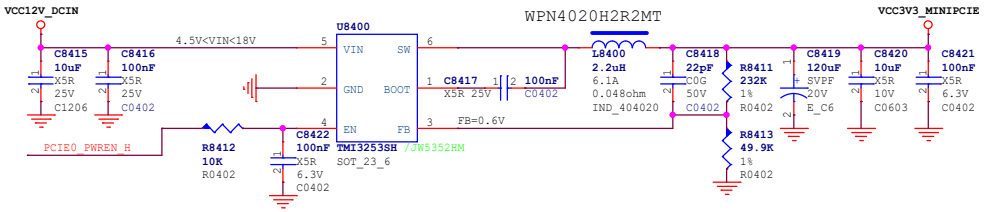
Option with 81.PCIe-PCIe Slot_36P and USBHUB_HOST4







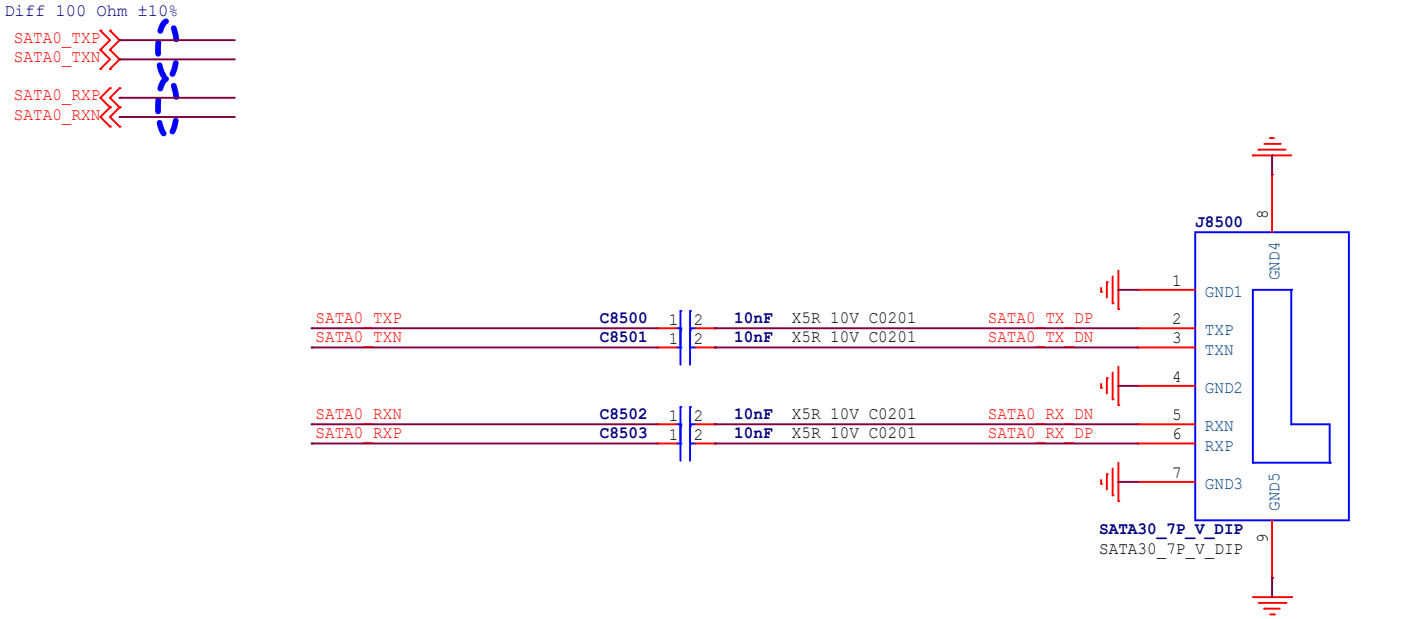




Rockchip Confidential

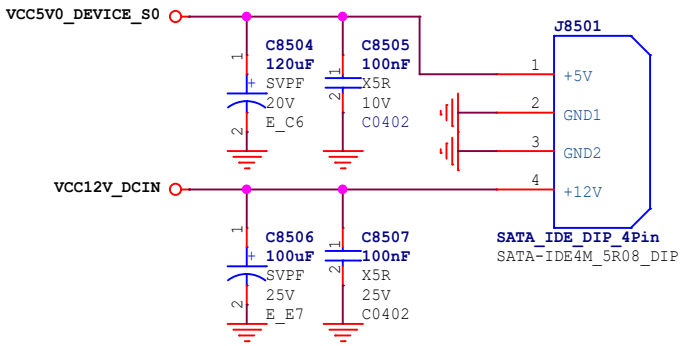
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	84.MiniPCIe Slot_with 4G(Opt)				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	57 of 65

SATA3.0 *Option with 81.PCIe-PCIe Slot_36P*



SATA_POWER

The current is estimated according to the actual number of SATA
High power switching separate power supply is recommended for more than 2

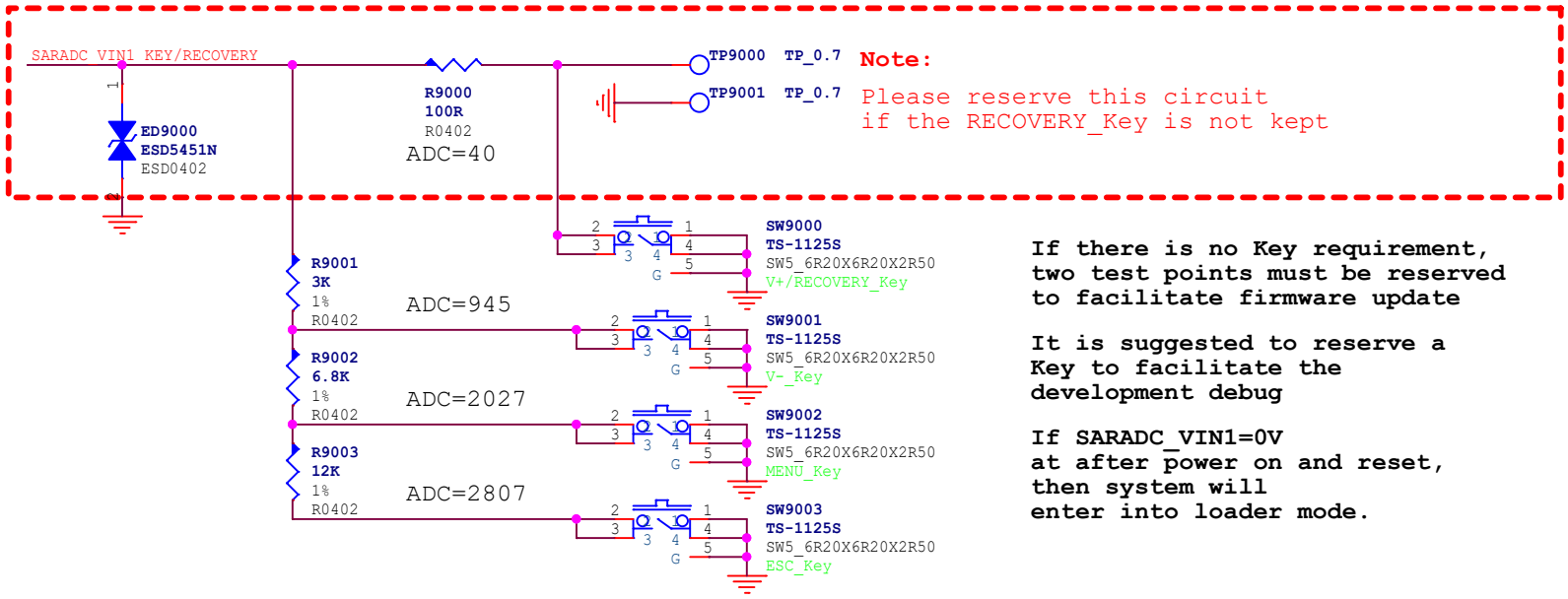


Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	85.SATA3.0 Slot_7P(Opt)		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang Reviewed by: Default	Sheet:	58 of 65

SARADC_VIN1_KEY/RECOVERY
RESET_L
PWRON_L
SARADC_VIN0_BOOT

KEY

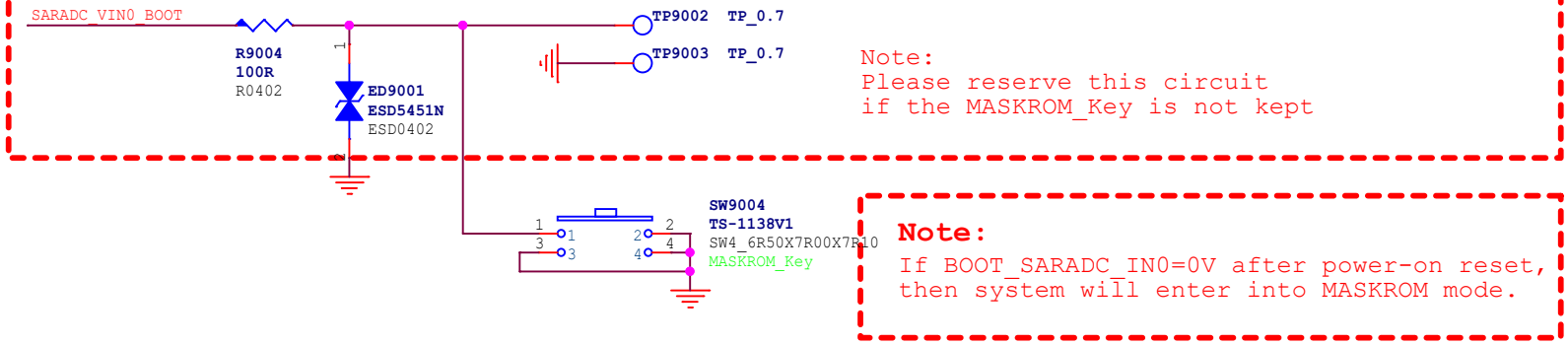


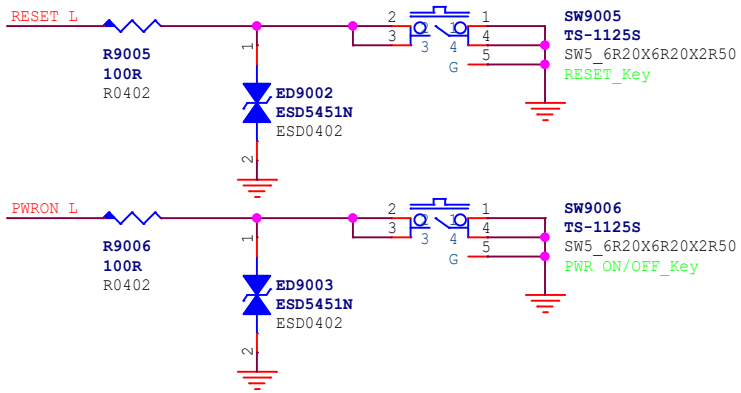
If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

If SARADC_VIN1=0V at after power on and reset, then system will enter into loader mode.

MASKROM Key





Rockchip Confidential

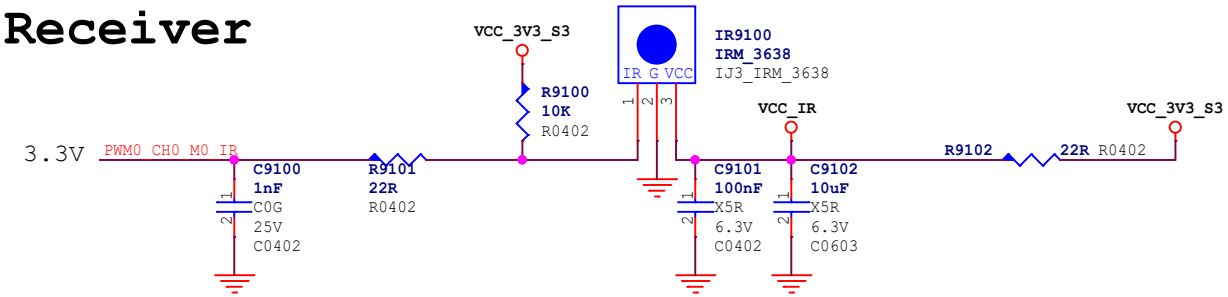
Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	90.Key-PowerON/Reset/V+/V-/etc		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang / Reviewed by:	Sheet:	59 of 65

PWM0_CH0_M0_IR

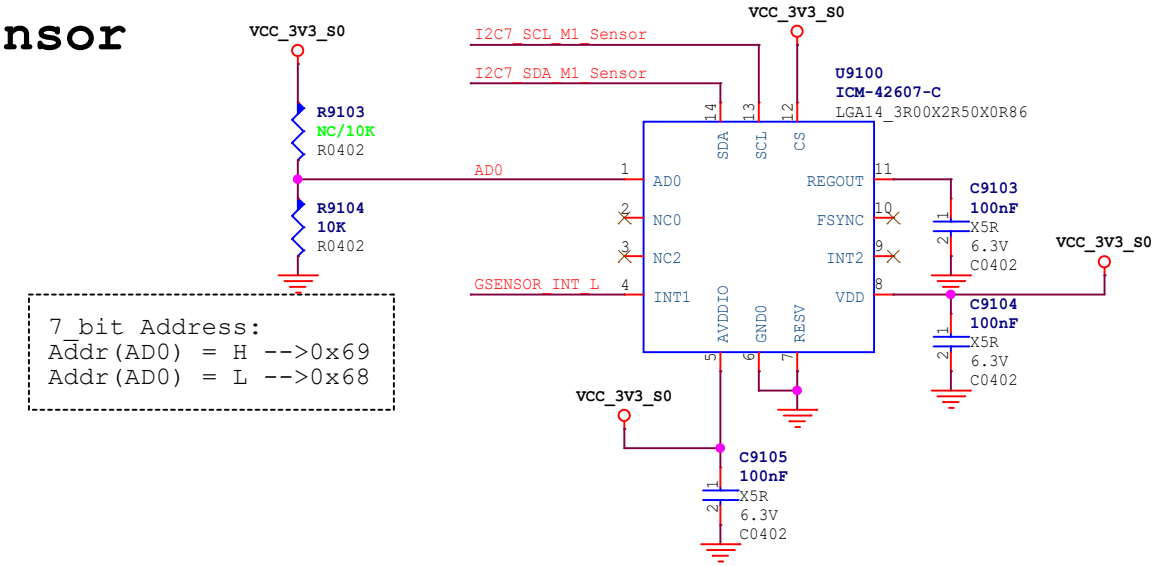
I2C7_SCL_M1_Sensor
I2C7_SDA_M1_Sensor

GSENSOR_INT_L

IR Receiver



Gyroscope+G-sensor



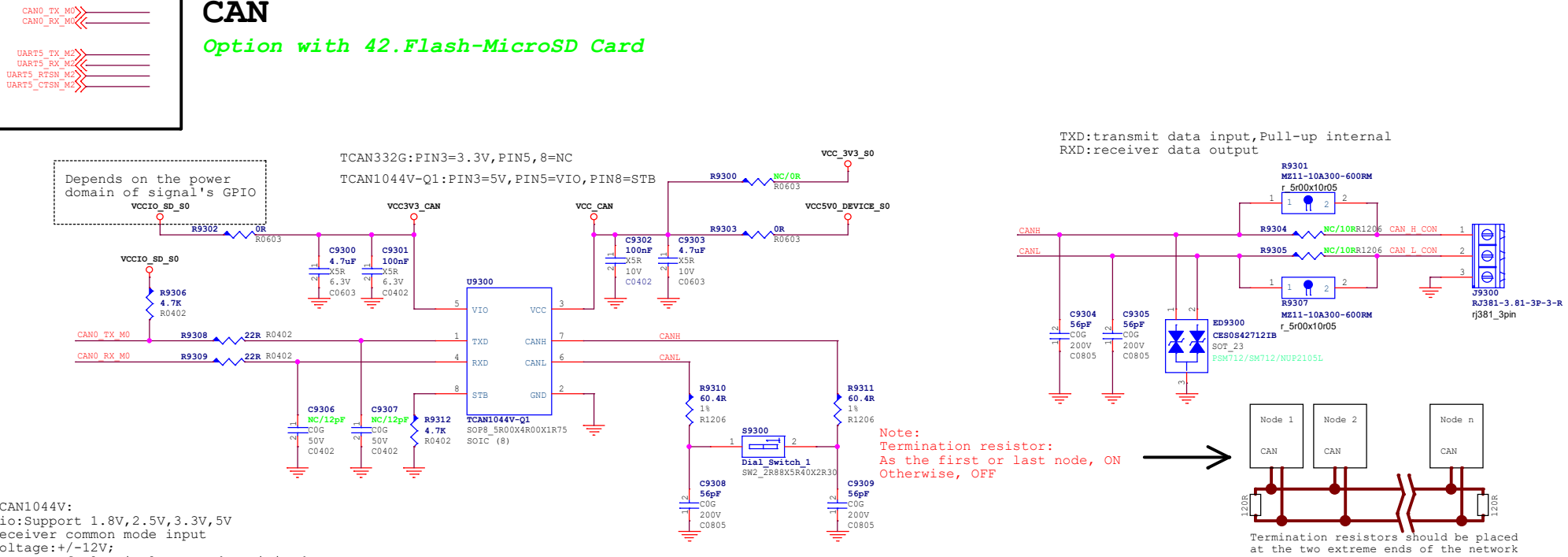

```
7_bit Address:
Addr(AD0) = H -->0x69
Addr(AD0) = L -->0x68
```

Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	91.Sensors/IR Receiver		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by: Wesley Huang	Reviewed by:	Sheet:	60 of 65

CAN

Option with 42.Flash-MicroSD Card



TCAN1044V:
Vio:Support 1.8V,2.5V,3.3V,5V
Receiver common mode input voltage:+/-12V;
Support of classical CAN and optimized CAN FD performance at 2,5,and 8 Mbps.
Temperature grade:-40 to 125

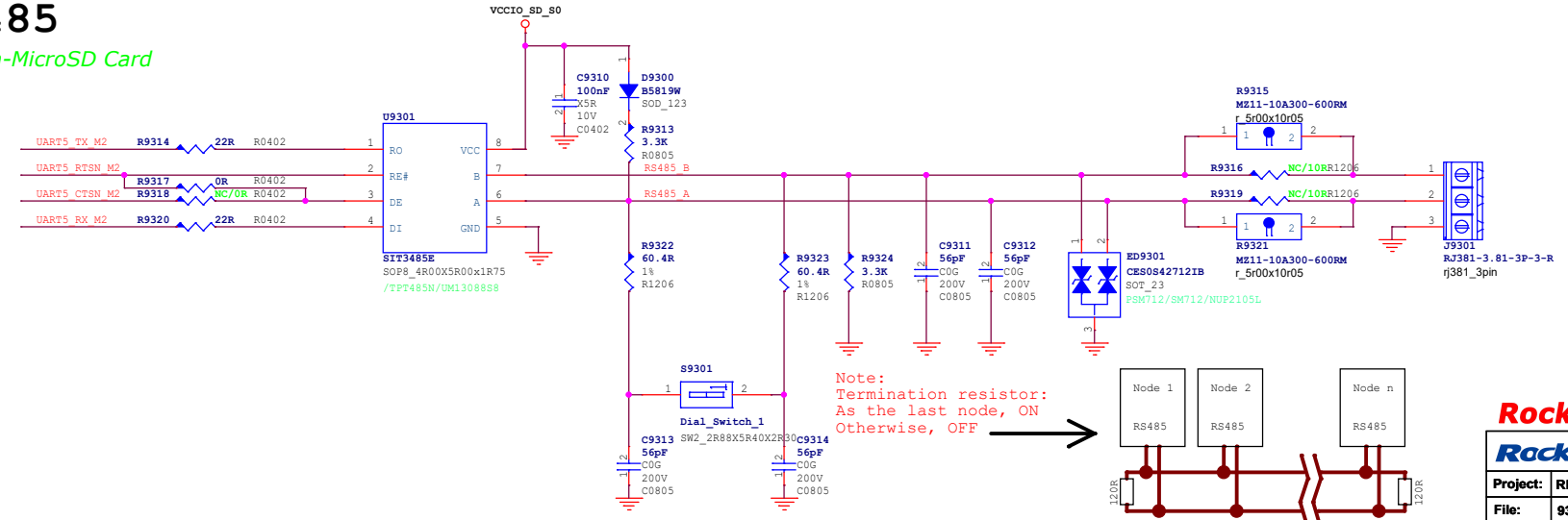
STB(Standby)
The STB pin is an input pin used for mode control of the transcervier.The STB pin can be supplied from either the system processor or from a static system voltage source,If normal mode is the only intended mode of operation then the STB pin can be tired directly to GND.

Table 5. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received See section 8.3.3.1
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

UART RS485

Option with 42.Flash-MicroSD Card



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	93.UART/CAN Port(Opt)				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	61 of 65

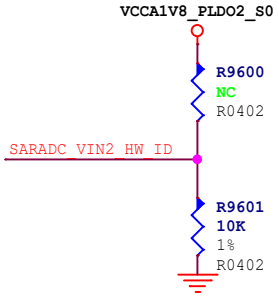
Work_LED

Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	95.LED		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang / Reviewed by:	Sheet:	62 of 65

SARADC_VIN2_HW_ID

HW_ID



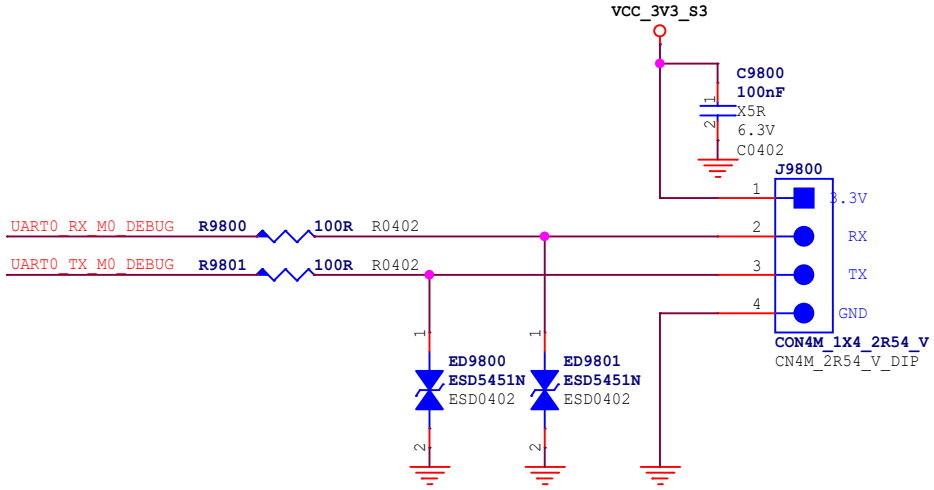
Config Table for SARADC_VIN2_HW_ID

Item	Rup	Rdown	ADC Value	VERSION
HW_ID1	NC	10K	0	HW_ID0
HW_ID2	10K	1.13K	416	RESERVE
HW_ID3	10K	2.49K	816	RESERVE
HW_ID4	10K	4.3K	1231	RESERVE
HW_ID5	10K	6.8K	1658	RESERVE
HW_ID6	10K	10K	2048	RESERVE
HW_ID7	10K	14.7K	2437	RESERVE
HW_ID8	10K	23.2K	2862	RESERVE
HW_ID9	10K	40.2K	3279	RESERVE
HW_ID10	10K	88.7K	3680	RESERVE
HW_ID11	10K	NC	4095	RESERVE

Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	96.HW_ID				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	63 of 65

UART0_RX_M0_DEBUG
UART0_TX_M0_DEBUG

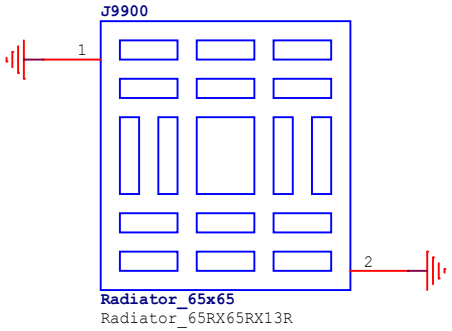
Debug UART_M0



Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	98.Debug UART		
Date:	Thursday, May 30, 2024	Rev:	V1.1
Designed by:	Wesley Huang / Reviewed by:	Sheet:	64 of 65

Heatsink

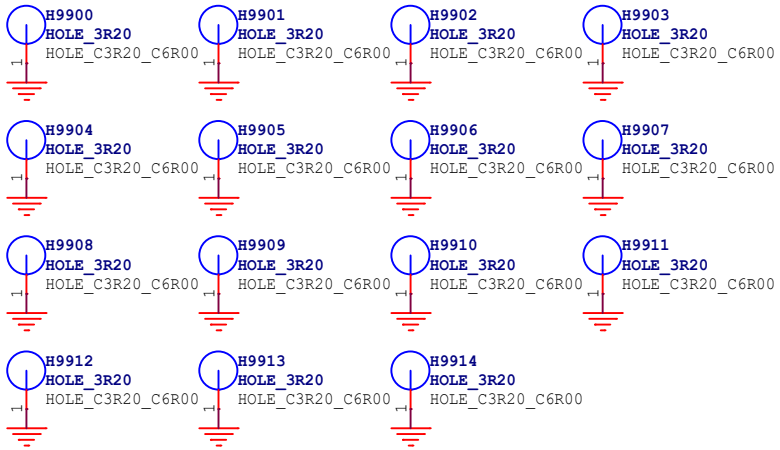


Mark

TOP Mark

BOTTOM Mark

Hole



Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	99.Mark/Hole/Heatsink				
Date:	Thursday, May 30, 2024			Rev:	V1.1
Designed by:	Wesley Huang	Reviewed by:		Sheet:	65 of 65