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Rockchip RK3576 Hardware Design Guide

(Hardware Development Center)

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Preface

Overview

This guide primarily introduces the key points and considerations for the hardware design of the RK3576 processor, aimed at assisting RK customers in shortening the product design period, enhancing product design stability, and reducing the failure rate. Follow the guide and use RK's core templates. for necessary modifications, adhere to high-speed digital circuit and RK's PCB design standards.

Chip model

This document is suitable for **RK3576**

Intended Audience

This guide is mainly intended for:

- Hardware development engineers
- Layout engineers
- Technical support engineers
- Test engineers

Revision History

This part records description of each version, and any updates of previous version are included in the latest one.

Versio n No.	Author	Revision Date	Revision Description	Remark
V1.1	Hardware Developme nt Center	2024.05.28	Initial release	

Abbreviation

缩略语包括文档中常用词组的简称：

缩写	英文解释	中文解释
ASRC	Asynchronous Sample Rate Converter	异步采样率转换器
ARM	Advanced RISC Machine	高级精简指令集计算机
CAN	Controller Area Network	控制器局域网络
CEC	Consumer Electronics Control	消费电子控制
CIF	Camera Input Format	相机并行接口
CPU	Central processing unit	中央处理器
CSI	Camera Serial Interface	相机串行接口
DC/DC	Direct current-Direct current converter	直流/直流变换器
DDR	Double Data Rate	双倍速率同步动态随机存储器
DP	DisplayPort	显示接口
DSI	Display Serial Interface	显示串行接口
DSM	Digital Signal Modulator	数字信号调制 这里特指基于数字信号调制的数字音频脉冲输出接口
EBC	E-book controller	电子书控制器
eDP	Embedded DisplayPort	嵌入式数码音视讯传输接口
eMMC	Embedded Multi Media Card	内嵌式多媒体存储卡
ESD	Electro-Static discharge	静电释放
ESR	Equivalent Series Resistance	等效电阻
FSPI	Flexible Serial Peripheral Interface	灵活串行外设接口
GPU	Graphics Processing Unit	图形处理单元
HDMI	High Definition Multimedia Interface	高清晰度多媒体接口
HPD	Hot Plug Detect	热插拔检测
I2C	Inter-Integrated Circuit	内部整合电路(两线式串行通讯总线)
I2S	Inter-IC Sound	集成电路内置音频总线
ISP	Image Signal Processing	图像信号处理
JTAG	Joint Test Action Group	联合测试行为组织定义的一种国际标准测试协议（IEEE 1149.1 兼容）
LDO	Low Drop Out Linear Regulator	低压差线性稳压器
LCDC	LCD Controller	LCD 控制器并行接口
LCM	LCD Module	LCD 显示模组

缩写	英文解释	中文解释
MAC	Media Access Control	以太网媒体接入控制器
MIPI	Mobile Industry Processor Interface	移动产业处理器接口
NPU	Neural network Processing Unit	神经网络处理器
PCB	Printed Circuit Board	印制电路板
PCIe	Peripheral Component Interconnect -express	外设组件互联标准
PCM	Pulse Code Modulation	脉冲编码调制
PDM	Pulse density modulation	脉冲密度调制
PLL	Phase-locked loop	锁相环
PMIC	Power Management IC	电源管理芯片
PMU	Power Management Unit	电源管理单元
PWM	Pulse width modulation	脉冲宽度调制
RGB	RGB color mode is a color standard in industry	RGB 色彩模式, 是工业界的一种颜色标准
GMAC	Gigabit Media Access Controller	千兆媒体访问控制器
RGMII	Reduced Gigabit Media Independent Interface	简化千兆媒体独立接口
RMII	Reduced Media Independent Interface	简化媒体独立接口
RK	Rockchip Electronics Co.,Ltd.	福州瑞芯微电子股份有限公司
SAI	Serial Audio Interface	串行音频接口 兼容 I2S、PCM、TDM 协议, 见 SAI 数字音频接口章节具体描述
SARADC	Successive approximation register Analog to digital converter	逐次逼近寄存器型模数转换器
SATA	Serial Advanced Technology Attachment	串行高级技术附件
SD Card	Secure Digital Memory Card	安全数码卡
SDIO	Secure Digital Input and Output Card	安全数字输入输出卡
SDMMC	Secure Digital Multi Media Card	安全数字多媒体存储卡
SPDIF	Sony/Philips Digital Interface Format	SONY、PHILIPS 数字音频接口
SPI	Serial Peripheral Interface	串行外设接口
TF Card	Micro SD Card(Trans-flash Card)	外置记忆卡
TSADC	Temperature sensing A / D converter	温度感应模数转换器
UART	Universal Asynchronous Receiver / Transmitter	通用异步收发传输器
VOP	Video Output Processor	视频输出处理器
USB2.0	Universal Serial Bus 2.0	通用串行总线
USB3.2 Gen1x1	Universal Serial Bus 3.2 Superspeed	通用串行总线

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1 System Introduction

1.1 Overview

RK3576 is a high performance, low power processor for ARM-based PC and Edge Computing device, personal mobile internet device and other digital multimedia applications, and integrates quad-core Cortex-A72 and quad-core Cortex-A53 with separately NEON coprocessor.

RK3576 video decoder supports H.265, VP9, AV1 and AVS2 etc. up to 4K@120fps and H.264 up to 4k@60fps, and video encoder supports H.264 and H.265 up to 4k@60fps, high-quality JPEG encoder/decoder supports up to 4k@60fps.

Embedded 3D GPU makes RK3576 completely compatible with OpenGL ES 1.1/2.0/3.2, OpenCL 2.0 and Vulkan 1.1. Dedicated 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

RK3576 introduces a new generation 16-Megapixel ISP(Image Signal Processor). It implements a lot of algorithm accelerators, such as HDR, 3A, CAC, 3DNR, 2DNR, Sharpening, Dehaze, Enhance, Debayer, Small Angle Lens-Distortion Correction and so on.

The build-in NPU supports INT4/INT8/INT16/FP16/BF16/TF32 hybrid operation, with a computing power of up to 6 TOPS. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RK3576 supports high-performance dual channel external memory interface(LPDDR4/LPDDR4X/LPDDR5) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

1.2 Chip Block Diagram

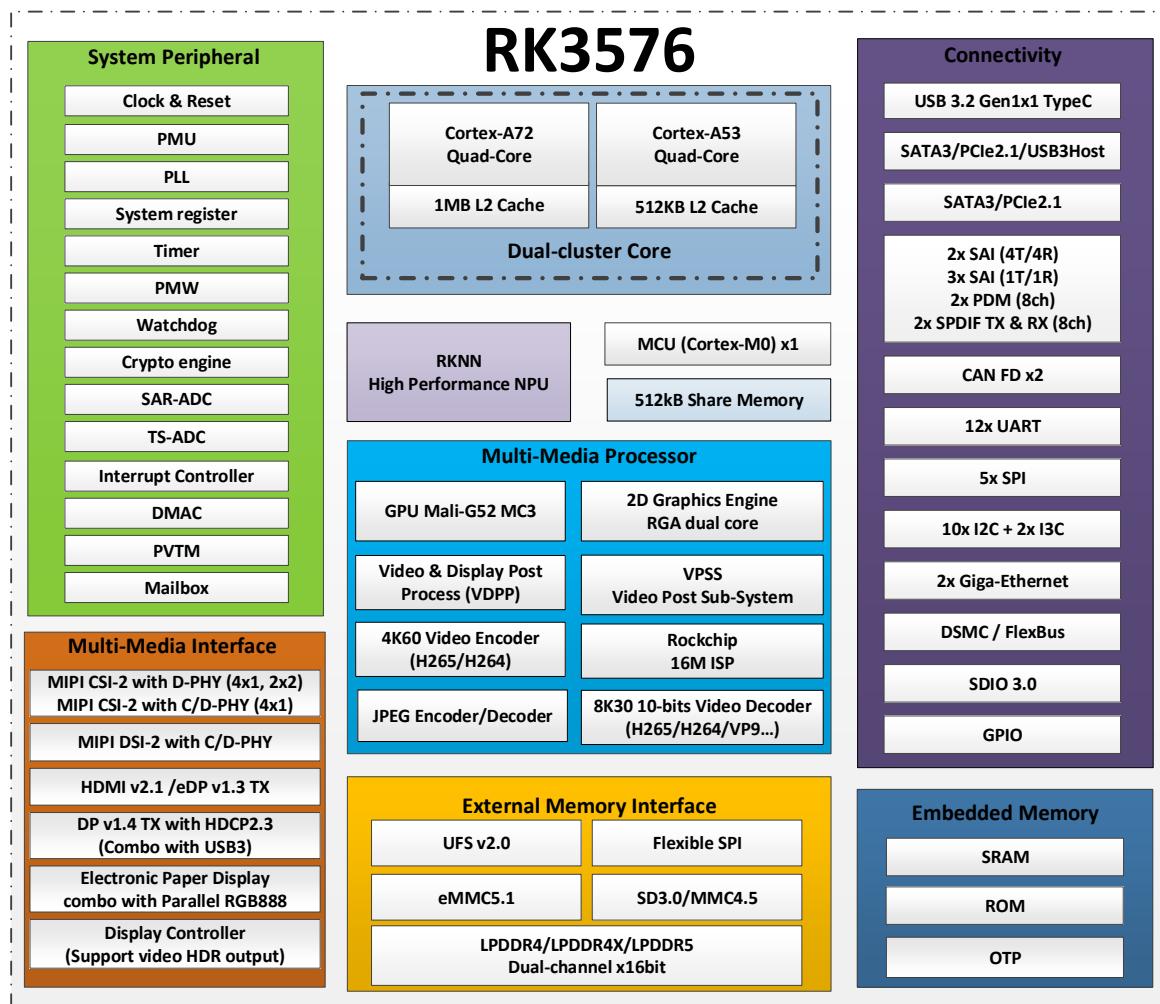


Figure 1-1 RK3576 block diagram

1.3 Application Block Diagram

1.3.1 RK3576 EVB Block Diagram

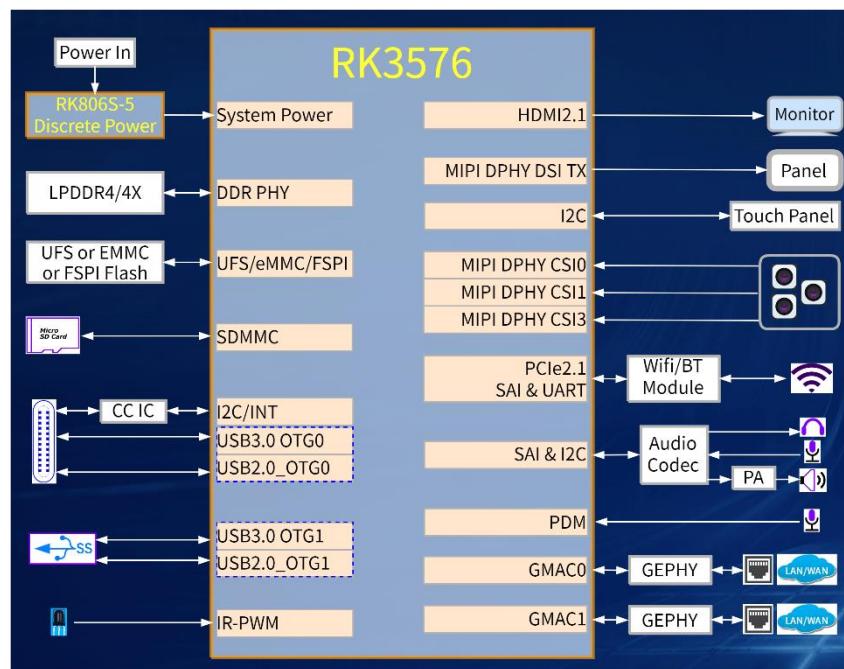


Figure 1-2 EVB Block Diagram

1.3.2 RK3576 Intelligent NVR Application Block Diagram

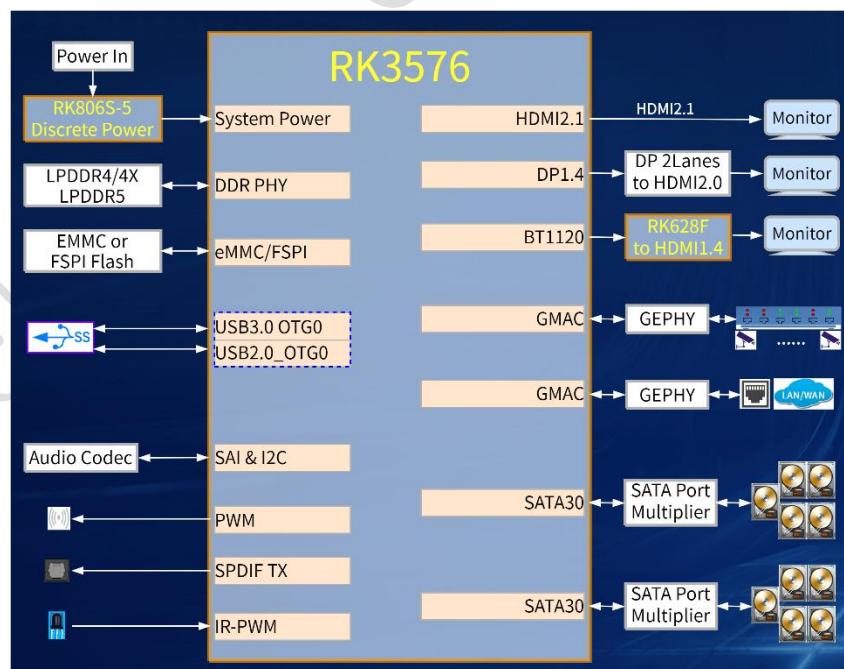


Figure 1-3 Intelligent NVR Application Block Diagram

The above are examples of the RK3576 application scheme. For more details, please refer to the reference design schematic released by RK.

2 Schematic Diagram Design Suggestions

2.1 Minimum System Design

2.1.1 Clock Circuit

The internal oscillator circuit of the RK3576 chip, together with the external 24MHz crystal, forms the system clock. The XOUT_24M network must be connected with a 22ohm resistor to limit the current and prevent overdriving. The 510Kohm resistor between XOUT_24M and Xin_24M networks should not be modified at will.

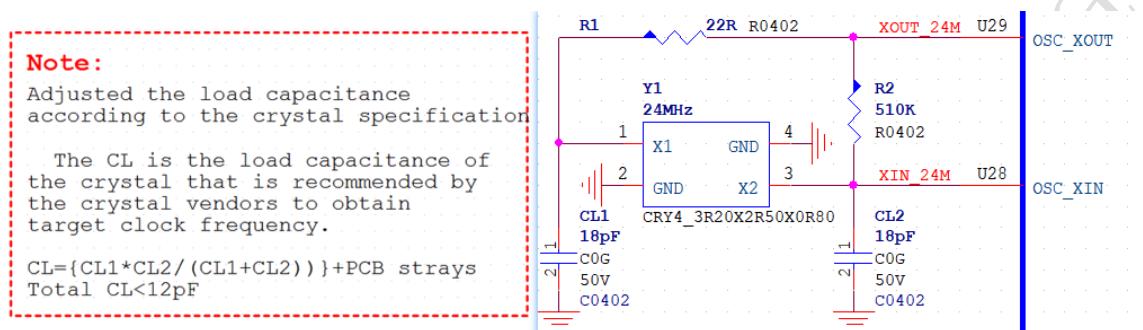


Figure 2-1 RK3576 Crystal Connection and Device Parameters



NOTE

Note 1: The CL value of crystal selected should no more than 12pF.

Note 2: The crystal external capacitors CL1 and CL2 should be selected according to the actual crystal's CL value requirements, and the frequency tolerance at room temperature should be within 20ppm;

The CL1 and CL2 used by RK is 18pF which is not a general value, and the capacitor material is recommended to use COG or NPO;

It is recommended to use a 4-pin surface-mounted crystal, with two GND pins fully connected to the PCB ground to enhance the clock's ability to resist ESD interference.

The RK3576 supports the active crystal oscillator input scheme:

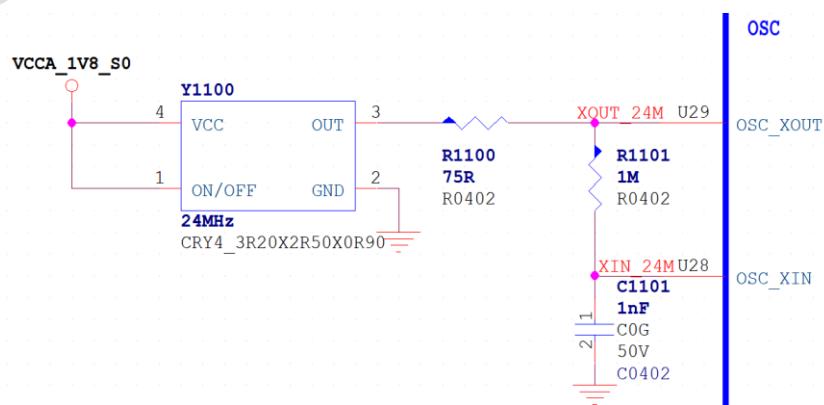


Figure 2-2 The Connection Method and Device Parameters of RK3576 Active Crystal Oscillator

For scenarios that require clock sources from the same source, the active crystal oscillator can be replaced with a dual-channel clock generator. One clock signal of the clock generator is input to RK3576, and the other one is input to other chips.



NOTE

Note 1: R1100 maybe affect the duty ratio. Different active crystal oscillators may have different parameters for this. The adjustment method is as follows: (a) On the software, sets 24M CLK from REF_CLK0_OUT (Pin V29) foot BAPASS output, and uses an oscilloscope to test the 24M CLK output from this foot. (b) If the 24M CLK output from Pin V29 is not 50% duty ratio, adjust the R1100 parameter to make the duty ratio as close to 50% as possible; (c) If the selected active 24M crystal oscillator output CLK voltage is low (not reaching 1.8V, such as 0.8V), it may not be possible to achieve a 50% duty ratio by adjusting the R1100 parameter.

Note 2: Active crystal oscillator clock requirements: Level 1.35V-1.8V, duty ratio 50%, frequency offset 20ppm.

When RK3576 in standby mode, can choose to switch the working clock source to the clock provided by the PMU_PVTM module or an externally input 32.768KHz clock, and turn off the OSC oscillation circuit, which can achieve better standby power consumption. At this time, only the IO interrupt wake-up of the PMUIO0 and PMUIO1 power domains is supported. If the required wake-up source is related to the 24MHz clock, then the 24MHz clock cannot be turned off.

The clock oscillation loop integrated in the PVTM (Process-Voltage-Temperature Monitor) module can generate a clock, the frequency of which is determined by the delay unit of the clock oscillation loop circuit. The generated clock can be used as the clock source for the chip's standby mode; when using an externally input 32.768KHz clock as the RK3576 chip's sleep clock, the optimal chip standby power consumption can be achieved, and the PVTM module can also be turned off at this time.

The externally input 32.768KHz clock can be obtained from an external RTC clock source. The 32.768KHz clock input pin of the RK3576 is shown in the following figure:

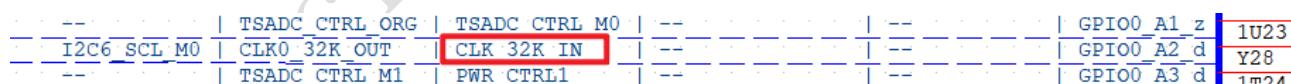


Figure 2-3 RK3576 32.768KHz standby clock input pin

External 32.768kHz RTC clock parameters as follow:

Table 2-1 RK3576 32.768KHz clock requirement

Parameter	Spec.			Description
	Min	Max	Unit	
Frequency	32.768000		kHz	
Frequency bias	+/-30		ppm	
Clock amplitude	0.7*VDD	VDD	V	VDD: PMUIO0 power voltage
Duty ratio	45	55	%	

**NOTE**

Note1: When using this function, the IOMUX of the pin must be set to CLK32K_IN function, and the input amplitude must meet the power supply requirements of the PMUIO0 Domain.

Note2: For chips with open-drain outputs, such as RTC chips, it is important to ensure that the internal pull-down of the GPIO where CLK_32K_IN is located is disabled.

RK3576 can provide working clocks to external devices:

- REF_CLK0_OUT/REF_CLK1_OUT/REF_CLK2_OUT: Reserved clock output pins, selected according to actual requirements, supporting the following frequencies: 12MHz, 24MHz, 25MHz, 26MHz, 27MHz, 37.125MHz, 74.25MHz, 10MHz, 20MHz, 40MHz, 50MHz, 58.5MHz, 100MHz.
- CLK0_32K_OUT/CLK1_32K_OUT: 32.768KHz clock output, can be provided to devices such as Wi-Fi, BT, PCIe as working clocks or sleep clocks (if the system 24MHz oscillator needs to be turned off in standby mode, the clock cannot be output).
- ETH0_CLK_25M_OUT/ETH1_CLK_25M_OUT: 25MHz clock output, can be provided to Ethernet PHY and other devices as working clocks.
- CAM_CLK0_OUT/CAM_CLK1_OUT/CAM_CLK2_OUT: Default 24MHz clock output, can be provided to Camera and other devices as working clocks; can also be divided by PLL to obtain frequencies of 27MHz, 37.125MHz, 74.25MHz, each clock can output different frequencies.
- VI_CIF_CLKOUT: Default 24MHz clock output, can be provided to Camera and other devices as working clocks; can also be divided by PLL to obtain frequencies of 27MHz, 37.125MHz, 74.25MHz.

**NOTE**

Note1: The IO Domain of the clocks mentioned above must match the IO voltage level of the external device. If they do not match, voltage level conversion circuits must be added.

Note2: Please evaluate whether the clock requirements of the external devices can be met based on their specific needs.

2.1.2 Reset/Watchdog/TSADC Circuit

The hardware reset of the RK3576 chip is initiated through Pin W28 (NPOR) input, which must be controlled externally, and it is active low. To ensure the stability and normal operation of the chip, the required minimum reset time is 100 cycles of the 24MHz master clock, which is at least 4us.

Pin W28 (NPOR) requires an additional 100nF capacitor to eliminate jitter on the reset signal, enhance anti-interference capability, and prevent abnormal system resets caused by false triggering.

The pull-up power supply of the RESET_L network must be consistent with the IO power domain where the NPOR pin is located (PMUIO0_VCC1V8).

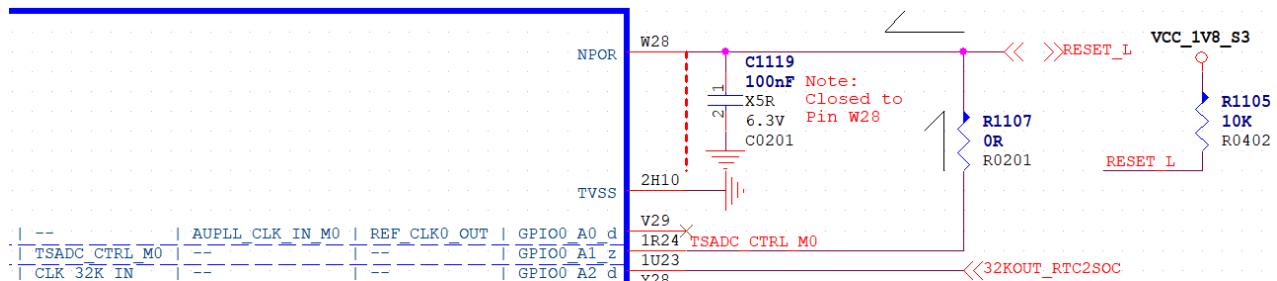


Figure 2-4 RK3576 Reset Input

The RK3576 chip internally integrates a Watchdog Timer, which can output a low level through the TSADC_CTRL_M0 pin to perform a hardware reset of the RK3576 when a reset signal is generated.

The RK3576 chip internally integrates a 6 channels TSADC (Temperature-Sensor ADC) module. When the internal temperature of the chip exceeds the threshold, the internal TSADC_SHUT signal is sent to the CRU module to reset the RK3576 chip. Simultaneously, a low level can be output through the TSADC_CTRL_M0 pin to perform a hardware reset of the RK3576. As shown in Figure 2-3, the TSADC_CTRL_M0 network is connected to the RESET_L network.

RK3576 reset signal path as follow:

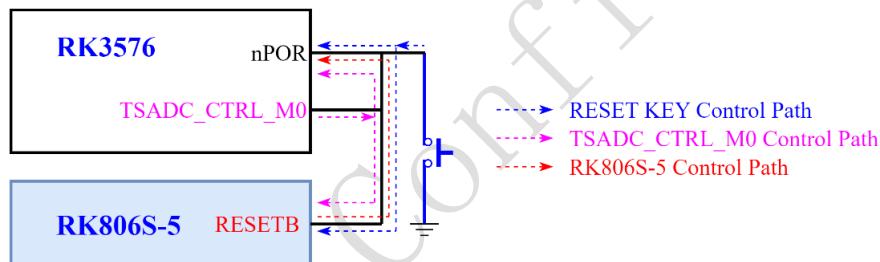


Figure 2-5 RK3576 Reset Signal Path

Upon the initial power-up, after all the power supplies have been energized, the RESETB pin of the RK806S-5 will continuously output a low level until the set delay time has elapsed and then it will stop. Since there is a pull-up resistor externally on the RESET_L, the RESET_L network will jump to a high level, thus completing the power-up reset process. When the RK806S-5 is in operation or sleep mode, if the RESETB pin is pulled low, the RK806S-5 will also restart, and the power-up sequence for the restart will be the same as the first power-up.

Upon the initial power-up, after all power supplies have stabilized, the RESETB pin of the RK806S-5 will continuously output a low level. It will remain in this state until the set delay time elapses. Due to the external pull-up resistor on the RESET_L, the RESET_L network transitions to a high level, completing the power-up reset process. When the RK806S-5 is in working or sleep mode, if the RESETB pin is pulled low, the RK806S-5 will also reboot, and the power-up sequence will be identical to the initial power-up.



NOTE

If an external watchdog circuit is used and its output is connected to the TSADC_CTRL_M0 pin, it is required to select a watchdog chip with open-drain output.

2.1.3 PMU Unit Circuit

To meet the low power requirements, RK3576 has a PMU (Power Management Unit) to control and manage the internal power of the chip. This module supports IO control of peripheral power circuits by internal registers or the PMUIO power domain, enabling power supply and shutdown of other functional modules. It also supports IO interrupt wake-up, thereby realizing the standby and wake-up functions of the chip.

2.1.4 System Booting Order

The RK3576 chip supports multiple booting methods. After the chip reset, the integrated boot code can boot through the following interface devices. The specific boot order can be selected according to the actual application requirements (see the "Boot Order Selection" description below).

- Serial Flash(FSPI0、FSPI1_M0、FSPI1_M1)
- eMMC
- UFS
- SDMMC0 Card

If there is no boot code in the above devices, the system code can be downloaded through the USB2.0 OTG0 interface USB2_OTG0_DP/DM signals. Additionally, firmware can be burned from the USB 3.2 Gen1x1 OTG0 interface's USB3_OTG0_SSRX1P/N and USB3_OTG0_SSTX1P/N signals. Please note that if USB3.0 firmware upgrade and 2Lane DP support are required, the USB3.2 Gen1x1 OTG0+DP 2Lane (Swap ON) scheme must be adopted.

Boot Order Selection:

The boot order of the RK3576 Boot can be set via the SARADC_IN0_BOOT Pin (Pin A25), booting from different peripherals. On the hardware to set different pull-up and pull-down resistor values, configuring Config1-Config11, a total of 11 modes of peripheral boot order. The corresponding configuration should be selected according to the actual application requirements.

For example, if eMMC booting is the default choice, Config10 or Config11 mode can be selected. If UFS booting is the default choice, Config7 or Config8 mode can be selected.

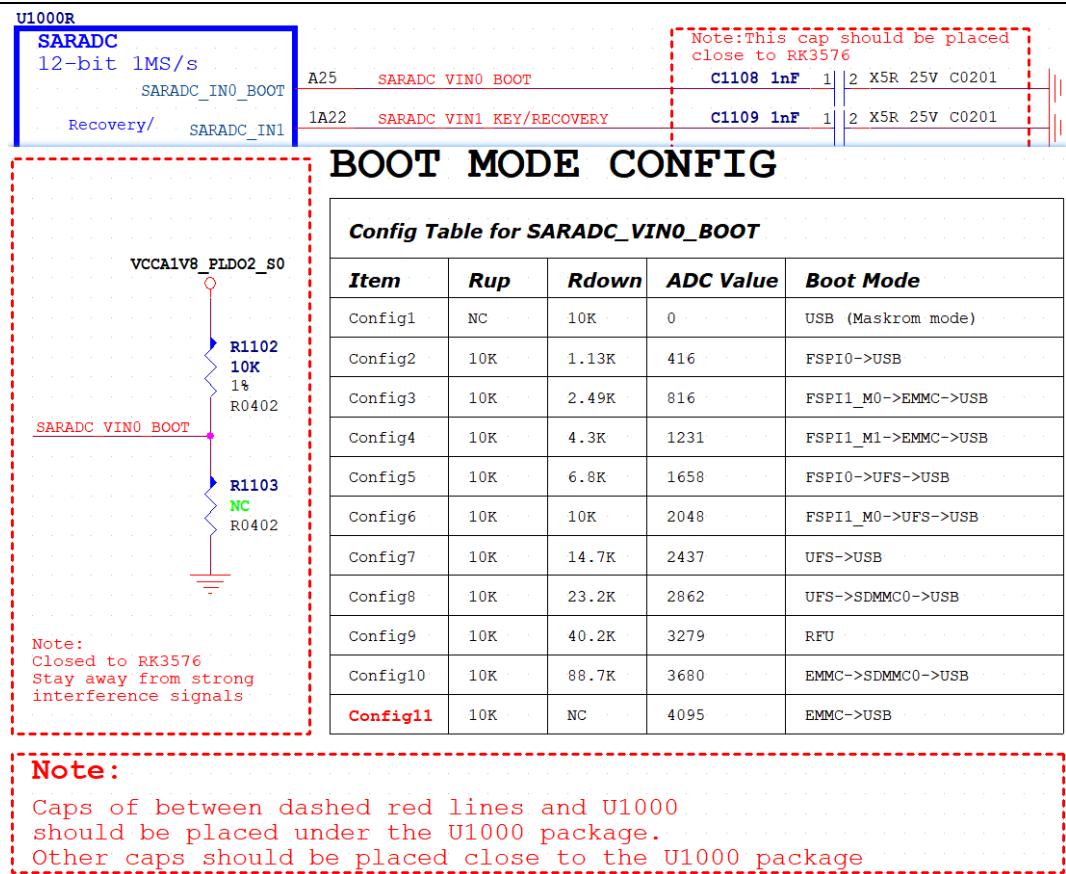


Figure 2-6 Boot Order Selection

According to the Config1 setting, shorting SARADC_IN0_BOOT to ground can set the device into Maskrom state. Earlier RK chips did not have the SARADC_IN0_BOOT function, so entering Maskrom required shorting EMMC_CLK/DATA. However, RK3576 supports the SARADC_IN0_BOOT function, it's don't need to short EMMC_CLK/DATA to enter Maskrom.

SARADC_IN1 is used for grounding to enter Recovery mode, while other SARADC pins can be configured according to application requirements.



NOTE

Note1: SARADC_IN0_BOOT is dedicated for BOOT configuration and cannot be used for other functions.

Note2: RK3576 does not support PCIe BOOT. If there is a requirement to boot from an SSD hard drive connected via the PCIe interface, it is necessary to connect an SPI FLASH to the FSPI interface. During booting, the code in the SPI FLASH first initializes the PCIe driver, then loads the system from the SSD, thereby completing the boot process.

2.1.5 System Initialization Configuration Signals

In the RK3576, there's a crucial signal that affects the system's boot configuration, which needs to be configured before powering up and kept stable:

- SDMMC0_DETIN pin (Pin 1U21): Determines whether the VCCIO1 power domain is configured as SDMMC0 or JTAG functionality. After system reset, the chip configures the default startup functionality

of the corresponding module based on the input level of this pin. The Pin 1U21 pin needs to have a 1nF capacitor added to eliminate jitter on the reset signal, enhancing noise immunity.

The JTAG functionality of RK3576 is multiplexed with SDMMC0 functionality, and the functionality is switched through the SDMMC0_DETN pin. Therefore, this pin also needs to be configured before power-up. Otherwise, the absence of JTAG functionality output will affect debugging during the boot stage, while the absence of SDMMC0 output will affect the SDMMC0 boot functionality.

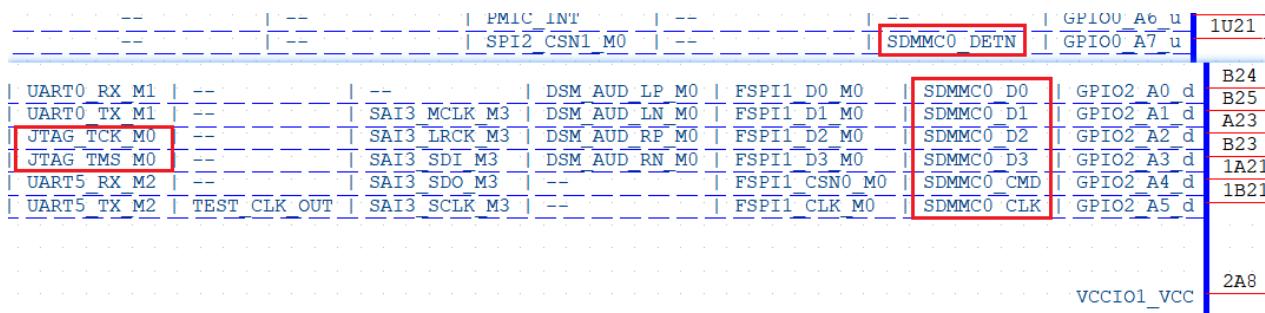


Figure 2-7 RK3576 SDMMC0_DETN pin and SDMMC0/JTAG multiplexed pins

- When this pin is detected as a high level, the corresponding IO switches to JTAG functionality.
- When it's detected as a low level (typically pulled low when an SD card is inserted, unless special handling is needed), the corresponding IO switches to SDMMC0 functionality.
- After the system boots up, it can be switched to be controlled by registers, freeing up this pin.
- For easy reference, the configuration status and functionality of this pin are described in the following table:

Table 2-2 Description of RK3576 System Initialization Configuration Signals

Signal Name	Internal Pull-up/down Configuration	Description
SDMMC0_DETN	Pull-up	SDMMC0/JTAG pin multiplex selection control signal: 0: Recognized as SD card insertion, SDMMC0/JTAG pin multiplexed as SDMMC0 functionality; 1: Not recognized as SD card insertion, SDMMC0/JTAG pin multiplexed as JTAG functionality (Default)

2.1.6 JTAG and UART Debug Circuit

2.1.6.1 RK3576 JTAG Circuit

The JTAG interface of the RK3576 chip conforms to the IEEE1149.1 standard, allowing PC to connect to a DSTREAM emulator via SWD mode (two-wire mode) for debugging the ARM Core inside the chip.

The signal description of the JTAG interface is as follows:

Table 2-3 RK3576 JTAG Debug Interface Signals

Signal name	Description
JTAG_TCK_M0/M1	SWD mode clock input

Signal name	Description
JTAG_TMS_M0/M1	SWD mode data input/output

The JTAG of RK3576 has 2 multiplexed pins. Among them, JTAG_TCK_M0/JTAG_TMS_M0 is located in the VCCIO1 domain and shares IOMUX with SDMMC0. JTAG_TCK_M1/JTAG_TMS_M1 is located in the PMUIO1 domain and shares IOMUX with UART Debug—UART0 M0. The IOMUX sharing situation is shown in the diagram below:

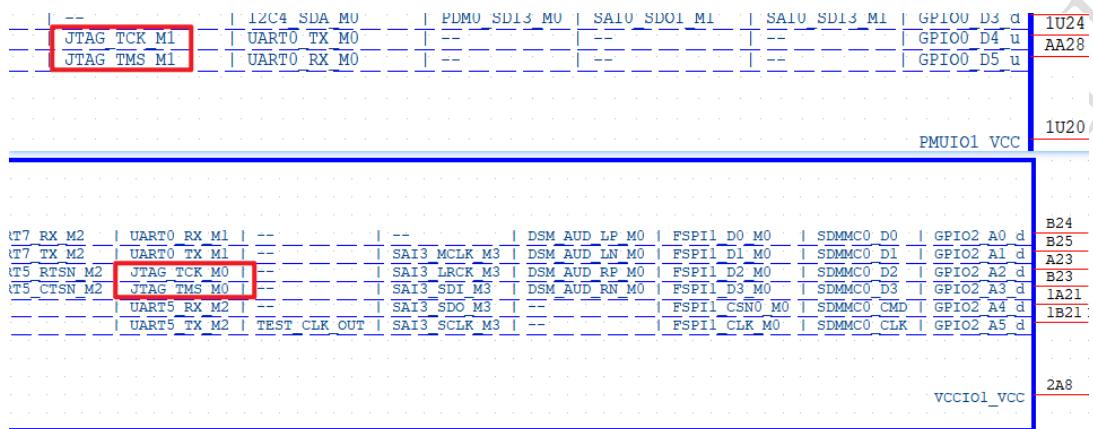


Figure 2-8 RK3576 JTAG Signals

Notes on JTAG application:

- (1) **JTAG_TCK_M0/JTAG_TMS_M0:** If JTAG_M0 is used for JTAG Debug function, it is necessary to ensure that the SDMMC0_DETn pin is at a high level during the boot stage when connecting to the emulator. Otherwise, JTAG_M0 cannot enter JTAG debug mode. The configuration is described in the previous section. After the system boots up, it will switch to be controlled by registers.
- (2) **JTAG_TCK_M1/JTAG_TMS_M1:** JTAG_M1 is multiplexed with UART0_M0. In actual projects, it is recommended to reserve 2.54mm pin headers or test points for Pin 1U24 (JTAG_TCK_M1/UART0_TX_M0) and Pin AA28 (JTAG_TMS_M1/UART0_RX_M0) for JTAG Debug or UART Debug. The circuit for JTAG is shown in the diagram below, the series 100ohm resistors must not be omitted, and TVS diodes should be added to enhance electrostatic surge capability, preventing damage to chip pins during development.

Note: IO level must be matched.

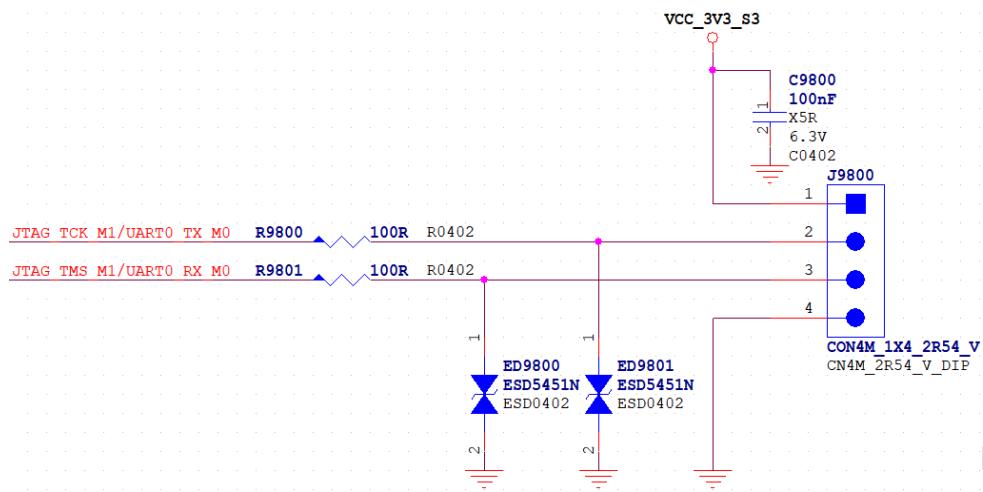


Figure 2-9 RK3576 JTAG Connection Diagram

2.1.6.2 RK3576 UART Debug Circuit

RK3576 UART Debug defaults used UART0_RX_M0/UART0_TX_M0, with a default baud rate of 1500000bps.

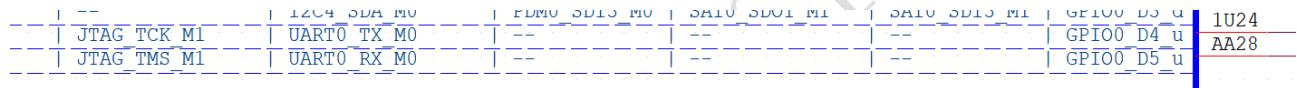


Figure 2-10 RK3576 UART0 M0 pin

The 100ohm resistors in series with UART0_RX_M0/UART0_TX_M0 must not be removed, and TVS diodes should be added to enhance electrostatic surge capability, preventing damage to chip pins during development. It is advisable to reserve 2.54mm pin headers. If not feasible, using test points with a diameter of 0.7mm or above is recommended for easier soldering.

Note: IO level must be matched.

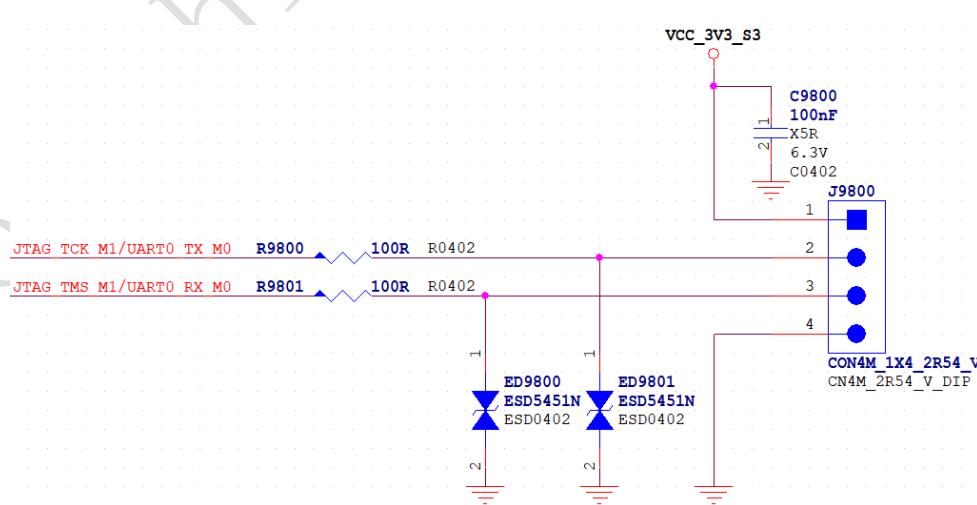


Figure 2-11 RK3576 Debug UART0 Connection Diagram

2.1.7 DDR Circuit

2.1.7.1 DDR Controller Introduction

The RK3576 DDR controller interface supports JEDEC SDRAM standard interface and features:

- Compatibility with LPDDR4/LPDDR4X/LPDDR5 standards.
- Support for a 32-bit data bus width, composed of 2 16bits DDR channels, with each channel capable of addressing a maximum capacity of 8GB. The combined capacity of the two channels can reach up to 16GB.
- Support for Power Down, Self Refresh, and other modes.
- Programmable output and ODT impedance adjustment with dynamic PVT compensation.

2.1.7.2 Circuit Design Suggestion

The RK3576 DDR PHY and each DRAM chip's schematic diagrams need to be consistent with the reference design, including decoupling capacitors.

RK3576 supports LPDDR4/LPDDR4X/LPDDR5, each with different I/O signals. Accordingly, select the corresponding signals based on the type of DRAM. The RK3576 DDR PHY I/O Map table is as follows:

Table 2-4 RK3576 DDR PHY I/O Map

Pin Number	LPDDR4	LPDDR4X	LPDDR5
W1	LP4_DQ0_A	LP4X_DQ0_A	LP5_DQ0_A
1T1	LP4_DQ1_A	LP4X_DQ1_A	LP5_DQ1_A
1P1	LP4_DQ2_A	LP4X_DQ2_A	LP5_DQ2_A
U1	LP4_DQ3_A	LP4X_DQ3_A	LP5_DQ3_A
1V3	LP4_DQ4_A	LP4X_DQ4_A	LP5_DQ4_A
1W4	LP4_DQ5_A	LP4X_DQ5_A	LP5_DQ5_A
AC1	LP4_DQ6_A	LP4X_DQ6_A	LP5_DQ6_A
AB1	LP4_DQ7_A	LP4X_DQ7_A	LP5_DQ7_A
1V1	LP4_DMI0_A	LP4X_DMI0_A	LP5_DMI0_A
1U1	LP4_DQS0P_A	LP4X_DQS0P_A	LP5_RDQS0P_A
Y1	LP4_DQS0N_A	LP4X_DQS0N_A	LP5_RDQS0N_A
1V5	--	--	LP5_WCK0P_A
1V4	--	--	LP5_WCK0N_A
AF1	LP4_DQ8_A	LP4X_DQ8_A	LP5_DQ8_A
1AB1	LP4_DQ9_A	LP4X_DQ9_A	LP5_DQ9_A
1AD1	LP4_DQ10_A	LP4X_DQ10_A	LP5_DQ10_A
AH1	LP4_DQ11_A	LP4X_DQ11_A	LP5_DQ11_A
1Y1	LP4_DQ12_A	LP4X_DQ12_A	LP5_DQ12_A
1W2	LP4_DQ13_A	LP4X_DQ13_A	LP5_DQ13_A
1AA3	LP4_DQ14_A	LP4X_DQ14_A	LP5_DQ14_A
1AA1	LP4_DQ15_A	LP4X_DQ15_A	LP5_DQ15_A

Pin Number	LPDDR4	LPDDR4X	LPDDR5
AE1	LP4_DMI1_A	LP4X_DMI1_A	LP5_DMI1_A
1AB4	LP4_DQS1P_A	LP4X_DQS1P_A	LP5_RDQS1P_A
1AB3	LP4_DQS1N_A	LP4X_DQS1N_A	LP5_RDQS1N_A
1AA6	--	--	LP5_WCK1P_A
1AA5	--	--	LP5_WCK1N_A
T1	LP4_A0_A	LP4X_A0_A	LP5_A0_A
1N1	LP4_A1_A	LP4X_A1_A	LP5_A1_A
1R3	LP4_A2_A	LP4X_A2_A	LP5_A2_A
1T2	LP4_A3_A	LP4X_A3_A	LP5_A3_A
1M5	LP4_A4_A	LP4X_A4_A	LP5_A4_A
1P5	LP4_A5_A	LP4X_A5_A	LP5_A5_A
1R5	--	--	LP5_A6_A
1L1	LP4_CLKP_A	LP4X_CLKP_A	LP5_CLKP_A
P1	LP4_CLKN_A	LP4X_CLKN_A	LP5_CLKN_A
1R4	LP4_CSN0_A	LP4X_CSN0_A	--
1T4	LP4_CSN1_A	LP4X_CSN1_A	--
1N3	LP4_CKE0_A	LP4X_CKE0_A	LP5_CSN0_A
1N5	LP4_CKE1_A	LP4X_CKE1_A	LP5_CSN1_A
1D2	LP4_DQ0_B	LP4X_DQ0_B	LP5_DQ0_B
1F2	LP4_DQ1_B	LP4X_DQ1_B	LP5_DQ1_B
1G1	LP4_DQ2_B	LP4X_DQ2_B	LP5_DQ2_B
K1	LP4_DQ3_B	LP4X_DQ3_B	LP5_DQ3_B
1C3	LP4_DQ4_B	LP4X_DQ4_B	LP5_DQ4_B
1B3	LP4_DQ5_B	LP4X_DQ5_B	LP5_DQ5_B
A5	LP4_DQ6_B	LP4X_DQ6_B	LP5_DQ6_B
G1	LP4_DQ7_B	LP4X_DQ7_B	LP5_DQ7_B
B4	LP4_DMI0_B	LP4X_DMI0_B	LP5_DMI0_B
H1	LP4_DQS0P_B	LP4X_DQS0P_B	LP5_RDQS0P_B
1F1	LP4_DQS0N_B	LP4X_DQS0N_B	LP5_RDQS0N_B
1G5	--	--	LP5_WCK0P_B
1G4	--	--	LP5_WCK0N_B
1A1	LP4_DQ8_B	LP4X_DQ8_B	LP5_DQ8_B
B1	LP4_DQ9_B	LP4X_DQ9_B	LP5_DQ9_B
B2	LP4_DQ10_B	LP4X_DQ10_B	LP5_DQ10_B
A2	LP4_DQ11_B	LP4X_DQ11_B	LP5_DQ11_B
1E1	LP4_DQ12_B	LP4X_DQ12_B	LP5_DQ12_B
1C1	LP4_DQ13_B	LP4X_DQ13_B	LP5_DQ13_B
E1	LP4_DQ14_B	LP4X_DQ14_B	LP5_DQ14_B
D1	LP4_DQ15_B	LP4X_DQ15_B	LP5_DQ15_B

Pin Number	LPDDR4	LPDDR4X	LPDDR5
1B1	LP4_DMI1_B	LP4X_DMI1_B	LP5_DMI1_B
A3	LP4_DQS1P_B	LP4X_DQS1P_B	LP5_RDQS1P_B
B3	LP4_DQS1N_B	LP4X_DQS1N_B	LP5_RDQS1N_B
1D4	--	--	LP5_WCK1P_B
1E4	--	--	LP5_WCK1N_B
L1	LP4_A0_B	LP4X_A0_B	LP5_A0_B
1J1	LP4_A1_B	LP4X_A1_B	LP5_A1_B
1J3	LP4_A2_B	LP4X_A2_B	LP5_A2_B
1G2	LP4_A3_B	LP4X_A3_B	LP5_A3_B
1F4	LP4_A4_B	LP4X_A4_B	LP5_A4_B
1K5	LP4_A5_B	LP4X_A5_B	LP5_A5_B
1H5	--	--	LP5_A6_B
1K1	LP4_CLKP_B	LP4X_CLKP_B	LP5_CLKP_B
N1	LP4_CLKN_B	LP4X_CLKN_B	LP5_CLKN_B
1J5	LP4_CSN0_B	LP4X_CSN0_B	--
1K4	LP4_CSN1_B	LP4X_CSN1_B	--
1K2	LP4_CKE0_B	LP4X_CKE0_B	LP5_CSN0_B
1M3	LP4_CKE1_B	LP4X_CKE1_B	LP5_CSN1_B
1U5	LP4_RESET	LP4X_RESET	LP5_RESET

For LPDDR4/LPDDR4X/LPDDR5:

- DQ and CA sequences do not support swapping; they must be allocated according to the reference diagram.

DDR PHY ZQ must be connected to 240 ohm 1% to DDRPHY_VDDQ_S0 power supply.

Built-in Retention function: During DDR self-refresh, the DDR controller end's DDRPHY_CKE_VDDQ power pin must remain powered, while other power supplies can be turned off. The VDDQ power supply of the DDR chip can be turned off 5ns after tCKELCK closes, but other power supplies must remain on.

LPDDR5 introduces WCK clock; LPDDR5 has two operational clocks:

- LP5_CLKP/N (CK_t/CK_c): Used for controlling command and address operations.
- LP5_WCKP/N (WCK_t/WCK_c): WCK can operate at twice or four times the CK frequency.
- During Write operations, WCK serves as both the clock and Write data strobe.
- During Read operations, WCK serves as the clock for DQ and RDQS, where RDQS is the Read data strobe signal.

2.1.7.3 DDR Chip Peripheral Circuit Design:

- For LPDDR4X/LPDDR5 chips, the ZQ pin must be connected to 240 ohm 1% to the DDRPHY_VDDQ_S0 power supply.
- For LPDDR4 chips, the ZQ pin must be connected to 240 ohm 1% to the VDD2_DDR_S3 power supply.
- For LPDDR4/4X chips, the ODT_CA pin must be connected to the VDD2_DDR_S3 power supply.

2.1.7.4 DDR Topology and Matching Design

For LPDDR4/LPDDR4X/LPDDR5, each chip has a single 32-bit configuration, and DQ and CA adopt a point-to-point topology.

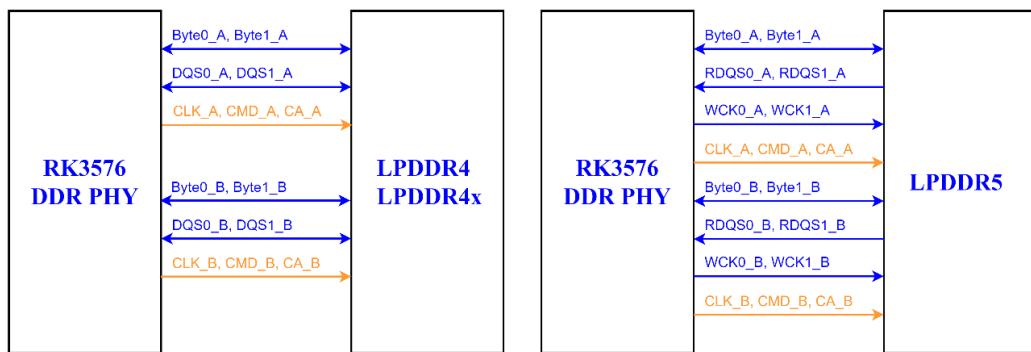


Figure 2-12 LPDDR4/LPDDR4X/LPDDR5 Point-to-Point Topology

Matching Method: LPDDR4/LPDDR4X/LPDDR5 chips support ODT for DQ, CLK, CMD, and CA, all of which can be connected point-to-point.

2.1.7.5 DDR Power Design and Power-Up Sequence Requirement

The summary of power supply for RK3576 DDR PHY is as follows:

DDR PHY Power		LPDDR4/4X	LPDDR5
DDR PLL Power	DDRPHY_PLL_DVDD	0.75V-0.85V	0.75V-0.85V
	DDRPHY_PLL_AVDD1V8	1.8V	1.8V
DIGITAL CORE Power	DDRPHY_DVDD	0.75V-0.85V	0.75V-0.85V
DDR IO Power	DDRPHY_VDDQ	0.61V	0.51V
CK Power	DDRPHY_CK_VDDQ	0.61V	0.51V
LP4/4X_CKE&LP5_CS&Reset Power	DDRPHY_CKE_VDDQ	1.1V	1.05V
Note: Voltage value is the Typ value			

The summary of power supply for LPDDR4/4X/LPDDR5 chips is as follows:

DDR chip Power		LPDDR4	LPDDR4X	LPDDR5
Core Power1	VDD1	1.8V	1.8V	1.8V
Core Power2&CA Power	VDD2/VDD2H	VDD2=1.1V	VDD2=1.1V	VDD2H=1.05V
	VDD2L	/	/	0.9V
I/O Buffer Power	VDDQ	1.1V	0.61V	0.51V
Note: Voltage value is the Typ value				

Attention Points for PMIC Power Supply Circuit Design:

- Please note that according to the actual DRAM chips used, adjust the resistance value of the divider resistance connected to PMIC RK806S-5 FB6 (Pin31) to match the output voltage of VDDQ_DDR_S0 with the chips.

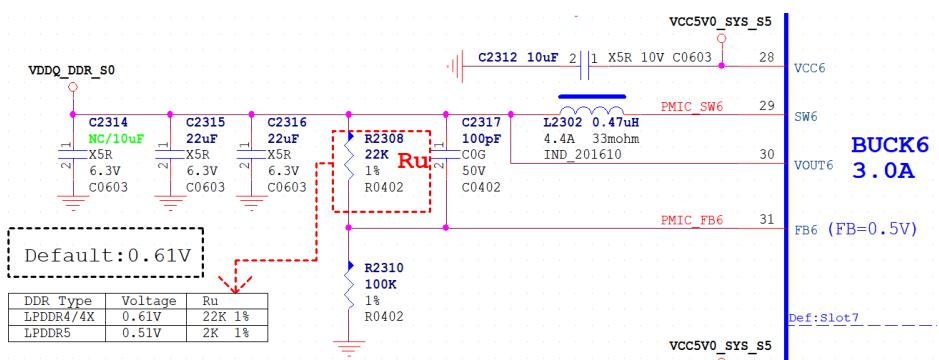


Figure 2-13 Parameter Adjustment for RK806S-5 BUCK6 FB6

- Please note that according to the actual DRAM chips used, adjust the resistance value of the divider resistance connected to PMIC RK806S-5 FB9(Pin66) to match the output voltage of VDD2_DDR_S3 with the chips.

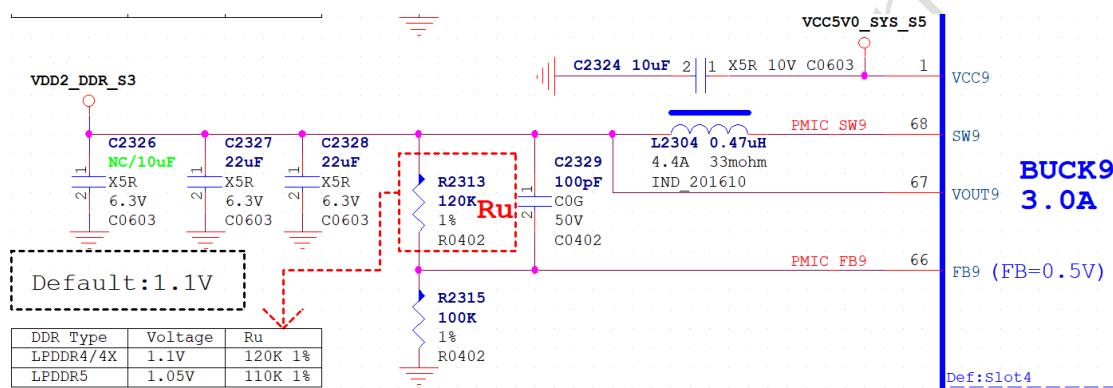


Figure 2-14 Parameter Adjustment for RK806S-5 BUCK9 FB9

The RK3576 reference template "RK3576_Template_LP4XD200P132SD6_24X34_2133MHz" provides designs compatible with LPDDR4 and LPDDR4X. It is important to select the appropriate circuit according to the actual materials used.

- When using LPDDR4 chips, if product is not sensitive to the power consumption of the standby, mount R3805 (Q3800/Q3801/R3810/R3811/C3845 and R3807 are not stick); if sensitive, it's need to use Q3800/Q3801/R3810/R3811/C3845 circuit (R3805 and R3807 are not mounted). The Q3800/Q3801/R3810/R3811/C3845 circuits are designed to realise that VDDQ_DRAM_S0 could be powered down during standby.
- When using LPDDR4X chips, only resistor R3807 should be mounted, and the components enclosed in the green box (Q3800/Q3801/R3810/R3811/C3845) is don't need.

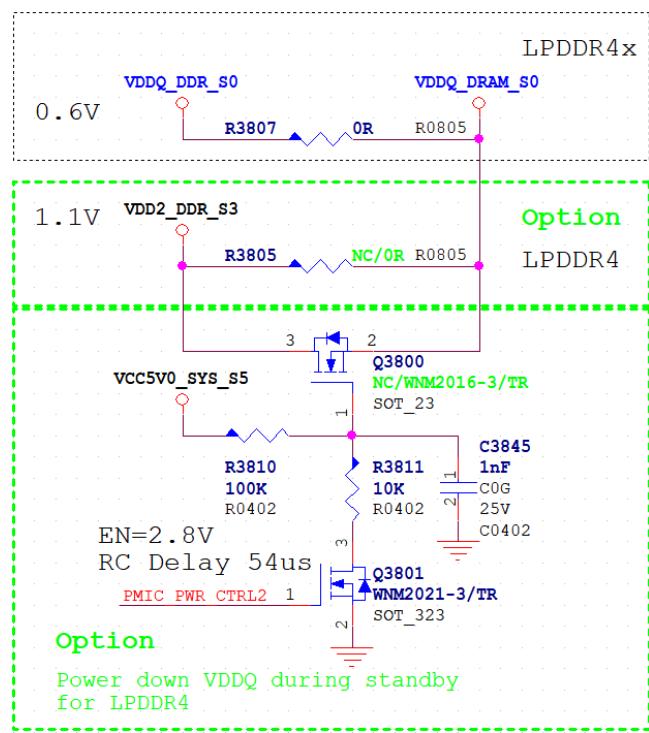


Figure 2-15 Power Supply Selection for LPDDR4/LPDDR4X Compatibility Design

Please refer to the respective JEDEC standards for the power-up timing requirements of each type of DRAM.

- The power-up timing sequence for LPDDR4/4X SDRAM is as shown in Figure 2-16.

- While applying power (after Ta), RESET_n is recommended to be LOW ($\leq 0.2 \times V_{DD2}$) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 5. V_{DD1} must ramp at the same time or earlier than V_{DD2} . V_{DD2} must ramp at the same time or earlier than V_{DDQ} .

Table 5 — Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2} V_{DD2} must be greater than $V_{DDQ} - 200$ mV

- NOTE 1 Ta is the point when any power supply first reaches 300 mV.
 NOTE 2 Voltage ramp conditions in Table 5 apply between Ta and power-off (controlled or uncontrolled).
 NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges.
 NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
 NOTE 5 The voltage difference between any of V_{SS} and V_{SSQ} pins must not exceed 100 mV.

Figure 2-16 power-up timing sequence for LPDDR4/4X SDRAM

- The power-up timing sequence for LPDDR5 SDRAM is as shown in Figure 2-17.

- 1) While applying power (after Ta), RESET_n is recommended to be LOW ($\leq 0.2 \times VDD2H$) and all other inputs shall be between VILmin and VIHmax. The SDRAM outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 17. VDD1 must ramp at the same time or earlier than VDD2H. VDD2H must ramp at the same time or earlier than VDD2L. VDD2L must ramp at the same time or earlier than VDDQ.

Table 17 — Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2H
	VDD2H must be equal to or greater than VDD2L
	VDD2L must be greater than VDDQ-200mV

NOTE 1 Ta is the point when any power supply first reaches 300mV.

NOTE 2 Voltage ramp conditions in Table 17 apply between Ta and power-off (controlled or uncontrolled).

NOTE 3 Tb is the point at which all supply voltages are within their defined ranges.

NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

Figure 2-17 The power-up timing sequence for LPDDR5 SDRAM

2.1.7.6 Supported DDR Models List:

Please refer to the document "Rockchip_Support_List_DDR" for RK3576 supported DDR models, which download on the Rockchip Electronics Redmine platform: <https://redmine.rock-chips.com/projects/fae/documents>

2.1.8 eMMC Circuit

2.1.8.1 eMMC Controller Introduction

The RK3576 eMMC controller features the following characteristics:

- Compatible with specifications 5.1, 5.0, 4.51, and 4.41.
- Supports three data bus widths: 1-bit, 4-bit, and 8-bit.
- Supports modes such as HS400 ES, HS400, HS200, DDR50, etc.
- Supports CMD Queue.

2.1.8.2 eMMC Circuit Design Recommendations

The RK3576 eMMC interface is multiplexed with the FSPIO interface. When designing the eMMC interface, please follow the reference schematic for eMMC signal connections, including the decoupling capacitors for each power rail.

When using eMMC, place the boot code in the eMMC.

Note: If the chips used support HS400 ES mode, it will default to operating in HS400 ES mode.

2.1.8.3 eMMC Topology and Matching Design

eMMC connection diagram:

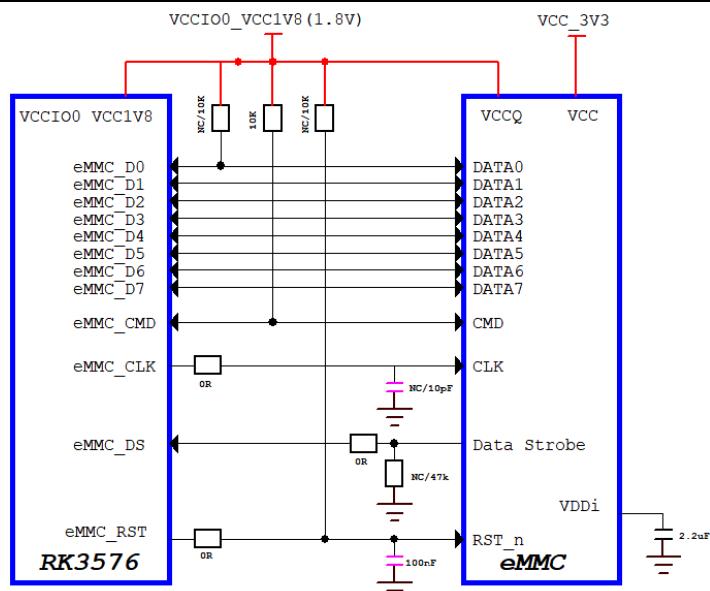


Figure 2-18 eMMC connection diagram

The recommended eMMC interface pull-up/down and matching design for the RK3576 is shown in the table below:

Table 2-5 RK3576 eMMC interface design

Signal	Internal pull up/down configuration	Connection method	Description (chip end)
eMMC_D[7: 0]	Pull-up	Direct Connection, D0 externally reserved pull-up resistor with recommended resistance of 10K ohm, other Data use internal pull-up resistors of RK3576	eMMC data transmission/reception
eMMC_CLK	/	Series 0-ohm resistor at the RK3576 end, reserve a 10pF capacitor to ground at the chip end	eMMC clock transmission
eMMC_CMD	Pull-up	Direct Connection, external pull-up resistor must be connected with recommended resistance of 10K ohm	eMMC command transmission/reception
eMMC_STRB	Pull-down	Series 0-ohm resistor at the eMMC end, and reserve a 47K ohm pull-down resistor	Reference Strobe for eMMC data and command reception
eMMC_RST	Pull-up	Series 0-ohm resistor at the RK3576 end, external reserved pull-up resistor, connect a 100nF capacitor to ground at the chip end	eMMC reset signal

**NOTE**

Note 1: When GPIO resources are sufficient, it is recommended to connect eMMC_RST to the chip's RST_n pin, while also connecting a 100nF capacitor to ground at the chip end.

Note 2: In case of insufficient GPIO pins, eMMC_RST may not be connected to the chip's RST_n pin. However, a pull-up resistor should be connected to the chip's RST_n pin. In this scenario, the 100nF capacitor to ground at the chip end may be omitted.

2.1.8.4 eMMC Power-On Sequence Requirements

The eMMC interface of the RK3576 chip belongs to the VCCIO0_1V8 power domain, with only one power supply group and no timing requirements.

For the eMMC chips, there are two power supply groups. Please refer to the JEDEC standard for power-up timing sequence.

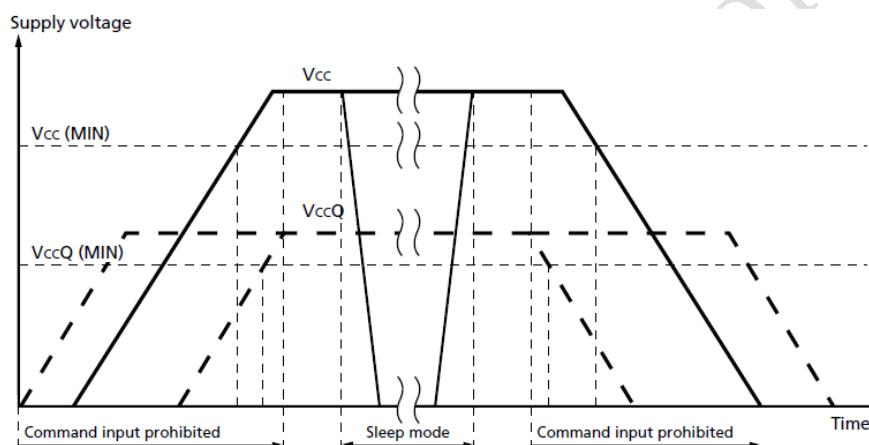


Figure 2-19 eMMC chip power up/down timing sequence

2.1.8.5 Supported eMMC Models List

Please refer to “RKeMMC SupportList” for RK3576 supported eMMC models, which download on the RK Redmine platform: <https://redmine.rock-chips.com/projects/fae/documents>

2.1.9 UFS Circuit

2.1.9.1 UFS Controller Introduction

The RK3576 UFS controller has the following features:

- Supports the UFS 2.0 protocol.
- Supports 2-lane data transmission, with a maximum speed of 5.8Gbps per lane.

2.1.9.2 UFS Circuit Design Recommendations

For RK3576 UFS, when designing the UFS interface, please follow the reference schematic for UFS signal

connections.

When using UFS, place the boot code in the UFS.

Pay attention to the following three points when circuit design:

- The reset signal UFS_RSTN and clock signal UFS_REFCLK of UFS are 1.2V, and VCCIO7_VCC should be powered by 1.2V.

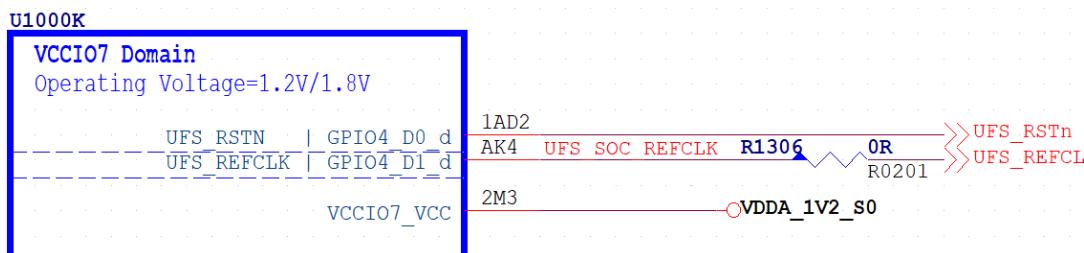


Figure 2-20 UFS Control Signal Power Domain

- UFS supports chips for UFS 2.0/ UFS 2.1/ UFS 2.2/ UFS 3.0/ UFS 3.1. Different protocol chips have different power requirements, so power design should be based on the chip specification. RK3576 does not support UFS chips for version 4.0 and above.

Table 2-6 RK3576 power supply design

Supported Particles	VCCQ	VCCQ2	VCC
UFS2.0	1.2V	1.8V	3.3V
UFS2.1	Not Connect	1.8V	3.3V
UFS2.2	Not Connect	1.8V	3.3V
UFS3.0	1.2V	Not Connect	2.5V/3.3V
UFS3.1	1.2V	Not Connect	2.5V/3.3V
Do not support UFS4.0 Device!			

- At the UFS chip end: Use three decoupling capacitors for power supply as follows. The capacitance values for different protocol chips vary and should be selected according to the chip specification.

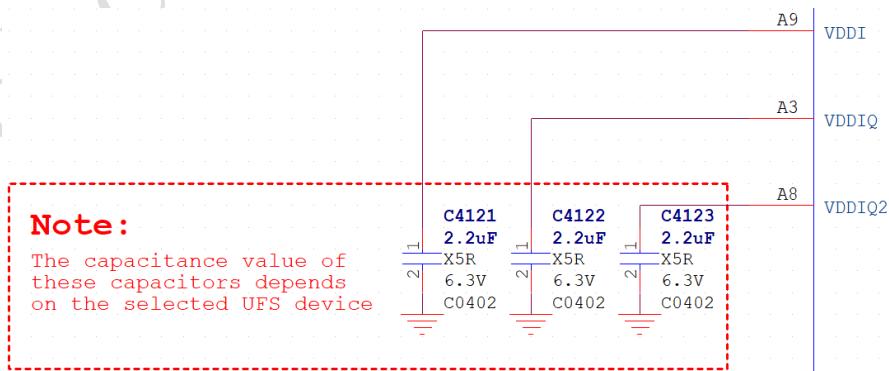


Figure 2-21 decoupling capacitors for different protocol

2.1.9.3 UFS Topology and Matching Design

UFS connection diagram:

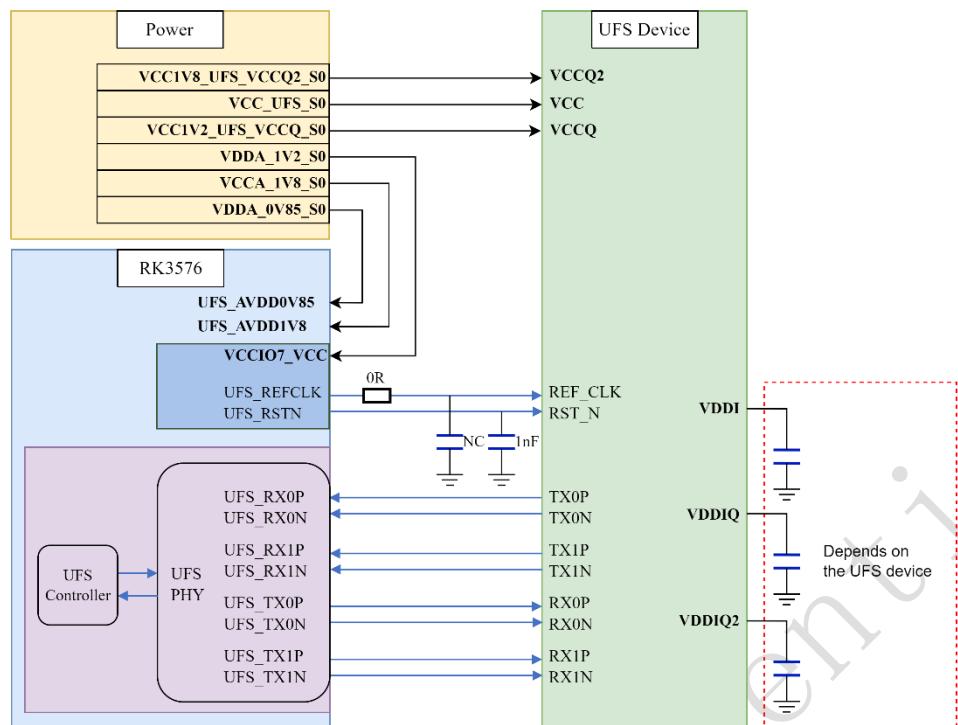


Figure 2-22 UFS connection diagram

The recommended UFS interface pull-up/down and matching design is shown in the table below:

Table 2-7 RK3576 UFS interface design

Signal	Connection method	Description (chip end)
UFS_TX_D0P/N	Direct connection	UFS data transmission
UFS_TX_D1P/N	Direct connection	UFS data transmission
UFS_RX_D0P/N	Direct connection	UFS data reception
UFS_RX_D1P/N	Direct connection	UFS data reception
UFS_REFCLK	Series 0-ohm resistor at the RK3576 end, and reserve a capacitor place to ground at the UFS end	UFS reference clock
UFS_RSTN	Direct connection. Reserve a 1nF capacitor to ground at the UFS end.	UFS reset signal

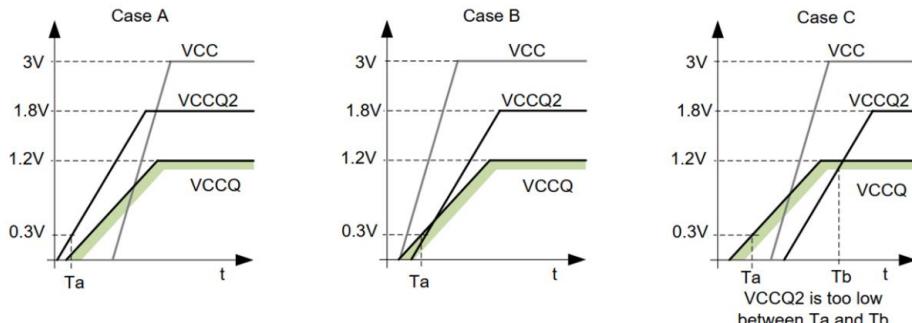
2.1.9.4 UFS Power-Up and Power-Down Timing Requirements

For the RK3576 chip's UFS interface, there are two sets of power supplies, UFS_AVDD0V85 and UFS_AVDD1V8. It is required that UFS_AVDD0V85 be powered up before UFS_AVDD1V8.

The power domain VCCIO7_VCC for UFS control signals needs to be powered up before the UFS chips.

UFS chips have three sets of power supplies. Please refer to the JEDEC standard for power-up timing.

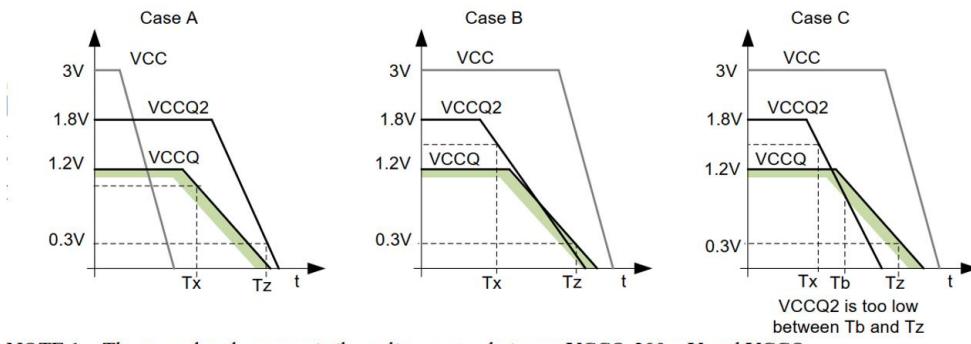
Figure 7.6 shows three power up ramp examples: case A and case B meet the requirement, while case C violates it in the time interval from T_a to T_b (V_{CCQ2} is lower V_{CCQ} - 200 mV).



NOTE 1 The green band represents the voltage range between V_{CCQ} -200 mV and V_{CCQ} .

Figure 7.6 — Power up ramps

Figure 7.7 shows three power down ramp examples: case A and case B meet the requirement, while case C violates it in the time interval from T_b to T_z .



NOTE 1 The green band represents the voltage range between V_{CCQ} -200 mV and V_{CCQ} .

Figure 7.7 — Power off ramps

Figure 2-23 UFS Chip Power-Up and Power-Down Timing

Typical power-up timing recommended by the reference diagram is as follows:

Relative timing	Power pin
(1)	UFS_AVDD0V85 of RK3576
(2)	UFS_AVDD1V8 of RK3576
(3)	VCCIO7_VCC of RK3576
(4)	VCCQ2 of UFS
(5)	VCCQ of UFS
Must after (3)	VCC of UFS

2.1.9.5 Supported UFS Models List

Please refer to RK document “RK_UFS SupportList” for RK3576 supported UFS chips, which download on the RK redmine platform: <https://redmine.rock-chips.com/projects/fae/documents>

2.1.10 FSPI Flash Circuit

2.1.10.1 FSPI Flash (support Boot) Interface Introduction

There are two FSPI controller in RK3576, which is a flexible serial interface controller used for FSPI device.

Key features of RK3576 FSPI controllers include:

- Support for serial NOR Flash and serial NAND Flash.

- Compatibility with SDR mode.
- Support for 1-line, 2-line, and 4-line modes.

**NOTE**

The RK3576 FSPI interface is used for connecting the SPI Flash for Boot. It is can not connecting other functional SPI Flash devices.

2.1.10.2 FSPI Flash Circuit Design Recommendation

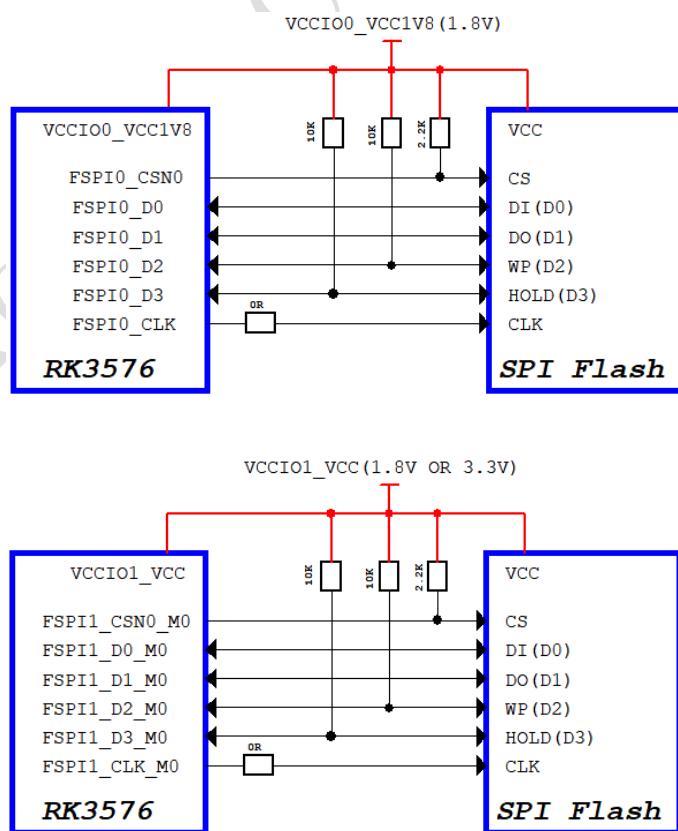
RK3576's FSPI0 interface is multiplexed with the eMMC interface, located in the VCCIO0 power domain (supporting only 1.8V). The FSPI1 interface has two multiplexed interfaces (suffixes _M0 and _M1), distributed in the VCCIO1 and VCCIO3 domains (both supporting 1.8V/3.3V).

When designing the FSPI Flash interface, please follow the reference design schematic diagram for connecting FSPI Flash signals.

When using FSPI Flash, ensure that the boot code is placed in the FSPI Flash, and pay attention to whether the IO drive voltage mode configuration of RK3576's corresponding power domain matches the actual supply voltage.

2.1.10.3 FSPI Flash Topology and Matching Design

FSPI Flash Connection Diagram:



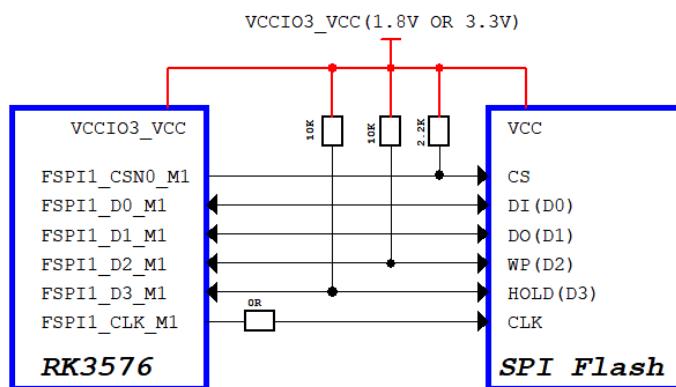


Figure 2-24 FSPI Flash Connection Diagram

The recommended FSPI interface pull-up and matching designs are as shown in the following tables:

Table 2-8 FSPI interface designs

Signal	Internal Pull-Up/Down Configuration	Connection Method	Description (Chip End)
FSPI0_D[3: 0]	Pull up	Direct connection; when in 1-line mode, external pull-up resistors are needed for D2 and D3, with a recommended resistance of 10K ohm	FSPI data transmission/reception
FSPI0_CLK	/	Series a 0-ohm resistor at the RK3576 end	FSPI clock transmission
FSPI0_CSNO	Pull up	Direct connection, using internal pull-up resistors of RK3576 for pull-up	FSPI chip selection signal
FSPI0_CSN1 or FSPI0_RSTN (same GPIO)	Pull up	FSPI_CSN1: Direct connection, using internal pull-up resistors of RK3576 for pull-up	FSPI_CSN1: FSPI chip selection signal
		Direct connection, using internal pull-up resistors of RK3576 for pull-up; connection based on chip requirements	FSPI_RSTN: FSPI reset signal

Table 2-9 RK3576 FSPI1_M0 interface design

Signal	Internal Pull-Up/Down Configuration	Connection Method	Description (Chip End)
FSPI1_D[3: 0]_M0	Pull up	Direct connection; when in 1-line mode, external pull-up resistors are needed for D2 and D3, with a recommended resistance of 10K ohm	FSPI data transmission/reception
FSPI1_CLK_M0	/	Series a 0-ohm resistor at the RK3576 end	FSPI clock transmission

Signal	Internal Pull-Up/Down Configuration	Connection Method	Description (Chip End)
FSPI1_CS0_M0	Pull up	Direct connection, external must connect a 2.2kohm pull up resistor	FSPI chip selection signal

Table 2-10 RK3576 FSPI1_M1 interface design

Signal	Internal Pull-Up/Down Configuration	Connection Method	Description (Chip End)
FSPI1_D[3: 0]_M1	Pull up	Direct connection; when in 1-line mode, external pull-up resistors are needed for D2 and D3, with a recommended resistance of 10K ohm	FSPI data transmission/reception
FSPI1_CLK_M1	/	Series a 0-ohm resistor at the RK3576 end	FSPI clock transmission
FSPI1_CS0_M1	Pull up	Direct connection, using internal pull-up resistors of RK3576 for pull-up	FSPI chip selection signal
FSPI1_CS1_M1 or FSPI1_RSTN_M1 (same GPIO)	Pull up	FSPI_CS1: Direct connection, using internal pull-up resistors of RK3576 for pull-up	FSPI_CS1: FSPI chip selection signal
		FSPI_RSTN: Direct connection, using internal pull-up resistors of RK3576 for pull-up; connection based on chip requirements	FSPI_RSTN: FSPI reset signal

Points to Note:

- Due to the default low level of CSN on FSPI1_M0 during power-up, when connecting FSPI, the CSN pin must be pulled up to a high level using a 2.2K/4.7K resistor to ensure that CSN is high during power-up.
- The RSTN function of FSPI is controlled by the specified GPIO. During boot, the corresponding GPIO will act. After entering the system, chip reset is controlled by controlling GPIO.
- When use the FSPI0 detecting BOOT level, **the GPIO1_B0 where FSPI0_RSTN is located changes from pull-down to pull-up. If this process affects the status of external devices, be careful not to use this IO to control sensitive peripherals.**
- When use FSPI1_M1 detecting BOOT level, **the GPIO1_C2 where FSPI1_RSTN_M1 is located changes from pull-down to pull-up. If this process affects the status of external devices, be careful not to use this IO to control sensitive peripherals.**

2.1.10.4 FSPI Power-up Timing Requirements

The RK3576 chip's FSPI Flash interface has only one set of power supply and no timing requirements.

The SPI Flash has only one power source, and the power must be the same as the power domain selected for the corresponding FSPI interface.

Note: It is required that CS must be pulled high when the power is powered on.

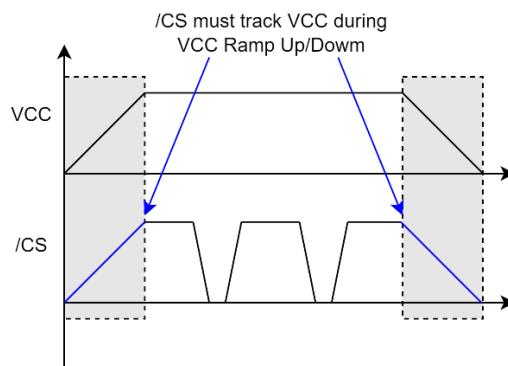


Figure 2-25 Illustration of the relationship between FSPI CS and the VCC during power-up and power-down.

2.1.10.5 Supported SPI Flash Models List

Please refer to RK document “RK_SpiNor_and_SLC_Nand_SupportList” for RK3576 supported SPI Flash chips, which download on the RK redmine platform: <https://redmine.rock-chips.com/projects/fae/documents>

2.1.11 GPIO Circuit

2.1.11.1 GPIO Types

RK3576 GPIOs have the following four types:

- (1) 1.8V only type, operating at a voltage of 1.8V.
- (2) 1.8V/1.2V type. VCCIO7 adopts this type, which needs to select the supply voltage according to the scenario. When using the UFS function, the two GPIOs of VCCIO7 need to operate in the UFS control signal mode, and use 1.2V power supply. When the UFS function is not used, a voltage of 1.8V is used, and the GPIOs of VCCIO7 can be used as ordinary GPIOs.
- (3) 1.8V/3.3V type. When configured as 3.3V type IO, a 3.3V power supply is used. When configured as 1.8V type GPIO, a 1.8V power supply is used.
- (4) eMMC IO type, operating at a voltage of 1.8V.

All of the above four types of GPIOs support Retention IO (Core Power Off and IO Power On) and do not support fail-safe (Core Power Off and IO Power off). **Note: When allocating GPIOs, certain functional pins need to maintain their state before standby. Software needs to enable the Retention function. When enabling the Retention function, LOGIC_DVDD of RK3576 can be powered off, but the power supply of the GPIO domain must be powered.**

These GPIOs support CMOS input and Schmitt trigger input; Pull-up (PU), pull-down (PD), and PU/PD Disable can be set via registers, enabling or disabling pull-up/down according to the application requirements of the product.

These GPIOs support interruptable functionality.

2.1.11.2 GPIO Pin Naming Description

For example, the functions such as JTAG_TMS_M1 and UART0_RX_M0 are multiplexed on GPIO0_D5 as shown in the diagram below. When allocating, only one function can be selected for use.



- Except for GPIOs related to booting, the remaining GPIOs default to input upon reset.
- GPIO_{x_xx_u}: "_u" indicates that the default state of this GPIO upon reset is internal pull-up.
- GPIO_{x_xx_d}: "_d" indicates that the default state of this GPIO upon reset is internal pull-down.
- GPIO_{x_xx_z}: "_z" indicates that the default state of this GPIO upon reset is high impedance.
- Each function name suffix is followed by _M0, M1, M2, or M3, representing the same function multiplexed to different GPIOs. Only one of them can be selected at a time. For example, when selecting the UART2 function, you must choose the combination of UART2_TX_M0 and UART2_RX_M0. The combination of UART2_TX_M0 and UART2_RX_M1 is not supported. This constraint applies to all functions with different IOMUX.

2.1.11.3 GPIO Drive Capability

In RK3576, GPIOs provide multiple levels of adjustable drive strength, including Level 0-5 for most GPIOs and Level 0-3 for some GPIOs. For specific details, please refer to the "RK3576_PinOut" document. Additionally, the initial default drive strength varies depending on the GPIO type. Please refer to the chip TRM for configuration, or consult Table 5 in the "RK3576_PinOut" document for "Support Drive Strength" and "Default IO Drive Strength" columns.

The drive strength levels for GPIOs are as follows:

Table 2-11 RK3576 GPIO Output Driver Strength

GPIO Type	Output Driver Strength Level	Output Driver Strength Value
eMMC IO	Level 0	3mA,100ohm
	Level 1	4.5mA,66ohm
	Level 2	6mA,50ohm
	Level 3	7.2mA,40ohm
	Level 4	9mA,33ohm
	Level 5	12mA,25ohm
1.8V/3.3V	Level 0	3mA,100ohm
	Level 1	4.5mA,66ohm
	Level 2	6mA,50ohm
	Level 3	7.5mA,40ohm
	Level 4	9mA,33ohm
	Level 5	12mA,25ohm
1.8V/1.2V	Level 0	2.5mA,100ohm
	Level 1	5mA,50ohm
	Level 2	7.5mA,33ohm
	Level 3	10mA,25ohm
1.8V only	Level 0	2.5mA,100ohm
	Level 1	5mA,50ohm
	Level 2	7.5mA,33ohm

GPIO Type	Output Driver Strength Level	Output Driver Strength Value
	Level 3	10mA,25ohm

2.1.11.4 GPIO power supply

The power supply pins for GPIO domains are described as follows:

Table 2-12 RK3576 GPIO power supply pins

Power domain	GPIO type	Pin name	Description
PMUIO0	1.8V	PMUIO0_VCC1V8	1.8V Only IO supply for this GPIO domain (group).
PMUIO1	1.8V/3.3V	PMUIO1_VCC	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO0	1.8V	VCCIO0_VCC1V8	1.8V Only IO supply for this GPIO domain (group).
VCCIO1	1.8V/3.3V	VCCIO1_VCC	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO2	1.8V/3.3V	VCCIO2_VCC	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO3	1.8V/3.3V	VCCIO3_VCC	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO4	1.8V/3.3V	VCCIO4_VCC	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO5	1.8V/3.3V	VCCIO5_VCC	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO6	1.8V/3.3V	VCCIO6_VCC	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO7	1.2V/1.8V	VCCIO7_VCC	1.2V or 1.8V IO supply for this GPIO domain (group).

PMUIO0 and VCCIO0 are fixed-level power domains and cannot be configured.

For PMUIO1 and VCCIO1~VCCIO6 power domains, the RK3576 chip can automatically detect the hardware-configured voltage, so there is no need for software configuration.

For example, if PMUIO1 is configured as 1.8V, PMUIO1_VCC = 1.8V; if configured as 3.3V, PMUIO1_VCC = 3.3V (The connection method for VCCIO1~VCCIO6 is the same as PMUIO1).

Notes:

- The GPIO power domains of the SoC need to be powered up before the peripherals.
- When the GPIO power supply of the peripheral device is the same as that of the RK3576 GPIO, the external pull-up power of GPIO uses the power supply from the host side for pulling up.
- When the GPIO power supply of the peripheral device is not the same as that of the RK3576 GPIO, the GPIO of the peripheral device needs to be powered up later than the RK3576 GPIO. In this case, the external pull-up power of GPIO needs to use the power supply from the peripheral device for pulling up.
- For RK3576 using a motherboard-daughterboard configuration, it is recommended that the core board provide 3.3V and 1.8V power supplies to the baseboard, and the peripherals on the baseboard use the power supply provided by the core board. If this cannot be achieved, then it must be noted that the peripherals on the baseboard cannot be powered up first, and the external pull-up resistor power for GPIO must also come from the baseboard power supply to avoid leakage current from the core board's power supply through the pull-up resistor to the peripheral device.
- Ensure that the voltage level of the GPIO power domain matches the IO level of the interface external chip/device.
- Place at least one 100nF or 1uF decoupling capacitor close to each power supply pin of the power domains. Detailed design refer to the reference schematic, and any arbitrary removal is not allowed.
- If none of the GPIOs in a power domain are used, the power supply for that domain can be turned off,

and the pin can be left floating.

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2.2 Power Supply Design

2.2.1 RK3576 Power Supply Introduction

2.2.1.1 RK3576 Power Supply Requirements

Table 2-13 RK3576 power supply requirements

Module	Power pin	Description
PLL	PLL_DVDD0V75、PLL_AVDD1V8	System PLL power
DDR PLL	DDRPHY_PLL_DVDD、DDRPHY_PLL_AVDD1V8	DDR PLL power
DDR_VDD	DDRPHY_DVDD	DDR digital CORE power
DDR_VDDQ_CK	DDRPHY_CK_VDDQ	LPDDR4/4X and LPDDR5 CK power
DDR_VDDQ_CKE	DDRPHY_CKE_VDDQ	LPDDR4/4X_CKE & LPDDR5_CS &RESET power
DDR VDDQ	DDRPHY_VDDQ	DDR IO power (except CK\CKE\RESET power)
CPU_BIG	CPU_BIG_DVDD	CPU_BIG(4*A72) power
CPU_LIT	CPU_LIT_DVDD	CPU_LIT(A53) power
GPU	GPU_DVDD	GPU power
NPU	NPU_DVDD	NPU power
LOGIC	LOGIC_DVDD	SoC logic power
LOGIC MEM	LOGIC_MEM_DVDD	SoC logic Memory power
PMU_0V75	PMU_LOGIC_DVDD0V75	PMU logic power
OSC	OSC_AVDD1V8	system crystal oscillator power
UFS OSC	OSC_UFS_AVDD	UFS crystal oscillator power
MPHY(UFS2.0)	UFS_AVDD0V85、UFS_AVDD1V8	UFS2.0 PHY power
GPIO	PMUIO0_VCC1V8、PMUIO1_VCC、VCCIO0_VCC1V8、VCCIO1_VCC、VCCIO2_VCC、VCCIO3_VCC、VCCIO4_VCC、VCCIO5_VCC、VCCIO6_VCC、VCCIO7_VCC	Power for each GPIO
SARADC/TSADC/OTP	SARADC_AVDD1V8	SARADC/TSADC/OTP power
OTP	OTP_DVDD0V75	OTP power
USB2.0 PHY	USB2_OTG_DVDD0V75、USB2_OTG_AVDD1V8、USB2_OTG_AVDD3V3	USB2.0 OT0 and USB2.0 OT1 PHY power
USB3.0/DP1.4 Combo PHY	USB3_OTG0_DP_TX_AVDD0V85、USB3_OTG0_DP_TX_DVDD0V85、USB3_OTG0_DP_TX_AVDD1V8	USB3.2_Gen1x1 OTG0/DP 1.4 Combo PHY power
PCIE2.1/SATA3.1/USB3.0 Combo PHY	PCIE0_SATA0_AVDD0V85、PCIE0_SATA0_AVDD1V8、PCIE1_SATA1_USB3_OTG1_AVDD0V85、	PCIE2.1/SATA3.1/USB3.2_Gen1x1 OTG1 Combo PHY related power

Module	Power pin	Description
	PCIE1_SATA1_USB3_OTG1_AVDD1V8	
MIPI D/C PHY DS1 TX/CSI RX Combo	MIPI_DCPHY_AVDD、 MIPI_DCPHY_AVDD1V2、 MIPI_DCPHY_AVDD1V8	MIPI D/C Combo PHY related power
MIPI DPHY CSI PHY	MIPI_DPHY_CSI1/2_RX_AVDD0V75、 MIPI_DPHY_CSI1/2_RX_AVDD1V8、 MIPI_DPHY_CSI3/4_RX_AVDD0V75、 MIPI_DPHY_CSI3/4_RX_AVDD1V8	MIPI DPHY CSI1/2 power and MIPI DPHY CSI3/4 power
HDMI/eDP TX Combo PHY	HDMI_TX_EDP_TX_AVDDD0V75、 HDMI_TX_EDP_TX_AVDDC0V75、 HDMI_TX_EDP_TX_AVDDIO1V8、 HDMI_TX_EDP_TX_AVDDCMN1V8	HDMI2.1/eDP1.3 Combo PHY power

2.2.1.2 RK3576 Power-up Timing Requirements

In theory, adhere to the principle of low voltage first, high voltage later, and simultaneous power-up for the same voltage module. There are no timing requirements between different analog PHY modules. After the last voltage stabilizes, RESET_L must be held for at least 1ms before release (if RESET_L is also used to reset other peripherals, it must meet the requirements of the peripherals, typically released within 5ms-200ms).

The recommended typical power-on sequence according to the reference diagram is as follows:

(1) Digital modules, PLL, OTP, SARADC/TSADC power supplies:

Related timing	Power pin
(1)	PMU_LOGIC_DVDD0V75 / LOGIC_MEM_DVDD / LOGIC_DVDD / PLL_DVDD0V75 / OTP_DVDD0V75 / CPU_LIT_DVDD / CPU_BIG_DVDD / NPU_DVDD
(2)	PLL_AVDD1V8 / SARADC_AVDD1V8
(3)	SARADC_AVDD1V8
N/A	GPU_DVDD have no timing requirements

(2) MPHY(UFS2.0):

Related timing	Power pin
(1)	UFS_AVDD0V85
(2)	UFS_AVDD1V8

(3) USB PHY:

USB2.0 OTG PHY:

Related timing	Power pin
(1)	USB2_OTG_DVDD0V75
(2)	USB2_OTG_AVDD1V8
(3)	USB2_OTG_AVDD3V3

USB3 OTG0/DP1.4 PHY

Related timing	Power pin
(1)	USB3_OTG0_DP_TX_AVDD0V85 / USB3_OTG0_DP_TX_DVDD0V85
(2)	USB3_OTG0_DP_TX_AVDD1V8

(4) MIPI DCPHY:

Related timing	Power pin
(1)	MIPI_DCPHY_AVDD
(2)	MIPI_DCPHY_AVDD1V8
(3)	MIPI_DCPHY_AVDD1V2

(5) MIPI DPHY:

Related timing	Power pin
(1)	MIPI_DPHY_CSI1/2_RX_AVDD0V75 / MIPI_DPHY_CSI3/4_RX_AVDD0V75
(2)	MIPI_DPHY_CSI1/2_RX_AVDD1V8 / MIPI_DPHY_CSI3/4_RX_AVDD1V8

(6) HDMI/eDP TX Combo PHY:

Related timing	Power pin
(1)	HDMI_TX_EDP_TX_AVDDD0V75 / HDMI_TX_EDP_TX_AVDDC0V75
(2)	HDMI_TX_EDP_TX_AVDDIO1V8 / HDMI_TX_EDP_TX_AVDDCMN1V8

(7) PCIE20/SATA30 Combo PHY:

Related timing	Power pin
(1)	PCIE0_SATA0_AVDD0V85 / PCIE1_SATA1_USB3_OTG1_AVDD0V85
(2)	PCIE0_SATA0_AVDD1V8 / PCIE1_SATA1_USB3_OTG1_AVDD1V8

(8) DDR PHY:

Related timing	Power pin
(1)	DDRPHY_DVDD
(2)	DDRPHY_CKE_VDDQ
(3)	DDRPHY_VDDQ / DDRPHY_CK_VDDQ

The overall recommended power-on timing according to the reference schematic power network names allocated is as follows:

Related timing	Power pin
(1)	VDD_0V75_S3 / VDD_LOGIC_S0 / LOGIC_DVDD_MEM_S0 / CPU_LIT_DVDD_S0 / VDD_CPU_BIG_S0 / NPU_DVDD_S0 / VDDA_0V75_S0 / VDDA_DDR_PLL_S0 / DDRPHY_DVDD_S0 / VDDA_0V85_S0 / VDDA0V75_HDMI_S0 / GPU_DVDD_S0
(2)	VCC_1V8_S3 / VCCA_1V8_S0
(3)	VCC_1V8_S0
(4)	VDD2_DDR_S3 / VDDA_1V2_S0
(5)	VCC_3V3_S3 / VCCIO_SD_S0 / VCCA_3V3_S0 / VCCA1V8_PLDO2_S0
(6)	VDD2L_0V9_DDR_S3 / VCC_3V3_S0
(7)	DDRPHY_VDDQ_S0
(8)	RESET_L

2.2.1.3 RK3576 Power Down Timing Requirements

The power down process requires that RESET_L be pulled low first, followed by the power down of each power supply. The recommended power down sequence is as follows:

- During the power down process, the voltage difference between the 3.3V supply voltage for GPIOs and the 1.8V supply voltage for PMUIO0_VCC1V8 should not exceed 2V.
- During the power down process, the voltage difference between the USB2_OTG_AVDD3V3 supply voltage and the USB2_OTG_AVDD1V8 supply voltage should not exceed 2V.

2.2.2 Power Design Recommendations

2.2.2.1 Power-On and Standby Circuitry Solutions

For the first power-on of the RK3576, the power requirements for each module are as follows:

Table 2-14 power requirements for each module of RK3576

Module	Power pins	First Power-On Supply Requirements
PLL	PLL_DVDD0V75, PLL_AVDD1V8	Must be powered
DDR PLL	DDRPHY_PLL_DVDD, DDRPHY_PLL_AVDD1V8	Must be powered
DDR_VDD	DDRPHY_DVDD	Must be powered
DDR_VDDQ_CK	DDRPHY_CK_VDDQ	Must be powered
DDR_VDDQ_CKE	DDRPHY_CKE_VDDQ	Must be powered
DDR_VDDQ	DDRPHY_VDDQ	Must be powered
CPU_BIG	CPU_BIG_DVDD	Must be powered
CPU_LIT	CPU_LIT_DVDD	Must be powered
GPU	GPU_DVDD	Not required to be powered
NPU	NPU_DVDD	Must be powered
LOGIC	LOGIC_DVDD	Must be powered
LOGIC MEM	LOGIC_MEM_DVDD	Must be powered
PMU_0V75	PMU_LOGIC_DVDD0V75	Must be powered
OSC	OSC_AVDD1V8	Must be powered
UFS OSC	OSC_UFS_AVDD	Must be powered when UFS is enabled
MPHY(UFS2.0)	UFS_AVDD0V85, UFS_AVDD1V8	Must be powered when UFS is enabled
GPIO	PMUIO0_VCC1V8, PMUIO1_VCC	Must be powered
GPIO	VCCIO0_VCC1V8	Must be powered when EMMC/FSPI0 works
GPIO	VCCIO1_VCC	Must be powered when SDMMC0/FSPI1_M0 is enabled
GPIO	VCCIO3_VCC	Must be powered when FSPI1_M1 is enabled
GPIO	VCCIO7_VCC	Must be powered when UFS is enabled

Module	Power pins	First Power-On Supply Requirements
GPIO	VCCIO2_VCC, VCCIO4_VCC, VCCIO5_VCC, VCCIO6_VCC	Not required to be powered
SARADC/TSADC/OTP	SARADC_AVDD1V8	Must be powered
OTP	OTP_DVDD0V75	Must be powered
USB2.0 PHY	USB2_OTG_DVDD0V75, USB2_OTG_AVDD1V8, USB2_OTG_AVDD3V3	Must be powered
USB3.0/DP PHY	USB3_OTG0_DP_TX_AVDD0V85, USB3_OTG0_DP_TX_DVDD0V85, USB3_OTG0_DP_TX_AVDD1V8	Not required to be powered
PCIE2.1/SATA3.1/USB3.0 Combo PHY	PCIE0_SATA0_AVDD0V85, PCIE0_SATA0_AVDD1V8, PCIE1_SATA1_USB3_OTG1_AVDD0V85, PCIE1_SATA1_USB3_OTG1_AVDD1V8	Not required to be powered
MIPI D/C Combo PHY	MIPI_DCPHY_AVDD, MIPI_DCPHY_AVDD1V2, MIPI_DCPHY_AVDD1V8	Not required to be powered
MIPI CSI PHY	MIPI_DPHY_CSI1/2_RX_AVDD0V75, MIPI_DPHY_CSI1/2_RX_AVDD1V8, MIPI_DPHY_CSI3/4_RX_AVDD0V75, MIPI_DPHY_CSI3/4_RX_AVDD1V8	Not required to be powered
HDMI/eDP TX PHY	HDMI_TX_EDP_TX_AVDDD0V75, HDMI_TX_EDP_TX_AVDDC0V75, HDMI_TX_EDP_TX_AVDDIO1V8, HDMI_TX_EDP_TX_AVDDCMN1V8	Not required to be powered

The RK3576 chip supports the low-power standby solution. When entering the standby mode, the following table shows the power supply and power-off conditions

Table 2-15 RK3576 power supply requirements in standby mode

Module	Power pins	Standby mode Supply Requirements
PLL	PLL_DVDD0V75, PLL_AVDD1V8	Not required to be powered
DDR PLL	DDRPHY_PLL_DVDD, DDRPHY_PLL_AVDD1V8	Not required to be powered
DDR_VDD	DDRPHY_DVDD	Not required to be powered
DDR_VDDQ_CK	DDRPHY_CK_VDDQ	Not required to be powered
DDR_VDDQ_CKE	DDRPHY_CKE_VDDQ	Must be powered
DDR_VDDQ	DDRPHY_VDDQ	Not required to be powered
CPU_BIG	CPU_BIG_DVDD	Not required to be powered
CPU_LIT	CPU_LIT_DVDD	Not required to be powered
GPU	GPU_DVDD	Not required to be powered
NPU	NPU_DVDD	Not required to be powered

Module	Power pins	Standby mode Supply Requirements
LOGIC	LOGIC_DVDD	Not required to be powered
LOGIC MEM	LOGIC_MEM_DVDD	Not required to be powered
PMU_0V75	PMU_LOGIC_DVDD0V75	Must be powered
OSC	OSC_AVDD1V8	Not required to be powered
UFS OSC	OSC_UFS_AVDD	Not required to be powered
MPHY(UFS2.0)	UFS_AVDD0V85, UFS_AVDD1V8	Not required to be powered
GPIO	PMUIO0_VCC1V8, PMUIO1_VCC	Must be powered
GPIO	VCCIO0_VCC1V8	Not required to be powered
GPIO	VCCIO1_VCC	Not required to be powered
GPIO	VCCIO3_VCC	Not required to be powered
GPIO	VCCIO7_VCC	Not required to be powered
GPIO	VCCIO2_VCC, VCCIO4_VCC, VCCIO5_VCC, VCCIO6_VCC	Not required to be powered
SARADC/TSADC/OTP	SARADC_AVDD1V8	Not required to be powered
OTP	OTP_DVDD0V75	Not required to be powered
USB2.0 PHY	USB2_OTG_DVDD0V75, USB2_OTG_AVDD1V8, USB2_OTG_AVDD3V3	Not required to be powered
USB3.0/DP PHY	USB3_OTG0_DP_TX_AVDD0V85, USB3_OTG0_DP_TX_DVDD0V85, USB3_OTG0_DP_TX_AVDD1V8	Not required to be powered
PCIE2.1/SATA3.1/USB3.0 Combo PHY	PCIE0_SATA0_AVDD0V85, PCIE0_SATA0_AVDD1V8, PCIE1_SATA1_USB3_OTG1_AVDD0V85, PCIE1_SATA1_USB3_OTG1_AVDD1V8	Not required to be powered
MIPI D/C Combo PHY	MIPI_DCPHY_AVDD, MIPI_DCPHY_AVDD1V2, MIPI_DCPHY_AVDD1V8	Not required to be powered
MIPI CSI PHY	MIPI_DPHY_CSI1/2_RX_AVDD0V75, MIPI_DPHY_CSI1/2_RX_AVDD1V8, MIPI_DPHY_CSI3/4_RX_AVDD0V75, MIPI_DPHY_CSI3/4_RX_AVDD1V8	Not required to be powered
HDMI/eDP TX PHY	HDMI_TX_EDP_TX_AVDDD0V75, HDMI_TX_EDP_TX_AVDDC0V75, HDMI_TX_EDP_TX_AVDDIO1V8, HDMI_TX_EDP_TX_AVDDCMN1V8	Not required to be powered

This standby scheme only supports IO interrupt wakeup for PMUIO0 and PMUIO1.

In standby mode, at least the following sets of power supplies should not be cut off (the following are power pin names):

- DDRPHY_CKE_VDDQ: Provides power for DDR self-refresh.
- PMU_LOGIC_DVDD0V75: Provides power for the logic of PMUIO0 & PMUIO1 power domains.

- PMUIO0_VCC1V8: Provides power for PMU0 operation; provides IO power to maintain output state and interrupt response for the PMUIO0 power domain.
- PMUIO1_VCC: Provides IO power to maintain output state and interrupt response for the PMUIO1 power domain.

In standby mode, to support USB HID device wakeup, OSC and USB2.0 PHY need to be powered:

Table 2: Standby power supply requirements for USB wakeup supported by RK3576.

Table 2-16 Standby power supply requirements for USB wakeup supported by RK3576

Module	Power pins	Standby mode Supply Requirements
DDR_VDDQ_CKE	DDRPHY_CKE_VDDQ	Must be powered
PMU_0V75	PMU_LOGIC_DVDD0V75	Must be powered
OSC	OSC_AVDD1V8	Must be powered
GPIO	PMUIO0_VCC1V8、PMUIO1_VCC	Must be powered
USB2.0 PHY	USB2_OTG_DVDD0V75, USB2_OTG_AVDD1V8, USB2_OTG_AVDD3V3	Must be powered

In standby mode, to support IO interrupt wakeup from VCCIO0, VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, and VCCIO7, the power supplies VCCIO0_VCC1V8, VCCIO1_VCC, VCCIO2_VCC, VCCIO3_VCC, VCCIO4_VCC, VCCIO5_VCC, VCCIO6_VCC, VCCIO7_VCC, LOGIC_DVDD, and LOGIC_MEM_DVDD must be retained.

In standby mode, if GPIOs are connected to peripherals that require continuous power, the power domain corresponding to the GPIOs needs to be kept powered. Additionally, if GPIOs need to maintain their pre-standby state (such as output high, internal input pull-up, etc.), the retention function of the GPIO domain needs to be enabled. Specific functions are described in the GPIO section.

For example, in the second-level standby mode, to support Wi-Fi wakeup, since LOGIC_DVDD is cut off, IOs in the VCCIO0~7 domains cannot support interrupts. Therefore, the wakeup-related pins for Wi-Fi are placed in the PMUIO0 domain, while the remaining control-related GPIOs are allocated to the VCCIO3 power domain.

During normal operation, on the RK3576 chip, PMUIO0_VCC1V8, PMU_LOGIC_DVDD0V75, VCCIO3_VCC, OSC_AVDD1V8, and LOGIC_DVDD/LOGIC_MEM_DVDD are all powered. The diagram below illustrates the normal operating state.

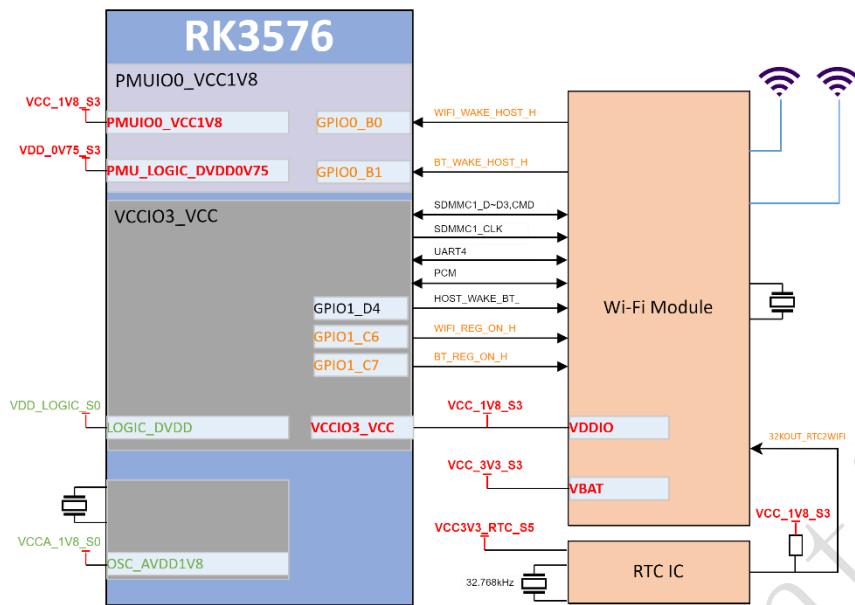


Figure 2-26 Wi-Fi working status diagram

After the system enters sleep mode, for scenarios where Wi-Fi functionality is still required, the Wi-Fi module needs to remain powered continuously. The control signals WIFI_REG_ON_H and BT_REG_ON_H for the Wi-Fi power need to be maintained at a high level. Therefore, before entering sleep mode, RK3576 needs to configure WIFI_REG_ON_H and BT_REG_ON_H to a high level. Then, in software, GPIO retention functionality should be enabled. Subsequently, power to OSC_AVDD1V8 and LOGIC_DVDD/LOGIC_MEM_DVDD should be disconnected. PMUIO0_VCC1V8, PMU_LOGIC_DVDD0V75, and VCCIO3_VCC need to remain powered. At this point, the control signals WIFI_REG_ON_H and BT_REG_ON_H for Wi-Fi will be maintained at a high level. The schematic for Wi-Fi operation after entering sleep mode is as follows, where the red power sources represent those maintained during standby, and the orange signals are those required for Wi-Fi operation during standby.

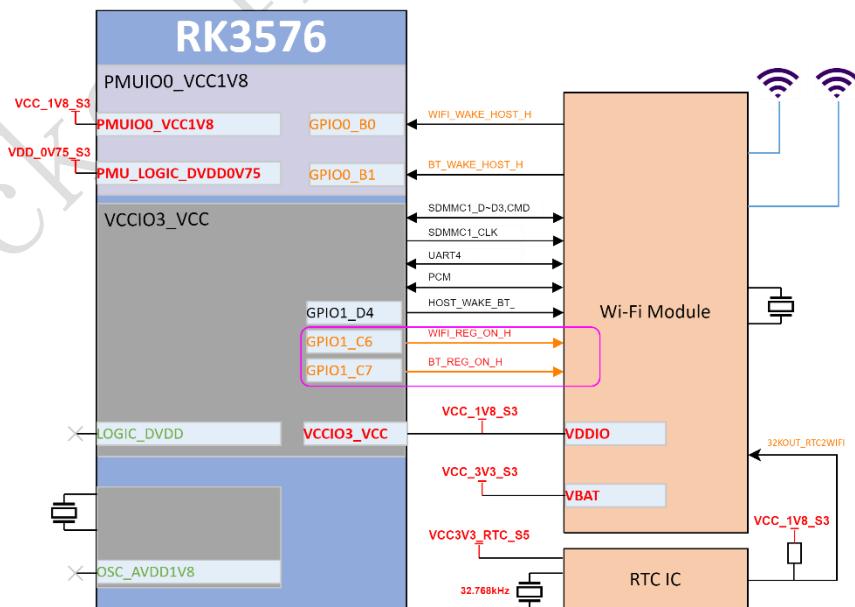


Figure 2-27 Wi-Fi sleep state diagram

If need support Wi-Fi wake up in standby mode, the following powers need to be keep powered.

Table 2-17 Standby power supply requirements for Wi-Fi wakeup supported by RK3576

Module	Power pins	Standby mode Supply Requirements
RK3576 DDR_VDDQ_CKE	DDRPHY_CKE_VDDQ	Must be powered
RK3576 PMU_0V75	PMU_LOGIC_DVDD0V75	Must be powered
RK3576 GPIO	PMUIO0_VCC1V8, PMUIO1_VCC, VCCIO3_VCC	Must be powered
Wi-Fi Module	VDDIO, VBAT	Must be powered
RTC IC	VCC_RTC	Must be powered

2.2.2.2 PLL power

The RK3576 chip's PLL include two parts, allocated as follows:

Table 2-18 RK3576 Internal PLL Introduction

Module	Power Supply	Standby Status
Within PMU unit	PLL_DVDD0V75, PLL_AVDD1V8	Power can be cut off
DDR PLL	DDRPHY_PLL_DVDD, DDRPHY_PLL_AVDD1V8	Power can be cut off

- PLL_DVDD0V75: Peak current 20mA
- PLL_AVDD1V8: Peak current 40mA
- DDRPHY_PLL_DVDD: Peak current 20mA
- DDRPHY_PLL_AVDD1V8: Peak current 30mA

It is recommended to use LDO for power supply:

- 0.75V/0.85V AC requirement: <20mV
- 1.8V AC requirement: <50mV

A stable PLL power supply helps improve chip stability. Decoupling capacitors should be placed close to the pins. The specific number and capacity of capacitors should refer to the reference design. Please do not adjust them.

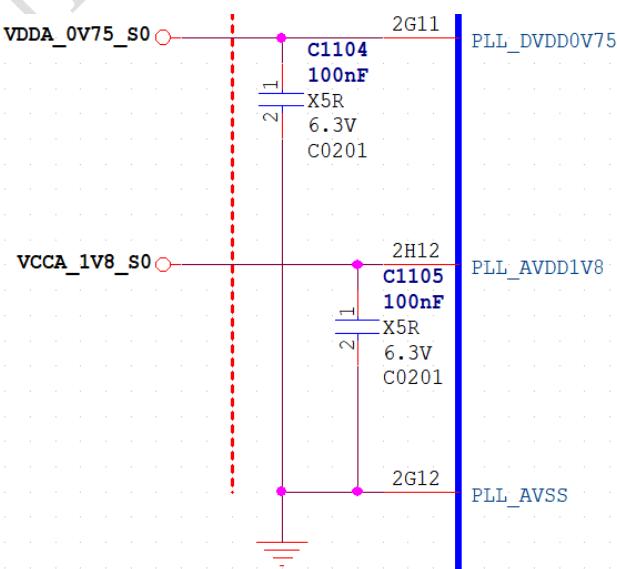


Figure 2-28 RK3576 SYS PLL power pin

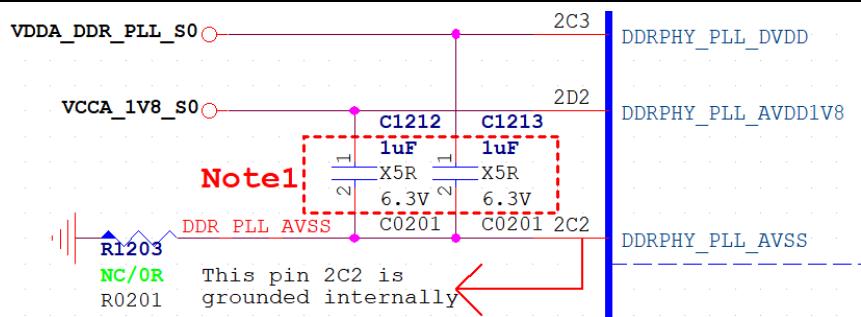


Figure 2-29 RK3576 DDR PLL power pin

2.2.2.3 OSC Power

The power supply OSC_1V8 of the RK3576 chip provides power to the crystal oscillator circuit.

- OSC_AVDD1V8: Peak current 10mA

It is recommended to use LDO for power supply:

- 1.8V AC requirement: <40mV

A stable OSC power supply helps improve chip stability. Decoupling capacitors should be placed close to the pins. The specific number and capacity of capacitors should refer to the schematic diagram. Please do not adjust them arbitrarily.

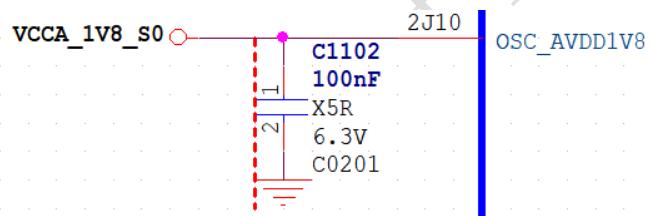


Figure 2-30 Power pins of the crystal oscillator circuit for the RK3576

2.2.2.4 PMU LOGIC Power

The power supply PMU_LOGIC_DVDD0V75 of the RK3576 chip provides power to the internal PMU unit's LOGIC, with a peak current of 30mA. Please do not omit the decoupling capacitors in the RK3576 reference design.

Both DC/DC and LDO can be used for power supply.

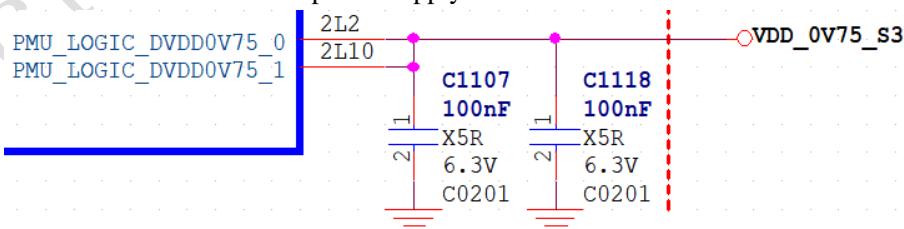


Figure 2-31 Power pins of PMU_LOGIC_DVDD0V75 for the RK3576

2.2.2.5 CPU_BIG_DVDD Power

The CPU_BIG_DVDD power supply of the RK3576 chip provides power to the four A72 cores. It is powered by the RK806S-5's BUCK1 or DC/DC power supply, supporting dynamic frequency and voltage regulation. The

default voltage upon power-up is 0.85V. The peak current can exceed 4A. Please do not omit the decoupling capacitors in the RK3576 chip reference design schematic.

During layout, place the capacitors indicated by the red box on the left side of the diagram on the backside of the RK3576 chip. The total capacitance for the CPU_BIG_DVDD power supply should be greater than 130uF to ensure that the power ripple is within +/-5%, avoiding excessive power ripple under heavy loads.

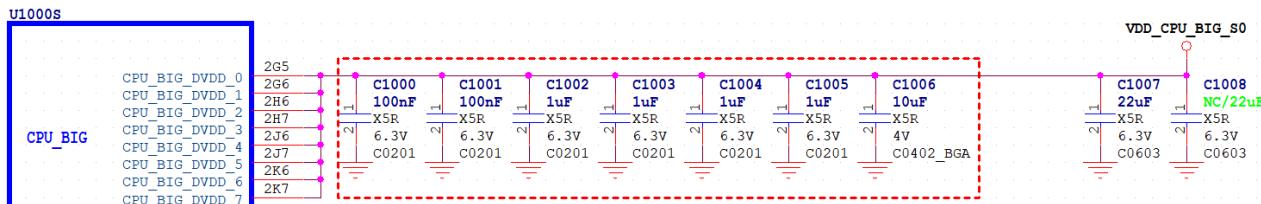


Figure 2-32 Power pins of CPU_BIG_DVDD for the RK3576

2.2.2.6 CPU_LIT_DVDD Power

The CPU_LIT_DVDD power supply of the RK3576 chip provides power to the internal four A53 cores. It is powered by the RK806S-5's BUCK3 power supply, supporting dynamic frequency and voltage regulation. The peak current can exceed 2.0A. Please do not omit the decoupling capacitors in the RK3576 chip reference design schematic.

During layout, place the capacitors indicated by the red box on the left side of the diagram under the RK3576 chip. The total capacitance for the CPU_LIT_DVDD power supply should be greater than 88uF to ensure that the power ripple is within +/-5%, avoiding excessive power ripple under heavy loads.

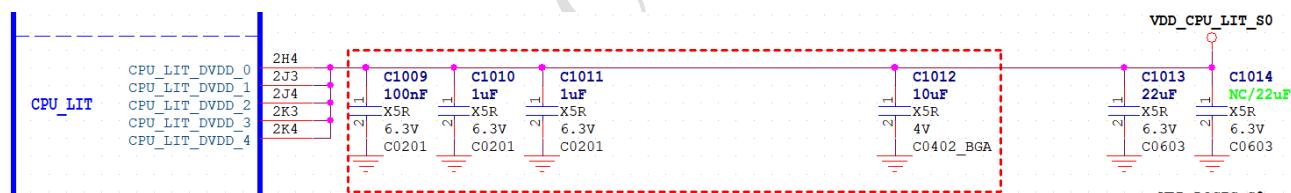


Figure 2-33 Capacitors for the CPU_LIT_DVDD power supply of the RK3576

2.2.2.7 GPU_DVDD Power

The GPU_DVDD power supply of the RK3576 chip provides power to the internal GPU unit. It is powered by the RK806S-5's BUCK5 and supports dynamic frequency and voltage regulation. The peak current can reach 3.0A. Please do not omit the decoupling capacitors in the RK3576 chip reference design schematic.

During layout, it is important to note that the capacitors indicated by the red box on the left side of the diagram should be placed under the RK3576 chip.

Near the output of the DCDC BUCK, there should be no main capacitor left. Instead, the main capacitor should be moved closer to the RK3576 chip, with a capacitance greater than 66uF, as shown in the red box on the right side of the diagram. This is to ensure that the power ripple is within +/-5%, avoiding excessive power ripple under heavy loads. The distance between the main capacitor and the RK3576 chip, copper trace width, and number of vias should comply with the constraints outlined in the PCB section.

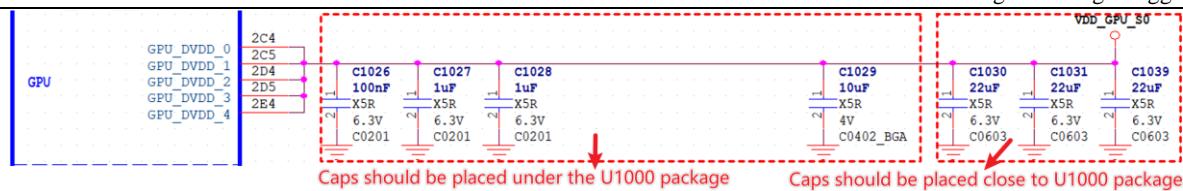


Figure 2-34 Power pins of GPU_DVDD for the RK3576

2.2.2.8 NPU Power

The NPU_DVDD power supply of the RK3576 chip provides power to the internal NPU unit. It is powered by the RK806S-5's BUCK2 and supports dynamic frequency and voltage regulation. The peak current can exceed 4A. Please do not omit the decoupling capacitors in the RK3576 chip reference design schematic.

During layout, please note that the capacitors indicated by the red box on the left side of the diagram should be placed under the RK3576 chip.

Near the output of the DCDC BUCK, there should be no main capacitor left. Instead, the main capacitor should be moved closer to the RK3576 chip, with a capacitance greater than 90uF, as shown in the red box on the right side of the diagram. This is to ensure that the power ripple is within +/-5%, avoiding excessive power ripple under heavy loads. The distance between the main capacitor and the RK3576 chip, copper trace width, and number of vias should comply with the constraints outlined in the subsequent PCB section.

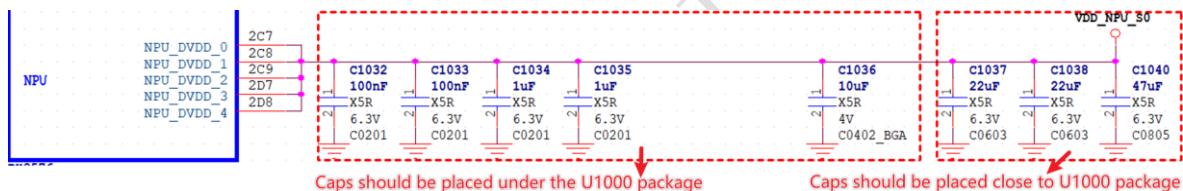


Figure 2-35 Power pins of NPU_DVDD for the RK3576

2.2.2.9 LOGIC_DVDD Power

The LOGIC_DVDD power supply of the RK3576 chip provides power to the internal logic unit. It is powered by the RK806S-5's BUCK7 and supports dynamic frequency and voltage regulation, with a default fixed voltage supply. The peak current can exceed 2.0A. Please do not omit the decoupling capacitors in the RK3576 chip reference design schematic.

During layout, place the capacitors indicated by the red box on the left side of the diagram under the RK3576 chip. The total capacitance for the LOGIC_DVDD power supply should be greater than 88uF to avoid excessive power ripple under heavy loads.

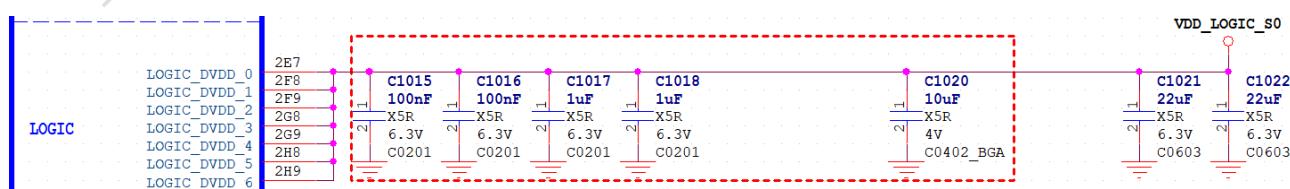


Figure 2-36 Power pins of LOGIC_DVDD for the RK3576

The LOGIC_MEM_DVDD power supply is the memory power supply for LOGIC_DVDD. By default, LOGIC_MEM_DVDD and LOGIC_DVDD are supplied together. For tablet solutions with batteries and less cost

sensitivity, consider adding a separate BUCK for LOGIC_MEM_DVDD, allowing independent DVFS for LOGIC_DVDD and LOGIC_MEM_DVDD to reduce power consumption. The current is TBD, and it is recommended to use BUCK for power supply.

The main requirements for the DC/DC BUCK are as follows:

- Output current greater than or equal to 2.0A.
- Output voltage accuracy requirement within $\pm 1.5\%$.
- BUCK transient response requirement: when the load jumps from 10% to 80% of the BUCK Max current, the slope is 1A/us, and the ripple requirement is within $\pm 5\%$.

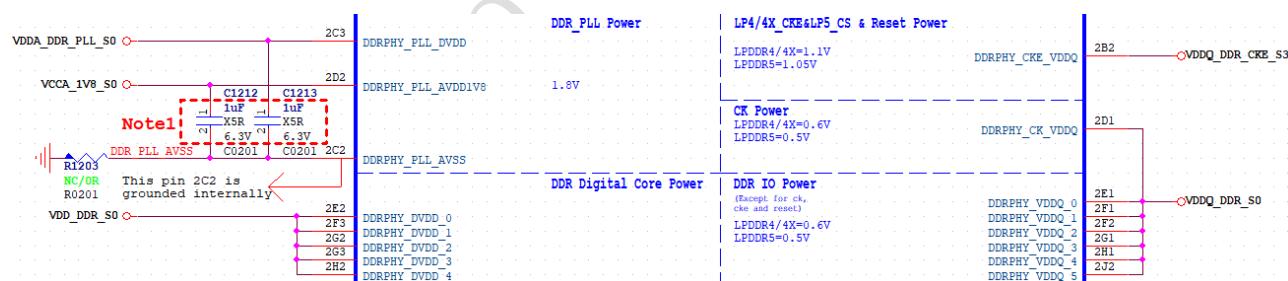
Place the capacitors indicated by the red box on the left side of the diagram under the RK3576 chip, directly below its pins.



Figure 2-37 Power pins of LOGIC_MEM_DVDD for the RK3576

2.2.2.10 DDR Power

The DDR PHY interface of the RK3576 chip supports LPDDR4/LPDDR4X/LPDDR5 voltage standards and has a total of 6 power supplies: DDRPHY_PLL_DVDD, DDRPHY_PLL_AVDD1V8, DDRPHY_DVDD, DDRPHY_CK_VDDQ, DDRPHY_CKE_VDDQ, and DDRPHY_VDDQ. Please refer to section **2.1.7.5 DDR Power Design and Power-Up Timing Requirements** for power supply details. When designing a product, confirm compliance with design requirements based on chip usage.



RK3576 chip to ensure that the power ripple is within 80mV and avoid excessive power ripple under heavy loads.

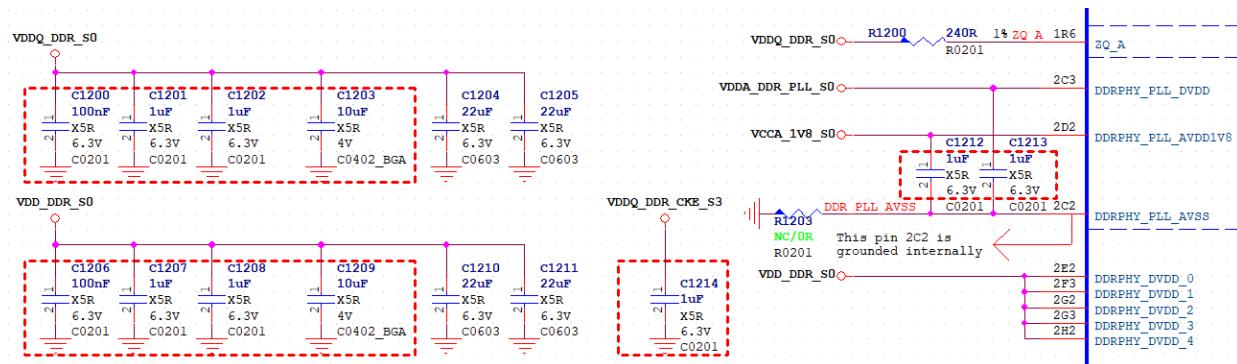


Figure 2-39 Filtering capacitors for DDR power supply of the RK3576

2.2.2.11 UFS (MPHY) Power

RK3576 has 1 UFS interface, refer to section **2.1.9 UFS circuit** for details.

The UFS_AVDD0V85 and UFS_AVDD1V8 power supplies provide power to the UFS MPHY. Please do not omit the decoupling capacitors in the RK3576 chip reference design schematic. When designing the power supply, it's necessary to reserve a 0603 0-ohm resistor.

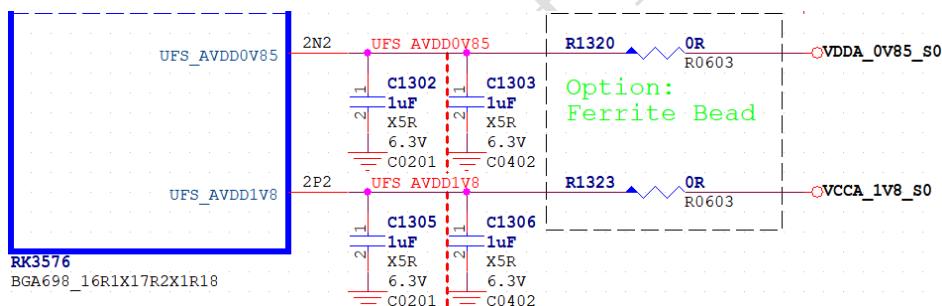


Figure 2-40 RK3576 USB2.0 PHY power pin

- UFS_AVDD0V85: peak current 120mA
 - UFS_AVDD1V8: peak current 40mA
- LDO is recommended for power supply:
- 0.85V AC requirement:<20mV
 - 1.8V AC requirement:<40mV

Stable power sources contribute to enhancing chip stability, and decoupling capacitors should be placed close to the pins. The specific number and capacity of capacitors should be referenced from the schematic diagram. Please avoid making arbitrary adjustments.

2.2.2.12 USB2.0 PHY Power

RK3576 features 2 USB2.0 interfaces. For specific connections, please refer to section **2.3.4 USB2/USB3 Circuit Unit Introduction**.

The power supplies USB2_OTG_DVDD0V75, USB2_OTG_AVDD1V8, and USB2_OTG_AVDD3V3 provide power to the USB2_OTG0 and USB2_OTG1 PHY. Please do not omit the decoupling capacitors in the

RK3576 chip reference design schematic.

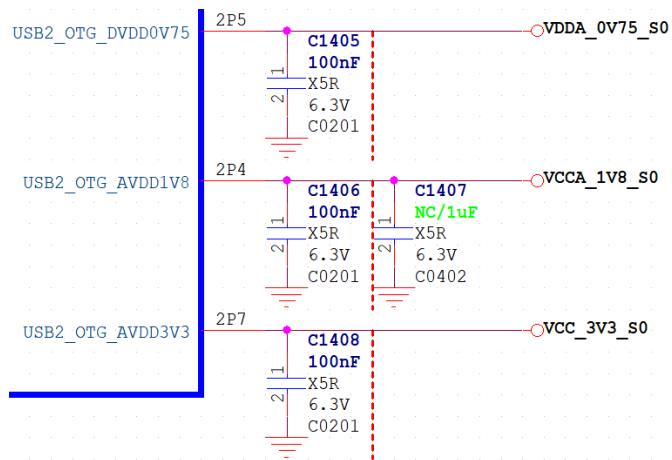


Figure 2-41 RK3576 USB2.0 PHY power pin

- USB2_OTG_DVDD0V75: Peak current 15mA
- USB2_OTG_AVDD1V8: Peak current 35mA
- USB2_OTG_AVDD3V3: Peak current 25mA

It is recommended to use LDO for power supply:

- 0.75V AC requirement: <25mV
- 1.8V AC requirement: <50mV
- 3.3V AC requirement: <200mV

Stable power sources contribute to enhancing chip stability, and decoupling capacitors should be placed close to the pins. The specific number and capacity of capacitors should be referenced from the schematic diagram. Please avoid making arbitrary adjustments.

Since the firmware of the RK3576 chip must be downloaded from the USB2_OTG0_DP/M interface, it is necessary to supply power to USB2_OTG_DVDD0V75, USB2_OTG_AVDD1V8, and USB2_OTG_AVDD3V3 during firmware burning.

2.2.2.13 USB3.0/DP1.4 Combo Power

RK3576 has 1 USB3.0/DP1.4 Combo PHY interface, with separate power supplies: USB3_OTG0_DP_TX_AVDD0V85, USB3_OTG0_DP_TX_DVDD0V85, and USB3_OTG0_DP_TX_AVDD1V8. Please do not omit the decoupling capacitors in the RK3576 chip reference design schematic.

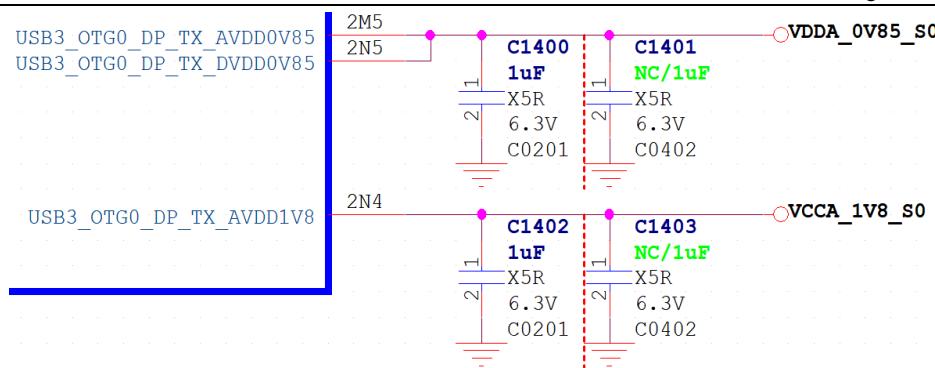


Figure 2-42 RK3576 USB30/DP1.4 Combo0 power pin

- USB3_OTG0_DP_TX_AVDD0V85 & USB3_OTG0_DP_TX_DVDD0V85: Peak current 220mA
- USB3_OTG0_DP_TX_AVDD1V8: Peak current 40mA

It is recommended to use LDO for power supply:

- 0.85V AC requirement:<20mV
- 1.8V AC requirement:<40mV

Stable power sources contribute to enhancing chip stability, and decoupling capacitors should be placed close to the pins. The specific number and capacity of capacitors should be referenced from the schematic diagram. Please avoid making arbitrary adjustments.

RK3576 supports firmware downloading via the USB3_OTG0_SS RX1P/N and USB3_OTG0_SS TX1P/N signals from the USB 3.2 Gen1x1 OTG0 interface. When upgrading firmware via USB3.0, USB3_OTG0_DP_TX_AVDD0V85, USB3_OTG0_DP_TX_DVDD0V85, and USB3_OTG0_DP_TX_AVDD1V8 must be powered.

2.2.2.14 PCIe/SATA/USB3 Combo PHY Power

RK3576 has 1 PCIe2.1/SATA3.1 Combo PHY interface and 1 PCIe2.1/SATA3.1/USB3.0 Combo PHY interface. There are a total of 4 power supplies: PCIE0_SATA0_AVDD0V85, PCIE0_SATA0_AVDD1V8, PCIE1_SATA1_USB3_OTG1_AVDD0V85, and PCIE1_SATA1_USB3_OTG1_AVDD1V8. Please do not omit the decoupling capacitors in the RK3576 chip reference design schematic. Capacitors on the left side of the red dashed line in the diagram need to be placed close to the chip pins.

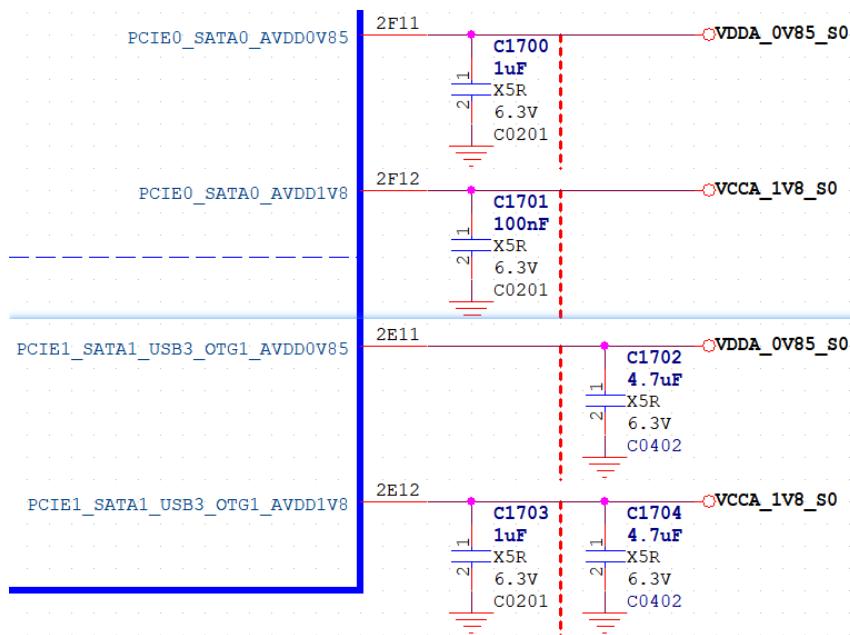


Figure 2-43 Power pins of RK3576 PCIe2.1 Combo PHY

- PCIE0_SATA0_AVDD0V85、PCIE1_SATA1_USB3_OTG1_AVDD0V85: Peak current 100mA
- PCIE0_SATA0_AVDD1V8、PCIE1_SATA1_USB3_OTG1_AVDD1V8: **Peak current 100mA**

It is recommended to use LDO for power supply:

- 0.85V AC requirement:<20mV
- 1.8V AC requirement:<50mV

Stable power sources contribute to enhancing chip stability, and decoupling capacitors should be placed close to the pins. The specific number and capacity of capacitors should be referenced from the schematic diagram. Please avoid making arbitrary adjustments.

The power supplies for PCIe2.1/SATA3.1 Combo PHY and PCIe2.1/SATA3.1/USB3.0 Combo PHY are independent. Unused PHY power supply routes (0V85 and 1V8) can be left unpowered, and the power supply pins should be grounded.

2.2.2.15 MIPI DPHY CSI RX PHY Power

RK3576 has 2 MIPI DPHY CSI RX interfaces, with a total of 4 power supplies:

MIPI_DPHY_CSI1/2_RX_AVDD0V75, MIPI_DPHY_CSI1/2_RX_AVDD1V8,

MIPI_DPHY_CSI3/4_RX_AVDD0V75, and MIPI_DPHY_CSI3/4_RX_AVDD1V8. Please do not omit the decoupling capacitors in the RK3576 chip reference design schematic. Capacitors on the left side of the red dashed line in the diagram should be placed under the RK3576 chip, and capacitors on the right side should be placed as close to the chip as possible.

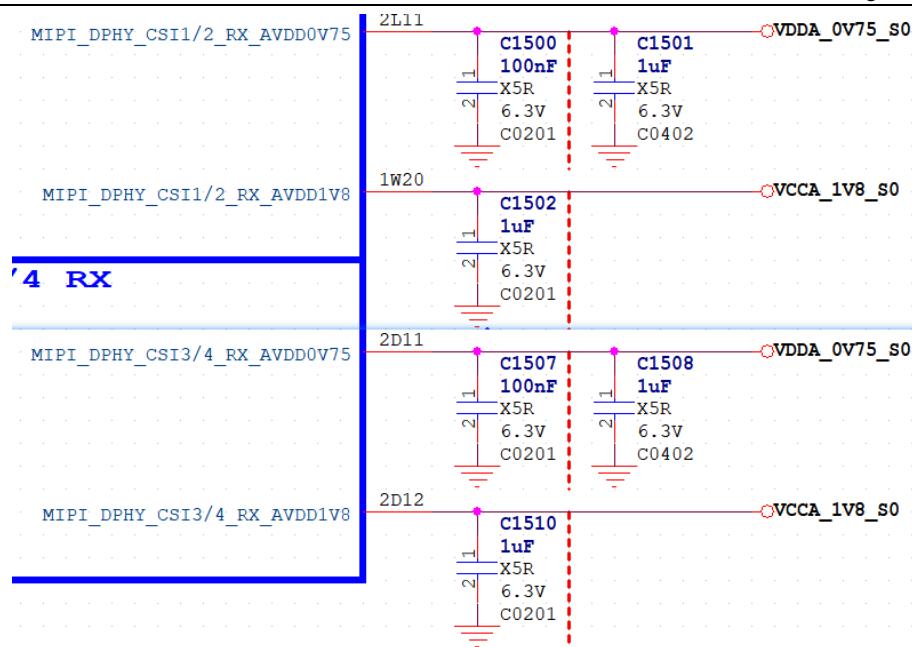


Figure 2-44 RK3576 MIPI DPHY CSI1/2/3/4 RX PHY power pin

- MIPI_DPHY_CSI1/2_RX_AVDD0V75、MIPI_DPHY_CSI3/4_RX_AVDD0V75: peak current 12mA
- MIPI_DPHY_CSI1/2_RX_AVDD1V8、MIPI_DPHY_CSI3/4_RX_AVDD1V8: peak current 3mA

It is recommended to use LDO for power supply:

- 0.75V AC requirement:<25mV
- 1.8V AC requirement:<50mV

Stable power sources contribute to enhancing chip stability, and decoupling capacitors should be placed close to the pins for effective operation. The specific number and capacity of capacitors should be referenced from the schematic diagram, and please refrain from making arbitrary adjustments.

For the two MIPI DPHY CSI RX PHY interfaces, if a particular function is not in use, the power supply to the inactive PHY can be disconnected. It can be either grounded or left floating.

2.2.2.16 MIPI DC PHY CSI RX Power

RK3576 features 1 MIPI DC PHY CSI RX interface. The power supplies MIPI_DC PHY_AVDD, MIPI_DC PHY_AVDD1V2, and MIPI_DC PHY_AVDD1V8 are for supplying power to the MIPI DC PHY. Please do not omit the decoupling capacitors in the RK3576 chip reference design schematic. Capacitors on the left side of the red dashed line in the diagram should be placed under the RK3576 chip, and capacitors on the right side should be placed as close to the chip as possible.

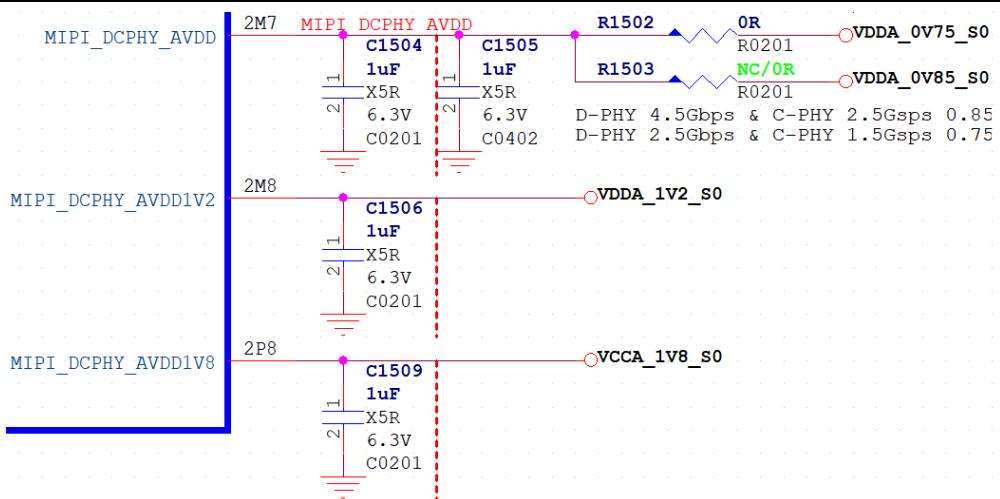


Figure 2-45 RK3576 MIPI D/C Combo PHY0 power pin

- MIPI_DCPHY_AVDD: peak current 65mA
- MIPI_DCPHY_AVDD1V2: peak current 2mA
- MIPI_DCPHY_AVDD1V8: peak current 20mA

It is recommended to use LDO for power supply:

- 0.75/0.85V AC requirement:<20mV
- **1.2V AC requirement:<20mV**
- 1.8V AC requirement:<50mV

Stable power sources contribute to enhancing chip stability, and decoupling capacitors should be placed close to the pins for effective operation. The specific number and capacity of capacitors should be referenced from the schematic diagram, and please refrain from making arbitrary adjustments.

If none of the functions of the MIPI D/C PHY are used, then MIPI_DCPHY_AVDD, MIPI_DCPHY_AVDD1V2, and MIPI_DCPHY_AVDD1V8 can be left unpowered, and the power supply pins should be left floating.

2.2.2.17 HDMI2.1/eDP1.3 Combo Power

RK3576 has 1 HDMI2.1/eDP Combo PHY interface. The power supplies HDMI_TX_EDP_TX_AVDD0V75, HDMI_TX_EDP_TX_AVDDC0V75, HDMI_TX_EDP_TX_AVDDIO1V8, and HDMI_TX_EDP_TX_AVDDCMN1V8 are for supplying power to the HDMI2.1/eDP Combo PHY. Please do not omit the decoupling capacitors in the RK3576 chip reference design schematic.

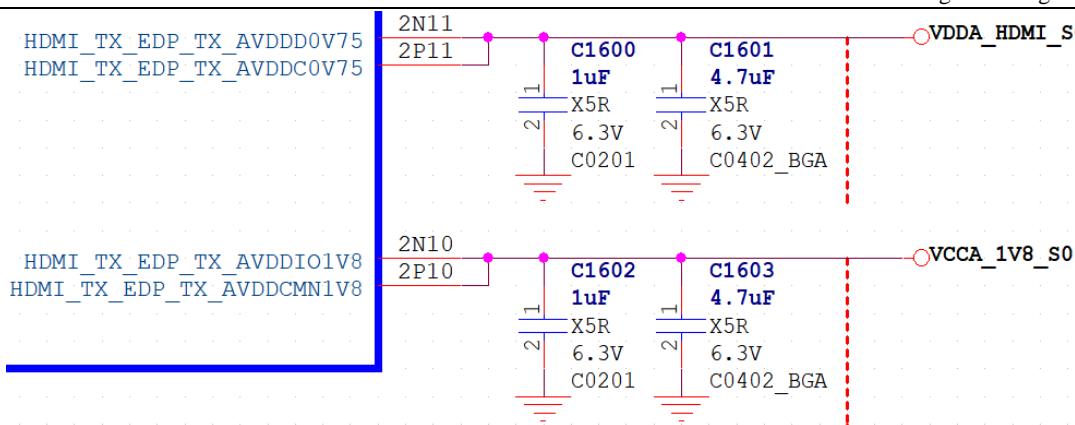


Figure 2-46 RK3576 HDMI2.1/EDP Combo PHY power pin

- HDMI_TX_EDP_TX_AVDDDD0V75: peak current 280mA
- HDMI_TX_EDP_TX_AVDDC0V75: peak current 1mA
- HDMI_TX_EDP_TX_AVDDIO1V8: peak current 160mA
- HDMI_TX_EDP_TX_AVDDCMN1V8: peak current 160mA

It is recommended to use LDO for power supply:

- 0.75V AC requirement:<20mV
- 1.8V AC requirement:<30mV

Stable power sources contribute to enhancing chip stability, and decoupling capacitors should be placed close to the pins for effective operation. The specific number and capacity of capacitors should be referenced from the schematic diagram, and please refrain from making arbitrary adjustments.

If the HDMI2.1/eDP1.3 TX function is not used, then HDMI_TX_EDP_TX_AVDDDD0V75, HDMI_TX_EDP_TX_AVDDC0V75, HDMI_TX_EDP_TX_AVDDIO1V8, and HDMI_TX_EDP_TX_AVDDCMN1V8 can be left unpowered. They can either be grounded or left floating.

2.2.2.18 SARADC/OTP Power

RK3576 has 1 SARADC with 8 input channels, and 1 OTP.

SARADC_AVDD1V8 supplies power to the SARADC, TSADC, and OTP. Please do not omit the decoupling capacitors in the RK3576 chip reference design schematic.

- SARADC_AVDD1V8: peak current 30mA

It's recommended to use LDO for power supply:

- 1.8V AC requirement:<50mV

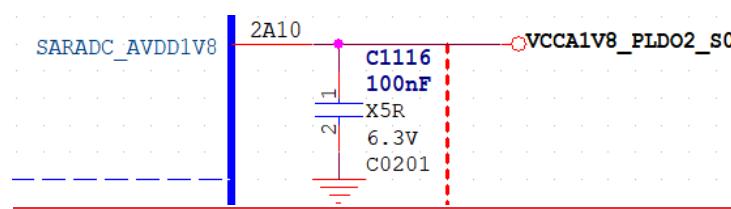


Figure 2-47 RK3576 SARADC power pin

OTP_DVDD0V75 is for supplying power to the OTP. Please do not omit the capacitors in the RK3576 chip reference design schematic.

- OTP_DVDD0V75: Peak current 1mA

It can use either an LDO or DC/DC for supplying power to the OTP.

Stable power sources contribute to enhancing chip stability, and decoupling capacitors should be placed close to the pins for effective operation. Please refer to the schematic diagram for specific capacitor numbers and capacities, and avoid making arbitrary adjustments.

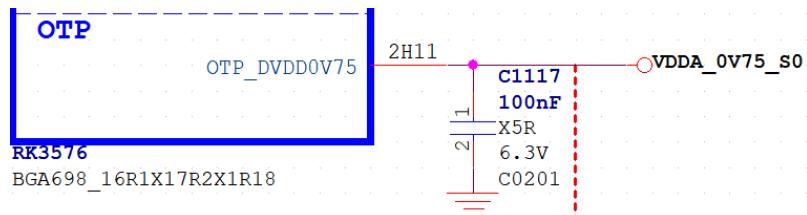


Figure 2-48 RK3576 SARADC power pin

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2.2.3 RK806S-5 Scheme Introduction

2.2.3.1 RK806S-5 Typical application diagram

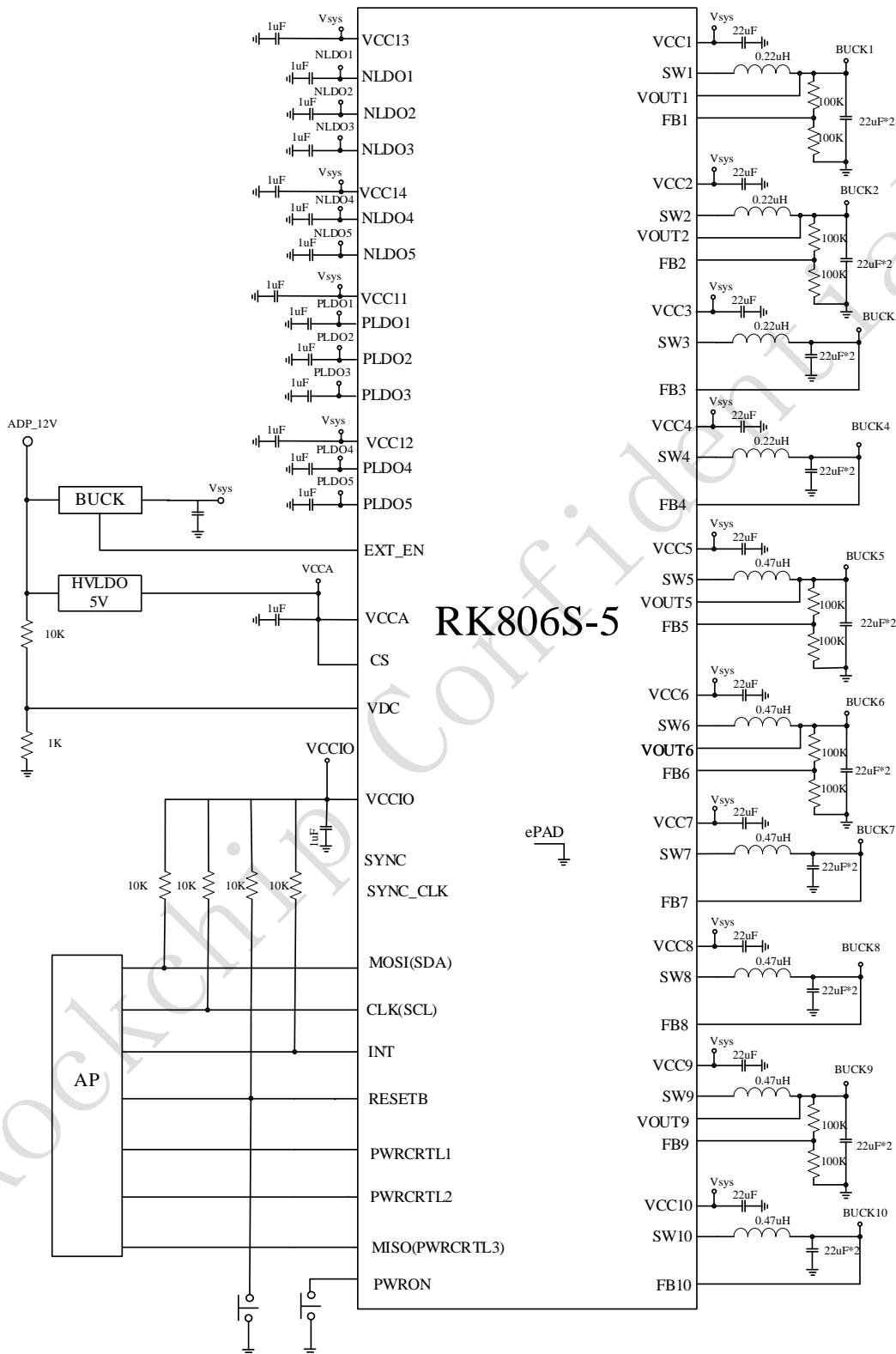


Figure 2-49 RK806S-5 Typical application diagram

2.2.3.2 RK806S-5 Features

- Input range: 2.7V-5.5V;
- Ultra-low standby current: 10uA;
- Supports two communication protocols: I2C or SPI;
- Ripple control architecture provides excellent transient response;
- Output levels programmable via I2C or SPI;
- Selectable power-on sequencing control;
- Power channels:
 - BUCK1: 0.5V-3.4V output, max 6.5A;
 - BUCK2/3/4: 0.5V-3.4V output, max 5A;
 - BUCK5/6/7/8/9/10: 0.5V-3.4V output, max 3A;
 - NLDO1/2/5: 0.5V-3.4V output, max 300mA;
 - NLDO3/4: 0.5V-3.4V output, max 500mA;
 - PLDO1/4: 0.5V-3.4V output, max 500mA;
 - PLDO2/3/5/6: 0.5V-3.4V output, max 300mA.
- External BUCK enable control;
- Package: 7mm x 7mm QFN68.

2.2.3.3 RK806S-5 Considerations

- In the application with RK3576, RK806S-5 defaults to the I2C working mode. During power-up, the CS pin needs to be connected to VCCA. The following schematic diagram illustrates the working mode of the I2C connection.

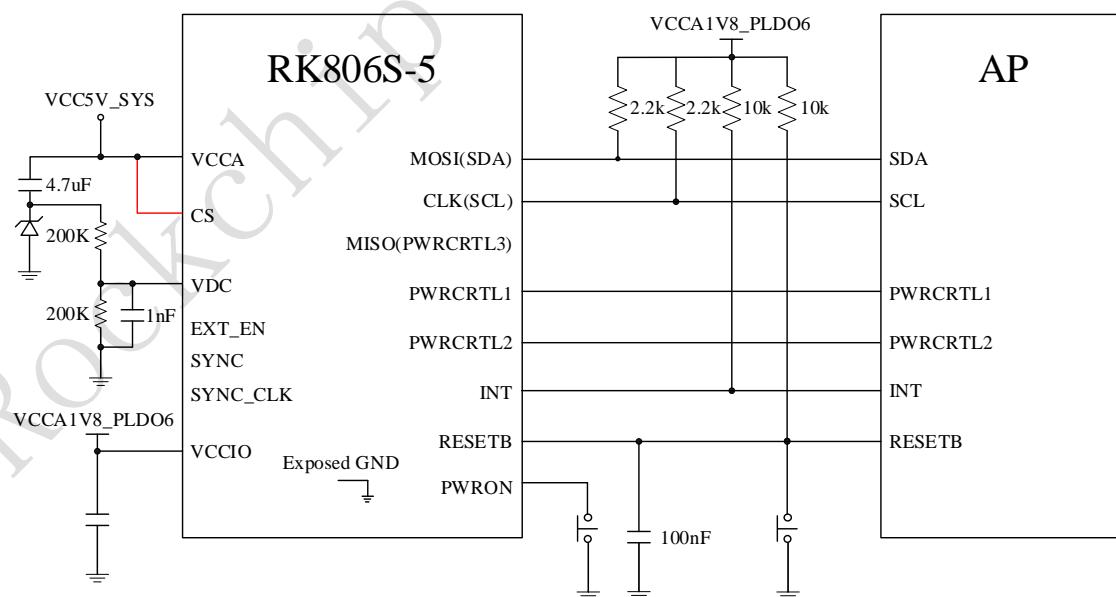


Figure 2-50 RK806S-5 Typical Application in I2C Mode

- VCCA (Pin21) of RK806S-5: This pin provides power to the internal digital logic and some analog controls of the RK806S-5 chip. It is required that the supply voltage for this pin is either the highest among all supply pins of RK806S-5 or greater than Vmax-0.3V. Therefore, VCCA must be powered up first or

simultaneously with other power sources. It is not allowed for other power sources to be powered up before VCCA.

- RESETB (Pin40) of RK806S-5: This pin outputs the reset signal to the host controller and also serves as an external reset signal input after the reset is pulled high. Since it has an input function, a 100nF capacitor is recommended in the application to enhance noise immunity. However, the total capacitance on the line should not exceed 0.3uF.
- PLDO6 of RK806S-5: It supplies power to the VCCIO of CS|MOSI(SDA)|CLK(SCL)|MISO(SLEEP3)|SLEEP2|SLEEP1 IOs. It is advisable to power the GPIO power domain connected to these IOs with the same power supply to achieve level matching and synchronous power-up and power-down.
- Pin32 (VDC) of RK806S-5: This pin is used for automatic power-on with an external power supply. The recognition threshold of VDC pin for high level is 0.8V, and it is recommended to be greater than 1V and less than or equal to VCCA voltage. When the power supply meets the requirements (VCCA\VCC1\VCC2 greater than 3.0V), if VDC detects a high level, RK806S-5 will power on. During high level on VDC, RK806S-5 cannot be shut down (if automatic power-on by adapter and hardware shutdown function is required, an RC delay needs to be added to VDC pin as shown in the following figure).

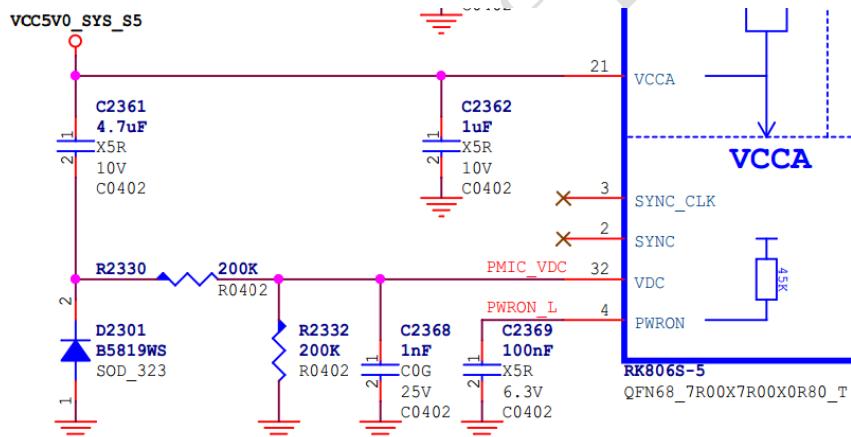


Figure 2-51 RK806S-5 VDC Pin

- Pin4 (PWRON) of RK806S-5: It connects to the power-on button. There is a 45Kohm resistor internally pulled up to VCCA on this pin. When pulled low for 20ms in the shutdown state, if the voltage meets the power-on conditions, the device will power on (Note: RK806S-5 defaults to 20ms). If pulled low during power-on, short press/long press interrupts will be sent to the host controller. If pulled low for more than 6 seconds, it will force a shutdown (6s\8s\10s\12s are optional via software).
- RK806S-5 has three PWRCTRL pins, namely PIN16\61\62 (PWRCTRL3\2\1). Except for PWRCTRL3 which is multiplexed with MISO, the rest have the same functions. These pins can control RK806S-5 to enter or exit SLEEP mode, and can also be used to control BUCK or LDO for rapid voltage regulation or switch output by configuring corresponding registers.
- VOUT pin of RK806S-5 BUCK: VOUT serves as both the ripple detection input of the COT architecture BUCK and the feedback voltage input. It is generally directly connected to the positive terminal of the output capacitor (VOUT line should be avoided from interference by other signals as much as possible).

- FB pin of RK806S-5 BUCK: BUCK1\2\5\6\9 have an additional FB pin compared to other BUCKs. BUCKs with FB pin can select VOUT pin or FB pin as the voltage feedback pin according to the timing. The reference voltage of FB is 0.5V. When using the FB pin, the voltage divider resistance is recommended to be between 10K ohm and 1M ohm. The calculation formula is $V_{out} = (R1/R2+1) * 0.5V$. Note: The default enabling of FB is set by the power-on sequence (OTP). Only power supplies where the default voltage needs to be changed (such as DDRPHY_DVDD) will use FB to adjust the default voltage.

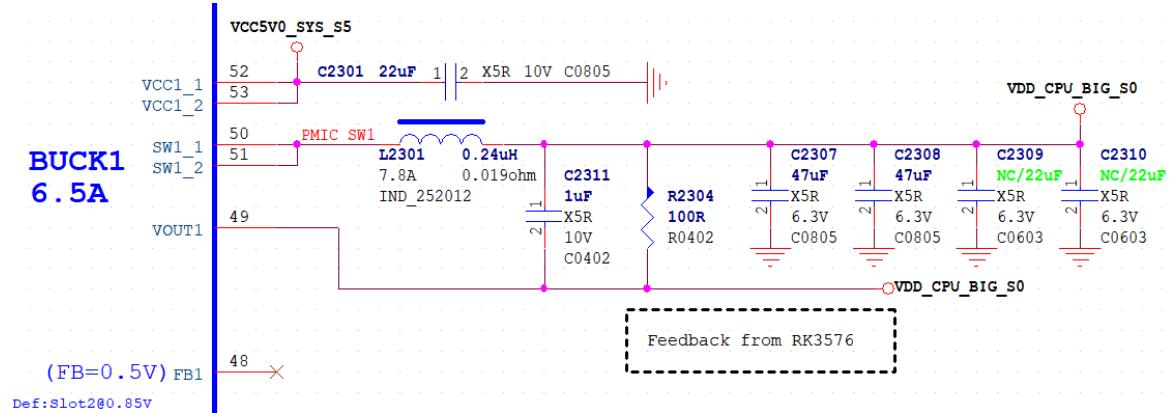


Figure 2-52 RK806S-5 BUCK1

- BUCK1 of RK806S-5: The maximum output full load current is 6.5A. The input capacitance is 22uF, the output capacitance is 66uF, the switching frequency is 2MHz (typical), and the inductance is 0.24uH. It is recommended to select the input and output capacitors with twice the working voltage, and the inductance ripple current should be around 30% of the full load current (above 7.8A for saturation current). The DCR is less than 15m ohm (for better conversion efficiency, it is recommended to select around 10m ohm).
- BUCK2\3\4 of RK806S-5: The maximum output full load current is 5A. The input capacitance is 22uF, the output capacitance is 66uF, the switching frequency is 2MHz (typical), and the inductance is 0.24uH. It is recommended to select the input and output capacitors with twice the working voltage, and the inductance ripple current should be around 30% of the full load current (above 6.5A for saturation current). The DCR is less than 20m ohm (for better conversion efficiency, it is recommended to select around 15m ohm).
- BUCK5\6\7\8\9\10 of RK806S-5: The maximum output full load current is 3A. The input capacitance is 10uF, the output capacitance is 44uF, the switching frequency is 2MHz (typical), and the inductance is 0.47uH. It is recommended to select the input and output capacitors with twice the working voltage, and the inductance ripple current should be around 30% of the full load current (above 4A for saturation current). The DCR is less than 40m ohm (for better conversion efficiency, it is recommended to select around 20m ohm).
- PLDO of RK806S-5: Except for PLDO6 (VCCIO), which also provides three PLDOs (PLDO1\PLDO4) with a load capacity of 300mA and two PLDOs (PLDO2\PLDO5) with a load capacity of 500mA. The output capacitance of each PLDO is guaranteed to be above 2.2uF. VCC11 is the power input pin for PLDO1\PLDO2\PLDO3, and VCC12 is the power input pin for PLDO4\PLDO5. To ensure that PLDO can start up normally and stabilize the voltage, the minimum input voltage of VCC11 and VCC12 is the highest output voltage of the lower LDO + 0.2V, and the minimum input voltage is not less than 2.0V.

- NLDO of RK806S-5: NLDO refers to LDO with N-channel adjustment tubes. Its characteristic is that the input voltage of the adjustment tube can be very low (no PLDO requires a minimum input voltage of 2.0V), only needs to be greater than 0.2V of the output voltage. However, the maximum output voltage must be 1.5V lower than VCCA (Pin21) voltage. Similarly, there are three NLDOs (NLDO1\NLDO3\NLDO4) with a load capacity of 300mA and two NLDOs (NLDO2\NLDO5) with a load capacity of 500mA. The output capacitance of each NLDO is guaranteed to be above 2.2uF. VCC13 is the power input pin for NLDO1\NLDO2\NLDO3, and VCC14 is the power input pin for NLDO4\NLDO5.
- RK806S-5 Power-On and Power-Off Conditions:
 - VDC Power-On Process:
 - ◆ VCCA has power.
 - ◆ VDC pin is higher than 0.8V, with a recommended value of around 1.0V.
 - ◆ EXT_EN outputs a high level.
 - ◆ Within 100mS after EXT_EN outputs a high level, the voltages of VCCA\VCC1\VCC2 exceed the VB_LO_SEL voltage (RK806S-5 value is 3.0V). Otherwise, the device will not power on.
 - ◆ Start the power-on process, with each DC/DC and LDO powered up according to the sequence.
 - ◆ After powering on, VDC can be pulled low or kept high without affecting the power-on state.
 - Power Key Power-On Process:
 - ◆ VCCA has power.
 - ◆ The voltage of the PWRON pin is pulled from a high level (greater than VCCA0.7) to a low level (less than VCCA0.3V), lasting more than 20ms (20/500ms OTP setting).
 - ◆ EXT_EN outputs a high level.
 - ◆ Within 100mS after EXT_EN outputs a high level, the voltages of VCCA\VCC1\VCC2 exceed 3.0V. Otherwise, the device will not power on.
 - ◆ Start the power-on process, with each DC/DC and LDO powered up according to the sequence.
 - Shutdown Methods:
 - ◆ The voltages of VCC9\VCC1\VCC2 are lower than the undervoltage setting voltage VB_UV_SEL.
 - ◆ The voltages of VCC9\VCC1\VCC2 are lower than the undervoltage warning value VB_LO_SEL, and VB_LO_ACT=0.
 - ◆ Write DEV_OFF=1 via I2C or SPI command.
 - ◆ Shutdown due to over-temperature protection (140/160 degrees).
 - ◆ Long press of the Power Key for more than 6 seconds forces a shutdown (6s/8s/10s/12s configurable).
 - ◆ Another PMIC pulls down the SYNC and RESET pins to initiate a coordinated shutdown.
- For detailed design specifications of RK806S-5, please refer to the relevant RK PMIC design document "AN_RK806_V1.0".

2.2.4 RK3576 with RK806S-5 PMIC Power Supply Scheme Introduction

2.2.4.1 RK3576+RK806S-5 Power Tree (AIOT REF)

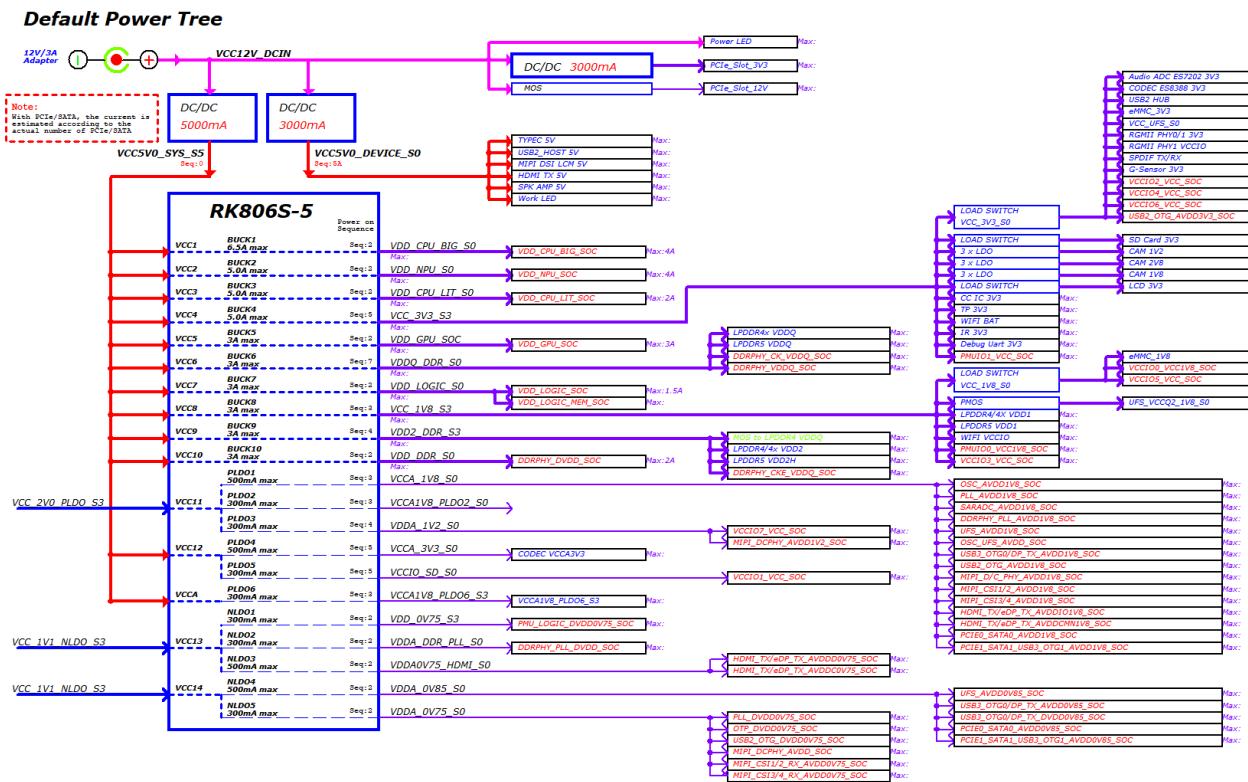


Figure 2-53 RK3576+RK806S-5 power tree

2.2.4.2 RK806S-5 Power-On Sequence

The power-on sequence inside RK806S-5 is fixed and cannot be replaced with other models like RK806-2.

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC5V0_SYS_S5	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5A	0.9V	ON	0.9V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	5A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCC_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Figure 2-54 RK3576+RK806S-5 power-on sequence

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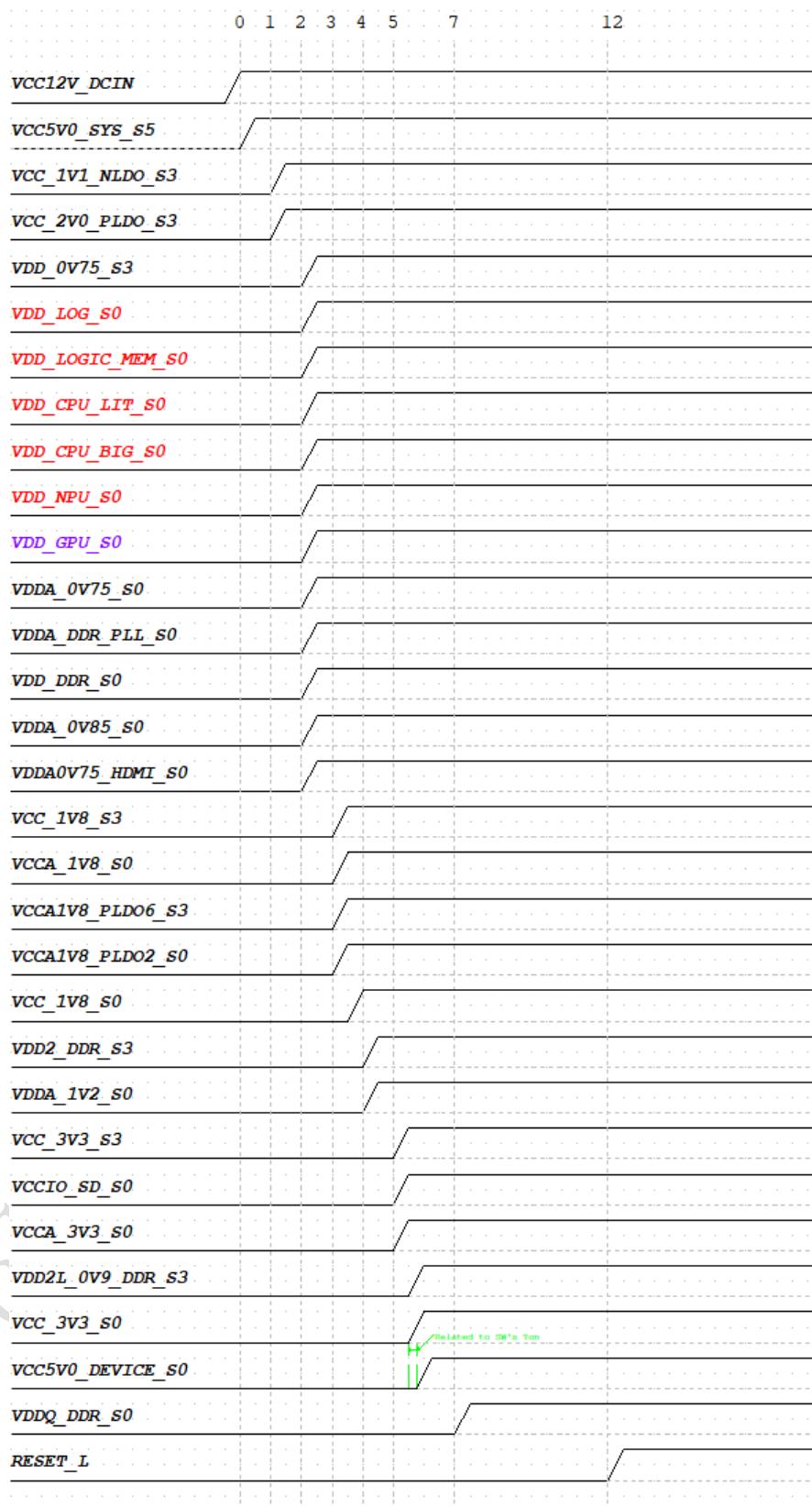


Figure 2-55 RK3576+RK806S-5 power-on sequence figure

2.2.4.3 Core Module Peak Current Table

The following data represents the peak currents of each core module during operation, provided for evaluating

power schemes and PCB layout.

Please note: The peak currents of individual modules cannot simply be summed up as the SoC's peak current. To assess thermal solutions, evaluate the average current consumption based on actual operating scenarios.

Table 2-19 RK3576 peak current

Maximum Current of RK3576 Core Modules for Reference					
Core Module Limit Current	Power Network	Voltage (V)	Peak Current (A)	Peak Power (W)	Remarks
	VDD_CPU_BIG	0.950	4.00	3.80	频率 2300MHz
	CPU_LIT_DVDD_S0	0.900	2.00	1.80	频率 2200MHz
	VDD_LOG_S0	0.750	2.00	1.5	
	GPU_DVDD_S0	0.850	3.00	2.55	频率 950MHz
	NPU_DVDD_S0	0.800	4.00	3.20	频率 1000MHz
	DDRPHY_DVDD_S0	0.850	2.00	1.70	频率 2133MHz

2.3 Functional Interface Design Guidelines

2.3.1 SDMMC

The RK3576 integrates two SDMMC controllers, both of which support the SDIO 3.0 protocol and MMC V4.51 protocol.

- 4-wire data bus width.
- Supports SDR104 mode, with a maximum frequency of up to 200MHz.

2.3.1.1 SDMMC0 Interface

- The SDMMC0 interface is multiplexed in the VCCIO1 power domain.
- SDMMC0 supports System Boot and is by default assigned for SD card functionality. It supports firmware upgrade via SD card when EMMC/UFS is empty, and also supports firmware upgrade of EMMC/UFS via SD card after EMMC/UFS is booted;
- SDMMC0 is multiplexed with JTAG and other functions, with the function selection controlled via the SDMMC_DETEN status. Refer to section 2.1.6 for details.
- VCCIO1 power supply requires external 3.3V or 1.8V.
- When using an SD card:
 - If only supporting SD2.0 mode, 3.3V power supply is sufficient.
 - If supporting SD3.0 mode compatible with SD2.0 mode, the power supply voltage needs to switch to 1.8V after negotiating SD3.0 mode with the SD card. PLDO5 of RK806S-5 separately supplies power to VCCIO1 to facilitate this process.
- When connecting an SDIO device, supply 1.8V or 3.3V based on the peripheral and actual operating mode.

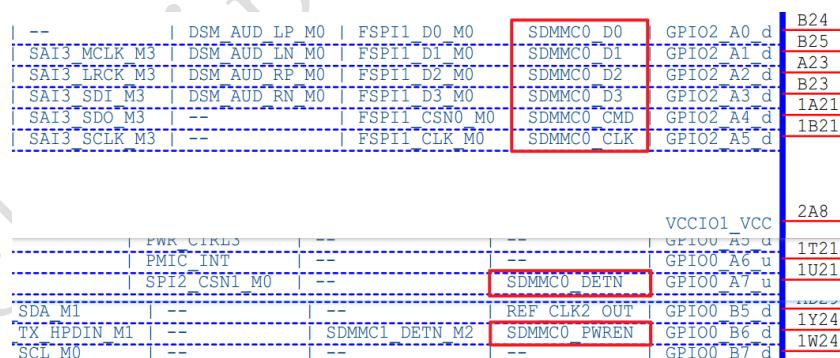


Figure 2-56 RK3576 SDMMC0 interface pin

- When implementing board-to-board connections via connectors, it is recommended to series-connect resistors with a certain resistance value (between 22ohm and 100ohm, depending on SI testing requirements), and to reserve TVS devices.
- When using an SD card, pay attention to the following:
 - (1) Ensure that the VDD pin of the SD card is powered at 3.3V, with decoupling capacitors not omitted and placed close to the card slot during layout.
 - (2) Series-connect 22ohm resistors to SDMMC_D[3:0], SDMMC_CMD, SDMMC_CLK, and 100ohm

resistors to SDMMC_DETIN.

- (3) Place ESD devices at the position of SDMMC_D[3:0], SDMMC_CMD, SDMMC_CLK, and SDMMC_DETIN signals in the SD card location. The parasitic capacitance of ESD devices must be less than 1pF to support SD3.0 mode. If only SD2.0 mode is needed, the parasitic capacitance of ESD devices can be relaxed to 9pF.
- (4) When using SDMMC0's probe BOOT gear, the GPIO0_B6 where SDMMC0_PWREN is located will output a high level, so SDMMC0_PWREN is directly used to control the SD card power supply Load switch's enable, and doesn't need to be inverted by the transistor. Note that if SDMMC0 detects SDMMC0_PWREN pull high process will affect the peripheral state, then you need to be careful not to use this IO to control sensitive peripherals, for example, when SARADC_IN0_BOOT configured as Config8 gear, UFS startup, will also go to detect the SD card, SDMMC0_PWREN will be pulled up a little. At this time, if there is no SD card on the hardware, you need to be careful not to use this IO to control sensitive peripherals, it is recommended that when you do not need an SD card, the SARADC_IN0_BOOT configuration selects Config7 instead of Config8;
- (5) Pay attention to the design of SD card power supply to ensure that the SD card power-off speed is fast enough to avoid incomplete power-off and re-powering when rapidly inserted and removed, leading to logic confusion in the SD card.
- (6) For low-power scenarios, when an SD card is connected, SDMMC0_DETIN will remain low, causing relatively high current consumption. For customers sensitive to power consumption, it is recommended to configure the internal SDMMC0_DETIN pin of the SoC as high-impedance in software, and increase the external pull-up resistor to 100k.

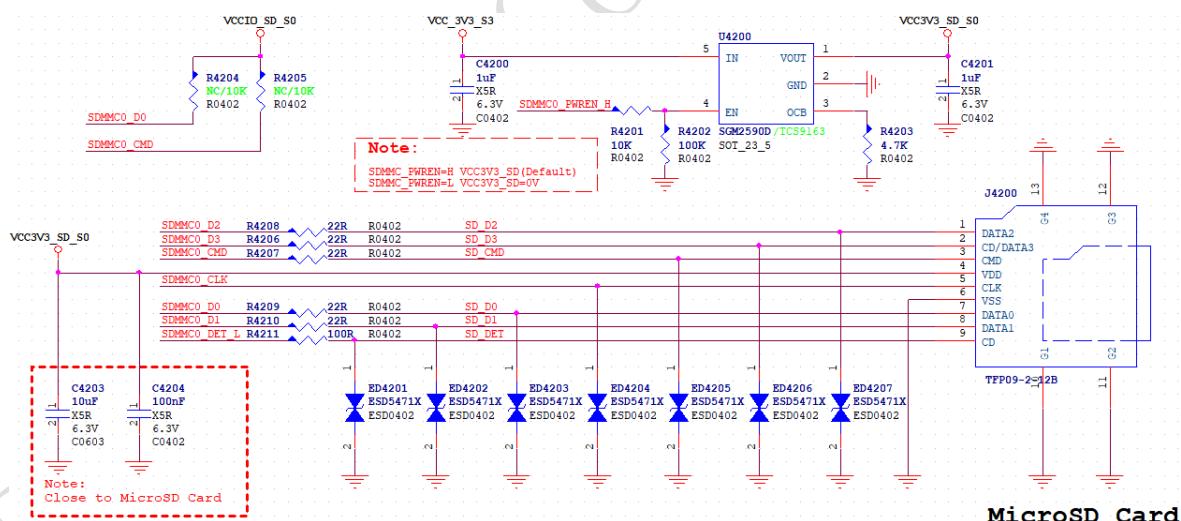


Figure 2-57 SD Card interface circuit

- (7) Recommended Pull-Up/down and Matching Design for SDMMC0 Interface:

Table 2-20 SDMMC0 interface design

Signal	Internal Pull-Up/Down Configuration	Connection Method	Description (Chip Side)
SDMMC0_D[3: 0]	Pull-up	Series-connect 22ohm resistor; External	SD data

		pull-up resistor should be reserved, recommended value: 10K ohm	transmission/reception
SDMMC0_CLK	/	Series-connect 22ohm resistor	SD clock transmission
SDMMC0_CMD	Pull-up	Series-connect 22ohm resistor; External pull-up resistor should be reserved, recommended value: 10K ohm	SD command transmission/reception
SDMMC0_DETN	Pull-up	Series-connect 100ohm resistor; Use corresponding internal pull-up resistor of the IO	SD card insertion detection

2.3.1.2 SDMMC1 Interface

- The SDMMC1 interface is multiplexed at two positions, one in the VCCIO3 power domain and the other in the VCCIO4 power domain. Only one of them can be used at a time. You must either use all connections in the VCCIO3 power domain or all connections in the VCCIO4 power domain. It does not support mixing connections, such as using VCCIO3 for some connections and VCCIO4 for others.
- System Boot functionality is not supported.
- VCCIO3 and VCCIO4 power supplies can be set to either 1.8V or 3.3V. Choose the appropriate voltage based on the requirements of the external device, ensuring consistency with the IO voltage of the external device.

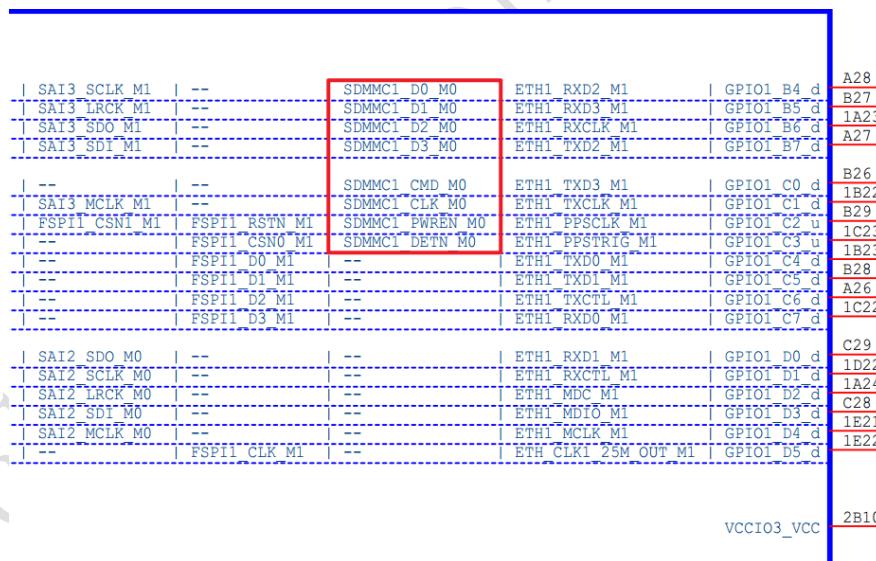


Figure 2-58 RK3576 SDMMC1 Interface M0 Functional Pins

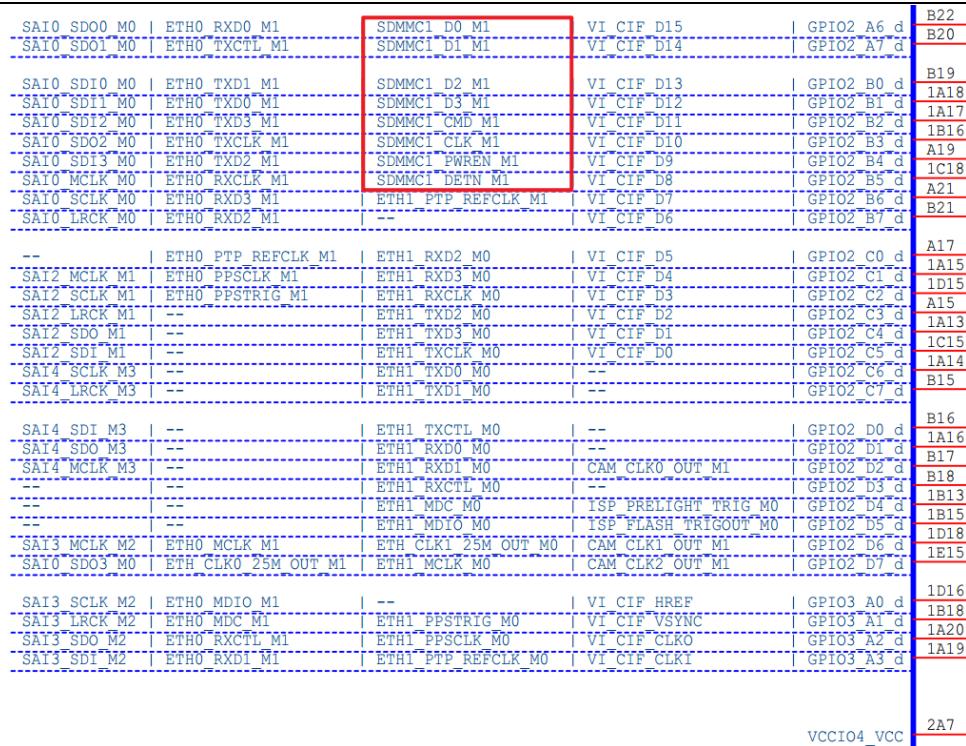


Figure 2-59 RK3576 SDMMC1 Interface M1 Functional Pins

- The recommend SDMMC1 interface pull-down and matching design are shown in the table

Table 2-21 SDMMC1 Interface Design

Signal	Internal chip pull-up and pull-down configuration	Connection method	Description (chip side)
SDMMC1_D[3: 0]	pull-up	Serial 22ohm resistor, can be deleted for shorter alignment. Use corresponding external pull-up resistor	SD data transmit/receive
SDMMC1_CLK	/	Serial 22ohm resistor	SD Clock Transmission
SDMMC1_CMD	pull-up	Serial 22ohm resistor, can be removed for shorter alignments. Using internal pull-up resistor for corresponding IOs.	SD command send/receive

When board-to-board connection is realised through the connector, it is recommended to connect resistors of certain resistance value in series (between 22ohm-100ohm, subject to meeting the SI test) and reserve TVS devices.

Note when SDMMC is connected to Wi-Fi:

- 1) Please make sure the IO level of the module is consistent with the IO level of the CPU, otherwise you need to do the level matching process;
- 2) Please select the crystal load capacitance according to the CL capacitance value of the actual crystal used, and control the frequency tolerance within 10ppm at room temperature;
- 3) Reserve π -type circuit for antenna matching adjustment;
- 4) Confirm the connection direction of PCM and UART interface, such as IN and OUT, TXD and RXD;
- 5) If the module needs to use 32.768k clock input, the RTC chip output needs pull-up resistor and the pull-up

voltage or voltage divider needs to meet the parameters of Wi-Fi module.

2.3.2 SARADC Circuit

RK3576 integrates a 12-bit SARADC controller with a speed of up to 1MS/s. The input voltage range is 0-1.8V, and it can provide 8 channels of SARADC input.

SARADC_IN0_BOOT is dedicated to setting the system boot sequence and cannot be used for other functions. The value obtained by voltage division sampling with pull-up and pull-down resistors is used to determine which interface to boot from. The settings are as follows: (Rup/Rdown represent pull-up and pull-down resistors, respectively).

Table 2-22 RK3576 SARADC_IN0_BOOT configuration

Item	Rup(Kohm)	Rdown(Kohm)	ADC	BOOT MODE
Config 1	NC	10	0	USB(Maskrom mode)
Config 2	10	1.13	416	FSPI0->USB
Config 3	10	2.49	816	FSPI1_M0->EMMC->USB
Config 4	10	4.3	1231	FSPI1_M1->EMMC->USB
Config 5	10	6.8	1658	FSPI0->UFS->USB
Config 6	10	10	2048	FSPI1_M0->UFS->USB
Config 7	10	14.7	2437	UFS->USB
Config 8	10	23.2	2862	UFS->SDMMC0->USB
Config 9	10	40.2	3279	RFU
Config 10	10	88.7	3680	EMMC->SDMMC0->USB
Config 11	10	NC	4095	EMMC->USB

If Rup=DNP, Rdown=10K, and when the RK3576 device is connected to a USB cable and powered on, the system can directly enter Maskrom.

SARADC_IN1 is used for sampling the key value input and is also reused as the Recovery mode button (cannot be modified).

SARADC_IN1 is pulled up to VCCA_1V8_S0 via a 10Kohm 1% resistor, defaulting to a high level (1.8V). If there is no key action and the system has already been programmed with firmware, it directly enters the system upon power-on. If the Recovery mode button is pressed at system startup, keeping SARADC_IN1 at a low level (0V), the RK3576 enters Loader flashing mode. When the PC detects the USB device, releasing the button restores SARADC_IN1 to a high level (1.8V), allowing firmware flashing.

Therefore, in products without a key situation, SARADC_IN1 floating may lead to an unstable state, potentially affecting boot-up. Hence, the 10Kohm 1% pull-up resistor for SARADC_IN1 must be retained without reduction to ensure the default normal boot judgment. For ease of development, it is recommended to reserve a button or a test point for SARADC_IN1.

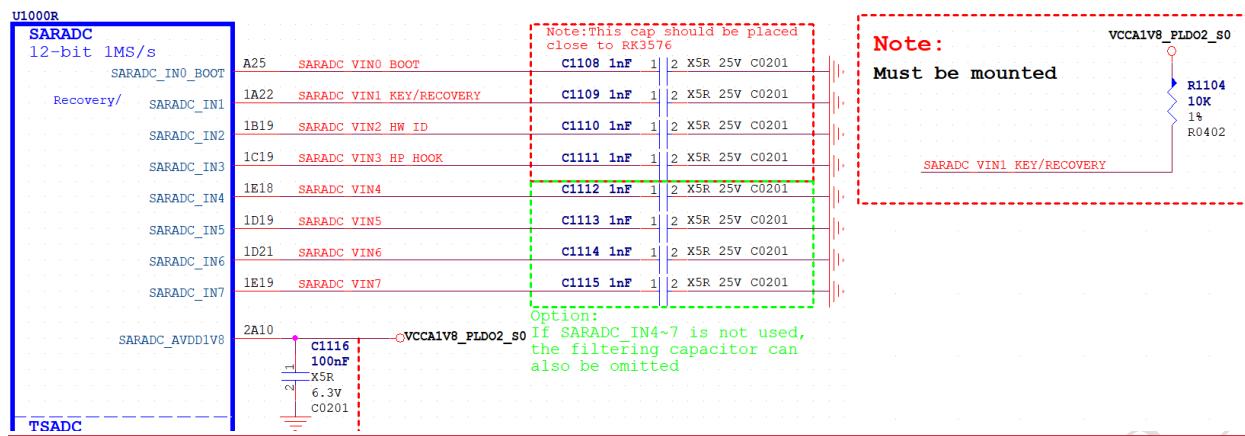


Figure 2-60 SARADC interface

On RK3576, the button array adopts a parallel structure, allowing adjustment of input key values by adding or removing buttons and adjusting the voltage division resistor ratio to meet customer product requirements. In the design, it is suggested that the difference between any two key values must be greater than 300, meaning the center voltage difference must be greater than 132mV.

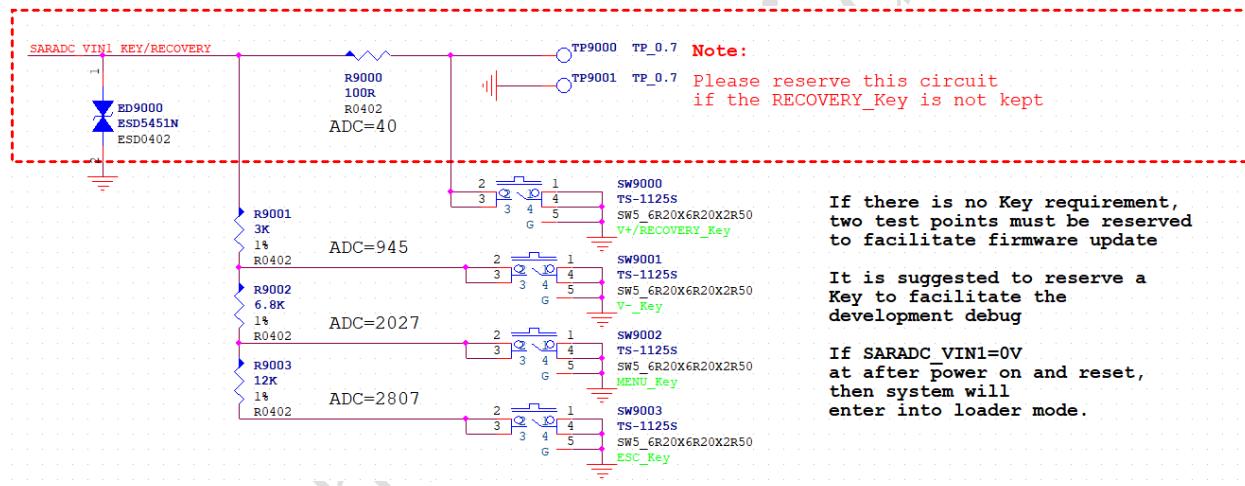


Figure 2-61 RK3576 SARADC button array circuit

For SARADC design on RK3576, some key points to note are:

- The decoupling capacitor for SARADC_AVDD_1V8 power supply must not be reduced. During layout, it should be placed close to the RK3576 pins.
- SARADC_IN[7:0] are in use, and a 1nF capacitor must be added near the pins for debouncing. Do not remove it, as it may cause sampling errors.
- When used for key collection, ESD protection should be implemented near the buttons. Additionally, when using a 0 key value, a 100ohm resistor must be connected in series to enhance electrostatic surge capability. If there is only one key, ESD protection must be placed near the button, passing through ESD → 100ohm resistor → 1nF capacitor → chip pin.

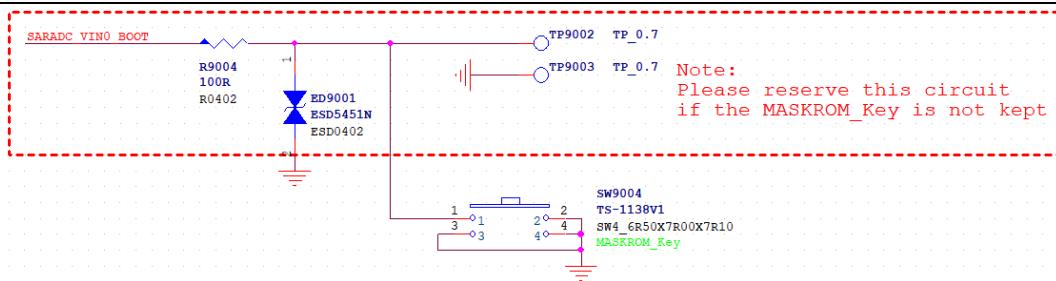


Figure 2-62 RK3576 SARADC single button circuit

2.3.3 OTP Circuit

The RK3576 has 32Kbit internal space and a high-order 4Kbit address of non-secure space for programming. It supports write, read, and idle modes, and in all these modes, the OTP_VDDOTP_0V75 pins must be powered.

The decoupling capacitors for OTP_VDDOTP_0V75 power supply cannot be removed, and during layout, they should be placed close to the RK3576 pins.

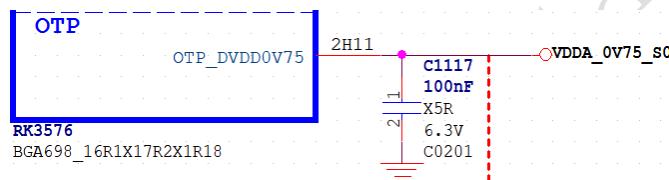


Figure 2-63 RK3576 OTP power pin

2.3.4 USB2/USB3 Circuit

The RK3576 chip has 2 built-in USB3 OTG controllers, and both USB3 controllers have embedded USB2.0 OTG.

2.3.4.1 Application of USB3 OTG0/DP1.4 Interface

The USB3.2 Gen1x1 OTG0/DP1.4 forms a Combo PHY, and the internal multiplexing diagram of the USB3 OTG0 controller and PHY is as follows:

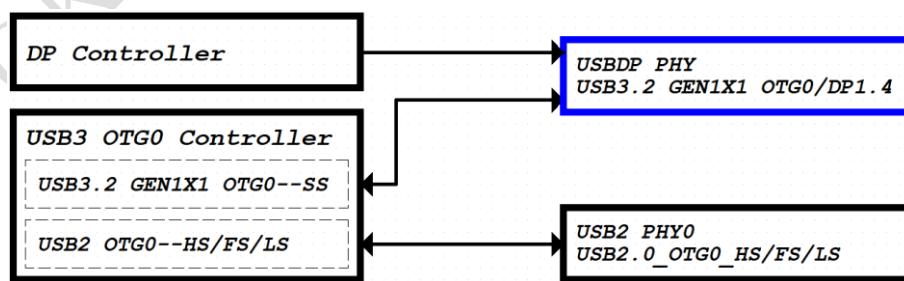


Figure 2-64 Internal Multiplexing Relationship between USB3/DP Controller and PHY

The USB3 OTG0 controller supports SS/HS/FS/LS, and the embedded USB2.0 (HS/FS/LS) signals use USB2.0 OTG PHY. The signal names are listed within the red box in the figure below. RK3576 defaults to using this interface for Firmware Download, so it's essential to reserve this interface in applications.



Figure 2-65 USB2 OTG0 Pins

**NOTE**

USB2_OTG0_DP/USB2_OTG0_DM support Download Firmware. If this interface is not used in the product, it must still be reserved during debugging and production processes. Note: USB2_OTG0_VBUSDET must also be connected!

The SS signal (5Gbps) of USB 3.2 is multiplexed with DP1.4 and uses a USB/DP Combo PHY. The signals are listed within the red box in the figure below.

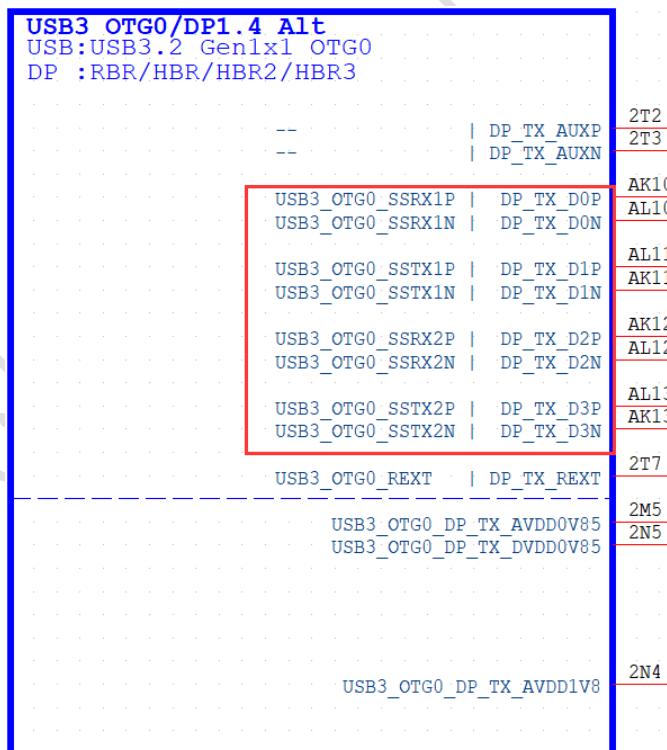


Figure 2-66 USB3 OTG0 and DP1.4 Pins

Since USB3 OTG and USB2.0 OTG share the same USB3 controller, USB3 and USB2.0 OTG can only function simultaneously as Device or HOST. It's not possible for USB3 OTG to be HOST while USB2.0 OTG acts as Device, or for USB3 OTG to be Device while USB2.0 OTG is HOST.

The USB3 OTG0 Controller and DP1.4 Controller combined with the USB3/DP1.4 Combo PHY form a complete TYPEC port. This Combo PHY supports Display Alter mode, with Lane0 and Lane2 acting as TX in DP

mode and RX in USB mode; TX and RX share Lane0 and Lane2.

This USB3/DP1.4 Combo PHY supports Lane swapping (SWAP), enabling five possible configurations for a TYPEC standard port.

- Configuration 1: Type-C 4Lane(with DP function)

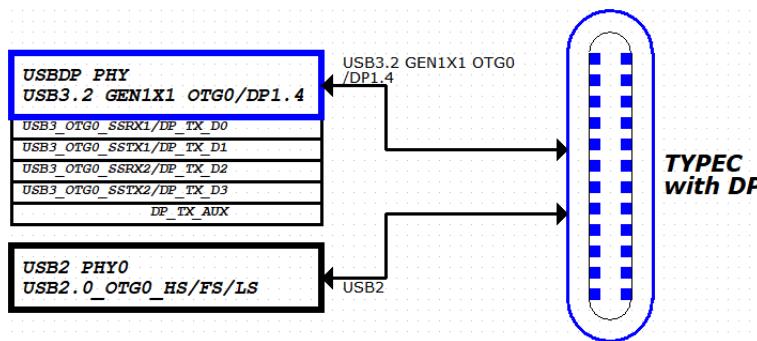


Figure 2-67 TYPEC 4Lane connection with DP block diagram

- Configuration 2: USB2.0 OTG+DP1.4 4Lane(Swap OFF)

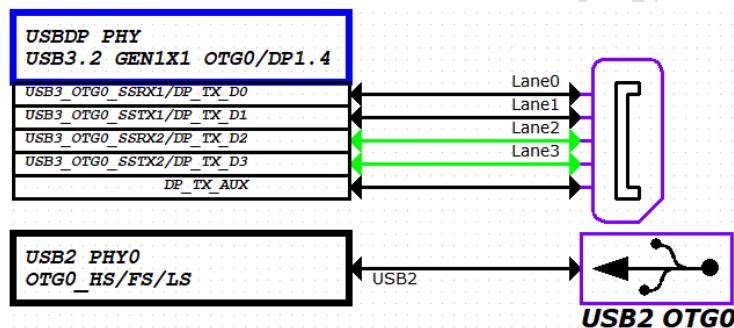


Figure 2-68 USB2.0 OTG+DP 4Lane block diagram

- Configuration 3: USB2.0 OTG+DP1.4 4Lane(Swap ON)

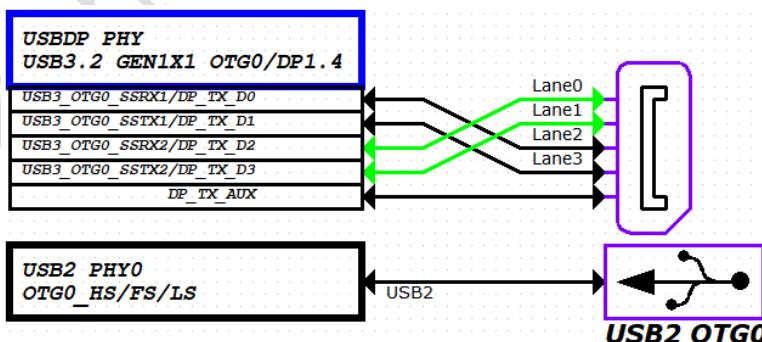


Figure 2-69 USB2.0 OTG+DP 4Lane (Swap ON) block diagram

- Configuration 4: USB3.2 Gen1x1 OTG0+DP1.4 2Lane (Swap OFF)

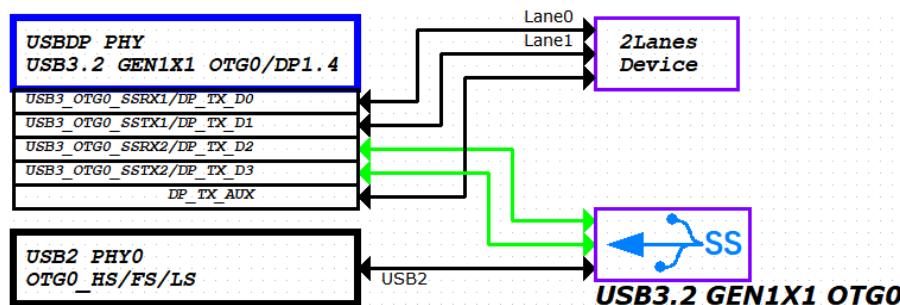


Figure 2-70 USB3.2 Gen1x1 OTG0+DP 2Lane (Swap OFF) block diagram

- Configuration 5: USB3.2 Gen1x1 OTG0+DP1.4 2Lane(Swap ON)

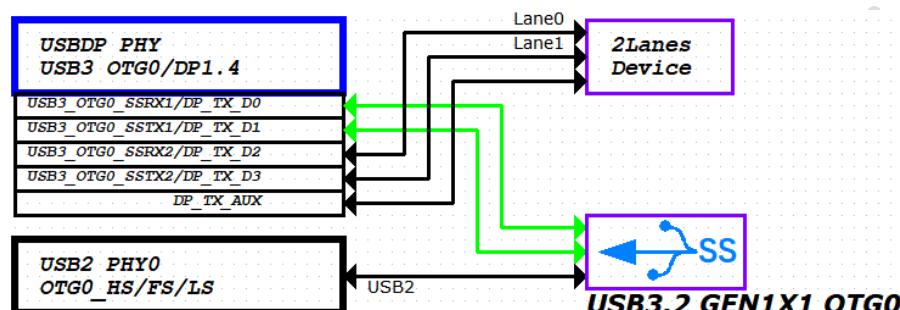


Figure 2-71 USB3.2 Gen1x1 OTG0+DP 2Lane(Swap ON) block diagram



NOTE

RK3576 supports firmware download via USB3_OTG0_SSRX1P/N and USB3_OTG0_SSTX1P/N signals from the USB 3.2 Gen1x1 OTG0 interface. To support USB 3.0 firmware upgrade and 2Lane DP, the USB3.2 Gen1x1 OTG0+DP 2Lane (Swap ON) scheme must be adopted.

2.3.4.2 Application of USB3 OTG1 Interface

PCIE1/SATA1/USB3 OTG1 form Comb PHY1, and the internal multiplexing diagram between USB3 OTG1 controller and PHY is as follows:

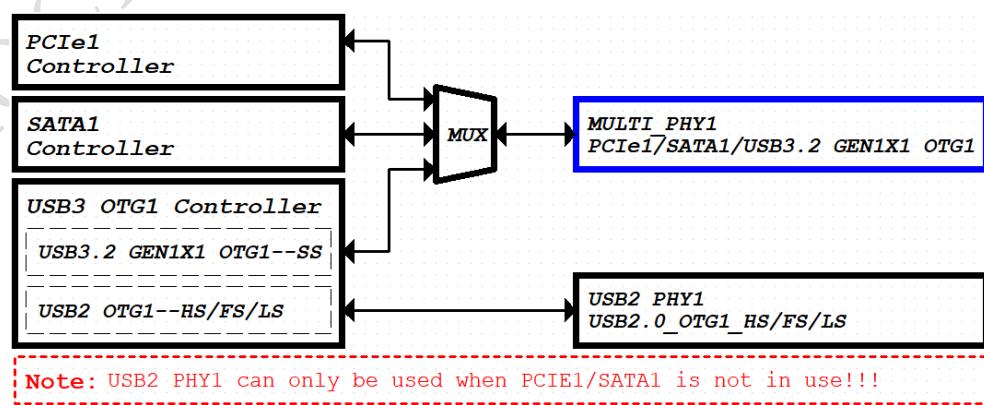


Figure 2-72 Internal Multiplexing Relationship between USB3 OTG1 Controller and PHY

The USB3 OTG1 controller supports SS/HS/FS/LS and embeds USB2.0 (HS/FS/LS) signals to form the

PCIE1/SATA1/USB3 OTG1 COMBO PHY1. The pin distribution is as follows:

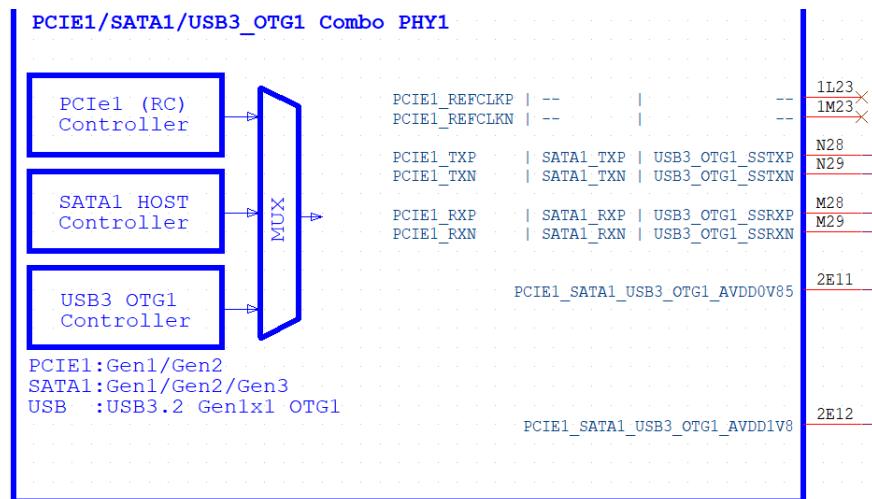


Figure 2-73 USB3 OTG1 Pins

The pin assignment for USB2.0 OTG1 is shown in the figure below:

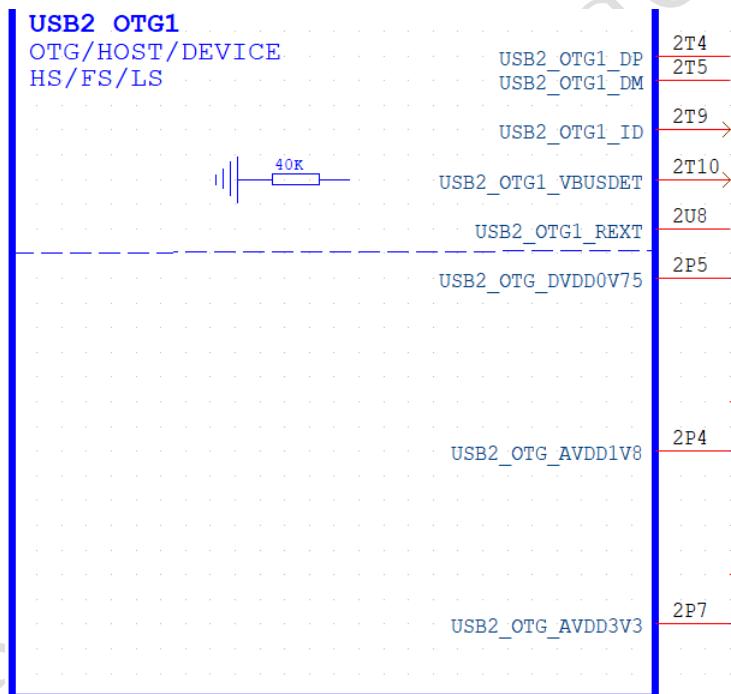


Figure 2-74 USB2 OTG1 Pins

Since USB3 OTG1 and USB2.0 OTG1 share the same USB3 controller, USB3 and USB2.0 OTG1 can only function simultaneously as Device or HOST. It's not possible for USB3 OTG1 to be HOST while USB2.0 OTG1 acts as Device, or for USB3 OTG1 to be Device while USB2.0 OTG1 is HOST.



NOTE

When the COMBO PHY1 of PCIE1/SATA1/USB3 OTG1 is set to PCIe or SATA functionality, USB3 OTG1 function cannot be used, and USB2.0 PHY1 also cannot be used. Therefore, to use USB2.0 OTG1, the COMBO PHY1 of PCIE1/SATA1/USB3 OTG1 must be set to USB3 functionality!

The application modes of USB3 OTG1 in the COMBO PHY1 of PCIE1/SATA1/USB3 OTG1 are as follows:

- Configuration 1: USB3.2 Gen1x1 OTG1

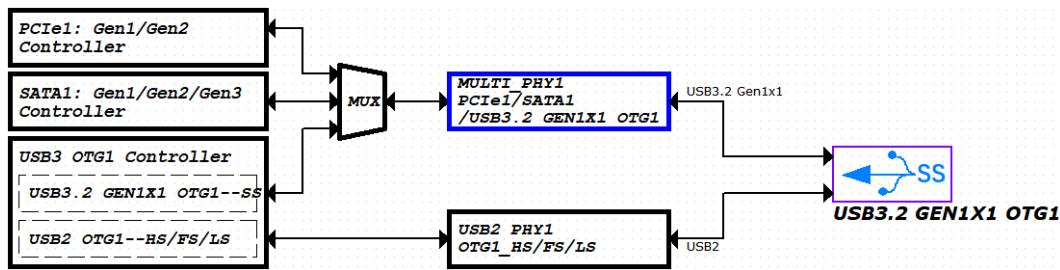


Figure 2-75 USB3.2 OTG1 connection block diagram

- Configuration 2: USB2 OTG1

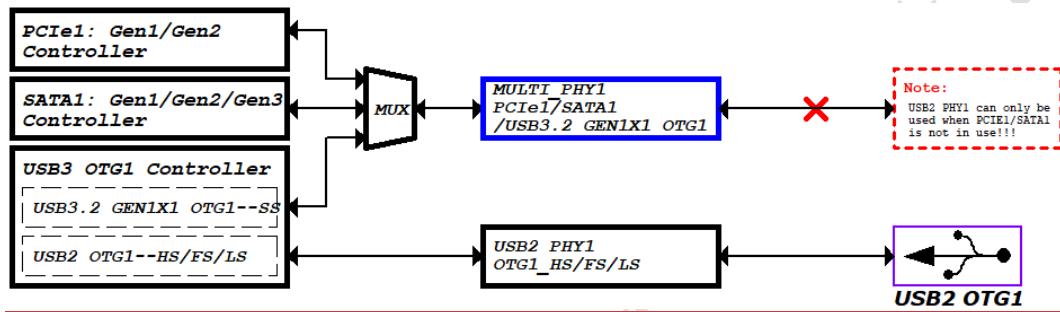


Figure 2-76 USB2 OTG1 connection block diagram

- Configuration 3: USB2/USB3 is not required. For details about how to use PCIE and SATA, see PCIE and SATA

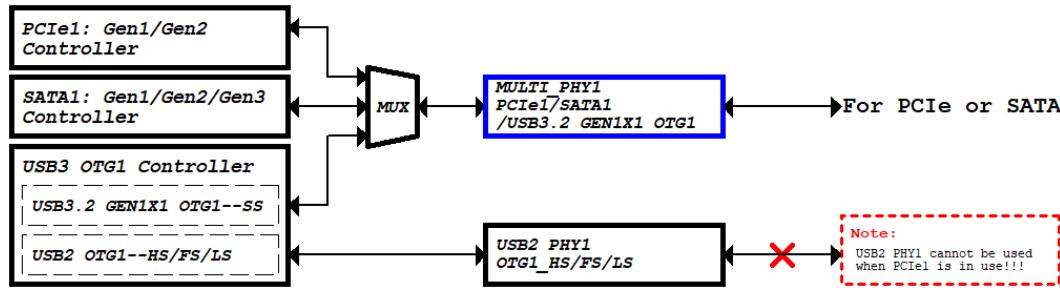


Figure 2-77 unused USB2/USB3 connection block diagram

When designing USB2/USB3, please note the following:

- USB2_OTG0_DP/USB2_OTG0_DM is used for system firmware burning. If this interface is not used in the product, it must still be reserved during debugging and production processes; otherwise, firmware burning during debugging and production will not be possible.
- USB2_OTG0_ID has an internal pull-up resistor of approximately 12Kohm to USB2_OTG_AVDD1V8.
- USB20_OTG0_VBUSDET is used for OTG and Device mode detection. There is an internal pull-down resistor of 40Kohm in the chip. When high, it indicates DEVICE mode, with a voltage range of 2.7-3.3V, typically 3.0V. It's recommended to place a 100nF capacitor near the pin.

OTG mode can be set to the following three modes:

- OTG Mode: Automatically switches between Device and HOST modes based on the ID pin status. When

ID is high, it's Device mode; when ID is pulled low, it's HOST mode. In Device mode, it also checks if VBUSDET pin is high (above 2.3V) before pulling DP high to start enumeration.

- Device Mode: In this mode, no ID pin is required. It only checks if VBUSDET pin is high (above 2.3V) before pulling DP high to start enumeration.
- HOST Mode: In this mode, ID and VBUSDET status are not relevant. (If the product only requires HOST mode but USB2_OTG0_DP/USB2_OTG0_DM is used for system firmware burning, both during debugging and production, this port needs to be used. Therefore, USB2_OTG0_VBUSDET signal must also be connected).

By default, it starts in Device mode before uboot. After uboot starts, these three modes can be configured according to actual requirements.

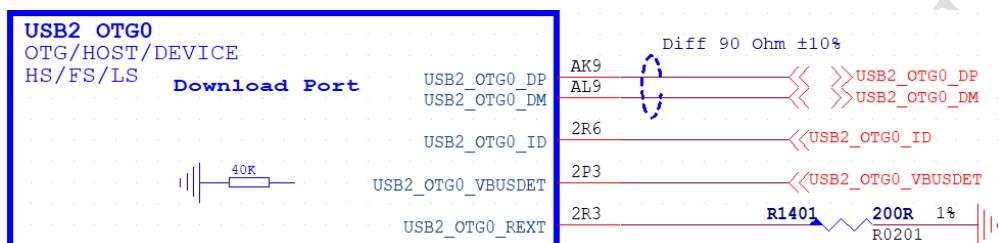


Figure 2-78 RK3576 USB2_OTG0 circuit

If using TYPEC interface, connect Pin "USB2_OTG0_VBUSDET" to 3.3V through a 4.7K pull-up resistor. If using a Micro USB2.0 interface, use the circuit as shown in the diagram.

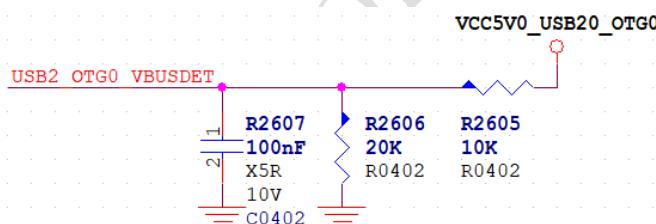


Figure 2-79 USB2_OTG0_VBUSDET detect circuit

- To improve USB performance, do not remove decoupling capacitors for PHY power lines, and place them near the pins during layout.
- To enhance ESD and surge protection, ESD devices must be reserved on all signals, and the parasitic capacitance of ESD for USB2.0 signals should not exceed 3pF. Additionally, DP/DM for USB2.0 signals should be connected with a 2.2ohm resistor in series to enhance ESD and surge protection, and should not be removed, as shown in the diagram. Similar treatment should be applied to other USB2 interfaces.

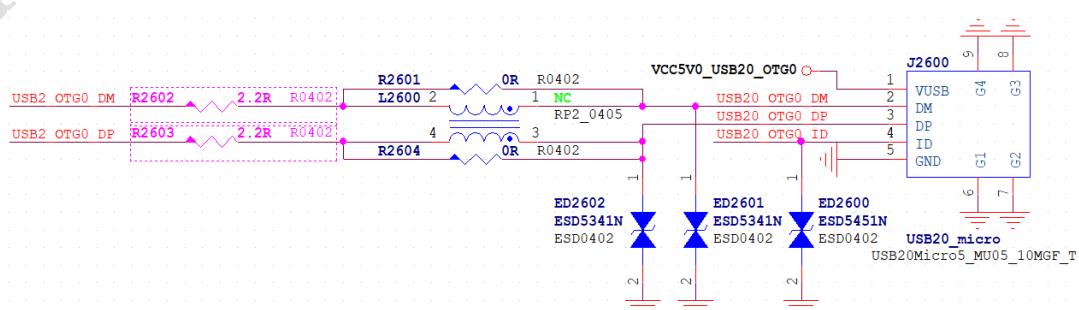


Figure 2-80 SUB2 signal series connect to 2.2ohm resistor

- To suppress electromagnetic radiation, consider reserving common mode chokes (common mode choke) on signal lines. Depending on the actual situation, resistors or common mode chokes can be used during debugging. For example, USB2_OTG0_DP/DM, and other USB2 interfaces should be treated similarly.

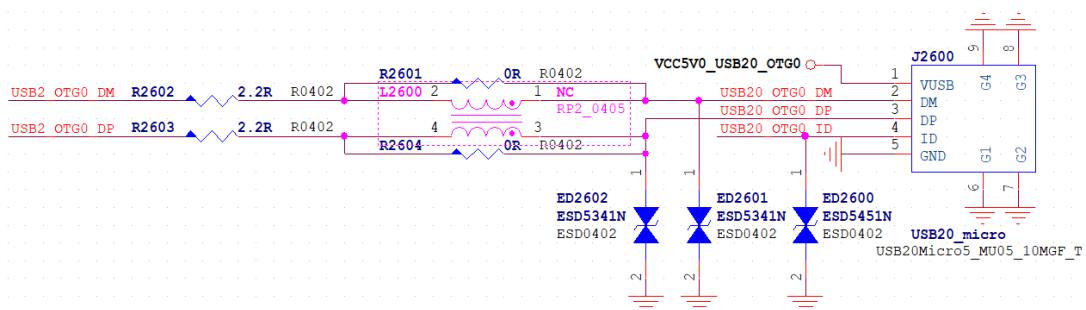


Figure 2-81 USB2 signal series connect to common mode inductor circuit

If the USB2_OTG0_ID signal is used, the ESD device must be reserved to strengthen the anti-static and surge capability, and the 100ohm resistor must be connected in series, which cannot be deleted, see the following figure:

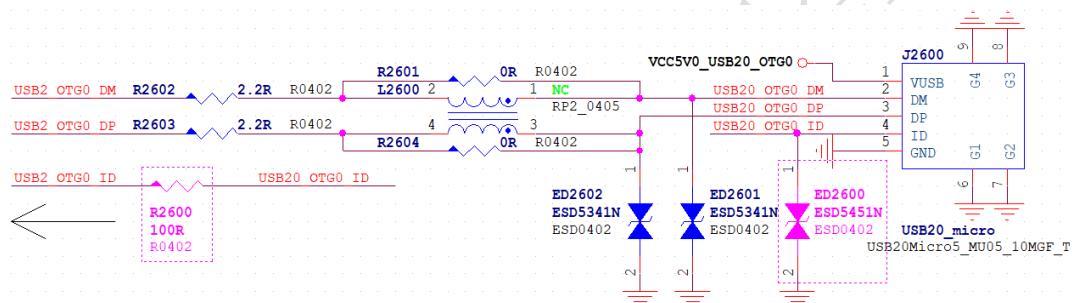


Figure 2-82 USB2_OTG0_ID pin circuit

When the HOST function is enabled, it is recommended that the current limiting switch be added to the 5V power supply, and the current limiting size can be adjusted according to the application needs. The current limiting switch is controlled by 3.3V GPIO. It is recommended that the capacitive filter 22uF and above 100nF be added to the 5V power supply. If the USB port may be connected to a mobile hard disk, it is recommended to increase the filter capacitance to more than 100uF.

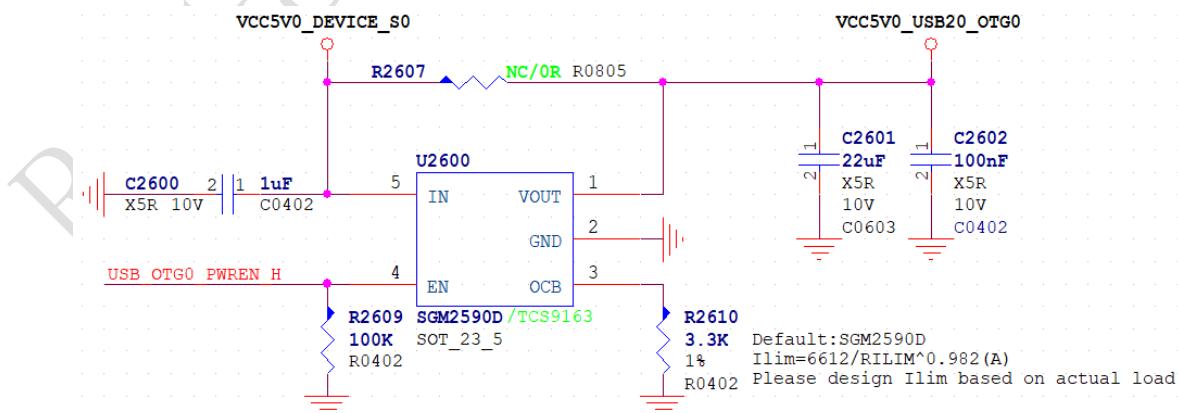


Figure 2-83 USB 5V current limiting switch circuit

The USB3.0 protocol requires adding a 100nF AC coupling capacitor to the SSTXP/N line. It's recommended to use a 0201 package for the AC coupling capacitor for lower ESR and ESL, reducing impedance changes on the

line.

All signals of the TYPEC connector must have ESD devices added, and they should be placed close to the USB connector during layout. For SSTXP/N and SSRXP/N signals, the parasitic capacitance of ESD should not exceed 0.3pF.

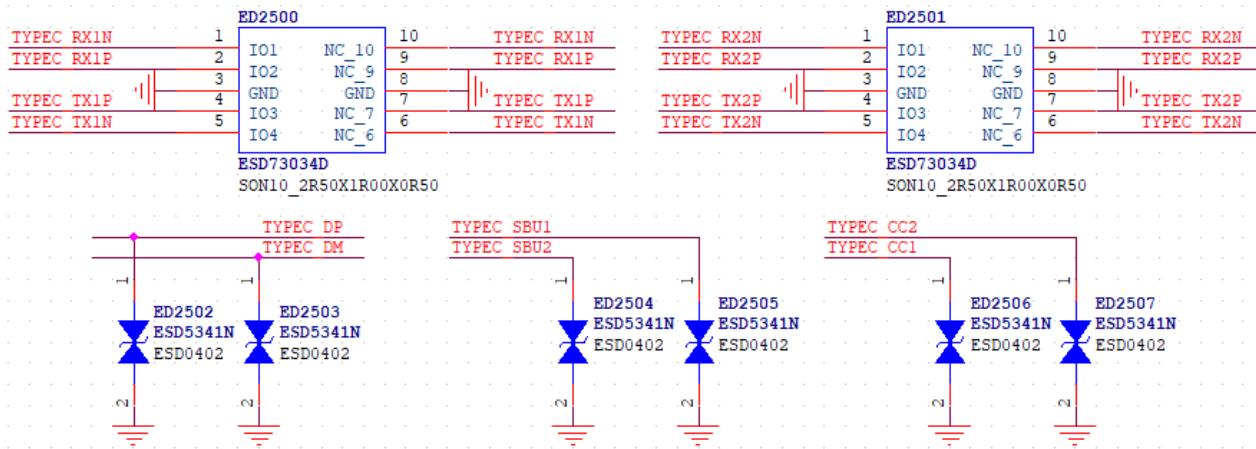


Figure 2-84 TYPEC connector ESD circuit

The following table shows the recommended matching design for USB2/USB3 ports:

Table 2-23 RK3576 USB2/USB3 interface design

Signal	Connection method	Description
USB2_OTG0_DP/DM	Serial connection with 2.2ohm resistor	USB HS/FS/LS mode data input/output
USB2_OTG1_DP/DM		
USB3_OTG0_SSTX1P/SSTX1N USB3_OTG0_SSTX2P/SSTX2N USB3_OTG1_SSTXP/SSTXN	Serial connection with 100nF capacitor (recommended 0201 package)	USB SS mode data output
USB3_OTG0_SSRX1P/SSRX1N USB3_OTG0_SSRX2P/SSRX2N USB3_OTG1_SSRXP/SSRXN	Serial connection with 0ohm resistor	USB SS mode data input
USB2_OTG0_ID USB2_OTG1_ID	Serial connection with 100ohm resistor (external pull-up required, pull-up power supply should be connected to the same supply as USB2_OTG_AVDD1V8)	USB OTG ID detection, required for Micro-USB interface
USB2_OTG0_VBUSDET USB2_OTG1_VBUSDET	Voltage divider detection	USB OTG insertion detection

2.3.5 SATA3.1 Circuit

The RK3576 chip features 2 SATA3.1 controllers, and PCIe as well as USB3_OTG1 controllers share Comb PHY0/1, as shown in the diagram below.

- Supports SATA PM function, each port can support up to 5 devices.
- Supports SATA speeds of 1.5Gb/s, 3.0Gb/s, and 6.0Gb/s.
- Supports eSATA.

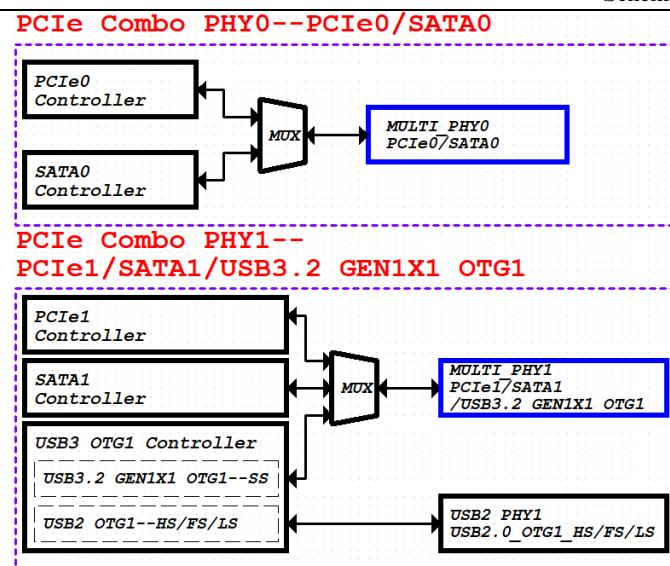
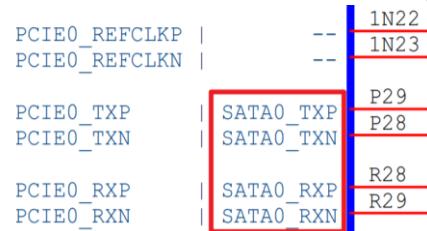
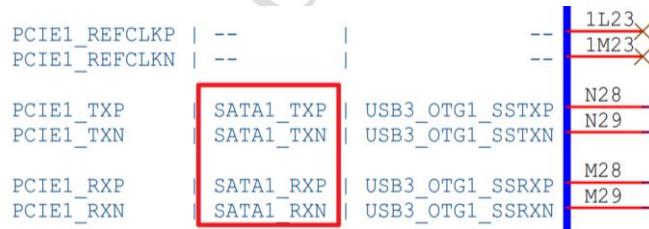


Figure 2-85 Reusing Relationship between PIPE_PHY0/1 and SATA3.1 controllers

SATA0 controller uses Comb PHY0 (shared with PCIE0 Controller).



SATA1 controller uses Comb PHY1 (shared with PCIE1 Controller and USB3_OTG1 controller).



Related control IOs for SATA0/1 controllers include:

- SATA0_ACTLED: Controls LED blinking when data is transferred through the SATA0 interface.
- SATA1_ACTLED: Controls LED blinking when data is transferred through the SATA1 interface.
- SATA_CPDAT: Input for hot-plug detection of SATA devices.
- SATA_MPSWIT: Input for switch detection of SATA hot-plug devices.
- SATA_CPOD: Output for power switch control of SATA hot-plug devices.
- SATA_CPDAT, SATA_MPSWIT, SATA_CPOD are shared interfaces for SATA0/1, can be configured as SATA0 or SATA1 through registers.
- SATA0_ACTLED, SATA1_ACTLED are reused in two locations, one in VCCIO6 power domain, and one in VCCIO4 power domain.

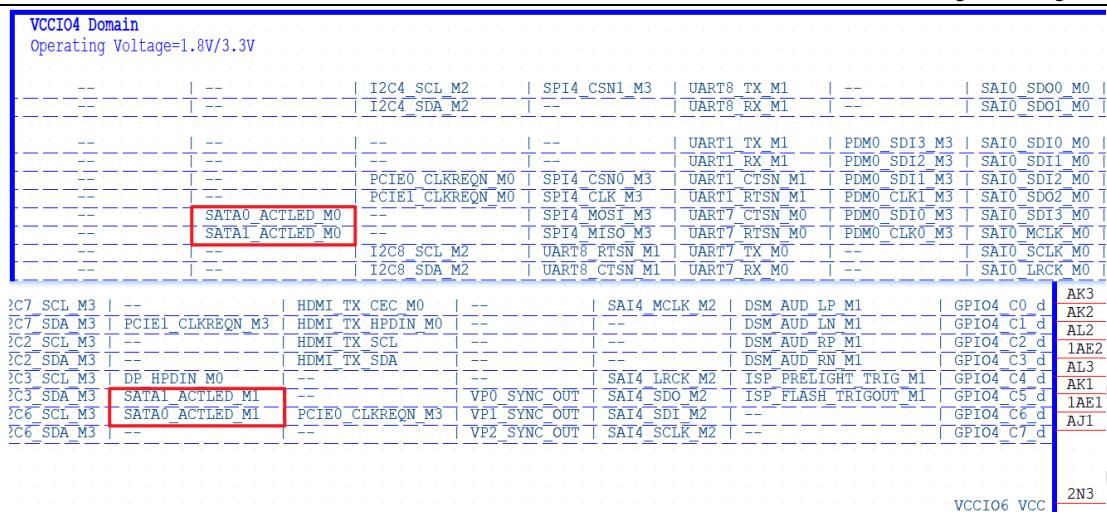


Figure 2-86 SATA0/1 Related Control IO Pins

Considerations for SATA design:

- When designing slots, peripheral circuits and power supplies must meet Spec requirements.
- When connecting an external SATA PM to a SATA interface, support for a maximum of 5 ports is provided, not supporting multiple SATA PMs exceeding 6 ports.
- For SATA interface TXP/N, RXP/N, 10nF AC coupling capacitors are serially connected, AC coupling capacitors are recommended to use 0201 package for lower ESR and ESL, which can also reduce impedance changes on the line.
- All signals of the eSATA interface socket must have ESD devices added, placed near the socket during layout, and the parasitic capacitance of ESD should not exceed 0.4pF.
- SATA interface design recommendations as follow

Table 2-24 RK3576 SATA Interface Design Recommendations:

Signal	Connection Method	Description
SATA0_TXP/TXN	Serial connection with 10nF capacitor (recommended 0201 package)	SATA data output
SATA0_RXP/RXN	Serial connection with 10nF capacitor (recommended 0201 package)	SATA data input
SATA1_TXP/TXN	Serial connection with 10nF capacitor (recommended 0201 package)	SATA data output
SATA1_RXP/RXN	Serial connection with 10nF capacitor (recommended 0201 package)	SATA data input

2.3.6 PCIe2.1 Circuit

RK3576 has 2 PCIe 2.1 controllers, both of which support only RC mode (RC: Root Complex), not EP, as follows:

- Controller 0(1Lane), PCIe0 Controller x1 Lane(Only RC)
- Controller 1(1Lane), PCIe1 Controller x1 Lane(Only RC)

The two PCIe 2.1 controllers are combined with SATA3.1/USB3.2_Gen1x1 to form two Combo PHYs: PCIe2.1/SATA3.1 Combo PHY0 and PCIe2.1/SATA3.1/USB3.2_Gen1x1 Combo PHY1.

The mapping between controllers and PHYs is as follows:

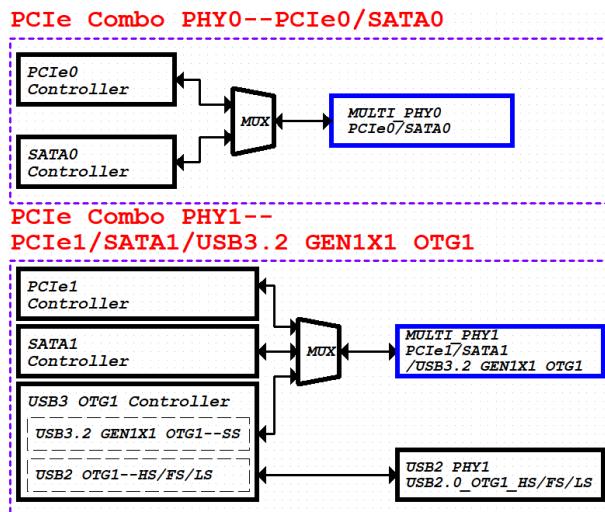


Figure 2-87 Mapping between RK3576 PCIe Controller and PHYs

- PCIe0 controller (RC) shares PCIe2.1/SATA3.1 Combo PHY0 with SATA0 controller.

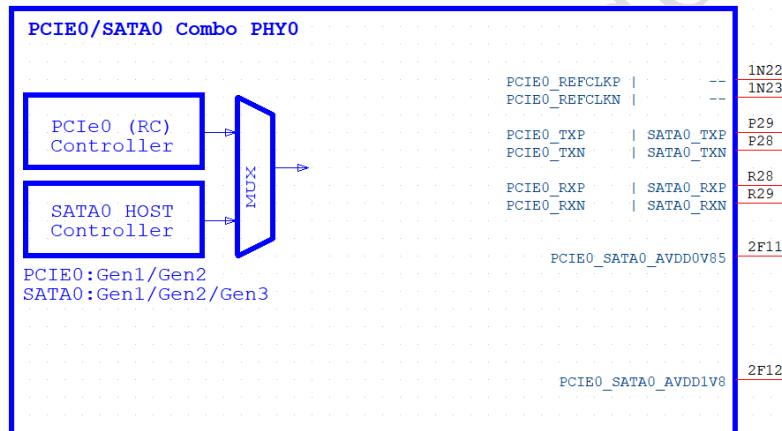


Figure 2-88 PCIe2.1/SATA3.1 Combo PHY0

- PCIe1 controller (RC), SATA1 controller, and USB3_OTG1 controller share PCIe2.1/SATA3.1/USB3.2_Gen1x1 Combo PHY1.

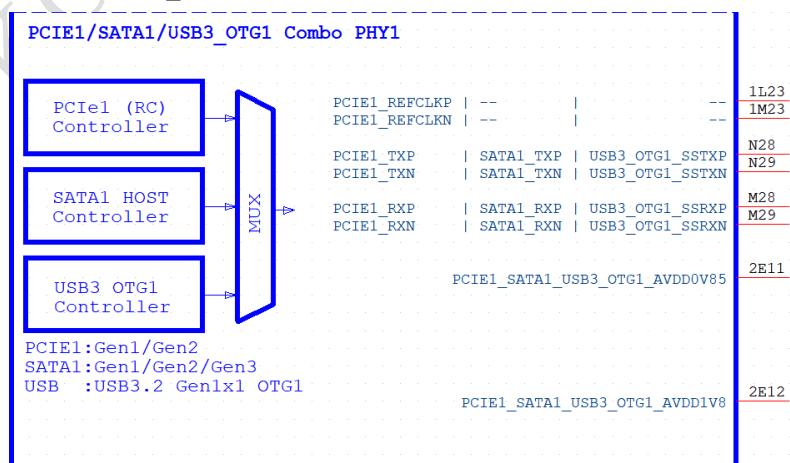


Figure 2-89 PCIe2.1/SATA3.1/USB3.0 Combo PHY1

For PCIE0/1_REFCLKP/N, it can support both output and input. By default, output is provided to EP devices.



Figure 2-90 Path diagram when PCIE0/1_REFCLKP/N clock is output

If PCIE0/1_REFCLKP/N is used as input, the path diagram is as follows:

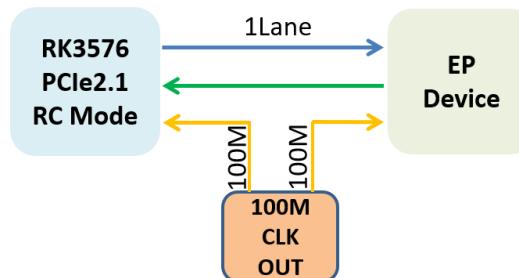


Figure 2-91 Path diagram when PCIE0/1_REFCLKP/N clock is input

Considerations for PCIe 2.1 design:

- When designing slots, peripheral circuits, and power supplies, they must meet Spec requirements.
- For PCIe 2.1 interface, 100nF AC coupling capacitors are serially connected to TXP/N differential signals. AC coupling capacitors are recommended to use 0201 package for lower ESR and ESL, which can also reduce impedance changes on the line.
- PCIE0/1_CLKREQN must use functional pins and cannot be replaced by GPIO.
- PCIE0/1_PERSTN/WAKEN/PRSNT on the RK3576 are not specified with specific IOs, directly using GPIO pins with level matching for control functions is sufficient.
- For standard PCIe Slots: PCIE_x_CLKREQN, PCIE_x_WAKEN, PCIE_x_PERSTN are normally at 3.3V level, attention should be paid to proper level matching on the RK3576 side.
- When using PCIe functions, the reused SATA/USB functions cannot be used. Refer to the respective module descriptions for SATA/USB functions.
- When PCIe 2.1 function module is not in use, the data lines PCIE0/1_TXP/TXN, PCIE0/1_RXP/RXN, and reference clock lines PCIE0/1_REFCLKP/REFCLKN can be left floating. Grounding treatment is required for AVDD0V85 and AVDD1V8 power supplies, and corresponding dts configuration in software needs to be disabled.
- PCIe 2.1 interface design recommendations as follow:

Table 2-25 RK3576 PCIe 2.1 Interface Design Recommendations

Signal	Connection Method	Description
PCIE0/1_TXP/TXN	Serial connection with 100nF (0201) capacitor	PCIe data output
PCIE0/1_RXP/RXN	Direct connection	PCIe data input
PCIE0/1_REFCLKP/CLKN	Direct connection	PCIe reference clock input or output
PCIE0/1_CLKREQN	Serial connection with 0ohm resistor	PCIe reference clock request input (RC mode)

Signal	Connection Method	Description
PCIE0/1_WAKEN (RK3576 does not have this signal, use GPIO instead)	Serial connection with 0ohm resistor	PCIe wake-up input (RC mode)
PCIE0/1_PERSTN (RK3576 does not have this signal, use GPIO instead)	Serial connection with 0ohm resistor	PCIe global reset output (RC mode)
PCIE0/1_PRSNT (RK3576 does not have this signal, use GPIO instead)	Serial connection with 0ohm resistor	Add-In Card insertion detection input (RC mode)
PCIE_BUTTONRSTN (Not used temporarily)	Not used, no need to connect	External physical reset of PCIe Controller

Table 2-26 PCIe control signal multiplexing and corresponding power domain distribution

PCIe control signal	Multiplexing	Multiplexing Domain
PCIE0_CLKREQN_M*	M0, M1, M2, M3	M0: VCCIO4 M1: VCCIO3 M2: VCCIO2 M3: VCCIO6
PCIE1_CLKREQN_M*	M0, M1, M2, M3	M0: VCCIO4 M1: VCCIO3 M2: VCCIO2 M3: VCCIO6

Distribution on the schematic:

- There are 2 IOMUX on the VCCIO2 power domain:

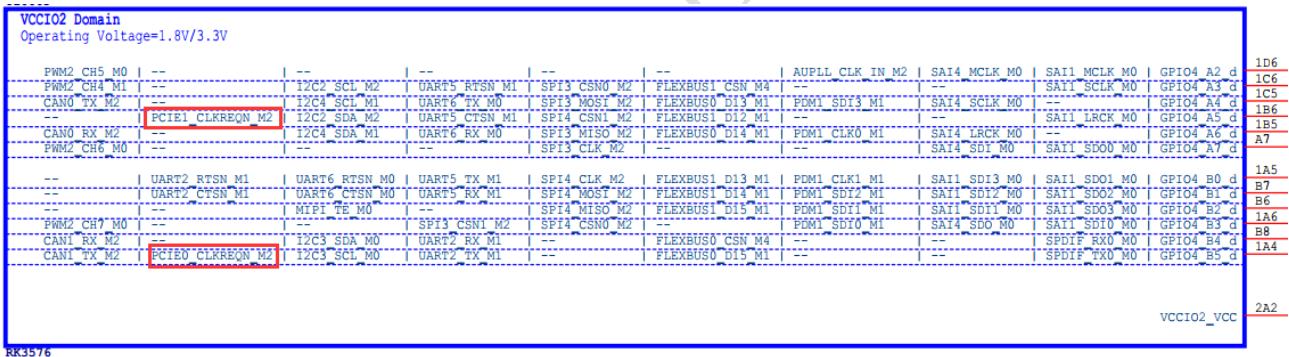


Figure 2-92 PCIe control signal pin in VCCIO2

- There are 4 IOMUX on the VCCIO3 power domain, where the two signals PCIE0/1_BUTTONRSTN are not used for now:

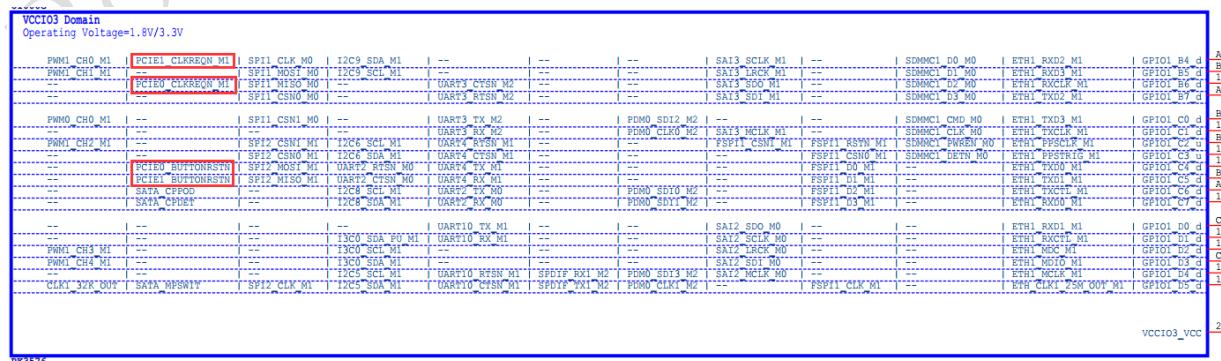


Figure 2-93 PCIe control signal pin in VCCIO3

- There are 2 IOMUX on the VCCIO4 power domain:

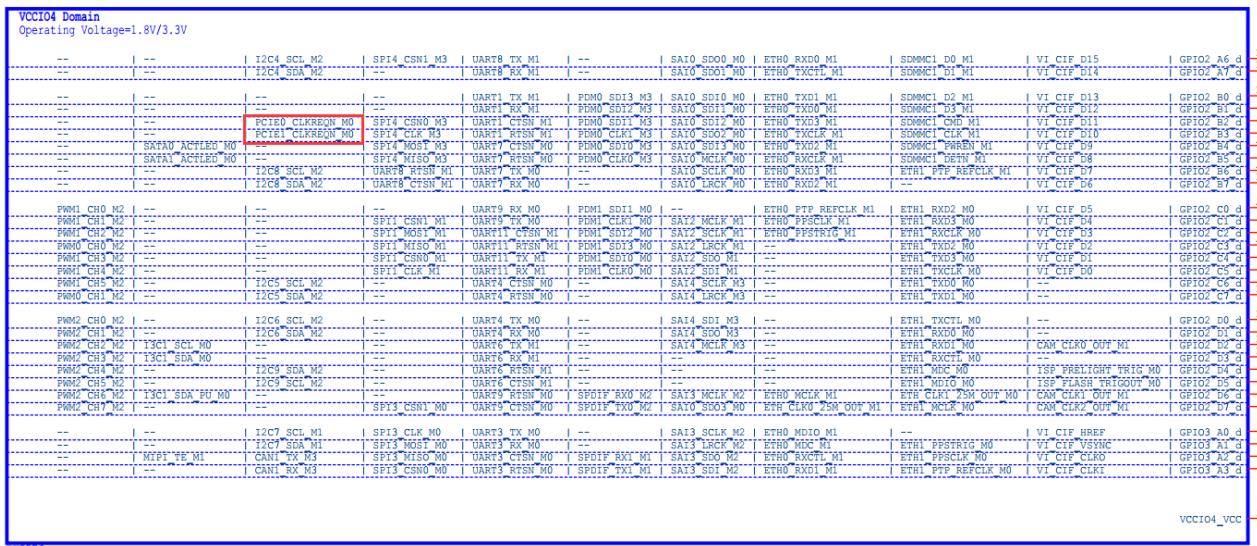


Figure 2-94 PCIe control signal pin in VCCIO4

- There are 2 IOMUX on the VCCIO6 power domain:

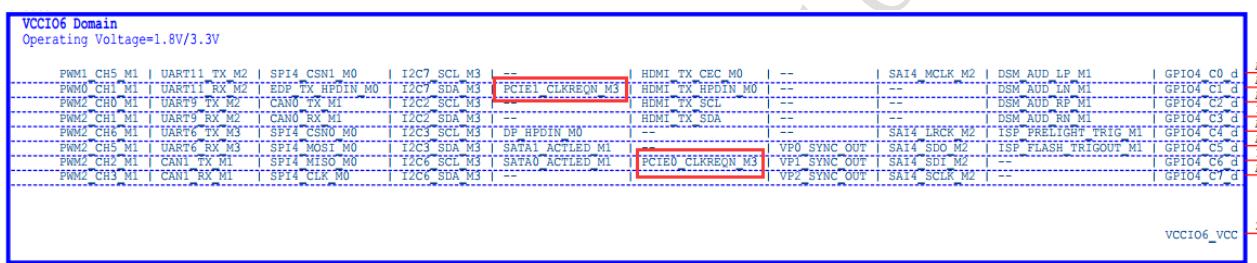


Figure 2-95 PCIe control signal pin in VCCIO6

2.3.7 Video Input Interface Circuit

2.3.7.1 MIPI DPHY CSI RX Interface

RK3576 has 2 MIPI DPHY CSI RX interface, both support MIPI V1.2. The maximum transmission rate per channel is 2.5Gbps.

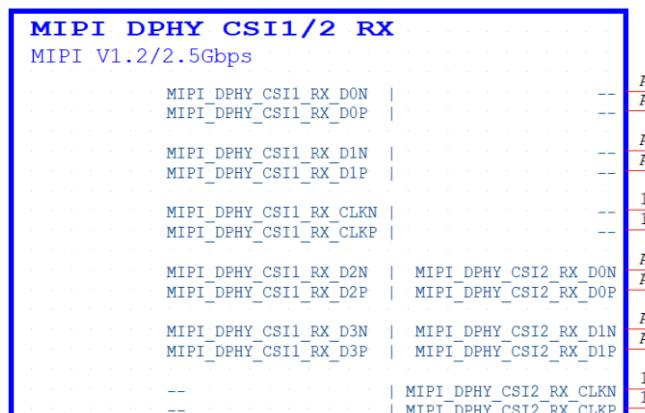


Figure 2-96 BK3576 MIPI DPHY CSI1/2 RX

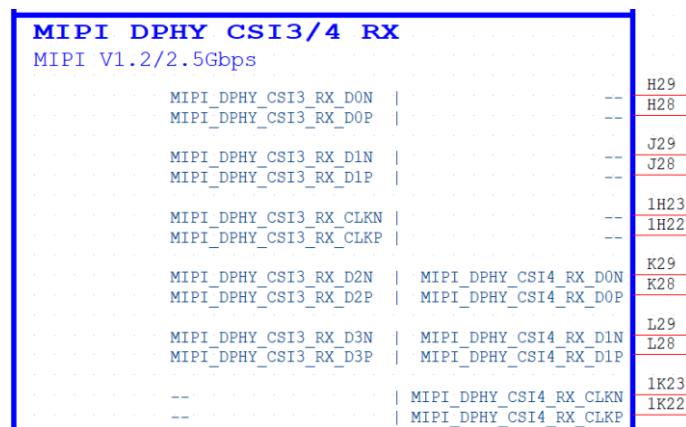


Figure 2-97 RK3576 MIPI DPHY CSI3/4 RX

MIPI DPHY CSI1/2 RX interface supported mode as follow:

- Support 4Lane mode, MIPI_DPHY_CSI1_RX_D[3:0] data refer to MIPI_DPHY_CSI1_RX_CLK
- Support 2Lane+2Lane mode
 - MIPI DPHY CSI1_RX_D[1:0] data refer to MIPI_DPHY_CSI1_RX_CLK
 - MIPI DPHY CSI2_RX_D[1:0] data refer to MIPI_DPHY_CSI2_RX_CLK

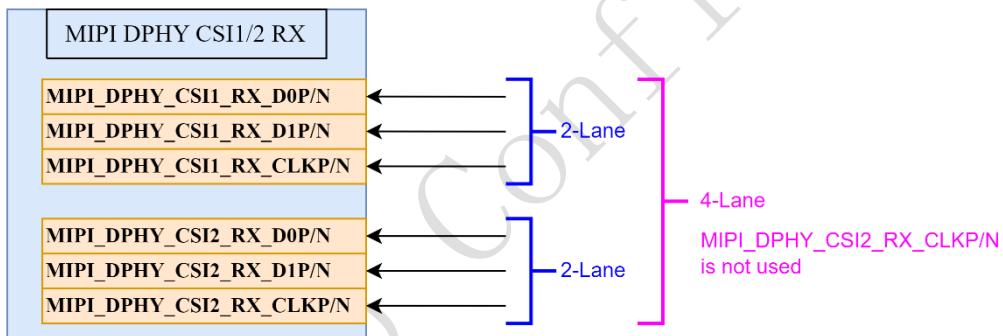


Figure 2-98 RK3576 MIPI DPHY CSI1/2 RX mode and data, clock assign

MIPI DPHY CSI3/4 RX interface supported mode as follow:

- Support 4Lane mode, MIPI_DPHY_CSI3_RX_D[3:0] data refer to MIPI_DPHY_CSI3_RX_CLK
- Support 2Lane+2Lane mode
 - MIPI DPHY CSI3_RX_D[1:0] data refer to MIPI_DPHY_CSI3_RX_CLK
 - MIPI DPHY CSI4_RX_D[1:0] data refer to MIPI_DPHY_CSI4_RX_CLK

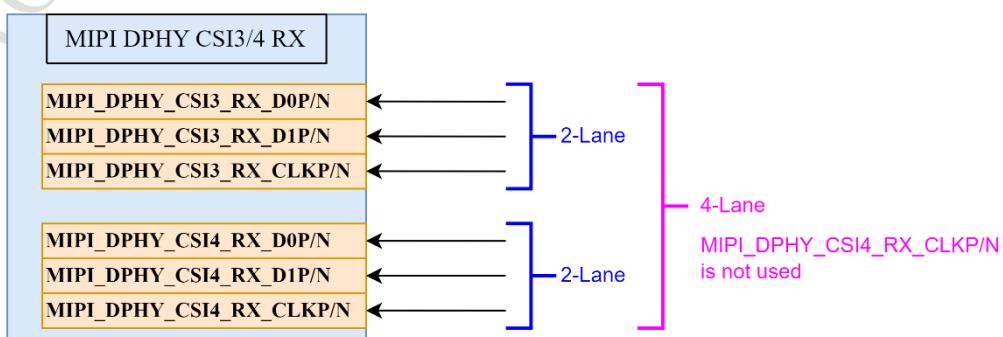


Figure 2-99 RK3576 MIPI DPHY CSI3/4 RX mode and data, clock assign

The recommended matching design of MIPI DPHY CSI1/2/3/4 RX as follow:

Table 2-27 RK3576 MIPI DPHY CSI1/2/3/4 RX interface design

Signal	Connection method	Description
MIPI_DPHY_CSI1_RX_D0P/D0N	Direct connection	MIPI CSI1 data Lane0 input
MIPI_DPHY_CSI1_RX_D1P/D1N	Direct connection	MIPI CSI1 data Lane1 input
MIPI_DPHY_CSI1_RX_D2P/D2N	Direct connection	MIPI CSI1 data Lane2 input
MIPI_DPHY_CSI2_RX_D0P/D0N		MIPI CSI2 data Lane0 input
MIPI_DPHY_CSI1_RX_D3P/D3N	Direct connection	MIPI CSI1 data Lane3 input
MIPI_DPHY_CSI2_RX_D1P/D1N		MIPI CSI2 data Lane1 input
MIPI_DPHY_CSI1_RX_CLKP/CLKN	Direct connection	MIPI CSI1 clock input
MIPI_DPHY_CSI2_RX_CLKP/CLKN	Direct connection	MIPI CSI2 clock input
MIPI_DPHY_CSI3_RX_D0P/D0N	Direct connection	MIPI CSI3 data Lane0 input
MIPI_DPHY_CSI3_RX_D1P/D1N	Direct connection	MIPI CSI3 data Lane1 input
MIPI_DPHY_CSI3_RX_D2P/D2N	Direct connection	MIPI CSI3 data Lane2 input
MIPI_DPHY_CSI4_RX_D0P/D0N		MIPI CSI4 data Lane0 input
MIPI_DPHY_CSI3_RX_D3P/D3N	Direct connection	MIPI CSI3 data Lane3 input
MIPI_DPHY_CSI4_RX_D1P/D1N		MIPI CSI4 data Lane1 input
MIPI_DPHY_CSI3_RX_CLKP/CLKN	Direct connection	MIPI CSI3 clock input
MIPI_DPHY_CSI4_RX_CLKP/CLKN	Direct connection	MIPI CSI4 clock input

2.3.7.2 MIPI_DCPHY_CSI_RX Interface

The RK3576 has a MIPI DCPHY CSI RX Combo PHY; DPHY supports version V2.0 and CPHY supports version V1.1. DPHY mode has 4Lane with a maximum transfer rate of 4.5Gbps/Lane; CPHY mode has 3Trios with a maximum transfer rate of 5.7Gbps/Trio.

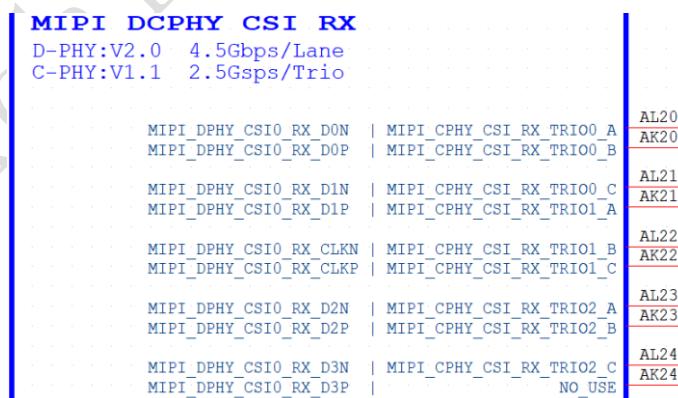


Figure 2-100 RK3576 MIPI DCPHY CSI RX signal pin

DPHY, CPHY configuration support:

- The TX and RX of the MIPI DCPHY Combo PHY can only support simultaneous configuration into DPHY TX, DPHY RX modes, or simultaneous configuration into CPHY TX, CPHY RX modes. Configuration of one as DPHY TX and one as CPHY RX, or one as CPHY TX and one as DPHY RX is not supported.

MIPI DCPHY support when working in DPHY mode:

- Support 4Lane/2Lane/1Lane mode, MIPI_DPHY_CSI0_RX[3:0] data refer to MIPI_DPHY_CSI0_RX_CLK
- Does not support splitting into 2Lane+2Lane

Supported when MIPI DCPHY is working in CPHY mode:

- Support 0/1/2 Trio, each Trio has Trio_A/Trio_B/Trio_C 3 wires, MIPI_CPHY_CSI_RX_TRIO[2:0]_A, MIPI_CPHY_CSI_RX_TRIO[2:0]_B, MIPI_CPHY_CSI_RX_TRIO[2:0]_C.

MIPI DCPHY CSI RX Combo PHY design note:

- In order to improve the MIPI DCPHY CSI RX Combo PHY performance, the decoupling capacitors of each power supply of the PHY should not be removed, and please place them close to the pins in the layout (note that the MIPI DCPHY CSI RX and MIPI DCPHY DSI TX power supplies are combined in the same way);
- MIPI_DCPHY_AVDD voltage selection: when the MIPI rate is greater than DPHY 2.5Gbps or CPHY 1.5Gsp, the MIPI_DCPHY_AVDD voltage is configured to 0.85V; when the MIPI rate is less than DPHY 2.5Gbps or CPHY 1.5Gsp, the MIPI_DCPHY_AVDD voltage is configured to 0.75V.

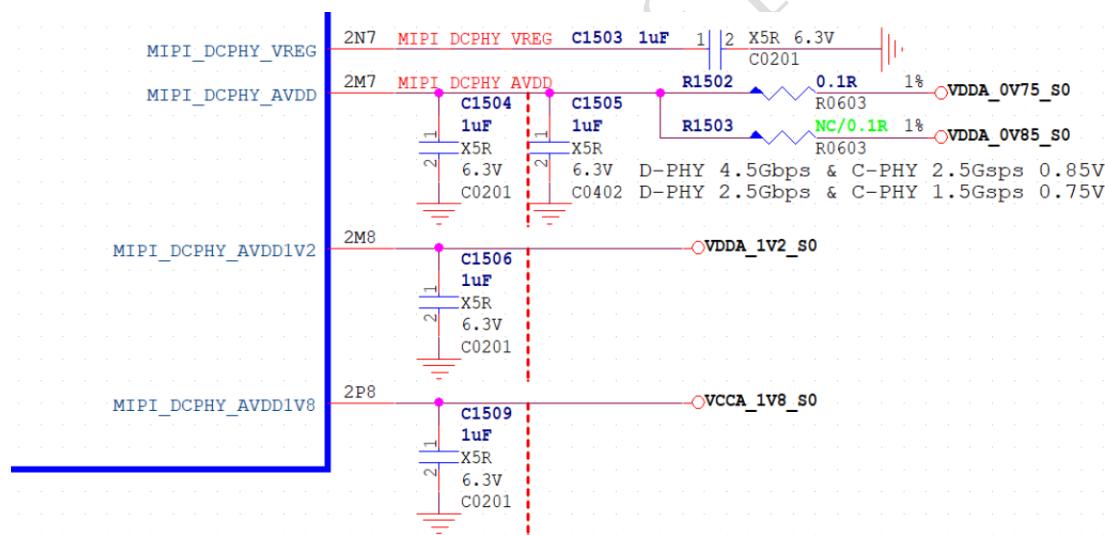


Figure 2-101 MIPI DCPHY CSI RX Combo PHY Power Supply Decoupling Capacitor and Power Supply

- The 1uF capacitor of MIPI_DCPHY_VREG must not be removed and must be placed close to the corresponding pin during layout;
- MIPI DCPHY CSI RX Combo PHY matching design recommendations are shown in the table below:

Table 2-28 RK3576 MIPI DCPHY CSI RX Combo PHY interface design

Signal (DPHY/CPHY)	Connect method	Description
MIPI_DPHY_CSI0_RX_D0P/D0N	Direct connection	MIPI_DPHY_CSI0_RX data Lane0 input
MIPI_DPHY_CSI0_RX_D1P/D1N	Direct connection	MIPI_DPHY_CSI0_RX data Lane1 input
MIPI_DPHY_CSI0_RX_D2P/D2N	Direct connection	MIPI_DPHY_CSI0_RX data Lane2 input
MIPI_DPHY_CSI0_RX_D3P/D3N	Direct connection	MIPI_DPHY_CSI0_RX data Lane3 input

Signal (DPHY/CPHY)	Connect method	Description
MIPI_DPHY_CSI0_RX_CLKP/CLKN	Direct connection	MIPI_DPHY_CSI0_RX clock input
MIPI_CPHY_CSI_RX_TRIO0_A/B/C	Direct connection	MIPI_CPHY_CSI_RX_TRIO0 input
MIPI_CPHY_CSI_RX_TRIO1_A/B/C	Direct connection	MIPI_CPHY_CSI_RX_TRIO1 input
MIPI_CPHY_CSI_RX_TRIO2_A/B/C	Direct connection	MIPI_CPHY_CSI_RX_TRIO2 input

2.3.7.3 CIF(DVP) Interface

CIF interface power supply domain powered by VCCIO4. In actual product design, according to the product Camera's actual IO power supply requirements (1.8V or 3.3V), select the corresponding power supply, at the same time, the I2C pull-up level must be consistent with it, otherwise it will result in the Camera work abnormally or can not work.

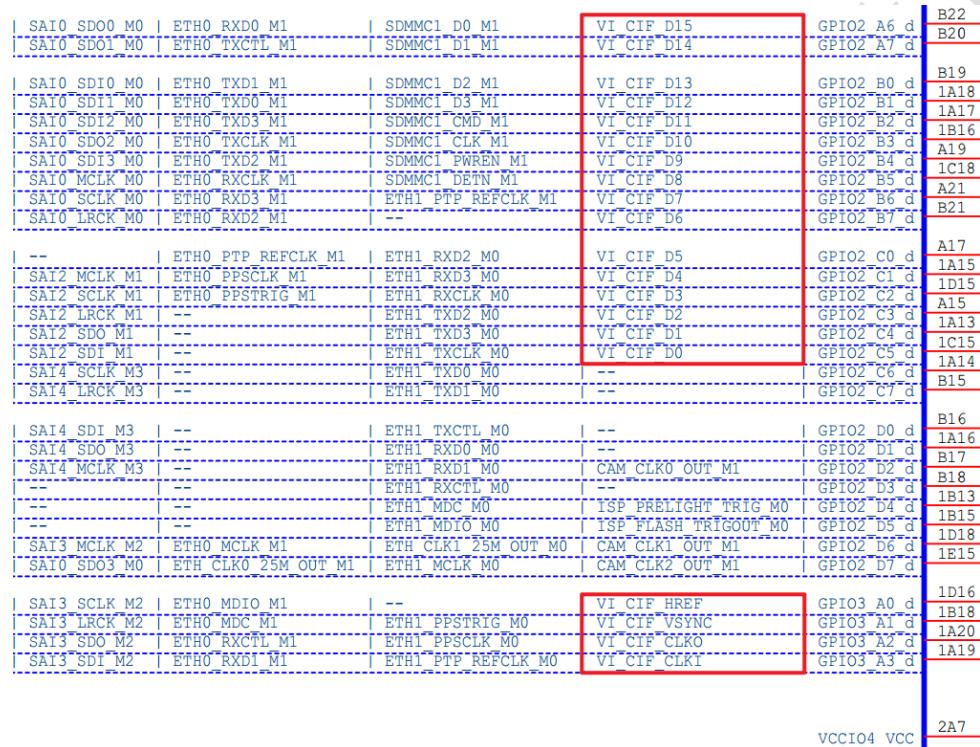


Figure 2-102 RK3576 CIF function pin

The CIF interface support the following format:

- Supports BT601 RAW8/10/12 YCbCr 422 8bit input
- Supports BT656 YCbCr 422 8-bit progressive/interlaced input
- Supports 16-Pins BT1120 YCbCr 422 8-bit progressive/interlaced input
- Supports 2/4 mixed BT.656/BT1120 YCbCr 422 input

The mapping between the 8/10/12/16bit data of CIF[15:0] is as follows, with high and low alignment supported:

Table 2-29 RK3576 CIF data correspondence

	Mode	16bit	12bit	10bit	8bit		Mode	16bit	12bit	10bit	8bit
低对齐	VI_CIF_D0	VI_CIF_D0	VI_CIF_D0	VI_CIF_D0	VI_CIF_D0	高对齐	VI_CIF_D0	VI_CIF_D0			
	VI_CIF_D1	VI_CIF_D1	VI_CIF_D1	VI_CIF_D1	VI_CIF_D1		VI_CIF_D1	VI_CIF_D1			
	VI_CIF_D2	VI_CIF_D2	VI_CIF_D2	VI_CIF_D2	VI_CIF_D2		VI_CIF_D2	VI_CIF_D2			
	VI_CIF_D3	VI_CIF_D3	VI_CIF_D3	VI_CIF_D3	VI_CIF_D3		VI_CIF_D3	VI_CIF_D3			
	VI_CIF_D4	VI_CIF_D4	VI_CIF_D4	VI_CIF_D4	VI_CIF_D4		VI_CIF_D4	VI_CIF_D4	VI_CIF_D0		
	VI_CIF_D5	VI_CIF_D5	VI_CIF_D5	VI_CIF_D5	VI_CIF_D5		VI_CIF_D5	VI_CIF_D5	VI_CIF_D1		
	VI_CIF_D6	VI_CIF_D6	VI_CIF_D6	VI_CIF_D6	VI_CIF_D6		VI_CIF_D6	VI_CIF_D6	VI_CIF_D2	VI_CIF_D0	
	VI_CIF_D7	VI_CIF_D7	VI_CIF_D7	VI_CIF_D7	VI_CIF_D7		VI_CIF_D7	VI_CIF_D7	VI_CIF_D3	VI_CIF_D1	
	VI_CIF_D8	VI_CIF_D8	VI_CIF_D8	VI_CIF_D8	VI_CIF_D8		VI_CIF_D8	VI_CIF_D8	VI_CIF_D4	VI_CIF_D2	VI_CIF_D0
	VI_CIF_D9	VI_CIF_D9	VI_CIF_D9	VI_CIF_D9	VI_CIF_D9		VI_CIF_D9	VI_CIF_D9	VI_CIF_D5	VI_CIF_D3	VI_CIF_D1
	VI_CIF_D10	VI_CIF_D10	VI_CIF_D10				VI_CIF_D10	VI_CIF_D10	VI_CIF_D6	VI_CIF_D4	VI_CIF_D2
	VI_CIF_D11	VI_CIF_D11	VI_CIF_D11				VI_CIF_D11	VI_CIF_D11	VI_CIF_D7	VI_CIF_D5	VI_CIF_D3
	VI_CIF_D12	VI_CIF_D12					VI_CIF_D12	VI_CIF_D12	VI_CIF_D8	VI_CIF_D6	VI_CIF_D4
	VI_CIF_D13	VI_CIF_D13					VI_CIF_D13	VI_CIF_D13	VI_CIF_D9	VI_CIF_D7	VI_CIF_D5
	VI_CIF_D14	VI_CIF_D14					VI_CIF_D14	VI_CIF_D14	VI_CIF_D10	VI_CIF_D8	VI_CIF_D6
	VI_CIF_D15	VI_CIF_D15					VI_CIF_D15	VI_CIF_D15	VI_CIF_D11	VI_CIF_D9	VI_CIF_D7

BT1120 16bit mode data correspondence, support YC Swap

Table 2-30 RK3576 BT1120 16bit mode data correspondence table

Pin Name	Default mode		Swap opened	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1
VI_CIF_D0	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]
VI_CIF_D1	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]
VI_CIF_D2	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]
VI_CIF_D3	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]
VI_CIF_D4	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]
VI_CIF_D5	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]
VI_CIF_D6	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]
VI_CIF_D7	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]
VI_CIF_D8	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]
VI_CIF_D9	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]
VI_CIF_D10	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]
VI_CIF_D11	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]
VI_CIF_D12	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]
VI_CIF_D13	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]
VI_CIF_D14	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]
VI_CIF_D15	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]

The CIF interface pull-down and matching design recommendations are listed in the table below:

Table 2-31 RK3576 CIF interface design

Signal	Chip internal pull-up and pull-down configurations	Connection method	Description (chip end)
VI_CIF_D[15: 0]	Pull-down	Direct connection, if possible, it is recommended to reserve a series resistance near the chip end.	CIF data input
VI_CIF_HREF	Pull-down	Direct connection, if possible, it is recommended to reserve a series resistance near the chip end.	CIF line sync input
VI_CIF_VSYNC	Pull-down	Direct connection, if possible, it is recommended to reserve a series resistance near the chip end.	CIF field sync input
VI_CIF_CLKIN	Pull-down	Series 22ohm resistor near the device end	CIF clock input
VI_CIF_CLKOUT	/	Series 22ohm resistor near the device end	CIF clock output, can be provided to the device as the MCLK operating clock

When the board-to-board connection is achieved through the connector, it is recommended to connect a resistor of a certain resistance value in series (between 22ohm-100ohm, subject to the ability to satisfy the SI test) and to reserve the TVS device.

2.3.7.4 Points to Note When Designing the MIPI CSI RX/CIF

- The DVDD power supply of Camera has different cases such as 1.2V/1.5V/1.8V, please provide the exact power supply according to the Camera's datasheet, the reference circuit is 1.2V by default;
- Some Camera's DVDD current is relatively high, more than 100mA it is recommended to use DCDC power supply;
- Several power supplies of Camera have power-up timing requirements, please adjust the power-up timing accordingly to the Camera's datasheet, the default power-up timing of the reference diagram is: 1.8V → 1.2V → 2.8V;
- When using Camera with CIF interface, please note that the DOVDD (IO power supply) and VCCIO6 power supply of Camera must use the same voltage;
- When using two Camera, the power supply can be separated or combined according to the actual situation of demand, the default is separated in the reference diagram;
- If Camera with AF function, VCC2V8_AF needs to be powered separately; or shared with AVCC2V8_DVP, which must be isolated by magnetic beads;
- Decoupling capacitors for all power supplies of Camera must not be deleted, but must be kept and placed close to the seat;
- The PWDN signal of the Camera must be controlled using GPIO and the GPIO level must match the Camera IO level;
- Camera's Reset signal is recommended to use GPIO control, GPIO level must be matched with Camera IO level, 100nF capacitor of Reset signal must not be deleted, placed close to the cradle to strengthen the

- anti-static ability;
- Camera's MCLK can be obtained from the following:
 - VI_CIF_CLKOUT
 - REF_CLK0_OUT/REF_CLK1_OUT/REF_CLK2_OUT
 - CAM_CLK0_OUT/CAM_CLK1_OUT/CAM_CLK2_OUT
 - Note: The level of the clock must match the Camera IO level, if not, the level must be level shifted or resistor divided to match the level;
- If two Camera are of the same model, pay attention to whether the I2C address is the same, if the address is also the same, then two I2C buses are needed.

2.3.8 Video Output Interface Circuit

The RK3576 chip has a VOP display output processor, which reads video data and UI data from the frame buffer of the system memory, performs appropriate processing such as cropping, colour space conversion, scaling and overlaying, and outputs to each of the high-speed display interfaces.

There are three Port outputs, which can output to DP, HDMI/eDP, MIPI DSI, and LCDC (Parallel Interface) video interfaces.

Maximum video output capacity:

- (1) Triple screen heterodyne solution, such as 4096x2160@60Hz, 2560x1600@60Hz, 1920x1080@60Hz;
- (2) Dual-screen heterodyne solution, such as 4096x2160@120Hz, 2560x1600@60Hz.

VOP and video interface output path diagram:

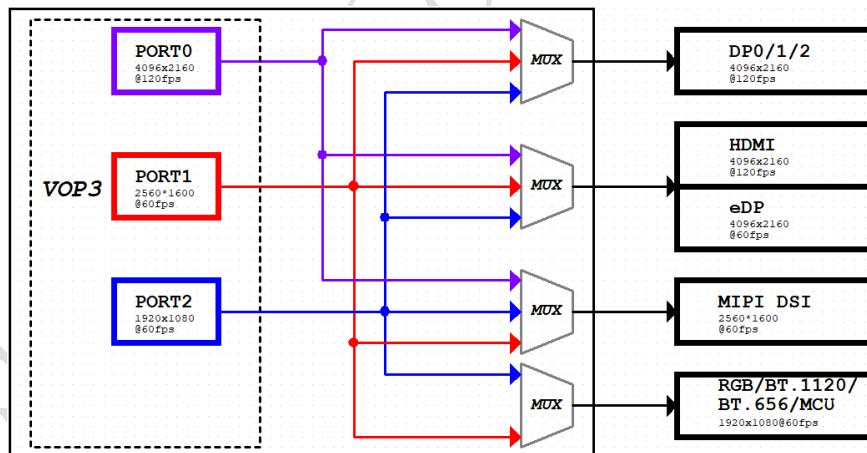


Figure 2-103 RK3576 VOP and video interface output path

2.3.8.1 HDMI2.1/eDP TX Interface

The RK3576 has a built-in HDMI/eDP TX Combo PHY.

The HDMI/eDP TX Combo PHY supports the following two modes:

- HDMI TX Mode: supports up to HDMI2.1, supports HDMI FRL mode and is backward compatible with HDMI TMDS mode, supports RGB/YUV444/YUV422/YUV420 (Up to 10bit) format.
- eDP TX Mode: Supports up to eDP1.3, maximum resolution of 4K@60Hz, and RGB/YUV444/YUV422(Up to 10bit) format.

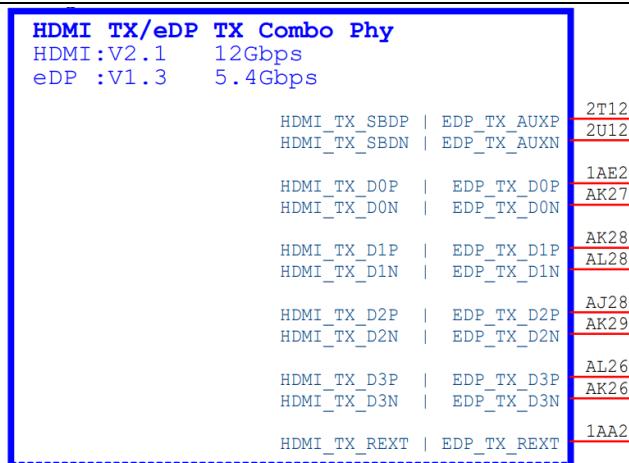


Figure 2-104 RK3576 HDMI/eDP Combo PHY pin

HDMI/EDP_TX_REXT is the external reference resistor pin for HDMI/eDP Combo PHY, external 8.2K resistor with 1% accuracy to ground, the resistor value must not be changed, and the layout is placed close to the RK3576 chip pin.



Figure 2-105 RK3576 HDMI/EDP_TX_REXT pin

● HDMI2.1 TX Mode

The RK3576 supports HDMI2.1 and is compatible with HDMI2.0 and HDMI1.4.

HDMI2.1 operates in FRL mode; and when HDMI2.0 or below modes, it operates in TMDS mode.

AC coupling voltage mode driver is used.

As shown in the figure below, the AC coupling capacitance tolerance value is 220nF, which shall not be changed arbitrarily, and the AC coupling capacitor is recommended to use 0201 package, lower ESR and ESL, which also reduces the impedance change on the line.

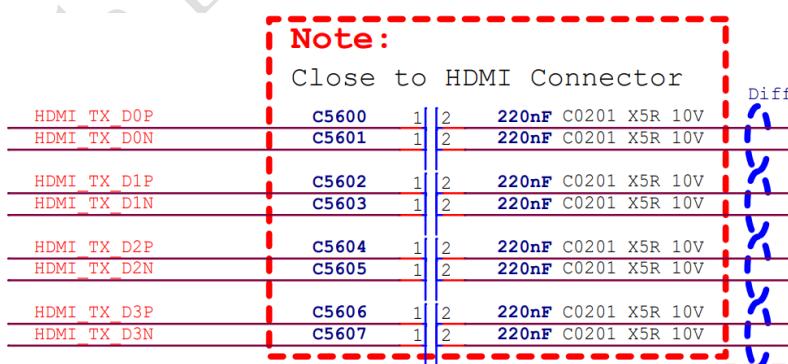


Figure 2-106 RK3576 HDMI TX AC coupling capacitor peripheral circuitry

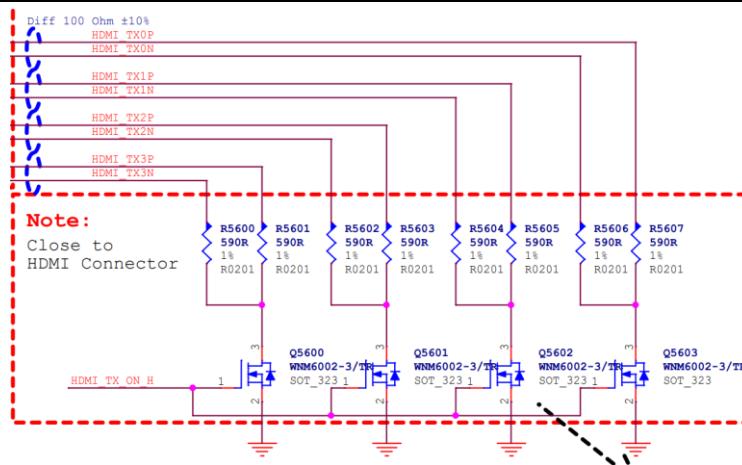


Figure 2-107 RK3576 HDMI TX mode peripheral circuitry

- Working in HDMI2.1 mode, HDMI_TX_ON_H is configured low and the four MOS tubes do not conduct.
- When working in HDMI2.0 and below modes, HDMI_TX_ON_H is configured high, the MOS tubes will conduct, and the 590ohm resistor to ground and the 50ohm resistor pull-up on the Sink side form a DC bias of about 3V.
- If only work in HDMI2.0 and below mode, the external is HDMI A seat, you can use the cost-saving scheme, consider the need for HDMI certification, you can delete the three MOS tubes, the 590ohm resistor to ground merged with the MOS after the MOS is connected, AC capacitance can not be deleted, see the following design schematic.
- If only work in HDMI2.0 and the following modes, the board docking HDMI receiver chip (such as RK628F), do not need HDMI_TX_ON_H control MOS tube open/close, MOS tubes can be deleted, leaving only eight 590ohm directly to ground, AC capacitors can not be deleted.

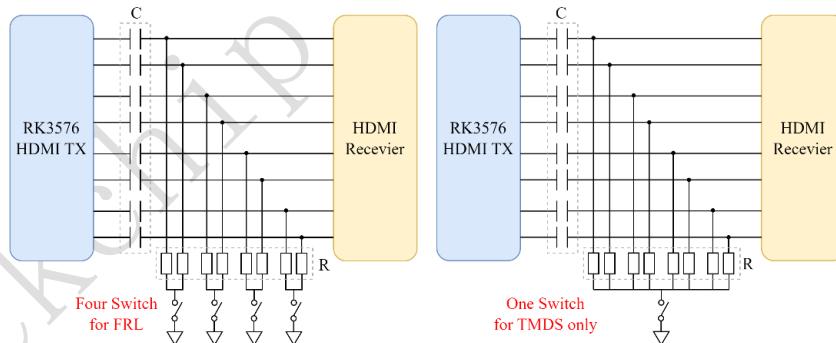


Figure 2-108 RK3576 HDMI TMDS only mode peripheral circuitry



Note

Note1: If you only need to support HDMI2.0 and below modes, the MOS can not be omitted. It's need to ensure that when the machine is not powered on, the tube can not be on, because the HDMI CTS Test ID 7-3 TMDS Voff test item requires that the DUT is not powered on, the Voff voltage must be within AVcc +10mV, otherwise this test item can not be passed;

Note2: Control MOS tube Coss can not be too large, otherwise it will affect the signal quality, it is recommended to follow the reference diagram model or the corresponding Coss value.

FRL mode: In the traditional TMDS architecture, a separate channel is used to transmit the Clock, but in the FRL architecture, the Clock is embedded in the Data channel, and the Clock is resolved by Clock Recovery at the Sink side.

Table 2-32 Relationship between FRL rate and channel

Channel rate	Channels
3Gbps	3
6Gbps	3
6Gbps	4
8Gbps	4
10Gbps	4
12Gbps	4

The HPDIN signal on the HDMI2.1 connector block is multiplexed with HDMI_TX_SBDN, and when HDMI device insertion is detected, HDMITX_HPDIN_M0 outputs a high level to notify RK3576.

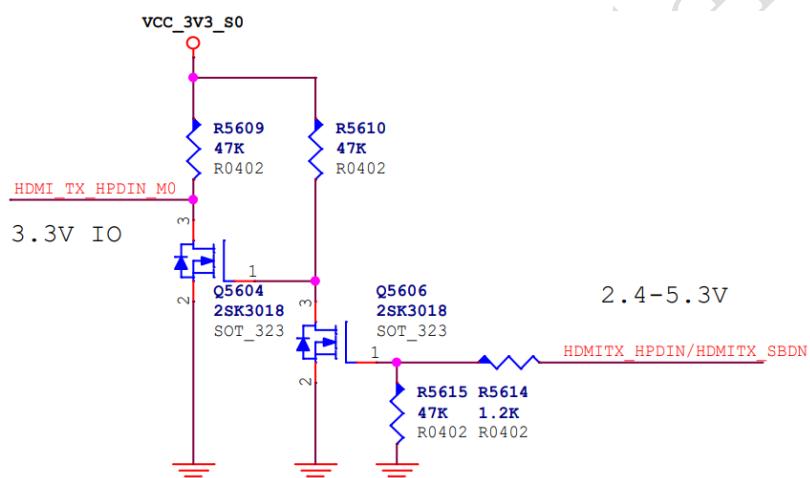


Figure 2-109 RK3576 HDMI TX HPD circuit

HDMI_TX_HPDIN is multiplexed in the common GPIO domain, the level changes with the voltage of the power domain where it is located, the power domain supply voltage, and the pull-up resistor power supply of the peripheral circuits must be adjusted synchronously.

HDMI_TX_HPDIN is multiplexed in two different power domains, one in the IOs of the VCCIO6 power domain and one in the IOs of the PMUIO1 power domain.

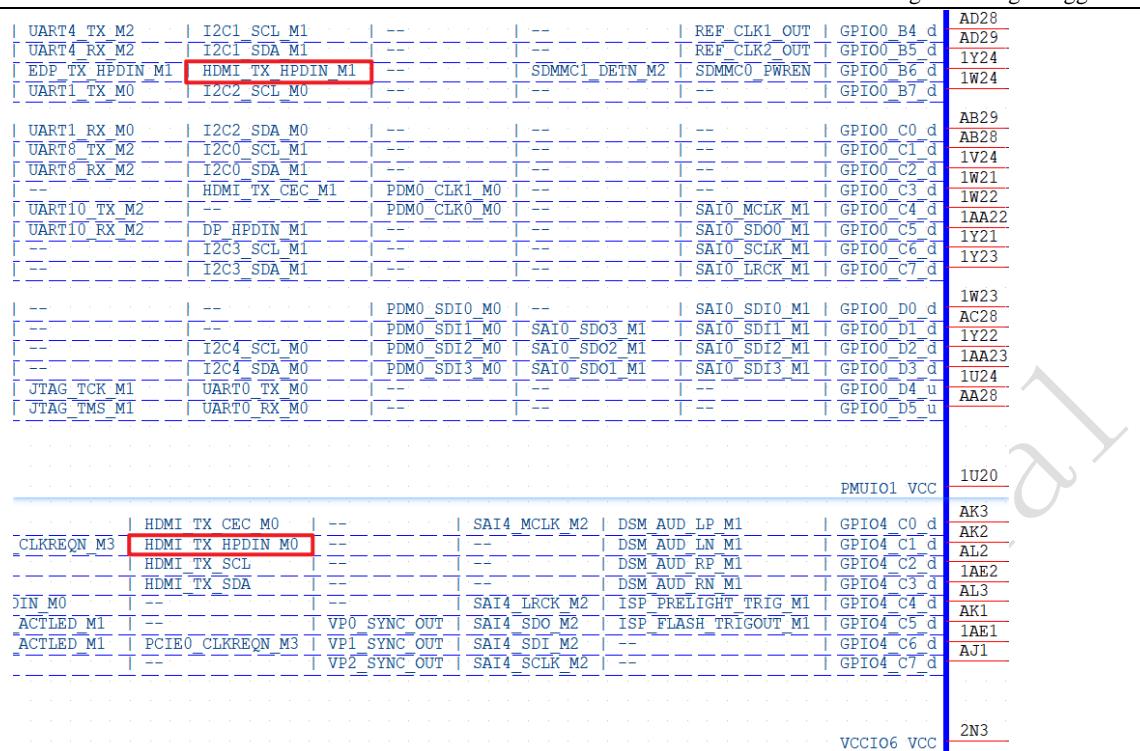


Figure 2-110 RK3576 HDMI_TX_HPDIN M0/M1 function pin

HDMI_TX_CEC is the HDMI controller CEC function multiplexed to the ordinary GPIO function, the level follow with the power domain voltage, the power domain power supply voltage has changed, the pull-up resistor power supply of the peripheral circuits must be adjusted synchronously.

HDMI_TX_CEC are multiplexed in two locations, one in the VCCIO6 power domain's IO, one in the PMUIO1 power domain's IO.

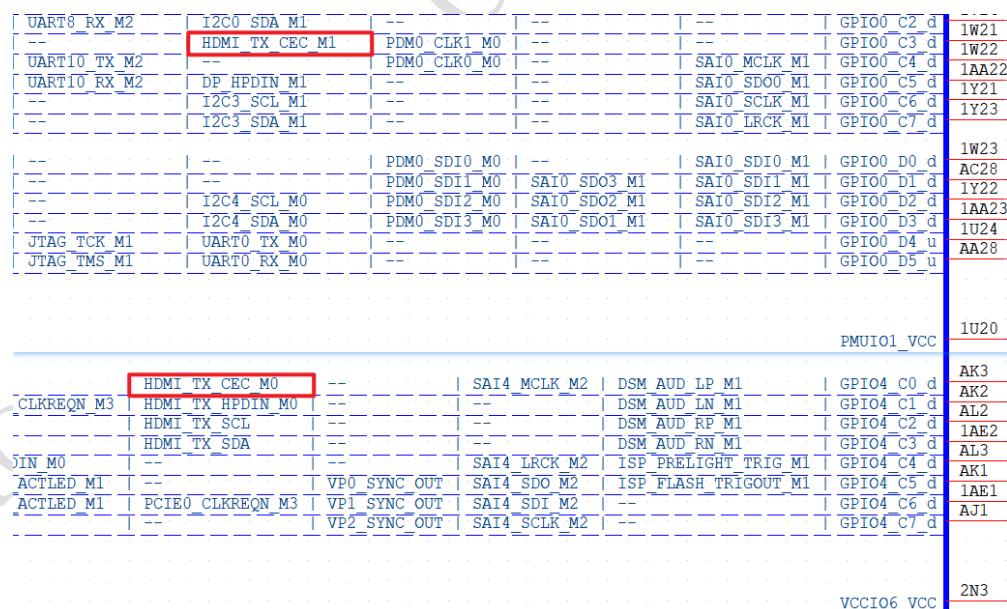


Figure 2-111 RK3576 HDMI_TX_CEC M0/M1 function pin

The CEC protocol specifies a 3.3V level, but the protocol requires that 3.3V be applied to the CEC pin through a 27K resistor, and leakage is not allowed to exceed 1.8uA.

Test ID 7-15: CEC Line Degradation

Reference	Requirement
[HDMI: Table 4-40] CEC line Electrical Specifications for all Configurations	A device with power removed (from the CEC circuitry) shall not degrade communication between other CEC devices (e.g. the line shall not be pulled down by the powered off device). Maximum CEC line leakage current must be $\leq 1.8\mu A$

Figure 2-112 HDMI CEC protocol requirements

The RK3576 IO Domain will have leakage on the IO if there is voltage on the IO when it is not powered up. For example, RK3576 has been powered off, but the HDMI cable is still connected to the Sink side (TV or monitor), at this time there is power at the Sink side of the CEC, which will leak through the HDMI cable to the RK3576 IO, resulting in CEC leakage of more than 1.8uA, so it is necessary to add an external isolation circuit. As shown in the figure below, the figure R5619 resistance value of 27Kohm and shall not be arbitrarily modified, Q5608 default selection of 2SK3018, if you want to change to other models, the junction capacitance must be equivalent, if the junction capacitance is too large, not only affect the work, but also can not pass the certification.

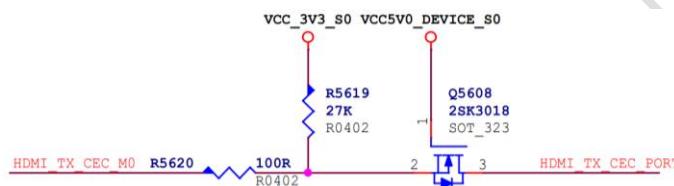


Figure 2-113 HDMI TX CEC isolation circuit

HDMI_TX_DDC_SCL/DDC_SDA is the HDMI TX controller I2C/DDC bus, the function is distributed in the VCCIO6 power domain's IO, level follow with the power domain's voltage, the power domain power supply voltage changed, the pull-up resistor power supply of peripheral circuits must be adjusted synchronously.

DDC_SCL/DDC_SDA protocol is 5V level, RK3576 IO does not support the 5V level, so must increase the level conversion circuit, the default use of MOS level conversion, MOS model default selection 2SK3018, if you want to change the other models, the junction capacitance must be match, if the junction capacitance is too large, affecting timing, not only affects the work, but also can not be certified. Certification.

Pull-up resistor is recommended to refer to the default value, do not modify.

D5601 diode must not be deleted, used to prevent leakage from the Sink side to VCC5V0_DEVICE_S0.

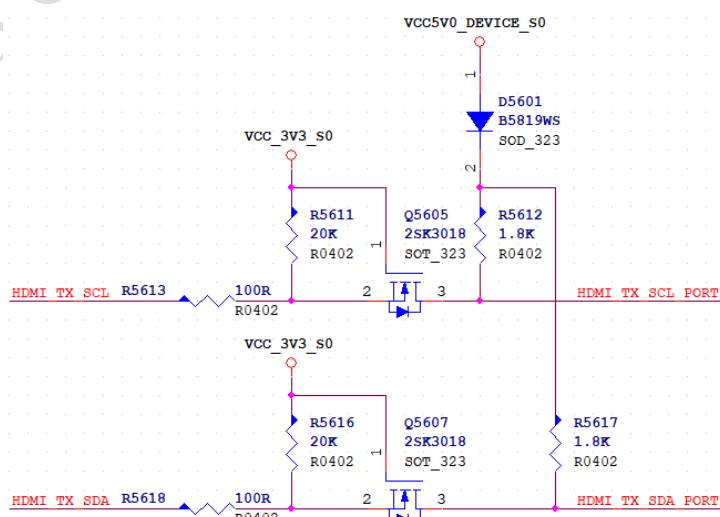


Figure 2-114 HDMI TX DDC level conversion circuit

HDMI seat Pin18's voltage needs to be guaranteed between 4.8-5.3V, the pin needs to be placed 1uF decoupling capacitor, and close to the HDMI seat pin placement when layout.

In order to strengthen the anti-static ability, the signal must be reserved ESD devices, HDMI2.1 signal ESD parasitic capacitance shall not exceed 0.2pF, other signals ESD parasitic capacitance is recommended to use no more than 1pF.

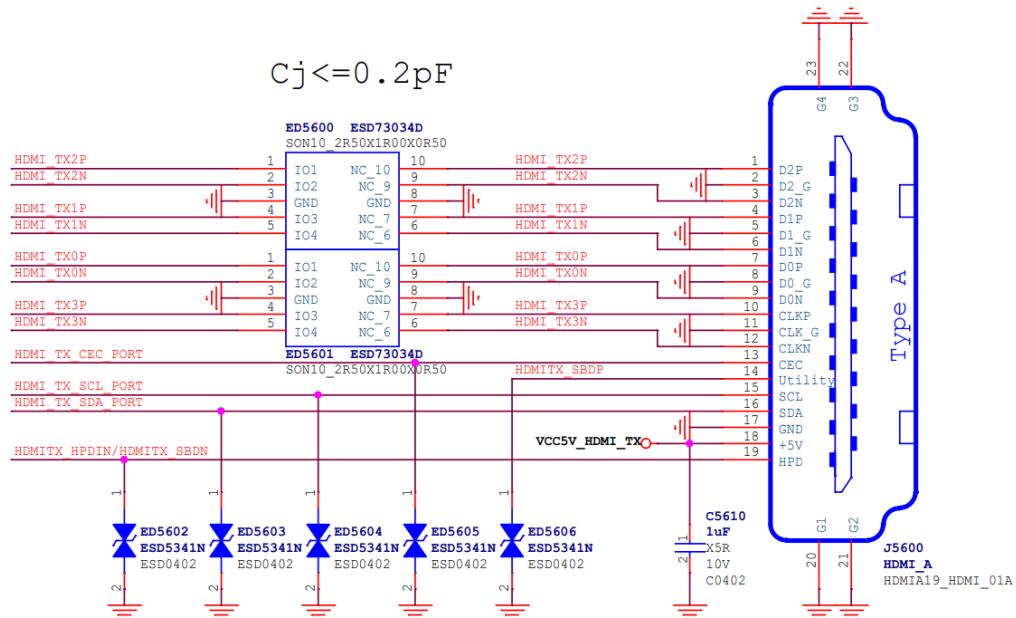


Figure 2-115 HDMI TX connector ESD circuit

The recommended HDMI TX matching design as follow:

Table 2-33 RK3576 HDMI TX interface design

Signal	Connection method	Description
HDMI_TX_D0P/D0N	Series 220nF capacitor (0201 package), 590ohm resistor to ground	RFL mode Lane0/TMDS data Lane0 output
HDMI_TX_D1P/D1N	Series 220nF capacitor (0201 package), 590ohm resistor to ground	RFL mode Lane1/TMDS data Lane1 output
HDMI_TX_D2P/D2N	Series 220nF capacitor (0201 package), 590ohm resistor to ground	RFL mode Lane2/TMDS data Lane2 output
HDMI_TX_D3P/D3N	Series 220nF capacitor (0201 package), 590ohm resistor to ground	RFL mode Lane3/TMDS clock output
HDMI_TX_SBDP/SBDN	Series 1uF capacitor (0201 package)	ARC/eARC channel
HDMI/EDP_TX_REXT	8200 ohm with 1% accuracy resistor to ground	HDMI/EDP_TX PHY external reference resistor
HDMI_TX_HPD	MOS isolated conversion	HDMI insert detection
HDMI_TX_CEC	MOS isolated conversion	HDMI CEC signal
HDMI_TX_SCL	MOS level conversion	HDMI DDC clock
HDMI_TX_SDA	MOS level conversion	HDMI DDC data input/output

- eDP TX mode

Support eDP V1.3 version, total 4Lane, eDP TX max output resolution up to 4K@60Hz.

- Each Lane rate can support 1.62/2.7/5.4Gbps;
- Support 1Lane or 2Lane or 4Lane mode;
- Supports AUX channel with rate up to 1Mbps;
- Does not support Swap.

eDP_TX_D0P/D0N, eDP_TX_D1P/D1N, eDP_TX_D2P/D2N, eDP_TX_D3P/D3N needs connect a 100nF AC coupling capacitors(0201 packages recommended) in series for lower ESR and ESL, and also reduces impedance variations on the line, and close to the RK3576 pin placement when layout.

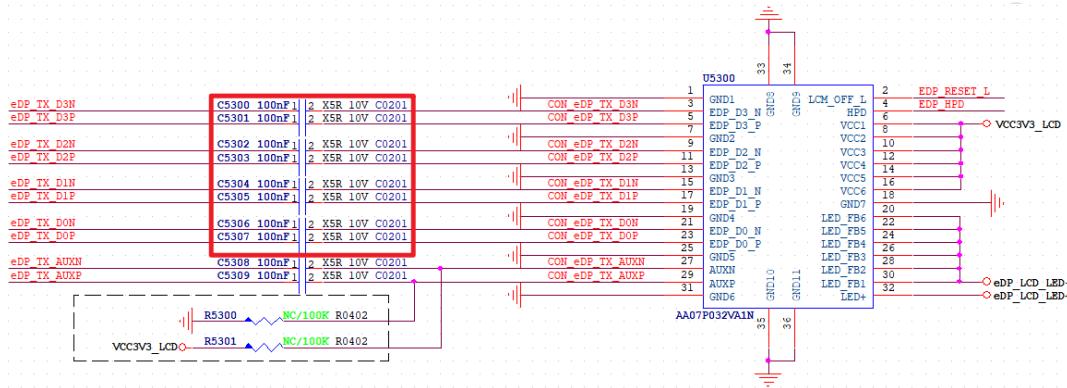


Figure 2-116 RK3576 eDP TX signal AC coupling capacitor

eDP_TX_AUXP/AUXN need to be connected in series with a 100nF AC coupling capacitor close to the interface end, AUXP need to reserve a 100Kohm resistor to ground, and AUXN reserve a 100K resistor to pull-up to 3.3V. In eDP V12 protocol version or above, the pull-up and down resistors can be left unposted.

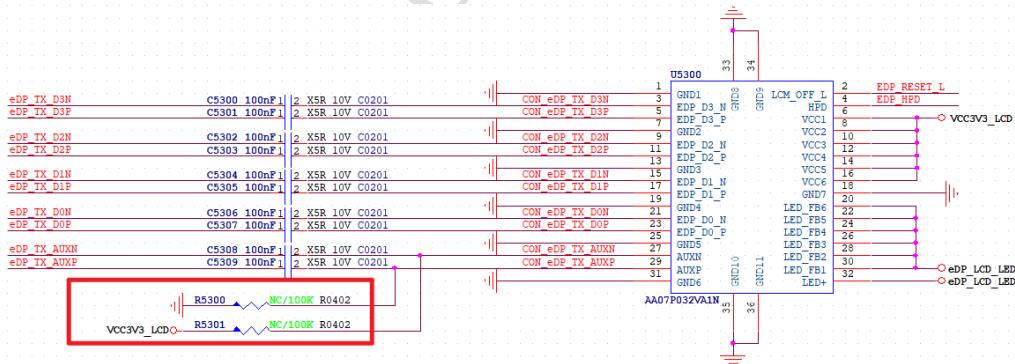


Figure 2-117 RK3576 eDP TX AUX signal pull-up/down resistor

the recommended eDP TX PHY interface matching design as follow:

Table 2-34 RK3576 eDP TX PHY interface design

Signal	Connection method	Description
eDP_TX_D0P/D0N	Series 100nF capacitor (0201 package)	eDP data Lane0 output
eDP_TX_D1P/D1N	Series 100nF capacitor (0201 package)	eDP data Lane1 output
eDP_TX_D2P/D2N	Series 100nF capacitor (0201 package)	eDP data Lane2 output
eDP_TX_D3P/D3N	Series 100nF capacitor (0201 package)	eDP data Lane3 output
eDP_TX_AUXP/AUXN	Series 100nF capacitor	eDP AUX channel

2.3.8.2 MIPI_DCPHY_TX Interface

The RK3576 has a MIPI D-PHY/C-PHY Combo PHY TX:

- D-PHY supports version V2.0, D-PHY mode with 0/1/2/3 Lane, 2 wires per Lane; maximum transfer rate 2.5Gbps/Lane.
- MIPI_DPHY_TX max resolution support 2560x1600@60Hz.
- C-PHY supports version V1.1, C-PHY mode with 0/1/2 Trio, 3 wires per Trio A/B/C; maximum transmission rate 1.7Gps/Trio.
- MIPI_CPHY_TX supports maximum resolution of 2560x1600@60Hz.

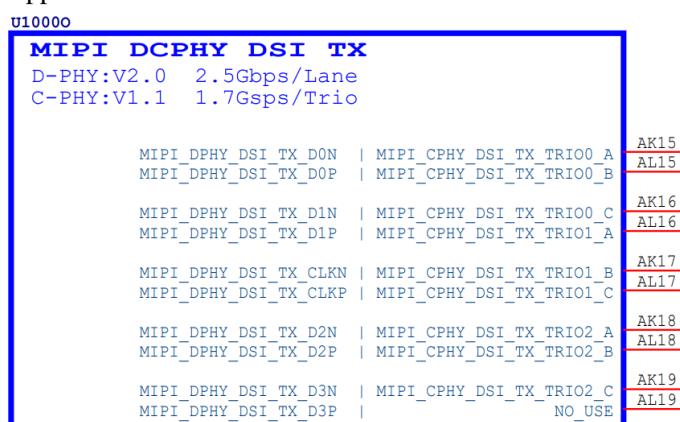


Figure 2-118 RK3576 MIPI DC PHY TX signal pin

DPHY and CPHY configuration support:

- The TX and RX of the MIPI D-PHY/C-PHY Combo PHY can only support simultaneous configuration into DPHY TX, DPHY RX modes or simultaneous configuration into CPHY TX, CPHY RX modes, and does not support one configuration into DPHY TX and one into CPHY RX;

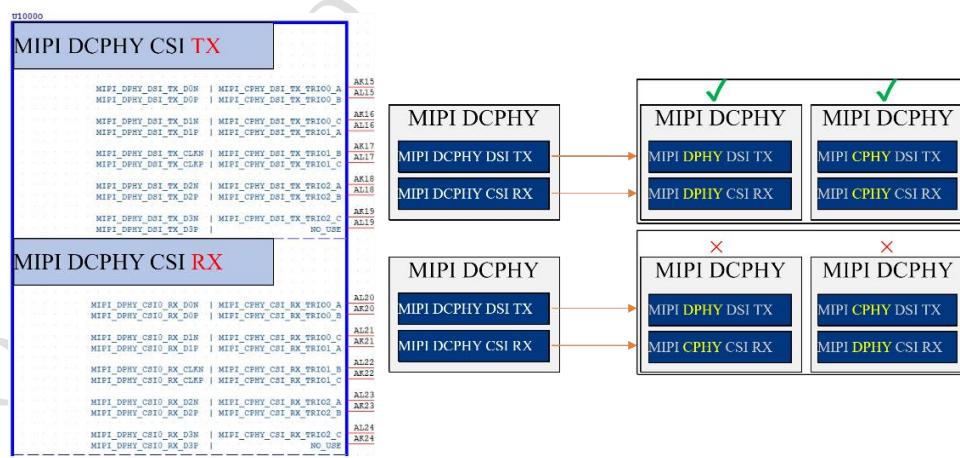


Figure 2-119 RK3576 MIPI DC PHY Combo PHY combination

MIPI DC PHY mode supports the following when working in D-PHY:

- supports 4Lane mode, MIPI_DPHY_TX_D[3:0] data refer to MIPI_DPHY_TX_CLK.

MIPI DC PHY mode supports the following when working in C-PHY:

- supports 0/1/2 Trio, 3 wires per Trio A/B/C, MIPI_CPHY_TX_TRIO[2:0]_A, MIPI_CPHY_TX_TRIO[2:0]_B, MIPI_CPHY_TX_TRIO[2:0]_C.

Please note in MIPI D-PHY/C-PHY Combo PHY TX design:

- In order to improve the MIPI D-PHY/C-PHY Combo PHY TX performance, the decoupling capacitors for each power supply of PHY should not be deleted, and please place them close to the pins during the layout (RX and TX are Combo PHYs with the same power supply).
- MIPI D-PHY/C-PHY Combo PHY TX matching design recommendations are shown in the table below:

Table 2-35 RK3576 MIPI D-PHY/C-PHY Combo PHY TX interface design

Signal	Connection method	Description
MIPI_DPHY_TX_D0P/D0N	Direct connection, common mode inductance reserved for electromagnetic radiation suppression	MIPI_DPHY_TX data Lane0 output
MIPI_DPHY_TX_D1P/D1N	Direct connection, common mode inductance reserved for electromagnetic radiation suppression	MIPI_DPHY_TX data Lane1 output
MIPI_DPHY_TX_D2P/D2N	Direct connection, common mode inductance reserved for electromagnetic radiation suppression	MIPI_DPHY_TX data Lane2 output
MIPI_DPHY_TX_D3P/D3N	Direct connection, common mode inductance reserved for electromagnetic radiation suppression	MIPI_DPHY_TX data Lane3 output
MIPI_DPHY_TX_CLKP/CLKN	Direct connection, common mode inductance reserved for electromagnetic radiation suppression	MIPI_DPHY_TX clock output
MIPI_CPHY_TX_TRIO0_A/B/C	Direct connection, common mode inductance reserved for electromagnetic radiation suppression	MIPI_CPHY_TX_TRIO0 output
MIPI_CPHY_TX_TRIO1_A/B/C	Direct connection, common mode inductance reserved for electromagnetic radiation suppression	MIPI_CPHY_TX_TRIO1 output
MIPI_CPHY_TX_TRIO2_A/B/C	Direct connection, common mode inductance reserved for electromagnetic radiation suppression	MIPI_CPHY_TX_TRIO2 output

2.3.8.3 DP TX Interface

The RK3576 supports a DP1.4 TX PHY (and USB3 OTG0 Combo) with a maximum output resolution of 4K@YUV422-120Hz.

- Each Lane rate can support 1.62/2.7G/5.4/8.1Gbps;
- Supports 1Lane or 2Lane or 4Lane mode;
- supports RGB/YUV444/YUV422/YUV420 (up to 10bit) format;
- supports Multi Stream Transport (MST).

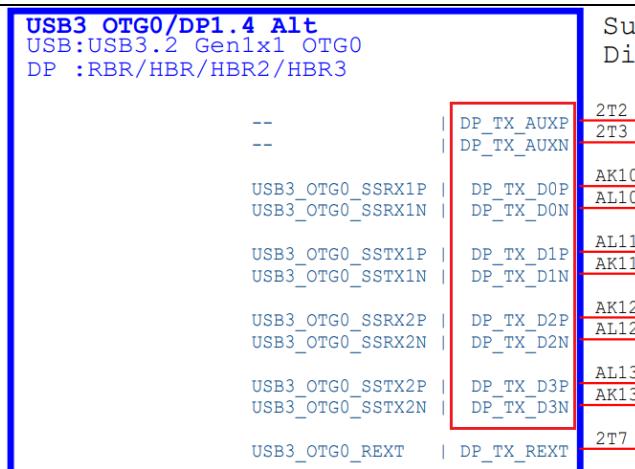


Figure 2-120 RK3576 DP TX pin

- Supports Swap on and Swap off mode

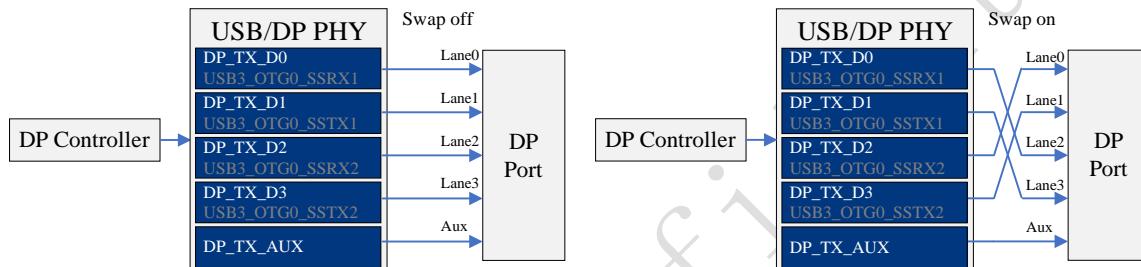


Figure 2-121 RK3576 DP Swap ON/OFF mode

- Supports 3 Channels MST(Multi-Stream Transport) display. MST supports triple displays up to 4096x2160@60Hz, 2560x1600@60Hz, 1920x1080@60Hz.

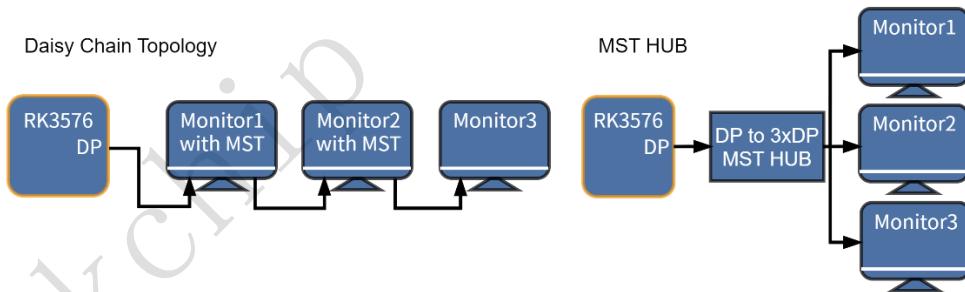


Figure 2-122 RK3576 DP 3 Channels MST mode

Please note in DP TX PHY design:

- In order to improve the DP TX PHY performance, the decoupling capacitors of each power supply of PHY, **USB3_OTG0_DP_TX_AVDD0V85**, **USB3_OTG0_DP_TX_DVDD0V85**, **USB3_OTG0_DP_TX_AVDD1V8**, shall not be deleted, and shall be placed close to the pins during layout.
- DP_TX_D0P/D0N**, **DP_TX_D1P/D1N**, **DP_TX_D2P/D2N**, **DP_TX_D3P/D3N** need to be connected in series with 100nF AC coupling capacitors, AC coupling capacitors are recommended to use 0201 packages, lower ESR and ESL, and also reduces impedance changes on the line. Layout is placed close to the RK3576 pin;

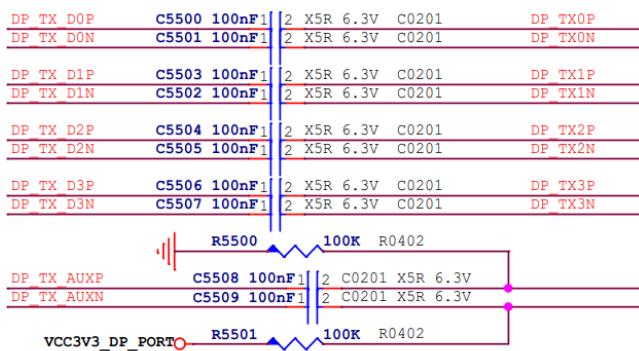


Figure 2-123 RK3576 DP TX signal AC coupling capacitor

- USB3_OTG0_REXT/DP_TX_REXT is the external reference resistor pin for USB DP Combo PHY, external 8200ohm precision 1% resistor to ground, resistor value must not be changed, layout placed close to the RK3576 chip pin.



Figure 2-124 RK3576 DP_TX_REXT pin

The recommended DPTX PHY interface matching design as follow:

Table 2-36 RK3576 DP TX PHY interface design

Signal	Connection method	Description
DP_TX_D0P/D0N	Series 100nF capacitor (Q201 package)	DP data Lane0 output
DP_TX_D1P/D1N	Series 100nF capacitor (Q201 package)	DP data Lane1 output
DP_TX_D2P/D2N	Series 100nF capacitor (Q201 package)	DP data Lane2 output
DP_TX_D3P/D3N	Series 100nF capacitor (Q201 package)	DP data Lane3 output
DP_TX_AUXP/AUXN	Series 100nF capacitor	DP AUX channel
USB3_OTG0_REXT/DP_TX_REXT	8200ohm resistor with 1% accuracy to ground	External Reference Resistor for USB/DP PHY

2.3.8.4 LCDC/BT1120/MCU TX Interface

RK3576 LCDC TX interface, supports parallel 24bit RGB mode, 16bit BT1120 mode, 8bit BT656 mode and MCU mode, of which, RGB, BT1120 and BT656 resolutions are supported as follows:

- 24bit RGB mode: Maximum output resolution up to 1920x1080@60Hz;
- 16bit BT1120 mode: Maximum output resolution up to 1920x1080@60Hz;
- 8bit BT656 mode: maximum resolution up to 720x576@60Hz supports PAL and NTSC;

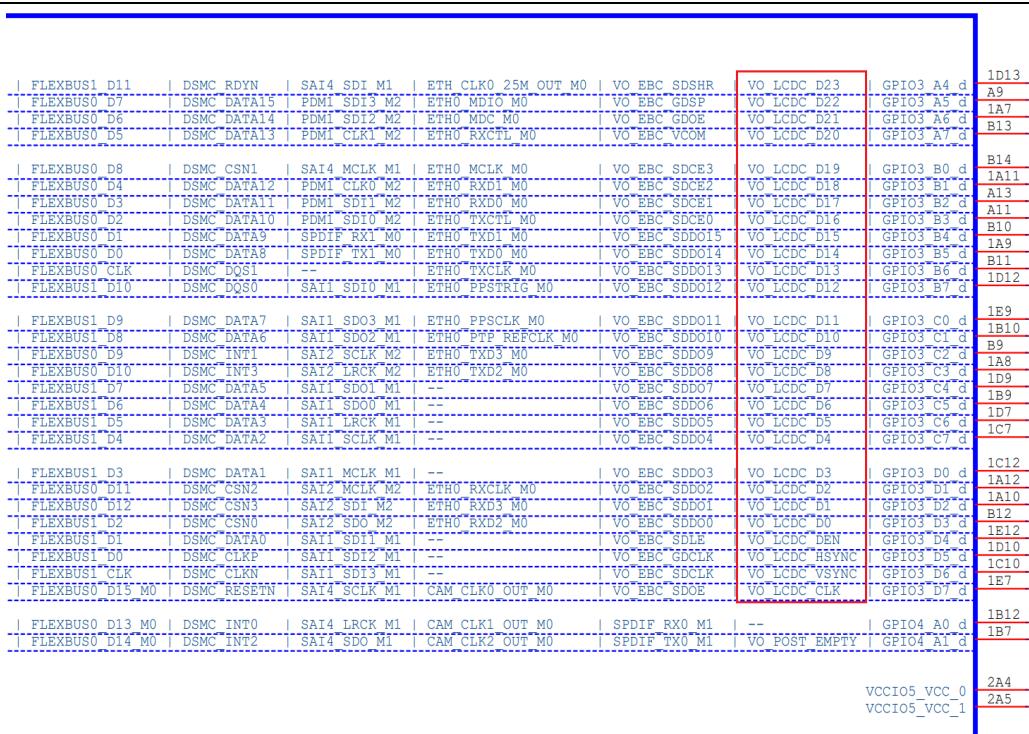


Figure 2-125 RK3576 VOP RGB/BT1120/MCU function pin

RGB、BT1120、BT656、MCU multiplexing relation as follow:

Table 2-37 RK3576 RGB、BT1120、BT656、MCU multiplexing relation table

interface	RGB888 (MCU24)	RGB666	RGB565	BT656(8bit)	BT1120 (16bit)	MCU(8bit)	MCU(16bit)
dclk	dclk	dclk	dclk	dclk	dclk	mcu_r_s	mcu_r_s
vsync	vsync	vsync	vsync			mcu_csn	mcu_csn
hsync	hsync	hsync	hsync			mcu_wrn	mcu_wrn
den	den	den	den				
data	data	data	data	data[7:0]	data[15:0]	data[7:0]	data[15:0]
VO_LCDC_D23	✓R7	✓	✓	✗	✓ (D15)	✓ (D7_m1)	✓ (D15)
VO_LCDC_D22	✓R6	✓	✓	✗	✓ (D14)	✓ (D6_m1)	✓ (D14)
VO_LCDC_D21	✓R5	✓	✓	✗	✓ (D13)	✓ (D5_m1)	✓ (D13)
VO_LCDC_D20	✓R4	✓	✓	✗	✓ (D12)	✓ (D4_m1)	✓ (D12)
VO_LCDC_D19	✓R3	✓	✓	✗	✓ (D11)	✓ (D3_m1)	✓ (D11)
VO_LCDC_D18	✓R2	✓	✗	✗	✗	✗	✗
VO_LCDC_D17	✓R1	✗	✗	✗	✗	✗	✗
VO_LCDC_D16	✓R0	✗	✗	✗	✗	✗	✗
VO_LCDC_D15	✓G7	✓	✓	✗	✓ (D10)	✓ (D2_m1)	✓ (D10)
VO_LCDC_D14	✓G6	✓	✓	✗	✓ (D9)	✓ (D1_m1)	✓ (D9)
VO_LCDC_D13	✓G5	✓	✓	✗	✓ (D8)	✓ (D0_m1)	✓ (D8)
VO_LCDC_D12	✓G4	✓	✓	✓D7	✓ (D7)	✓ (D7_m0)	✓ (D7)
VO_LCDC_D11	✓G3	✓	✓	✓D6	✓ (D6)	✓ (D6_m0)	✓ (D6)
VO_LCDC_D10	✓G2	✓	✓	✓D5	✓ (D5)	✓ (D5_m0)	✓ (D5)
VO_LCDC_D9	✓G1	✗	✗	✗	✗	✗	✗
VO_LCDC_D8	✓G0	✗	✗	✗	✗	✗	✗
VO_LCDC_D7	✓B7	✓	✓	✓D4	✓ (D4)	✓ (D4_m0)	✓ (D4)
VO_LCDC_D6	✓B6	✓	✓	✓D3	✓ (D3)	✓ (D3_m0)	✓ (D3)
VO_LCDC_D5	✓B5	✓	✓	✓D2	✓ (D2)	✓ (D2_m0)	✓ (D2)
VO_LCDC_D4	✓B4	✓	✓	✓D1	✓ (D1)	✓ (D1_m0)	✓ (D1)
VO_LCDC_D3	✓B3	✓	✓	✓D0	✓ (D0)	✓ (D0_m0)	✓ (D0)
VO_LCDC_D2	✓B2	✓	✗	✗	✗	✗	✗
VO_LCDC_D1	✓B1	✗	✗	✗	✗	✗	✗
VO_LCDC_D0	✓B0	✗	✗	✗	✗	✗	✗
Remarks		Select high order	Not supported M1	Support YC SWAP	Support M1	Select high order	

- BT1120 output interface data correspondence, support YC Swap
- RGB666, RGB565, MCU 16bit, BT1120 selects high bit to connect with peripherals
- BT656 only M0 does not support multiplexed M1, MCU 8bit supports multiplexed M0, M1

Table 2-38 RK3576 BT1120 output format list

Pin Name	Default mode		Swap opened	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1
BT1120_D0	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]
BT1120_D1	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]
BT1120_D2	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]
BT1120_D3	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]
BT1120_D4	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]
BT1120_D5	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]
BT1120_D6	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]
BT1120_D7	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]
BT1120_D8	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]
BT1120_D9	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]
BT1120_D10	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]
BT1120_D11	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]
BT1120_D12	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]
BT1120_D13	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]
BT1120_D14	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]
BT1120_D15	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]

Please note in RGB/BT1120/MCU output interface design:

- These parallel signal output interface power domains are powered by VCCIO5. In actual product design, the corresponding power supply needs to be selected according to the actual IO power requirement (1.8V or 3.3V) of the peripheral devices, and it must be consistent;
- In order to improve the performance of the parallel signal output interface, the decoupling capacitor of the VCCIO5 power supply must not be deleted and should be placed close to the pin during layout.

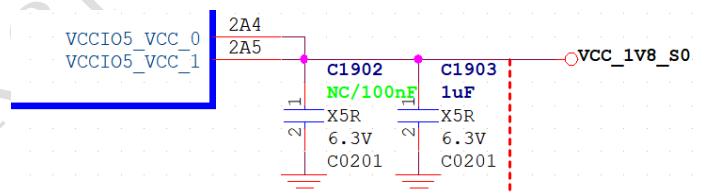


Figure 2-126 decoupling capacitor for RK3576 LCDC/BT1120/MCU VCCIO5 power

Parallel output interface pull-up/down and matching design recommendations are shown in the table:

Table 2-39 RK3576 LCDC output interface design

Signal	Chip internal pull-up/down configurations	Connection method	Description (chip end)
BT1120_D[15: 0]	pull-down	Direct connection, it is recommended to reserve a series resistance near the chip end.	BT1120 data output

Signal	Chip internal pull-up/down configurations	Connection method	Description (chip end)
BT1120_CLK	/	Series 22ohm resistor near the device end	BT1120 clock output
RGB_D[24:0]	pull-down	Direct connection, it is recommended to reserve a series resistance near the chip end.	RGB data output
RGB_CLK	/	Series 22ohm resistor near the device end	RGB clock output
MCU_D[16:0]	pull-down	Direct connection, it is recommended to reserve a series resistance near the chip end.	MCU data output
MCU_RS	pull-down	Direct connection, it is recommended to reserve a series resistance near the chip end.	Parameter , command selection
MCU_CSN	pull-down	Direct connection, it is recommended to reserve a series resistance near the chip end.	CS signal
MCU_WRN	pull-down	Direct connection, it is recommended to reserve a series resistance near the chip end.	Write enable signal
MCU_RDN	pull-down	Direct connection, it is recommended to reserve a series resistance near the chip end.	Read Enable signal, the chip does not support

- When board-to-board connection is achieved through the connector, it is recommended to string a resistor with a certain resistance value (between 22ohm-100ohm, subject to being able to satisfy the SI test) and reserve TVS devices.
- MCU_REN RK3576 chip does not support, this signal can read back the registers to get the status and version of the panel. When not connected to a master, the screen side is required to be held at a fixed high level.

2.3.8.5 EBC TX Interface

RK3576 chip has an EBC interface, is used to drive the E-ink e-ink screen TCON module, support 8bit/16bit output, up to 32 levels of grey scale, support for direct mode, LUT mode and three-window mode, holding window display mode support. Maximum resolution: 2560x1920@85Hz.

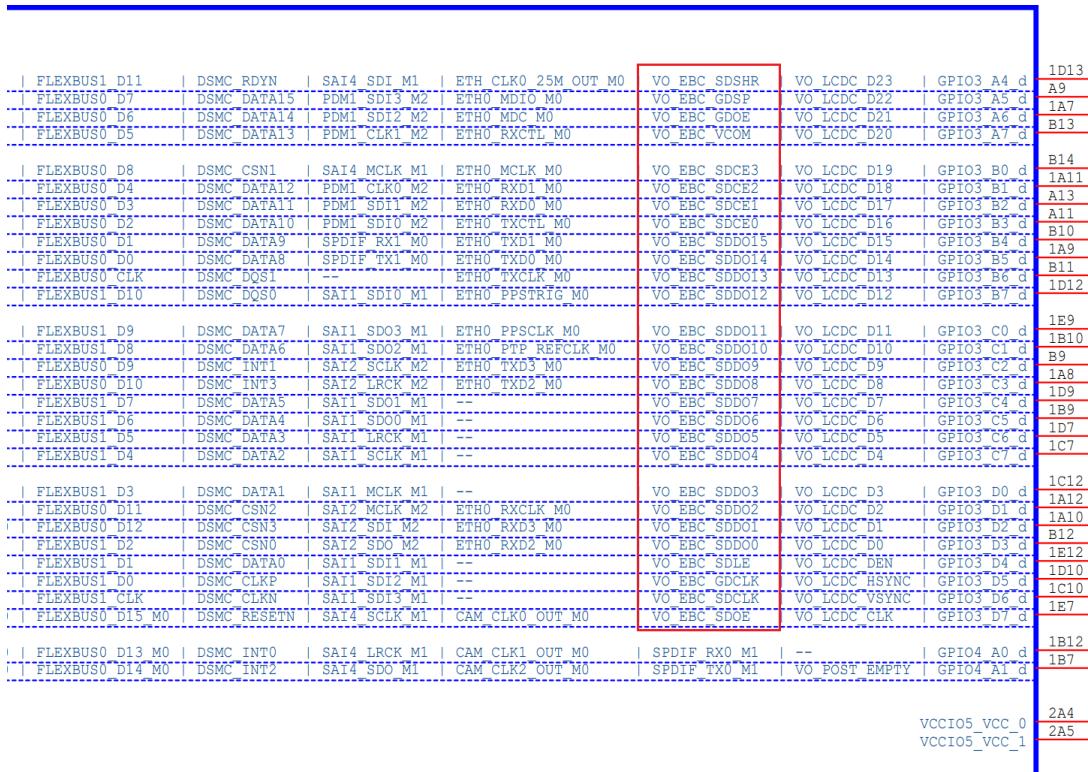


Figure 2-127 RK3576 VOP EBC function pin

Please note in the design of EBC output interface:

- The power domain of EBC output interface is VCCIO5 power supply. In actual product design, it is necessary to select the corresponding power supply according to the actual IO power supply requirement of the peripheral (1.8V or 3.3V), and it must be consistent.
 - To improve the performance of the EBC output interface, the decoupling capacitor of the VCCIO5 power supply must not be deleted, and please place it close to the pin when layout;

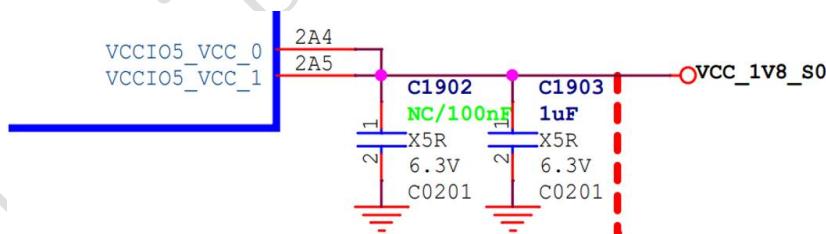


Figure 2-128 decoupling capacitor for RK3576 EBC VCCIO5

The recommended design of the EBC output interface pull-down and matching is shown in Table

Table 2-40 RK3576 EBC output interface design

Signal	Chip internal pull-up/down configurations	Connection method	Description (chip end)
EBC_SDDO[15:0]	pull-down	direct connect	Source driver data output
EBC_SDCE[3:0]	pull-down	direct connect	Source chip select/ Start pulse source driver
EBC_VCOM	pull-down	direct connect	Com voltage control
EBC_GDOE	pull-down	direct connect	Gate output enable

Signal	Chip internal pull-up/down configurations	Connection method	Description (chip end)
EBC_GDSP	pull-down	direct connect	Gate start pulse
EBC_SDSHR	pull-down	direct connect	Source driven shift register
EBC_SDLE	pull-down	direct connect	Source data latch enable
EBC_SDOE	pull-down	direct connect	Source data output enable
EBC_GDCLK	pull-down	direct connect	Gate driver clock
EBC_SDCLK	pull-down	direct connect	Source driver clock

- When board-to-board connection is achieved through the connector, it is recommended to connect a resistor of a certain resistance value in series (between 22ohm-100ohm, subject to the ability to satisfy the SI test) and to reserve a TVS device.

2.3.8.6 LCD Screen and Touch Screen Design Notes

- For the current limiting resistor on the FB side of the LED backlight boost IC, please choose 1% precision resistor and select the appropriate package size according to the power requirement.
- For the EN/PWM pin of the LED backlight boost IC, choose the GPIO with internal pull-down and external pull-down resistor to avoid the flashing screen phenomenon when powering up.
- LED backlight drive voltage output, please choose the appropriate rated voltage filter capacitor.
- For the Schottky diode of the LED backlight boost circuit, please choose the appropriate model according to the operating current and pay attention to the reverse breakdown voltage of the diode to avoid reverse breakdown at no load.
- For the inductor of LED backlight boost circuit, please match the inductance, saturation current, DCR, etc. according to the actual model.
- The signal level of the screen and touch screen should be matched with the IO driver level of the chip, such as RST/Stand by and other signals.
- The power supply of the screen must be controllable and not provided by default when powering up.
- The decoupling capacitors for the screen and touchscreen must not be deleted, they must be retained.
- The I2C bus of TP must add 2.2K pull-up to VCC3V3_TP power supply, it is recommended not to share the bus with other devices, if you must share, pay attention to the pull-up power supply and address conflict.
- For TP IC with Charge pump, please pay attention to the rated voltage of capacitor.
- For the screen, when connecting to the board via FPC, it is recommended to connect a resistor with a certain resistance value (between 22ohm-100ohm, subject to SI test), and reserve TVS devices.
- It is recommended to reserve common mode inductors at the interface for screens with serial interface.

2.3.9 Audio Circuit Design

2.3.9.1 Audio Subsystem Overview

The RK3576 provides rich audio interface capabilities and resources, with a total of 10 groups of SAI interfaces, 2 groups of PDM interfaces, 6 SPDIF_TX interfaces, 3 SPDIF_RX interfaces, 1 group of DSM interfaces, as well as 4 new ASRC processing units.

Among them, 5 groups of SAI interfaces, 2 groups of PDM interfaces, 2 SPDIF_TX interfaces, 2 SPDIF_RX interfaces, and 1 group of DSM interfaces are provided externally, and the IO domains of these interfaces are multiplexed as well as the power domains to which they belong are shown in the table below, for users to flexibly allocate their choices.

Table 2-41 RK3576 External Audio Interface and IO Multiplexing

External Interface	Multiplexing (M0)	Multiplexing (M1)	Multiplexing (M2)	Multiplexing (M3)
SAI0(4TX+4RX)	VCCIO4	PMUIO1	VCCIO0	-
SAI1(4TX+4RX)	VCCIO2	VCCIO5	-	-
SAI2(1TX+1RX)	VCCIO3	VCCIO4	VCCIO5	-
SAI3(1TX+1RX)	VCCIO0	VCCIO3	VCCIO4	VCCIO1
SAI4(1TX+1RX)	VCCIO2	VCCIO5	VCCIO6	VCCIO4
PDM0(8channel)	PMUIO1	VCCIO0	VCCIO3	VCCIO4
PDM1(8channel)	VCCIO4	VCCIO2	VCCIO5	-
SPDIF_TX0	VCCIO2 GPIO4_B5	VCCIO5 GPIO4_A1	VCCIO4 GPIO2_D7	-
SPDIF_TX1	VCCIO5 GPIO3_B5	VCCIO4 GPIO3_A3	VCCIO3 GPIO1_D5	-
SPDIF_RX0	VCCIO2 GPIO4_B4	VCCIO5 GPIO4_A0	VCCIO4 GPIO2_D6	-
SPDIF_RX1	VCCIO5 GPIO3_B4	VCCIO4 GPIO3_A2	VCCIO3 GPIO1_D4	-
DSM(2channal,Stereo)	VCCIO1	VCCIO6	-	-

The remaining unspecified audio interfaces are used for the matching of video input/output interfaces, and their internal power domains are as follows, which are consistent with the power domains belonging to their matching corresponding video interfaces, and the following table also gives the relevant information about their internal multiplexing assignments:

Table 2-42 RK3576 audio interface for internal use and multiplexing

interface for internal (related to video)	note
SAI5(4RX only)	HDMI TX, ARC
SAI6(4TX+4RX)	Reuse in two places 1. HDMI TX, audio play 2. eDP, audio play
SPDIF_RX2	HDMI TX, ARC

interface for internal (related to video)	note
SPDIF_TX2	Reuse in two places 1. HDMI TX, audio play 2. eDP, audio play
SAI7(4TX only)	DP, audio play/MST
SAI8(4TX only)	DP, audio play/MST
SAI9(4TX only)	DP, audio play/MST
SPDIF_TX3	DP, audio play/MST
SPDIF_TX4	DP, audio play/MST
SPDIF_TX5	DP, audio play/MST

2.3.9.2 Audio Subsystem Block Diagram

The RK3576 audio subsystem block diagram is shown below. It includes information about the external/internal interfaces and their internal power domain PDs:

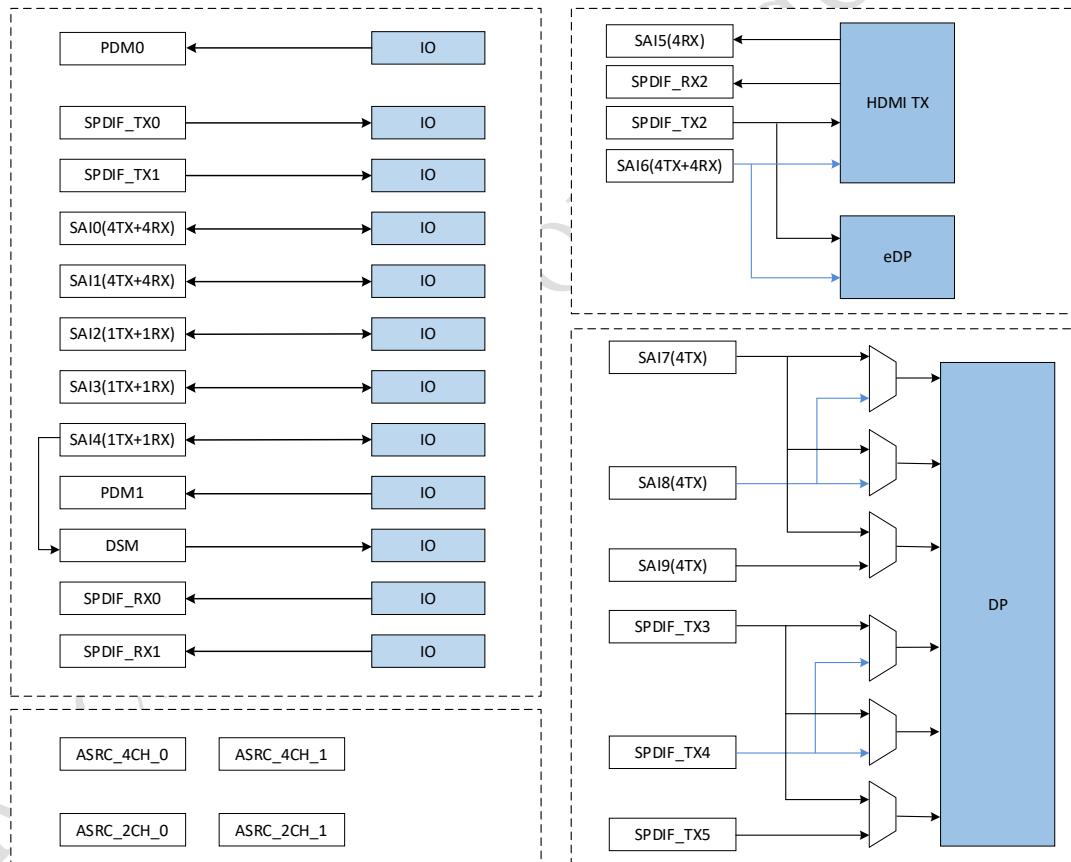


Figure 2-129 audio subsystem block diagram

2.3.9.3 SAI Digital Audio Interface

RK3576 provides a total of 10 sets of SAI interfaces, of which 5 sets are exposed externally.

SAI stands for Serial Audio Interface, which is a serial interface used for digital audio data communication. It supports a wide range of audio protocols, including PCM, I2S, and TDM formats, and can be used for mono, stereo,

and multichannel audio transmission. As the most widely used digital audio interface, SAI can be used for communication between audio ADCs, audio DACs, audio codecs, DSPs, and other peripherals. It can also provide integrated audio input and output support for video input/output interfaces.

The SAI interfaces of RK3576 have the following characteristics:

- Supports bit widths from 8 to 32 bits, including common configurations such as 32 bits, 24 bits, and 16 bits.
- Supports up to 128 channels (slots).
- Supports mono mode.
- In Master mode, the maximum designed rate for TX/RX and in Slave mode for RX is 50M SCLK.
- In Slave mode, the maximum designed rate for TX is 25M SCLK.

As an example of the external SAI interfaces, SAI0 and SAI1 support 4 TX Lanes + 4 RX Lanes, while SAI2, SAI3, and SAI4 support 1 TX Lane + 1 RX Lane. Here, TX represents the output data line (SDO_x), and RX represents the input data line (SDI_x). The maximum sampling rate for each TX or RX data line can be calculated as follows: IO rate / (slots * width), where slots represent the number of channels and width represents the bit width. Typical sampling rate calculations are provided below for reference, and other sampling rates can be configured accordingly.

Table 2-43 RK3576 SAI Interface Sample Rate Reference at Different Channels and Bit Widths

Mode	Slots	Width	LRCK Sample Rate(kHz)	SCLK Rate (MHz)
I2S	2	32	16	1.024
I2S	2	32	44.1	2.8224
I2S	2	32	48	3.072
TDM8	8	32	16	4.096
TDM8	8	32	44.1	11.2896
TDM8	8	32	48	12.288
TDM16	16	32	16	8.192
TDM16	16	32	44.1	22.5792
TDM16	16	32	48	24.576
TDM32	32	32	48	49.152

The above is the theoretical calculation value, the actual rate is also affected by the IO signal quality, alignment delay and other factors. Please pay attention to the design of the relevant clock, signal distribution, optimise the alignment.

The following table describes the reuse of external SAI interfaces:

Table 2-44 RK3576 Multiplexing to External SAI Interface Description

External Interface	Multiplexing No.	IO Domain	Combined method
SAI0(4TX+4RX)	M0	VCCIO4	SDI0/1/2/3 + SDO0/1/2/3
SAI0(4TX+4RX)	M1	PMUIO1	SDI0 + SDO0 + SDIO123/321*
SAI0(4TX+4RX)	M2	VCCIO0	SDI0 + SDO0 + SDIO123/321*
SAI1(4TX+4RX)	M0	VCCIO2	SDI0 + SDO0 + SDIO123/321

External Interface	Multiplexing No.	IO Domain	Combined method
SAI1(4TX+4RX)	M1	VCCIO5	SDI0/1/2/3 + SDO0/1/2/3
SAI2(1TX+1RX)	M0	VCCIO3	SDI+SDO
SAI2(1TX+1RX)	M1	VCCIO4	SDI+SDO
SAI2(1TX+1RX)	M2	VCCIO5	SDI+SDO
SAI3(1TX+1RX)	M0	VCCIO0	SDI+SDO
SAI3(1TX+1RX)	M1	VCCIO3	SDI+SDO
SAI3(1TX+1RX)	M2	VCCIO4	SDI+SDO
SAI3(1TX+1RX)	M3	VCCIO1	SDI+SDO
SAI4(1TX+1RX)*	M0	VCCIO2	SDI+SDO
SAI4(1TX+1RX)	M1	VCCIO5	SDI+SDO
SAI4(1TX+1RX)	M2	VCCIO6	SDI+SDO
SAI4(1TX+1RX)	M3	VCCIO4	SDI+SDO

Note:

- SDIO123/321 indicates the same pin multiplexing SDI and SDO;
- SAI4 is internally connected to the DSM module, so external SAI4 is not available when the DSM module is in use;

2.3.9.3.1 SAI0 Digital Audio Interface

The SAI0 interface consists of independent 4TX Lanes and 4RX Lanes. For both output data lines (SDOx) and input data (SDIx), use the same set of bit/frame (SCLK/LRCK) reference clocks.

SAI0 interface supports both master and slave working modes, which can be configured by software. SAI0 provides a flexible compatibility configuration mode, allowing customization of LRCK and DATA frame formats to achieve compatibility with most I2S, PCM, and TDM formats. It also provides three I2S formats (standard, left-aligned, right-aligned) and direct configuration for early PCM format.

The SAI0 pins in this group are multiplexed in three different power domains. SAI0_M0 is multiplexed with VCCIO4, SAI0_M1 is multiplexed with PMUIO1, and SAI0_M2 is multiplexed with VCCIO0. These three multiplexing options cannot be used simultaneously; only one of them can be used at a time. SAI0_M0 can fully expose all signals in the group, while SAI0_M1 and SAI0_M2 have some data lines with multiplexing relationships. It is possible to internally remap the order of different data lines (SDOx or SDIx), for example, using SDO1 and SDO3 alternately to form a 2-lane configuration.

In the design, it is necessary to ensure that the IO levels of the SAI peripheral match the corresponding IO power domain.

Pull-up and pull-down recommendations for SAI0 interface and matching design are shown in the table below.

Table 2-45 RK3576 SAI0 interface signal description

Signal	Pull-up/ down by default	Connection method	Description
SAI0_MCLK_M0	pull-down	connect 22ohm resistor in series	SAI system clock output
SAI0_SCLK_M0	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI0_LRCK_M0	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection

Signal	Pull-up/ down by default	Connection method	Description
SAI0_SDO0_M0	pull-down	direct connection	SAI Serial Output Data Line 0
SAI0_SDO1_M0	pull-down	direct connection	SAI Serial Output Data Line 1
SAI0_SDO2_M0	pull-down	direct connection	SAI Serial Output Data Line 2
SAI0_SDO3_M0	pull-down	direct connection	SAI Serial Output Data Line 3
SAI0_SDI0_M0	pull-down	direct connection	SAI Serial Input Data Line 0
SAI0_SDI1_M0	pull-down	direct connection	SAI Serial Input Data Line 1
SAI0_SDI2_M0	pull-down	direct connection	SAI Serial Input Data Line 2
SAI0_SDI3_M0	pull-down	direct connection	SAI Serial Input Data Line 3
SAI0_MCLK_M1	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI0_SCLK_M1	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI0_LRCK_M1	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection
SAI0_SDO0_M1	pull-down	direct connection	SAI Serial Output Data Line 0
SAI0_SDO1_M1/ SAI0_SDI3_M1	pull-down	direct connection	SAI Serial Output Data Line 1/ SAI Serial input Data Line 3
SAI0_SDO2_M1/ SAI0_SDI2_M1	pull-down	direct connection	SAI Serial Output Data Line 2/ SAI Serial input Data Line 2
SAI0_SDO3_M1/ SAI0_SDI1_M1	pull-down	direct connection	SAI Serial Output Data Line 3/ SAI Serial input Data Line 1
SAI0_SDI0_M1	pull-down	direct connection	SAI Serial input Data Line 0
SAI0_MCLK_M2	pull-up	connect 22ohm resistor in series	SAI System Clock Output
SAI0_SCLK_M2	pull-up	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI0_LRCK_M2	pull-up	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection
SAI0_SDO0_M2	pull-up	direct connection	SAI Serial Output Data Line 0
SAI0_SDO1_M2/ SAI0_SDI3_M2	pull-up	direct connection	SAI Serial Output Data Line 1/ SAI Serial input Data Line 3
SAI0_SDO2_M2/ SAI0_SDI2_M2	pull-up	direct connection	SAI Serial Output Data Line 2/ SAI Serial input Data Line 2
SAI0_SDO3_M2/ SAI0_SDI1_M2	pull-down	direct connection	SAI Serial Output Data Line 3/ SAI Serial input Data Line 1
SAI0_SDI0_M2	pull-down	direct connection	SAI Serial input Data Line 0

Note:

- In order to improve the performance of SAI interface, the decoupling capacitor corresponding to the VCCIO power domain should not be deleted and should be placed close to the pins when layout;
- When the board-to-board connection is realised through the connector, it is recommended that the clock/control/signal are connected in series with resistors (between 22ohm-100ohm, subject to SI test), and TVS devices are reserved.

2.3.9.3.2 SAI1 Digital Audio Interface

The SAI1 interface consists of independent 4TX (transmit) Lanes and 4RX (receive) Lanes. For both output data lines (SDOx) and input data (SDIx), use the same set of bit/frame (SCLK/LRCK) reference clocks.

The SAI1 interface supports master and slave operation modes, which can be configured through software. SAI1 provides a flexible compatibility configuration mode that allows customization of LRCK and DATA frame formats, making it compatible with most I2S, PCM, and TDM formats. Additionally, it offers three I2S formats (standard, left-aligned, right-aligned) and direct configuration for early PCM format.

The SAI1 pins are multiplexed in two different power domains. SAI1_M0 is multiplexed with VCCIO2, while SAI1_M1 is multiplexed with VCCIO5. These two multiplexing options cannot be used simultaneously; only one of them can be used at a time. Some data lines of SAI1_M0 have multiplexing relationships, while SAI1_M1 can fully expose all signals as a complete group. The internal remapping of different data lines, such as SDOx or SDIx, can be configured to change their order. For example, SDO1 and SDO3 can be combined as 2 lanes with alternate extraction for usage.

In the design, it is necessary to ensure that the IO voltage levels of the SAI peripheral match the corresponding IO power domain.

The recommended pull-up/pull-down and matching design for the SAI1 interface is shown in the table.

Table 2-46 RK3576 SAI1 interface signal description

Signal	Pull-up/ down by default	Connection method	Description
SAI1_MCLK_M0	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI1_SCLK_M0	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI1_LRCK_M0	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection
SAI1_SDO0_M0	pull-down	direct connection	SAI Serial Output Data Line 0
SAI1_SDO1_M0/ SAI1_SDI3_M0	pull-down	direct connection	SAI Serial Output Data Line 1/ SAI Serial Input Data Line 3
SAI1_SDO2_M0/ SAI1_SDI2_M0	pull-down	direct connection	SAI Serial Output Data Line 2/ SAI Serial Input Data Line 2
SAI1_SDO3_M0/ SAI1_SDI1_M0	pull-down	direct connection	SAI Serial Output Data Line 3/ SAI Serial Input Data Line 1
SAI1_SDI0_M0	pull-down	direct connection	SAI Serial Input Data Line 0
SAI1_MCLK_M1	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI1_SCLK_M1	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI1_LRCK_M1	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection
SAI1_SDO0_M1	pull-down	direct connection	SAI Serial Output Data Line 0
SAI1_SDO1_M1	pull-down	direct connection	SAI Serial Output Data Line 1
SAI1_SDO2_M1	pull-down	direct connection	SAI Serial Output Data Line 2
SAI1_SDO3_M1	pull-down	direct connection	SAI Serial Output Data Line 3
SAI1_SDI0_M1	pull-down	direct connection	SAI Serial Input Data Line 0
SAI1_SDI1_M1	pull-down	direct connection	SAI Serial Input Data Line 1

Signal	Pull-up/ down by default	Connection method	Description
SAI1_SDI2_M1	pull-down	direct connection	SAI Serial Input Data Line 2
SAI1_SDI3_M1	pull-down	direct connection	SAI Serial Input Data Line 3

Note:

- In order to improve the performance of SAI interface, the decoupling capacitor corresponding to the VCCIO power domain should not be deleted and should be placed close to the pins when layout;
- When the board-to-board connection is realised through the connector, it is recommended that the clock/control/signal are connected in series with resistors (between 22ohm-100ohm, subject to SI test), and TVS devices are reserved.

2.3.9.3.3 SAI2 Digital Audio Interface

The SAI2 interface consists of independent 1TX (transmit) Lane and 1RX (receive) Lane. For both output data lines (SDOx) and input data (SDIx), use the same set of bit/frame (SCLK/LRCK) reference clocks.

The SAI2 interface supports master and slave operation modes, which can be configured through software. SAI2 provides a flexible compatibility configuration mode that allows customization of LRCK and DATA frame formats, making it compatible with most I2S, PCM, and TDM formats. Additionally, it offers three I2S formats (standard, left-aligned, right-aligned) and direct configuration for early PCM format.

The SAI2 pins are multiplexed in three different power domains. SAI2_M0 is multiplexed with VCCIO3, SAI2_M1 is multiplexed with VCCIO4, and SAI2_M2 is multiplexed with VCCIO5. These three multiplexing options cannot be used simultaneously; only one of them can be used at a time.

In the design, it is necessary to ensure that the IO voltage levels of the SAI peripheral match the corresponding IO power domain.

The recommended pull-up/pull-down and matching design for the SAI2 interface is shown in the table.

Table 2-47 RK3576 SAI2 interface signal description

Signal	Pull-up/ down by default	Connection method	Description
SAI2_MCLK_M0	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI2_SCLK_M0	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI2_LRCK_M0	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection
SAI2_SDO_M0	pull-down	direct connection	SAI Serial Output Data Line
SAI2_SDI_M0	pull-down	direct connection	SAI Serial Input Data Line
SAI2_MCLK_M1	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI2_SCLK_M1	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI2_LRCK_M1	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection
SAI2_SDO_M1	pull-down	direct connection	SAI Serial Output Data Line
SAI2_SDI_M1	pull-down	direct connection	SAI Serial Input Data Line
SAI2_MCLK_M2	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI2_SCLK_M2	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI2_LRCK_M2	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection

Signal	Pull-up/ down by default	Connection method	Description
SAI2_SDO_M2	pull-down	direct connection	SAI Serial Output Data Line
SAI2_SDI_M2	pull-down	direct connection	SAI Serial Input Data Line

Note:

- In order to improve the performance of SAI interface, the decoupling capacitor corresponding to the VCCIO power domain should not be deleted and should be placed close to the pins when layout;
- When the board-to-board connection is realised through the connector, it is recommended that the clock/control/signal are connected in series with resistors (between 22ohm-100ohm, subject to SI test), and TVS devices are reserved.

2.3.9.3.4 SAI3 Digital Audio Interface Translation

The SAI3 interface consists of independent 1TX Lanes and 1RX Lanes. For both output data lines (SDOx) and input data (SDIx), use the same set of bit/frame (SCLK/LRCK) reference clocks.

The SAI3 interface supports both master and slave modes, which can be configured through software. SAI3 provides a flexible compatibility configuration mode that allows customization of LRCK and DATA frame formats, making it compatible with the majority of I2S, PCM, and TDM formats. Additionally, it offers three I2S formats (conventional, left-aligned, right-aligned) and direct configuration for early PCM format.

The group of SAI pins is multiplexed across four different power domains. SAI3_M0 is multiplexed with VCCIO0, SAI3_M1 is multiplexed with VCCIO3, SAI3_M2 is multiplexed with VCCIO4, and SAI3_M3 is multiplexed with VCCIO1. Only one set can be used at a time, and simultaneous usage of multiple multiplexed pins is not allowed. Therefore, it is necessary to ensure that the IO voltage levels of the SAI peripheral match the corresponding IO power domain.

The recommended pull-up/down and matching designs for the SAI3 interface are shown in the table below.

Table 2-48 RK3576 SAI3 interface signal description

Signal	Pull-up/ down by default	Connection method	Description
SAI3_MCLK_M0	pull-up	connect 22ohm resistor in series	SAI System Clock Output
SAI3_SCLK_M0	pull-up	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI3_LRCK_M0	pull-up	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection
SAI3_SDO_M0	pull-down	direct connection	SAI Serial Output Data Line
SAI3_SDI_M0	pull-up	direct connection	SAI Serial Input Data Line
SAI3_MCLK_M1	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI3_SCLK_M1	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI3_LRCK_M1	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection
SAI3_SDO_M1	pull-down	direct connection	SAI Serial Output Data Line
SAI3_SDI_M1	pull-down	direct connection	SAI Serial Input Data Line
SAI3_MCLK_M2	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI3_SCLK_M2	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI3_LRCK_M2	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection

Signal	Pull-up/ down by default	Connection method	Description
SAI3_SDO_M2	pull-down	direct connection	SAI Serial Output Data Line
SAI3_SDI_M2	pull-down	direct connection	SAI Serial Input Data Line
SAI3_MCLK_M3	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI3_SCLK_M3	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI3_LRCK_M3	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection
SAI3_SDO_M3	pull-down	direct connection	SAI Serial Output Data Line
SAI3_SDI_M3	pull-down	direct connection	SAI Serial Input Data Line

Note:

- In order to improve the performance of SAI interface, the decoupling capacitor corresponding to the VCCIO power domain should not be deleted and should be placed close to the pins when layout;
- When the board-to-board connection is realised through the connector, it is recommended that the clock/control/signal are connected in series with resistors (between 22ohm-100ohm, subject to SI test), and TVS devices are reserved.

2.3.9.3.5 SAI4 Digital Audio Interface Translation

The SAI4 interface consists of independent 1TX Lanes and 1RX Lanes. Both the output data lines (SDOx) and input data (SDIx) reference the same set of bit/frame clocks (SCLK/LRCK).

The SAI4 interface supports both master and slave modes, which can be configured through software. SAI4 provides a flexible compatibility configuration mode that allows customization of LRCK and DATA frame formats, making it compatible with the majority of I2S, PCM, and TDM formats. Additionally, it offers three I2S formats (conventional, left-aligned, right-aligned) and direct configuration for early PCM format.

The group of SAI pins is multiplexed across three different power domains. SAI4_M0 is multiplexed with VCCIO2, SAI4_M1 is multiplexed with VCCIO5, SAI4_M2 is multiplexed with VCCIO6, and SAI4_M3 is multiplexed with VCCIO4. Only one set can be used at a time, and simultaneous usage of multiple multiplexed pins is not allowed. Therefore, it is necessary to ensure that the IO voltage levels of the SAI peripheral match the corresponding IO power domain.

In the design, it is important to verify the IO voltage levels of the SAI peripheral to ensure they match the corresponding IO power domain.

Table 2-49 RK3576 SAI4 interface signal description

Signal	Pull-up/ down by default	Connection method	Description
SAI4_MCLK_M0	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI4_SCLK_M0	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI4_LRCK_M0	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection
SAI4_SDO_M0	pull-down	direct connection	SAI Serial Output Data Line
SAI4_SDI_M0	pull-down	direct connection	SAI Serial Input Data Line
SAI4_MCLK_M1	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI4_SCLK_M1	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI4_LRCK_M1	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection

Signal	Pull-up/ down by default	Connection method	Description
SAI4_SDO_M1	pull-down	direct connection	SAI Serial Output Data Line
SAI4_SDI_M1	pull-down	direct connection	SAI Serial Input Data Line
SAI4_MCLK_M2	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI4_SCLK_M2	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI4_LRCK_M2	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection
SAI4_SDO_M2	pull-down	direct connection	SAI Serial Output Data Line
SAI4_SDI_M2	pull-down	direct connection	SAI Serial Input Data Line
SAI4_MCLK_M3	pull-down	connect 22ohm resistor in series	SAI System Clock Output
SAI4_SCLK_M3	pull-down	connect 22ohm resistor in series	SAI Continuous Serial Clock, Bit Clock
SAI4_LRCK_M3	pull-down	connect 22ohm resistor in series	SAI Frame Clock for Channel Selection
SAI4_SDO_M3	pull-down	direct connection	SAI Serial Output Data Line
SAI4_SDI_M3	pull-down	direct connection	SAI Serial Input Data Line

Note:

- In order to improve the performance of SAI interface, the decoupling capacitor corresponding to the VCCIO power domain should not be deleted and should be placed close to the pins when layout;
- When the board-to-board connection is realised through the connector, it is recommended that the clock/control/signal are connected in series with resistors (between 22ohm-100ohm, subject to SI test), and TVS devices are reserved.
- SAI4 is internally connected to the DSM module, so the external SAI4 is not available when the DSM module is in use.

2.3.9.4 PDM Digital Audio Interface

The RK3576 provides a total of 2 sets of 8-channel PDM interfaces, all of which are externally accessible.

The PDM (Pulse Density Modulation) interface is commonly used for connecting digital microphones or recording analog microphones through analog audio ADCs with PDM interfaces. The sampling rates typically used are 16kHz, 48kHz, or 8kHz, while some products with ultrasonic requirements may require a sampling rate of 96kHz.

Both sets of PDM interfaces operate in the master receive mode, where RK3576 provides the PDM clock and receives data. They support 8-channel input capability with a bit width of 16 to 32 bits and a maximum sampling rate of 192kHz.

The following diagram illustrates the data format of the PDM interface. PDM_DATA consists of Data(R) and Data(L), where PDM is a 1-bit sampling interface. The Data(R) and Data(L) are sampled at the rising and falling edges of the CLK, respectively. Each PDM_SDIx data line can transmit audio data for two channels. Therefore, the four SDIx data lines of one set of PDM interface can accommodate the needs of up to 8 microphones (or 6 microphones + 2 playback channels, totaling 8 channels).

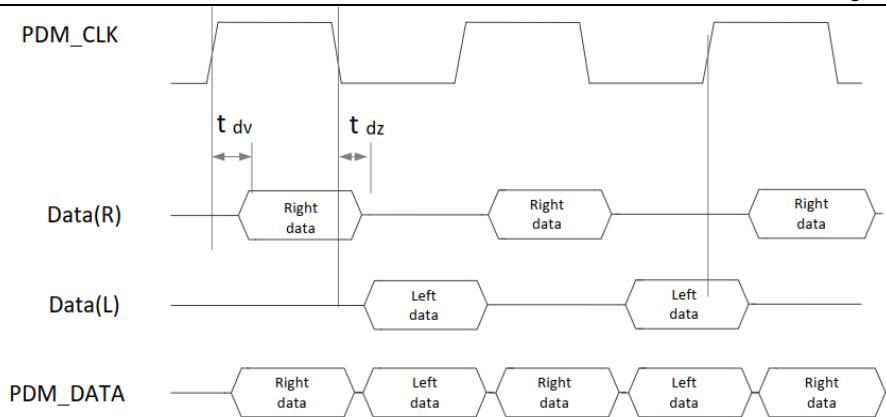


Figure 2-130 RK3576 PDM data format

The correspondence between common sample rates and PDM_CLK is shown in the following table, which can be used as a reference during hardware debug. The quality of the clock signal has a direct impact on the quality of the PDM recording, so when dividing the frequency of the PLL, it is necessary to use a fractional PLL + integer frequency division.

Table 2-50 RK3576 PDM_CLK Frequency and Sample Rate Comparison Table

PDM_CLK frequency	Sampling rate
3.072MHz	12kHz, 24kHz, 48kHz, 96kHz, 192kHz
2.8224MHz	11.025kHz, 22.05kHz, 44.1kHz, 88.2kHz, 176.4kHz
2.048MHz	8kHz, 16kHz, 32kHz, 64kHz, 128kHz

The following table describes the multiplexing of the PDM interface:

Table 2-51 Description of the multiplexing of the RK3576 PDM interface

Interface	No.	IO Domain	compose
PDM0	M0	PMUIO1	CLK0+CLK1+SDI0123
PDM0	M1	VCCIO0	CLK0+CLK1+SDI0123
PDM0	M2	VCCIO3	CLK0+CLK1+SDI0123
PDM0	M3	VCCIO4	CLK0+CLK1+SDI0123
PDM1	M0	VCCIO4	CLK0+CLK1+SDI0123
PDM1	M1	VCCIO2	CLK0+CLK1+SDI0123
PDM1	M2	VCCIO5	CLK0+CLK1+SDI0123

2.3.9.4.1 PDM0 Digital Audio Interface

The PDM0 pin is multiplexed in four different power domains. PDM0_M0 is multiplexed with PMUIO1, PDM0_M1 is multiplexed with VCCIO0, PDM0_M2 is multiplexed with VCCIO3, and PDM0_M3 is multiplexed with VCCIO4. These four multiplexing options cannot be used simultaneously; only one of them can be used at a time. It is necessary to verify the IO voltage levels of the PDM peripheral to match the corresponding IO power domain.

The recommended pull-up/pull-down and matching design for the PDM0 interface are shown in the table. To improve the impact of PCB routing on the clock, two synchronous and in-phase PDM clocks, PDM_CLK0 and PDM_CLK1, are provided. They can be freely paired with PDM_SDIx data lines. In specific product designs, reasonable and flexible allocation should be made based on the peripheral connection and PCB routing conditions

to avoid the impact of long branches and multiple loads on signal quality in cases where a single CLK signal is routed.

Table 2-52 RK3576 PDM0 interface signal descripyion

Signal	Pull-up/ down by default	Connection method	Description
PDM0_CLK0_M0	pull-down	connect 22ohm resistor in series	PDM clock 0
PDM0_CLK1_M0	pull-down	connect 22ohm resistor in series	PDM clock 1
PDM0_SDI0_M0	pull-down	direct connection	PDM input data line0
PDM0_SDI1_M0	pull-down	direct connection	PDM input data line 1
PDM0_SDI2_M0	pull-down	direct connection	PDM input data line 2
PDM0_SDI3_M0	pull-down	direct connection	PDM input data line 3
PDM0_CLK0_M1	pull-down	connect 22ohm resistor in series	PDM clock 0
PDM0_CLK1_M1	pull-up	connect 22ohm resistor in series	PDM clock 1
PDM0_SDI0_M1	pull-down	direct connection	PDM input data line0
PDM0_SDI1_M1	pull-up	direct connection	PDM input data line 1
PDM0_SDI2_M1	pull-up	direct connection	PDM input data line 2
PDM0_SDI3_M1	pull-up	direct connection	PDM input data line 3
PDM0_CLK0_M2	pull-down	connect 22ohm resistor in series	PDM clock 0
PDM0_CLK1_M2	pull-down	connect 22ohm resistor in series	PDM clock 1
PDM0_SDI0_M2	pull-down	direct connection	PDM input data line0
PDM0_SDI1_M2	pull-down	direct connection	PDM input data line 1
PDM0_SDI2_M2	pull-down	direct connection	PDM input data line 2
PDM0_SDI3_M2	pull-down	direct connection	PDM input data line 3
PDM0_CLK0_M3	pull-down	connect 22ohm resistor in series	PDM clock 0
PDM0_CLK1_M3	pull-down	connect 22ohm resistor in series	PDM clock 1
PDM0_SDI0_M3	pull-down	direct connection	PDM input data line0
PDM0_SDI1_M3	pull-down	direct connection	PDM input data line 1
PDM0_SDI2_M3	pull-down	direct connection	PDM input data line 2
PDM0_SDI3_M3	pull-down	direct connection	PDM input data line 3

Note:

- In order to improve the performance of PDM interface, the decoupling capacitor corresponding to the VCCIO power domain should not be deleted and should be placed close to the pins when layout;
- When the board-to-board connection is realised through the connector, it is recommended that the clock/control/signal are connected in series with resistors (between 22ohm-100ohm, subject to SI test), and TVS devices are reserved.

2.3.9.4.2 PDM1 Digital Audio Interface

The PDM1 pin is multiplexed in three different power domains. PDM1_M0 is multiplexed with VCCIO4, PDM1_M1 is multiplexed with VCCIO2, and PDM1_M2 is multiplexed with VCCIO5. These three multiplexing options cannot be used simultaneously; only one of them can be used at a time. It is necessary to verify the IO

voltage levels of the PDM peripheral to match the corresponding IO power domain.

The recommended pull-up/pull-down and matching design for the PDM1 interface are shown in the table. To improve the impact of PCB routing on the clock, two synchronous and in-phase PDM clocks, PDM_CLK0 and PDM_CLK1, are provided. They can be freely paired with PDM_SDIx data lines. In specific product designs, reasonable and flexible allocation should be made based on the peripheral connection and PCB routing conditions to avoid the impact of long branches and multiple loads on signal quality in cases where a single CLK signal is routed.

Table 2-53 RK3576 PDM1 interface signal descripyion

Signal	Pull-up/ down by default	Connection method	Description
PDM1_CLK0_M0	pull-down	connect 22ohm resistor in series	PDM clock 0
PDM1_CLK1_M0	pull-down	connect 22ohm resistor in series	PDM clock 1
PDM1_SDI0_M0	pull-down	direct connection	PDM input data line0
PDM1_SDI1_M0	pull-down	direct connection	PDM input data line 1
PDM1_SDI2_M0	pull-down	direct connection	PDM input data line 2
PDM1_SDI3_M0	pull-down	direct connection	PDM input data line 3
PDM1_CLK0_M1	pull-down	connect 22ohm resistor in series	PDM clock 0
PDM1_CLK1_M1	pull-down	connect 22ohm resistor in series	PDM clock 1
PDM1_SDI0_M1	pull-down	direct connection	PDM input data line0
PDM1_SDI1_M1	pull-down	direct connection	PDM input data line 1
PDM1_SDI2_M1	pull-down	direct connection	PDM input data line 2
PDM1_SDI3_M1	pull-down	direct connection	PDM input data line 3
PDM1_CLK0_M2	pull-down	connect 22ohm resistor in series	PDM clock 0
PDM1_CLK1_M2	pull-down	connect 22ohm resistor in series	PDM clock 1
PDM1_SDI0_M2	pull-down	direct connection	PDM input data line0
PDM1_SDI1_M2	pull-down	direct connection	PDM input data line 1
PDM1_SDI2_M2	pull-down	direct connection	PDM input data line 2
PDM1_SDI3_M2	pull-down	direct connection	PDM input data line 3

Note:

- In order to improve the performance of PDM interface, the decoupling capacitor corresponding to the VCCIO power domain should not be deleted and should be placed close to the pins when layout;
- When the board-to-board connection is realised through the connector, it is recommended that the clock/control/signal are connected in series with resistors (between 22ohm-100ohm, subject to SI test), and TVS devices are reserved.

2.3.9.5 SPDIF Digital Audio Interface

The RK3576 provides 2 external SPDIF_TX digital audio output interfaces and 2 external SPDIF_RX digital audio input interfaces, supporting a maximum resolution of 24 bits.

SPDIF(Sony/Philips Digital Interface Format) is a abbreviation for the SONY and PHILIPS digital audio interface. In terms of transmission medium, in the consumer market, SPDIF is commonly divided into two types:

coaxial and optical. While the signals they transmit are the same, they rely on different carriers, resulting in differences in interface and cable appearance. The communication speed of SPDIF is generally limited by the carrier, so the specifications of the interface devices used need to be considered during hardware design. However, optical signal transmission does not require consideration of interface voltage levels and impedance issues. It offers more flexibility and stronger anti-interference capabilities.

2.3.9.5.1 SPDIF_TX0 Digital Audio Interface

The SPDIF_TX0 pin is multiplexed in three different power domains, as shown in the table below.

The recommended pull-up/pull-down and matching design for the SPDIF interface are shown in the table. It is necessary to verify the IO voltage levels of the SPDIF_TX peripheral to match the corresponding IO power domain.

Table 2-54 RK3576 SPDIF_TX0 interface signal description

Signal and Multiplexing	Default Pull-up/Pull-down	Connection Method	Power Domain	Associated IO
SPDIF_TX0_M0	pull-down	connect 22ohm resistor in series	VCCIO2	GPIO4_B5
SPDIF_TX0_M1	pull-down	connect 22ohm resistor in series	VCCIO5	GPIO4_A1
SPDIF_TX0_M2	pull-down	connect 22ohm resistor in series	VCCIO4	GPIO2_D7

Note:

- To improve the performance of the SPDIF interface, the decoupling capacitors corresponding to the VCCIO power domain must not be removed. Please place them close to the pins during layout.
- When implementing board-to-board connections through connectors, it is recommended to use series resistors (between 22 ohms and 100 ohms, depending on SI testing requirements) and to reserve TVS components.

2.3.9.5.2 SPDIF_TX1 Digital Audio Interface

The SPDIF_TX1 pin is multiplexed in three different power domains, as shown in the table below.

The recommended pull-up/pull-down and matching design for the SPDIF interface are shown in the table. It is necessary to verify the IO voltage levels of the SPDIF_TX peripheral to match the corresponding IO power domain.

Table 2-55 RK3576 SPDIF_TX1 interface signal description

Signal and Multiplexing	Default Pull-up/Pull-down	Connection Method	Power Domain	Associated IO
SPDIF_TX1_M0	pull-down	connect 22ohm resistor in series	VCCIO5	GPIO3_B5
SPDIF_TX1_M1	pull-down	connect 22ohm resistor in series	VCCIO4	GPIO3_A3
SPDIF_TX1_M2	pull-down	connect 22ohm resistor in series	VCCIO3	GPIO1_D5

Note:

- To improve the performance of the SPDIF interface, the decoupling capacitors corresponding to the VCCIO power domain must not be removed. Please place them close to the pins during layout.
- When implementing board-to-board connections through connectors, it is recommended to use series resistors (between 22 ohms and 100 ohms, depending on SI testing requirements) and to reserve TVS components.

2.3.9.5.3 SPDIF_RX0 Digital Audio Interface

The SPDIF_RX0 pin is multiplexed in three different power domains, as shown in the table below.

The recommended pull-up/pull-down and matching design for the SPDIF interface are shown in the table. It is necessary to verify the IO voltage levels of the SPDIF_RX peripheral to match the corresponding IO power domain.

Table 2-56 RK3576 SPDIF_RX0 interface signal description

Signal and Multiplexing	Default Pull-up/Pull-down	Connection Method	Power Domain	Associated IO
SPDIF_RX0_M0	pull-down	connect 22ohm resistor in series	VCCIO2	GPIO4_B4
SPDIF_RX0_M1	pull-down	connect 22ohm resistor in series	VCCIO5	GPIO4_A0
SPDIF_RX0_M2	pull-down	connect 22ohm resistor in series	VCCIO4	GPIO2_D6

Note:

- To improve the performance of the SPDIF interface, the decoupling capacitors corresponding to the VCCIO power domain must not be removed. Please place them close to the pins during layout.
- When implementing board-to-board connections through connectors, it is recommended to use series resistors (between 22 ohms and 100 ohms, depending on SI testing requirements) and to reserve TVS components.

2.3.9.5.4 SPDIF_RX1 Digital Audio Interface

The SPDIF_RX1 pin is multiplexed in three different power domains, as shown in the table below.

The recommended pull-up/pull-down and matching design for the SPDIF interface are shown in the table. It is necessary to verify the IO voltage levels of the SPDIF_RX peripheral to match the corresponding IO power domain.

Table 2-57 RK3576 SPDIF_RX1 interface signal description

Signal and Multiplexing	Default Pull-up/Pull-down	Connection Method	Power Domain	Associated IO
SPDIF_RX1_M0	pull-down	connect 22ohm resistor in series	VCCIO5	GPIO3_B4
SPDIF_RX1_M1	pull-down	connect 22ohm resistor in series	VCCIO4	GPIO3_A2
SPDIF_RX1_M2	pull-down	connect 22ohm resistor in series	VCCIO3	GPIO1_D4

Note:

- To improve the performance of the SPDIF interface, the decoupling capacitors corresponding to the VCCIO power domain must not be removed. Please place them close to the pins during layout.
- When implementing board-to-board connections through connectors, it is recommended to use series resistors (between 22 ohms and 100 ohms, depending on SI testing requirements) and to reserve TVS components.

2.3.9.6 Asynchronous Sample Rate Converter Module:

The ASRC (Asynchronous Sample Rate Converter) module does not have a specific hardware IO interface, but it has a significant impact on audio solution design, compatibility, synchronization, and real-time functionality in actual products. Therefore, it is introduced in this section.

In an audio system, the ASRC is typically used to convert audio data from one sample rate to another or to

convert "asynchronous same sample rate" data based on different clocks. Therefore, the ASRC module can be seen as middleware for audio interfaces such as SAI, PDM, and SPDIF. By utilizing the ASRC, devices or interfaces with different sample rates and asynchronous clocks can maintain the coherence and stability of audio communication.

The RK3576 provides 4 sets of ASRC modules, covering both external and internal audio modules. They support a sample rate range from 8kHz to 384kHz, as shown in the typical table below. The conversion range ranges from 1:8 (down-conversion) to 8:1 (up-conversion).

Table 2-58 Typical Sample Rates of RK3576 ASRC Modules

ASRC Module Typical Input/Output Sample Rate
8KHz, 16KHz, 32KHz, 64KHz, 128KHz
12KHz, 24KHz, 48KHz, 96KHz, 192KHz, 384KHz
11.025KHz, 22.05KHz, 44.1KHz, 88.2KHz, 176.4KHz, 352.8KHz

The module names and their corresponding internal power domains are described as follows:

Table 2-59 RK3576 ASRC Asynchronous Sample Rate Converter Modules

Module Name	Internal Power Domain
ASRC_4CH_0	PD_AUDIO
ASRC_4CH_1	PD_AUDIO
ASRC_2CH_0	PD_AUDIO
ASRC_2CH_1	PD_AUDIO

2.3.9.7 DSM Audio Interface

The DSM (Direct Stream Modulation) PWM Audio interface refers to the direct digital encoding (Direct Stream Digital) of audio PCM data into a 1-bit signal stream. In designs that lack high-performance audio DACs but require voice audio output, this interface can be used to obtain audio signals through first-order RC low-pass filtering, as shown in the diagram below. The filtered digital signal is converted into an audio signal.

DSM PWM Audio is a low-cost audio output solution. For scenarios that require high audio quality, it is still recommended to use an external audio codec or DAC.

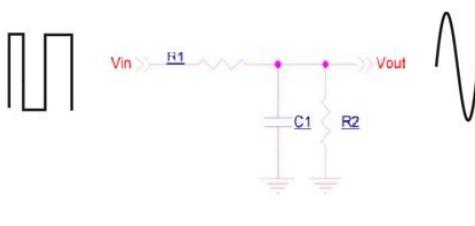


Figure 2-131 RK3576 DSM PWM Audio Low-Pass Filter Schematic

This interface provides two pairs of differential outputs, which can meet stereo audio requirements. For detailed information about the interface and RC low-pass filter parameter calculation, please refer to the "DSM AUDIO Audio Interface Circuit Design" document.

The DSM pins are multiplexed in two different power domains. DSM_AUD_M0 is multiplexed with VCCIO1, and DSM_AUD_M1 is multiplexed with VCCIO6. The two multiplexing locations cannot be used simultaneously;

only one set can be used at a time.

The quality of the clock signal directly affects the output quality of DSM. Therefore, when dividing the PLL frequency, a fractional PLL with integer division should be used.

It is important to note that SAI4 is internally connected to the DSM module. Therefore, when using the DSM module, the external SAI4 cannot be used.

Table 2-60 RK3576 DSM PWM Audio interface signal description

Signal and Multiplexing	Default Pull-up/Pull-down	Connection Method	Power Domain
DSM_AUD_LP_M0	pull-up	Serial RC low-pass filtering	VCCIO1
DSM_AUD_LN_M0	pull-up	Serial RC low-pass filtering	VCCIO1
DSM_AUD_RP_M0	pull-up	Serial RC low-pass filtering	VCCIO1
DSM_AUD_RN_M0	pull-down	Serial RC low-pass filtering	VCCIO1
DSM_AUD_LP_M1	pull-up	Serial RC low-pass filtering	VCCIO6
DSM_AUD_LN_M1	pull-up	Serial RC low-pass filtering	VCCIO6
DSM_AUD_RP_M1	pull-up	Serial RC low-pass filtering	VCCIO6
DSM_AUD_RN_M1	pull-down	Serial RC low-pass filtering	VCCIO6

Note:

- To improve the performance of the interface, the decoupling capacitors corresponding to the VCCIO power domain must not be removed. Please place them close to the pins during layout.
 - When implementing board-to-board connections through connectors, it is recommended to use series resistors (between 22 ohms and 100 ohms, depending on SI testing requirements) and to reserve TVS components.

2.3.9.8 Audio Peripheral Design Reference

In this section, design suggestions are provided for common audio scenarios that users can refer to.

2.3.9.8.1 Playback Devices, Headphones, Speakers

For speaker playback requirements, the following implementation options are available. RK3576 can be connected to a codec or audio DAC via I2S to achieve analog output, and then drive the speakers through an audio amplifier for power amplification. For stereo or mono output, the SAI interface can operate in I2S mode to meet the requirements. For multi-channel scenarios, the TDM mode of the SAI interface can be used.

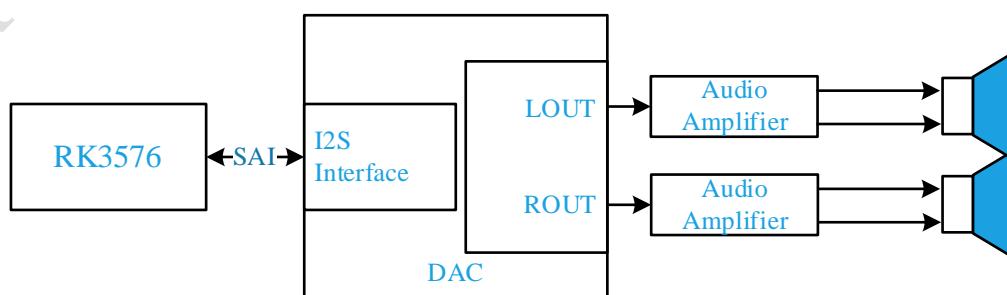


Figure 2-132 RK3576 Speaker Output Diagram

For scenarios with low audio quality requirements and strict cost constraints, the following diagram illustrates the path using DSM PWM Audio output. It is recommended to evaluate the audio quality before using this solution, such as for simple voice prompts.

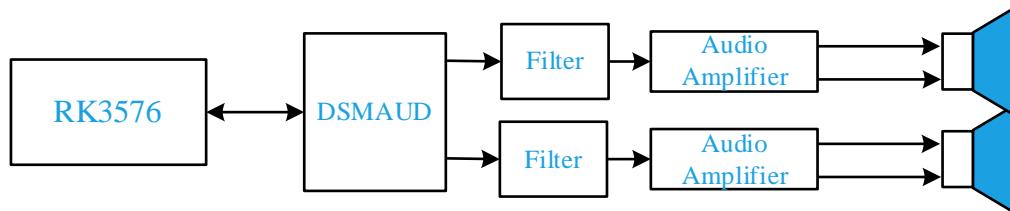


Figure 2-133 RK3576 Low-Cost Speaker Output Diagram

2.3.9.8.2 Recording Devices, Microphones

In applications such as tablets and laptops, there is a need for both playback and recording. In such cases, an integrated codec with ADC and DAC is typically used to achieve the required functionality, as shown in the diagram below.

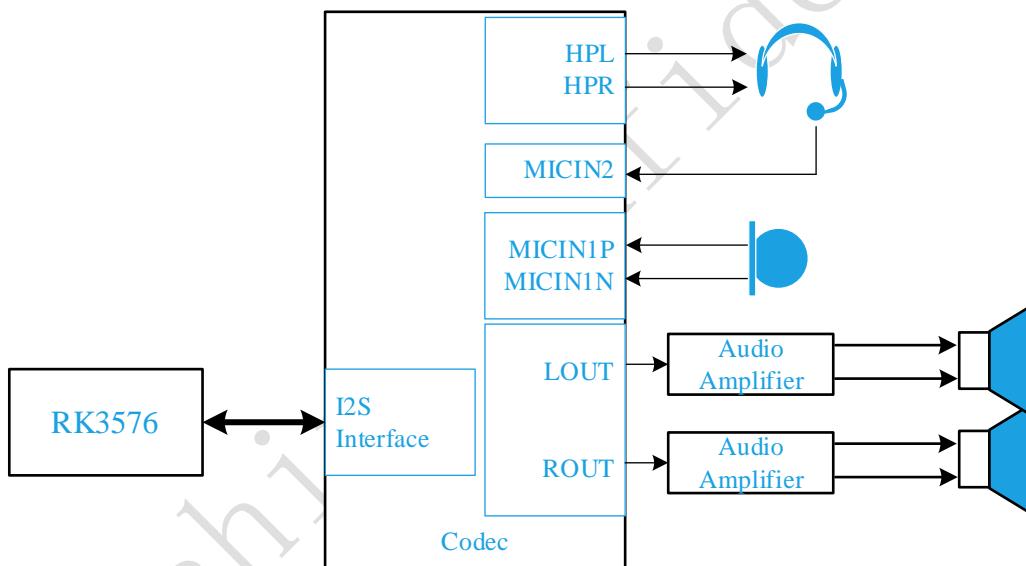


Figure 2-134 Typical Audio Solution Diagram for RK3576

In the AIoT reference design and EVB board, an ES8388 codec is used to implement the aforementioned functionality, as depicted in the following diagram. In actual schematic design, pay attention to the configuration of control signals, I2C signals, and audio signal levels for the connections to the codec to ensure compatibility.

If you directly use the circuit from the reference design, it is recommended to keep the analog interfaces consistent with the headphone, LINEOUT, and MIC interfaces as much as possible. This allows you to use the SDK software configurations. If any adjustments are made, you will need to modify the code accordingly to ensure the logic and physical mapping of audio channels for operations such as headphone switching and amplifier enablement.

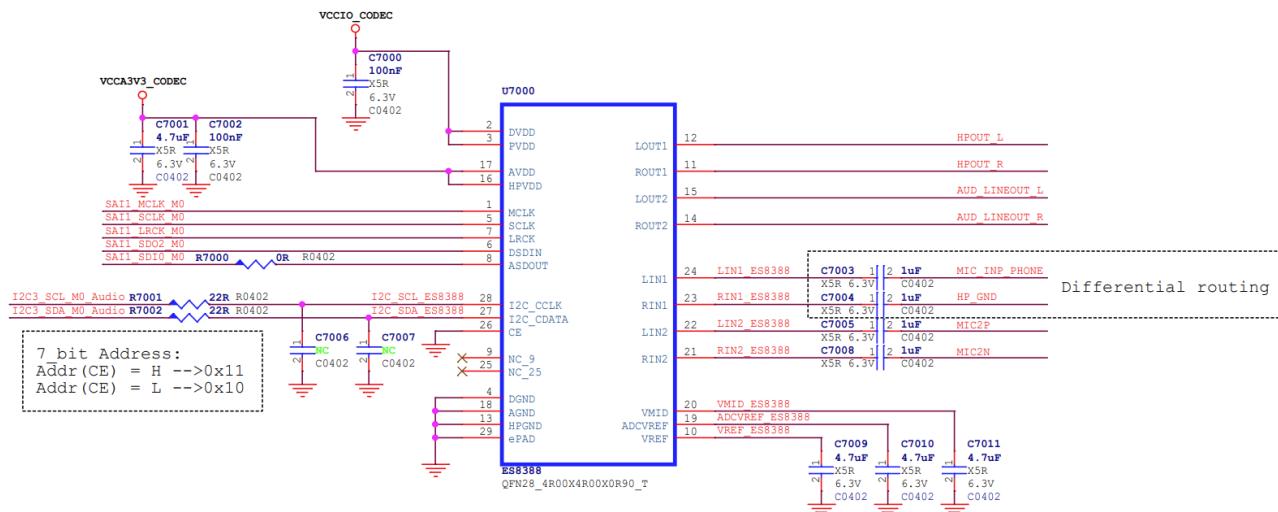


Figure 2-135 Typical Audio Solution Circuit Diagram for RK3576

It is important to note that the reference design uses a headphone interface with DET detection, and the internal pull-up of the HP_DET_L pin is enabled by default. This configuration should be adjusted based on the actual type of headphone jack being used.

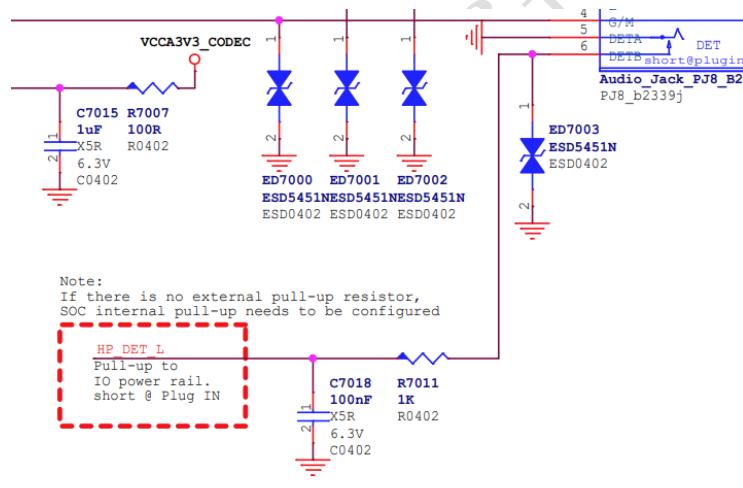


Figure 2-136 HP_DET_L Pin Pull-Up/Down Configuration for RK3576

For microphone inputs, it is recommended to use a pseudo-differential routing approach for both electret and single-ended output analog microphones. The 0-ohm series resistors near the microphone in the following diagram serve as a reminder to pay attention during layout.

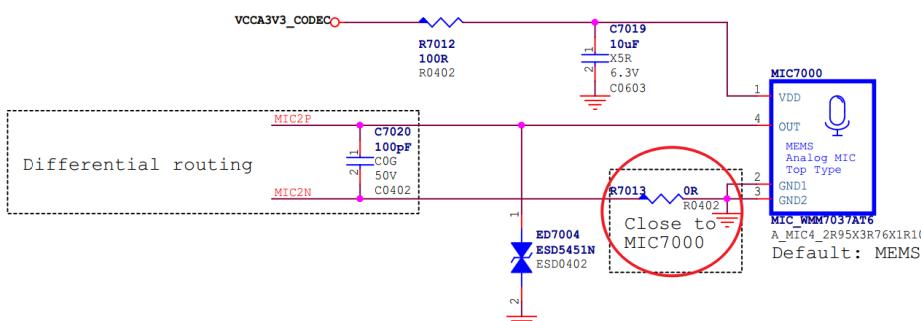


Figure 2-137 Pseudo-Differential Handling of Microphone Inputs

2.3.9.8.3 Introduction to Multi-Microphone Solutions

For scenarios that require multiple microphone inputs (microphone arrays, far-field recognition), there are three common expansion methods:

- Method 1: Multiple microphones and speaker capture can be achieved through the SAI (I2S/TDM) interface with a codec and audio ADC.
- Method 2: Multiple microphones and speaker capture can be achieved through a codec with a PDM interface.
- Method 3: Recording can be done using microphones with a PDM interface, while speaker capture can be achieved through a codec with a PDM interface and audio ADC.

If there is a lack of available channels, multiple SDIx data lines can be used to achieve multi-channel input, or cascaded input can be achieved through the TDM mode of the SAI interface. Simply stack identical circuits in hardware.

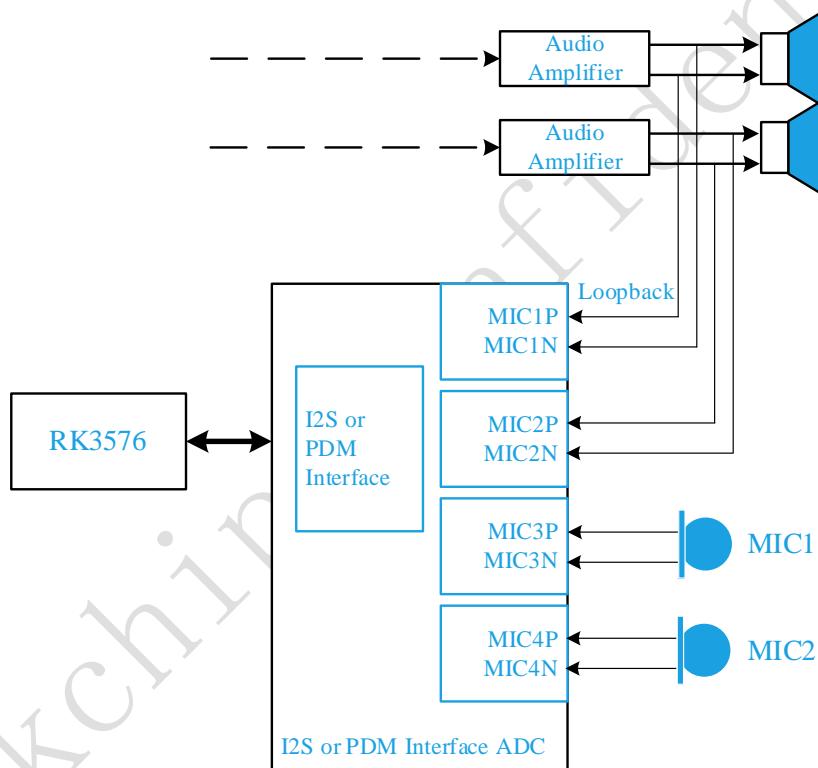


Figure 2-138 RK3576 Multi-Microphone Solution Diagram

In the AIoT reference design, a circuit reference using multiple ES7202 devices for connecting multiple analog silicon microphones and capture is provided, as shown in the diagram below. In actual schematic design, pay attention to the configuration of control signals, I2C signals, and PDM signals for the connections to the audio ADC to ensure compatibility.

In multi-microphone scenarios, the quantity and layout of the microphones need to be determined based on the specific algorithms. It is recommended to consult with algorithm providers to determine the relevant parameters and specifications. Here is a general recommendation for microphone selection:

- Sensitivity Desired value $\geq -38 \text{ dBV}$ @ 94 dB, 1 kHz. Analog MEMS microphones can generally meet this requirement, while electret condenser microphones (ECM) require careful selection. It is recommended that the sensitivity difference between soldered microphones be $\leq \pm 1 \text{ dB}$ if possible.

- (2) Signal-to-Noise Ratio (SNR): Desired value ≥ 64 dB. For cost considerations, some designs may relax this requirement to ≥ 60 dB.
 - (3) Acoustic Overload Point (AOP): Typical value ≥ 120 dB SPL. If the device itself produces high-power audio output, such as large speakers or TV soundbars that may receive high dB sound input, the AOP requirement needs to be increased.
 - (4) Frequency Response: Typical value $\leq \pm 2$ dB @ 100 Hz - 8 kHz (1/2 sample rate, generally 16 kHz sampling). If possible, it can be $\leq \pm 1.5$ dB.
 - (5) Total Harmonic Distortion (THD): Typical value ≥ 110 dB SPL @ 1%.

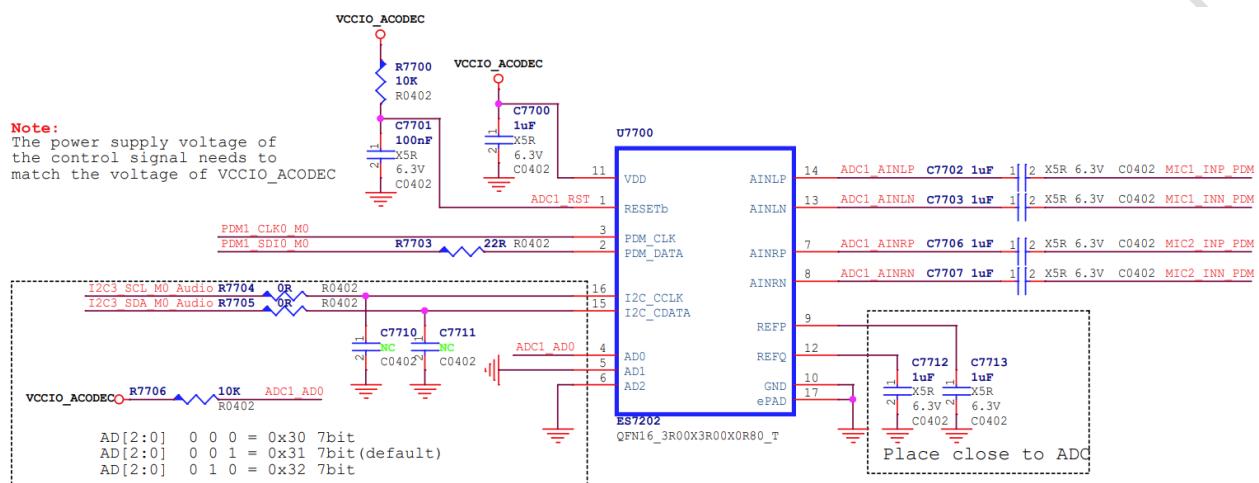


Figure 2-139 Circuit Reference for Multiple Analog Silicon Microphones and Capture

2.3.10 GMAC Interface Circuit

The RK3576 chip has two GMAC controllers that provide RMII or RGMII interfaces to connect to external Ethernet PHYs.

The GMAC controllers support the following functionalities:

- RGMII interface with data transfer rates of 10/100/1000 Mbps.
 - RMII interface with data transfer rates of 10/100 Mbps.

GMAC0 is multiplexed in two different power domains: GMAC0_M0 in the VCCIO5 power domain and GMAC0_M1 in the VCCIO4 power domain. These two multiplexing options cannot be used simultaneously; only one set can be used at a time.

FLEXBUS1_D11	DSMC_RDYN	SAI4_SDI_M1	ETH0_CLK0_25M_OUT_M0	VO_EBC_SDSHR	VO_LCDC_D23	GPIO3_A4_d	1D13
FLEXBUS0_D7	DSMC_DATA15	PDM1_SDI3_M2	ETH0_MDIO_M0	VO_EBC_GDSP	VO_LCDC_D22	GPIO3_A5_d	A9
FLEXBUS0_D8	DSMC_DATA14	PDM1_SDI2_M2	ETH0_MDC_M0	VO_EBC_GDOE	VO_LCDC_D21	GPIO3_A6_d	1A7
FLEXBUS0_D5	DSMC_DATA13	PDM1_CLK1_M2	ETH0_RXCTL_M0	VO_EBC_VCOM	VO_LCDC_D20	GPIO3_A7_d	B13
FLEXBUS0_D8	DSMC_CS1	SAI4_MCLK_M1	ETH0_MCLK_M0	VO_EBC_SDCE3	VO_LCDC_D19	GPIO3_B0_d	B14
FLEXBUS0_D4	DSMC_DATA12	PDM1_CLK0_M2	ETH0_RXDI_M0	VO_EBC_SDCE2	VO_LCDC_D18	GPIO3_B1_d	1A11
FLEXBUS0_D3	DSMC_DATA11	PDM1_SDI1_M2	ETH0_RXD0_M0	VO_EBC_SDCE1	VO_LCDC_D17	GPIO3_B2_d	A13
FLEXBUS0_D2	DSMC_DATA10	PDM1_SDIO_M2	ETH0_TXCTL_M0	VO_EBC_SDCE0	VO_LCDC_D16	GPIO3_B3_d	A11
FLEXBUS0_D1	DSMC_DATA9	SPDIF_RX1_M0	ETH0_RXD1_M0	VO_EBC_SDDO15	VO_LCDC_D15	GPIO3_B4_d	B10
FLEXBUS0_D0	DSMC_DATA8	SPDIF_RX1_M0	ETH0_RXD0_M0	VO_EBC_SDDO14	VO_LCDC_D14	GPIO3_B5_d	1A9
FLEXBUS0_CLK	DSMC_DQ01	--	ETH0_TXCLK_M0	VO_EBC_SDDO13	VO_LCDC_D13	GPIO3_B6_d	B11
FLEXBUS1_D10	DSMC_DQ00	SAI1_SDIO_M1	ETH0_PPSTRIG_M0	VO_EBC_SDDO12	VO_LCDC_D12	GPIO3_B7_d	1D12
FLEXBUS1_D9	DSMC_DATA7	SAI1_SDO3_M1	ETH0_PPSCLK_M0	VO_EBC_SDDO11	VO_LCDC_D11	GPIO3_C0_d	IE9
FLEXBUS1_D8	DSMC_DATA6	SAI1_SDO2_M1	ETH0_PTF_REFCLK_M0	VO_EBC_SDDO10	VO_LCDC_D10	GPIO3_C1_d	1B10
FLEXBUS0_D9	DSMC_IN11	SAI2_SCLK_M2	ETH0_TXD3_M0	VO_EBC_SDDO9	VO_LCDC_D9	GPIO3_C2_d	B9
FLEXBUS0_D10	DSMC_IN13	SAI2_LRCK_M2	ETH0_TXD2_M0	VO_EBC_SDDO8	VO_LCDC_D8	GPIO3_C3_d	1A8
FLEXBUS1_D7	DSMC_DATA5	SAI1_SDO1_M1	ETH0_TXD1_M0	VO_EBC_SDDO7	VO_LCDC_D7	GPIO3_C4_d	1D9
FLEXBUS1_D6	DSMC_DATA4	SAI1_SDIO_M1	--	VO_EBC_SDDO6	VO_LCDC_D6	GPIO3_C5_d	1B9
FLEXBUS1_D5	DSMC_DATA3	SAI1_LRCK_M1	--	VO_EBC_SDDO5	VO_LCDC_D5	GPIO3_C6_d	1D7
FLEXBUS1_D4	DSMC_DATA2	SAI1_SCLK_M1	--	VO_EBC_SDDO4	VO_LCDC_D4	GPIO3_C7_d	1C7
FLEXBUS1_D3	DSMC_DATA1	SAI1_MCLK_M1	--	VO_EBC_SDDO3	VO_LCDC_D3	GPIO3_D0_d	1C12
FLEXBUS0_D11	DSMC_CS2	SAI2_MCLK_M2	ETH0_RXCLK_M0	VO_EBC_SDDO2	VO_LCDC_D2	GPIO3_D1_d	1A12
FLEXBUS0_D12	DSMC_CS3	SAI2_SDI_M2	ETH0_RXD3_M0	VO_EBC_SDDO1	VO_LCDC_D1	GPIO3_D2_d	1A10
FLEXBUS1_D2	DSMC_CS0	SAI2_SDIO_M2	ETH0_RXD2_M0	VO_EBC_SDDO0	VO_LCDC_D0	GPIO3_D3_d	B12
FLEXBUS1_D1	DSMC_DATA0	SAI1_SDO1_M1	--	VO_EBC_SDCE1	VO_LCDC_DEN	GPIO3_D4_d	1E12
FLEXBUS1_D0	DSMC_CLKP	SAI1_SDO2_M1	--	VO_EBC_GDCLR	VO_LCDC_HSYNC	GPIO3_D5_d	1D10
FLEXBUS1_CLK	DSMC_CLKN	SAI1_SDO3_M1	--	VO_EBC_SDCLR	VO_LCDC_VSYNC	GPIO3_D6_d	1C10
FLEXBUS0_D15_M0	DSMC_RXSEIN	SAI4_SCLK_M1	CAM_CLK0_OUT_M0	VO_EBC_SDDE	VO_LCDC_CLK	GPIO3_D7_d	1E7
FLEXBUS0_D13_M0	DSMC_INTO	SAI4_LRCK_M1	CAM_CLK1_OUT_M0	SPIF_RX0_M1	--	GPIO4_A0_d	1B12
FLEXBUS0_D14_M0	DSMC_INT2	SAI4_SDO_M1	CAM_CLK2_OUT_M0	SPIF_TX0_M1	VO_POST_EMPTY	GPIO4_A1_d	1B7
						VCCIO5_VCC_0	2A4
						VCCIO5_VCC_1	2A5

Figure 2-140 RK3576 GMAC0_M0 Function Pin

--	SAI0_SD00_M0	ETH0_RXDO_M1	SDMMC1_D0_M1	VI_CIF_D15	GPIO2_A6_d	B22
--	SAI0_SD01_M0	ETH0_RXCTL_M1	SDMMC1_D1_M1	VI_CIF_D14	GPIO2_A7_d	B20
PDM0_SD13_M3	SAI0_SD10_M0	ETH0_RXD1_M1	SDMMC1_D2_M1	VI_CIF_D13	GPIO2_B0_d	B19
PDM0_SD12_M3	SAI0_SD11_M0	ETH0_RXD0_M1	SDMMC1_D3_M1	VI_CIF_D12	GPIO2_B1_d	1A18
PDM0_SD11_M3	SAI0_SD12_M0	ETH0_RXD3_M1	SDMMC1_CMD_M1	VI_CIF_D11	GPIO2_B2_d	1A17
PDM0_CLK1_M3	SAI0_SD02_M0	ETH0_RXCLK_M1	SDMMC1_CLK_M1	VI_CIF_D10	GPIO2_B3_d	B16
PDM0_SD10_M3	SAI0_SD13_M0	ETH0_RXD2_M1	SDMMC1_PWREN_M1	VI_CIF_D9	GPIO2_B4_d	A19
PDM0_CLK0_M3	SAI0_MCLK_M0	ETH0_RXCLK_M1	SDMMC1_DETN_M1	VI_CIF_D8	GPIO2_B5_d	1C18
--	SAI0_SCLK_M0	ETH0_RXD3_M1	ETH1_PTF_REFCLK_M1	VI_CIF_D7	GPIO2_B6_d	A21
--	SAI0_LRCK_M0	ETH0_RXD2_M1	--	VI_CIF_D6	GPIO2_B7_d	B21
PDM1_SD11_M0	--	ETH0_PTF_REFCLK_M1	ETH1_RXD2_M0	VI_CIF_D5	GPIO2_C0_d	A17
PDM1_CLK1_M0	SAI2_MCLK_M1	ETH0_PPCLK_M1	ETH1_RXD3_M0	VI_CIF_D4	GPIO2_C1_d	1A15
PDM1_SD12_M0	SAI2_SCLK_M1	ETH0_PPSTRIG_M1	ETH1_RXCLK_M0	VI_CIF_D3	GPIO2_C2_d	D15
PDM1_SD13_M0	SAI2_LRCK_M1	--	ETH1_RXD2_M0	VI_CIF_D2	GPIO2_C3_d	A15
PDM1_SD10_M0	SAI2_SDO_M1	--	ETH1_RXD3_M0	VI_CIF_D1	GPIO2_C4_d	1A13
PDM1_CLK0_M0	SAI2_SD1_M1	--	ETH1_RXCLK_M0	VI_CIF_D0	GPIO2_C5_d	1C15
--	SAI4_SCLK_M3	--	ETH1_RXD0_M0	--	GPIO2_C6_d	A14
--	SAI4_LRCK_M3	--	ETH1_RXDI_M0	--	GPIO2_C7_d	B15
--	SAI4_SDI_M3	--	ETH1_RXCTL_M0	--	GPIO2_D0_d	B16
--	SAI4_SDO_M3	--	ETH1_RXDO_M0	--	GPIO2_D1_d	1A16
--	SAI4_MCLK_M3	--	ETH1_RXDI_M0	CAM_CLK0_OUT_M1	GPIO2_D2_d	B17
--	--	--	ETH1_RXCTL_M0	--	GPIO2_D3_d	B18
--	--	--	ETH1_MDC_M0	ISP_PREFLIGHT_TRIGGER_M0	GPIO2_D4_d	1B13
--	--	--	ETH1_MDI0_M0	ISP_FLASH_TRIGGEROUT_M0	GPIO2_D5_d	B15
SPDIF_RX0_M2	SAI3_MCLK_M2	ETH0_MCLK_M1	ETH1_CLK1_25M_OUT_M0	CAM_CLK1_OUT_M1	GPIO2_D6_d	1D18
SPDIF_RX0_M2	SAI0_SD03_M0	ETH0_CLK0_25M_OUT_M1	ETH1_MCLK_M0	CAM_CLK2_OUT_M1	GPIO2_D7_d	E15
--	SAI3_SCLK_M2	ETH0_MDIO_M1	--	VI_CIF_HREF	GPIO3_A0_d	1D16
--	SAY3_LRCK_M2	ETH0_MDC_M1	ETH1_PPSTRIG_M0	VI_CIF_VSYNC	GPIO3_A1_d	1B18
SPDIF_RX1_M1	SAY3_SDO_M2	ETH0_RXCTL_M1	ETH1_PPCLK_M0	VI_CIF_CLK0	GPIO3_A2_d	1A20
SPDIF_RX1_M1	SAY3_SD1_M2	ETH0_RXDI_M1	ETH1_PTF_REFCLK_M0	VI_CIF_CLK1	GPIO3_A3_d	1A19
					VCCIO4_VCC	2A7

Figure 2-141 RK3576 GMAC0_M1 Function Pin

GMAC1 is multiplexed in two different power domains: GMAC1_M0 in the VCCIO4 power domain and GMAC1_M1 in the VCCIO3 power domain. These two multiplexing options cannot be used simultaneously; only one set can be used at a time.

--	SA10 SD00 M0	ETH0 RXD0 M1	SDMMC1 D0 M1	VI CIF D15	GPIO2 A6 d	B24
--	SA10 SD01 M0	ETH0 TXCTL M1	SDMMC1 D1 M1	VI CIF D14	GPIO2 A7 d	B20
PDM0 SDI2 M3	SA10 SDI0 M0	ETH0 TXD1 M1	SDMMC1 D2 M1	VI CIF D13	GPIO2 B0 d	B19
PDM0 SDI2 M3	SA10 SDI1 M0	ETH0 TXD0 M1	SDMMC1 D3 M1	VI CIF D12	GPIO2 B1 d	1A18
PDM0 SDI1 M3	SA10 SDI2 M0	ETH0 TXD3 M1	SDMMC1 CMD M1	VI CIF D11	GPIO2 B2 d	1A17
PDM0 CLK1 M3	SA10 SDI0 M0	ETH0 RXCLK M1	SDMMC1 CLK M1	VI CIF D10	GPIO2 B3 d	1B16
PDM0 SDIO M3	SA10 SDI3 M0	ETH0 TXD2 M1	SDMMC1 PWRN M1	VI CIF D9	GPIO2 B4 d	A19
PDM0 CLK0 M3	SA10 MCLK M0	ETH0 RXCLK M1	SDMMC1 DEIN M1	VI CIF D8	GPIO2 B5 d	1C18
--	SA10 SCLK M0	ETH0 RXD3 M1	ETH1 PTP REFCLK M1	VI CIF D7	GPIO2 B6 d	A21
--	SA10 LRCK M0	ETH0 RXD2 M1	--	VI CIF D6	GPIO2 B7 d	B21
PDM1 SDI1 M0	--	ETH0 PTP REFCLK M1	ETH1 RXD2 M0	VI CIF D5	GPIO2 C0 d	A17
PDM1 CLK1 M0	SA12 MCLK M1	ETH0 PPCLK M1	ETH1 RXD3 M0	VI CIF D4	GPIO2 C1 d	1A15
PDM1 SDI2 M0	SA12 SCLK M1	ETH0 PPSTRIG M1	ETH1 RXCLK M0	VI CIF D3	GPIO2 C2 d	1D15
PDM1 SDI3 M0	SA12 LRCK M1	--	ETH1 TXD1 M0	VI CIF D2	GPIO2 C3 d	A15
PDM1 SDIO M0	SA12 SD0 M1	--	ETH1 TXD3 M0	VI CIF D1	GPIO2 C4 d	1A13
PDM1 CLK0 M0	SA12 SD1 M1	--	ETH1 TXCLK M0	VI CIF D0	GPIO2 C5 d	1C15
--	SA14 SCLK M3	--	ETH1 TXD0 M0	--	GPIO2 C6 d	A14
--	SA14 LRCK M3	--	ETH1 TXD1 M0	--	GPIO2 C7 d	B15
--	SA14 SDI M3	--	ETH1 TXCTL M0	--	GPIO2 D0 d	B16
--	SA14 SDO M3	--	ETH1 RXD0 M0	--	GPIO2 D1 d	1A16
--	SA14 MCLK M3	--	ETH1 RXDI M0	CAM CLK0 OUT M1	GPIO2 D2 d	B17
--	--	--	ETH1 RXCTL M0	--	GPIO2 D3 d	B18
--	--	--	ETH1 MDC M0	ISP PRELIGHT TRIG M0	GPIO2 D4 d	1B13
--	--	--	ETH1 MDIO M0	ISP FLASH TRIGOUT M0	GPIO2 D5 d	1B15
SPDIF RX0 M2	SA13 MCLK M2	ETH0 MCLK M1	ETH CLK1 25M OUT M0	CAM CLK1 OUT M1	GPIO2 D6 d	1D18
SPDIF TX0 M2	SA10 SD03 M0	ETH CLK0 25M OUT M1	ETH1 MCLK M0	CAM CLK2 OUT M1	GPIO2 D7 d	1E15
--	SA13 SCLK M2	ETH0 MDIO M1	--	VI CIF HREF	GPIO3 A0 d	1D16
--	SAT3 LRCK M2	ETH0 MDC M1	ETH1 PPSTRIG M0	VI CIF VSYNC	GPIO3 A1 d	1B18
SPDIF RX1 M1	SAT3 SDO M2	ETH0 RXCTL M1	ETH1 PPCLK M0	VI CIF CLR0	GPIO3 A2 d	1A20
SPDIF TX1 M1	SAT3 SDI M2	ETH0 RXD1 M1	ETH1 PTP REFCLK M0	VI CIF CLR1	GPIO3 A3 d	1A19
VCCIO4_VCC						

Figure 2-142 RK3576 GMAC1_M0 Function Pin

--	SA13 SCLK M1	--	SDMMC1 D0 M0	ETH1 RXD2 M1	GPIO1 B4 d	A28
--	SA13 LRCK M1	--	SDMMC1 D1 M0	ETH1 RXD3 M1	GPIO1 B5 d	B27
--	SAT3 SDO M1	--	SDMMC1 D2 M0	ETH1 RXCLK M1	GPIO1 B6 d	1A23
--	SA13 SDI M1	--	SDMMC1 D3 M0	ETH1 TXD2 M1	GPIO1 B7 d	A27
--	PDM0 SDI2 M2	--	SDMMC1 CMD M0	ETH1 TXD3 M1	GPIO1 C0 d	B26
PDM0 CLK0 M2	SA13 MCLK M1	--	SDMMC1 CLK M0	ETH1 TXCLK M1	GPIO1 C1 d	1B22
--	FSP11 CSNI M1	FSP11 RSTN M1	SDMMC1 PWRN M0	ETH1 PPCLK M1	GPIO1 C2 d	B29
--	--	FSP11 CSNO M1	SDMMC1 DEIN M0	ETH1 PPSTRIG M1	GPIO1 C3 d	1C23
--	--	FSP11 D0 M1	--	ETH1 TXD0 M1	GPIO1 C4 d	1B23
--	--	FSP11 D1 M1	--	ETH1 TXD1 M1	GPIO1 C5 d	A26
PDM0 SDIO M2	--	FSP11 D2 M1	--	ETH1 TXCTL M1	GPIO1 C6 d	1C22
PDM0 SDI1 M2	--	FSP11 D3 M1	--	ETH1 RXD0 M1	GPIO1 C7 d	C29
--	SA12 SDO M0	--	--	ETH1 RXD1 M1	GPIO1 D0 d	1D22
--	SAT2 SCLK M0	--	--	ETH1 RXCTL M1	GPIO1 D1 d	1A24
--	SA12 LRCK M0	--	--	ETH1 MDC M1	GPIO1 D2 d	C28
SAT2 SDI M0	--	--	--	ETH1 MDIO M1	GPIO1 D3 d	1E21
SPDIF RX1 M2	PDM0 SDI3 M2	SA12 MCLK M0	--	ETH CLK1 25M OUT M1	GPIO1 D4 d	1E22
SPDIF TX1 M2	PDM0 CLK1 M2	FSP11 CLK M1	--	VCCIO3_VCC		2B10

Figure 2-143 RK3576 GMAC1_M1 Function Pin

Considerations for RGMII/RMII interface design:

- GMAC0 has two multiplexing options. GMAC0_M0 is in the VCCIO5 power domain and can support 1.8V or 3.3V voltage levels, determined by VCCIO5_VCC (Pin 2A4+2A5). GMAC0_M1 is in the VCCIO4 power domain and can support 1.8V or 3.3V voltage levels, determined by VCCIO4_VCC (Pin 2A7).
- GMAC1 has two multiplexing options. GMAC1_M0 is in the VCCIO4 power domain and can support 1.8V or 3.3V voltage levels, determined by VCCIO4_VCC (Pin 2A7). GMAC1_M1 is in the VCCIO3 power domain and can support 1.8V or 3.3V voltage levels, determined by VCCIO3_VCC (Pin 2B10).
- The GMACx_M0 and GMACx_M1 multiplexing options cannot be used simultaneously. For example, GMAC0_M0 and GMAC0_M1 cannot be used at the same time.

- It is recommended to use 1.8V voltage level for RGMII/RMII interfaces to achieve better signal quality.
- The decoupling capacitors for the VCCIOx_VCC power supplies of the RGMII/RMII interfaces should not be removed. Place them close to the pins during layout.
- ETH_CLK0_25M_OUT_Mx should have a 0-ohm resistor reserved on the RK3576 side to improve signal quality if necessary.
- ETH_CLK1_25M_OUT_Mx should have a 0-ohm resistor reserved on the RK3576 side to improve signal quality if necessary.
- TXD0~TXD3, TXCLK, and TXCTL should have 0-ohm resistors reserved on the RK3576 side to improve signal quality if necessary.
- RXD0~RXD3, RXCLK, and RXCTL should have 22-ohm resistors connected on the PHY side to improve signal quality.
- The recommended pull-up/pull-down and matching design for RGMII/RMII interfaces on the RK3576 chip as follow table:

Table 2-61 RK3576 RGMII/RMII Interface Design

Signal	IO Type (3576)	Connection	RGMII Interface	Signal Description	RMII Interface	Signal Description
ETHx_TXD[3: 0]_Mx	output	Reserved with 0-ohm resistor, close to RK3576	RGMIIx_TXD[3: 0]	Data Transmit	RMIIx_RXD[1: 0]	Data Transmit
ETHx_TXCLK_Mx	output	Reserved with 0-ohm resistor, close to RK3576	RGMIIx_RXCLK	Data Transmit Reference Clock	--	--
ETHx_TXCTL_Mx	output	Reserved with 0-ohm resistor, close to RK3576	RGMIIx_RXCTL	Data Transmit Enable (rising edge) and Data Transmit Error (falling edge)	RMIIx_RXEN	Data Transmit Enable Signal
ETHx_RXD[3: 0]_Mx	input	Connected with 22-ohm resistor, close to PHY	RGMIIx_RXD[3: 0]	Data Receive	RMIIx_RXD[1: 0]	Data Receive
ETHx_RXCLK_Mx	input	Connected with 22-ohm resistor, close to PHY	RGMIIx_RXCLK	Data Receive Reference Clock	--	--
ETHx_RXCTL_Mx	input	Connected with 22-ohm resistor, close to PHY	RGMIIx_RXCTL	Data Receive Valid (rising edge) and Receive Error (falling edge)	RMIIx_RXCTL	Data Receive Valid and Carrier Sense
ETHx_MCLK_Mx	input/output	Output Mode: Reserved with 0-ohm resistor, close to RK3576 input Mode: Connected with 22-ohm resistor, close to PHY	RGMIIx_MCLKIN 125M	PHY provides 125MHz clock to MAC, optional	RMII_MCLKIN 50M or RMII_MCLKOUT 50M	RMII Data Transmit and Data Receive Reference Clock
ETH_CLKx_25M_OUT_Mx	output	Reserved with 0-ohm resistor, close to RK3576	ETH_CLKx_25M_OUT_Mx	RK3576 provides 25MHz clock instead of PHY crystal	ETH_CLKx_25M_OUT_Mx	RK3576 provides 25MHz clock instead of PHY crystal
ETHx_MDC_Mx	output	Reserved with 0-ohm resistor, close to RK3576	RGMIIx_MDC	Management Data Clock	RMIIx_MDC	Management Data Clock
ETHx_MDIO_Mx	input/output	External pull-up with 1.5K-1.8Kohm resistor	RGMIIx_MDIO	Management Data Output/Input	RMIIx_MDIO	Management Data Output/Input

- When board-to-board connection is realised through the connector, it is recommended to connect a resistor in series (between 22ohm-100ohm, subject to the ability to satisfy the SI test) and to reserve a TVS device.
- RGMII connection diagram 1, please refer to the reference diagram for the specific circuit (GEPHY working clock uses an external 25MHz crystal):

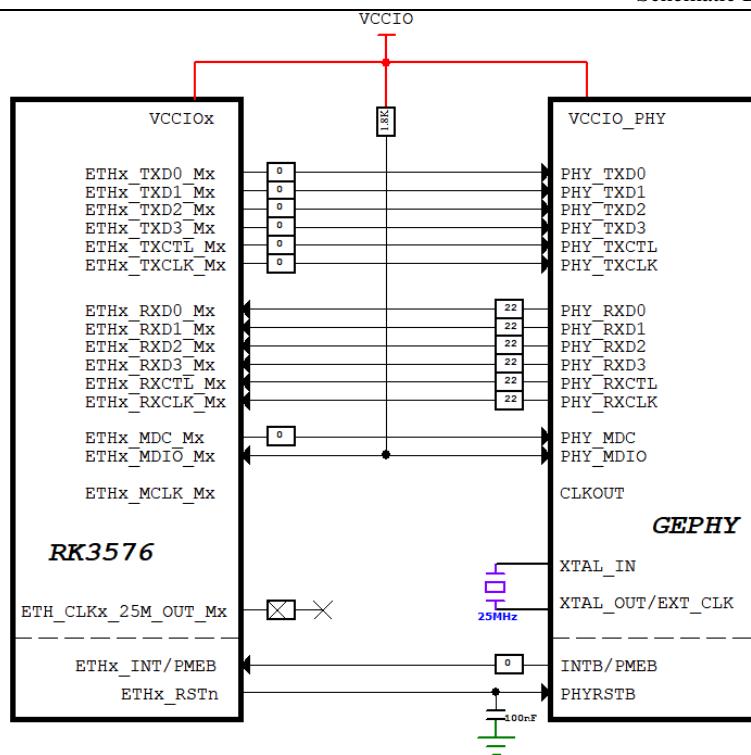


Figure 2-144 RGMII connection diagram 1

- RGMII Connection Diagram 2 (using RTL8211F/YT8531C as an example), please refer to the reference diagram for specific circuitry (GEPHY working clock uses 25MHz provided by RK3576).

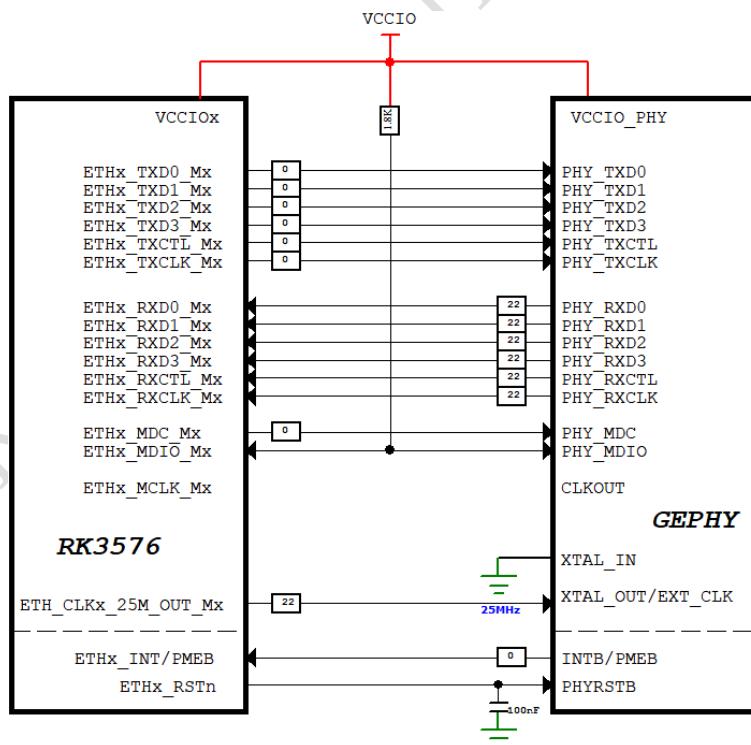


Figure 2-145 RGMII Connection Diagram 2

- RMII Connection Diagram 1 (using RTL8201F/YT8512C as an example), please refer to the reference diagram for specific circuitry (ETHx_MCLK_Mx uses the output mode, which means that FEPHY working clock also serves as the reference clock for the RMII interface. Note that some FEPHY may not support this mode).

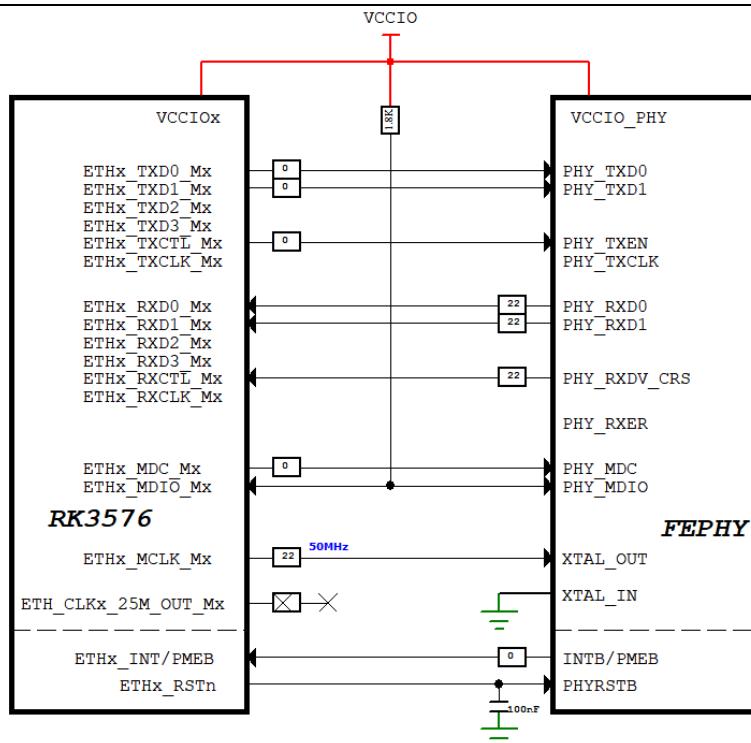


Figure 2-146 RMII Connection Diagram 1

- RMII Connection Diagram 2, please refer to the reference diagram for specific circuitry (FEPHY working clock uses a 25MHz crystal, ETHx_MCLK_Mx uses the output mode as the reference clock for the RMII interface, and FEPHY's TXCLK needs to be configured as the input mode).

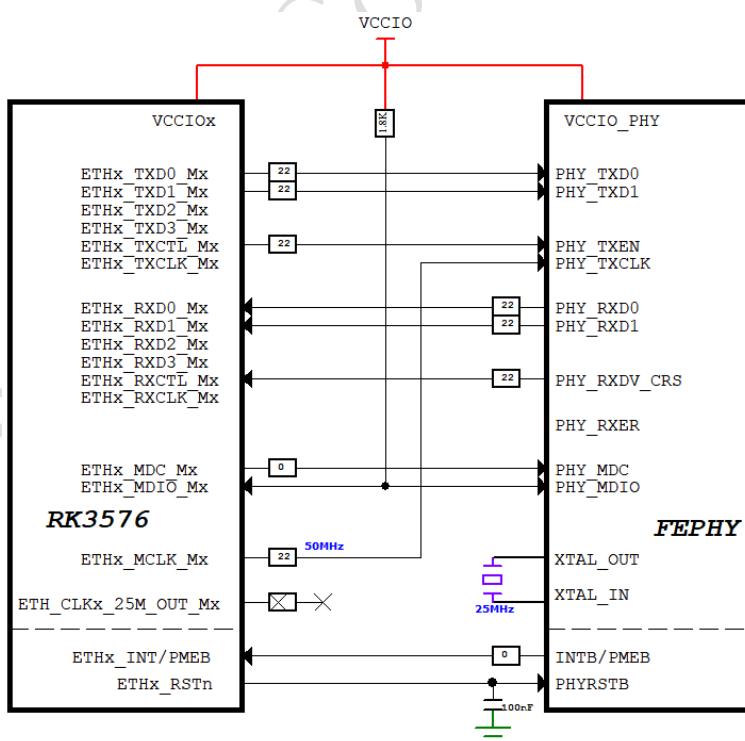


Figure 2-147 RMII Connection Diagram 2

- RMII Connection Diagram 3 (using RTL8201F/YT8512C as an example), please refer to the reference diagram for specific circuitry (using the 25MHz provided by RK3576 as a substitute for the FEPHY crystal, ETHx_MCLK_Mx uses the input mode as the reference clock for the RMII interface, and

FEPHY's TXCLK needs to be configured as the output mode).

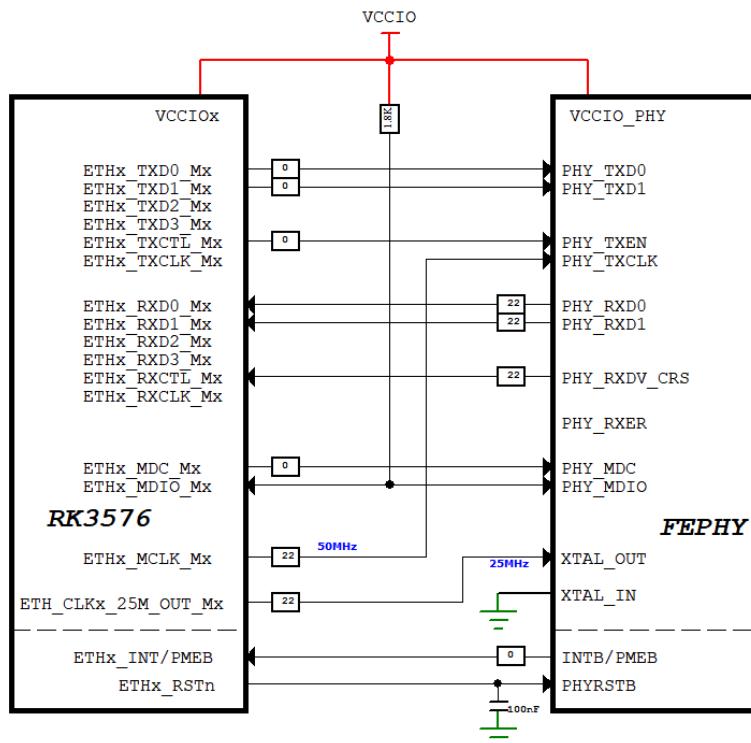


Figure 2-148 RMII Connection Diagram 3

- RMII Connection Diagram 4, please refer to the reference diagram for specific circuitry (FEPHY working clock uses an external 25MHz crystal, ETHx_MCLK_Mx uses the input mode, and the reference clock for the RMII interface is provided by FEPHY. FEPHY's TXCLK needs to be configured as the output mode).

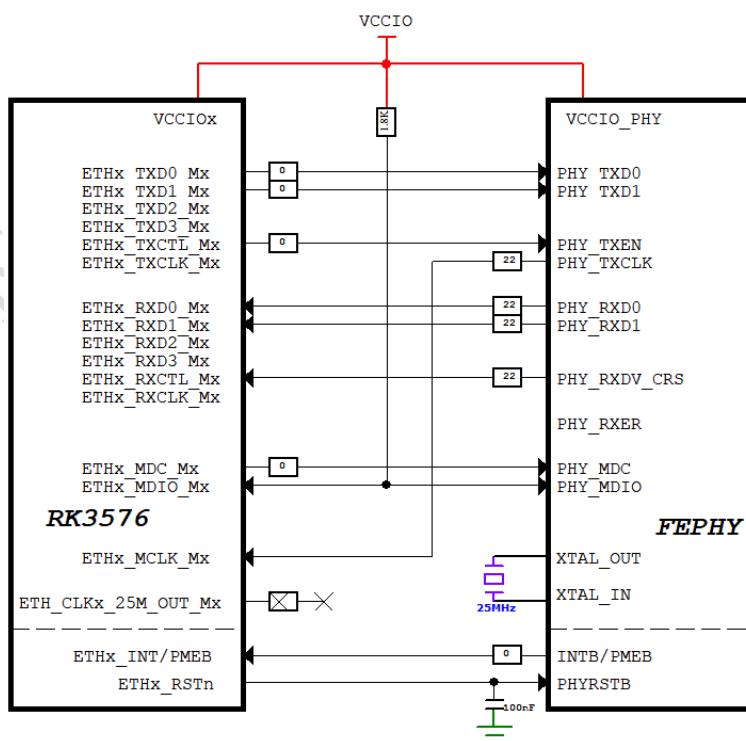


Figure 2-149 RMII Connection Diagram 4

- RMII Connection Diagram 5 (using RTL8201F/YT8512C as an example), please refer to the reference diagram for specific circuitry (using the 25MHz provided by RK3576 as a substitute for the FEPHY crystal, ETHx_MCLK_Mx uses the input mode as the reference clock for the RMII interface, and the reference clock for the RMII interface is provided by FEPHY. FEPHY's TXCLK needs to be configured as the output mode).

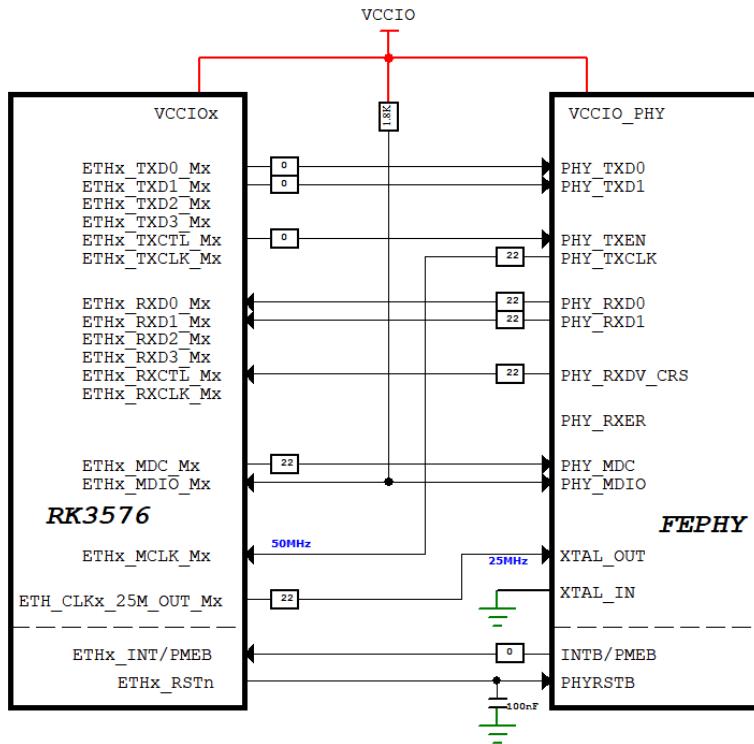


Figure 2-150 RMII Connection Diagram 5

- In RGMII mode, the internal TX/RX clock paths of the RK3576 chip integrate a delay line for adjustment. The default configuration in the reference diagram is that the timing between TXCLK and data is controlled by the MAC, and the timing between RXCLK and data is controlled by the PHY (for example, RTL8211F/FI has a default 2ns delay enabled for RXCLK, other PHYs should pay attention to this configuration).
- The Reset signal of the Ethernet PHY needs to be controlled by GPIO, and the GPIO level must match the PHY IO level. A 100nF capacitor should be added near the PHY pins to enhance electrostatic protection. Note: The reset pin of RTL8211F/FI only supports a 3.3V level.
- INTB/PMEB of RTL8211F/FI is an open-drain output and an external pull-up resistor must be added.
- When using an external crystal for the PHY, select the capacitance value of the crystal according to the actual load capacitance, keeping the frequency offset within +/-20ppm.
- The external resistor connected to the RSET pin of RTL8211F/FI is 2.49K ohm with a precision of 1% and should not be modified arbitrarily.
- The hardware configuration for PHY initialization must match the actual requirements.
- MDIO requires an external pull-up resistor, recommended value is 1.5-1.8Kohm, and the pull-up voltage must match the IO voltage.
- The connection of the center tap of the transformer must follow the reference diagram. If replacing with another Ethernet PHY, it is recommended to refer to the reference design provided by the respective

PHY manufacturer, as different PHY manufacturers may have different connection methods.

- For the 1000pF isolation capacitor, it is recommended to use a high-voltage safety capacitor with sufficient electrical clearance to ensure lightning protection.
- The 75-ohm resistor on the high-voltage side of the network transformer should be in a package size of 0805 or above.
- To achieve a lightning protection level of 4KV or above, additional surge protectors are required. Ordinary isolation transformers can only meet the 2KV level requirement.
- If there are requirements for differential testing against lightning strikes, TVS diodes need to be added to the MDI differential pairs.
- Make sure to confirm the consistency between the RJ45 package and the schematic. RJ45 connectors have Tab down and Tab up variants, and the signal order is reversed. If using RTL8211F/FI, it is recommended to use Tab down, and the MDI order is straight.

2.3.11 FlexBus Interface Circuit

The RK3576 chip features a flexible parallel bus interface called the FlexBus interface, which enables high-speed IO switching. It can emulate both standard and irregular protocols.

The characteristics of the FlexBus controller are as follows:

- It consists of two groups of 16-bit FlexBus, where the data lines of FlexBus0 can be used for both transmission (TX) and reception (RX), while the data lines of FlexBus1 can only be used for reception (RX).
- It supports 2/4/8/16-bit parallel data transfer. For data widths of 3/5/6/7 bits, the 3-bit data is sent in 4-bit mode within one clock cycle, where only TXDATA[2:0] contains valid data, and the remaining bits are set to 0. It requires data to be stored in DDR (Double Data Rate synchronous dynamic random-access memory) with a 4-bit alignment. For widths of 5/6 bits, etc., the data is sent in 8-bit mode. From the perspective of the FlexBus interface, only 2/4/8/16-bit modes are supported.
- The maximum speed can reach 100MHz.

Table 2-62 RK3576 FlexBus signal input/output direction

Pin name	direction	Pin name	direction
FLEXBUS0_D0	output/input	FLEXBUS1_D0	input
FLEXBUS0_D1	output/input	FLEXBUS1_D1	input
FLEXBUS0_D2	output/input	FLEXBUS1_D2	input
FLEXBUS0_D3	output/input	FLEXBUS1_D3	input
FLEXBUS0_D4	output/input	FLEXBUS1_D4	input
FLEXBUS0_D5	output/input	FLEXBUS1_D5	input
FLEXBUS0_D6	output/input	FLEXBUS1_D6	input
FLEXBUS0_D7	output/input	FLEXBUS1_D7	input
FLEXBUS0_D8	output/input	FLEXBUS1_D8	input
FLEXBUS0_D9	output/input	FLEXBUS1_D9	input
FLEXBUS0_D10	output/input	FLEXBUS1_D10	input
FLEXBUS0_D11	output/input	FLEXBUS1_D11	input

Pin name	direction	Pin name	direction
FLEXBUS0_D12	output/input	FLEXBUS1_D12	input
FLEXBUS0_D13	output/input	FLEXBUS1_D13	input
FLEXBUS0_D14	output/input	FLEXBUS1_D14	input
FLEXBUS0_D15	output/input	FLEXBUS1_D15	input
FLEXBUS0_CLK	output	FLEXBUS1_CLK	output/input
FLEXBUS0_CS	output	FLEXBUS1_CS	output

The FlexBus interface is multiplexed in the VCCIO2 and VCCIO5 power domains:

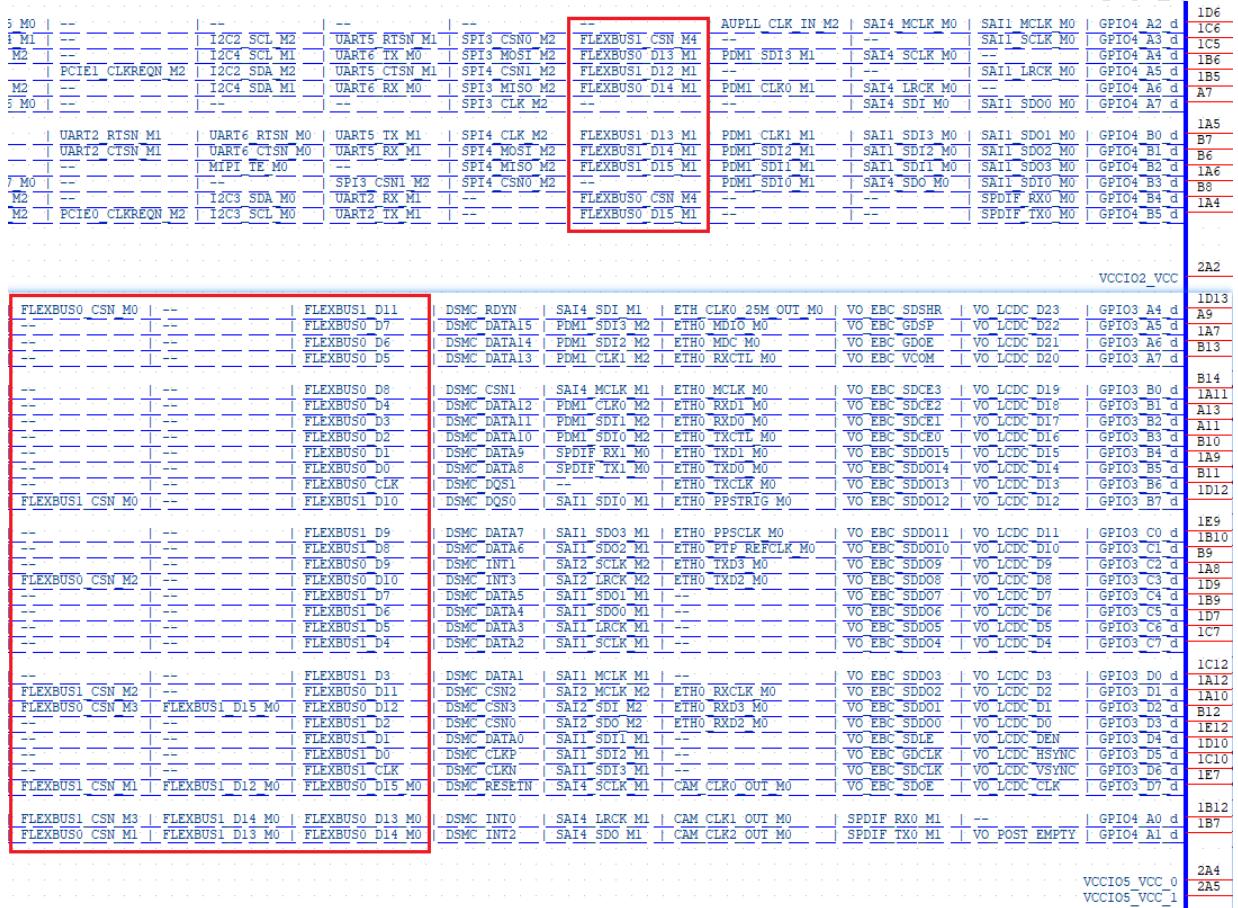


Figure 2-151 RK3576 FlexBus function pin

Considerations in FlexBus Interface Design:

- The FlexBus is multiplexed in the VCCIO2 and VCCIO5 power domains and can support 1.8V or 3.3V voltage levels. In actual product design, it is necessary to select the corresponding power supply (1.8V or 3.3V) based on the actual IO power requirements of the external devices, and it must be consistent. The main functional pins of FlexBus are multiplexed in the VCCIO5 power domain. When only using the FlexBus pins in the VCCIO5 power domain, the following configurations can be achieved: (1) Support up to 16 bits for FlexBus0 alone, while FlexBus1 can connect to a maximum of 10 bits of external devices (FlexBus1 also operates in 16-bit mode, but only 10 bits contain valid data, and the remaining bits are filled with zeros); (2) Support up to 16 bits for FlexBus1 alone, while FlexBus0 can connect to a maximum of 10 bits of external devices (FlexBus0 also operates in 16-bit mode, but only 10 bits contain valid data).

and the remaining bits are filled with zeros).

- The FlexBus pins in the VCCIO2 power domain are complementary to the FlexBus functionality in VCCIO5. By using a combination of FlexBus pins in VCCIO5 and VCCIO2, a mode of 16-bit FlexBus0 + 16-bit FlexBus1 can be achieved. In this case, it is important to ensure that VCCIO2 and VCCIO5 have consistent power supply domains. A typical application scenario is the combination of a high-speed 16-bit ADC and a 16-bit DAC.

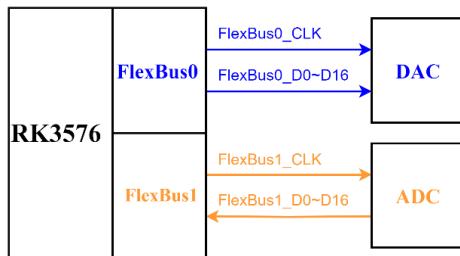


Figure 2-152 RK3576 FlexBus typical application

- To ensure the performance of FlexBus, it is recommended to prioritize the use of FlexBus data and clock signals in the VCCIO5 power domain. For example, if a mode of 14-bit FlexBus0 + 14-bit FlexBus1 is required, signals such as FlexBus0_D0~FlexBus0_D13, FlexBus0_CLK, FlexBus1_D0~FlexBus1_D13, and FlexBus1_CLK from VCCIO5 should be used, while the chip select signals FlexBus0_CSN_M4 and FlexBus1_CSN_M4 can be provided by the FlexBus pins in VCCIO2.
- FlexBus0_CLK and FlexBus1_CLK should have series 0-ohm resistors connected on the RK3576 end to improve signal quality if conditions permit.
- When implementing board-to-board connections through connectors, it is recommended to add series resistors (between 22 ohms and 100 ohms, depending on meeting SI testing requirements) and reserve TVS devices for protection.

2.3.12 DSMC interface circuit

Double Data Rate Serial Memory Controller (DSMC) is a double data rate serial interface mainly used for communication with PSRAM devices or peripheral communication with LocalBus devices (such as FPGA).

The characteristics of the DSMC controller are as follows:

- Supports double data rate interface.
- Supports 8-line and 16-line serial transmission modes.
- Supports up to 4 chip selects.
- The maximum speed of DSMC_CLKP/N is 100MHz.

The DSMC interface is multiplexed in the VCCIO5 power domain.

DSMC_RDYN	SAI4_SDI_M1	ETH0_CLK0_25M_OUT_M0	VO_EBC_SDSHR	VO_LCDC_D23	GPIO3_A4_d	1D13
DSMC_DATA15	PDM1_SDI3_M2	ETH0_MDI0_M0	VO_EBC_GDSP	VO_LCDC_D22	GPIO3_A5_d	A9
DSMC_DATA14	PDM1_SDI2_M2	ETH0_MDC_M0	VO_EBC_GDOE	VO_LCDC_D21	GPIO3_A6_d	1A7
DSMC_DATA13	PDM1_CLK1_M2	ETH0_RXCTL_M0	VO_EBC_VCOM	VO_LCDC_D20	GPIO3_A7_d	B13
DSMC_CSN1	SAI4_MCLK_M1	ETH0_MCLK_M0	VO_EBC_SDCE3	VO_LCDC_D19	GPIO3_B0_d	B14
DSMC_DATA12	PDM1_CLK0_M2	ETH0_RXDI_M0	VO_EBC_SDCE2	VO_LCDC_D18	GPIO3_B1_d	1A11
DSMC_DATA11	PDM1_SDI1_M2	ETH0_RXDO_M0	VO_EBC_SDCE1	VO_LCDC_D17	GPIO3_B2_d	A13
DSMC_DATA10	PDM1_SDIO_M2	ETH0_TXCTL_M0	VO_EBC_SDCE0	VO_LCDC_D16	GPIO3_B3_d	A11
DSMC_DATA9	SPDIF_RX1_M0	ETH0_RXDI_M0	VO_EBC_SDDO15	VO_LCDC_D15	GPIO3_B4_d	B10
DSMC_DATA8	SPDIF_TX1_M0	ETH0_RXDO_M0	VO_EBC_SDDO14	VO_LCDC_D14	GPIO3_B5_d	1A9
DSMC_DQS1	--	ETH0_TXCLK_M0	VO_EBC_SDDO13	VO_LCDC_D13	GPIO3_B6_d	B11
DSMC_DQS0	SAI1_SDIO_M1	ETH0_PPSTRIG_M0	VO_EBC_SDDO12	VO_LCDC_D12	GPIO3_B7_d	1D12
DSMC_DATA7	SAI1_SDO3_M1	ETH0_PPSCLR_M0	VO_EBC_SDDO11	VO_LCDC_D11	GPIO3_C0_d	1E9
DSMC_DATA6	SAI1_SDO2_M1	ETH0_PTP_REFCLK_M0	VO_EBC_SDDO10	VO_LCDC_D10	GPIO3_C1_d	1B10
DSMC_INT1	SAI2_SCLK_M2	ETH0_TXD3_M0	VO_EBC_SDDO9	VO_LCDC_D9	GPIO3_C2_d	B9
DSMC_INT3	SAI2_LRCK_M2	ETH0_TXD2_M0	VO_EBC_SDDO8	VO_LCDC_D8	GPIO3_C3_d	1A8
DSMC_DATA5	SAI1_SDO1_M1	--	VO_EBC_SDDO7	VO_LCDC_D7	GPIO3_C4_d	1D9
DSMC_DATA4	SAI1_SDO0_M1	--	VO_EBC_SDDO6	VO_LCDC_D6	GPIO3_C5_d	1B9
DSMC_DATA3	SAI1_LRCK_M1	--	VO_EBC_SDDO5	VO_LCDC_D5	GPIO3_C6_d	1D7
DSMC_DATA2	SAI1_SCLK_M1	--	VO_EBC_SDDO4	VO_LCDC_D4	GPIO3_C7_d	1C7
DSMC_DATA1	SAI1_MCLK_M1	--	VO_EBC_SDDO3	VO_LCDC_D3	GPIO3_D0_d	1C12
DSMC_CSN2	SAI2_MCLK_M2	ETH0_RXCLK_M0	VO_EBC_SDDO2	VO_LCDC_D2	GPIO3_D1_d	1A12
DSMC_CSN3	SAI2_SDI_M2	ETH0_RXD3_M0	VO_EBC_SDDO1	VO_LCDC_D1	GPIO3_D2_d	1A10
DSMC_CSN0	SAI2_SDO_M2	ETH0_RXD2_M0	VO_EBC_SDDO0	VO_LCDC_D0	GPIO3_D3_d	B12
DSMC_DATA0	SAI1_SD1_M1	--	VO_EBC_SDLE	VO_LCDC_DEN	GPIO3_D4_d	1E12
DSMC_CLKP	SAI1_SD2_M1	--	VO_EBC_GDCLK	VO_LCDC_HSYNC	GPIO3_D5_d	1D10
DSMC_CLKN	SAI1_SD3_M1	--	VO_EBC_SDCLK	VO_LCDC_VSYNC	GPIO3_D6_d	1C10
DSMC_RESETN	SAI1_SCLK_M1	CAM_CLK0_OUT_M0	VO_EBC_SDOE	VO_LCDC_CLK	GPIO3_D7_d	1E7
DSMC_INT0	SAI4_LRCK_M1	CAM_CLK1_OUT_M0	SPDIF_RX0_M1	--	GPIO4_A0_d	1B12
DSMC_INT2	SAI4_SDO_M1	CAM_CLK2_OUT_M0	SPDIF_TX0_M1	VO_POST_EMPTY	GPIO4_A1_d	1B7
					VCCIO5_VCC_0	2A4
					VCCIO5_VCC_1	2A5

Figure 2-153 RK3576 DSMC function pin

Considerations in DSMC interface design:

- The DSMC is multiplexed in the VCCIO5 power domain and can support 1.8V or 3.3V voltage levels. In actual product design, the power supply should be selected based on the actual IO power requirements of the external device (1.8V or 3.3V) and must be consistent.
- The clock of DSMC supports both single-ended and differential clock modes, depending on the requirements of the external device.
- DSMC's INT0 and INT1 support hardware interrupts with fast response, while INT2 and INT3 only support software interrupts.
- DSMC_CLKP and DSMC_CLKN should have series 0-ohm resistors connected on the RK3576 end to improve signal quality if conditions permit.
- When implementing board-to-board connections through connectors, it is recommended to add series resistors (between 22 ohms and 100 ohms, depending on meeting SI testing requirements) and reserve TVS devices for protection.

Table 2-63 RK3576 Operating Modes and Precautions

Pin name	16bit mode	8bit mode	note
DSMC_DQS1	DSMC_DQS1	/	
DSMC_DATA8~	DSMC_DATA8~	/	
DSMC_DATA15	DSMC_DATA15	/	
DSMC_DQS0	DSMC_DQS0	DSMC_DQS0	
DSMC_DATA0~	DSMC_DATA0~	DSMC_DATA0~	
DSMC_DATA7	DSMC_DATA7	DSMC_DATA7	
DSMC_CLKN	DSMC_CLKN	DSMC_CLKN	Used with differential clocking

Pin name	16bit mode	8bit mode	note
DSMC_CLKP	DSMC_CLKP	DSMC_CLKP	Supports single-ended clock mode
DSMC_CSN0	DSMC_CSN0	DSMC_CSN0	
DSMC_CSN1	DSMC_CSN1	DSMC_CSN1	
DSMC_CSN2	DSMC_CSN2	DSMC_CSN2	Supports up to 4 CS
DSMC_CSN3	DSMC_CSN3	DSMC_CSN3	
DSMC_INT0	DSMC_INT0	DSMC_INT0	Hardware interrupts
DSMC_INT1	DSMC_INT1	DSMC_INT1	fast response time
DSMC_INT2	DSMC_INT2	DSMC_INT2	Supports only software interrupts, which are slower to respond than hardware interrupts
DSMC_INT3	DSMC_INT3	DSMC_INT3	
DSMC_RDYN	DSMC_RDYN	DSMC_RDYN	
DSMC_RESETN	DSMC_RESETN	DSMC_RESETN	Based on peripheral requirements

2.3.13 UART Interface Circuit

The RK3576 chip features 12 UART controllers, which support the following functionalities:

- Support for full-duplex and half-duplex communication.
- Each UART controller includes two 64-byte FIFOs for data reception and transmission.
- Support for baud rates: 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, 4Mbps, and 8Mbps.
- Programmable baud rate and support for non-integer clock dividers.
- Support for interrupt-based or DMA-based modes.
- Support for 5-8 bit width transmission.
- Support for RS485 automatic send/receive function.

The RS485 automatic send/receive function refers to the capability of the SoC, when communicating with an external device via UART to RS485 conversion, to immediately control the RS485 chip to switch from transmit to receive mode after sending data. This avoids data loss caused by some external devices immediately returning data after receiving it, while the SoC fails to timely control the RS485 chip to switch from transmit to receive mode.

When communicating with RS485 using UART, there are two modes: 3-wire mode and 4-wire mode. In 3-wire mode, the UART's RSTN pin is connected to the RS485's RE and DE pins. In 4-wire mode, RSTN is connected to RS485's RE, and CTSN is connected to RS485's DE.

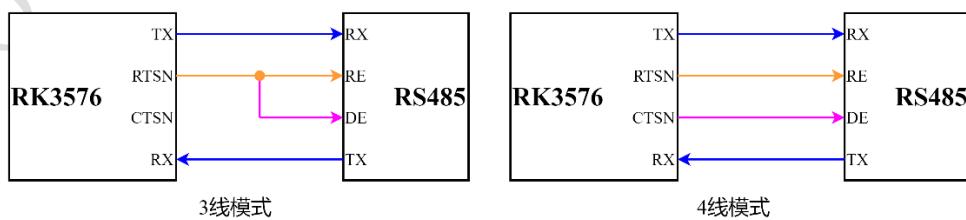


Figure 2-154 Schematic diagram of RS485 auto transceiver for RK3576 UART

To ensure flexibility in different product applications, the 12 UARTs are multiplexed in different power domains, indicated by the suffixes _M0/_M1/_M2/_M3 to differentiate the different multiplexing locations. The _M0/_M1/_M2/_M3 suffixes cannot be used simultaneously, and when allocating them, only one group can be

selected. It is not supported to have some signals using M0, some using M1, and others using M2.

The specific distribution of UART interfaces on the RK3576 as follow:

Table 2-64 RK3576 UART interface distribuiton

UART No.	Multiplexing situation	Multiplexing power domains
UART0	M0, M1	M0: PMUIO1 M1: VCCIO1
UART1	M0, M1, M2	M0: PMUIO1 M1: VCCIO4 M2: VCCIO5
UART2	M0, M1, M2	M0: VCCIO3 M1: VCCIO2 M2: VCCIO5
UART3	M0, M1, M2	M0: VCCIO4 M1: VCCIO5 M2: VCCIO3
UART4	M0, M1, M2	M0: VCCIO4 M1: VCCIO3 M2: PMUIO1
UART5	M0, M1, M2	M0: VCCIO5 M1: VCCIO2 M2: VCCIO1
UART6	M0, M1, M2, M3	M0: VCCIO2 M1: VCCIO4 M2: VCCIO0 M3: VCCIO6
UART7	M0, M1, M2	M0: VCCIO4 M1: VCCIO0 M2: VCCIO1
UART8	M0, M1, M2	M0: VCCIO5 M1: VCCIO4 M2: PMUIO1
UART9	M0, M1, M2	M0: VCCIO4 M1: VCCIO5 M2: VCCIO6
UART10	M0, M1, M2	M0: VCCIO5 M1: VCCIO3 M2: PMUIO1
UART11	M0, M1, M2	M0: VCCIO5 M1: VCCIO4 M2: VCCIO6

Table 2-65 RK3576 UART Flow Control Interface Distribution

UART No.	Multiplexing situation	Multiplexing power domains
UART0_RTSN UART0_CTSN	-	
UART1_RTSN UART1_CTSN	M0, M1, M2	M0: PMUIO1 M1: VCCIO4 M2: VCCIO5
UART2_RTSN UART2_CTSN	M0, M1, M2	M0: VCCIO3 M1: VCCIO2 M2: VCCIO5

UART No.	Multiplexing situation	Multiplexing power domains
UART3_RTSN UART3_CTSN	M0 , M1 , M2	M0: VCCIO4 M1: VCCIO5 M2 : VCCIO3
UART4_RTSN UART4_CTSN	M0 , M1	M0: VCCIO4 M1: VCCIO3
UART5_RTSN UART5_CTSN	M0 , M1 , M2	M0: VCCIO5 M1: VCCIO2 M2 : VCCIO1
UART6_RTSN UART6_CTSN	M0 , M1 , M2	M0: VCCIO2 M1: VCCIO4 M2: VCCIO0
UART7_RTSN UART7_CTSN	M0 , M1	M0: VCCIO4 M1: VCCIO0
UART8_RTSN UART8_CTSN	M0 , M1	M0: VCCIO5 M1: VCCIO4
UART9_RTSN UART9_CTSN	M0 , M1	M0: VCCIO4 M1: VCCIO5
UART10_RTSN UART10_CTSN	M0 , M1	M0: VCCIO5 M1: VCCIO3
UART11_RTSN UART11_CTSN	M0 , M1	M0: VCCIO5 M1: VCCIO4

Where UART0 M0 is by default the Debug UART for the RK3576.

According to the IO level of the UART peripheral, adjust the corresponding power domain supply, which must be consistent.

The UART interface pull-up and matching design recommendations are shown in the table:

Table 2-66 RK3576 UART interface design

Signal	Connection method	Description (chip end)
UARTx_RX	direct connect	UART data input
UARTx_TX	direct connect	UART data output
UARTx_CTSn	direct connect	UART Allowed to send signals
UARTx_RTn	direct connect	UART request to send signal

TVS devices are reserved when board-to-board connections are made via connectors.

2.3.14 I3C Interface Circuit

The RK3576 chip has 2 I3C controllers that support the following features:

- Support for I3C bus master mode with a maximum data rate of 12.5Mbit/s for pure I3C devices.
- Compatibility with I2C bus master mode with a maximum data rate of 400Kbit/s for pure I2C devices.
- Support for 7-bit and 10-bit addressing modes.**

When operating in I3C-compatible I2C mode, three pins are used: I3C_SCL, I3C_SDA, and I3C_SDA_PU.

The I3C_SDA pin is connected to I3C_SDA_PU through a pull-up resistor, and the I3C_SCL pin is connected to the pull-up power supply through a pull-up resistor. The pull-up power supply must be consistent with the GPIO power domain.

When only operating in I2C mode, only two pins are required: I3C_SCL and I3C_SDA. The hardware wiring method is the same as for I2C.

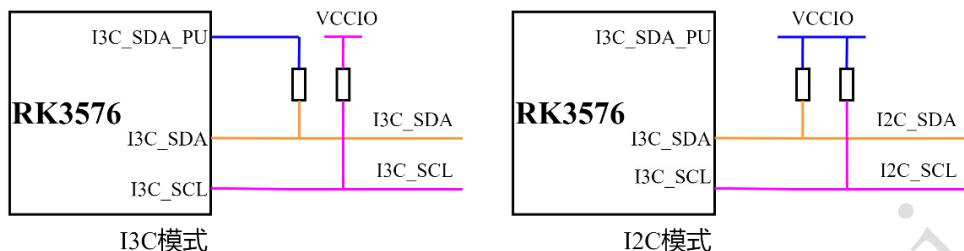


Figure 2-155 I3C Mode and I2C Mode Wiring Diagram of RK3576 I3C

Considerations for different product applications:

The 2 I3C controllers are multiplexed in different power domains and distinguished by the suffixes _M0/_M1/_M2. The _M0/_M1/_M2 suffixes cannot be used simultaneously, and when allocating them, only one group can be selected. For example, I3C1_M0 cannot be selected together with I3C1_M1 or any other M*.

The distribution of I3C interfaces on the RK3576 chip is provided in the following table:

Table 2-67 RK3576 I3C interface distribution

I3C No.	Multiplexing situation	Multiplexing power domains
I3C0	M0, M1	M0: PMUIO1 M1: VCCIO3
I3C1	M0, M1, M2	M0: VCCIO4 M1: VCCIO1 M2: VCCIO5

Adjust the power supply of the corresponding I3C peripheral based on the IO voltage level. It must be consistent.

The I3C signal SCL requires an external pull-up resistor. Select the appropriate resistor value (e.g., 2.2kohm) based on the bus load.

Ensure that the addresses of different devices on the I3C bus do not conflict, and the pull-up power supply must be consistent with the power supply.

Recommended I3C interface pull-up and matching design are as follows:

Table 2-68 RK3576 I3C interface design

Signal	Connection method	Description (chip end)
I3Cx_SCL	Direct Connection	I3C Clock
I3Cx_SDA	Direct Connection	I3C Data Output/Input
I3Cx_SDA_PU	Connected to I3Cx_SDA via a pull-up resistor	Pull-up power supply for I3Cx_SDA

When implementing board-to-board connections through connectors, it is recommended to reserve TVS devices.

2.3.15 I2C Interface Circuit

The RK3576 chip features 11 I2C controllers that support the following features:

- Support for I2C bus master mode.
- Support for software-programmable clock frequency and a maximum data rate of 400Kbit/s.
- Support for 7-bit and 10-bit addressing modes.

To ensure flexibility in different product applications, the 11 I2C controllers are multiplexed in different power domains, indicated by the suffixes _M0/_M1/_M2/_M3 to differentiate the different multiplexing locations. The _M0/_M1/_M2/_M3 suffixes cannot be used simultaneously, and when allocating them, only one group can be selected. For example, it is not supported to select I2C1_M0 and I2C1_M1 or any other M* together.

The distribution of I2C interfaces on the RK3576 chip is provided in the following table:

Table 2-69 RK3576 I2C interface distribution

I2C No.	Multiplexing situation	Multiplexing power domains
I2C0	M0, M1	M0: PMUIO0 M1: PMUIO1
I2C1	M0, M1	M0: PMUIO0 M1: PMUIO1
I2C2	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO0 M2: VCCIO2 M3: VCCIO6
I2C3	M0, M1, M2, M3	M0: VCCIO2 M1: PMUIO1 M2: VCCIO5 M3: VCCIO6
I2C4	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO2 M2: VCCIO4 M3: VCCIO5
I2C5	M0, M1, M2, M3	M0: VCCIO1 M1: VCCIO3 M2: VCCIO4 M3: VCCIO5
I2C6	M0, M1, M2, M3	M0: PMUIO0 M1: VCCIO3 M2: VCCIO4 M3: VCCIO6
I2C7	M0, M1, M2, M3	M0: VCCIO0 M1: VCCIO4 M2: VCCIO5 M3: VCCIO6

I2C No.	Multiplexing situation	Multiplexing power domains
I2C8	M0, M1, M2, M3	M0: VCCIO1 M1: VCCIO3 M2: VCCIO4 M3: VCCIO5
I2C9	M0, M1, M2, M3	M0: VCCIO0 M1: VCCIO3 M2: VCCIO4 M3: VCCIO5
HDMI_TX_I2C	-	VCCIO6

HDMI_TX_SCL/HDMI_TX_SDA is the I2C/DDC bus for the HDMI TX controller, and it is a dedicated bus.

I2C1 is allocated by default for the PMIC (Power Management IC) and it is recommended not to modify this allocation for software convenience.

Adjust the power supply of the corresponding I2C peripheral based on the IO voltage level, and it should be consistent.

The I2C signals SCL and SDA require external pull-up resistors. Select the appropriate resistor value (e.g., 2.2kohm) based on the bus load.

Ensure that the addresses of different devices on the I2C bus do not conflict, and the pull-up power supply must be consistent with the GPIO power domain.

Recommended I2C interface pull-up and matching design are as follows:

Table 2-70 RK3576 I2C Interface Design

Signal	Connection Method	Description (Chip end)
I2Cx_SCL	Direct Connection	I2C Clock
I2Cx_SDA	Direct Connection	I2C Data Output/Input

When implementing board-to-board connections through connectors, it is recommended to reserve TVS devices.

2.3.16 SPI Interface Circuit

In addition to the FSPI controller, the RK3576 chip has five general-purpose SPI controllers that support the following features:

- Support for both master and slave modes.
- Support for 4-bit, 8-bit, and 16-bit serial data transfer.
- Support for full-duplex and half-duplex mode.

To ensure flexibility in different product applications, the five SPI controllers are multiplexed in different power domains, indicated by the suffixes _M0/_M1/_M2/_M3 to differentiate the different multiplexing locations. The _M0/_M1/_M2/_M3 suffixes cannot be used simultaneously, and when allocating them, only one group can be selected. It is not supported to select M0 for some signals and M1 for others; this functionality is not available.

The distribution of SPI interfaces on the RK3576 chip is as follows:

Table 2-71 RK3576 SPI Interface Distribution

SPI No.	Multiplexing situation	Multiplexing power domains
SPI0	M0, M1, M2	M0: PMUIO1 M1: VCCIO1 M2: VCCIO0
SPI1	M0, M1, M2	M0: VCCIO3 M1: VCCIO4 M2: VCCIO5
SPI2	M0, M1, M2	M0: PMUIO0 M1: VCCIO3 M2: VCCIO5
SPI3	M0, M1, M2	M0: VCCIO4 M1: VCCIO5 M2: VCCIO2
SPI4	M0, M1, M2, M3	M0: VCCIO6 M1: VCCIO5 M2: VCCIO2 M3: VCCIO4

Adjust the power supply of the corresponding SPI peripheral based on the IO voltage level. It must be consistent.

The recommended SPI Interface Pull-Up and Matching Design as follow:

Table 2-72 RK3576 SPI Interface Design

Signal	Connection Method	Description (Chip end)
SPIx_CLK	Direct Connection	SPI Clock
SPIx_MOSI	Direct Connection	SPI Data Output (Master)
SPIx_MISO	Direct Connection	SPI Data Input (Master)
SPIx_CS0	Direct Connection	SPI Chip Select 0
SPIx_CS1	Direct Connection	SPI Chip Select 1

When implementing board-to-board connections through connectors, it is recommended to reserve TVS devices.

2.3.17 CAN Interface Circuit

The RK3576 chip has 2 CAN controllers that support the following features:

- Support CAN FD
- Support 1Mbps

To ensure flexibility in different product applications, the two CAN controllers are multiplexed in different power domains, differentiated by the suffixes _M0/_M1/_M2/_M3. The _M0/_M1/_M2/_M3 suffixes cannot be used simultaneously, and when allocating them, only one group can be selected. For example, if CAN_M0 is selected, CAN_M1 cannot be selected.

The distribution of CAN interfaces on the RK3576 chip is as follows:

Table 2-73 RK3576 CAN Interface Distribution

CAN No.	Multiplexing situation	Multiplexing power domains
CAN0	M0, M1, M2, M3	M0: VCCIO1 M1: VCCIO6 M2: VCCIO2

CAN No.	Multiplexing situation	Multiplexing power domains
		M3: VCCIO5
CAN1	M0, M1, M2, M3	M0: VCCIO1 M1: VCCIO6 M2: VCCIO2 M3: VCCIO4

Adjust the power supply of the corresponding CAN peripheral based on the IO voltage level. It must be consistent.

Recommended CAN interface pull-up and matching design:

Table 2-74 RK3576 CAN Interface Design

Signal	Connection Method	Description (Chip end)
CANx_RX	Direct Connection	CAN Data Input
CANx_TX	Direct Connection, external pull-up resistor required (recommended value: 4.7k ohm)	CAN Data Output

When implementing board-to-board connections through connectors, it is recommended to reserve TVS devices.

2.3.18 PWM Interface Circuit

The RK3576 chip integrates 3 independent PWM controllers, supporting a maximum of 16 PWM channels. PWM0 controller has 2 channels, PWM0_CH0~PWM0_CH1, PWM1 controller has 6 channels (PWM1_CH0~PWM1_CH5), and PWM2 controller has 8 channels (PWM2_CH0~PWM2_CH7).

The functionality of the 3 PWM controllers is summarized as follows:

Table 2-75 RK3576 PWM Functionality

Function	PWM0--2CH	PWM1--6CH	PWM2--8CH
Waveform Generator	NO	All 6 channels supported, sharing a lookup table (depth: 768). Example: 1 channel with 768 granularity; 3 channels with 256 granularity; 6 channels with 128 granularity.	NO
IR Input	Supports only 1, can be configured on any of the PWM0_CH0~PWM0_CH1 channels	NO	Supports only 1, can be configured on any of the PWM2_CH0~PWM2_CH7 channels
IR Output	NO	NO	Supports only 1, can be configured on any of the PWM2_CH0~PWM2_CH7 channels

Function	PWM0--2CH	PWM1--6CH	PWM2--8CH
Dual-Phase Counter	NO	<p>Supports 3 dual-phase counters (can be used as single-phase counters or frequency counters, supporting up to 20M frequency)</p> <p>CH0+CH3 form one dual-phase counter</p> <p>CH1+CH4 form one dual-phase counter</p>	<p>Supports 4 dual-phase counters (can be used as single-phase counters or frequency counters, supporting up to 20M frequency)</p> <p>CH0+CH4 form one dual-phase counter</p> <p>CH1+CH5 form one dual-phase counter</p> <p>CH2+CH6 form one dual-phase counter</p> <p>CH3+CH7 form one dual-phase counter</p>
Global Control Mode (Supports synchronized update of multiple channels configuration)	YES	YES	YES
Output Offset Mode (PWM output waveform offset by specified time)	YES	YES	YES

In addition to the above, PWM supports the following features:

- Capture mode support.
- Continuous mode or one-shot mode support.
- Each channel has two clock inputs to choose from: one is a fixed frequency from the crystal input, and the other is from the PLL bus with configurable frequency.

To ensure flexibility in different product applications, the 16 PWM channels are multiplexed in different power domains, differentiated by the suffixes _M0/_M1/_M2/_M3.

The distribution of PWM interfaces on the RK3576 chip is as follows:

Table 2-76 RK3576 PWM interface distribution

PWM No.	Multiplexing situation	Multiplexing power domains
PWM0_CH0	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO3 M2: VCCIO4 M3: VCCIO5
PWM0_CH1	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO6 M2: VCCIO4 M3: VCCIO5

PWM No.	Multiplexing situation	Multiplexing power domains
PWM1_CH0	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO3 M2: VCCIO4 M3: VCCIO5
PWM1_CH1	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO3 M2: VCCIO4 M3: VCCIO5
PWM1_CH2	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO3 M2: VCCIO4 M3: VCCIO5
PWM1_CH3	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO3 M2: VCCIO4 M3: VCCIO5
PWM1_CH4	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO3 M2: VCCIO4 M3: VCCIO5
PWM1_CH5	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO6 M2: VCCIO4 M3: VCCIO5
PWM2_CH0	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO6 M2: VCCIO4 M3: VCCIO5
PWM2_CH1	M0, M1, M2, M3	M0: VCCIO0 M1: VCCIO6 M2: VCCIO4 M3: VCCIO5
PWM2_CH2	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO6 M2: VCCIO4 M3: VCCIO5
PWM2_CH3	M0, M1, M2, M3	M0: PMUIO1 M1: VCCIO6 M2: VCCIO4 M3: VCCIO5

PWM No.	Multiplexing situation	Multiplexing power domains
PWM2_CH4	M0, M1, M2, M3	M0: VCCIO1 M1: VCCIO2 M2: VCCIO4 M3: VCCIO5
PWM2_CH5	M0, M1, M2, M3	M0: VCCIO2 M1: VCCIO6 M2: VCCIO4 M3: VCCIO5
PWM2_CH6	M0, M1, M2, M3	M0: VCCIO2 M1: VCCIO6 M2: VCCIO4 M3: VCCIO5
PWM2_CH7	M0, M1, M2, M3	M0: VCCIO2 M1: VCCIO0 M2: VCCIO4 M3: VCCIO5

- Adjust the power supply of the corresponding power domain based on the IO voltage level of the PWM peripheral. It must be consistent.
- When implementing board-to-board connections through connectors, it is recommended to serially connect resistors with a specific resistance value (between 22 ohms and 100 ohms, depending on meeting SI testing requirements) and reserve TVS (Transient Voltage Suppression) devices.
- When receiving signals from an infrared (IR) receiver, the following considerations should be taken into account:
 - In standby mode, support for IR receiver wake-up is required while considering low power consumption (i.e., LOGIC_DVDD power-off solution). Only PWM0_CH0/PWM0_CH1 can be used as the input for the IR receiver.
 - The power supply for the IR receiver should use VCC_3V3_S3.
 - The power supply for the IR receiver should be filtered with an RC filter consisting of a resistor (22-100 ohms) and a capacitor (10uF or higher).
 - The IR receiver defaults to a carrier frequency of 38KHz. If a different frequency is used, software adjustments are necessary.
 - The output level of the IR receiver must match the IO voltage level of the RK3576.
 - It is recommended to connect a 22-ohm resistor and a 1nF capacitor in series with the output pin of the IR receiver before connecting it to the RK3576, to enhance the ability to withstand electrostatic discharge surges.

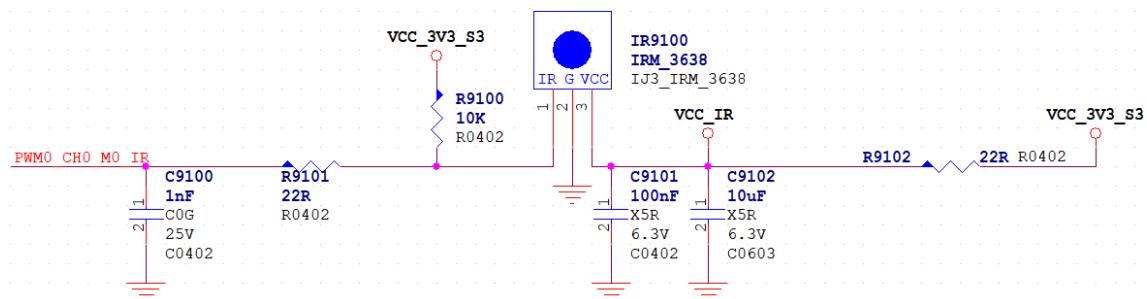


Figure 2-156 Infrared Receiver Circuit

- When laying out the IR receiver, it should be placed far away from wireless module antennas, such as Wi-Fi antennas, to avoid interference with infrared signal reception during wireless data transmission.
- The layout of the IR receiver should avoid direct exposure to onboard LED light sources to prevent the flickering frequency of LEDs from affecting infrared reception.
- It is recommended to implement a ground trace for the IR signal. If a ground trace cannot be implemented, it is suggested to maintain a separation distance of at least 2 times the line width between the IR signal and other signals.

2.3.19 RK3576 Methods for Processing Unused Module Pins

Please see the document "RK3576 Methods for Processing Unused Pins_V1.0".

When each analogue PHY is not in use, if the power supply is not powered, you need to pay attention to the software DTS configuration to Disable the corresponding analogue PHY function.

3 PCB Design Recommendations

3.1 PCB Stackup Design

To minimize reflections during high-speed signal transmission, impedance matching must be done between the signal source, receiver, and transmission lines. The specific impedance of a single-ended signal line depends on its trace width and the relative position to the reference plane. The trace width/spacing for differential pairs with specific impedance requirements depends on the chosen PCB stackup structure. Since the minimum trace width and spacing depend on the PCB type and cost requirements, the selected PCB stackup structure must meet all impedance requirements on the board, including inner and outer layers, single-ended and differential lines, etc.

Design principles for layer definition:

- Ideally, a symmetric structure design should be adopted. Symmetry includes the thickness and type of dielectric layers, copper foil thickness, and symmetry of the distribution of graphics (large copper layers, signal layers).
- The adjacent layers to the main chip should be complete ground planes, providing reference planes for device surface routing.
- The main power supply should be adjacent to its corresponding ground plane layer as much as possible.
- All signal layers should be adjacent to ground planes, and direct adjacency between two signal layers should be avoided as much as possible to provide a complete reference ground plane.
- If adjacent routing between two layers is required, the distance between them should be as far as possible, and the signals should be oriented perpendicular to each other to minimize inter-layer signal crosstalk.

Recommended PCB layer definition scheme: When determining the specific PCB layer configuration, the above principles should be flexibly applied based on actual requirements. Avoid rigidly following a predefined layout. Currently, RK3576 mainly uses 6-layer vias and 8-layer vias for the stackup. The following stackup is provided as an example to assist engineers in selecting and evaluating stackup structures. If choosing a different type of stackup, please recalculate the impedance based on the specifications provided by the PCB manufacturer.

3.1.1 8-Layer PCB Stackup

In the design of an 8-layer PCB stackup, it is recommended to stack the layers as follows: TOP-Gnd-Power-Power/Signal-Gnd-Signal-Gnd-Bottom. The reference plane for the top signal layer (L1) is L2, and the reference plane for the bottom signal layer (L8) is L7. The signal layers L6 have reference planes L5 and L7, with L5 being the primary reference plane. The specific configuration may vary depending on the stackup requirements. The copper thickness for all layers should be 1oz. The diagram below shows a reference stackup for a 1.6mm board thickness, and the core thickness can be adjusted based on the board thickness requirements.

Table 3-1 8-Layer PCB Stackup

8层通孔1.6+/-0.16mm				
Layer	Mother Board	Typical layer thickness (mil)	Dielectric Constant	DF
	Solder Mask	1.10		
L1	1/3oz+plating	1.20		
	Prepreg(1080)	2.70	4.00	0.019
L2	copper	1.20		
	Core	8.00	4.2	0.015
L3	copper	1.20		
	Prepreg (1080)	3.30	4.00	0.019
L4	copper	1.20		
	Core	24.00	4.2	0.015
L5	copper	1.20		
	Prepreg (1080)	3.30	4.00	0.019
L6	copper	1.20		
	Core	8.00	4.2	0.015
L7	copper	1.20		
	Prepreg(1080)	2.70	4.00	0.019
L8	1/3oz+plating	1.20		
	Solder Mask	1.10		
		63.80		

Impedance		40 ohm	45 ohm	50 ohm	55 ohm	80 ohm	85 ohm	90 ohm	95 ohm	100 ohm
Reference Layer	width	width	width	width	width/space	width/space	width/space	width/space	width/space	
Layer	Reference Layer									
L1	L2	6.5	5.4	4.5	3.5	5/3.8	4.6/4.2	4.2/4.6	3.85/4.95	3.5/5.3
L1	L3		22.5							
L3	L2/L4	5.7	4.5	3.6		4.7/5.3	4.2/5.8	3.8/6.2	3.5/7.5	3/7
L6	L5/L7	5.7	4.5	3.6		4.7/5.3	4.2/5.8	3.8/6.2	3.5/7.5	3/7
L8	L7	6.5	5.4	4.5	3.5	5/3.8	4.6/4.2	4.2/4.6	3.85/4.95	3.5/5.3

Note: The unit of line width and line spacing is mil. Line space refers to the air gap.

3.1.2 6-Layer (Pseudo 8-Layer) PCB Stackup

For improved signal quality, a 6-layer PCB stackup with a pseudo 8-layer design is recommended, utilizing a structure where layers L3 and L4 are spaced apart. The suggested layer stackup is as follows: TOP-GND-POWER-Signal/POWER-GND-Bottom. The reference plane for the top signal layer (L1) is L2, and the reference plane for the bottom signal layer (L6) is L5. The signal layer L4 has reference planes L3 and L5, with L5 being the primary reference plane. The specific configuration may vary depending on the stackup requirements. The copper thickness for all layers should be 1oz. The diagram below shows a reference stackup for a 1.6mm board thickness, and the core thickness can be adjusted based on the board thickness requirements.

It is recommended to compare the cost of the 6-layer(pseudo 8-layer) board with the actual cost of an 8-layer board. If the pseudo 8-layer board does not offer cost advantages over the 8-layer board, it is advisable to directly use the 8-layer board solution.

Table 3-2 6-Layer (Pseudo 8-Layer) PCB Stackup

6层通孔（假8层）1.6+/-0.16mm				
Layer	Mother Board	Typical layer thickness (mil)	Dielectric Constant	DF
	Solder Mask	1.1		
L1	1/3oz+plating	1.2		
	Prepreg (1080)	2.7	4	0.019
L2	copper	1.2		
	Core	3	4.2	0.015
L3	copper	1.2		
	Prepreg (2116)	4	4	0.019
	Core	32	4.2	0.015
	Prepreg (2116)	4	4	0.019
L4	copper	1.2		
	Core	3	4.2	0.015
L5	copper	1.2		
	Prepreg (1080)	2.7	4	0.019
L6	1/3oz+plating	1.2		
	Solder Mask	1.1		
		60.8		

Impedance		40 ohm	45 ohm	50 ohm	55 ohm	80 ohm	85 ohm	90 ohm	95 ohm	100 ohm
Reference Layer	width	width	width	width	width/space	width/space	width/space	width/space	width/space	
Layer	Reference Layer									
L1	L2	6.5	5.4	4.5	3.5	5/3.8	4.6/4.2	4.2/4.6	3.85/4.95	3.5/5.3
L1	L3		12.5							
L3	L2/L4	5.7	4.6	3.6		4.4/5.6	3.9/6.1	3.5/6.5	3.5/9.5	3/9
L4	L3/L5	5.7	4.6	3.6		4.4/5.6	3.9/6.1	3.5/6.5	3.5/9.5	3/9
L6	L5	6.5	5.4	4.5	3.5	5/3.8	4.6/4.2	4.2/4.6	3.85/4.95	3.5/5.3

Note: The unit of line width and line spacing is mil. Line space refers to the air gap.

3.1.3 6-Layer PCB Stackup

In the design of a 6-layer PCB stackup, it is recommended to stack the layers as follows: TOP-GND-POWER-Signal/POWER-GND-Bottom. The reference plane for the top signal layer (L1) is L2, and the reference plane for the bottom signal layer (L6) is L5. The signal layer L4 has reference planes L3 and L5, with L3 being the primary reference plane. The specific configuration may vary depending on the stackup requirements. The copper thickness for all layers should be 1oz. The diagram below shows a reference stackup for a 1.6mm board thickness, and the core thickness can be adjusted based on the board thickness requirements.

Table 3-3 6-Layer PCB Stackup

6层通孔1.6+/-0.16mm				
Layer	Mother Board	Typical layer thickness (mil)	Dielectric Constant	DF
	Solder Mask	1.1		
L1	1/3oz-plating	1.2		
	Prepreg (1080)	2.7	4	0.019
L2	copper	1.20		
	Core	21.60	4.2	0.015
L3	copper	1.20		
	Prepreg (1080)	3	4	0.019
L4	copper	1.20		
	Core	21.60	4.2	0.015
L5	copper	1.20		
	Prepreg (1080)	2.70	4	0.019
L6	1/3oz-plating	1.20		
	Solder Mask	1.10		
		61		

Layer	Reference Layer	Impedance	40 ohm	45 ohm	50 ohm	55 ohm	80 ohm	85 ohm	90 ohm	95 ohm	100 ohm
		width	width	width	width	width	width/space	width/space	width/space	width/space	width/space
L1	L2	6.5	5.4	4.5	3.5	5/3.8	4.6/4.2	4.2/4.6	3.85/4.95	3.5/5.3	
L1	L3										
L3	L2/L4	5.9	4.65	3.7		4.5/5.5	4.05/5.95	3.6/6.4	3.5/8.7	3/8	
L4	L3/L5	5.9	4.65	3.7		4.5/5.5	4.05/5.95	3.6/6.4	3.5/8.7	3/8	
L6	L5	6.5	5.4	4.5	3.5	5/3.8	4.6/4.2	4.2/4.6	3.85/4.95	3.5/5.3	

Note: The unit of line width and line spacing is mil. Line space refers to the air gap.

3.2 Fanout Design for RK3576

The RK3576 package has a total of 698 balls, with a mixed pitch consisting of 0.55mm, 0.6mm, and 0.65mm, as shown in the diagram.

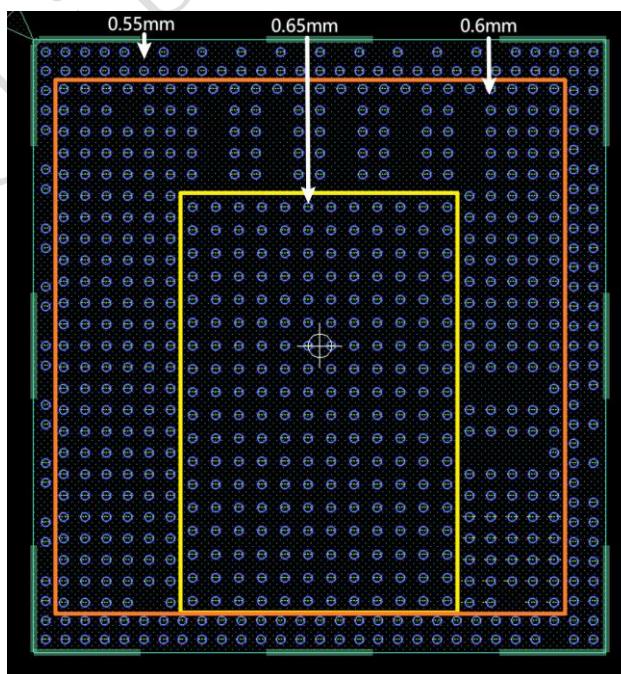


Figure 3-1 RK3576 package with ball pitches

- Outer two circles of Ball's fan-out design

For the RK3576 SoC, the fanout design should of the outermost two rows of balls and some of the balls in the third row after removing certain balls, from the TOP layer, routing can be done with a minimum trace width of 3.5mil for local fanout. After that, it is recommended to transition to the corresponding characteristic impedance traces as soon as possible, with the minimum trace width kept short, following the required line width and spacing for fanout.

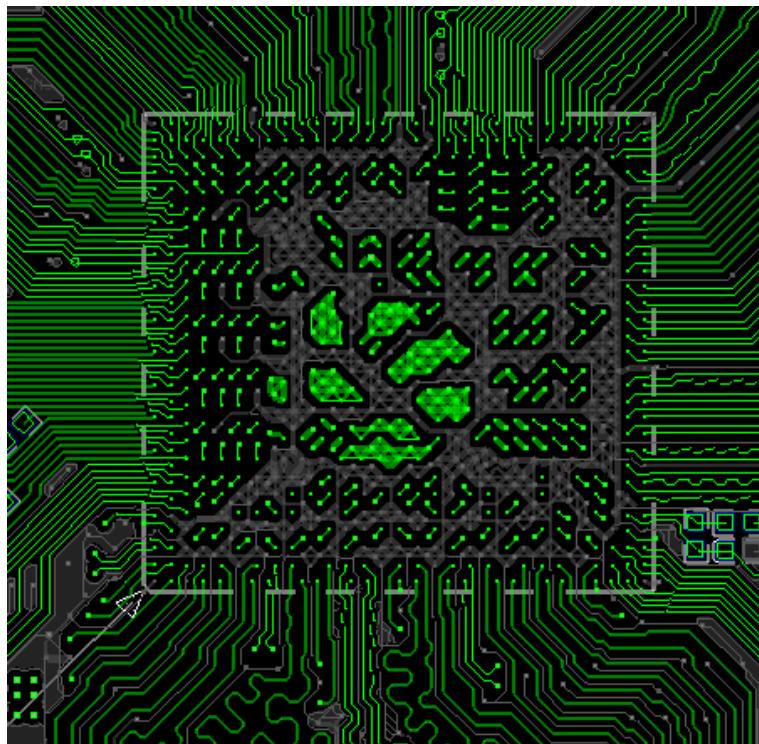


Figure 3-2 RK3576 fanout diagram 1

- The inner rows of ball's fan-out design

Starting from the fourth row and some of the third row, it is necessary to transition to inner layers. The transition vias should be placed in a regular pattern, and it is recommended to have a gap of 2-4 rows between each transition via row, allowing for larger channels for the ground and power planes.

In the case of the ground plane copper cladding pictured below, there are multiple channels connected to the outside ground, which facilitates signal integrity, power integrity as well as heat dissipation.

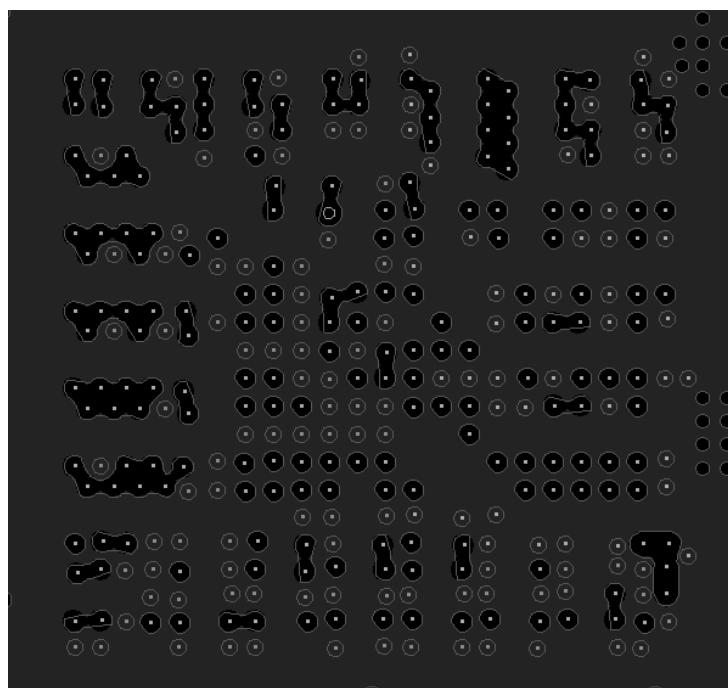


Figure 3-3 RK3576 fanout diagram 2

The power plane should have regular placement of vias to provide as large a copper coverage as possible for various power supplies, improving power delivery quality.

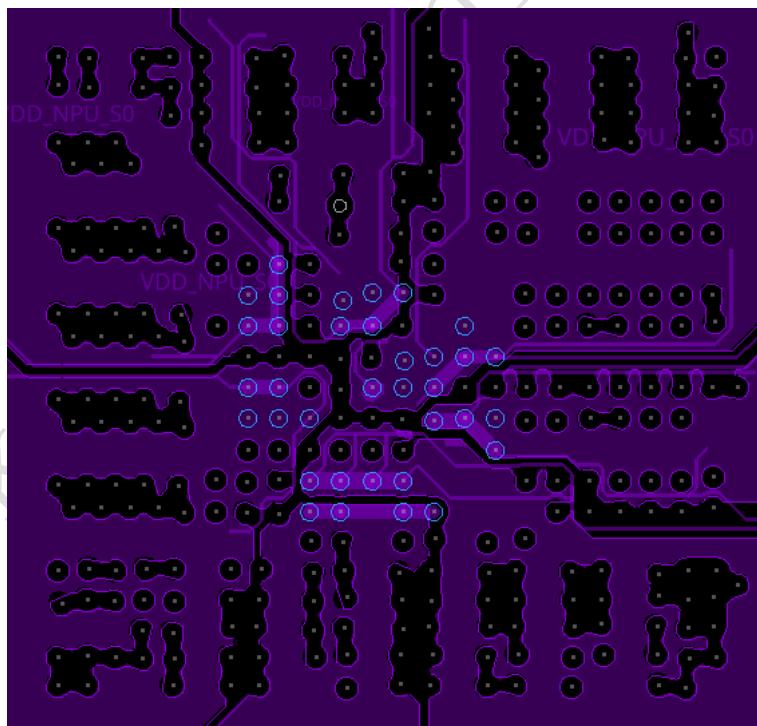


Figure 3-4 RK3576 fanout diagram 3

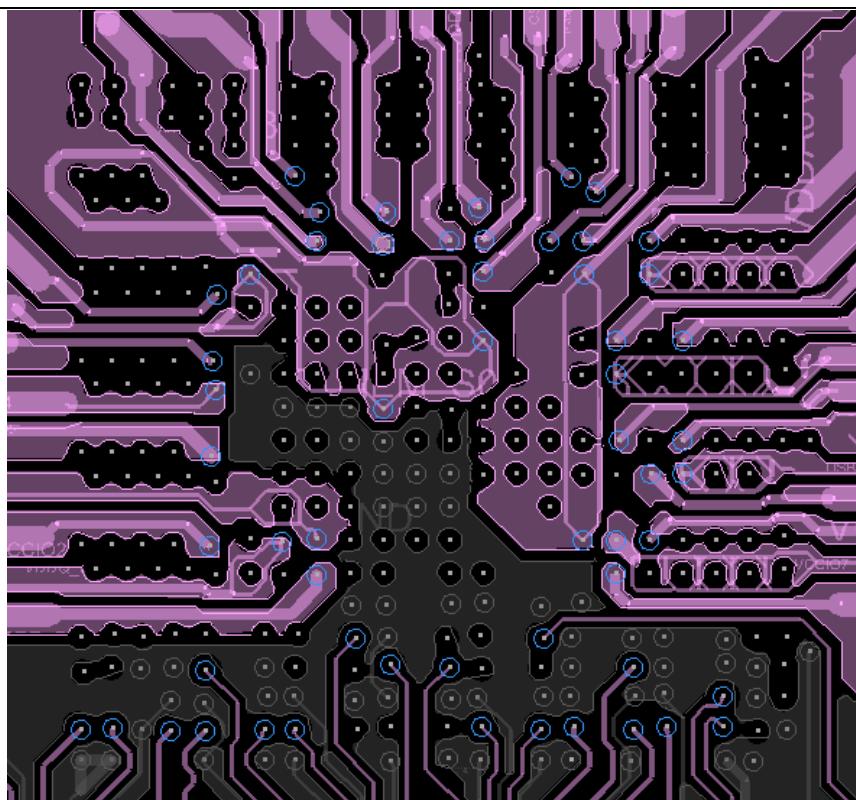


Figure 3-5 RK3576 fanout diagram 4

After the regular placement of vias, the bottom layer routing can use a 4mil trace width for fanout.

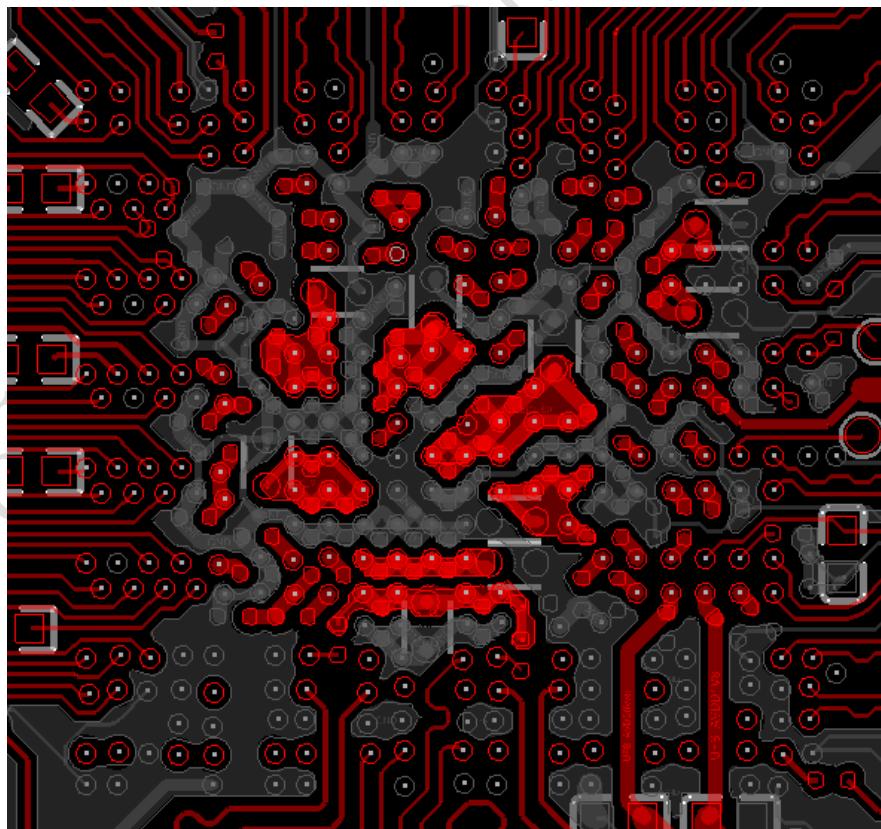


Figure 3-6 RK3576 fanout diagram 5

3.3 General Layout Recommendations

3.3.1 Suggestions for Capture and Allegro

- When generating a netlist using OrCAD Capture, if you encounter the error shown in the diagram, you need to set the Char Limit to 255.

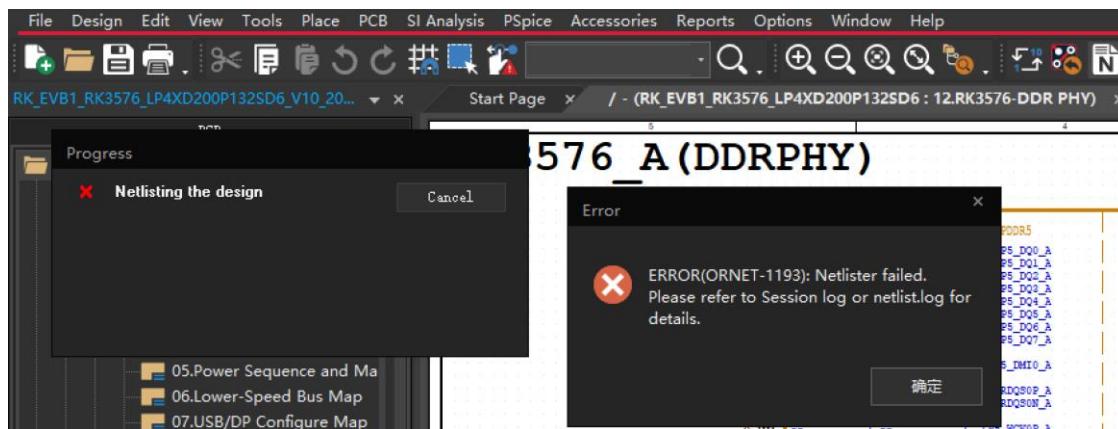


Figure 3-7 Create Netlist error

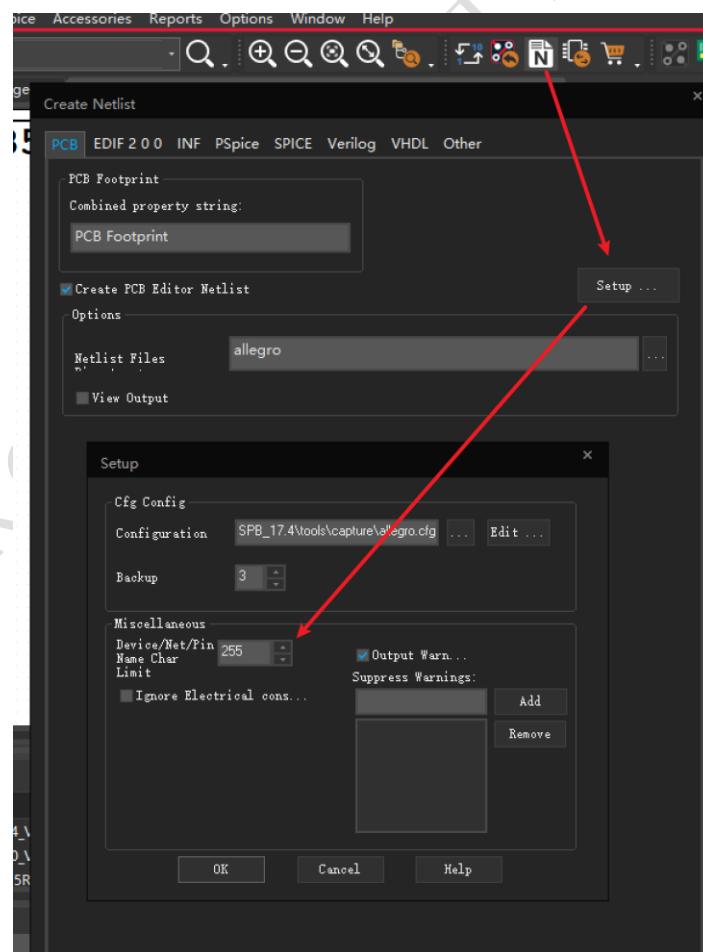


Figure 3-8 Char Limit setup

- When import logic using Allegro, if you encounter the error shown in the diagram, you need to

synchronize the Long name size setting to 255.

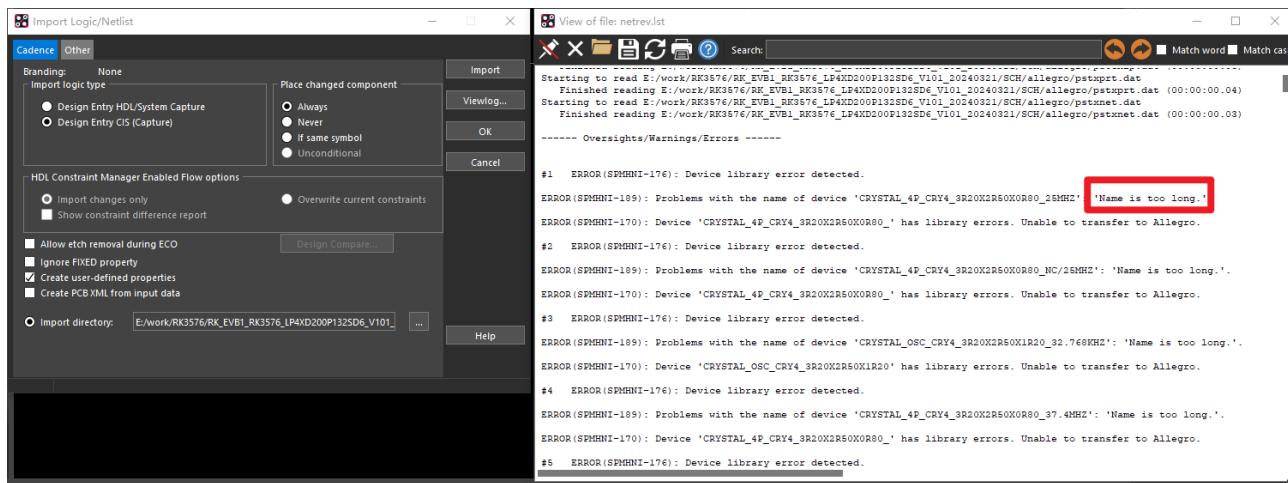


Figure 3-9 Import Logic error

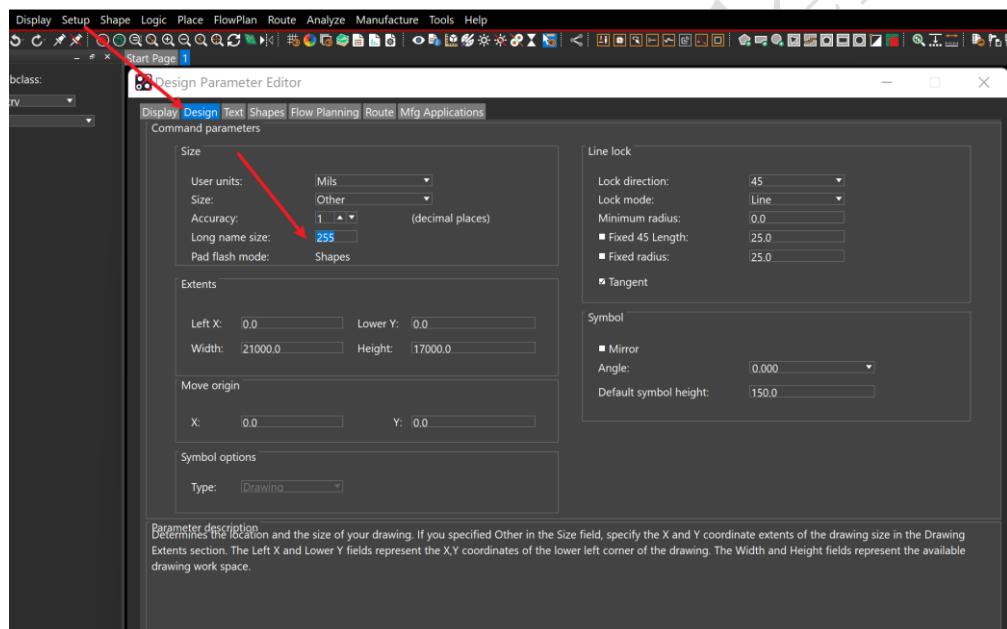


Figure 3-10 Long name size setup

- Non-functional annular rings can damage the copper plating and increase parasitic capacitance of vias. It is recommended to remove non-functional annular rings and solder rings on inner layers to enhance the integrity of copper planes. In Allegro, you can disable non-functional annular rings and solder rings on inner layers using the following methods:
- For Allegro 16.6: Go to Setup -> Unused Pads Suppression and select the pins and vias you want to disable.

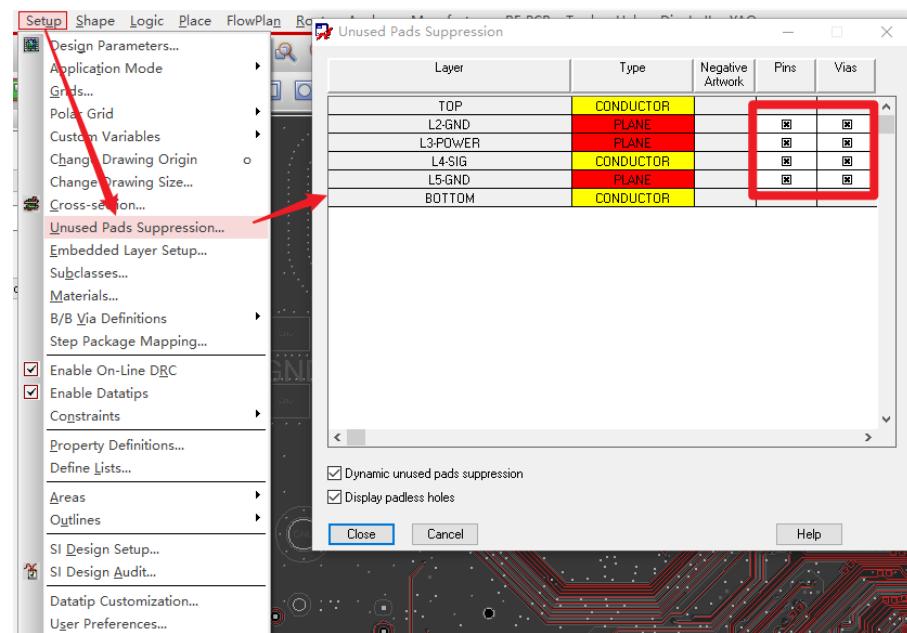


Figure 3-11 Disabling non-functional annular rings and solder rings in Allegro 16.6

- For Allegro 17.4: Xsection-Physical-Unused Pads/Via Suppression and select the pins and vias you want to disable.

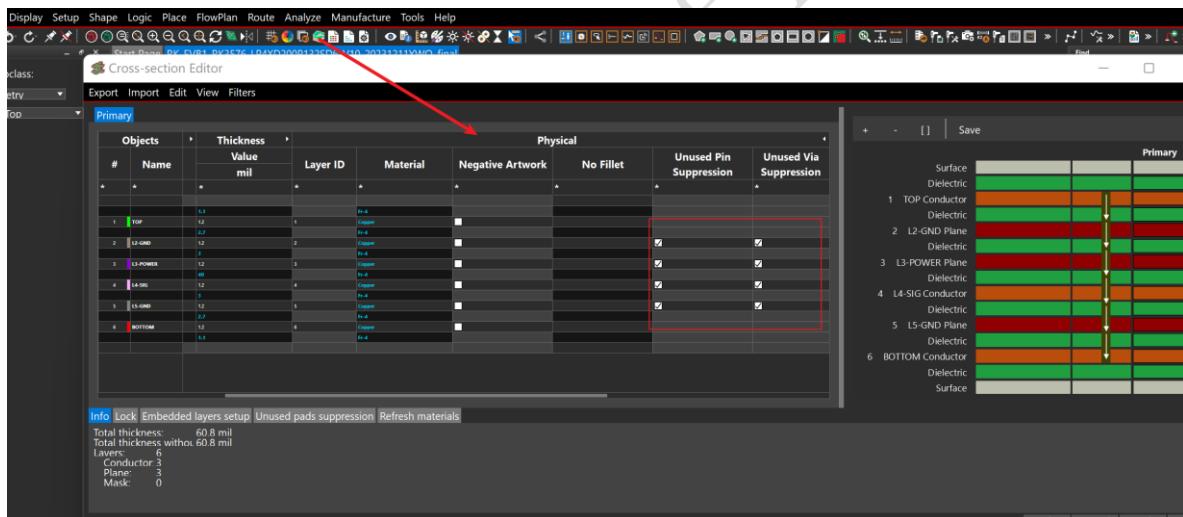


Figure 3-12 Disabling non-functional annular rings and solder rings in Allegro 17.4

3.3.2 Layout Recommendations

- Interface Placement: Unless limited by structural constraints or length-matching requirements, place the interfaces as close as possible to the main RK3576 chip. Keep the overall trace lengths as short as possible, especially for critical signal lines.
- Component Placement: Consider debugging, maintenance, and heat dissipation when arranging components.
- Circuit Module Layout: Aim for balanced, compact, and aesthetically pleasing layouts for circuit modules, while minimizing loop areas.
- Spacing between Circuit Modules: Provide appropriate spacing between different circuit modules to

reduce mutual interference, especially for high-frequency components.

- Decoupling Capacitor Placement: Place decoupling capacitors as close as possible to the power pins of the IC to minimize the loop formed between power and ground.
- Clock Signal Termination Resistors: Place the series termination resistors for clock signals, such as eMMC clock, close to the RK3576 (SoC) side. It is recommended to keep the distance between the resistor and the pin within 400mil.

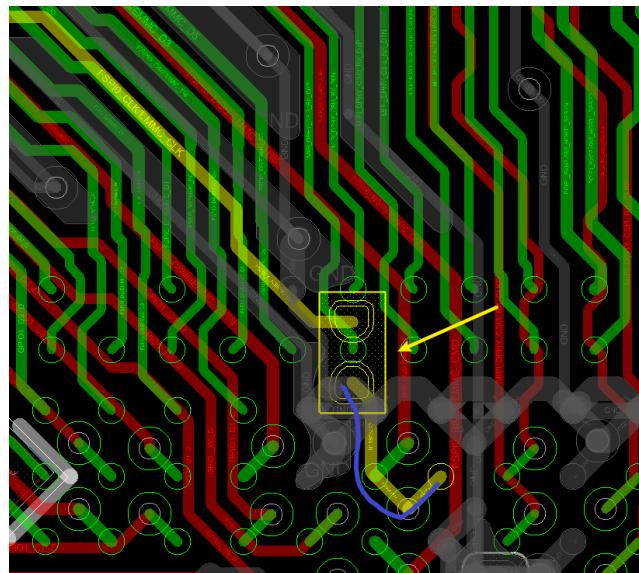
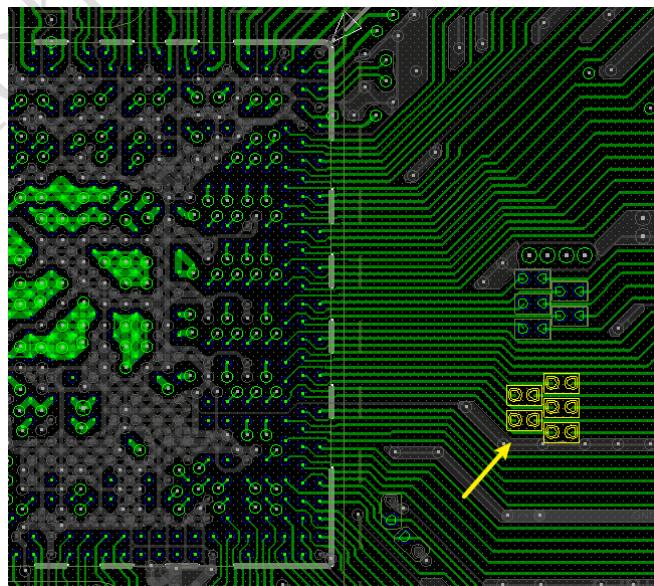


Figure 3-13 Placement of clock signal' series connected resistors

- Place the series connected resistors for TX signals close to the transmitting end and for RX signals close to the receiving end. Keep the trace lengths between the pins and resistors within 400mil. For example, for GMAC's TXD0-TXD3, TXCLK, and TXEN, place the series matching resistors close to the RK3576 (source) end, and for RXD0-RXD3, RXCLK, and RXDV, place the series matching resistors close to the PHY end.



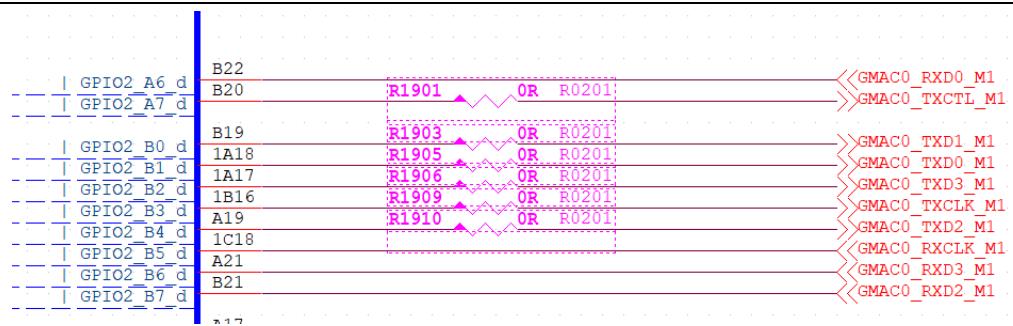
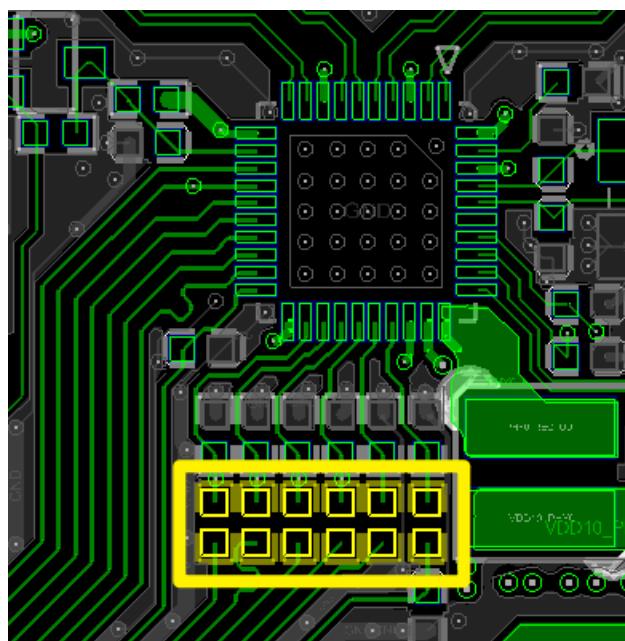


Figure 3-14 Placement of TX series resistors



Close to PHY

PHY0_RXD0/RXDLY	R6744 OR R0402	GMAC0_RXD0_M1
PHY0_RXD1/TXDLY	R6745 OR R0402	GMAC0_RXD1_M1
PHY0_RXD2/PLLOFF	R6746 OR R0402	GMAC0_RXD2_M1
PHY0_RXD3/PHYAD0	R6747 OR R0402	GMAC0_RXD3_M1
PHY0_RXCLK/PHYAD1	R6748 OR R0402	GMAC0_RXCLK_M1 C67341 2 NC C0402
PHY0_RXCTL/PHYAD2	R6749 OR R0402	GMAC0_RXCTL_M1

Figure 3-15 Placement of RX series resistors

- Place ESD protection components near the interfaces, and consider placing coupling capacitors near connectors.

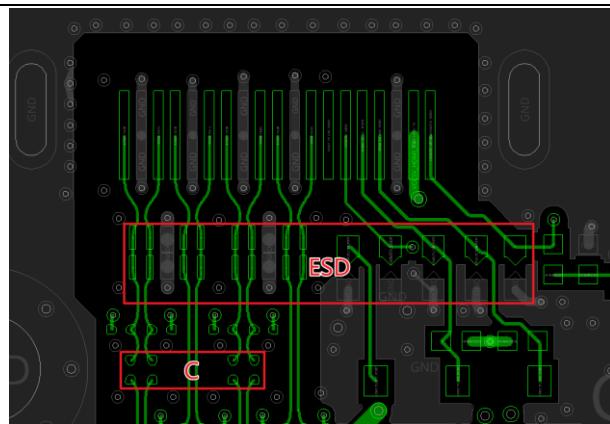


Figure 3-16 Placement of ESD protection components and coupling capacitors

3.3.3 Routing Recommendations

- (1) Trace length should include package and via.
- (2) Minimize sharp corners in routing, and consider using 135-degree angles instead of 90-degree angles.
- (3) Remove all non-functional pads.
- (4) Avoid routing around clock devices (such as crystals, oscillators, clock buffers), switching power supplies, magnetic components, and through-holes for connectors.
- (5) It is recommended not to place test points on high-speed signals.
- (6) The distance between traces and the copper plane of the same layer should be equal to or greater than 4 times the trace width.

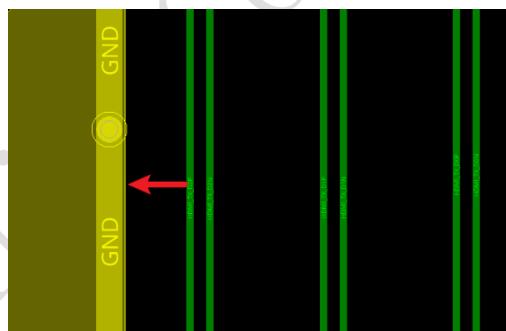


Figure 3-17 Distance between traces and same-layer copper plane

- (7) Avoid crossing different regions with high-speed signals. It is recommended to keep a distance of at least 40mil between the high-speed signal and the edge of the reference plane.

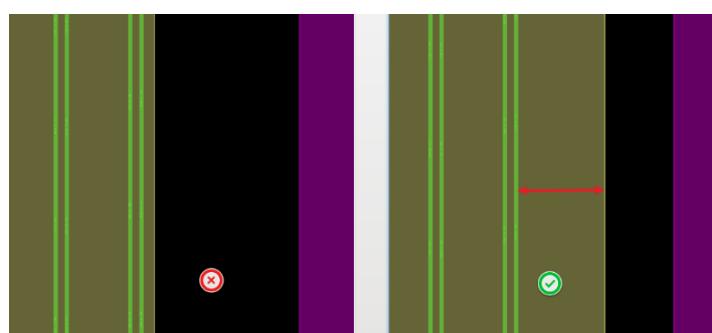


Figure 3-18 High-speed signal and reference plane edge

- (8) Use serpentine routing to reduce crosstalk caused by routing.

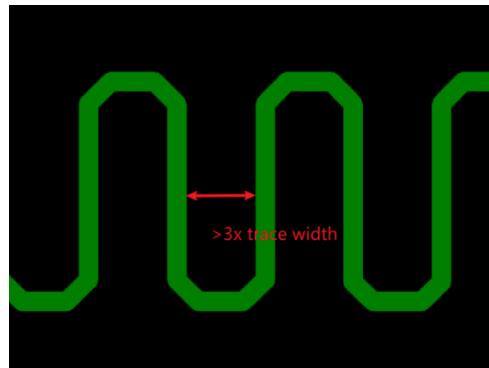


Figure 3-19 Serpentine Trace Recommendation

- (9) Minimize the stub length as much as possible, it is recommended to keep the stub length as zero.

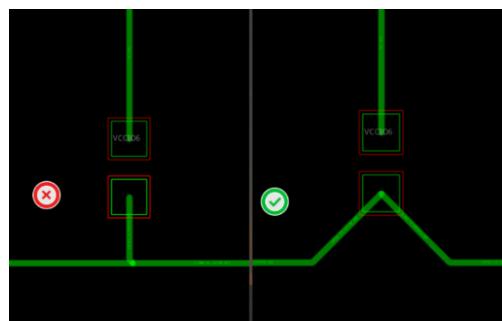


Figure 3-20 Trace Stub

- (10) Due to reduced impedance caused by surface-mounted component pads, to minimize the impact of impedance variation, it is recommended to remove a layer of the reference plane directly below the pad. Common surface-mounted components include capacitors, ESD protection devices, common mode chokes, connectors, etc.

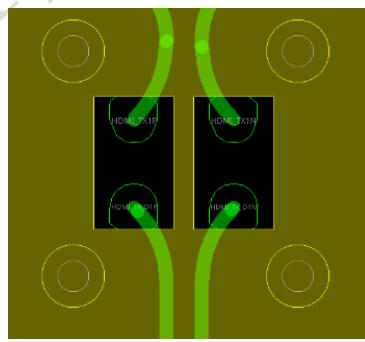


Figure 3-21 Removal of reference plane under surface-mounted component pads

- (11) When copper is placed on the connector pads, ensure that the ground copper does not exceed the ground pad.

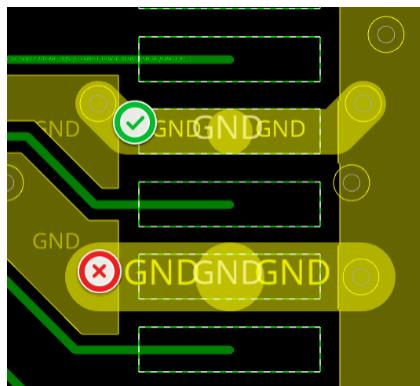


Figure 3-22 Copper placement on connector pads

- (12) The distance between the ground copper on the connector and the signal pad should be at least 3 times the trace width.

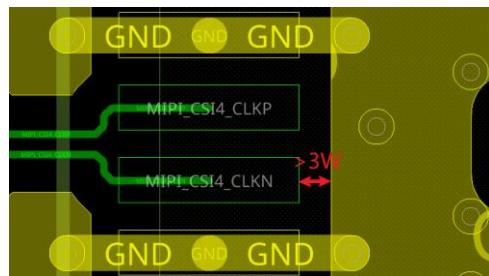


Figure 3-23 Ground copper on connector

- (13) It is recommended to have at least one ground via near each ground pad of a high-speed connector, and the via should be placed as close as possible to the pad.

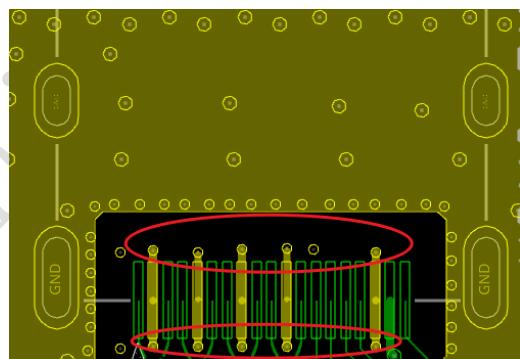


Figure 3-24 Ground via near connector pad

- (14) Use routing to connect the gaps in the BGA area.

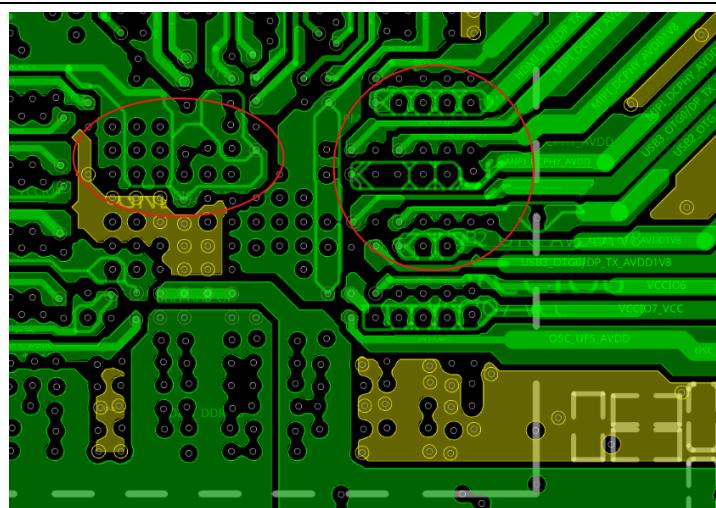


Figure 3-25 Routing in the BGA area

(15) Avoid the stub effect of vias, especially when the stub length exceeds 12mil. It is recommended to evaluate the impact of via stubs on signal integrity through simulation.

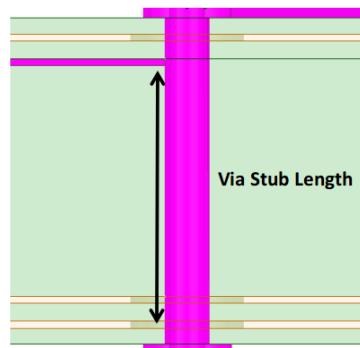


Figure 3-26 Via stub effect

(16) It is recommended to have one ground via for each GND pin of ICs (such as eMMC chips, flash chips).

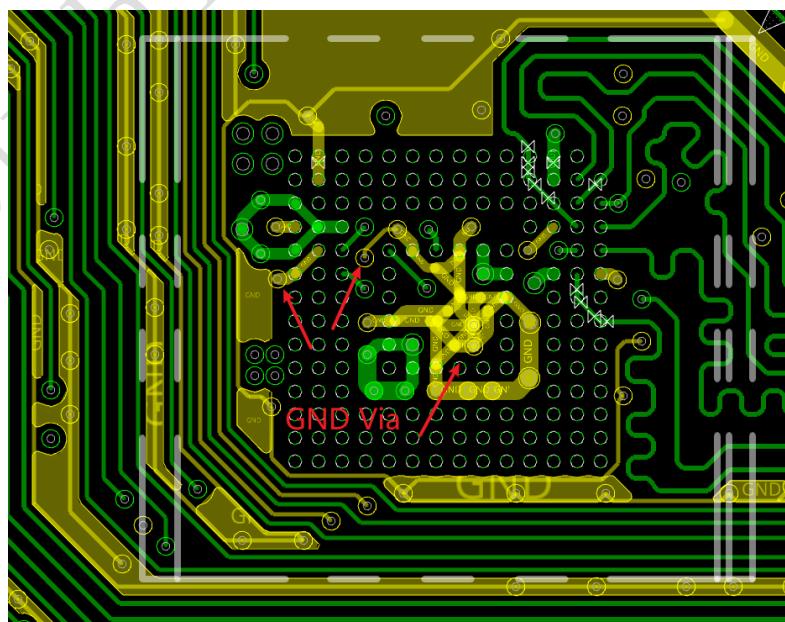


Figure 3-27 Ground via for IC GND pins

- (17) It is recommended to have one ground via for each GND pin of ESD protection devices, and the via should be placed as close as possible to the pad.

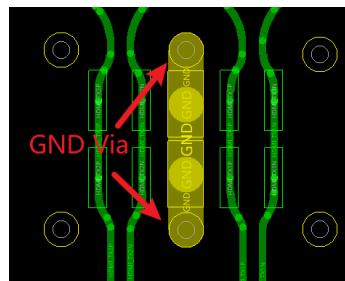


Figure 3-28 ESD device with ground via

- (18) When changing layers and the reference planes before and after the change are ground planes, place a companion via next to the signal via to ensure the continuity of the return path. For single-ended signals, it is recommended to place a return via next to the signal via to reduce crosstalk between vias.

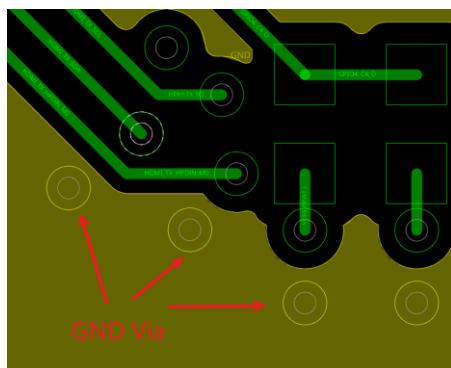


Figure 3-29 Single-ended signal via transition

- (19) For important high-speed single-ended signals such as clock signals, reset signals (e.g., emmc_clk, emmc_datastrobe, RGMII_CLK, etc.), it is recommended to surround them with ground traces. Place a ground via every 500mil along the ground trace.

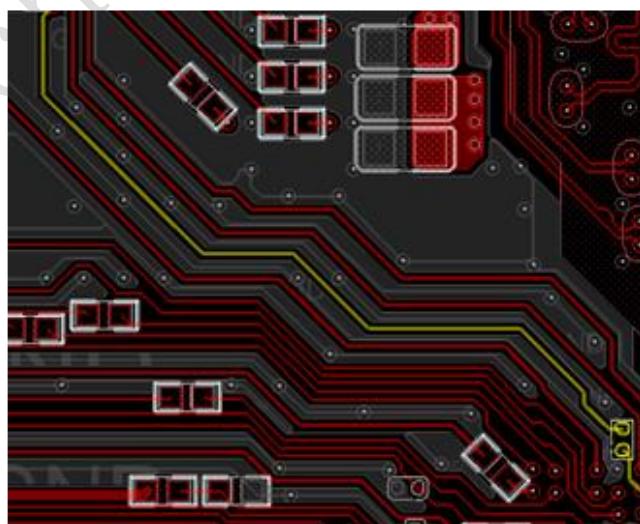


Figure 3-30 Ground trace for single-ended signals

- (20) Intra-pair skew is the term used to define the difference length between + and - in a differential pair. Inter-

pair skew is used to define the difference length between a differential pair and another differential pair. The space between signals is defined as air-gap distance.

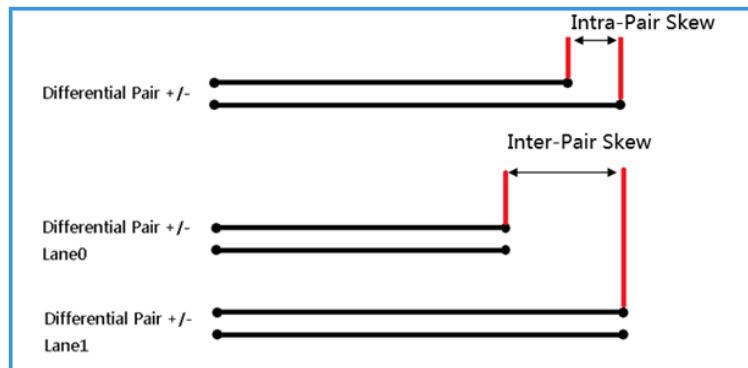


Figure 3-31 Differential Pair Skew

- (21) Route trace over continuous GND plane without interruption. Any discontinuity or split on the reference plane will degrade signal integrity significantly.

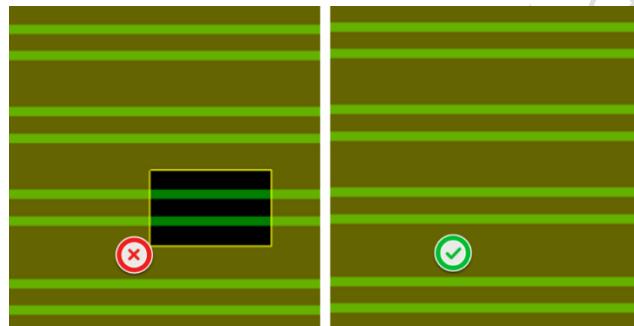


Figure 3-32 Incomplete Reference Plan

- (22) When the reference plane of the routing has cross-power layers, it is recommended that ground capacitance be added to each of the 2 power layers to provide a complete return path.

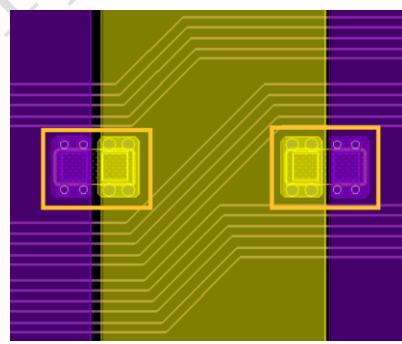


Figure 3-33 Cross-Power Plan

- (23) Differential signals require equal lengths within pairs, that is, the time delay difference between P and N should be as small as possible. Therefore, when the time delay difference occurs between the differential lines P and N, the nearby winding is compensated. Special attention should be paid to the size of the winding, which should meet the requirements shown in the figure below to reduce the impact of sudden changes in impedance.

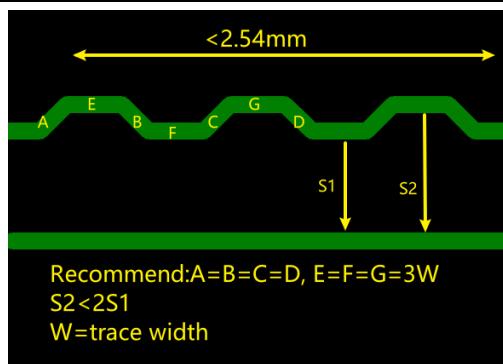


Figure 3-34 Winding Dimension

(24) If there is an unequal length (within 300mil) in the differential pair, make the compensation as soon as possible.

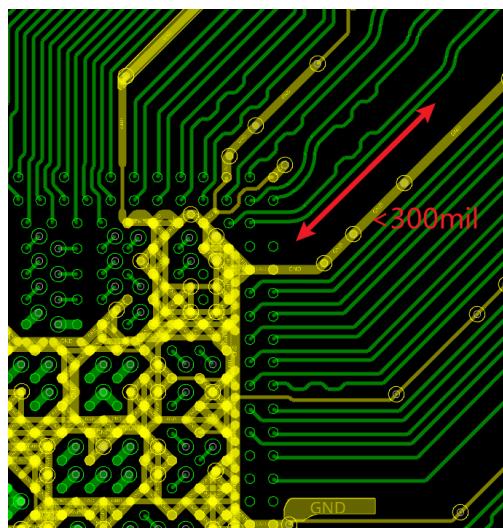


Figure 3-35 Skew Compensation

(25) Place ground stitching vias near the signal transition vias. For differential signals, both signal vias and stitching vias should be placed symmetrically.

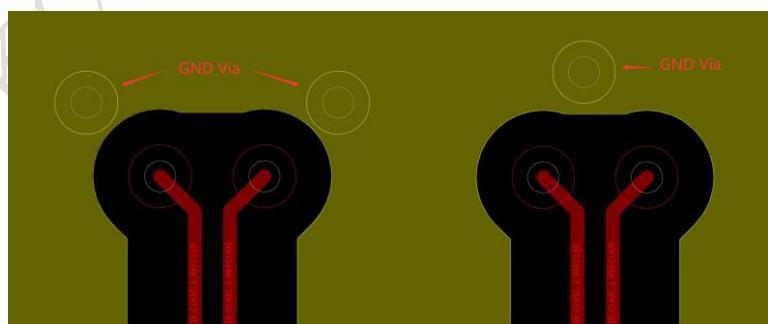


Figure 3-36 Gnd Via for Differential Via

(26) Route differential pairs on symmetry.

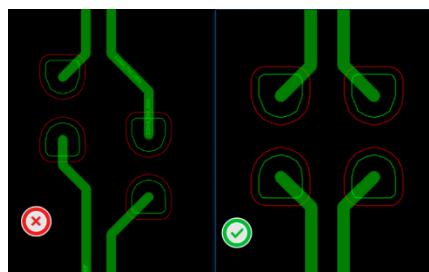


Figure 3-37 symmetry layout

(27) Proposed ground shielding.

L: GND via interval length.

D: Distance from shielding to trace $\geq 4*W$.

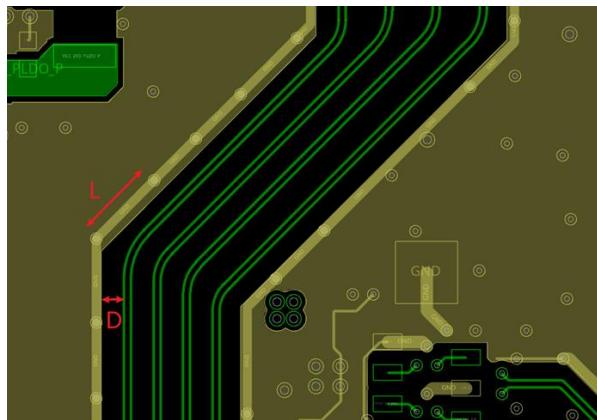


Figure 3-38 Ground Shielding

3.4 Routing Requirements for Signal Running $\geq 8\text{GT/s}$

RK3576 below the interface signal can work in 8GT/s and above rate, due to the high rate, PCB design requirements will be more stringent, in the "3.3 Layout General Recommendations" chapter based on the need to be in accordance with the requirements of this chapter to the wiring.

Table 3-4 RK3576 Differential Signal $\geq 8\text{GT/s}$

Interface	Signal
DP1.4@8.1Gbps	DP_TX_D0P;DP_TX_D0N; DP_TX_D1P;DP_TX_D1N; DP_TX_D2P;DP_TX_D2N; DP_TX_D3P;DP_TX_D3N;
HDMI2.1@12Gbps	HDMI_TX_D0P;HDMI_TX_D0N; HDMI_TX_D1P;HDMI_TX_D1N; HDMI_TX_D2P;HDMI_TX_D2N; HDMI_TX_D3P;HDMI_TX_D3N;

3.4.1 Void the Ground Plane Under the BGA Pads

If these interface operating $\geq 8\text{GT/s}$, we strongly recommend to void the GND reference plane (on Layer 2) under the BGA pad of signal in Table 3-1 to reduce capacitance. The voiding size is 7mil in radius.

If these interface operating below 8GT/s, for example, DP only running at 5.4GT/s or lower, then there is no need to void.

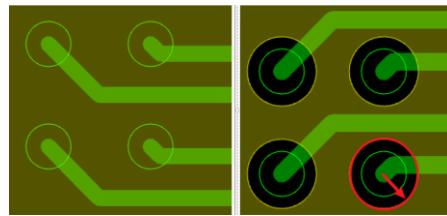


Figure 3-39 Reference Plane Voiding

3.4.2 Avoiding Glass Weave Effect

The glass weave effect refers to the difference in dielectric constant between the glass fiber and epoxy resin used to fill and laminate PCB substrates. When the D+ trace of a differential pair is located above the resin filling while the D- trace is located above the glass fiber, it can result in different characteristic impedances and time delays between the D+ and D- traces. This leads to a timing skew within the differential pair, which can affect the eye diagram quality.

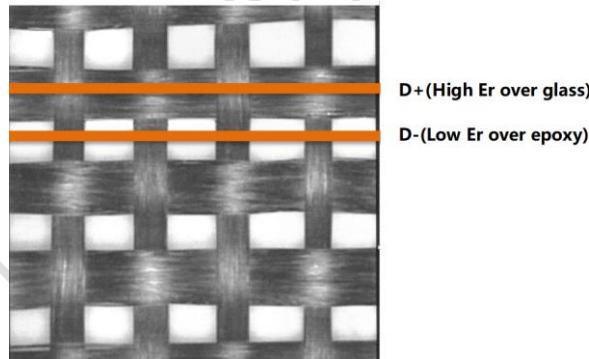


Figure 3-40 Glass weave effect

When the data rate of the interface in Table 3-1 reaches 8GT/s and the trace length exceeds 1.5 inches, it is important to carefully address the glass weave effect. It is recommended to use one of the following methods to mitigate the impact of the glass weave effect.

Method 1: Change the routing angle to be between 10° and 35° , or rotate the PCB by 10° during fabrication to ensure that none of the traces are parallel to the glass fibers.

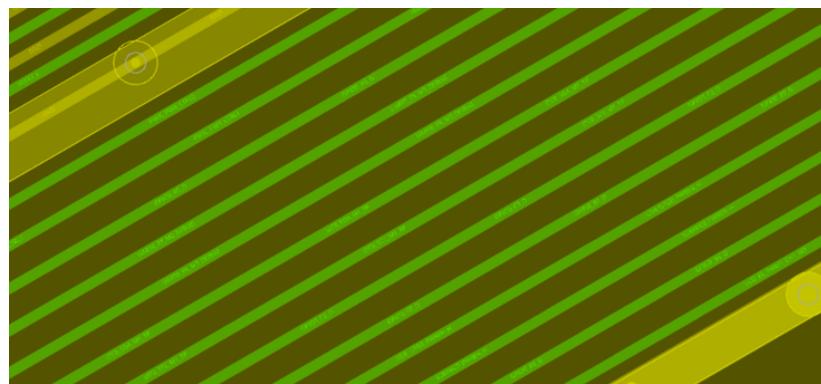


Figure 3-41 Changing routing angle

Method 2: Use a zigzag routing pattern as shown below. The width "W" in the diagram should be at least 3 times the distance between glass weaves. The recommended values are W=60mil, $\theta=10^\circ$, L=340mil.

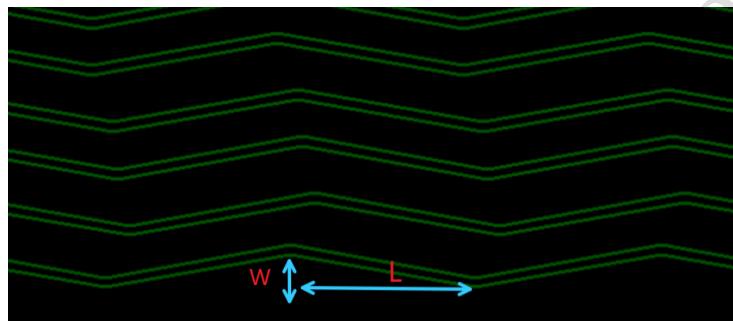


Figure 3-42 Zigzag routing pattern

3.4.3 Differential Via Recommendations

If the operating speed of the interfaces in Table 3-1 is $\geq 8\text{GT/s}$, the recommended size for the differential via pairs should be optimized through simulation based on the actual stack-up. The following are the reference dimensions for the vias based on the EVB through-hole stack-up:

R_Drill=0.1mm (drill radius)

R_Pad=0.2mm (pad radius)

D1: Center-to-center spacing of the differential vias

D2: Size of the solder mask opening from the top layer to the bottom layer

D3: Center-to-center spacing between the signal via and the return ground via

Table 3-5 reference dimensions for the differential vias.

Method	D1(mil)	D2(mil)	D3(mil)	Differential via Impedance
1	26	18	22~26	100 ohm
2	24	18	22~26	95 ohm
3	22	18	22~26	90 ohm
4	22	15	22~26	85 ohm

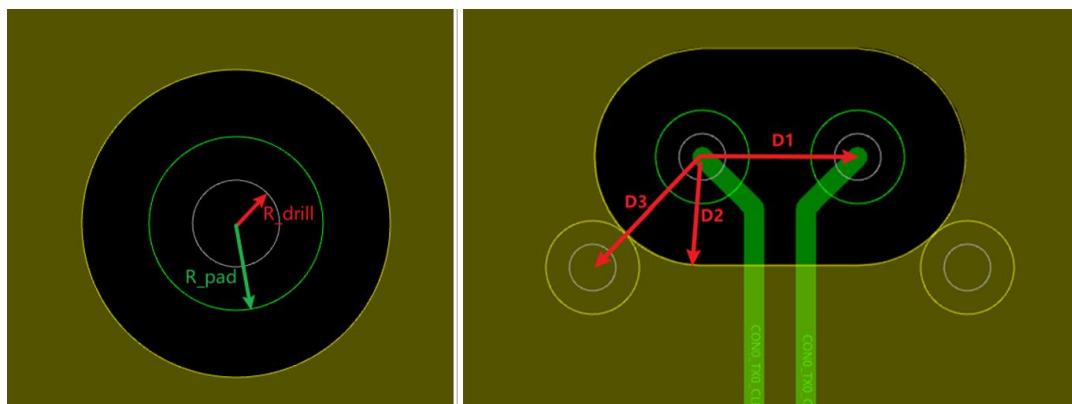


Figure 3-43 dimensions for the differential via

3.4.4 Coupling Capacitor Pad Reference Layer Void Optimization Recommendations

If the operating speed of the interfaces in Table 3-1 is $\geq 8\text{GT/s}$, the recommended optimization for the differential coupled capacitor pads is as follows:

Based on the interface selection, void one or two layers of the ground plane. If voiding the ground reference layer directly beneath the capacitor pad (L2), a layer separation reference is required, meaning that L3 should be the ground reference layer. If voiding both L2 and L3 ground reference layers, then L4 should be the ground reference layer. The void size should be determined through simulation based on the actual stack-up. The following are the reference dimensions based on EVB:

Additionally, four ground vias should be placed around the coupling capacitors to connect the ground reference layers of L2~L4.

Table 3-6 reference values for the void size of the coupling capacitor pads

Interface	Void layer	D1	H	L
DP1.4	L2 and L3	25mil	22mil	Equal to pad length
HDMI2.1	L2 and L3	25mil	20mil	Equal to pad length

D1: centre distance between differential coupling capacitors;

L: length of the void;

H: width of the void.

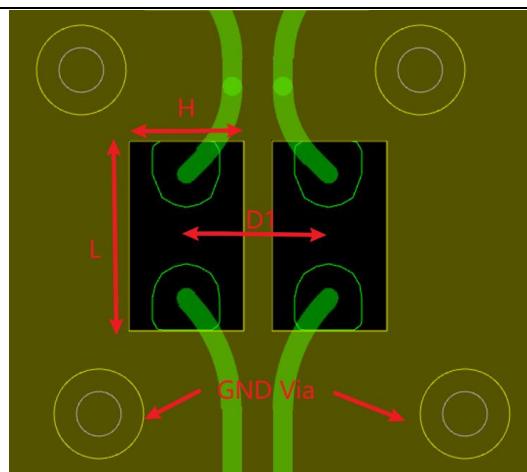


Figure 3-44 Schematic of coupling capacitor pad void dimensions

3.4.5 ESD Pad Reference Layer Void Optimization

If the operating speed of the interfaces in Table 3-1 is $\geq 8\text{GT/s}$, the recommended optimization for the ESD devices of these interfaces is as follows:

Void the ground reference layers (L2 and L3) directly beneath the ESD pads, with L4 serving as the separation reference layer and being connected to the ground plane. The void size should be determined based on the ESD model and the actual stack-up through simulation. The following are the reference dimensions based on the ESD model ESD73034D used in the EVB:

Additionally, four ground vias should be placed around each ESD device to connect the ground reference layers of L2~L4.

Table 3-7 reference dimensions for the void size of the ESD device pads

interface	Void layer	H	W
DP1.4	L2 and L3	22mil	Equal to pad length
HDMI2.1	L2 and L3	22mil	Equal to pad length

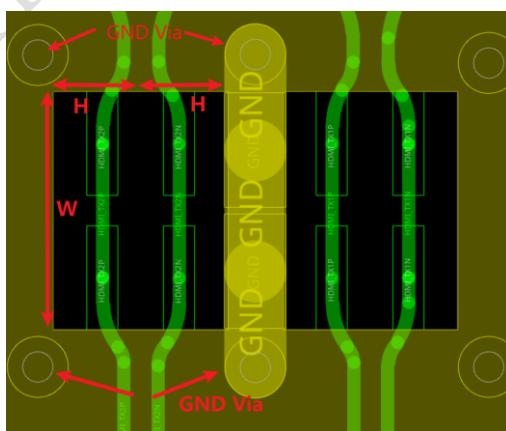


Figure 3-45 schematic diagram of the reference dimensions for the void size of the ESD device pads

3.4.6 Connector Pad Reference Layer Void Optimization Recommendations

If the operating speed of the interfaces in Table 3-1 is $\geq 8\text{GT/s}$, the connectors for these interfaces should

meet the corresponding standard requirements (such as HDMI2.1/DP1.4/). It is recommended to use connectors from manufacturers such as Molex, Amphenol, HRS, and so on.

Based on the interface selection, void one or two layers of the ground plane beneath the connector pads. If voiding the ground reference layer (L2) directly beneath the connector pad, a layer separation reference is required, meaning that L3 should be the ground reference layer. If voiding both L2 and L3 ground reference layers, then L4 should be the ground plane and serve as the separation reference layer. The void size should be determined based on the connector model and the actual stack-up through simulation.

It is recommended to place two ground vias near each ground pad of the connector, as close as possible to the pad.

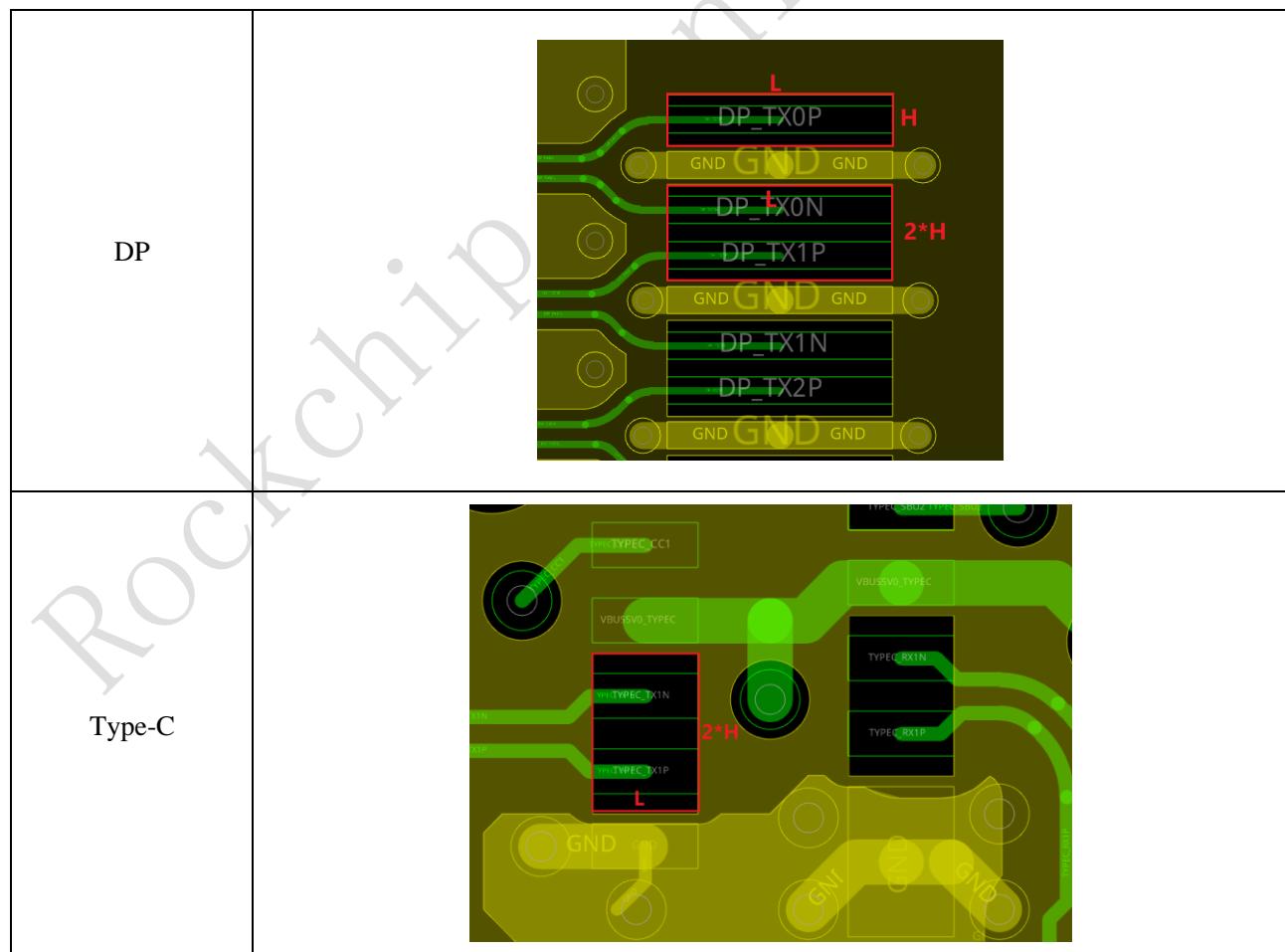
The following are the reference dimensions for the void size based on the EVB:

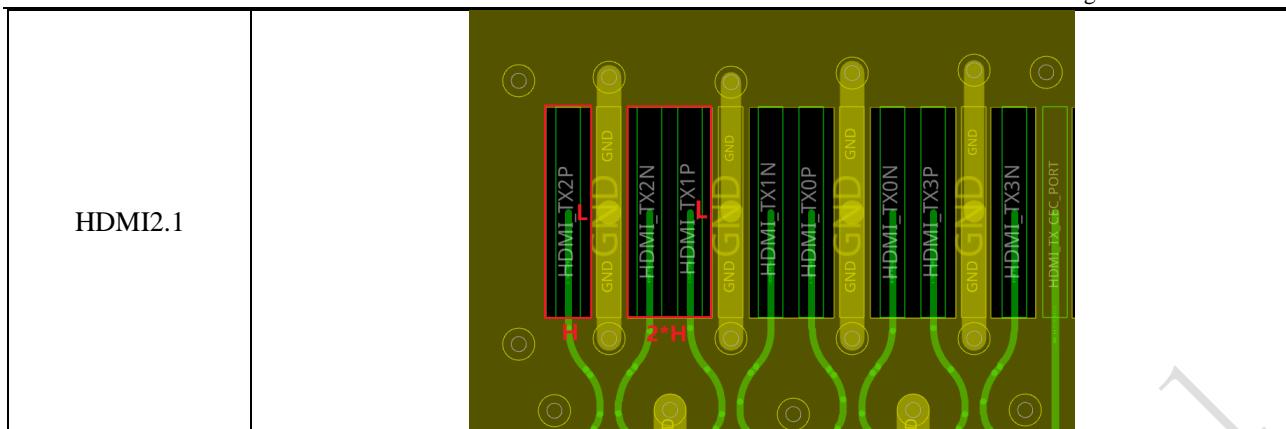
Table 3-8 reference dimensions for the void size of the connector pads

Connector	Model	Void Layer	H	L
DP	Molex 472720029	L2 and L3	22mil	Equal to pad length
Type-C	Molex 1054500101	L2 and L3	21mil	Equal to pad length
HDMI2.1	Molex 2086581051	L2 and L3	22mil	Equal to pad length

the recommended wiring methods for the connectors as follow:

Table 3-9 recommended wiring methods for the connectors.





3.5 Modules PCB Design Recommendations

- When laying out the interfaces/functional modules, unless constrained by structural limitations or length matching requirements, it is advisable to place the interfaces as close to the RK3576 as possible, with short traces, minimal layer changes, and no crossings.
- It is recommended to replicate the layout and routing of the reference template provided by RK for the minimum system, which includes RK3576, LPDDR4/4x/5, and PMIC RK806S-5.
- Without affecting the power plane, it is recommended to place as many back-drilled ground vias as possible in the various functional areas below the RK3576 (SoC).
- All signals of the interface circuits/functional modules should be grouped together and fully surrounded by a ground plane, isolated from signals of other modules to reduce mutual interference. The spacing between the back-drilled vias for ground connection should be $\leq 300\text{mil}$. The reference layer for all signals should be a complete ground plane to avoid interrupted signal return paths caused by consecutive vias.
- When signals need to change layers, it is recommended to add back-drilled vias near the position within 30mil, and the two back-drilled vias for differential signals should be symmetrically placed.
- Decoupling capacitors for the corresponding power domain under the RK3576 (SoC) should be placed close to the corresponding power pins. Each capacitor should be paired with one or more power vias and ground vias. The power fan-out should be wide and quickly widened to 20mil or more.
- Decoupling capacitors for grain ends/interface circuits must be placed near the corresponding pins, with short and wide traces to meet their respective current requirements.
- Please refer to the "Layout General Recommendations" in section 3.3 and the specific recommendations for each interface below.

3.5.1 Clock/Reset Circuit PCB Design

In the PCB design of the clock circuit, please pay attention to the following:

- The layout of the crystal circuit should be given priority. It should be placed on the same layer as the chip and as close as possible to avoid drilling vias. The traces of the crystal should be kept short, away from sources of interference, and preferably far from the board edges.
- The crystal and clock signals should be fully surrounded by a ground plane. Every 200-300mil, a GND via should be added to the ground trace, and the ground reference plane on the adjacent layer must be

intact.

- If the crystal circuit is placed on a different layer than the chip, the crystal traces must be fully surrounded by a ground trace to avoid interference.
- No traces are allowed near the clock traces Xin and Xout and the projection area below the crystal to prevent noise coupling into the clock circuit.
- On the top layer below the crystal, a ground ring can be placed. The ground ring is connected to the adjacent ground plane through vias to isolate noise.
- The second layer below the crystal should maintain an intact ground reference plane without any trace cuts to help isolate noise and maintain the crystal's output.

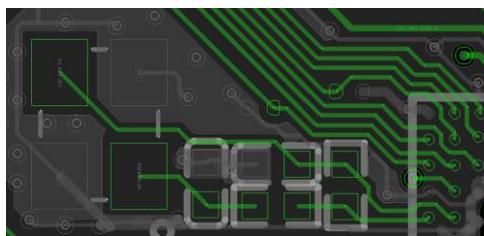


Figure 3-46 crystal layout and traces for RK3576

- For the decoupling capacitors of the power supplies PLL_DVDD0V75, PLL_AVDD1V8, OSC_AVDD1V8, and PMU_LOGIC_DVDD0V75, they must be placed on the backside of the chip's pins. When routing, try to route through the capacitor pads before reaching the chip's pins.

In the PCB design of the reset circuit, please pay attention to the following:

- During layout, keep the RESET_L reset signal away from the board edges and metal connectors to prevent abnormal resets caused by ESD, which could lead to module crashes.
- The decoupling capacitor for RESET_L filtering should be placed as close to the chip's pins as possible. The signal should pass through the capacitor before entering the chip. Note that the ground pad of the filtering capacitor must have a 0402 ground via, and if space allows, it is recommended to have two or more for better grounding.
- The RESET_L signal should be kept away from strong interference signals such as DCDC and RF to prevent interference. If the traces are long, it is recommended to surround them with a ground trace, and every 400mil, a GND via should be added to the ground trace.
- The TVS protection diode for the RESET_L button should be placed as close to the button as possible. The signal path should be: button → TVS → 100 ohm resistor → capacitor (near CPU & PMIC) → CPU & PMIC. When an ESD event occurs, the ESD current must pass through the TVS device for attenuation.

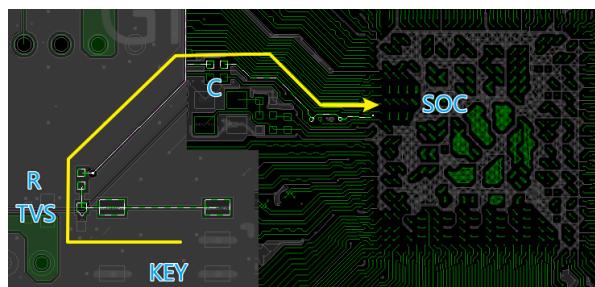


Figure 3-47 distribution of the RESET_L path on the PCB

3.5.2 PMIC/Power Circuit PCB Design

3.5.2.1 PCB Design for RK806S-5 Power Solution

In the overall layout, from the perspective of power quality, RK806S-5 should be placed as close to RK3576 as possible (considering heat dissipation design, it should be placed appropriately, not too close or too far). When placing it, prioritize arranging the traces (copper) from the power sources with higher output currents of RK806S-5 to RK3576 in a continuous manner, avoiding crossing if possible.

Consider the following:

- The 10nF capacitor for RESETB of RK806S-5 must be placed close to the RK806S-5 pin to improve the chip's anti-interference ability.
- As an example, for vias of size 0503, a single via is recommended to carry 0.8A for high-voltage power, and for low-voltage power (below 1V), the current calculation is 0.4A.
- The negative terminal of high-current BUCK input/output capacitors should have the same number of vias as the positive terminal to achieve better filtering effect (many engineers tend to overlook the vias for the negative terminal of capacitors).
- It is not recommended to use "thermal pads" for the solder pads or holes of power components. They should be fully covered with copper.
- It is recommended to avoid copper coverage on the pins of RK806S-5. All pins should be connected to the outside through traces, and the trace width should not exceed the width of the pins to prevent solder bridging issues when the solder pads become larger during PCB fabrication.
- The grounding pads (ePad) of RK806S-5 should have a sufficient number of vias. It is recommended to have a quantity of vias of 7x7 for size 0503 or 8x8 for size 0402 (e.g., RK3576 EVB1 adopts 9x9 for size 0503). This helps to reduce ground impedance and enhance heat dissipation.

Figure 3-46 shows the distribution of ePad vias for RK806S-5.

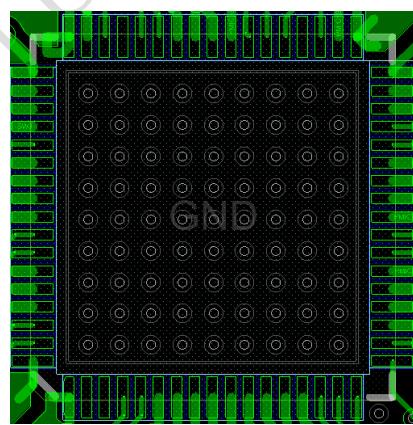


Figure 3-48 distribution of RK806S-5 ePad vias

- PCB Design Requirements for RK806S-5 BUCK1/BUCK3

(1) Power input via requirements: For areas requiring vias, if VCC1/3 is combined for power supply, at least 5 vias of size 0503 are required. If they are separated, each should have 3 or more vias of size 0503.

(2) Input capacitor requirements: The input capacitors must be placed as close to the chip as possible. If the input capacitors are placed on the backside of the chip, ensure that the GND terminal of the capacitors is close to the ePad of RK806S-5. This minimizes the connection loop between the input capacitors, VCC, and GND.

(3) SW trace requirements: The SW traces should be kept as short and wide as possible (after the chip pins, enlarge the area as early as possible) to improve current capability and power efficiency.

(4) Output capacitor requirements: The allocation of output capacitors should be based on the actual load conditions and ripple requirements, following the reference diagram.

(5) Power output via requirements: Determine the number of vias based on the actual application current. For example, in the case of RK3576, BUCK1 supplies 4A to CPU_BIG, and BUCK3 supplies 2A to CPU_LIT. The via requirements are as follows:

- The GND terminals of the output capacitors for BUCK1 and BUCK3 can be shared but require at least 15 vias of size 0503. If space allows, additional smaller vias can be added.
- If there are layer changes for BUCK1 output, ensure at least 10 vias of size 0503. For BUCK3, **at least 5 vias of size 0503 should be provided.**

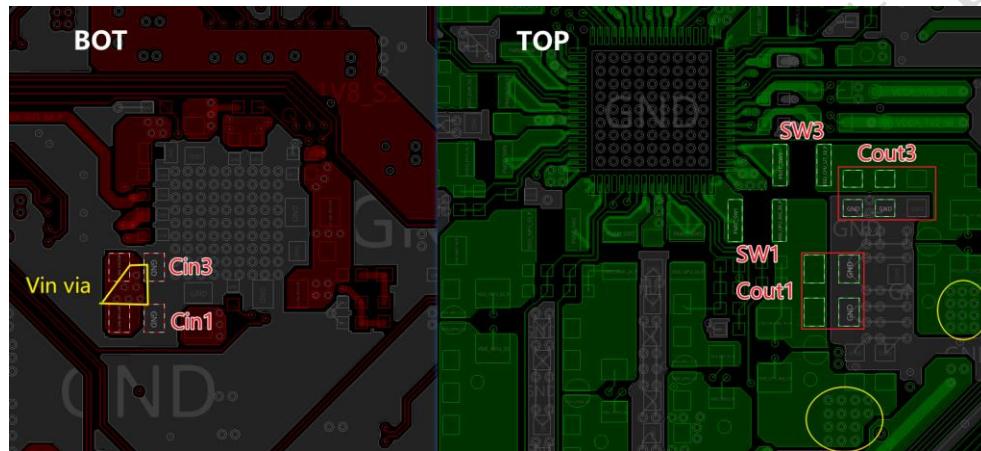


Figure 3-49 the layout and traces for RK806S-5 BUCK1/BUCK3

● PCB Design Requirements for RK806S-5 BUCK2

(1) Power input via requirements: For areas requiring vias, VCC2 power supply should have at least 3 vias of size 0503.

(2) Input capacitor requirements: The input capacitors must be placed as close to the chip as possible. If the input capacitors are placed on the backside of the chip, ensure that the GND terminal of the capacitors is close to the ePad of RK806S-5. This minimizes the connection loop between the input capacitors, VCC, and GND.

(3) SW trace requirements: The SW traces should be kept as short and wide as possible (after the chip pins, enlarge the area as early as possible) to improve current capability and power efficiency.

(4) Output capacitor requirements: The allocation of output capacitors should be based on the actual load conditions and ripple requirements, following the reference diagram.

(5) Power output via requirements: Determine the number of vias based on the actual application current. For example, in the case of RK3576, BUCK2 supplies 4A to the NPU. The via requirements are as follows: The GND terminal of the output capacitors should have at least 10 or more vias of size 0503. If space allows, additional smaller vias can be added. If there are layer changes for the output, ensure at least 10 or more vias of size 0503 for the layer change.

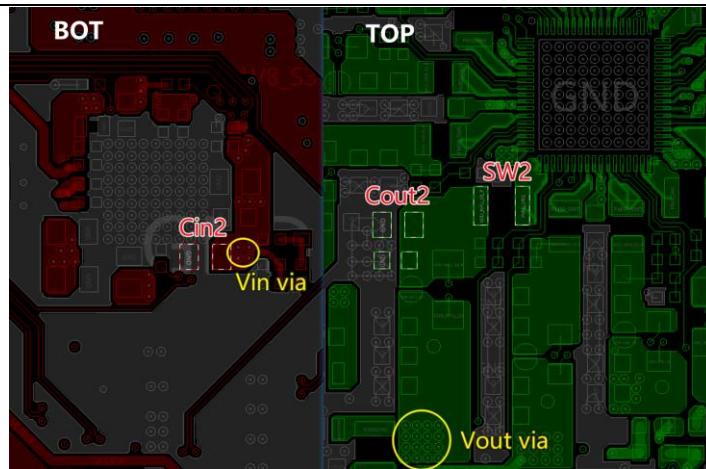


Figure 3-50 the layout and traces for RK806S-5 BUCK2

- PCB Design Requirements for RK806S-5 BUCK4

(1) Power input via requirements: For areas requiring vias, VCC4 power supply should have at least 3 vias of size 0503.

(2) Input capacitor requirements: The input capacitors must be placed as close to the chip as possible. If the input capacitors are placed on the backside of the chip, ensure that the GND terminal of the capacitors is close to the ePad of RK806S-5. This minimizes the connection loop between the input capacitors, VCC, and GND.

(3) SW trace requirements: The SW traces should be kept as short and wide as possible (after the chip pins, enlarge the area as early as possible) to improve current capability and power efficiency.

(4) Output capacitor requirements: The allocation of output capacitors should be based on the actual load conditions and ripple requirements.

(5) Power output via requirements: Determine the number of vias based on the actual application current. For example, in the case of RK3576, BUCK4 supplies 3.5A to the 3.3V power source. The via requirements are as follows: The GND terminal of the output capacitors should have at least 6 or more vias of size 0503. If insufficient, additional smaller vias can be added. If there are layer changes for the output, ensure at least 6 or more vias of size 0503 for the layer change. Please note that if BUCK4 has a larger load scenario, such as with a 5A load, the number of vias needs to be increased accordingly: The GND terminal of the output capacitors should have at least 9 or more vias of size 0503. If insufficient, additional smaller vias can be added. If there are layer changes for the output, ensure at least 9 or more vias of size 0503 for the layer change.

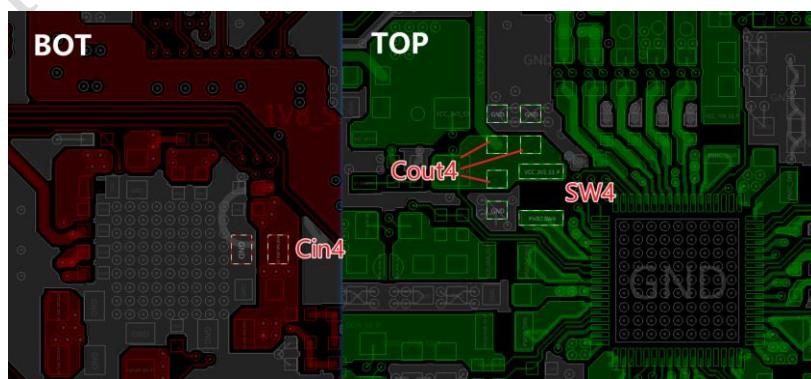


Figure 3-51 the layout and traces for RK806S-5 BUCK4

- PCB Design Requirements for RK806S-5 BUCK5/6/7/8/9/10

BUCK5/6/7/8/9/10 have a maximum output current of 3A.

- (1) Power input via requirements: For areas requiring vias, VCCx should have at least 2 vias of size 0503.
- (2) Input capacitor requirements: The input capacitors must be placed as close to the chip as possible. If the input capacitors are placed on the backside of the chip, ensure that the GND terminal of the capacitors is close to the ePad of RK806S-5. This minimizes the connection loop between the input capacitors, VCCx, and GND.
- (3) SW trace requirements: The SW traces should be kept as short and wide as possible (after the chip pins, enlarge the area as early as possible) to improve current capability and power efficiency.
- (4) Output capacitor requirements: The allocation of output capacitors should be based on the actual load conditions and ripple requirements, following the reference diagram.
- (5) Power output via requirements: The GND terminal of the output capacitors should have at least 6 vias of size 0503. If there are layer changes for the VOUTx output, ensure at least 6 or more vias of size 0503 for the layer change. It is important to note that the GND terminal of the input and output capacitors should have the same number of vias as the positive terminal. This ensures better filtering effectiveness.

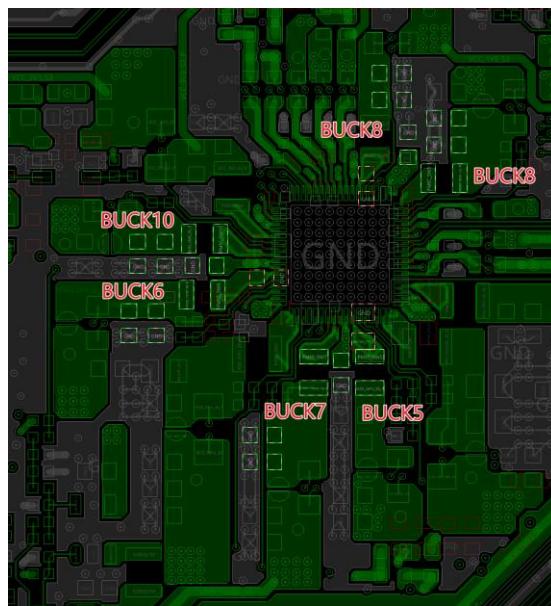


Figure 3-52 the layout and traces for RK806S-5 BUCK5/6/7/8/9/10

- PCB Design Requirements for RK806S-5 LDO

RK806S-5 integrates 11 LDOs, with 5 being NMOS LDOs and 6 being PMOS LDOs. Among them, NLDO1/2/5 and PLDO2/3/5/6 can handle a load of 300mA, while NLDO3/4 and PLDO1/4 can handle a load of 500mA.

The input capacitors must be placed as close to the chip as possible. The connection loop between the input capacitors, VCC11/12/13/14, and GND should be minimized. The VCCA capacitor of RK806S-5 must be placed near the pins, away from other sources of interference. The ground pad of the capacitor must be well grounded, ensuring the shortest possible path between the VCCA capacitor ground pad and the RK806S-5 ePad, without being divided by other signals.

The output capacitors must be placed as close to the chip as possible. The connection loop between the output capacitors, PLDO1/2/3/4/5/6, NLDO1/2/3/4/5, and GND should be minimized.

For LDOs with an output voltage of 1.8V and above, it is generally recommended to design the trace width as 1mm for 1A current. For LDOs with an output voltage below 1.8V, it is recommended to design the trace width as 1mm for 0.5A current. If the length of the trace exceeds 10cm, the width should be increased accordingly.

The trace width for LDO outputs should be increased as soon as possible after leaving the chip to meet the required current capacity. Pay special attention to the length and loss of traces for low-voltage, high-current NLDOs to meet the power supply voltage and ripple requirements of the target chip.

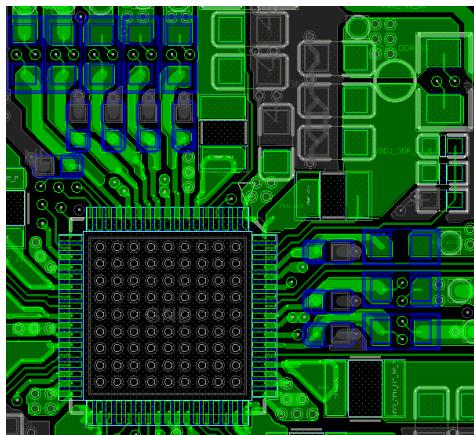


Figure 3-53 the layout and traces for RK806S-5 LDO

3.5.2.2 Discrete Power DC-DC PCB Design

The input capacitor Cin, output capacitor Cout, and DC/DC's GND should be placed between Vin Pin, Vout Pin, and the DC/DC circuit. The goal is to minimize the loop area between Vin, Vout, and DC/DC's GND. This helps reduce EMI (Electromagnetic Interference) and greatly improves the stability of the DC/DC circuit, as shown in the diagram below:

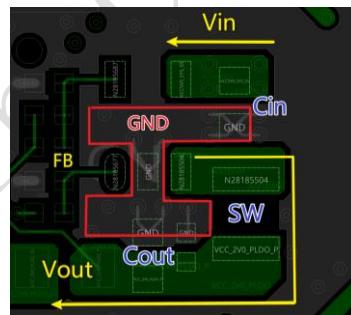


Figure 3-54 Discrete Power DC/DC Layout and Routing

The input capacitor Cin, output capacitor Cout, and DC/DC's GND should have multiple vias, recommended to have 4 or more 0503 vias. If there are layer changes for Vin and Vout, it is also recommended to have additional vias, preferably 4 or more 0503 vias (the number of vias depends on the current, as described below). The inductor should be placed as close to the DC/DC circuit as possible, and the traces should be made as wide and short as possible. The resistor at the FB terminal should be placed far away from sources of interference.

3.5.2.3 Discrete Power LDO PCB Design

The input capacitor Cin, output capacitor Cout, and LDO's GND should be placed between Vin Pin, Vout Pin, and the LDO circuit. The goal is to minimize the loop area between Vin, Vout, and LDO's GND. This helps reduce EMI (Electromagnetic Interference) and greatly improves the stability of the LDO circuit.



Figure 3-55 Discrete Power LDO Layout and Routing

The input capacitor C_{in} , output capacitor C_{out} , and LDO's GND should have multiple ground vias, recommended to have 4 or more 0503 vias. If there are layer changes for V_{in} and V_{out} , additional vias should be added, preferably 4 or more 0503 vias. The number of power vias and ground vias should be calculated based on the maximum power supply capacity of the chip, ensuring they meet the actual load power requirements.

LDOs have relatively low efficiency and generate significant heat. Therefore, special attention should be given to thermal dissipation for LDOs. Increasing the copper area and adding more vias can help with heat dissipation.

3.5.2.4 DC-DC Low Voltage High Current Power Supply Feedback Compensation Suggestions

In the RK3576 PMIC solution, for several high-current BUCK power supply sources, considering voltage, current, ripple, and PCB layout, three feedback compensation strategies are proposed:

- Proximal Feedback (Low current or high voltage applications)

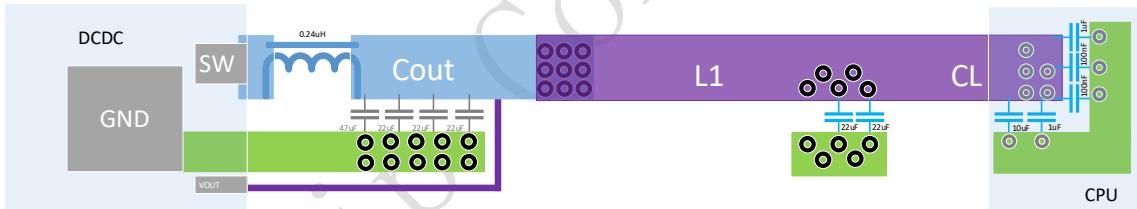


Figure 3-56 Proximal Feedback PCB Layout

Place the output capacitor C_{out} near the DC/DC and connect the feedback sampling point (FB/V_{OUT}) to the output filter capacitor C_{out} 's unconnected end.

Advantages: Better stability compared to other strategies, especially when the DC/DC is far from the load.

Disadvantages: Impedance and inductance introduced by the traces at high current and transient conditions can cause significant ripple.

Recommended for applications with low load current, short PCB traces, or relatively high output voltage.

- Distal Feedback (Conventional usage for RK)

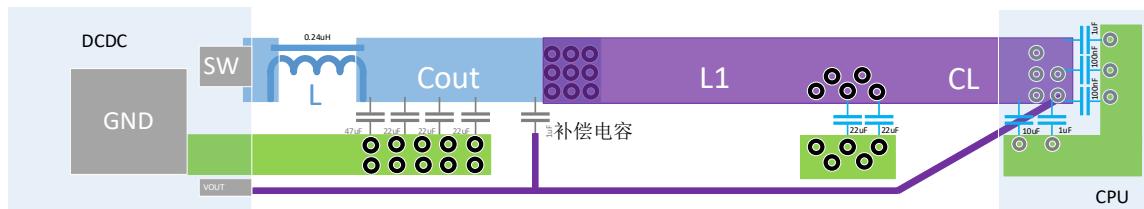


Figure 3-57 Distal Feedback PCB Layout

Take the feedback sampling point (FB/VOUT) of the DC/DC to the far end of the load.

Advantages: This method compensates for voltage losses due to IR drop under high current conditions, ensuring stable power supply voltage under heavy loads.

Disadvantages: It introduces an additional LC stage (L1 and CL) from the perspective of the DC/DC system, requiring appropriate feedforward compensation at the DC/DC end to counteract its impact. In practical use, if the load has fast transients, the ripple may still be larger than the proximal feedback method.

Although this compensation scheme increases the ripple, the benefits outweigh the drawbacks. This scheme is commonly used. However, with improved technology, the core supply voltage is getting lower, and the requirements for ripple are becoming smaller. Especially in large-scale applications, NPUs have new requirements for power supply transients, making this scheme gradually unable to meet the requirements.

- Distal Feedback with PCB Equivalent Inductance (Newly introduced)

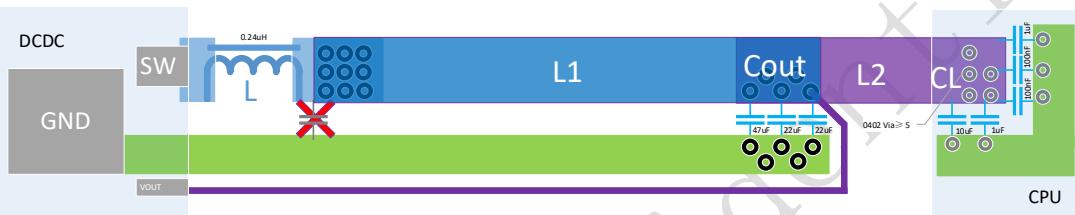


Figure 3-58 Distal Feedback with PCB Equivalent Inductance PCB Layout

Remove the main output capacitor (Cout) near the DC/DC. Move the main capacitor Cout as close to the load as possible. Sample the FB/Vout on the main capacitor and then use a short trace (L2) to connect to the load.

Design concept: The trace L1 in the diagram acts as a PCB inductance, which is in series with the inductance L. The combined effect of L and L1 is equivalent to a single inductance.

Design considerations: L2 should be as short and wide as possible to reduce voltage drop because this trace segment has no compensation. The voltage difference before and after L2 should be controlled within 10mV.

Characteristics:

- By removing the DC/DC-side capacitor and appropriately increasing the load-side capacitor, the cost is reduced.
- After the trace L1 acts as an inductance, the requirements for the L1 trace become lower, and it will not have a significant impact on ripple as long as the copper thickness can handle the current.
- The PCB traces act as an inductance equivalent to a hollow coil with an inductance value ranging from a few nH to a dozen nH.
- The DCR (DC resistance) of the traces only affects the efficiency of the DC/DC.
- Since the DC/DC tolerates inductance well, and the inductance itself usually has a tolerance of +/-20%, this inductive section has minimal impact on the DC/DC.

Disadvantages:

- L2 has no compensation, so the length and width of L2 need to be strictly controlled.

3.5.2.5 RK3576 CPU_BIG_DVDD Power Supply

CPU_BIG_DVDD adopts the distal feedback scheme as shown in the follow diagram (the distal feedback which PCB equivalent inductance is not used due to the satisfactory power supply ripple and limited space near the RK3576 position for capacitor placement).

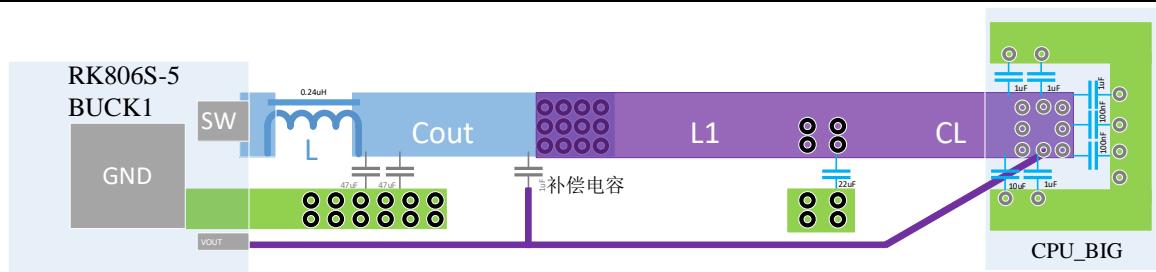


Figure 3-59 CPU_BIG PCB Layout schematic

The overall requirements are as follows:

- (1) There should be two 47uF capacitors at the DCDC output terminal, one 22uF capacitor near the RK3576, one 10uF capacitor, four 1uF capacitors, and two 100nF capacitors at the RK3576 pins.
- (2) The voltage feedback point should be taken from the RK3576 ball position, following the RK typical usage.
- (3) The CPU_BIG_DVDD power supply's copper coverage should strictly follow the PCB requirements provided below.
- (4) It is recommended to have a power supply DCR value below 13mohm.
- (5) The power supply PDN and recommended target impedance values are provided:

Table 3-10 Recommended PDN target impedance values for CPU_BIG_DVDD power supply

Frequency	Impedance (ohm)
100Khz~1Mhz	≤ 0.025
1Mhz ~30Mhz	≤ 0.035
30Mhz~100Mhz	≤ 0.11

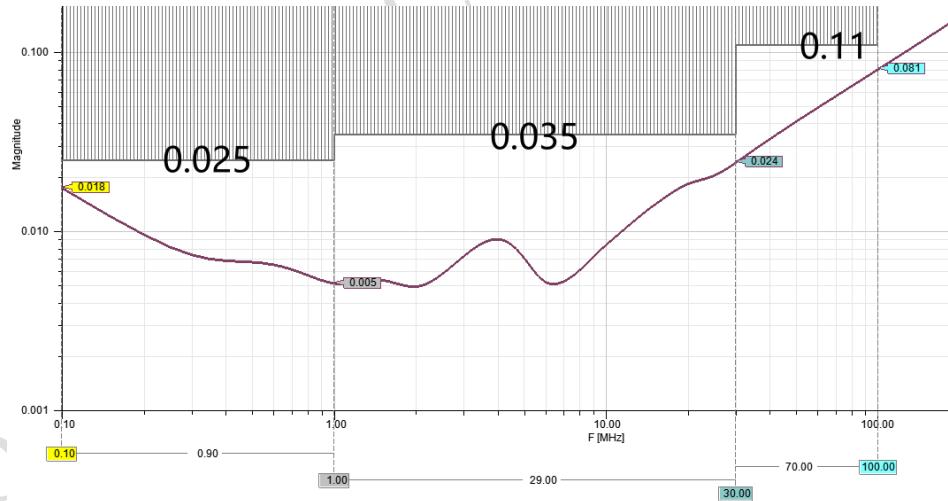


Figure 3-60 Recommended CPU_BIG_DVDD Power Supply PDN Requirements

Here are the recommendations for the PCB layout:

- (1) For the CPU_BIG_DVDD power supply pins beneath the RK3576 (SoC), it is suggested to have one corresponding power via for each ball (recommendation of 8 or more vias). The top layer should have a "#" patterned interconnection or be densely populated with traces to enhance current capability. It is recommended to use a trace width of 9 mil.

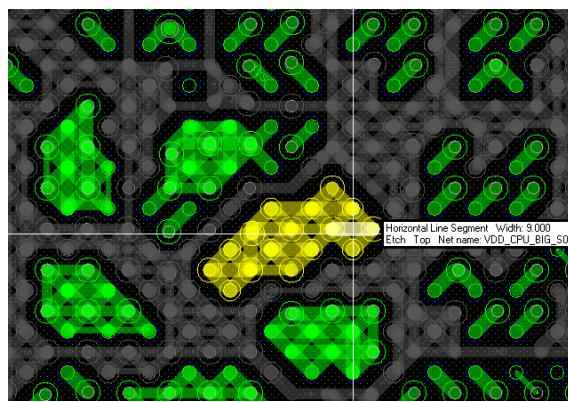


Figure 3-61 RK3576 chip CPU_BIG_DVDD power supply pin layout and vias

(2) In the CPU_BIG_DVDD area beneath the RK3576 (SoC), it is advisable to add ground return vias near the power vias, as long as they do not interfere with the power routing. It is recommended to have 8 or more such vias.

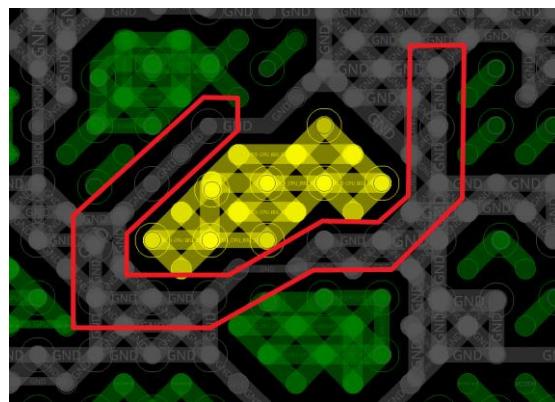


Figure 3-62 GND return vias for CPU_BIG_DVDD

(3) The decoupling capacitors near the CPU_BIG_DVDD power supply pins close to the RK3576 should be placed as close as possible to their corresponding power pins. The GND pad of the capacitors should be positioned near the GND ball of the RK3576. Other decoupling capacitors should also be placed as close as possible to the RK3576.



Figure 3-63 Decoupling capacitor on the back of the power supply pin of CPU_BIG_DVDD

(4) The width of the copper coverage for CPU_BIG_DVDD should meet the chip's current requirements. The copper coverage connected to the power chip's pins should be wide enough, without being excessively segmented by vias. Effective trace widths must be calculated to ensure that the paths connecting to each power pin of

CPU_BIG_DVDD are sufficient. The narrow area of CPU_BIG_DVDD beneath the RK3576 is recommended to have a copper width (W0) greater than 58 mils. Then, the copper width should be increased rapidly, and the outer region (W1) is suggested to be wider than 320 mils.



Figure 3-64 CPU_BIG_DVDD Power Layer Copper Cladding

(5) There should be at least one adjacent ground return plane for the power plane. The power plane helps reduce voltage drop, and the capacitance between the power plane and adjacent ground plane effectively reduces high-frequency Power Delivery Network (PDN) noise.

(6) It is recommended to use a copper thickness of 1oz for the power plane. If the layer count allows (e.g., for 8 or more layers), adding an extra power plane can help reduce current density.

(7) When transitioning layers for the CPU_BIG_DVDD power supply, it is advisable to have as many power vias as possible (10 or more 0503 vias) to minimize the voltage drop caused by layer transitions. The number of GND vias for decoupling capacitors should match the number of power vias; otherwise, the effectiveness of the capacitors will be greatly reduced.

3.5.2.6 RK3576 CPU_LIT_DVDD Power Supply

CPU_BIG_DVDD adopts the distal feedback scheme as shown in the follow diagram (the distal feedback which PCB equivalent inductance is not used due to the satisfactory power supply ripple and limited space near the RK3576 position for capacitor placement).

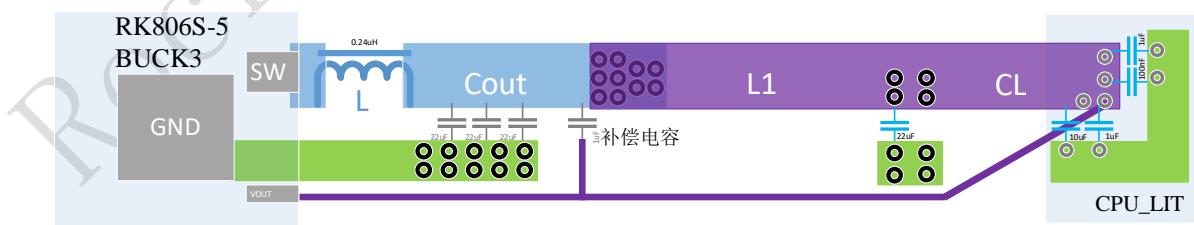


Figure 3-65 CPU_LIT PCB Layout schematic

The overall requirements are as follows:

- (1) There should be three 22uF capacitors at the DCDC output terminal, one 22uF capacitor near the RK3576, one 10uF capacitor, two 1uF capacitors, and one 100nF capacitors at the RK3576 pins.
- (2) The voltage feedback point should be taken from the RK3576 ball position, following the RK typical usage.
- (3) The CPU_LIT_DVDD power supply's copper coverage should strictly follow the PCB requirements

provided below.

(4) It is recommended to have a power supply DCR value below 20mohm.

(5) The power supply PDN and recommended target impedance values are provided:

Table 3-11 Recommended PDN target impedance values for CPU_LIT_DVDD power supply

Frequency	Impedance (ohm)
100Khz~1Mhz	≤ 0.035
1Mhz ~30Mhz	≤ 0.05
30Mhz~100Mhz	≤ 0.18

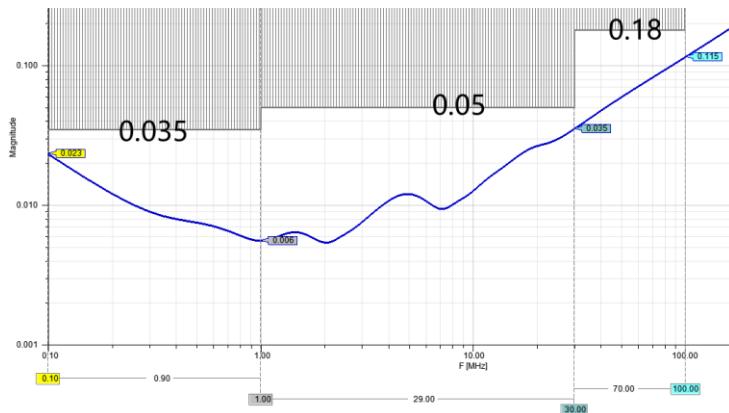


Figure 3-66 Recommended CPU_LIT_DVDD Power Supply PDN Requirements

Here are the recommendations for the PCB layout:

(1) For the CPU_LIT_DVDD power supply pins beneath the RK3576 (SoC), it is suggested to have one corresponding power via for each ball (recommendation of 4 or more vias). The top layer should have a "#" patterned interconnection or be densely populated with traces to enhance current capability. It is recommended to use a trace width of 9 mil.

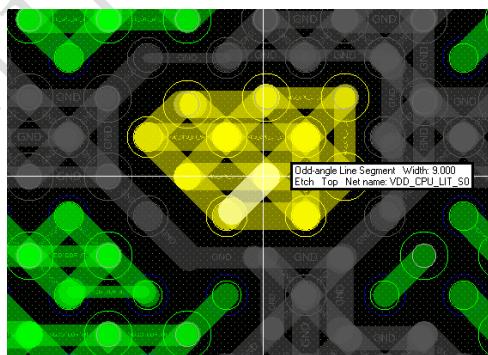


Figure 3-67 CPU_LIT_DVDD power supply pin layout and vias

(2) In the CPU_LIT_DVDD area beneath the RK3576 (SoC), it is advisable to add ground return vias near the power vias, as long as they do not interfere with the power routing. It is recommended to have 4 or more such vias.

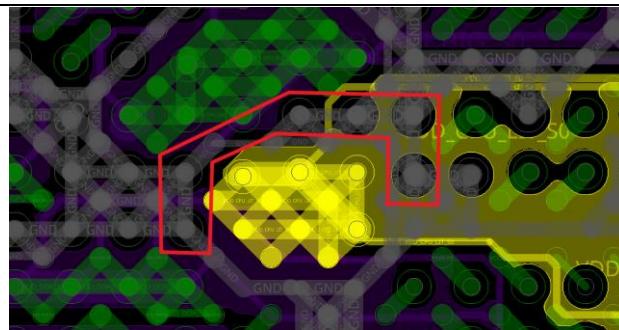


Figure 3-68 GND return vias for CPU_LIT_DVDD

(3) The decoupling capacitors near the CPU_LIT_DVDD power supply pins close to the RK3576 should be placed as close as possible to their corresponding power pins. The GND pad of the capacitors should be positioned near the GND ball of the RK3576. Other decoupling capacitors should also be placed as close as possible to the RK3576.



Figure 3-69 Decoupling capacitor on the back of the power supply pin of CPU_LIT_DVDD

(4) The width of the copper coverage for CPU_LIT_DVDD should meet the chip's current requirements. The copper coverage connected to the power chip's pins should be wide enough, without being excessively segmented by vias. Effective trace widths must be calculated to ensure that the paths connecting to each power pin of CPU_LIT_DVDD are sufficient. The narrow area of CPU_LIT_DVDD beneath the RK3576 is recommended to have a copper width (W_0) greater than 30 mils. Then, the copper width should be increased rapidly, and the outer region (W_1) is suggested to be wider than 200 mils.

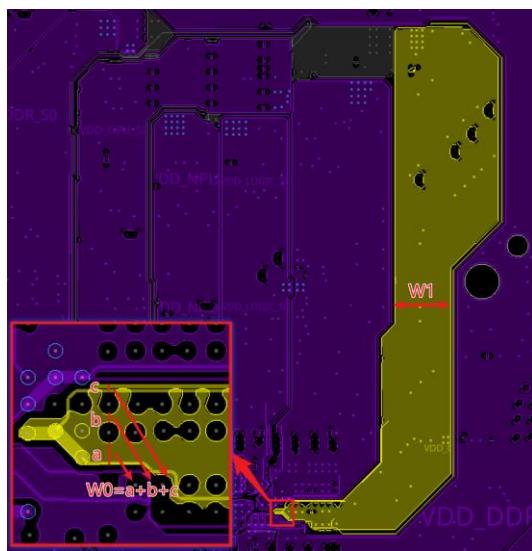


Figure 3-70 CPU_LIT_DVDD Power Layer Copper Cladding

(5) There should be at least one adjacent ground return plane for the power plane. The power plane helps reduce voltage drop, and the capacitance between the power plane and adjacent ground plane effectively reduces high-frequency Power Delivery Network (PDN) noise.

(6) It is recommended to use a copper thickness of 1oz for the power plane. If the layer count allows (e.g., for 8 or more layers), adding an extra power plane can help reduce current density.

(7) When transitioning layers for the CPU_LIT_DVDD power supply, it is advisable to have as many power vias as possible (6 or more 0503 vias) to minimize the voltage drop caused by layer transitions. The number of GND vias for decoupling capacitors should match the number of power vias; otherwise, the effectiveness of the capacitors will be greatly reduced.

3.5.2.7 RK3576 LOGIC Power Supply

RK3576 LOGIC adopts the distal feedback scheme as shown in the follow diagram (the distal feedback which PCB equivalent inductance is not used due to the satisfactory power supply ripple and limited space near the RK3576 position for capacitor placement).

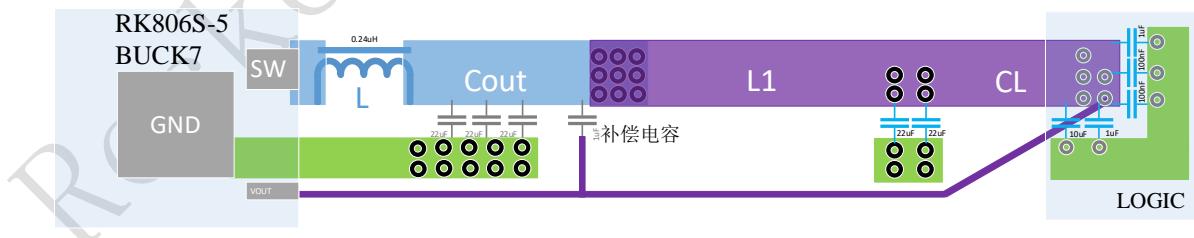


Figure 3-71 LOGIC PCB Layout schematic

The overall requirements are as follows:

- (1) There should be three 22uF capacitors at the DCDC output terminal,
- (2) for LOGIC_DVDD power supplu, two 22uF capacitor near the RK3576, one 10uF capacitor, two 1uF capacitors, and two 100nF capacitors at the RK3576 pins.
- (3) The voltage feedback point should be taken from the RK3576 ball position, following the RK typical usage.
- (4) The LOGIC power supply's copper coverage should strictly follow the PCB requirements provided below.

(5) It is recommended to have a power supply DCR value below 20mohm.

(6) The power supply PDN and recommended target impedance values are provided:

Table 3-12 Recommended PDN target impedance values for LOGIC_DVD power supply

Frequency	Impedance (ohm)
100Khz~1Mhz	≤ 0.03
1Mhz ~30Mhz	≤ 0.045
30Mhz~100Mhz	≤ 0.14

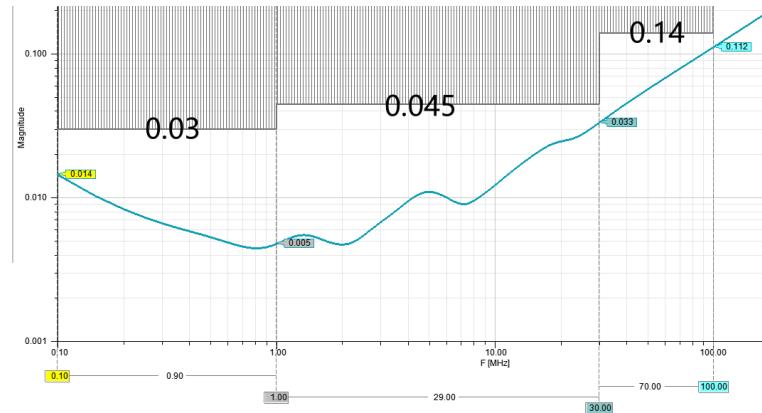


Figure 3-72 Recommended LOGIC_DVD Power Supply PDN Requirements

Here are the recommendations for the PCB layout:

(1) For the LOGIC_DVDD power supply pins beneath the RK3576 (SoC), it is suggested to have one corresponding power via for each ball (recommendation of 5 or more vias). The top layer should have a "#" patterned interconnection or be densely populated with traces to enhance current capability. It is recommended to use a trace width of 9 mil.



Figure 3-73 LOGIC_DVDD power supply pin layout and vias

(2) In the LOGIC_DVDD area beneath the RK3576 (SoC), it is advisable to add ground return vias near the power vias, as long as they do not interfere with the power routing. It is recommended to have 6 or more such vias.

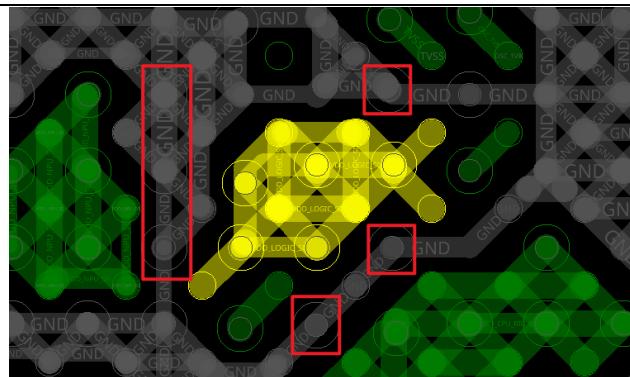


Figure 3-74 GND return vias for LOGIC_DVDD

(3) The decoupling capacitors near the LOGIC_DVDD power supply pins close to the RK3576 should be placed as close as possible to their corresponding power pins. The GND pad of the capacitors should be positioned near the GND ball of the RK3576. Other decoupling capacitors should also be placed as close as possible to the RK3576.



Figure 3-75 Decoupling capacitor on the back of the power supply pin of LOGIC_DVDD

(4) The width of the copper coverage for LOGIC_DVDD should meet the chip's current requirements. The copper coverage connected to the power chip's pins should be wide enough, without being excessively segmented by vias. Effective trace widths must be calculated to ensure that the paths connecting to each power pin of LOGIC_DVDD are sufficient. The narrow area of LOGIC_DVDD beneath the RK3576 is recommended to have a copper width (W_0) greater than 45 mils. Then, the copper width should be increased rapidly, and the outer region (W_1) is suggested to be wider than 200 mils.

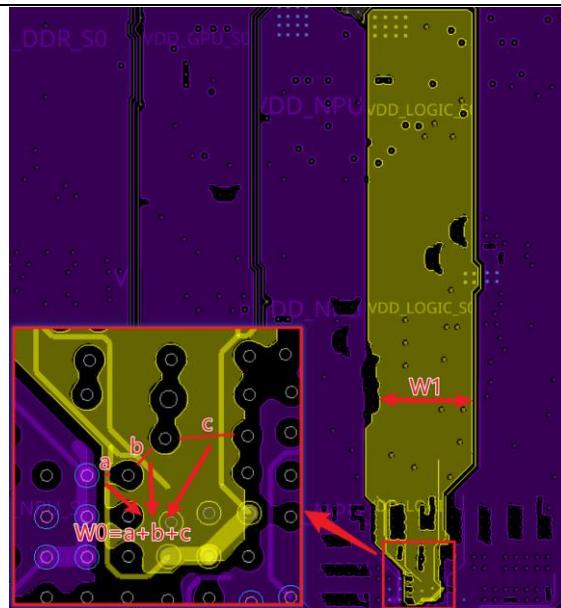


Figure 3-76 LOGIC_DVDD Power Layer Copper Cladding

(5) There should be at least one adjacent ground return plane for the power plane. The power plane helps reduce voltage drop, and the capacitance between the power plane and adjacent ground plane effectively reduces high-frequency Power Delivery Network (PDN) noise.

(6) It is recommended to use a copper thickness of 1oz for the power plane. If the layer count allows (e.g., for 8 or more layers), adding an extra power plane can help reduce current density.

(7) When transitioning layers for the LOGIC_DVDD power supply, it is advisable to have as many power vias as possible (6 or more 0503 vias) to minimize the voltage drop caused by layer transitions. The number of GND vias for decoupling capacitors should match the number of power vias; otherwise, the effectiveness of the capacitors will be greatly reduced.

3.5.2.8 RK3576 NPU_DVDD Power Supply

The NPU_DVDD power supply adopts the distal feedback scheme with PCB equivalence to an inductance, as shown in the diagram below:

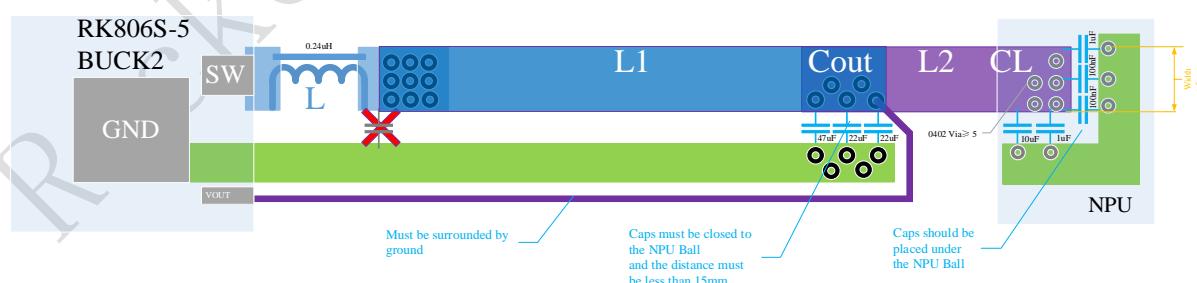


Figure 3-77 NPU PCB Layout schematic

The overall requirements are as follows:

(1) There are no capacitors at the DCDC output terminal. Near the RK3576, the main capacitor, Cout, consists of one 47uF capacitor and two 22uF capacitors. At the NPU_DVDD power supply pins of RK3576, there should be one 10uF capacitor, two 1uF capacitors, and two 100nF capacitors.

(2) The voltage feedback point is taken from the Cout capacitor location. The voltage feedback signal needs accompany with ground trace.

(3) At the Cout capacitor location near the RK3576 NPU_DVDD power supply pins, there should be five power vias and five ground vias.

(4) The distance L2 between the main capacitor and the NPU_DVDD power supply pins should not exceed 15mm. The power supply copper coverage should strictly follow the PCB requirements provided below.

(5) The distance between the main capacitor and the DCDC should not exceed 60mm.

(6) The power supply PDN (Power Delivery Network) and recommended target impedance values are provided in the table/diagram below.

Table 3-13 Recommended PDN target impedance values for NPU_DVDD power supply

Frequency	Impedance (ohm)
100Khz~1Mhz	≤ 0.03
1Mhz ~30Mhz	≤ 0.045
30Mhz~100Mhz	≤ 0.14

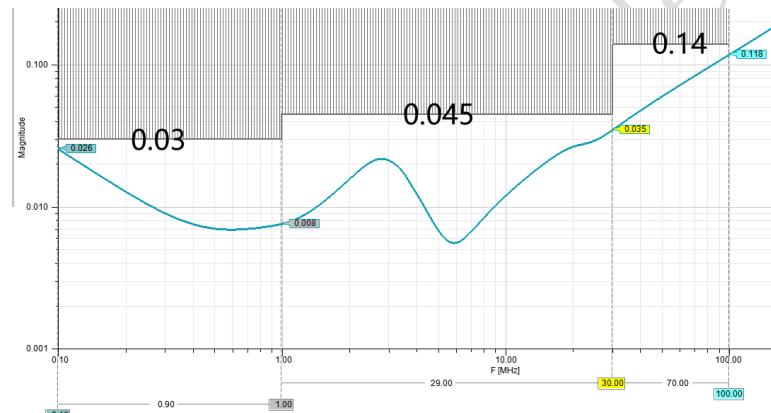


Figure 3-78 Recommended NPU_DVDD Power Supply PDN Requirements

Here are the recommendations for the PCB layout:

(1) For the NPU_DVDD power supply pins beneath the RK3576 (SoC), it is suggested to have one corresponding power via for each ball (recommendation of 5 or more vias). The top layer should have a "#" patterned interconnection or be densely populated with traces to enhance current capability. It is recommended to use a trace width of 9 mil.

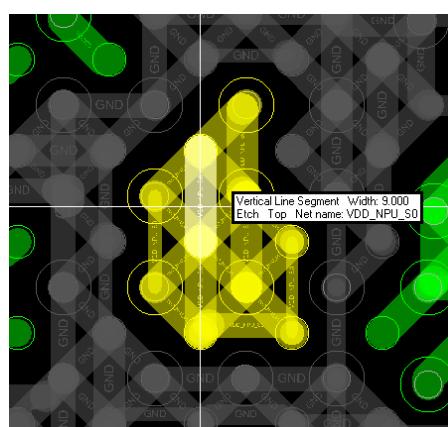


Figure 3-79 NPU_DVDD power supply pin layout and vias

(2) In the NPU_DVDD area beneath the RK3576 (SoC), it is advisable to add ground return vias near the power vias, as long as they do not interfere with the power routing. It is recommended to have 7 or more such vias.

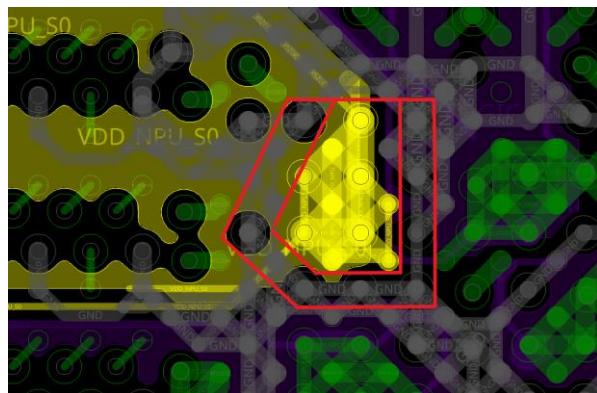


Figure 3-80 GND return vias for NPU_DVDD

(3) The decoupling capacitors near the NPU_DVDD power supply pins close to the RK3576 should be placed as close as possible to their corresponding power pins. The GND pad of the capacitors should be positioned near the GND ball of the RK3576. Other decoupling capacitors should also be placed as close as possible to the RK3576.

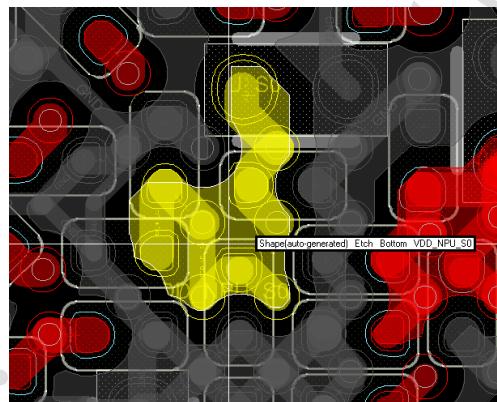


Figure 3-81 Decoupling capacitor on the back of the power supply pin of NPU_DVDD

(4) The main capacitor Cout needs to be placed as close as possible to the SoC, the feedback signal is taken from the main capacitor, the feedback line needs to be accompanied with the ground trace, and every 500 mils a ground via is needed to avoid being interfered.

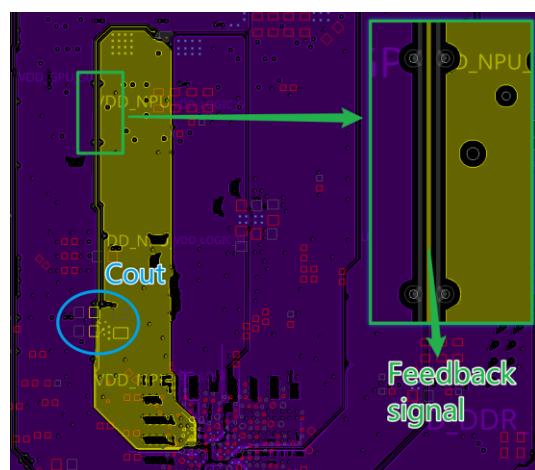


Figure 3-82 NPU_DVDD main capacitor and feedback line

(5) The width of the copper coverage for NPU_DVDD should meet the chip's current requirements. The copper coverage connected to the power chip's pins should be wide enough, without being excessively segmented by vias. Effective trace widths must be calculated to ensure that the paths connecting to each power pin of CPU_LIT_DVDD are sufficient. The narrow area of CPU_LIT_DVDD beneath the RK3576 is recommended to have a copper width (W0) greater than 60 mils. Then, the copper width should be increased rapidly, and the outer region (W1) is suggested to be wider than 220 mils.

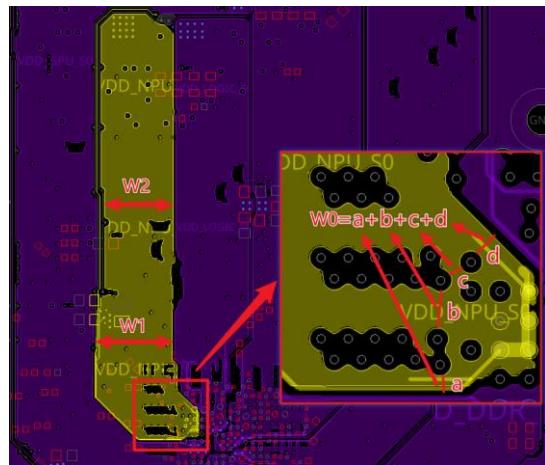


Figure 3-83 NPU_DVDD Power Layer Copper Cladding

(6) There should be at least one adjacent ground return plane for the power plane. The power plane helps reduce voltage drop, and the capacitance between the power plane and adjacent ground plane effectively reduces high-frequency Power Delivery Network (PDN) noise.

(7) It is recommended to use a copper thickness of 1oz for the power plane. If the layer count allows (e.g., for 8 or more layers), adding an extra power plane can help reduce current density.

(8) When transitioning layers for the NPU_DVDD power supply, it is advisable to have as many power vias as possible (8 or more 0503 vias) to minimize the voltage drop caused by layer transitions. The number of GND vias for decoupling capacitors should match the number of power vias; otherwise, the effectiveness of the capacitors will be greatly reduced.

3.5.2.9 RK3576 GPU_DVDD Power Supply

The GPU_DVDD power supply adopts the distal feedback scheme with PCB equivalence to an inductance, as shown in the diagram below:

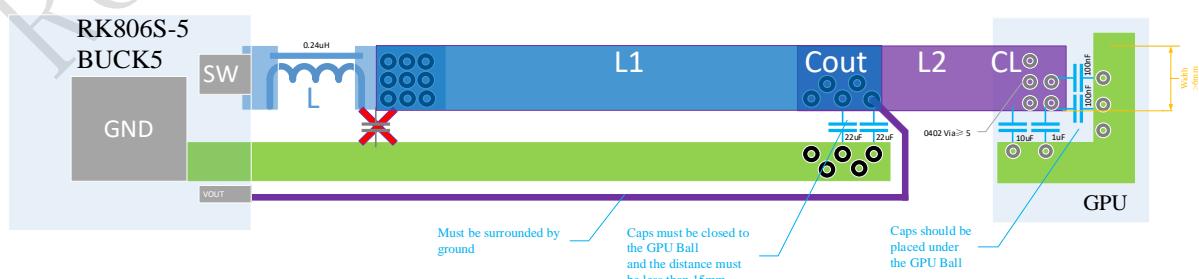


Figure 3-84 GPU PCB Layout schematic

The overall requirements are as follows:

(1) There are no capacitors at the DCDC output terminal. Near the RK3576, the main capacitor, Cout, consists of three 22uF capacitor. At the GPU_DVDD power supply pins of RK3576, there should be one 10uF capacitor, two 1uF capacitors, and one 100nF capacitors.

(2) The voltage feedback point is taken from the Cout capacitor location. The voltage feedback signal needs accompany with ground trace.

(3) At the Cout capacitor location near the RK3576 GPU _DVDD power supply pins, there should be five power vias and five ground vias.

(4) The distance L2 between the main capacitor and the GPU_DVDD power supply pins should not exceed 15mm. The power supply copper coverage should strictly follow the PCB requirements provided below.

(5) The distance between the main capacitor and the DCDC should not exceed 60mm.

(6) The power supply PDN (Power Delivery Network) and recommended target impedance values are provided in the table/diagram below.

Table 3-14 Recommended PDN target impedance values for GPU_DVDD power supply

Frequency	Impedance (ohm)
100Khz~1Mhz	≤ 0.035
1Mhz ~30Mhz	≤ 0.05
30Mhz~100Mhz	≤ 0.14

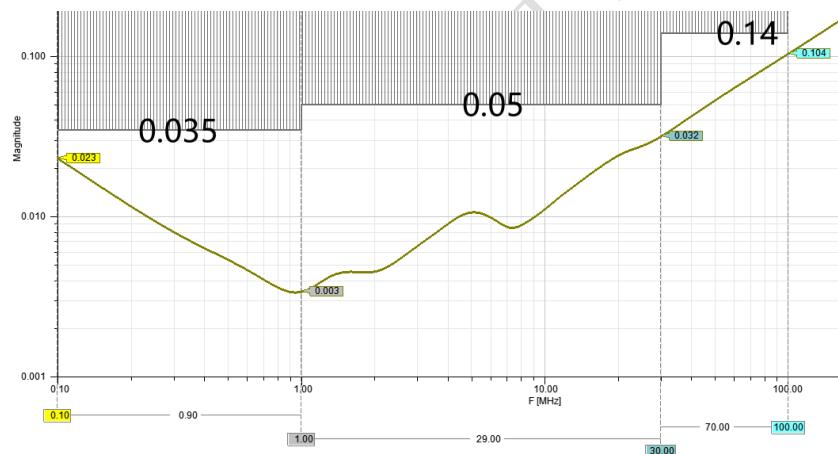


Figure 3-85 Recommended GPU_DVDD Power Supply PDN Requirements

Here are the recommendations for the PCB layout:

(1) For the GPU_DVDD power supply pins beneath the RK3576 (SoC), it is suggested to have one corresponding power via for each ball (recommendation of 5 or more vias). The top layer should have a "#" patterned interconnection or be densely populated with traces to enhance current capability. It is recommended to use a trace width of 9 mil.

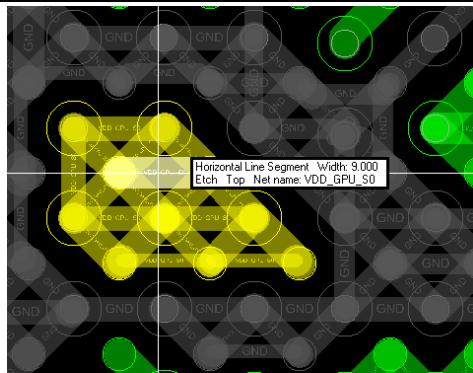


Figure 3-86 GPU_DVDD power supply pin layout and vias

(2) In the GPU_DVDD area beneath the RK3576 (SoC), it is advisable to add ground return vias near the power vias, as long as they do not interfere with the power routing. It is recommended to have 8 or more such vias.

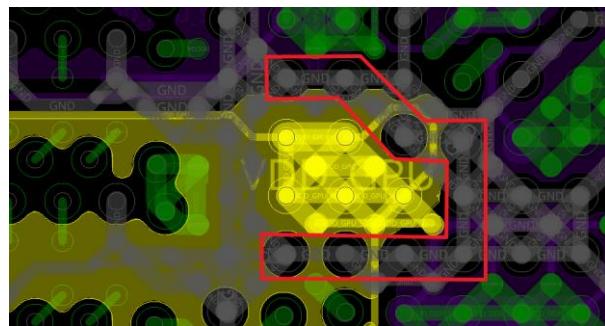


Figure 3-87 GND return vias for GPU_DVDD

(3) The decoupling capacitors near the GPU_DVDD power supply pins close to the RK3576 should be placed as close as possible to their corresponding power pins. The GND pad of the capacitors should be positioned near the GND ball of the RK3576. Other decoupling capacitors should also be placed as close as possible to the RK3576.

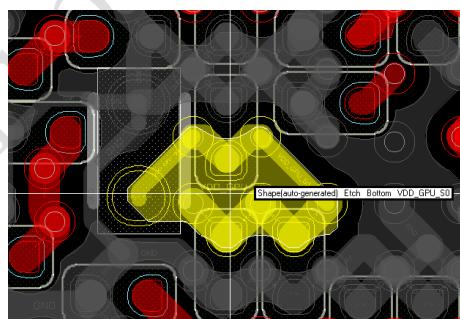


Figure 3-88 Decoupling capacitor on the back of the power supply pin of GPU_DVDD

(4) The main capacitor Cout needs to be placed as close as possible to the SoC, the feedback signal is taken from the main capacitor, the feedback line needs to be accompanied with the ground trace, and every 500 mils a ground via is needed to avoid being interfered.

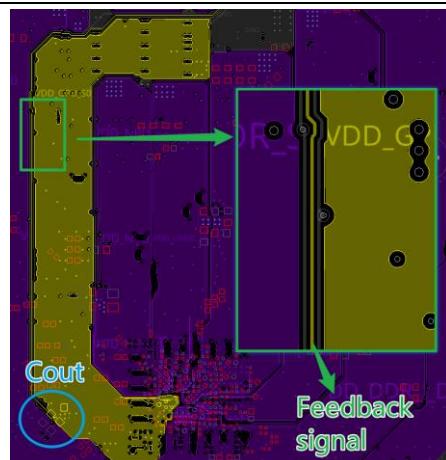


Figure 3-89 GPU_DVDD main capacitor and feedback line

(4) The width of the copper coverage for GPU_DVDD should meet the chip's current requirements. The copper coverage connected to the power chip's pins should be wide enough, without being excessively segmented by vias. Effective trace widths must be calculated to ensure that the paths connecting to each power pin of GPU_DVDD are sufficient. The narrow area of GPU_DVDD beneath the RK3576 is recommended to have a copper width (W0) greater than 60 mils. Then, the copper width should be increased rapidly, and the outer region (W1 and W2) is suggested to be wider than 250 mils.

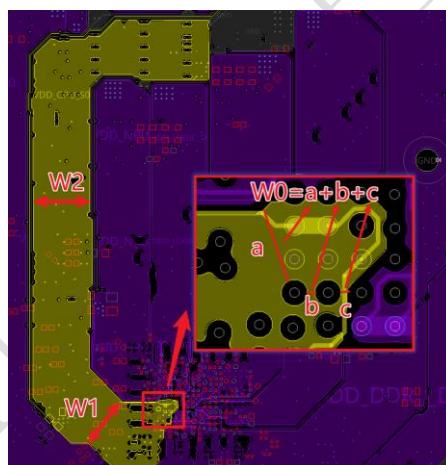


Figure 3-90 GPU_DVDD Power Layer Copper Cladding

(5) There should be at least one adjacent ground return plane for the power plane. The power plane helps reduce voltage drop, and the capacitance between the power plane and adjacent ground plane effectively reduces high-frequency Power Delivery Network (PDN) noise.

(6) It is recommended to use a copper thickness of 1oz for the power plane. If the layer count allows (e.g., for 8 or more layers), adding an extra power plane can help reduce current density.

(7) When transitioning layers for the GPU_DVDD power supply, it is advisable to have as many power vias as possible (6 or more 0503 vias) to minimize the voltage drop caused by layer transitions. The number of GND vias for decoupling capacitors should match the number of power vias; otherwise, the effectiveness of the capacitors will be greatly reduced.

3.5.2.10 RK3576 DDRPHY_DVDD Power Supply

DDRPHY_DVDD adopts the distal feedback scheme as shown in the follow diagram (the distal feedback which PCB equivalent inductance is not used due to the satisfactory power supply ripple and limited space near the RK3576 position for capacitor placement).

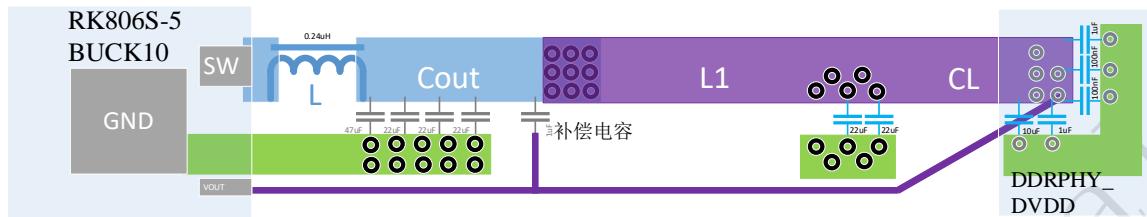


Figure 3-91 DDRPHY_DVDD PCB Layout schematic

The overall requirements are as follows:

- (1) There should be two 22uF capacitors at the DCDC output terminal, two 22uF capacitor near the RK3576, one 10uF capacitor, two 1uF capacitors, and one 100nF capacitors at the RK3576 pins.
- (2) The voltage feedback point should be taken from the RK3576 ball position, following the RK typical usage.
- (3) The DDRPHY_DVDD power supply's copper coverage should strictly follow the PCB requirements provided below.
- (4) It is recommended to have a power supply DCR value below 25mohm.
- (5) The power supply PDN and recommended target impedance values are provided:

Table 3-15 Recommended PDN target impedance values for DDRPHY_DVDD power supply

Frequency	Impedance (ohm)
100Khz~1Mhz	≤ 0.035
1Mhz ~30Mhz	≤ 0.045
30Mhz~100Mhz	≤ 0.15

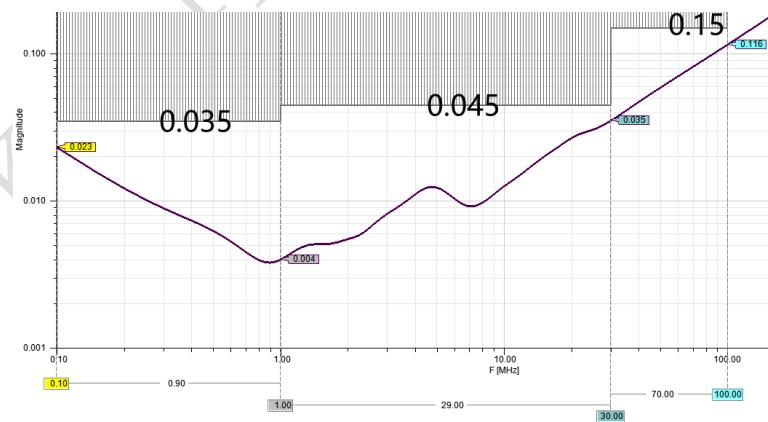


Figure 3-92 Recommended DDRPHY_DVDD Power Supply PDN Requirements

Here are the recommendations for the PCB layout:

- (1) For the DDRPHY_DVDD power supply pins beneath the RK3576 (SoC), it is suggested to have one corresponding power via for each ball (recommendation of 4 or more vias). The top layer should have a "#" patterned interconnection or be densely populated with traces to enhance current capability. It is recommended to use a trace width of 9 mil.



Figure 3-93 DDRPHY_DVDD power supply pin layout and vias

(2) In the DDRPHY_DVDD area beneath the RK3576 (SoC), it is advisable to add ground return vias near the power vias, as long as they do not interfere with the power routing. It is recommended to have 4 or more such vias.

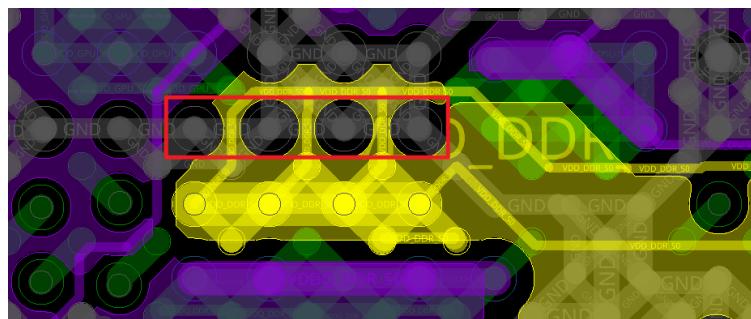


Figure 3-94 GND return vias for DDRPHY_DVDD

(3) The decoupling capacitors near the DDRPHY_DVDD power supply pins close to the RK3576 should be placed as close as possible to their corresponding power pins. The GND pad of the capacitors should be positioned near the GND ball of the RK3576. Other decoupling capacitors should also be placed as close as possible to the RK3576.



Figure 3-95 Decoupling capacitor on the back of the power supply pin of DDRPHY_DVDD

(4) The width of the copper coverage for DDRPHY_DVDD should meet the chip's current requirements. The copper coverage connected to the power chip's pins should be wide enough, without being excessively segmented by vias. Effective trace widths must be calculated to ensure that the paths connecting to each power pin of DDRPHY_DVDD are sufficient. The narrow area of DDRPHY_DVDD beneath the RK3576 is recommended to have a copper width (W0) greater than 45 mils. Then, the copper width should be increased rapidly, and the outer region (W1) is suggested to be wider than 200 mils.

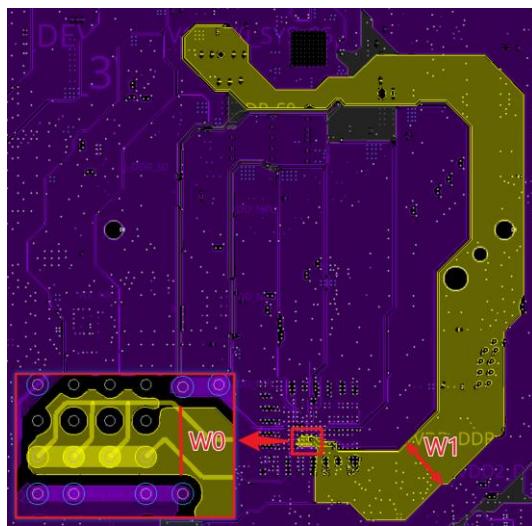


Figure 3-96 CPU_BIG_DVDD Power Layer Copper Cladding

(5) There should be at least one adjacent ground return plane for the power plane. The power plane helps reduce voltage drop, and the capacitance between the power plane and adjacent ground plane effectively reduces high-frequency Power Delivery Network (PDN) noise.

(6) It is recommended to use a copper thickness of 1oz for the power plane. If the layer count allows (e.g., for 8 or more layers), adding an extra power plane can help reduce current density.

(7) When transitioning layers for the DDRPHY_DVDD power supply, it is advisable to have as many power vias as possible (6 or more 0503 vias) to minimize the voltage drop caused by layer transitions. The number of GND vias for decoupling capacitors should match the number of power vias; otherwise, the effectiveness of the capacitors will be greatly reduced.

3.5.2.11 RK3576 DDRPHY_VDDQ Power Supply

DDRPHY_VDDQ uses the proximal Feedback scheme shown below

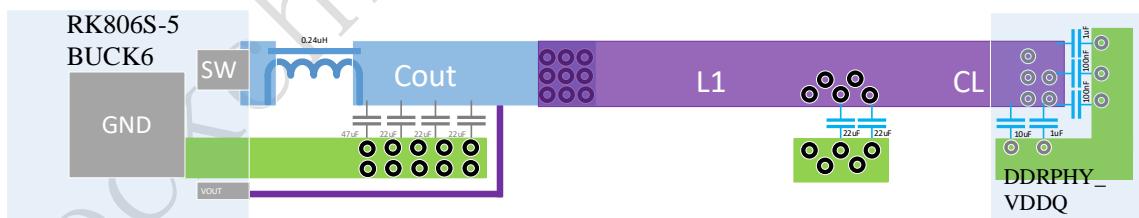


Figure 3-97 DDRPHY_VDDQ PCB Layout schematic

The overall requirements are as follows:

- (1) There should be two 22uF capacitors at the DCDC output terminal, two 22uF capacitor near the RK3576, one 10uF capacitor, two 1uF capacitors, and one 100nF capacitors at the RK3576 pins.
- (2) The voltage feedback point should be taken from the RK3576 ball position.
- (3) The DDRPHY_VDDQ power supply's copper coverage should strictly follow the PCB requirements provided below.
- (4) It is recommended to have a power supply DCR value below 25mohm.
- (5) The power supply PDN and recommended target impedance values are provided:

Table 3-16 Recommended PDN target impedance values for DDRPHY_VDDQ power supply

Frequency	Impedance (ohm)
100Khz~1Mhz	≤ 0.03
1Mhz ~30Mhz	≤ 0.045
30Mhz~100Mhz	≤ 0.15

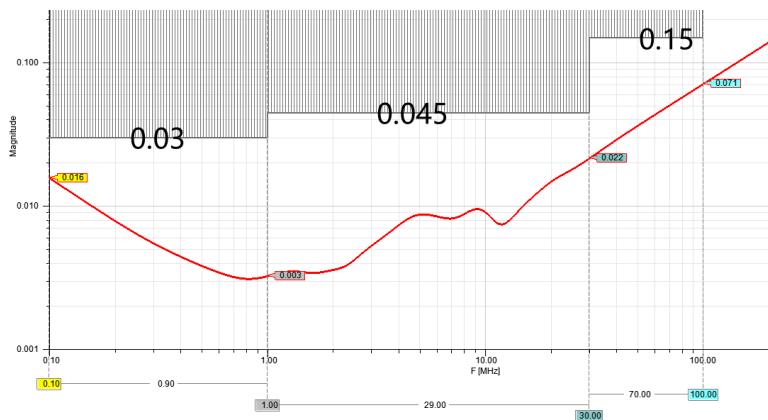


Figure 3-98 Recommended DDRPHY_VDDQ Power Supply PDN Requirements

Here are the recommendations for the PCB layout:

- (1) For the DDRPHY_VDDQ power supply pins beneath the RK3576 (SoC), it is suggested to have one corresponding power via for each ball (recommendation of 4 or more vias). The top layer should have a "#" patterned interconnection or be densely populated with traces to enhance current capability. It is recommended to use a trace width of 9 mil.

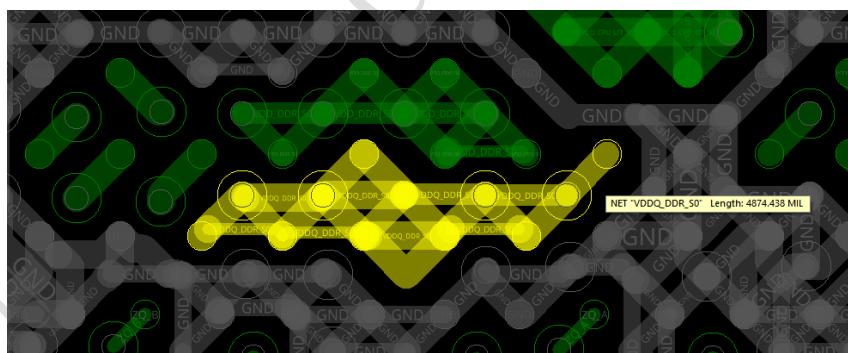


Figure 3-99 DDRPHY_VDDQ power supply pin layout and vias

- (2) In the DDRPHY_VDDQ area beneath the RK3576 (SoC), it is advisable to add ground return vias near the power vias, as long as they do not interfere with the power routing. It is recommended to have 4 or more such vias.



Figure 3-100 GND return vias for DDRPHY_VDDQ

(3) The decoupling capacitors near the DDRPHY_VDDQ power supply pins close to the RK3576 should be placed as close as possible to their corresponding power pins. The GND pad of the capacitors should be positioned near the GND ball of the RK3576. Other decoupling capacitors should also be placed as close as possible to the RK3576.

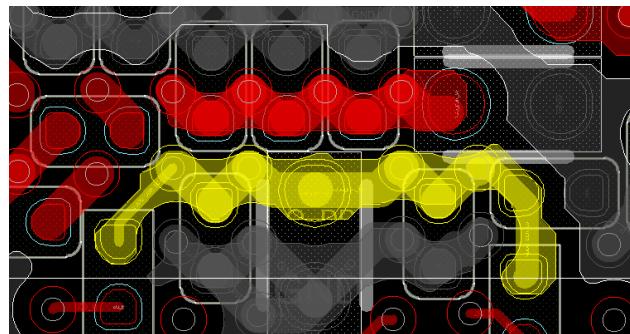


Figure 3-101 Decoupling capacitor on the back of the power supply pin of DDRPHY_VDDQ

(4) The width of the copper coverage for DDRPHY_VDDQ should meet the chip's current requirements. The copper coverage connected to the power chip's pins should be wide enough, without being excessively segmented by vias. Effective trace widths must be calculated to ensure that the paths connecting to each power pin of DDRPHY_VDDQ are sufficient. The narrow area of DDRPHY_VDDQ beneath the RK3576 is recommended to have a copper width (W_0) greater than 50 mils. Then, the copper width should be increased rapidly, and the outer region (W_1) is suggested to be wider than 200 mils.

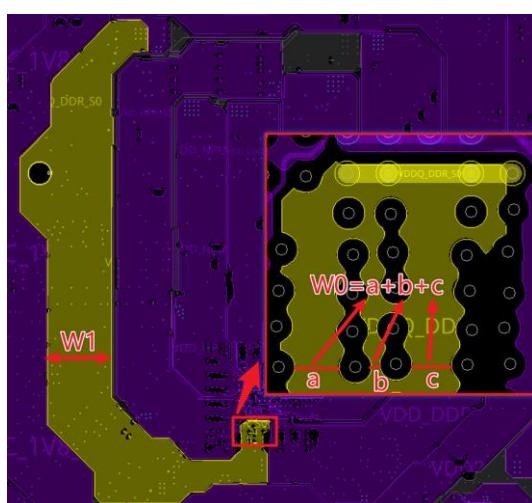


Figure 3-102 DDRPHY_VDDQ Power Layer Copper Cladding

(5) There should be at least one adjacent ground return plane for the power plane. The power plane helps reduce voltage drop, and the capacitance between the power plane and adjacent ground plane effectively reduces high-frequency Power Delivery Network (PDN) noise.

(6) It is recommended to use a copper thickness of 1oz for the power plane. If the layer count allows (e.g., for 8 or more layers), adding an extra power plane can help reduce current density.

(7) When transitioning layers for the DDRPHY_VDDQ power supply, it is advisable to have as many power vias as possible (6 or more 0503 vias) to minimize the voltage drop caused by layer transitions. The number of GND vias for decoupling capacitors should match the number of power vias; otherwise, the effectiveness of the capacitors will be greatly reduced.

3.5.2.12 RK3576 Other Power Supplies

For other power supplies beneath the RK3576 (SoC), it is recommended to have one corresponding power via for each ball, if possible. Additionally, near the power vias and without affecting the power routing, it is advisable to add GND return vias. It is preferable to have a complete GND return plane on the adjacent layer of the power traces.

The decoupling capacitors for the other power supplies of the RK3576 should be placed close to the chip's pins. When using double-sided placement, the capacitors should be placed on the backside of the chip's pins. Ideally, the routing should pass through the capacitor pads before reaching the chip's pins. Each capacitor's GND pad should correspond to a dedicated GND via.



Figure 3-103 RK3576 other power supply pin layout and vias

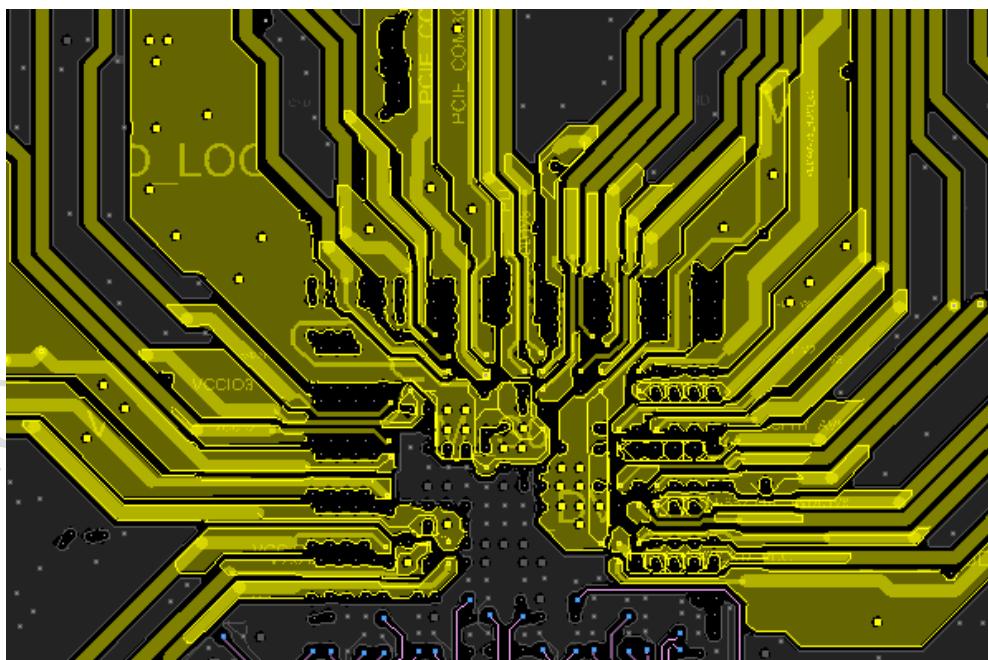


Figure 3-104 RK3576 Other Power Supplies inner Fan-out

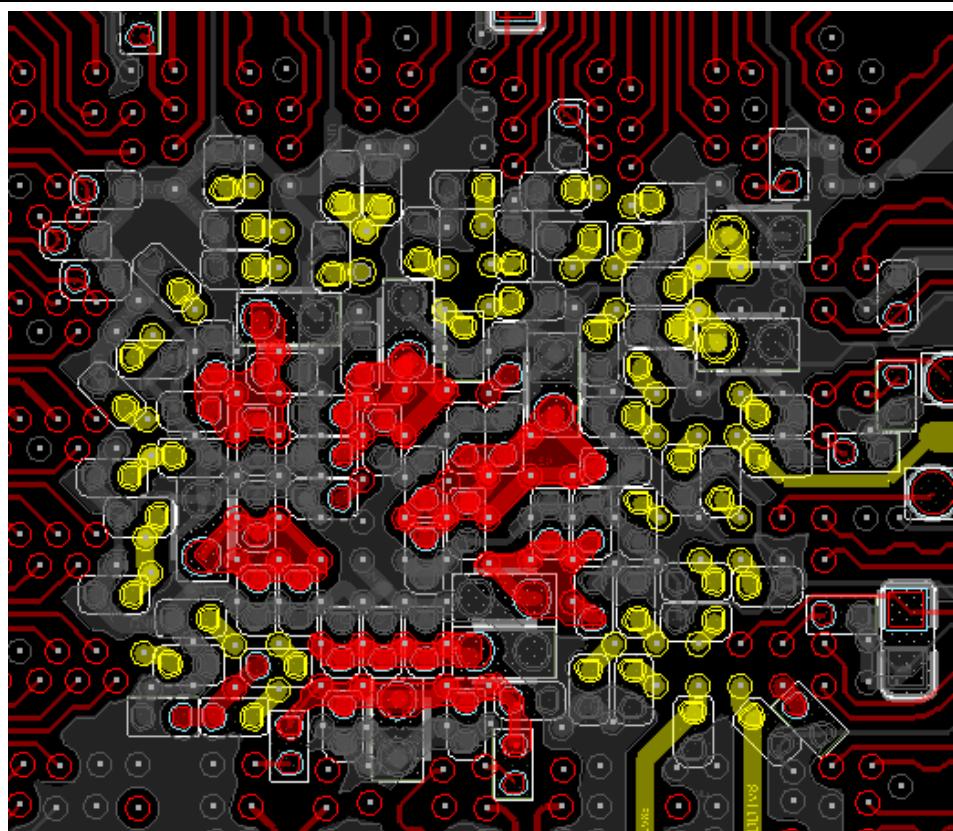


Figure 3-105 Decoupling capacitor on the back of the power supply pin of RK3576 Other Power Supplies

3.5.2.13 RK3576 VSS Pins

It is recommended to have as many GND return vias as possible for the VSS pins of the RK3576 (SoC) chip, without affecting the power plane. On the top layer, it is suggested to create a "#" pattern or densely populate traces in a crisscross manner. The recommended trace width is 9 mil.

The adjacent layers of the RK3576 (SoC) chip must form a complete GND plane, ensuring that the main reference ground is located near the CPU's ball. The ground vias should connect all VSS pins of the RK3576 and the entire ground plane. This ensures power integrity, provides better Signal Integrity (SI) and Power Integrity (PI) conditions, and enhances PCB heat dissipation.

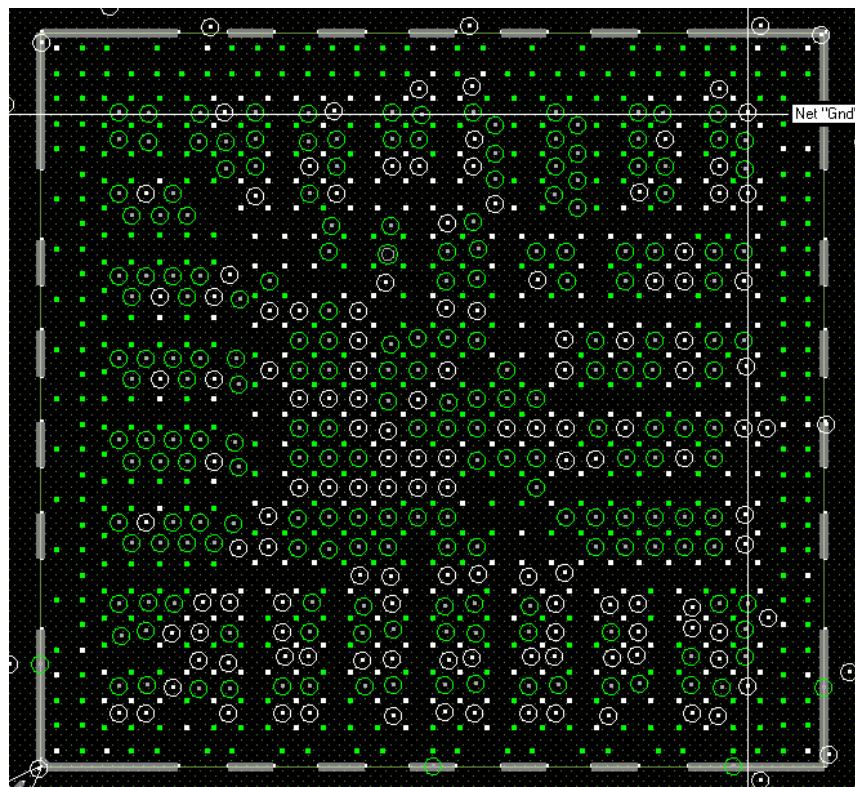


Figure 3-106 Distribution of BGA area vias and pads for RK3576

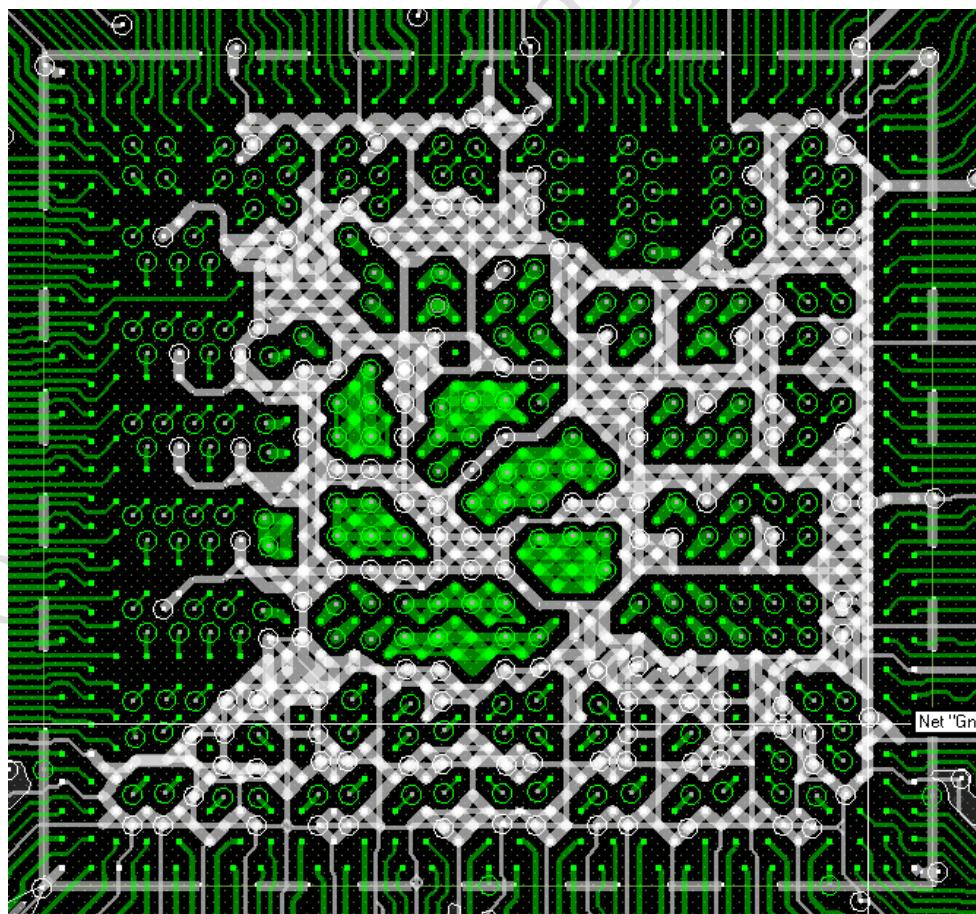


Figure 3-107 Routing and vias for RK3576 VSS pins

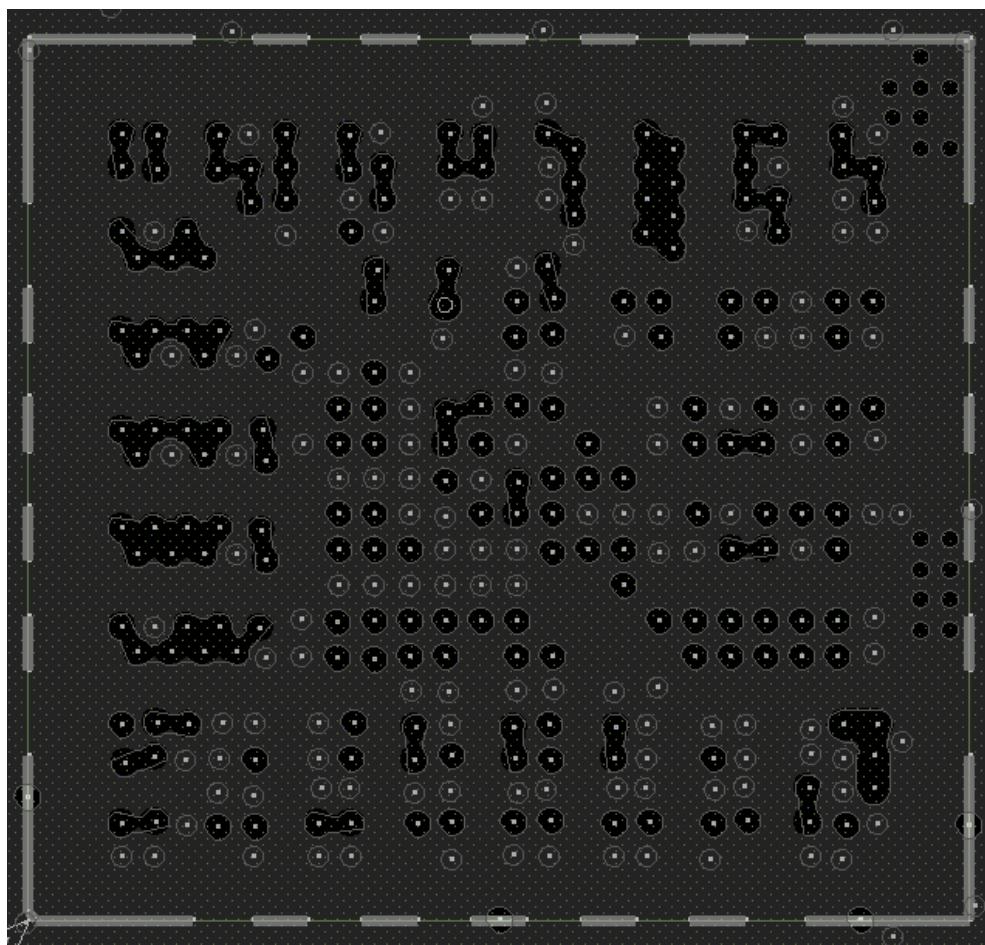


Figure 3-108 Copper coverage of the ground plane for RK3576

3.5.3 DDR interface PCB Design

As RK3576 DDR interface operates up to 4266Mbps, the PCB design is difficult, so it is strongly recommended to use the DDR template and corresponding DDR firmware provided by RK. DDR templates are released after rigorous simulation and verification. If you do not use DDR templates and design PCB by yourself, please refer to the following PCB design suggestions, then perform simulation.

(1) The CPU GND pads should have enough vias, it is recommended to strictly refer to the template design. The GND vias cannot be deleted. The 6-layer PTH PCB template design is as shown in the figure below.

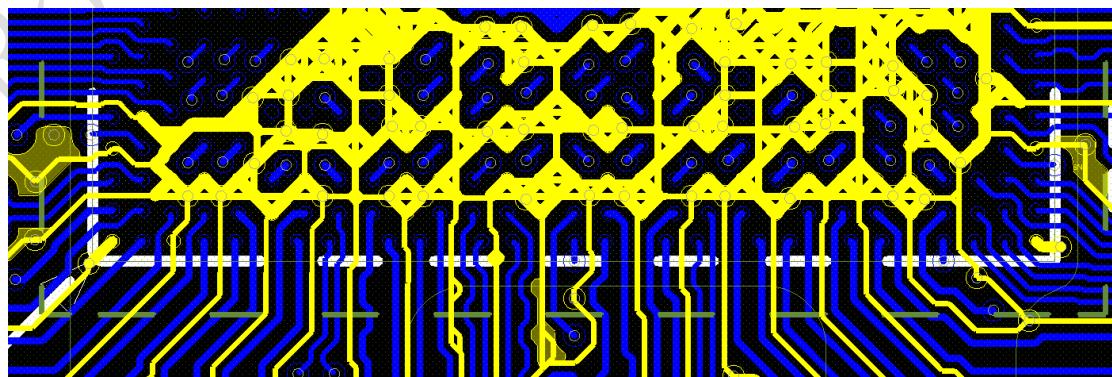


Figure 3-109 vias design of 6-layer PTH PCB template SOC area

(2) If a signal trace changes layer and the reference plane is GND, stitching GND vias should be added close to the layer change vias within 25 mils. One Signal via should have \geq one GND via. Increase GND via as much as you can.

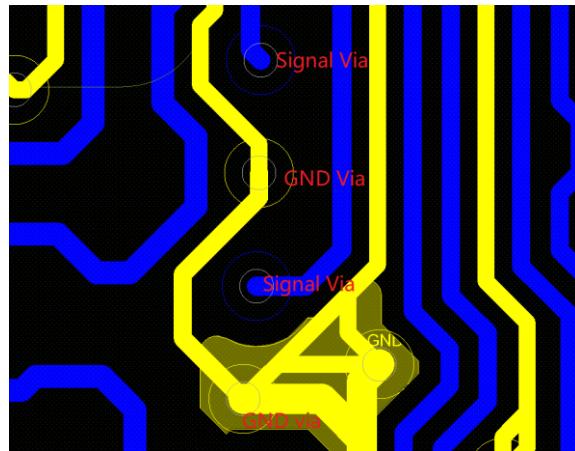


Figure 3-110 Schematic of the GND via corresponding to the signal via

(3) GND vias recommend to be placed between signal vias. Four signal vias together is not recommended. Use GND vias to separate signal vias as shown in the figure below, will improve performance.

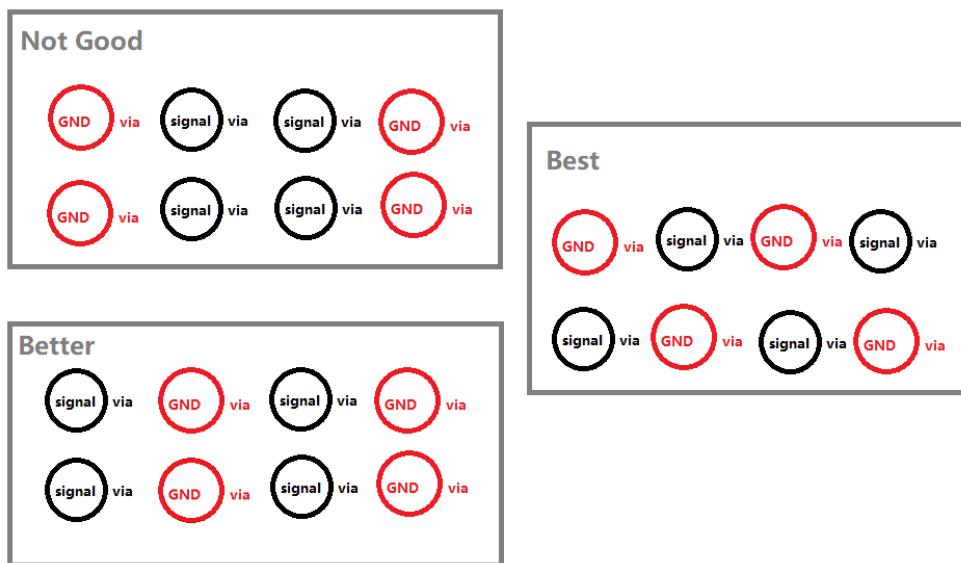


Figure 3-111 Schematic of different via design

(4) For a 6-layer board, it is recommended to route DDR signals on the first layer, fourth layer, and sixth layer. The signals DQ, DQS, address and control signals, and CLK signal should have at least one complete GND reference plane. For an 8-layer board, it is suggested to route DDR signals on the first layer, sixth layer, and eighth layer. Similarly, DQ, DQS, address and control signals, and CLK signal should have at least one complete GND reference plane. When signals are referencing both the GND plane and the power plane, it is advisable to place the signals closer to the GND plane to ensure that most of the return currents flow through the GND plane.

(5) Avoid return path discontinuities such as a slit, you can optimize the reference layer with GND traces.

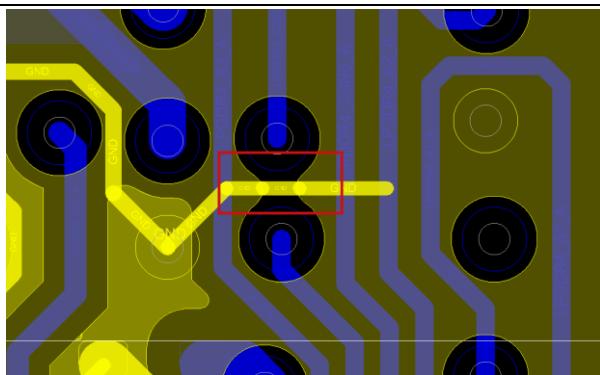


Figure 3-112 GND traces optimization the reference layer

(6) The recommended distance between the trace and the edge of the reference layer is ≥ 12 mil.



Figure 3-113 the distance between the trace and the edge of the reference layer

(7) An adequate spacing should be maintained between the inside traces of a bend. Recommend 3times the trace width or greater($S \geq 3W$).

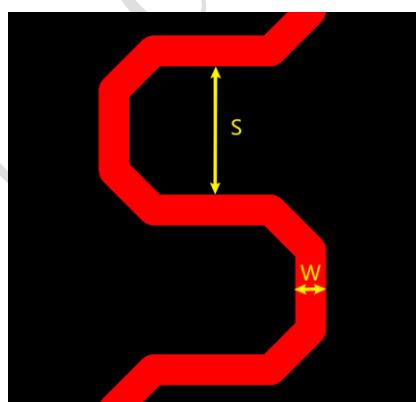


Figure 3-114 adequate spacing

(8) The propagation delay associated with vias should be accounted for in the trace length.

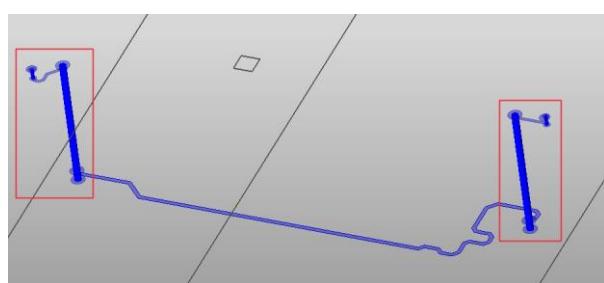


Figure 3-115 Schematic of vias length

(9) One via per GND pad of Dram chip. Add GND vias as much as you can.

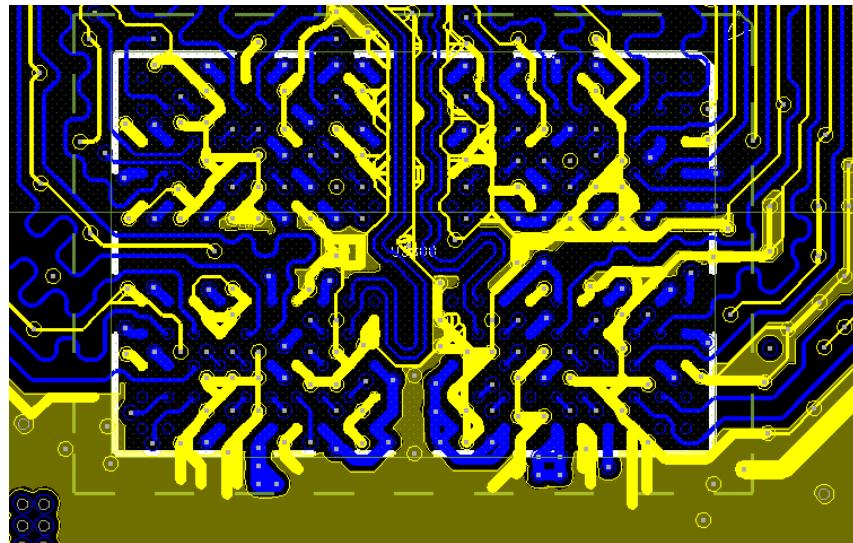


Figure 3-116 Schematic of the number of GND vias

(11) Remove unused via pads, because they cause unwanted capacitance and destroy plane.

(12) The closer the trace is to the via, the worse the reference plane is. Recommend route trace far away ($\geq 8\text{mil}$) from the via pad.

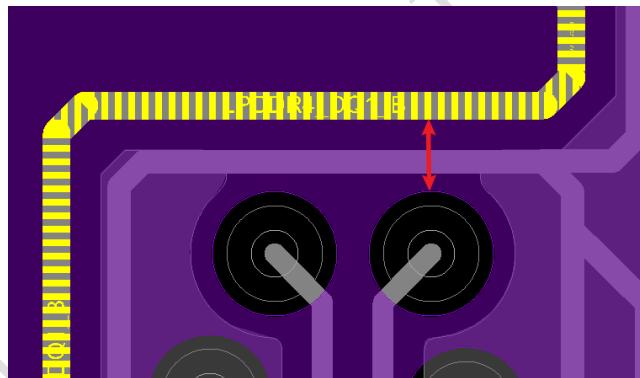


Figure 3-117 Recommended spacing for traces and via pads

(13) Avoid making slits of plane due to the via clearance as possible.

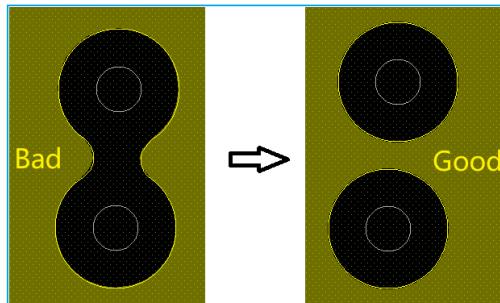


Figure 3-118 Schematic of route optimization plane slits

(13) DQS, CLK, WCLK signal should use ground shielding for the entire trace including vias. Recommend ground shielding line $\geq 400\text{mil}$, add one GND via.

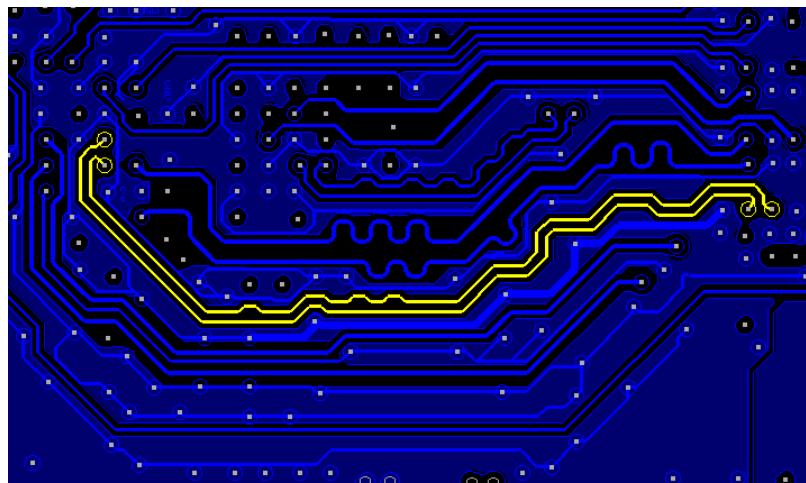


Figure 3-119 Schematic of ground shielding design

(14) For signals on inner layers, it is recommended to have one layer be referencing GND plane and another layer be referencing power plane. It is suggested to implement a paired ground shielding design for DQ signals, which can help improve signal quality. It is advisable to add a GND via every ≤ 400 mil along the paired grounding traces. Additionally, for signal via transitions between layers within a range of 25 mil (center-to-center distance of vias), it is recommended to include GND return vias.

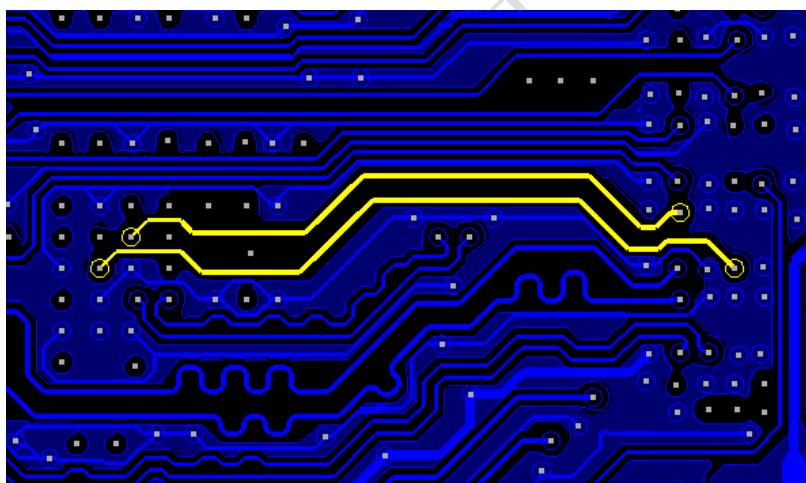


Figure 3-120 Schematic of ground shielding design

(15) For VDD2_DDR_S3, VDD2H_DDR_S3, VDD2L_0V9_DDR_S3power, recommend ≥ 6 vias (0503 via) when power layer is changed at DCDC output.

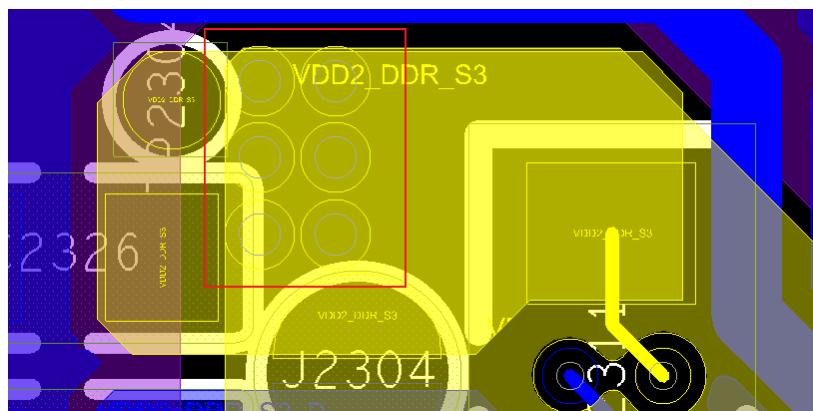


Figure 3-121 the vias requirement when power layer changed

(16) For VDDQ_DDR_S0, VDDQ_DRAM_S0, VDD2_DDR_S3 power, recommend ≥ 6 vias (0402 or 0503 via) when power layer is changed at DCDC output.

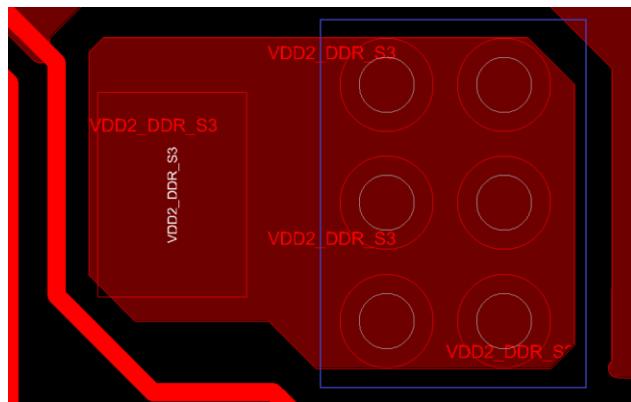


Figure 3-122 the vias requirement when VDD2_DDR_S3 power layer changed

(17) For VDD1_1V8_DDR power supply, it is recommended ≥ 2 vias(0503 via) when the power plane is changed.

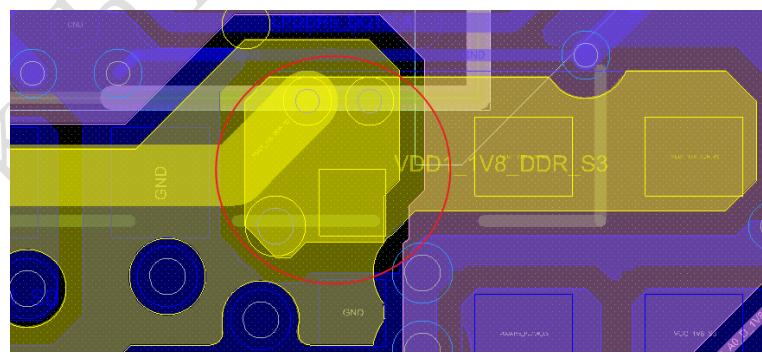


Figure 3-123 the vias requirement when VDD1_1V8_DDR power layer changed

(18) For LPDDR4/4X, VDDQ_DRAM_S0, VDD2_DDR_S3, VDD1_1V8_DDR power supply, it is recommended that one pin corresponds to one power via, for example as follows.

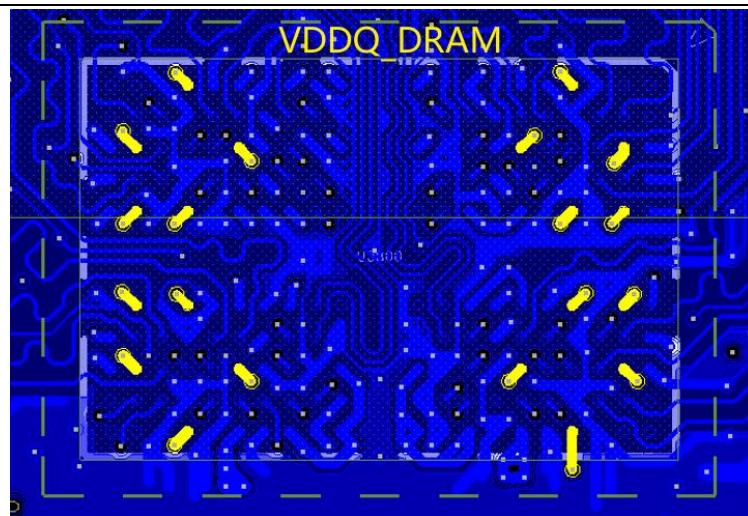


Figure 3-124 Requirements for the number of vias corresponding to the LPDDR4/4X chip VDDQ_DRAM_S0 power pins

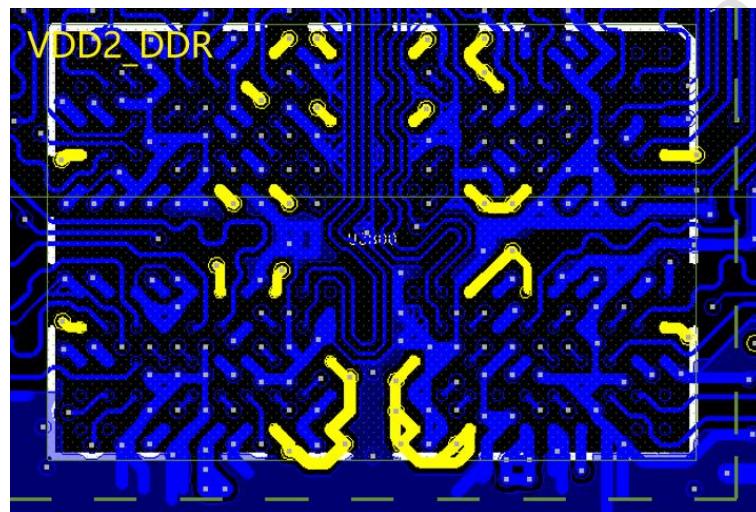


Figure 3-125 Requirements for the number of vias corresponding to the LPDDR4/4X chip VDD2_DDR_S3 power pins

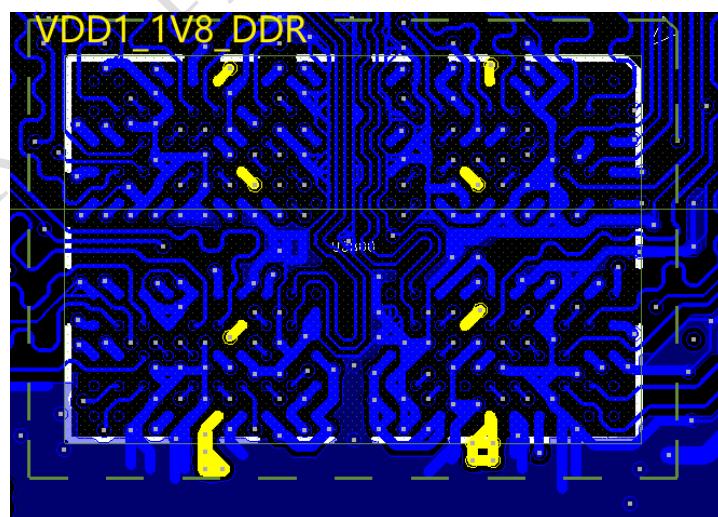


Figure 3-126 Requirements for the number of vias corresponding to the LPDDR4/4X chip VDD1_1V8_DDR power pins

(19) For LPDDR5, VDD2H_DDR_S3 power supply, it is recommended that one pin corresponds to at least 0.6 power via, for example as follows.

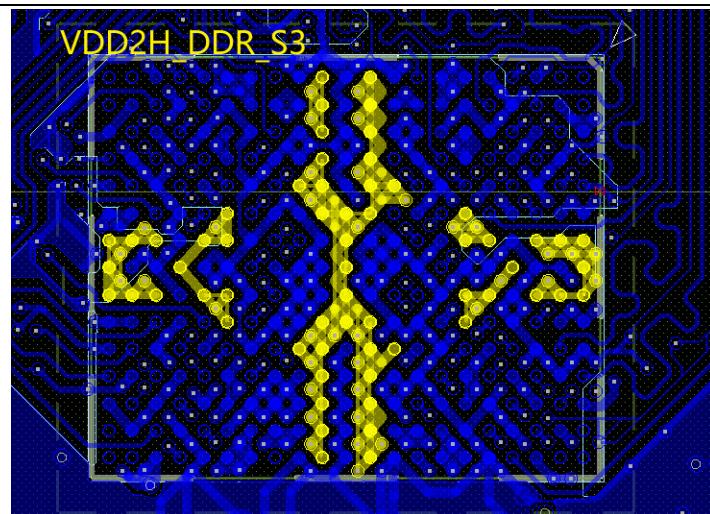


Figure 3-127 Requirements for the number of vias corresponding to the LPDDR5 chip VDD2H_DDR_S3 power pins

(20) For LPDDR5, VDD1_1V8_DD power supply, it is recommended that one pin corresponds to 1 power via, for example as follows.

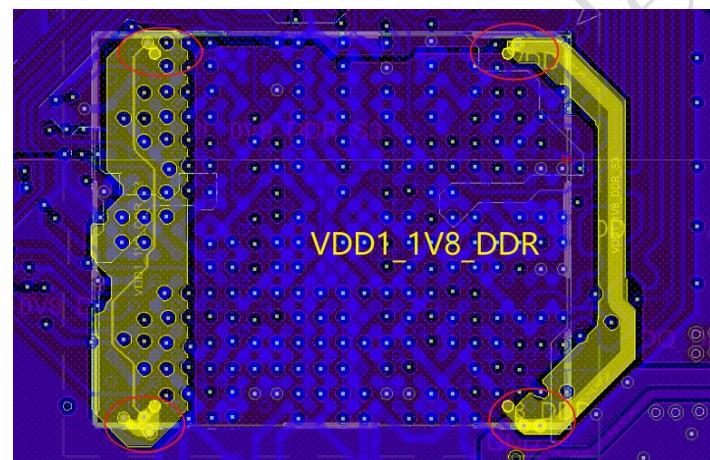


Figure 3-128 Requirements for the number of vias corresponding to the LPDDR5 chip VDD1_1V8_DDR power pins

(21) For LPDDR5, VDD2L_0V9_DDR_S3 power supply, it is recommended that one pin corresponds to at least 0.75 power via, for example as follows.

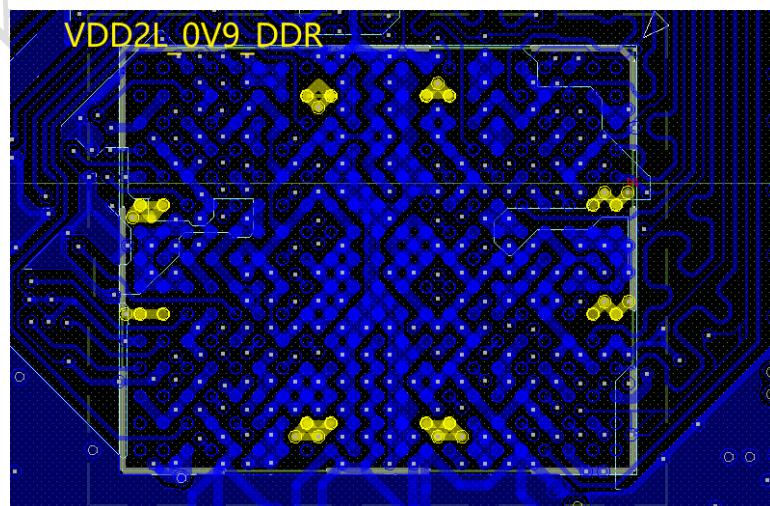


Figure 3-129 Requirements for the number of vias corresponding to the LPDDR5 chip VDD2L_0V9_DDR_S3 power pins

(22) At least one via per pad of Capacitor. For 0603 or 0805 capacitors, it is recommended that one pad corresponds to two vias.

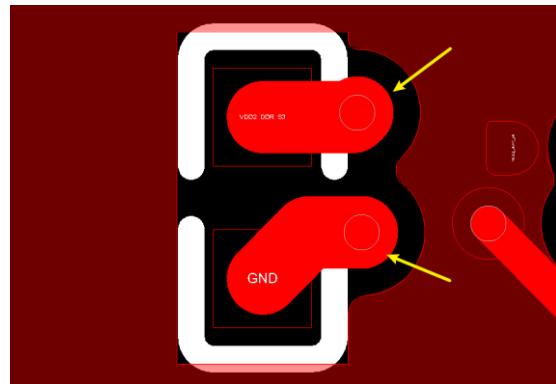


Figure 3-130 Number of vias corresponding to capacitor pads

(23) Place via closer to the pin to reduce the loop inductance.

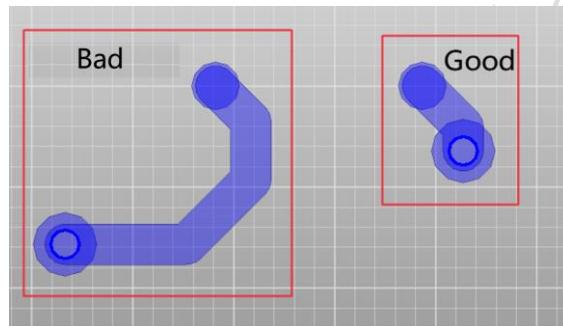


Figure 3-131 Schematic of placement of vias close to pins

(24) Avoid discontinuity in power plane by inserting other signal nets or matrix of vias with their associated anti-pads.

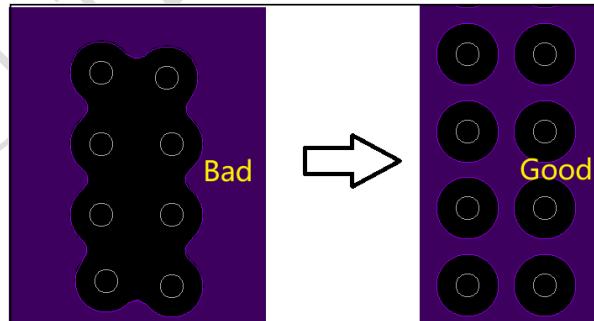


Figure 3-132 Schematic of the power plane being damaged by traces

(25) The decoupling capacitor should be placed close to the DDR chip pin, in order to reduce the loop inductance of the capacitors. The number of capacitors is recommended to refer to the DDR template design, and it is not recommended to delete the capacitors. Capacitors should be evenly placed.

(26) The recommended PDN requirement for the VDD2_DDR_S3 power at the LPDDR4X area is as shown below.

Table 3-17 the recommended PDN target impedance requirements of LPDDR4X chip VDD2_DDR_S3 power supply

Frequency	Impedance (ohm)
100Khz~1Mhz	≤ 0.03
1Mhz ~30Mhz	≤ 0.03
30Mhz~100Mhz	≤ 0.04

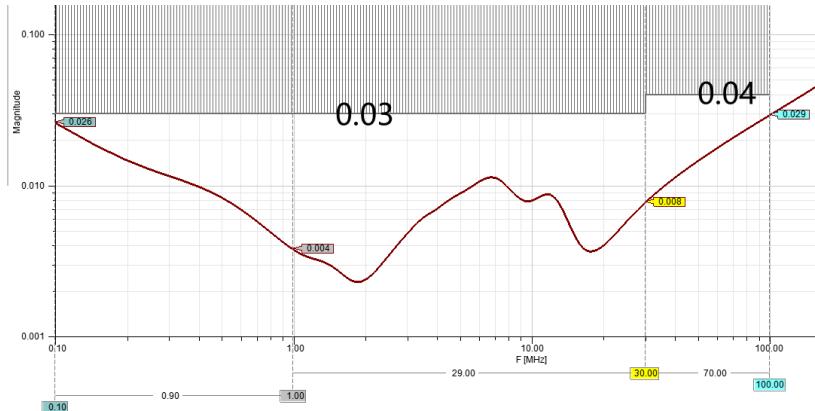


Figure 3-133 the recommended PDN requirements of LPDDR4X chip VDD2_DDR_S3 power supply

(27) The recommended PDN requirement for the VDDQ_DRAM_S0 power at the LPDDR4X area is as shown below.

Table 3-18 the recommended PDN target impedance requirements of LPDDR4X chip VDDQ_DRAM_S0 power supply

Frequency	Impedance (ohm)
100Khz~1Mhz	≤ 0.03
1Mhz ~30Mhz	≤ 0.03
30Mhz~100Mhz	≤ 0.04

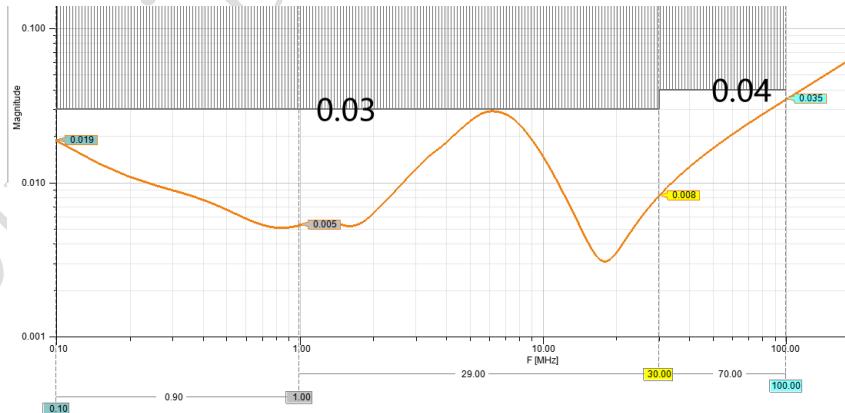


Figure 3-134 the recommended PDN requirements of LPDDR4X chip VDDQ_DRAM_S0 power supply

(28) The recommended PDN requirement for the VDD2L_0V9_DDR_S3 power at the LPDDR5 area is as shown below.

Table 3-19 the recommended PDN target impedance requirements of LPDDR5 chip VDD2L_0V9_DDR_S3 power supply

Frequency	Impedance (ohm)
100Khz~1Mhz	≤ 0.07

Frequency	Impedance (ohm)
1Mhz ~30Mhz	≤ 0.07
30Mhz~100Mhz	≤ 0.08

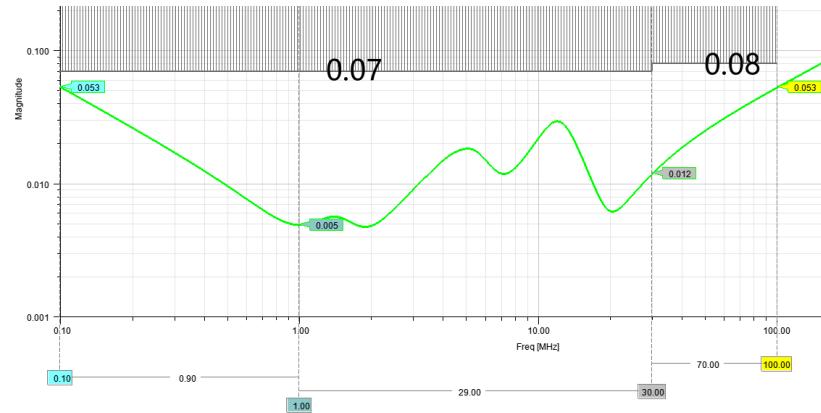


Figure 3-135 the recommended PDN requirements of LPDDR5 chip VDD2L_0V9_DDR_S3 power supply

(29) The recommended PDN requirement for the VDD2H_DDR_S3 power at the LPDDR5 area is as shown below.

Table 3-20 the recommended PDN target impedance requirements of LPDDR5 chip VDD2H_DDR_S3 power supply

Frequency	Impedance (ohm)
100Khz~1Mhz	≤ 0.03
1Mhz ~30Mhz	≤ 0.03
30Mhz~100Mhz	≤ 0.04

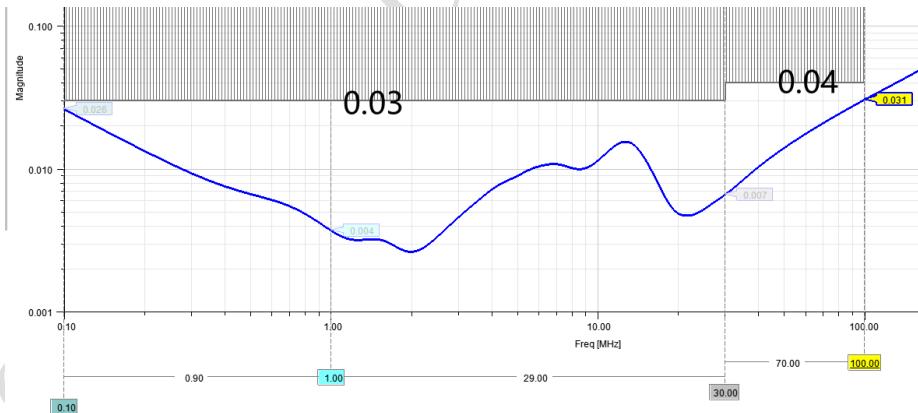


Figure 3-136 the recommended PDN requirements of LPDDR5 chip VDD2H_DDR_S3 power supply

3.5.3.1 LPDDR5 Interface

Table 3-21 LPDDR5 Routing Requirements

Parameter	Requirements
DQ, DM single-ended signal impedance	40 Ohm $\pm 10\%$
Address control lines single-ended signal impedance	50 Ohm $\pm 10\%$

Parameter	Requirements
Differential Signal Impedance	$90\text{ Ohm} \pm 10\%$
Equal length between DQ and DQS, WCLK (the same Byte)	$\leq 90\text{mil}$
Equal length between DM and DQS, WCLK (the same Byte)	$\leq 90\text{mil}$
Equal length between address, control lines and CLK	$\leq 90\text{mil}$
Equal length between DQS_P and DQS_N (the same Byte)	$\leq 5\text{mil}$
Equal length between WCLK_P and WCLK_N (the same Byte)	$\leq 5\text{mil}$
Equal length between CLK_P and CLK_N	$\leq 5\text{mil}$
Equal length between DQS, WCLK and CLK	$\leq 230\text{mil}$
The space between different Bytes (airgap)	≥ 2 times the trace width
The distance between DQ and DQ in the same Byte (airgap)	≥ 2 times the trace width
The distance between DQ and DQS in the same Byte (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width
The distance between DQ and WCLK in the same Byte (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width
Spacing between address control lines (airgap)	≥ 2 times the trace width
Spacing between CLK and other signal lines (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.5.3.2 LPDDR4X/ LPDDR4 Interface

Table 3-22 LPDDR4X, LPDDR4 Routing Requirements

Parameter	Requirements
DQ, DM single-ended signal impedance	$45\text{ Ohm} \pm 10\%$
Address control lines single-ended signal impedance	$50\text{ Ohm} \pm 10\%$
Differential Signal Impedance	$90\text{ Ohm} \pm 10\%$
Equal length between DQ and DQS (within the same Byte)	$\leq 90\text{mil}$
Equal length between DM and DQS (within the same Byte)	$\leq 90\text{mil}$
Equal length between address, control lines and CLK	$\leq 90\text{mil}$
Equal length between DQS_P and DQS_N (within the same Byte)	$\leq 5\text{mil}$
Equal length between CLK_P and CLK_N	$\leq 5\text{mil}$
Equal length between DQS and CLK	$\leq 230\text{mil}$
The space between different Bytes (airgap)	≥ 2 times the trace width
The distance between DQ and DQ in the same Byte (airgap)	≥ 2 times the trace width
The distance between DQ and DQS in the same Byte (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width
Spacing between address control lines (airgap)	≥ 2 times the trace width
Spacing between CLK and other signal lines (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.5.4 DP1.4 PCB Design

Table 3-23 Layout Requirements for DP1.4

Parameter	Requirement
Trace Impedance	$100\Omega \pm 10\%$ differential (DP only) $95\Omega \pm 10\%$ differential (USB3.0 / DP1.4 Alt)
Max intra-pair skew	<6mil
Max mismatch between data pairs	<1000mil
Max trace length on carrier board	<6 inches
Minimum airgap between pair to pair	Recommend ≥ 6 times the width of DP trace.
Minimum airgap between DP and other signal	Recommend ≥ 6 times the width of DP trace.
Maximum allowed via	Recommend ≤ 2 vias
AC Capacitor	Recommend 100nF (75nF to 200nF including tolerance)
ESD	Typical I/O-to-GND Capacitance $\leq 0.2\text{pF}$

Place GND through via in BGA zone as showed below and recommend to follow routing recommendations in Section 3.3.3, GND via interval length should less than 300mil.

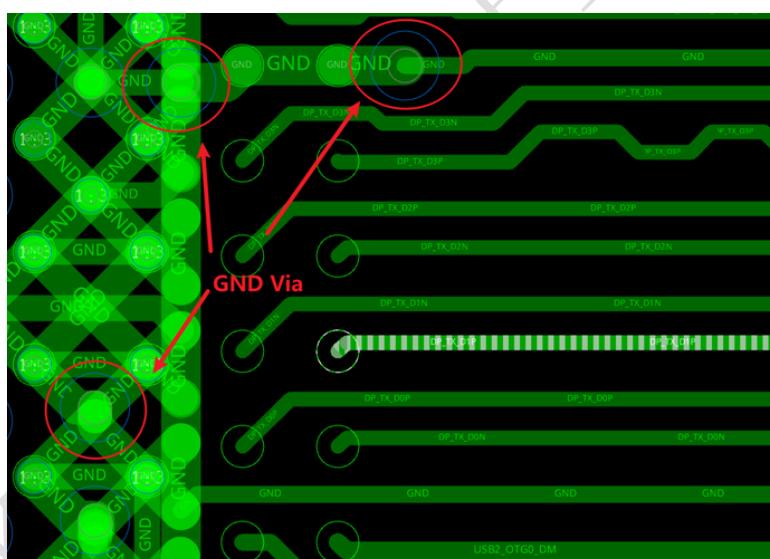


Figure 3-137 DP Ball Area Fanout layout

3.5.5 PCIe2.1 PCB Design

Table 3-24 Layout Requirements for PCIe2.1

Parameter	Requirement
Trace Impedance	$85\text{ohm} \pm 10\%$ differential
Max intra-pair skew	<6mil
Max inter-pair skew	<6inches
Max trace length on carrier board	<6inches

Parameter	Requirement
AC coupling capacitors	100nF $\pm 20\%$, discrete 0201 package preferable
Minimum airgap between pair to pair	≥ 4 times the width of the trace.
Max intra-pair skew of REFCLK	<12mil
Trace Impedance of REFCLK	100Ω $\pm 10\%$ differential
Minimum airgap between PCI-E and other Signals	Recommend ≥ 5 times the width of PCI-E trace. At least 4 times the width of PCI-E trace.
Maximum allowed via	Recommend ≤ 2 vias

3.5.6 HDMI 2.1 PCB Design

Table 3-25 Layout Requirements for HDMI2.1

Parameter	Requirement
Trace Impedance	100Ω $\pm 10\%$ differential
Max intra-pair skew	<6mil
Max mismatch between pairs	<480mil
Max trace length on carrier board	<4 inches
AC coupling capacitors	220nF $\pm 20\%$, discrete 0201 package preferable
Minimum airgap between pair to pair	Recommend ≥ 7 times the width of HDMI trace
Minimum airgap between HDMI and other Signals	Recommend ≥ 7 times the width of HDMI trace
Maximum allowed via	Recommend novias
ESD	Typical I/O-to-GND Capacitance $\leq 0.2\text{pF}$

(1) Place GND through via in BGA zone as showed below and recommend to follow routing recommendations in Section 3.3.3, GND via interval length should less than 150mil.

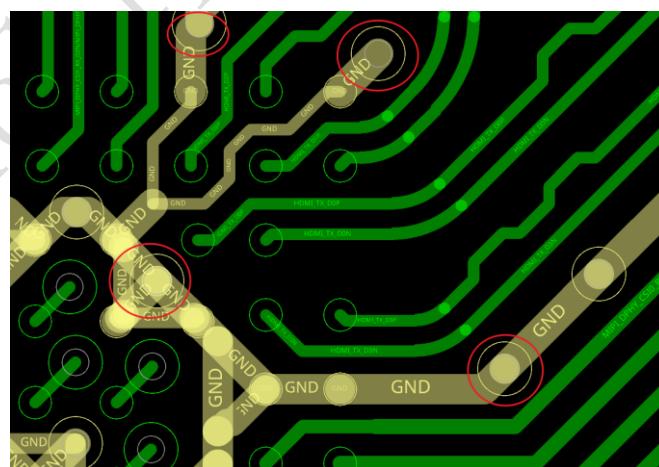


Figure 3-138 HDMI2.1 BGA Area Fanout layout

(2) Trace between DC blocking capacitor and resistor should be routed as differential pair.

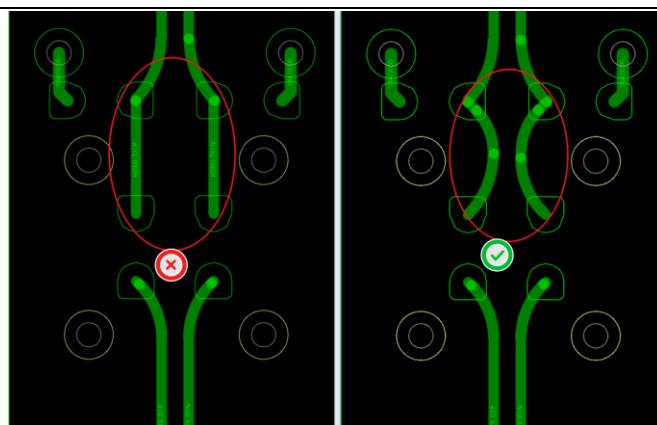


Figure 3-139 Differential signal wiring between capacitor and resistor

(3) Void reference plane under 590ohm resistor's pad. Keep no stub between trace and resistor pads.

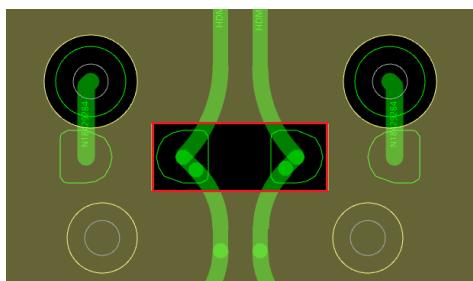


Figure 3-140 590ohm resistor layout diagram

3.5.7 UFS2.0 PCB Design

Table 3-26 Layout Requirements for UFS2.0

Parameter	Requirement
Trace Impedance	$100\text{ohm} \pm 10\%$ differential
Max intra-pair skew	<6mil
Max mismatch between pairs	<100mil
Max trace length on carrier board	<4 inches
Minimum airgap between pair to pair	Recommend ≥ 4 times the width of UFS trace
Minimum airgap between UFS and other Signals	Recommend ≥ 5 times the width of UFS trace
Maximum allowed via	Recommend ≤ 2 vias

(1) Place GND through via in BGA zone as showed below and recommend to follow routing recommendations in Section 3.3.3, GND via interval length should less than 300mil.

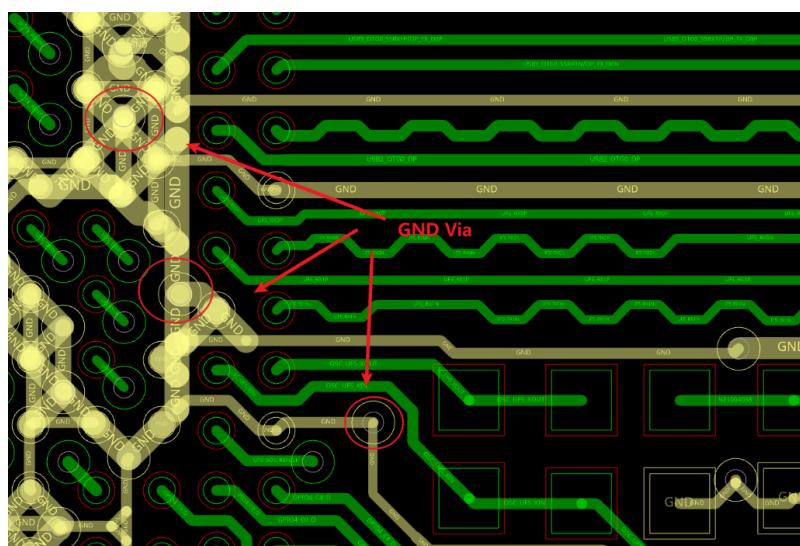


Figure 3-141 UFS2.0 BGA Area Fanout layout

(2) For the series connection resistor at UFS TX/RX link path, adjacent layers need to do void processing, void size with the size of the resistor can be, refer to the following.

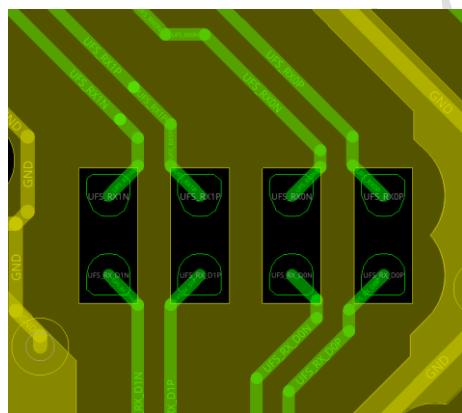


Figure 3-142 adjacent layers void processing

(3) The reference clock of UFS has strict phase noise requirements, so special attention is required

- The clock output from the master to the UFS (UFS_REFCLK) requires a full GND reference plane.
- Within The clock signal layer change 25mil (via centre spacing) add the GND return via.
- UFS_REFCLK requires a ground shielding for the entire trace: note that the ground trace should be connected to the GND vias and the GND plane, and the GND vias spacing is recommended to be $\leq 400\text{mil}$.



Figure 3-143 UFS_REFCLK ground shielding schematic

3.5.8 SATA 3.1 PCB Design

Table 3-27 Layout Requirements for SATA3.1

Parameter	Requirement
Trace Impedance	100Ω ±10% differential (100 Ohm target impedance is preferred, if stackup limits, 100 Ohm can not meet, at least meet 90 Ohm ± 10%)
Max intra-pair skew	<6mil
Max trace length on carrier board	<6 inches
AC coupling capacitors	10nF ±20%, discrete 0201 package preferable
Minimum airgap between pair to pair	≥4 times the width of SATA trace.
Minimum airgap space between SATA and other Signals	≥4 times the width of SATA trace.
Maximum allowed via	Recommend≤ 2 vias

3.5.9 USB2.0 PCB Design

Table 3-28 Layout Requirements for USB2.0

Parameter	Requirement
Trace Impedance	90Ω ±10% differential
Max intra-pair skew	<20mil
Max trace length on carrier board	<6 inches
Maximum allowed via	Recommend less than 4 vias Cannot exceed 6 vias

3.5.10 USB3.2 Gen1x1 PCB Design

Table 3-29 Layout Requirements for USB3.2 Gen1x1

Parameter	Requirement
Trace Impedance	$90\Omega \pm 10\%$ differential
Max intra-pair skew	<6mil
Max trace length on carrier board	<6 inches
AC coupling capacitors	$100nF \pm 20\%$, discrete 0201 package preferable
Minimum airgap between pair to pair	≥ 4 times the width of USB trace.
Minimum airgap between USB and other Signals	≥ 4 times the width of USB trace.
Maximum allowed via	Recommend less ≤ 2 vias
ESD	I/O capacitance to ground $\leq 0.2pF$

3.5.11 MIPI-D/C PHY TX PCB Design

Table 3-30 Layout Requirements for MIPI-DPHY

Parameter	Requirement
Trace Impedance	$100\Omega \pm 10\%$ differential (if stackup limits, 100 Ohm can not meet, at least meet $95\Omega \pm 10\%$. 100 Ohm is preferred first)
Max intra-pair skew	<6mil
Data to clock matching	<12mil
Max trace length	<6 inches
Maximum allowed via	4
Minimum airgap between pair to pair	Recommend ≥ 4 times the width of MIPI trace. At least 3 times the width of MIPI trace.
Minimum airgap between MIPI and other Signals	Recommend ≥ 4 times the width of MIPI trace. At least 3 times the width of MIPI trace.

Table 3-31 Layout Requirements for MIPI-CPHY TX

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Max intra-pair skew(TRIO_A\TRIO_B\TRIO_C)	< 6 mil
Inter-pair skew(TRIO0\TRIO1\TRIO2)	<100mil
Max trace length	<5 inches
Maximum allowed via	2
Airgap between Signals	Recommend ≥ 4 times the width of MIPI trace.
Minimum airgap between MIPI and other Signals	Recommend ≥ 4 times the width of MIPI trace.

Place GND through via in BGA zone as showed below.

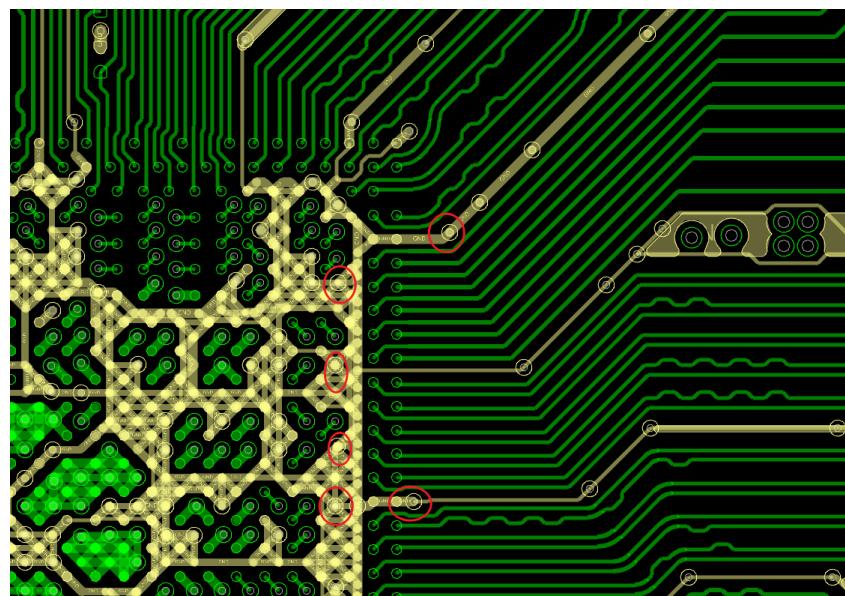


Figure 3-144 GND through via placement in MIPI BGA area

3.5.12 eDP PCB Design

Table 3-32 Layout Requirements for eDP

Parameter	Requirement
Trace Impedance	$90\Omega \pm 10\%$ differential (make sure EDP cable impedance is same as PCB)
Max intra-pair skew	<6mil
Max trace length on carrier board	<6 inches
Minimum airgap between pair to pair	≥ 4 times the width of EDP trace.
AC coupling capacitors	$220nF \pm 20\%$, discrete 0201 package preferable
Minimum airgap between EDP and other Signals	≥ 4 times the width of EDP trace.
Maximum allowed via	Recommend ≤ 2 vias

3.5.13 eMMC PCB Design

Table 3-33 Layout Requirements for eMMC

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock matching	<120mil
Max trace length	<3.5 inches
Minimum airgap of eMMC Signals	At least 2 times the width of eMMC trace.
Minimum airgap between eMMC and other Signals	Recommend 3 times the width of eMMC trace. At least 2 times the width of eMMC trace.
Maximum allowed via	Recommend ≤ 2 vias

eMMC signal should route with reference to ground plane, and place stitching via within 30mil (center-to-

center) of the signal transition vias. Via-stitch should able to connect both reference plane to ensure continuous grounding.

3.5.14 SDMMC PCB Design

Table 3-34 Layout Requirements for SDMMC/SDIO

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock mismatch	<120mil
Max trace length	<4 inches
Minimum airgap of SDMMC Signals	At least 2 times the width of SDMMC/SDIO trace.

3.5.15 FSPI PCB Design

Table 3-35 Layout Requirements for FSPI

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock mismatch	<200mil
Max trace length	<4 inches
Minimum airgap of FSPI Signals	At least 2 times the width of FSPI trace.

3.5.16 BT1120 PCB Design

Table 3-36 Layout Requirements for BT1120

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock mismatch	<180mil
Max trace length	<5 inches
Minimum airgap of BT1120 Signals	Recommend 2 times the width of BT1120 trace.

3.5.17 LCDC PCB Design

Table 3-37 Layout Requirements for LCDC

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock mismatch	<180mil
Max trace length	<5 inches
Minimum airgap of LCDC Signals	Recommend 2 times the width of LCDC trace.

3.5.18 RGB PCB Design

Table 3-38 Layout Requirements for RGB

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock mismatch	<180mil
Max trace length	<5 inches
Minimum airgap of RGB Signals	Recommend 2 times the width of RGB trace.

3.5.19 CIF PCB Design

Table 3-39 Layout Requirements for CIF

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock mismatch	<180mil
Max trace length	<5 inches
Minimum airgap of RGB Signals	Recommend 2 times the width of CIF trace.
Minimum airgap between CIF and other Signals	Recommend 3 times the width of CIF trace.

Note: For CIF interface, RK3576 is only used as RX, the actual layout length depends on the transmitter device (e.g. Camera), the above wiring requirements are for reference only.

3.5.20 EBC PCB Design

Table 3-40 Layout Requirements for EBC

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock mismatch	<180mil
Max trace length	<5 inches
Minimum airgap of EBC Signals	Recommend 2 times the width of EBC trace.

3.5.21 RGMII PCB Design

Table 3-41 Layout Requirements for RGMII

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
(TXD{0-3}, TXEN) to TXCLK mismatch	<120mil
(RXD{0-3}, RXDV) to RXCLK mismatch	<120mil
Max trace length	<5 inches
Minimum airgap of RGMII Signals	At least 2 times the width of RGMII trace.
Minimum airgap between RGMII and other Signals	Recommend 3 times the width of RGMII trace. At least 2 times the width of RGMII trace.

3.5.22 DSMC PCB Design

DSMC interface supports 3 routing method as follow:

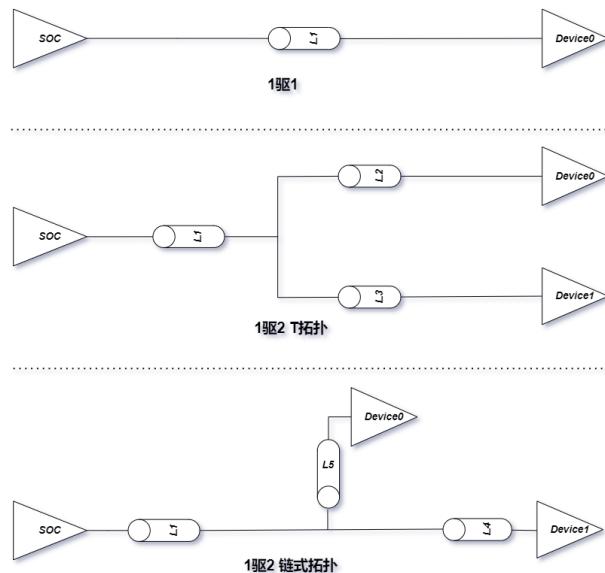


Table 3-42 Layout Requirements for DSMC

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended $100 \pm 10\%$ differential
Branch (L2/L3/L4/L5) trace lengths	$L2 < 500\text{mil}$ $L3 < 500\text{mil}$ $L4 < 1\text{inch}$ $L5 < 100\text{mil}$
Max trace length	$L1+L2 < 5\text{inch}$ $L1+L3 < 5\text{inch}$ $L1+L4 < 5\text{inch}$
1-drive-2 T topology branches for mismatch	$ L2-L3 < 100\text{mil}$
Data to clock mismatch	$< 120\text{mil}$
Minimum airgap of DSMCSignals	Recommend 3 times the width of DSMCtrace.
Minimum airgap between DSMCand other Signals	Recommend 3 times the width of DSMC trace. At least 2 times the width of DSMC trace.

3.5.23 FlexBus PCB Design

Table 3-43 Layout Requirements for FlexBus

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock mismatch	$< 180\text{mil}$
Max trace length	< 5 inches
Minimum airgap of FlexBus Signals	At least 2 times the width of Flexbus trace.

3.5.24 Audio Interface Circuit PCB Design

For the digital audio interface of the RK3576 platform, it is necessary to follow the high-speed signal routing recommendations section, and the related routing of the additional requirements are as follows

- All CLK signals are recommended to be connected in series with a 22-ohm resistor placed close to the RK3576 to improve signal quality.
- CLK signals should not be routed adjacent to each other to avoid crosstalk. They need to be individually grounded, and there must be ground vias within 300 mils of spacing between grounded traces.
- Decoupling capacitors for each IO power domain of the chip should be placed on the corresponding power pins, preferably on the backside of the PCB. For single-sided mounting, place them as close as possible to the chip.
- When multiple devices are connected to a Serial Audio Interface (SAI) (I2S/PCM/TDM) interface, the related CLK signals should be routed in a daisy-chain topology.
- When multiple devices are connected to a Pulse Density Modulation (PDM) interface, the related CLK signals should be routed in a daisy-chain topology. If there are available GPIO pins, both CLK signals within a PDM interface group can be used to optimize routing branches.
- SPDIF signals are recommended to be fully grounded throughout the routing, with ground vias within 300 mils of spacing between grounded traces.
- For routing requirements related to external audio signals, refer to the design guidelines of the corresponding devices. If not specified, the following instructions can be considered:
- Speaker SPKP/SPKN signals should be coupled and routed as a group, with the entire group grounded. The trace width should be calculated based on the peak output current and the routing should be kept as short as possible to control impedance.
- If magnetic beads, LC filters, or similar components are placed on the output of the speaker amplifier, it is recommended to place them close to the amplifier output to optimize EMI.
- Left and right channel outputs of the headphone should be individually grounded to avoid crosstalk and optimize isolation. The trace width is recommended to be greater than 10 mil.
- When connecting a microphone in single-ended mode, the MIC signal should be routed separately and individually grounded.
- When connecting a microphone in differential mode, including pseudo-differential cases, it should be routed as a differential pair and grounded as a group.
- The microphone signal routing is recommended to have a trace width of 8 mil or above.
- All audio signals should be kept away from high-speed signal lines such as LCD, DRAM, etc. Routing on adjacent layers to high-speed signal lines is prohibited. The adjacent layer to audio signals must be a ground plane, and no drilling or layer swapping should be done near high-speed signal lines.
- Audio signal routing should be kept away from inductor areas, RF signals, and components.
- For TVS protection diodes used in headphone jacks or microphones, it is recommended to place them as close as possible to the connector. The signal topology should be: Headphone jack/microphone → TVS → IC. This arrangement allows the ESD current to be attenuated by the TVS device. There should be no stubs in the routing of TVS devices, and it is advisable to add ground vias to the TVS ground pin, with at least two 0402 vias to enhance electrostatic discharge capability.

3.5.25 Wi-Fi/BT PCB Design

3.5.25.1 RF Module Layout

- During the overall layout, place the Wi-Fi module in a suitable position, preferably close to the board's edge. Keep the module away from high-speed signals such as DDR, HDMI, USB, LCD circuits, and magnetic components like speakers.
- The TOP layer below the module should not have any traces. Ensure that the reference plane is a complete ground plane. For signals like SDIO, PCIe, UART, and PCM, it is recommended to route them around the module's projection area before connecting them to the module pins. Try to avoid crossing RF and digital traces to reduce interference and crosstalk.
- Use appropriate layout techniques to minimize the length of signal paths and ensure impedance continuity.
- Separate and isolate the RF and digital sections of the module to prevent mutual interference.

3.5.25.2 RF Circuit Design

- The characteristic impedance of RF transmission lines should be 50 ohms, with impedance deviation controlled within +/-10%.
- Keep RF transmission lines short and direct, avoiding crossings with digital signal lines or power lines.
- Make transmission lines wide, preferably greater than 8mil, to reduce transmission losses. They can be referenced to adjacent layers, and both sides of the RF traces should be fully grounded with accompanying ground vias.
- Avoid sharp corners and acute bends in transmission line routing, as they can cause signal reflection and impedance mismatch. Use rounded corners or 45-degree angles whenever possible.
- Minimize branching and layer changes in transmission line routing.
- Ensure impedance matching between RF transmission lines and the module and antenna impedance. Provide space for PI or T-type matching circuits.
- For module RF pins, create voids in adjacent layers to reduce parasitic capacitance effects.
- If IPEX RF connectors are used, create voids below the connectors to reduce parasitic capacitance effects.

3.5.25.3 Crystals

- Pay special attention to the layout of crystal circuits. Place the crystals on the same layer as the chip and as close as possible. Keep the crystal traces as short as possible.
- Place the crystals away from components that may cause interference. Connect the crystal ground to the reference ground plane and minimize the length of the ground return path. It is recommended to isolate the ground around the crystal from the same layer ground.
- Avoid placing crystals near heat-generating components to prevent temperature changes from affecting crystal performance.
- Provide solid ground planes for crystals and clock signals. Add a GND via every 100mil along the ground traces and ensure the reference ground plane in adjacent layers is intact without any traces below.
- The clock specifications should have a Frequency Tolerance of < +/-10ppm and an ESR < 100 ohms.
- Route the 32.768k clock signal separately and provide solid ground traces. Add a GND via every 400mil

along the ground trace.

3.5.25.4 Power

- RF modules have higher requirements for power stability, so ensure that the power line design is reasonable to maintain stable operating voltage and current.
- RF module operation can be affected by power supply noise. Therefore, add sufficient filtering circuits at the power input, including capacitors, inductors, and filters, to reduce power supply noise and interference.
- Place the decoupling capacitors for the module's power filtering close to the module's power pins.
- Minimize the length of the power lines, reduce line impedance, and improve power stability and response speed.
- Separate the power lines of the RF module from the power lines of other modules as much as possible to avoid mutual interference and improve system stability and reliability.
- The VBAT trace for the module should be as wide as possible, with a peak current larger than 1A. It is recommended to have a width greater than 40mil, with ground vias around the trace.
- The VDDIO trace for the module should also be wide, with a width greater than 20mil.
- When placing external inductors, route the traces to pass through capacitors before entering the module's power pins.

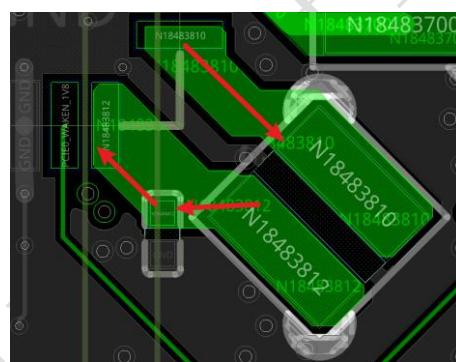


Figure 3-145 Schematic diagram of inductor and capacitor routing for the Wi-Fi module.

3.5.25.5 Antenna

- When arranging the antenna, consider the actual usage scenario and directional requirements of the device. Choose the antenna type and placement method wisely to achieve optimal signal coverage and reception performance.
- Place the antenna as close as possible to the RF output port of the module to minimize excessive insertion loss caused by long RF transmission lines on the motherboard.
- The antenna matching circuit should be located near the antenna connector. The antenna trace should have a characteristic impedance of 50 ohms, ensuring the integrity of the reference ground and avoiding abrupt impedance changes. No other signal lines or power lines should be present below the antenna trace. The accompanying ground for the trace should be connected to the main ground reference plane using ground vias.
- Avoid any components near the antenna that may cause electromagnetic interference, such as high-

frequency circuits and power lines, to avoid affecting the antenna's performance. The antenna should be kept away from any metallic or magnetic components, such as USB connectors, Ethernet ports, power supplies, power inductors, motors, and speakers. There should be sufficient clearance around the antenna.

- If using an on-board PCB antenna, ensure that the antenna keep-out area meets the antenna design requirements.
- Metal enclosures or metal plating can significantly affect antenna performance, so it is recommended to have an external antenna.
- If using a 2T2R MIMO antenna interface, consider the positioning of the two antennas. They should be placed as far apart as possible, with an isolation of at least 20dB. Also, consider placing them vertically to avoid mutual interference.

3.5.25.6 Signal Lines

- For SDIO Wi-Fi, refer to the PCB design requirements for SDIO signals in section 3.5.14.
- For PCIe Wi-Fi, refer to the PCB design requirements for PCIe signals in section 3.5.5.

3.5.26 VGA OUT PCB design

- When planning the overall layout, place the VGA connector close to the conversion chip to minimize the length of VGA analog signal traces.
- Decoupling capacitors for the power supply of the conversion chip should be located as close as possible to the respective power pins of the chip.
- Increase the trace width for VGA_R/G/B signals, preferably to 12 mil or above.
- The length difference between VGA_R/G/B traces should not exceed 200 mil.
- Place the 75-ohm resistors for VGA_R/G/B signals close to the chip.
- Position the filtering circuits for VGA_R/G/B signals near the VGA connector.
- Ensure that VGA_R/G/B signals are routed with separate ground planes throughout the entire length. Ground vias should be placed within 300 mil spacing between ground traces.
- The adjacent layers of VGA_R/G/B signals must be ground planes, not power planes.
- Keep VGA_R/G/B signals away from high-speed signal lines such as LCD and DRAM. Avoid routing traces in adjacent layers to high-speed signal lines and avoid drilling vias near them. Do not route traces through inductor areas. Keep them away from RF signals and devices.
- RC filtering for VGA_HSYNC/VSYNC signals should be placed near the VGA connector, and the trace length should not exceed 6 inches.
- Place TVS diodes as close as possible to the connector for all VGA connector signals. The signal path should be: VGA connector → TVS → chip pins. When ESD events occur, the ESD current must pass through the TVS device for attenuation. Avoid stubs on TVS traces.
- It is recommended to add ground vias for the TVS ground pins, with at least two 0402-sized vias to enhance electrostatic discharge capabilities.

3.5.27 LCD Screen and Touchscreen PCB Design

- Place the current-limiting resistor for the LED backlight IC's FB pin near the screen connector, not the

DC-DC converter.

- Pay attention to the placement of capacitors and power trace routing for the backlight boost circuit to minimize the charging and discharging loop of the power supply.
- If there are test points reserved for the screen and touchscreen connectors, place them close to the connectors, and keep the stubs on the traces as short as possible.

3.5.28 Camera PCB Design

- When using a connector for the camera: for MIPI differential signals passing through the connector, adjacent differential signal pairs must be isolated using ground pins. The MCLK signal should have a solid ground plane and be separated from the MIPI differential signals.
- In multi-camera designs, separate HSYNC and VSYNC signal lines from MCLK and differential signal lines with ground planes to avoid crosstalk.
- For projects in low-light environments, it is recommended to reserve positions for DVDD/AVDD LDOs on the module end. Avoid using DC-DC converters for DVDD and consider using LDOs instead to avoid affecting low-light environment debugging.
- Decoupling capacitors for AVDD/DOVDD/DVDD power supply of the connector should be placed as close as possible to the camera connector.
- If there are test points reserved near the camera connector, place them close to the connector, and keep the stubs on the traces as short as possible.
- When placing the camera, keep it away from high-power radiation devices such as wireless communication antennas.

4 Thermal Design Recommendations

Good thermal design is particularly important for enhancing the performance, system stability, and product safety of RK3576.

4.1 Thermal Simulation Results

For the packaging of RK3576 FCCSP698L_16.1mmx17.2mm with a mixed ball size of 0.55mm, 0.60mm, and 0.65mm, and using a 2S2P test board according to JESD 51-7/JESD 51-9 requirements, a thermal resistance simulation report will be generated by placing the system under natural convection (JEDEC JESD51-2 standard). It is important to note that the actual system design and environment for practical applications may differ from the mentioned standards, requiring analysis based on the application conditions.



NOTE

Please note that the thermal resistance provided is a reference value for the PCB without a heat sink. The specific temperature will depend on the design, size, thickness, material, and other physical factors of the board.

4.1.1 Result Review

The thermal resistance simulation results are shown in the following table

Table 4-1 RK3576 thermal resistance simulation results

Package (EHS-FCCSP)	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	ψ_{JT} (°C/W)
JEDEC PCB	15.84	6.96	0.67	0.031

Note:

- θ_{JB} is measured under specific conditions (JEDEC JESD51-8 standard) using the PCB specified in JESD51-7.
- Thermal resistance θ_{JC} is obtained according to JEDEC JESD51-14.
- The thermal characteristic parameter ψ_{JT} represents the difference between junction temperature and the center temperature of the top surface of the component package. ψ_{JT} is measured in the testing environment of θ_{JA} (JEDEC JESD51-2 standard).
- The data provided is simulated and should be used for reference purposes only. Please rely on physical testing for accurate results.

4.1.2 Explanation of Terms

The terms used in this chapter are explained as follows

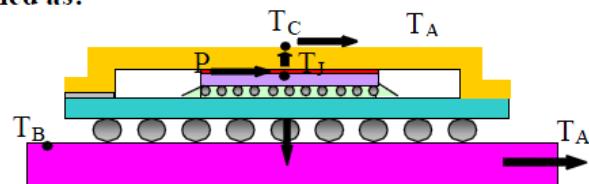
- T_J : The maximum junction temperature;
- T_A : The ambient or environment temperature;

- T_c : The maximum compound surface temperature;
- T_b : The maximum surface temperature of PCB bottom;
- P : Total input power

The thermal parameter can be define as following

1. Junction to ambient thermal resistance, θ_{JA} , defined as:

$$\theta_{JA} = \frac{T_J - T_A}{P}; \quad (1)$$



Thermal Dissipation of EHS-FCBGA

Figure 4-1 definition of θ_{JA}

2. Junction to case thermal resistance, θ_{JC} , defined as:

$$\theta_{JC} = \frac{T_J - T_C}{P}; \quad (2)$$

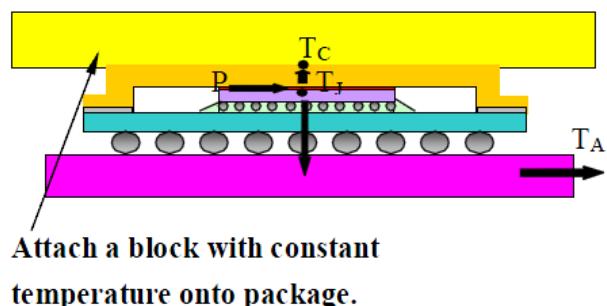


Figure 4-2 definition of θ_{JC}

3. Junction to board thermal resistance, θ_{JB} , defined as:

$$\theta_{JB} = \frac{T_J - T_B}{P}; \quad (3)$$

Attach a block with constant temperature

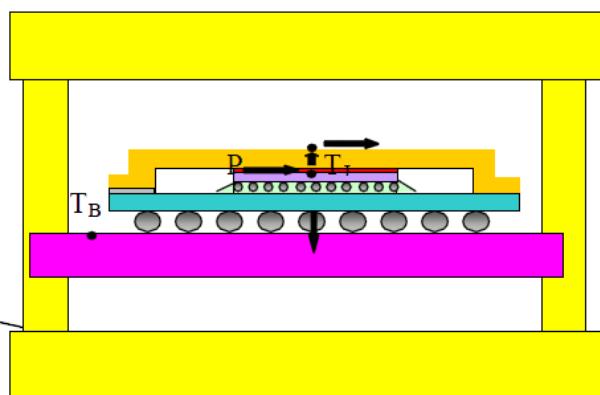


Figure 4-3 definition of θ_{JB}

4.2 Chip Internal Thermal Control Methods

4.2.1 Temperature Control Strategies

In the Linux kernel, there is a thermal control framework called the Linux Generic Thermal System Drivers. It provides different strategies for temperature control. Currently, the following strategies are commonly used:

- Power allocator: This strategy introduces a proportional-integral-derivative (PID) control. Based on the current temperature, it dynamically allocates power to different cooling devices. When the temperature is low, more power can be allocated, resulting in higher operating frequencies. As the temperature rises, the available power gradually decreases, leading to a reduction in the operating frequency. This strategy allows frequency limitation based on temperature.
- Stepwise: This strategy gradually reduces the frequency of the cooling devices based on the current temperature.
- Fair share: This strategy prioritizes the reduction of frequency in cooling devices with multiple frequency levels.
- Userspace: This strategy does not impose frequency limitations.

The RK3576 chip has an internal T-sensor for detecting on-chip temperature and defaults to using the power allocator strategy.

4.2.2 Temperature Control Configuration

The RK3576 SDK provides temperature control strategies specifically for the CPU and GPU. For detailed configuration, please refer to the "Rockchip_Developer_Guide_Thermal_CN.pdf"

<https://redmine.rock-chips.com/projects/fae/documents>

4.3 Circuit Thermal Design References

4.3.1 Circuit Schematic Thermal Design References

- Improve the overall power supply efficiency while maintaining stability, such as minimizing the use of high voltage difference LDOs to reduce heat generated during power conversion.
- Power down unused chip modules or implement power down handling in software, based on the actual product requirements.
- Select materials with high thermal conductivity. Estimate the required size of heat sinks based on product definition, usage environment, and other conditions. It is recommended to use larger heat sinks whenever possible.

4.3.2 PCB Thermal Design Reference

In the RK3576 product, the RK3576 chip is the highest heat-generating component, and all heat dissipation measures focus on the chip. Other major heat-generating components include the PMIC, charging IC, associated inductors, and backlight IC.

- A well-designed structure ensures heat exchange between the internal machine and the external air.
- During overall layout, distribute high-power or heat-generating components evenly to avoid localized

overheating. It is recommended to place RK3576 and RK806S-5 appropriately, neither too close nor too far apart, with a suggested spacing of 20mm to 50mm. Avoid placing them near the edges of the board as it hinders heat dissipation.

- It is recommended to use a PCB with six or more layers and increase the copper content. A copper thickness of 1oz is suggested. Utilize as many layers as possible for a ground plane, while other layers should fulfill power and signal routing needs. Also, try to create ground planes in those layers to aid heat dissipation using large copper foils.
- Several power domains of RK3576 (LOGIC_DVDD, GPU_DVDD, NPU_DVDD, CPU_BIG_DVDD, CPU_LIT_DVDD, DDRPHY_DVDD) have relatively high current. Ensure the trace routing or copper coverage can handle the current load to prevent excessive temperature rise.
- For chips with ePads, try to fill the vias above the ePads, and the adjacent layers must be ground planes. The backside copper should be as complete as possible, and it is recommended to leave it bare copper to enhance heat dissipation.
- The GND pins of the RK3576 chip on the top layer should be routed in a "well" shape with cross connections. It is suggested to use a trace width of 10mil for better chip cooling.
- For the GND pins of the RK3576 chip, it is recommended to increase the number of ground vias to provide more thermal paths. The adjacent layers must be ground planes to facilitate chip cooling.
- For the RK3576 chip's decoupling capacitor pads on the backside, it is recommended to use full copper coverage instead of flower-shape pads to maintain a complete copper plane and enhance heat dissipation.
- In open areas, without compromising the power layer, try to increase the number of ground vias to provide additional thermal paths and improve heat dissipation.

5 ESD/EMI Protection Design

5.1 Overview

This chapter gives suggestions for ESD/EMI protection design in RK3576 product design to help user better improve the anti-static and anti-EMI level of their products.

5.2 Explanation of Terms

The terminology in this chapter is explained as follows:

- ESD (Electro-Static Discharge): Refers to the release or discharge of static electricity.
- EMI (Electromagnetic Interference): Refers to electromagnetic interference, which includes both conducted interference and radiated interference.

5.3 ESD Protection

- Implement isolation on the mold and try to internally retract connectors within the casing. This elongates the distance for electrostatic discharge to reach the internal circuit, weakening its energy. Testing standards should transition from contact discharge conditions to air discharge, and so on.
- Take precautions to protect sensitive components and isolate them during PCB layout.
- Place the RK3576 chip and core components as close to the center of the PCB as possible. If they cannot be placed in the center, ensure that the shielding cover is at least 2mm away from the board edge and reliably grounded.
- PCB layout should be based on functional modules and signal flow. Keep sensitive sections independent from each other and isolate parts prone to interference.
- Place ESD devices reasonably, ideally at the source. ESD devices should be placed at interfaces or areas prone to electrostatic discharge.
- Keep components away from the board edges and at a distance from connectors.
- Ensure a good GND circuit on the PCB surface, and all connectors should have proper GND connections on the surface. If there are shielding covers, connect them to the surface GND as much as possible and add multiple ground vias at the solder joints of the shielding covers. To achieve this, avoid routing traces on the surface of connection socket sections and avoid cutting off the copper plane extensively.
- Do not route traces on the board edges of the surface layer and add multiple ground vias.
- Isolate signals from the ground when necessary.
- Expose more copper to enhance electrostatic discharge effectiveness or facilitate the addition of remedies such as foam padding.
- If there is board-to-board connection through connectors, it is recommended to series-connect all signals with a certain resistance (between 2.2ohm and 10ohm, depending on meeting SI testing requirements) and reserve TVS devices to enhance ESD surge protection.
- The 100nF capacitor for the nPOR pin of RK3576 must be placed close to the pin. The capacitor's ground pad must have a 0402 ground via, and if space permits, it is recommended to have two or more for better grounding.

- Critical signals such as Reset, clock, and interrupts should have a minimum distance of 5mm from the board edge.
- For other peripheral chips with Reset pins, it is recommended to add a 100nF capacitor close to the pin. The capacitor's ground pad must have a 0402 ground via, and if space permits, it is recommended to have two or more for better grounding.
- When designing the entire system as a floating ground device, avoid separating the interfaces with separate ground designs.
- If the machine's outer casing is metallic and the power supply has three prongs, ensure that the metal casing is properly connected to earth ground.
- Implement isolation on the PCB to confine electrostatic discharge to specific areas. For example, use separate vias for socket ground pins and internal ground layers, create keepout zones on the surface layer of the PCB, and keep the surface ground copper plane and pins as far apart as possible. This ensures that sensitive signals are far from areas prone to electrostatic discharge (surface ground copper plane), as shown in the diagram where the HDMI signal is isolated from GND on the surface layer.

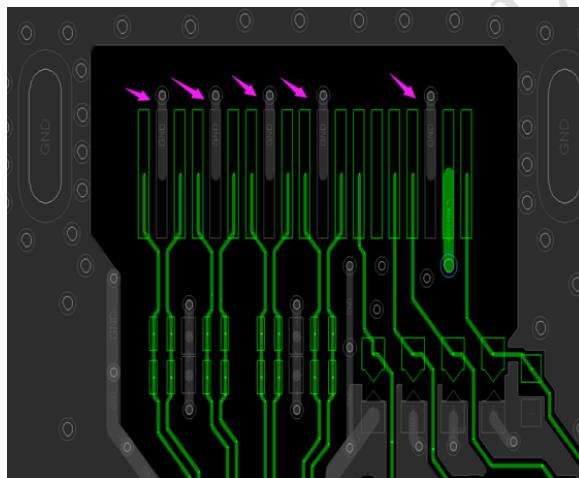


Figure 5-1 ESD protection schematic: isolate the HDMI signal from GND at the surface layer

5.4 EMI Protection

- Electromagnetic interference (EMI) involves three elements: the source of interference, the coupling path, and the sensitive device. Since we cannot deal with the sensitive equipment, we can only address EMI by tackling the interference source and the coupling channel. The best approach to solving EMI issues is eliminating the interference source. If that is not possible, efforts should be made to cut off the coupling path or avoid antenna effects.
- It is generally difficult to completely eliminate interference sources on the PCB. However, methods such as filtering, grounding, balancing, impedance control, and signal quality improvement (e.g., termination) can be employed. These methods are usually combined, but good grounding is the fundamental requirement.
- Common materials used for EMI mitigation include shielding covers, specialized filters, resistors, capacitors, inductors, ferrite beads, common mode inductors/ferrite cores, absorbing materials, and spread spectrum devices.

- Principles for selecting filters: If the load (receiver) has high impedance (common for single-ended signal interfaces like SDIO, RGB, CIF, etc.), capacitive filter components should be chosen and integrated into the circuit. If the load (receiver) has low impedance (e.g., power output interfaces), inductive filter components should be chosen and placed in series with the circuit. The use of filter components should not cause the signal quality to exceed the permissible range for signal integrity (SI). Common mode inductors are typically used to suppress EMI in differential interfaces.
- Shielding measures on the PCB require proper grounding; otherwise, radiation leakage or antenna effects may occur. The shielding of connectors should comply with relevant technical standards.
- RK3576 spread spectrum should be module-based. The degree of spread spectrum should be determined based on the signal requirements of the relevant sections. Refer to the RK3576 spread spectrum documentation for specific measures.
- Matching resistors should be retained for all cascaded clocks to provide matching impedance and improve signal quality.
- For DC power input, if conditions permit, it is advisable to reserve power common mode inductors or EMI filters.
- Additional common mode inductors or filtering circuits should be added to interfaces such as USB, HDMI, VGA, and display connectors.
- When using heat sinks, be aware that they can also couple EMI energy and cause radiation. In addition to meeting thermal design requirements, heat sinks should also meet EMI testing requirements. Grounding provisions should be made for heat sinks, and when grounding is required, the heat sink should be properly grounded. The number and selection of grounding points in this area cannot be determined precisely and should be adjusted based on actual testing in the laboratory with the first version of the hardware.
- The requirements for layout in terms of EMI are highly consistent with those for ESD. Most of the ESD layout requirements mentioned earlier apply to EMI protection. In addition, the following requirements should be added:
 - Strive to ensure signal integrity.
 - Differential lines should be matched in length and tightly coupled to ensure the symmetry of differential signals, minimizing the displacement of differential signals and avoiding the generation of common-mode signals that can cause EMI issues.
 - Components with metal enclosures, such as plug-in devices, should be designed to avoid coupling interference signals that can cause radiation. Also, avoid coupling interference signals from the device's enclosure to other signal lines.
 - Matching resistors for all cascaded clocks should be located near the CPU (source) end. The routing between the CPU pins and the resistors must be controlled within 400 mils.
 - If the PCB has more than 4 layers, it is recommended to route all clock signals on internal layers as much as possible.
 - Prevent power radiation by reducing the coverage of the power plane copper. The copper coverage of the power plane should be reduced by one H (the thickness of the dielectric between the power and ground planes), and it is recommended to reduce it by 20H.

6 Soldering Process

6.1 Overview

RK3576 are ROHS certified products, that is, they are all Lead-free products. This chapter regulates basic temperature settings of each period when customers use the chipset to SMT. It mainly introduces process control when using RK3576 chipset to do reflow soldering: lead-free process and mixed process.

6.2 Terms Interpretation

Terms in this chapter are explained below:

- Lead-free: Lead-free process;
- Pb-free: Pb-free process, all devices (main board, all ICs, resistors and capacitors, etc.) are lead-free devices, and the lead-free solder paste are used in the pure lead-free process;
- Reflow profile: reflow soldering
- Restriction of Hazardous Substances (ROHS): instructions for restricting use of certain hazardous components in electrical and electronic equipment;
- Surface Mount Technology(SMT);
- Sn-Pb: Sn-Pb mixing process refers to using lead solder paste and a mixed soldering process with both lead-free BGA and lead IC.

6.3 Reflow Soldering Requirements

6.3.1 Solder Paste Composition Requirements

The proportion of solder alloy and flux is 90%: 10%; volume ratio: 50%: 50%, solder paste refrigerating temperature is 2~10°C, it should be returned to normal temperature before use, and the return time should be 3~4 hours and the time should be recorded.

The solder paste needs to be stirred before brushing, manual stirring for 3 to 5 minutes or mechanical stirring for 3 minutes. After stirring, it will flow naturally.

6.3.2 SMT Profile

Since RK3576 chipset are made of environmental protection materials, Pb-Free process is recommended. The reflow profile shown below is only recommended for JEDEC J-STD-020D process requirements, and customers need to adjust according to actual production conditions.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidus temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body temperature (T_p)*	See classification temp in Table 4.1	See classification temp in Table 4.2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
 ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Figure 6-1 Reflow Soldering Profile Classification

Package Thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Figure 6-2 Heat Resistance of Lead-Free Process Device Packages Standard

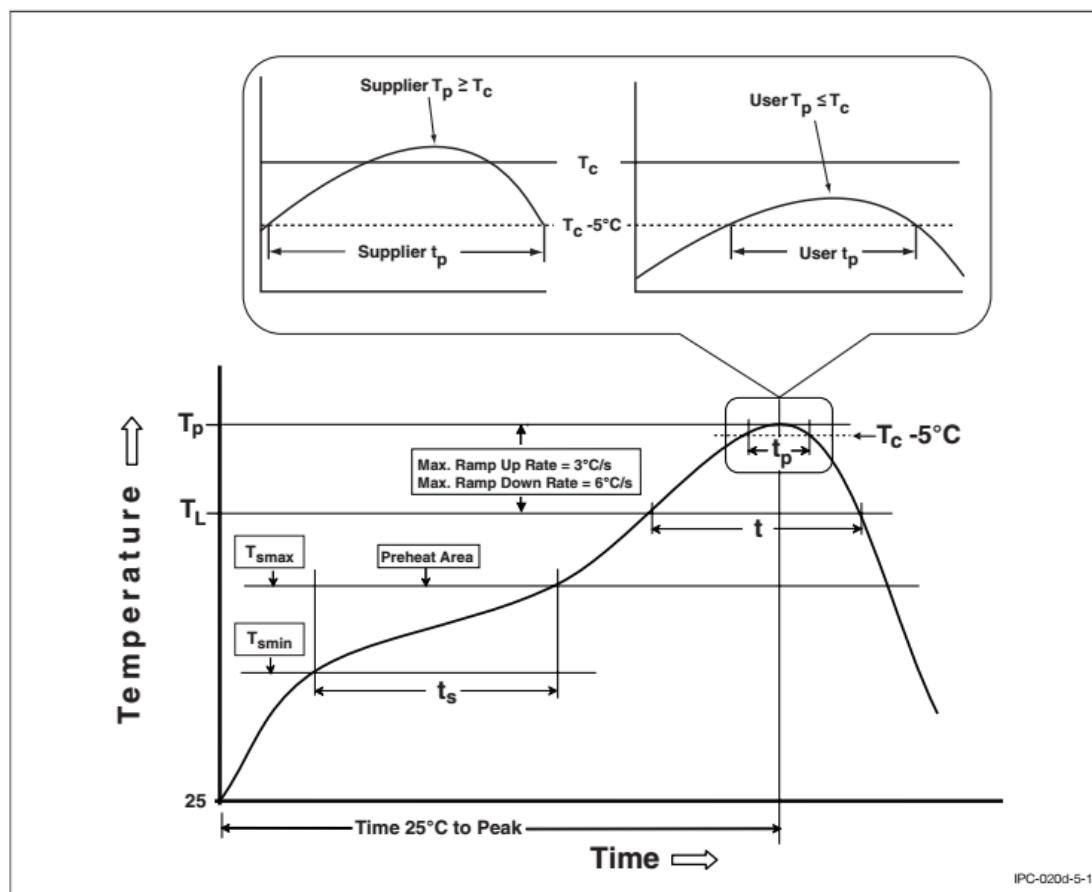


Figure 6-3 Lead-free Reflow Profile

6.3.3 SMT Recommendation Profile

The SMT profile recommended by RK is shown in Figure 6-4. See “RK3576 Production Process Requirements” for details:

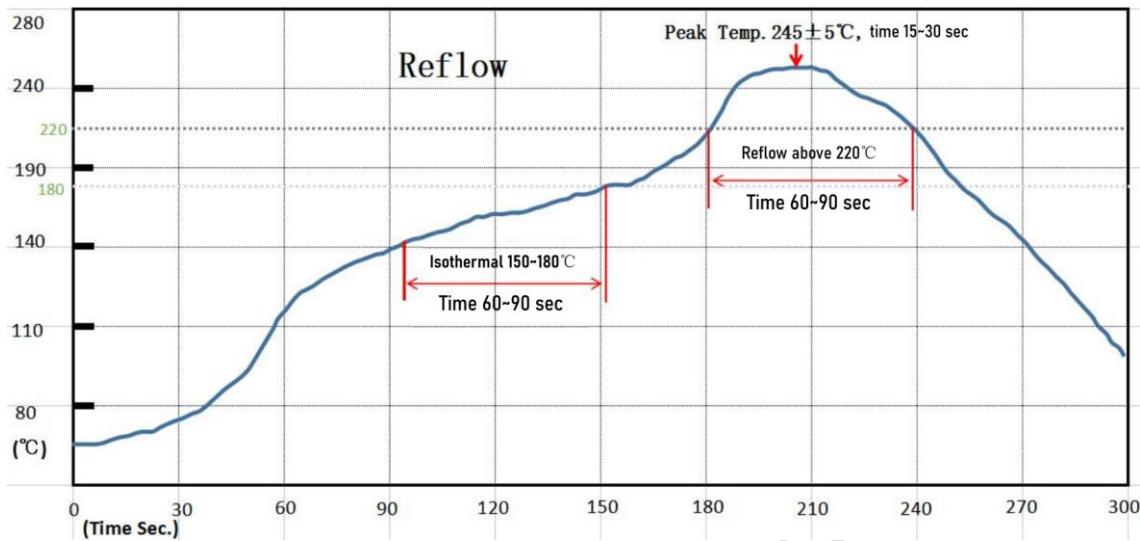


Figure 6-4 Lead-Free Reflow Soldering Process Recommended Profile Parameters

7 Packages and Storage Conditions

7.1 Overview

This chapter introduces the storage and directions for RK3576 usage to ensure the safety and correct usage of products.

7.2 Terms Interpretation

Terms in this chapter are explained below:

- Desiccant: a material used to adsorb moisture
- Floor life: the maximum time products are allowed to be exposed to environment, from before unpacking moisture barrier bag to reflow soldering
- HIC: Humidity Indicator Card
- MSL: Moisture Sensitivity Level
- MBB: Moisture Barrier Bag
- Rebake: to bake again
- Solder Reflow
- Shell Life
- Storage environment

7.3 Moisture Packages

The dry vacuum package material of product is shown as follows:

- Desiccant
- Six-point humidity card
- Moisture barrier bag: aluminum foil, silver opaque, with a mark of moisture sensitivity level

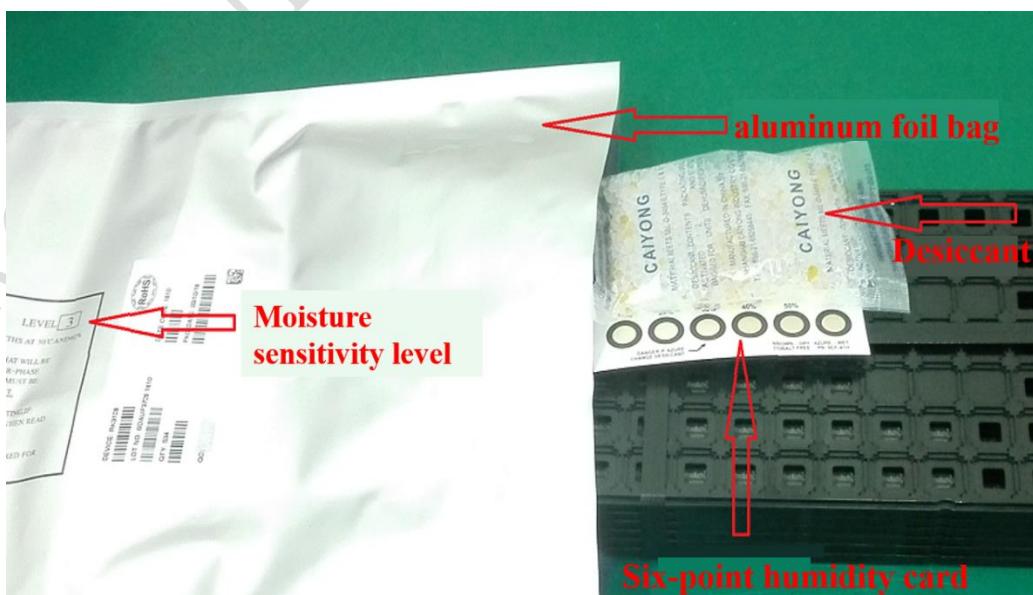


Figure 7-1 Chipset Dry Vacuum Package

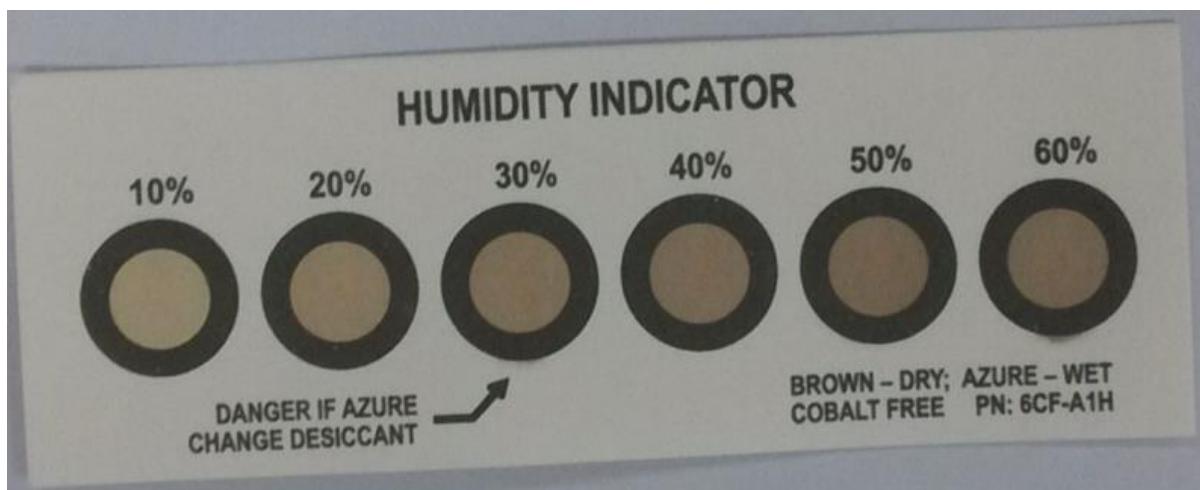


Figure 7-2 Six-Point Humidity Card

7.4 Product Storage

7.4.1 Storage Environment

The product is stored in vacuum packaging, and the storage time can reach 12 months when the temperature is $\leq 40^{\circ}\text{C}$ and the relative humidity is $<90\%$.

7.4.2 Exposure Time

For environmental conditions: $<30^{\circ}\text{C}$ and humidity 60%, please refer to Table 7-1 below.

The MSL level of RK3576 chipset is 3 and is very sensitive to humidity. If package is not used in time after unpacking, and if it is not baked and directly SMT after being left for a long time, there will be a high probability of chip failure.

Table 7-1 Moisture Sensitivity Levels (MSL)

MSL Level	Exposure time Factory environmental conditions: $\leq 30^{\circ}\text{C} / 60\% \text{RH}$
1	Unlimited at $\leq 300^{\circ}\text{C} / 85\% \text{RH}$
2	1 year
2a	4 week
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use, and must be reflowed within the time limit specified on the label.

7.5 Usage of Moisture Sensitive Products

After RK3576 packages are opened, it must meet the following conditions before reflow soldering:

- Continuous or cumulative exposure time is within 168 hours, and factory environment is $\leq 30^{\circ}\text{C}/60\%$

RH;

- Stored in <10% RH environment;

Chips must be baked to remove internal moisture under the following conditions to avoid layered or popcorn problems during reflow:

- When humidity indicator card is at $23\pm5^{\circ}\text{C}$, >10% points have changed color. (Please refer to humidity indicator cards for color change);
- Does not meet the specifications of 2a or 2b;

Please refer to Table 7-2 below for the time for chip re-baking:

Table 7-2 RK3576 Re-bake Reference Table

Package Body	MSL	High Temp Bake @125°C +10/-0°C		Medium Temp Bake @90°C +8/-0°C		Low Temp Bake @40°C +5/-0°C	
		Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h
Thickness ≤ 1.4mm	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days



Note

The Table shows the minimum baking time necessary after damp.

Low temperature baking is preferred.