Schematics Only for RK3576 DEMO1

RK_TABLET_DEMO1_RK3576_LP4XD200P132SD6_V12

Main Functions Introduction

1) PMIC: 1 x RK806S-5 + DiscretePower
2) RAM: 1 x LPDDR4x 32bit(Option 1 x LPDDR4 32bit)
3) ROM: 1 x eMMC5.1 + 1 x UFS
4) Support: 1 x Micro SD Card3.0
5) Support: 1 x USB TYPEC + 1 x USB2.0 Host
6) Support: 7 x SARADC + 1 x SARADC only for boot
7) Support: 1 x 2Lanes MIPI DCPHY RX Camera
8) Support: 1 x 4Lanes MIPI DPHY RX Camera
9) Support: 1 x 4Lanes MIPI DSI with Touch Connector
10) Support: 1 x a/b/g/n/ac/ax 2T2R PCIe WIFI6+ UART/PCM BT
11) Support: 1 x Headphone +2PA + 1 x Analog MIC
12) Support: 1 x MIC Connector
13) Support: 1 x G-Sensor
14) Support: Array Key(VOL+,VOL-)

Note:

The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic.
If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

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Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	00.Cover Page				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	1 of 50

Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. NC stands for component not mounted temporarily
2. If Value or option is NC, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

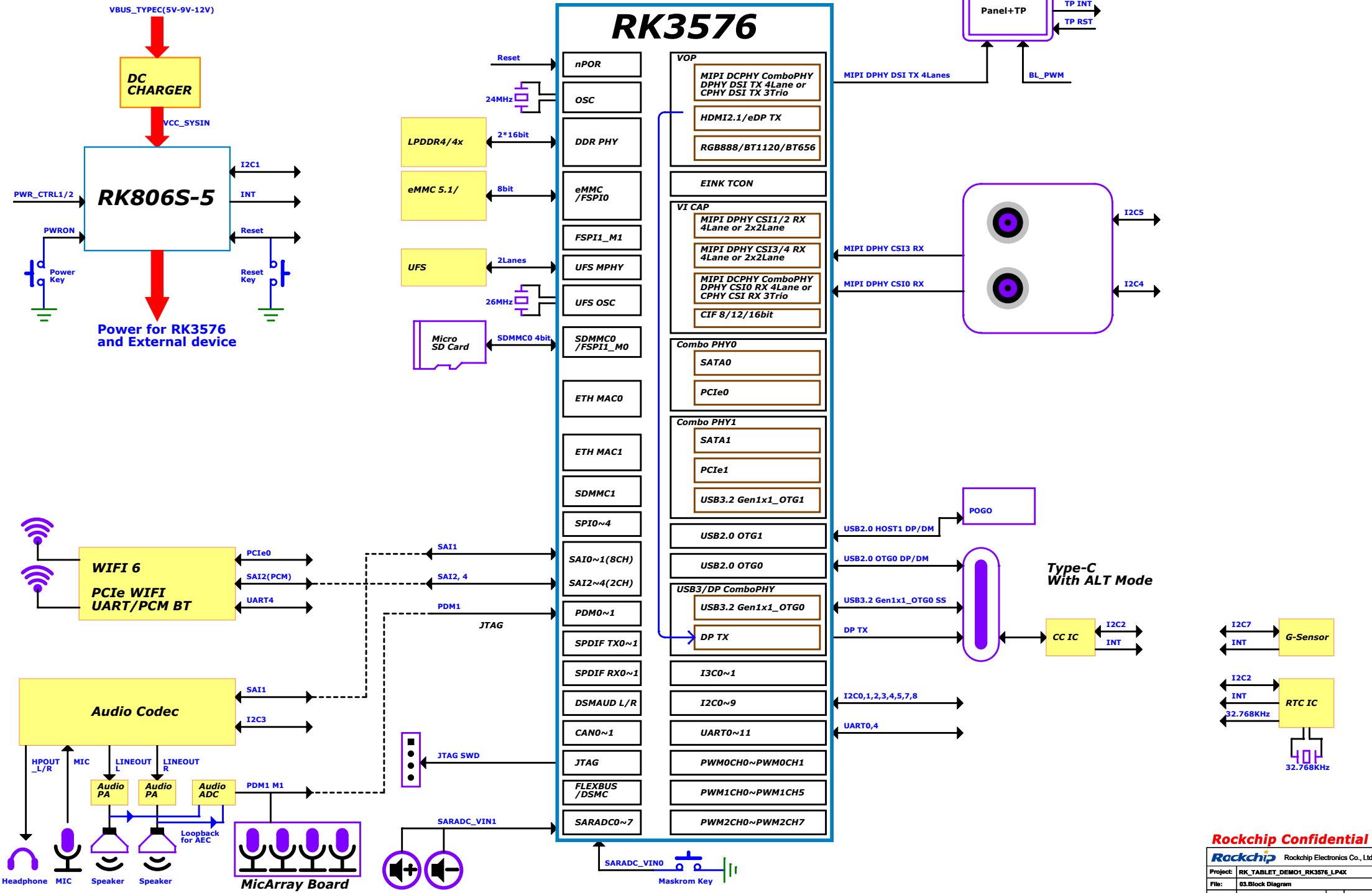
Rockchip Electronics Co., Ltd					
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	01.Index and Notes				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	2 of 50

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2023-12-14	Mark.Ye	1: Revision preliminary version;	
V1.1	2024-04-28	Mark.Ye	1: R7400 R7401 R7403 R7404 100K 改为20K; C7404 C7406 C7415 C7417 10nF改为100nF; 2: C4712 100nF改为NC； 3: NPU GPU电源22uF电容从RK806S-5移到靠近RK3576； 4:删除预留的C1006 C1012 C1020；	
V1.2	2024-05-30	Mark.Ye	1: PLDO2时序从slot3改为slot5； 2: SARADC_AVDD1V8供电改为默认从VCCA1V8_PLDO2_S0供电; 3: CAMERA 1.8V供电改成外挂LDO； 4: CPU_LIT的滤波电容C2332改为NC; 5. 删除预留的J9101插座； 6. HP_CTL_H从1.8VGPIO改到3.3V GPIO，以改善音频质量; 7. RK3576的PCB封装修改为BGA698_16R1X17R2X1R08； 8. VCC1V2_UFS_VCCQ_S0的DCDC使能信号调整；	

RK3576 Ref Block Diagram(Typical Application Case)

Rockchip IC | Other IC



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Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_TABLET_DEMO1_RK3576_LP4X
File:	03.Block Diagram
Date:	Thursday, May 30, 2024
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Designed by:	Mark.Ye
Reviewed by:	
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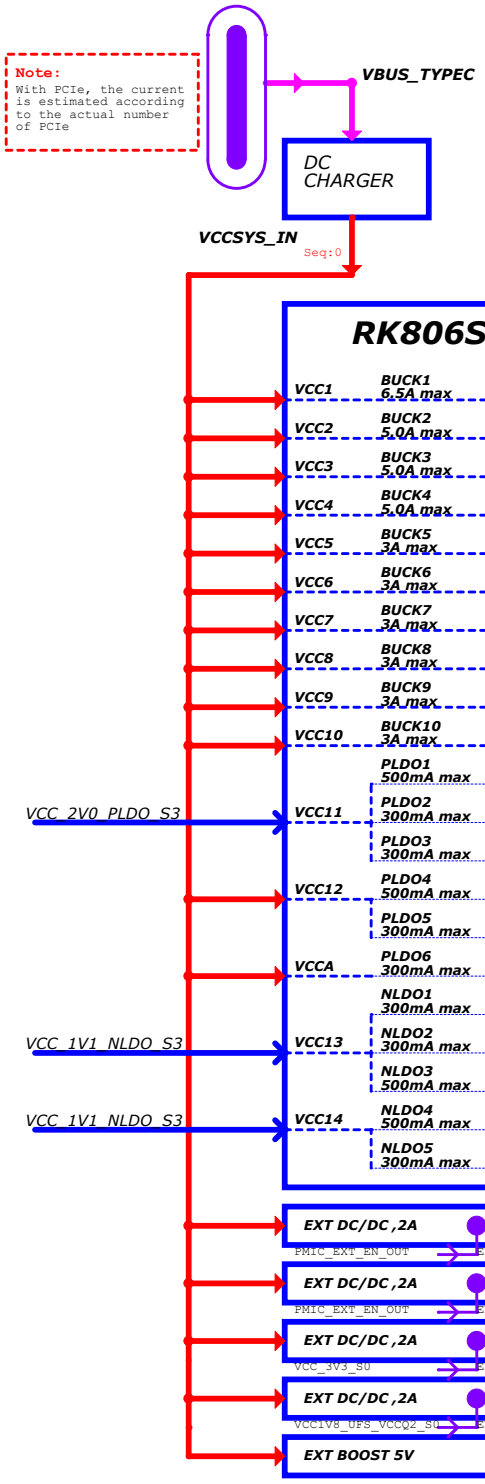
Power Tree

Note: Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

Note: The RK806S-5 LDO power distribution of the reference schematics is only suitable for the interface used in the reference schematics. If other interface functions are to be added to the reference schematics, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Note: With PCIe, the current is estimated according to the actual number of PCIe



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Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_TABLET_DEMO1_RK3576_LP4X
File:	04.Power Diagram
Date:	Thursday, May 30, 2024
Rev:	V1.2
Designed by:	Mark.Ye
Reviewed by:	
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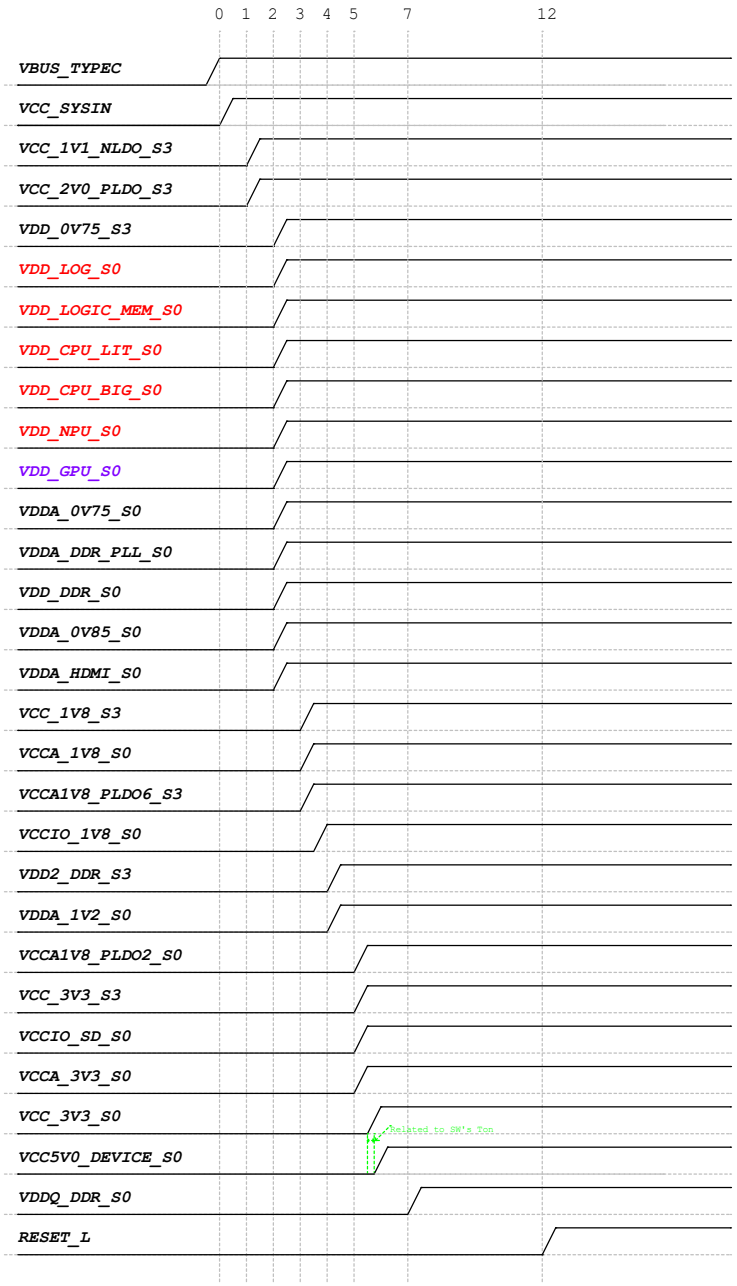
Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC_SYSIN	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC_SYSIN	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC_SYSIN	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC_SYSIN	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC_SYSIN	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC_SYSIN	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC_SYSIN	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_SYSIN	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_SYSIN	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC_SYSIN	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:5	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC_SYSIN	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC_SYSIN	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC_SYSIN	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCCIO_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Note:

The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

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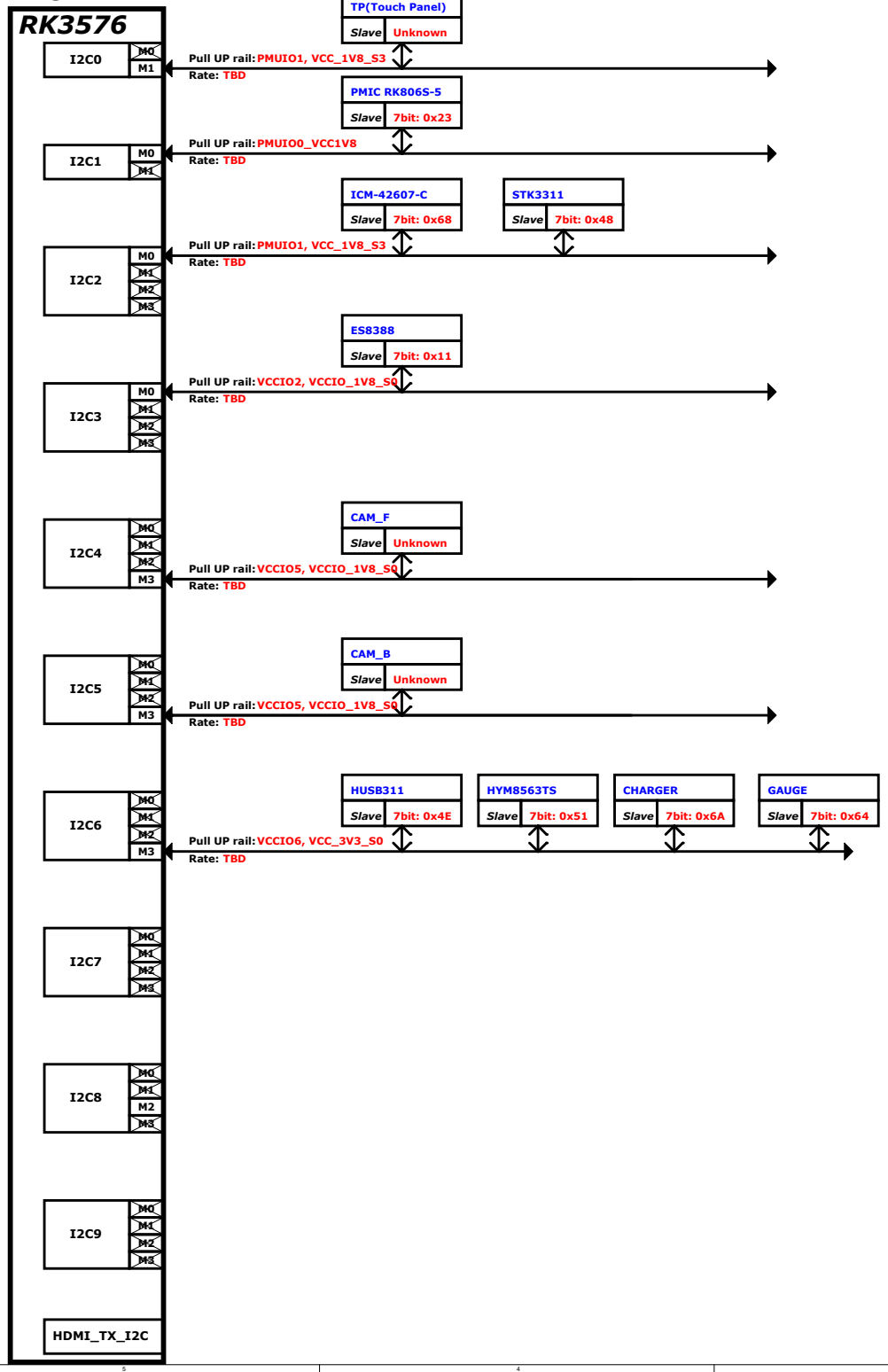
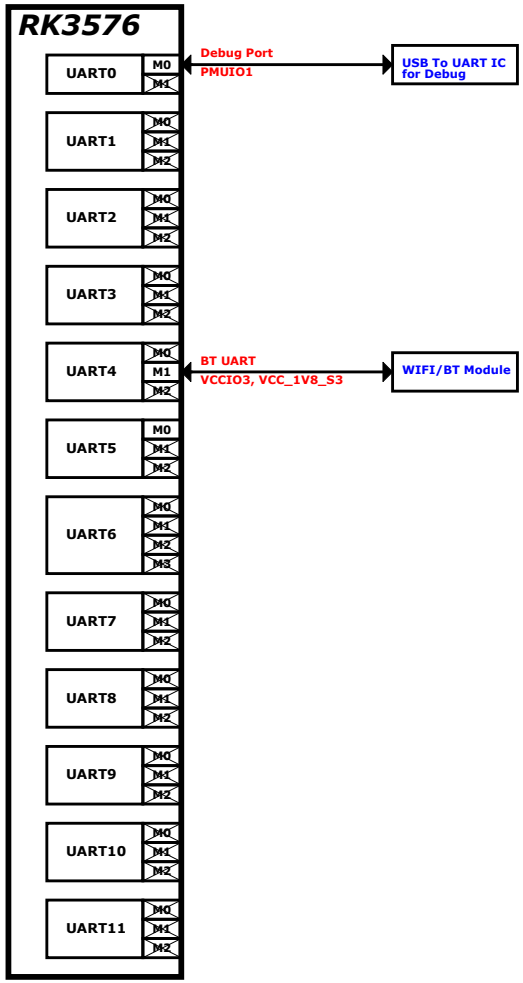
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	05.Power Sequence and Map				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	6 of 50

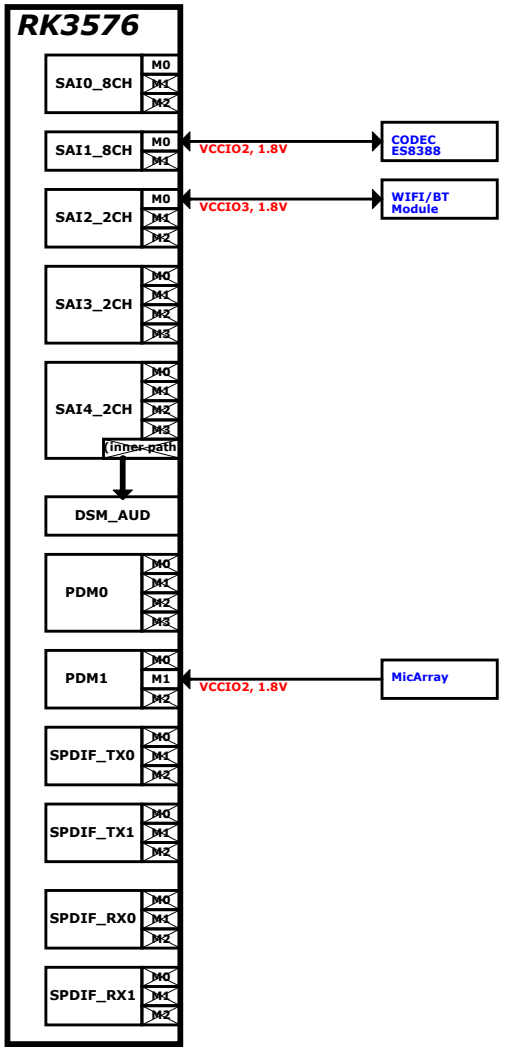
I2C MAP



UART MAP



Audio MAP



Note:

M0 Unselected IOmux path

M1 IOmux path in use

At the same time, only one path can be selected.

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_TABLET_DEMO1_RK3576_LP4X
File:	05.Lower-Speed Bus Map
Date:	Thursday, May 30, 2024
Rev:	V1.2
Designed by:	Mark Ye
Reviewed by:	
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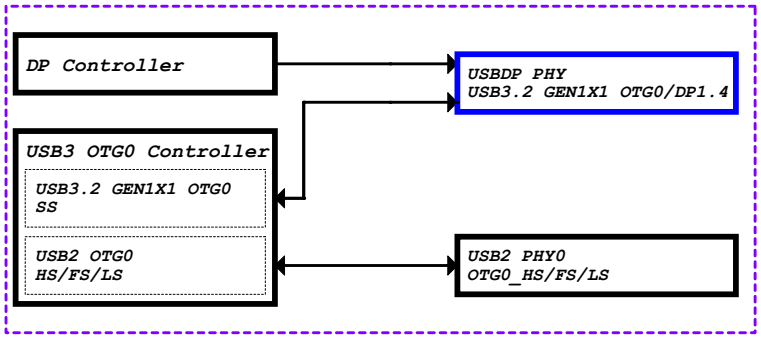
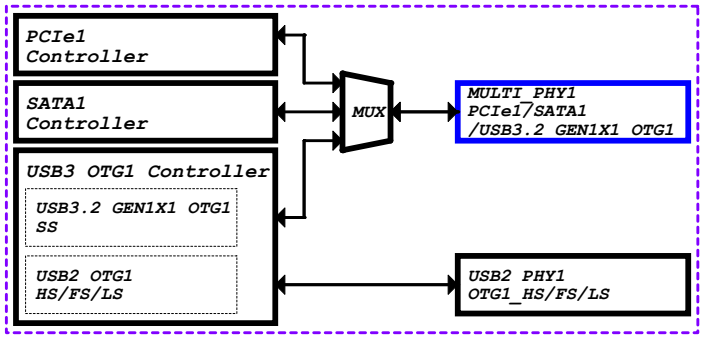
MULTI_PHY Path Map

USBDP PHY--USB3.2 GEN1X1 OTG0/DP1.4



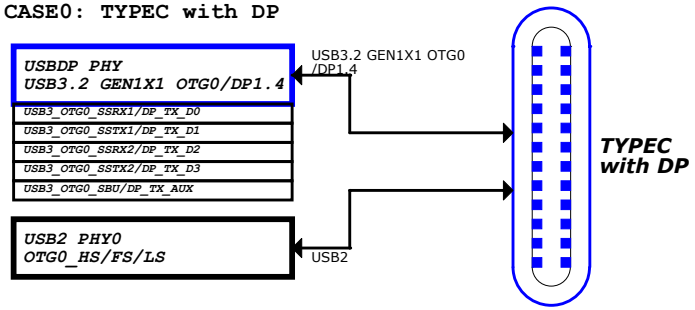
PCIe Combo PHY1--
PCIe1/SATA1/USB3.2 GEN1X1 OTG1



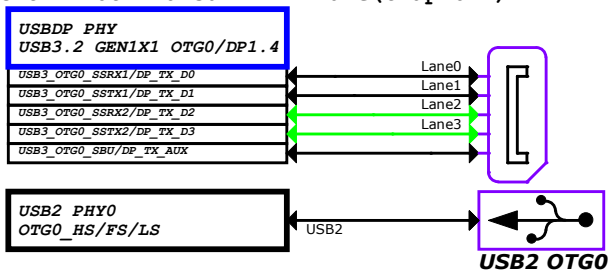
Note:
USB2 PHY1 can only be used when PCIE1/SATA1 is not in use!!!

USB OTG0/DP Application

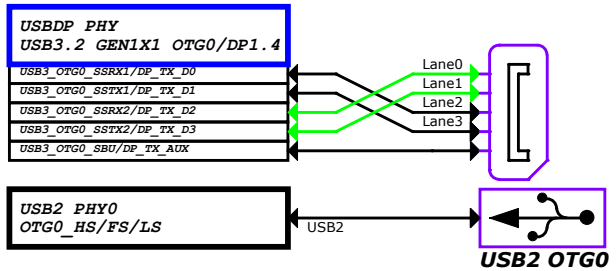
CASE0: TYPEC with DP



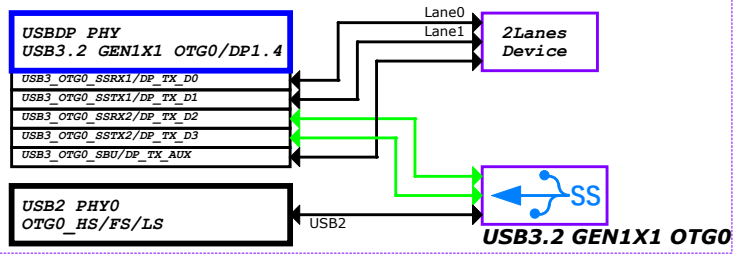
CASE1: USB2 OTG0 + DP 4Lane(Swap OFF)



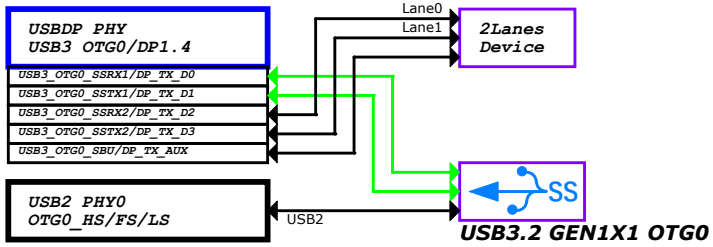
CASE2: USB2 OTG0 + DP 4Lane(Swap ON)



CASE3: USB3.2 GEN1X1 OTG0 + DP 2Lane(Swap OFF)



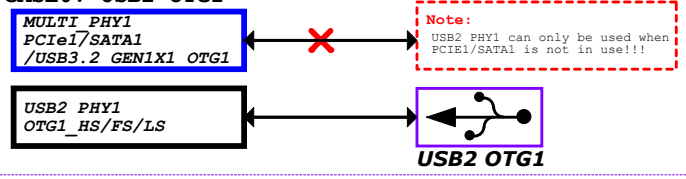
CASE4: USB3.2 GEN1X1 OTG0 + DP 2Lane(Swap ON)



Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

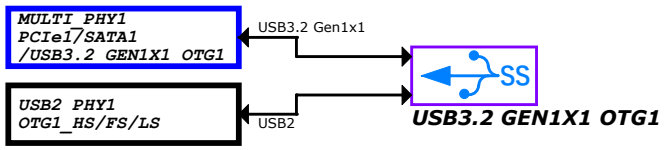
USB OTG1 Application

CASE0: USB2 OTG1



Note:
USB2 PHY1 can only be used when PCIE1/SATA1 is not in use!!!

CASE1: USB3.2 GEN1X1 OTG1



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Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_TABLET_DEMO1_RK3576_LP4X
File:	07.USB/DP Configure Map
Date:	Thursday, May 30, 2024
Rev:	V1.2
Designed by:	Mark.Ye
Reviewed by:	
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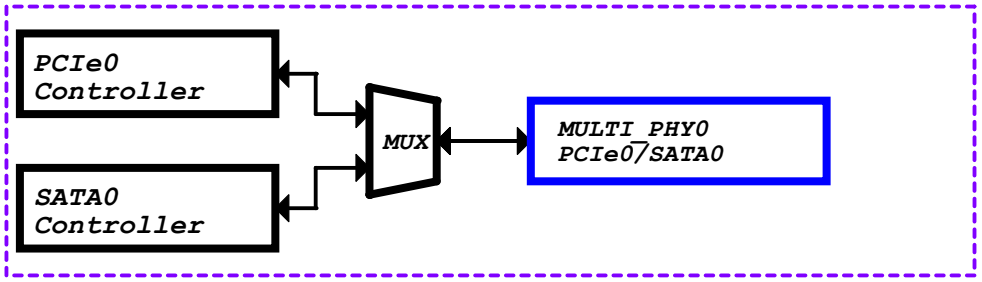
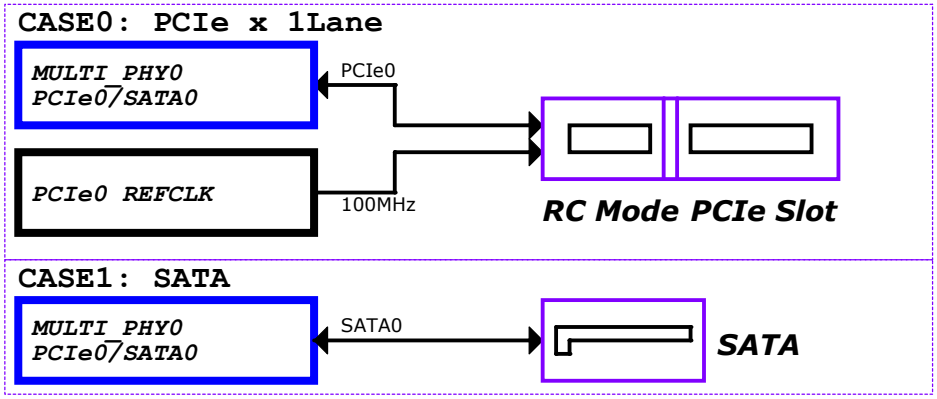
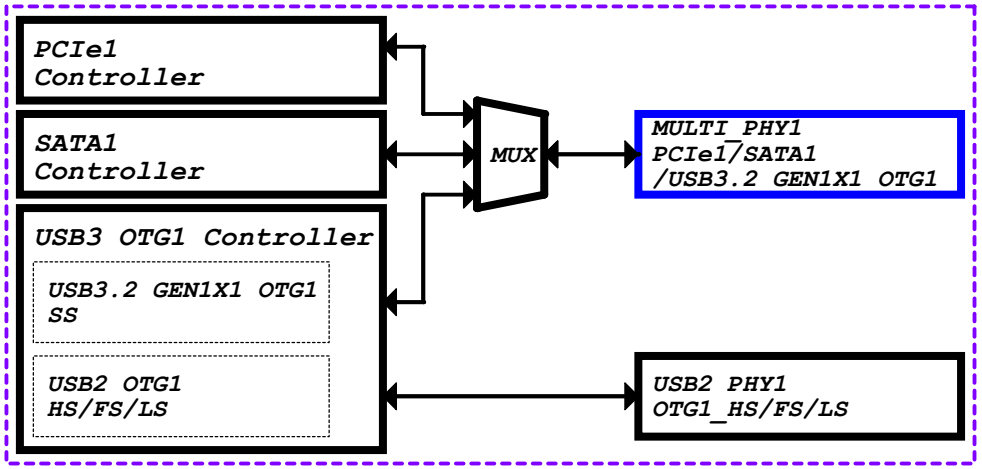
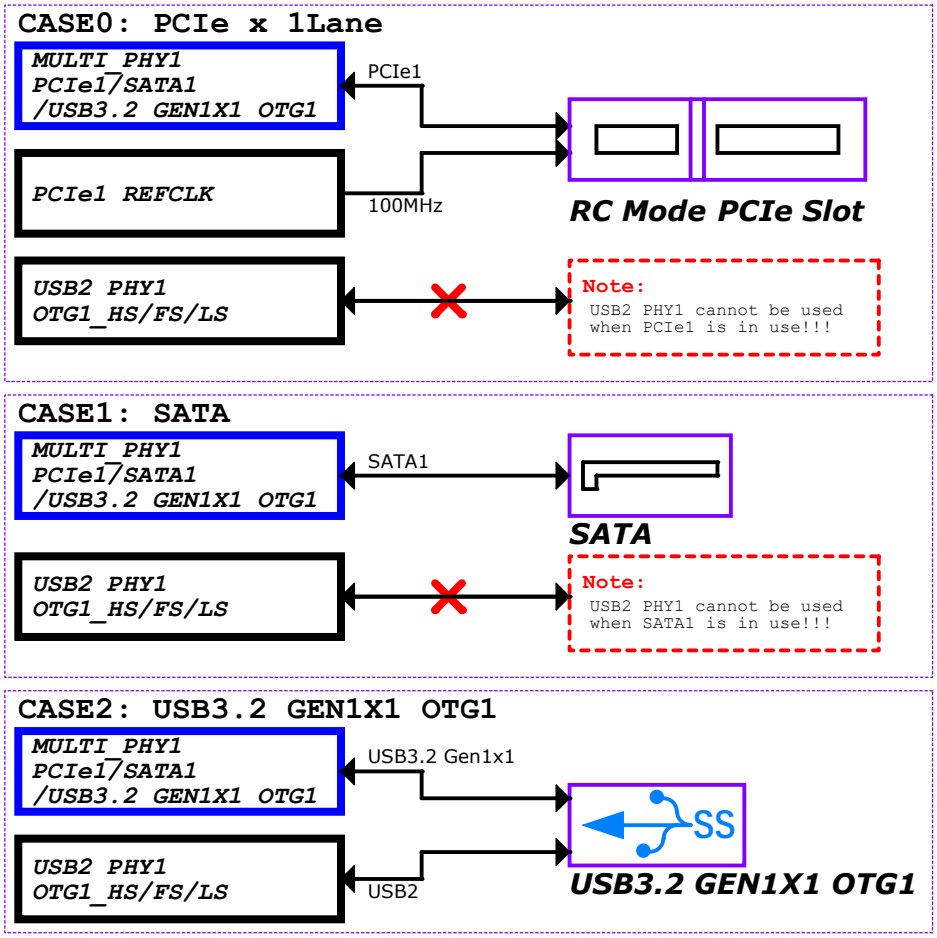
PCIe Combo PHY0--PCIe0/SATA0





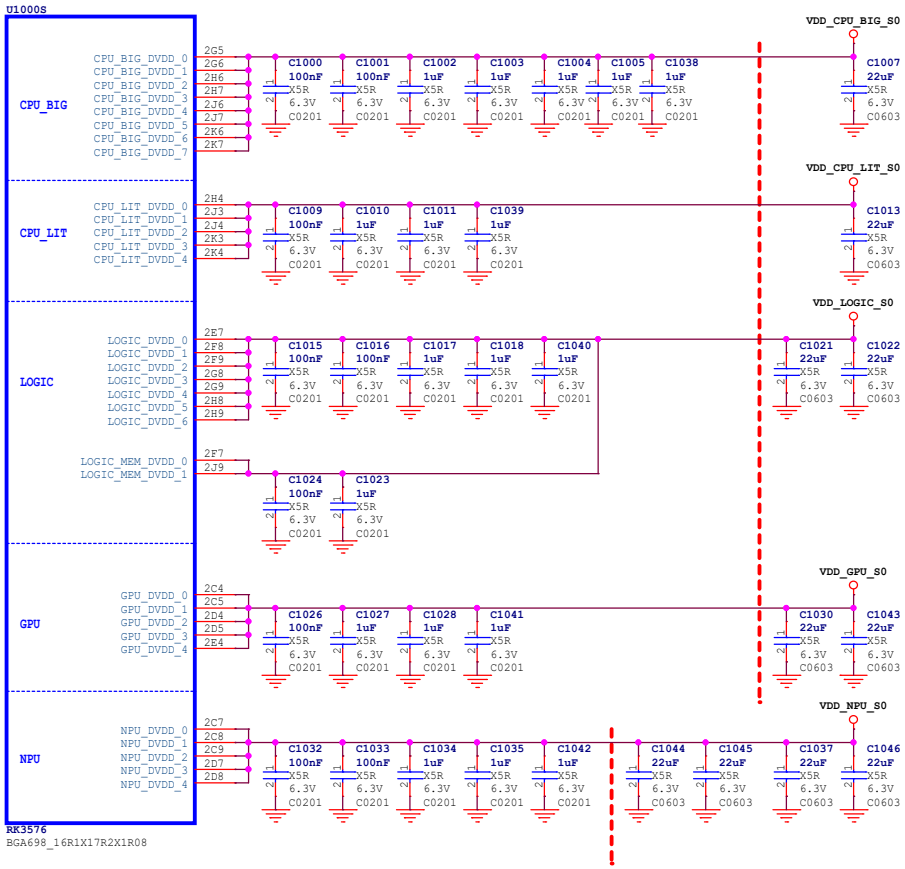
PCIe Combo PHY1--
PCIe1/SATA1/USB3.2 GEN1X1 OTG1





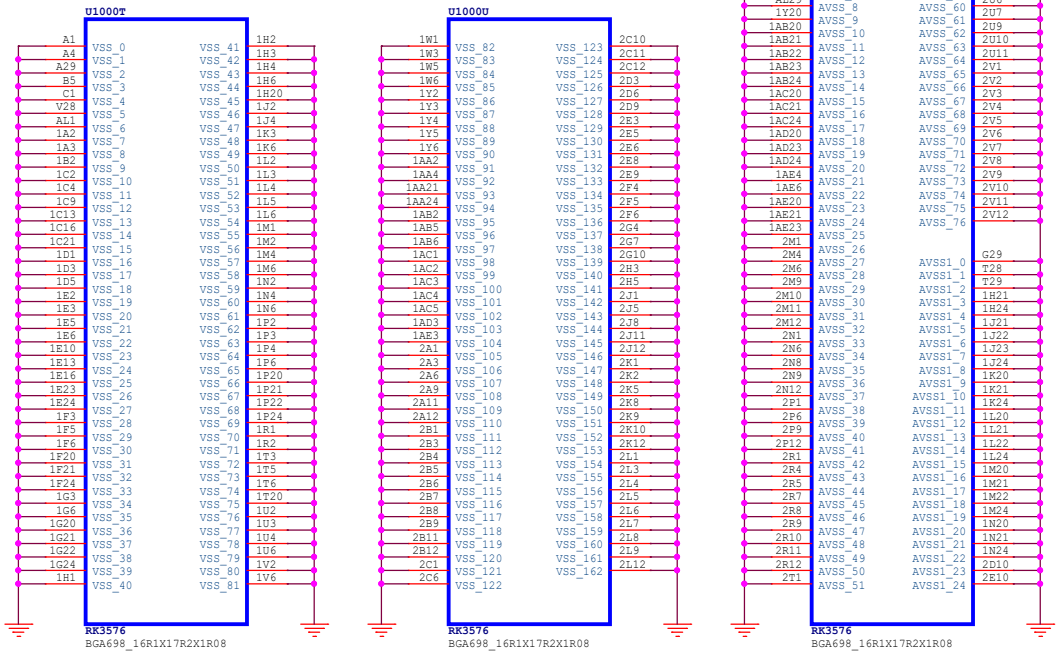
Rockchip Electronics Co., Ltd					
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	08.PCIe Combo PHY Configure Map				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	9 of 49

RK3576_S (Power)



Note:
Caps of between dashed red lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3576_T/U/V (GND)



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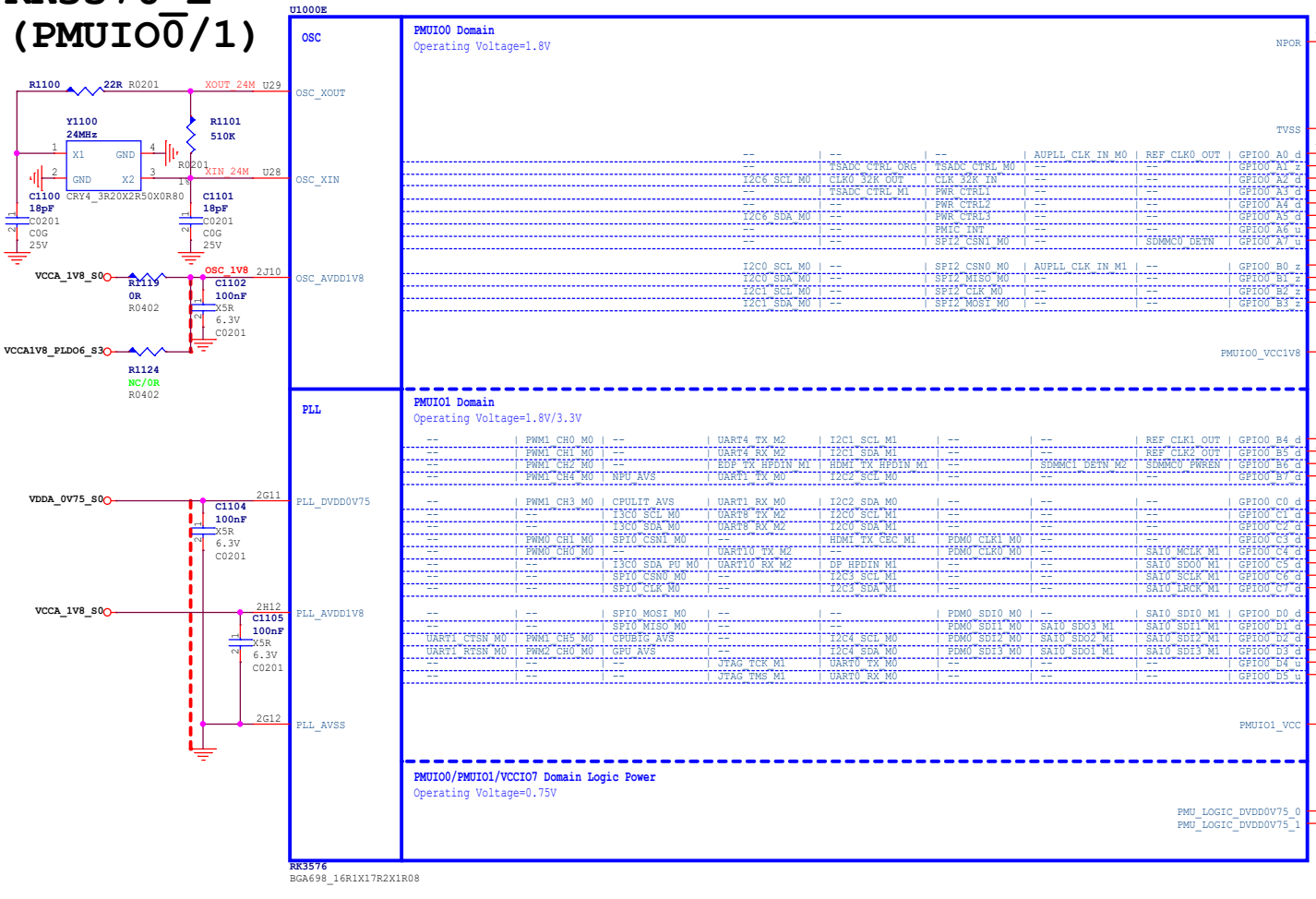
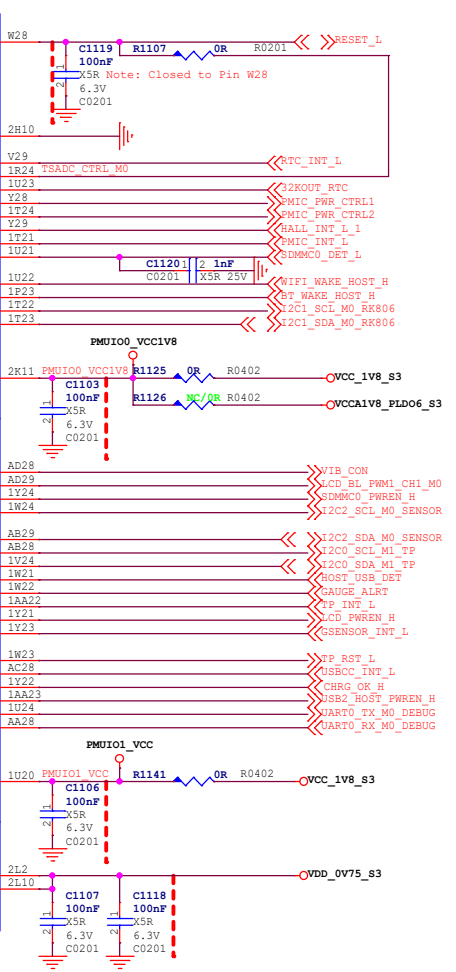
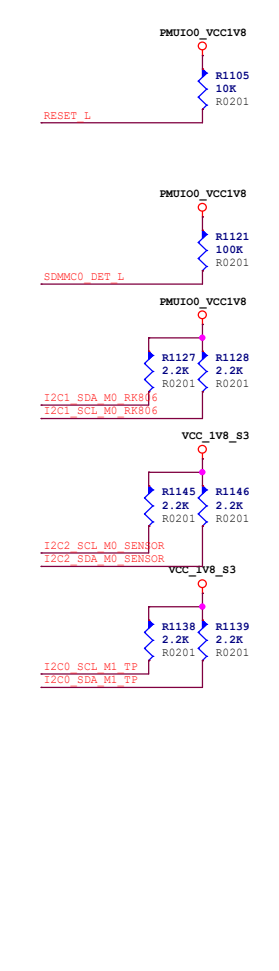
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	10.RK3576-Power/GND				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	11 of 50

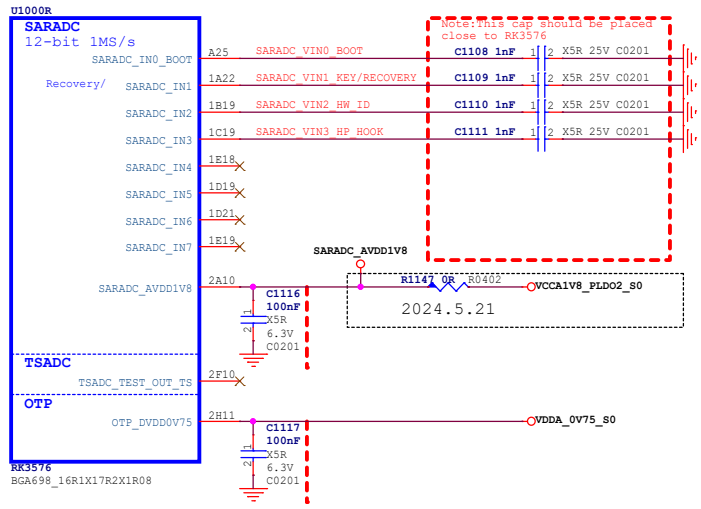
RK3576_E (PMUIO0/1)

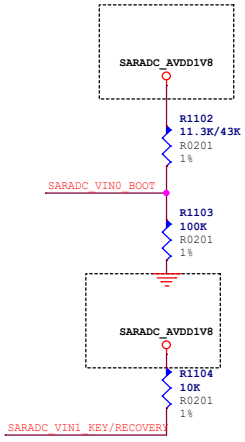






RK3576_R (SARADC)



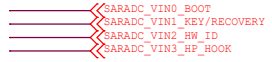


BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

Item	Rup	Rdown	ADC Value	Boot Mode
Config1	DNP	10K	0	USB (Maskrom mode)
Config2	100K	11.3K	416	FSPI0->USB
Config3	100K	24.9K	816	FSPI1_M0->EMMC->USB
Config4	100K	43K	1231	FSPI1_M1->EMMC->USB
Config5	100K	68K	1658	FSPI0->UFS->USB
Config6	100K	100K	2048	FSPI1_M0->UFS->USB
Config7	68K	100K	2438	UFS->USB
Config8	43K	100K	2864	UFS->SDMMC0->USB
Config9	24.9K	100K	3279	RFU
Config10	11.3K	100K	3679	EMMC->SDMMC0->USB
Config11	10K	DNP	4095	EMMC->USB

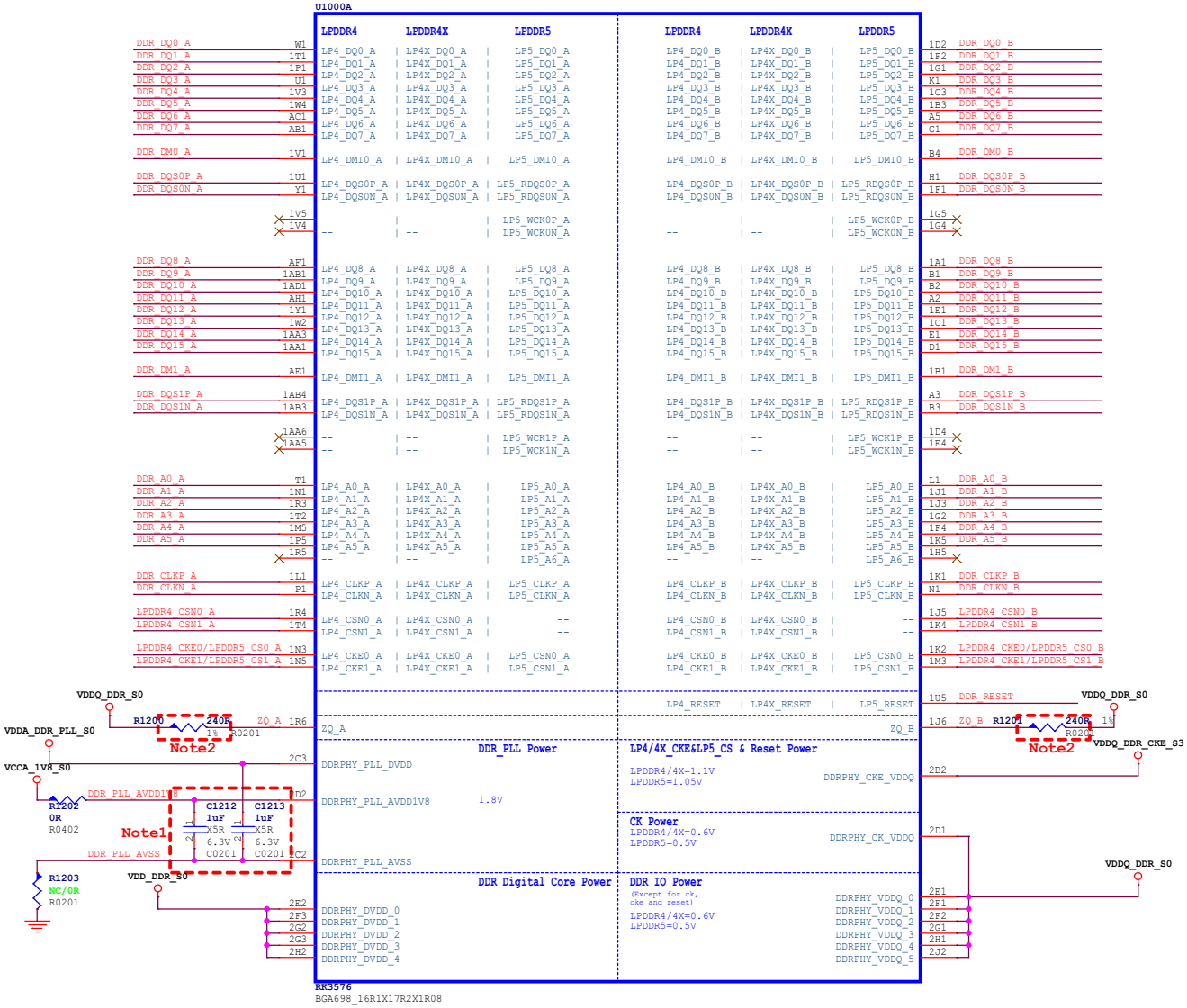
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



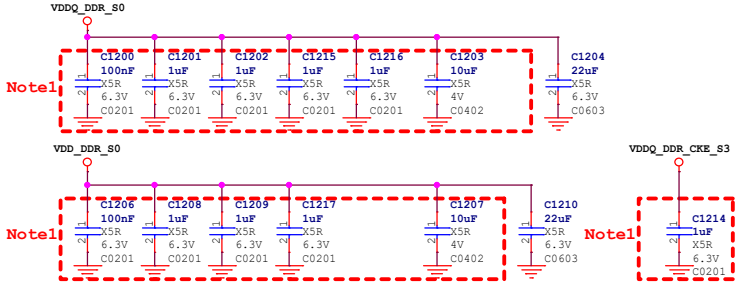
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_TABLET_DEMO1_RK3576_LP4X
File:	11.RK3576-OSC/PLL/PMUIO/SARADC
Date:	Thursday, May 30, 2024
Rev:	V1.2
Designed by:	Mark.Ye
Reviewed by:	
Sheet:	12 of 50

RK3576_A(DDRPHY)



DDR FILTER

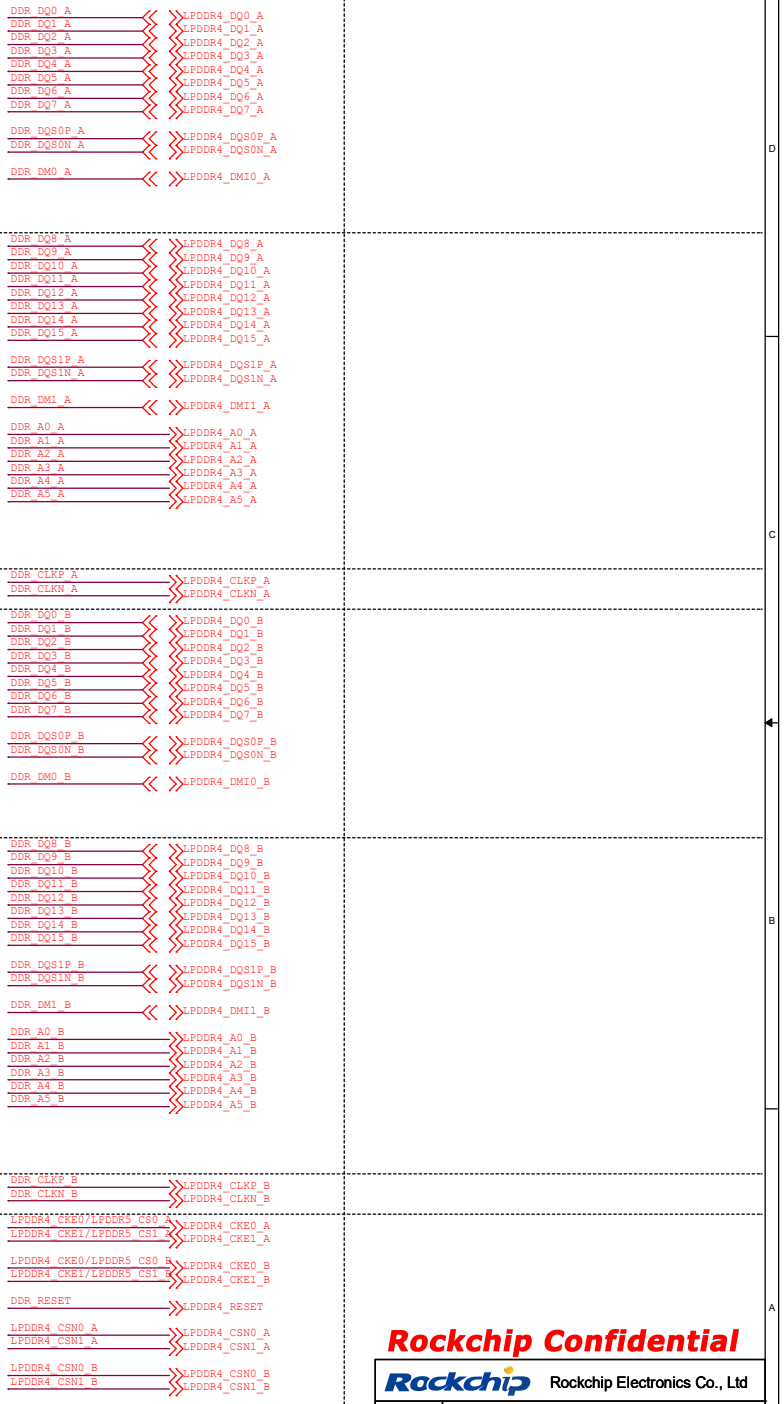


Note:
(1) Power Sequence: VDD-VDDQ_CKE-VDDQ
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

Note1:
Caps in the red line dotted box should be placed under the U1000 package

Note2:
Resistors in the red line dotted box should be placed under the U1000 package

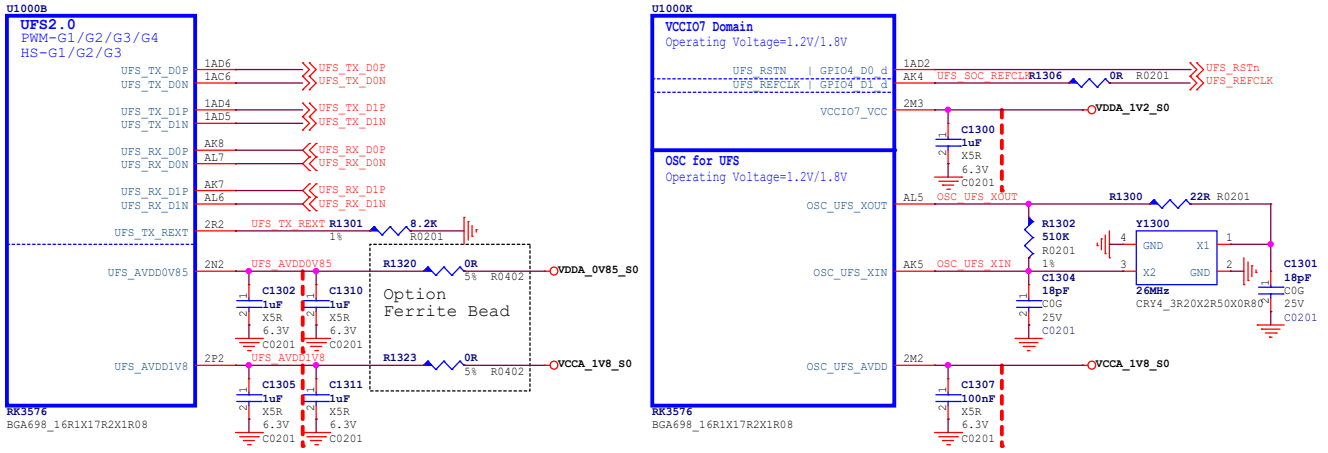
LPDDR4 Signal



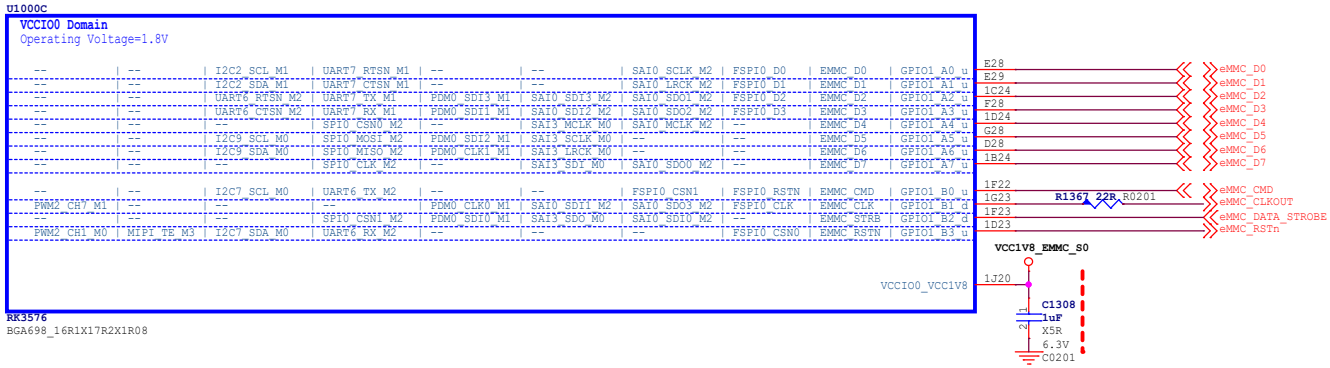
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	12.RK3576-DDR PHY				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	13 of 50

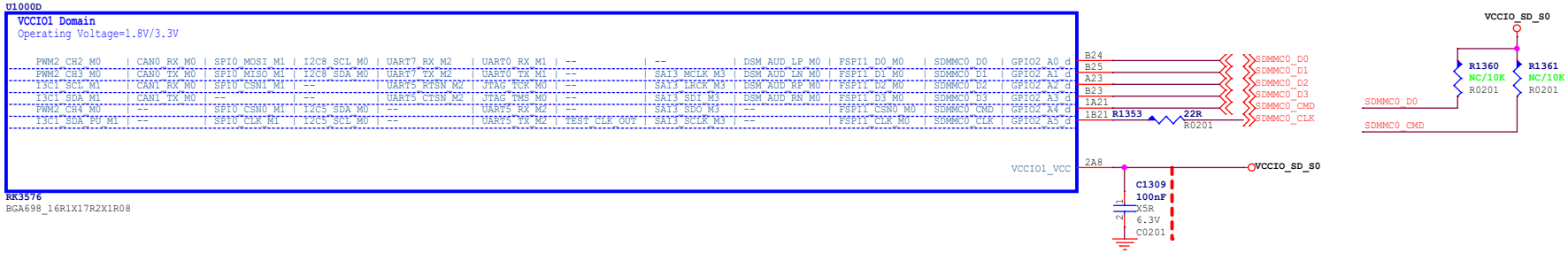
RK3576_B (UFS)



RK3576_C (VCCIO0)



RK3576_D (VCCIO1)



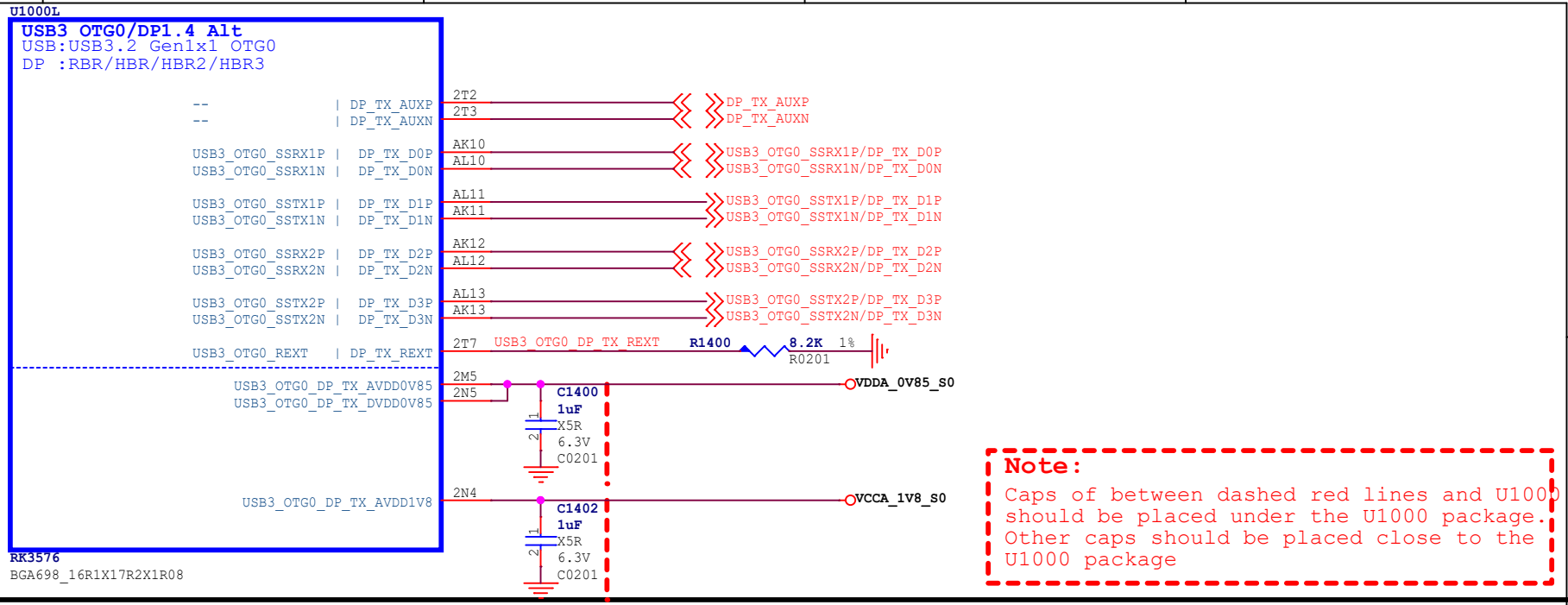
Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Rockchip Confidential

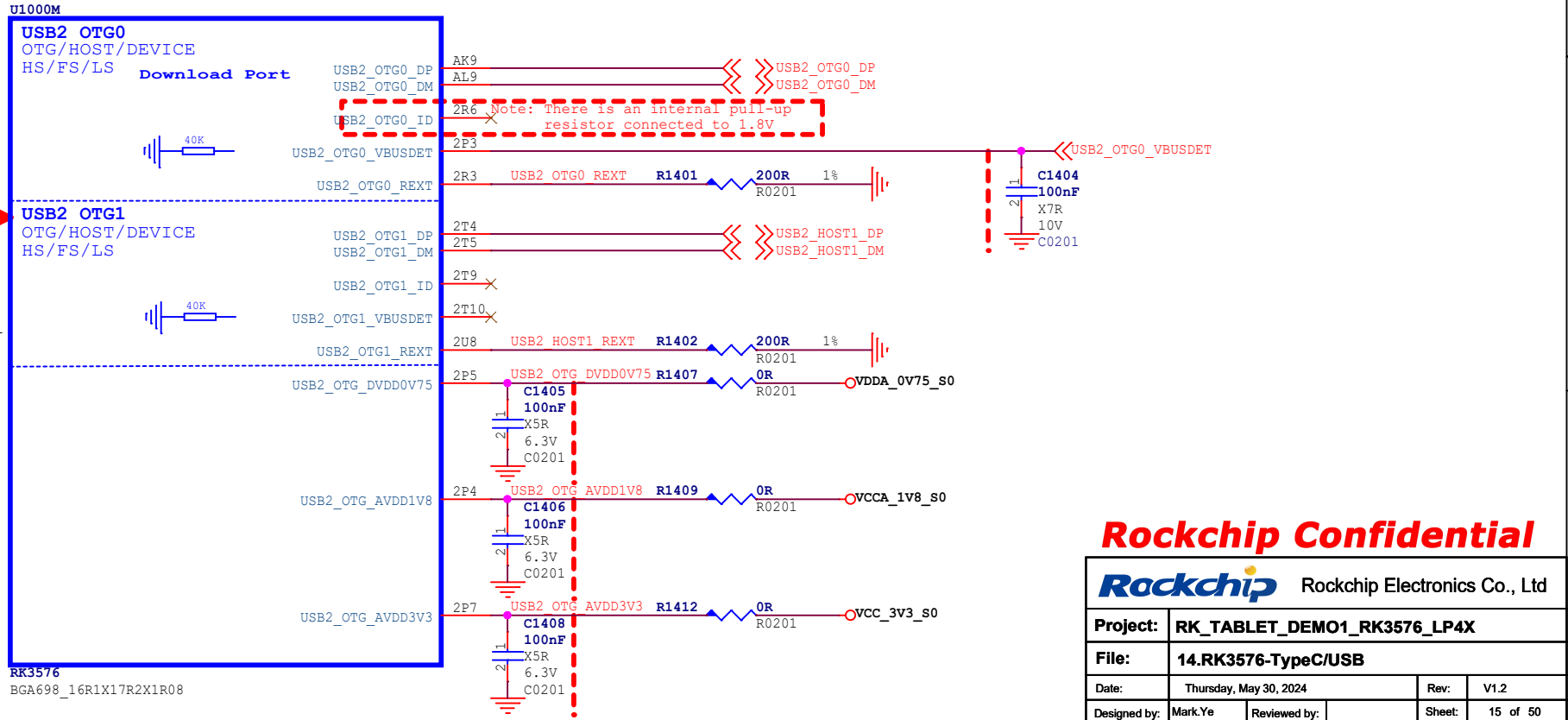
Rockchip Electronics Co., Ltd					
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	13.RK3576-eMMC/UFS/SD				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	14 of 50

RK3576_L (USB3/DP)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_M (USB2)



Note!!!
The USB2 PHY1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected

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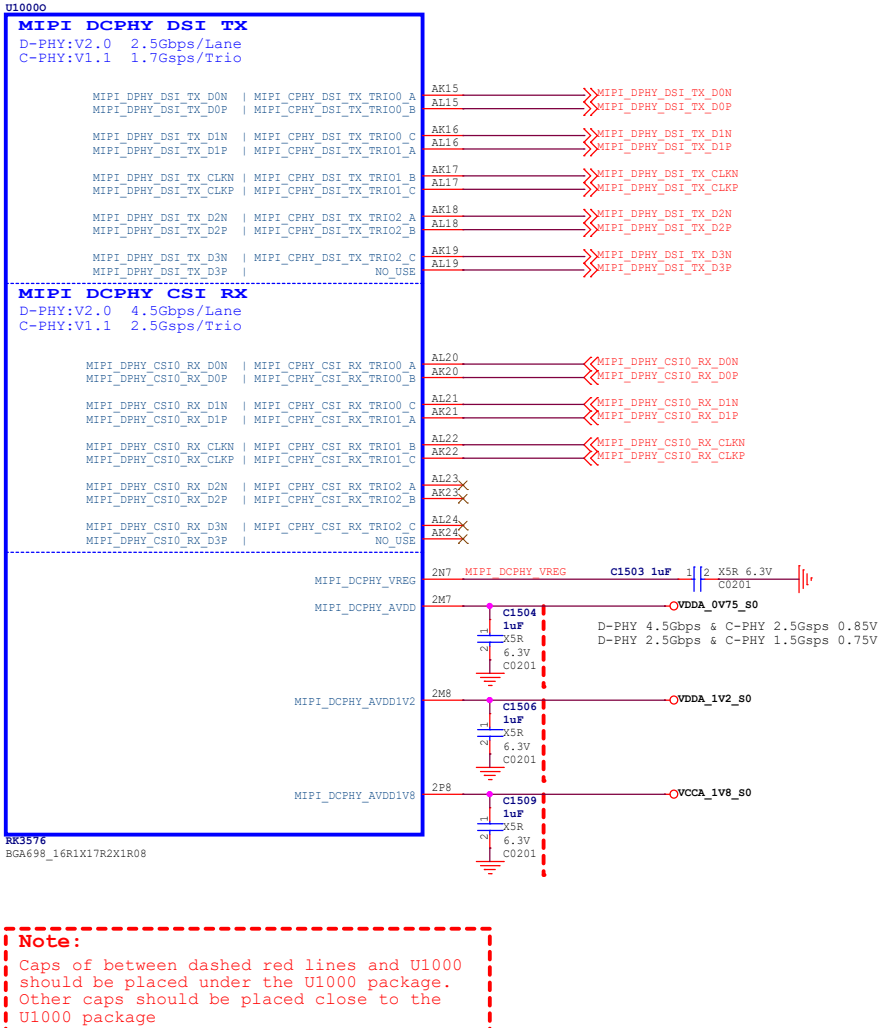
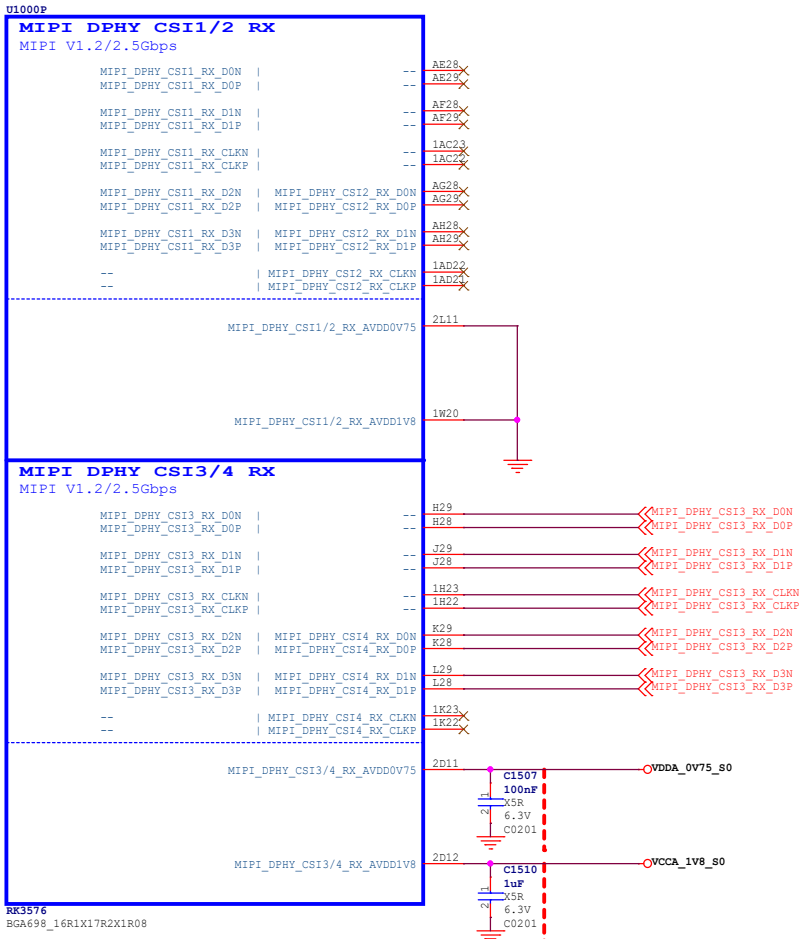
Rockchip Electronics Co., Ltd					
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	14.RK3576-TypeC/USB				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	15 of 50

RK3576_O(MIPI DCPHY)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_P(MIPI DPHY CSI RX)



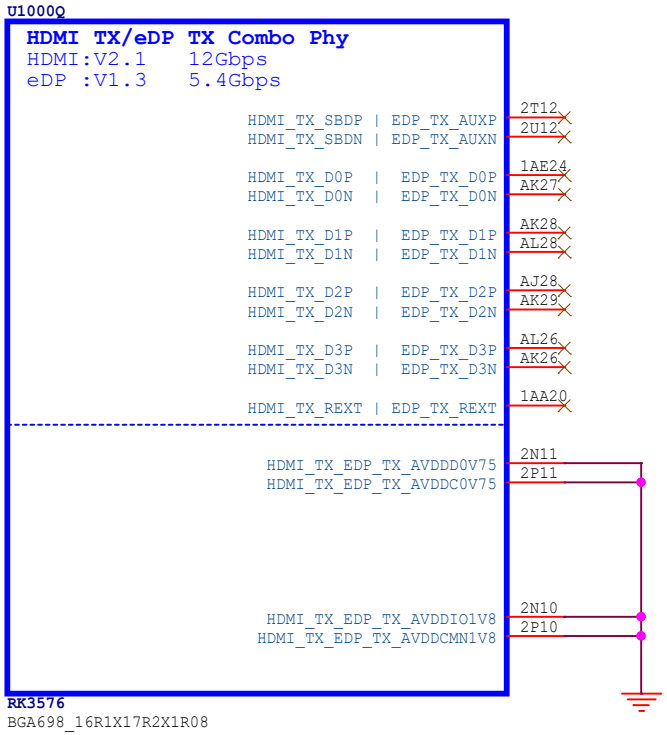
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	15.RK3576-MIPI DSI/CSI				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	16 of 50

RK3576_Q(HDMI/eDP)

Note:
HDMI 2.1 supports up to 4Kx2K@120Hz

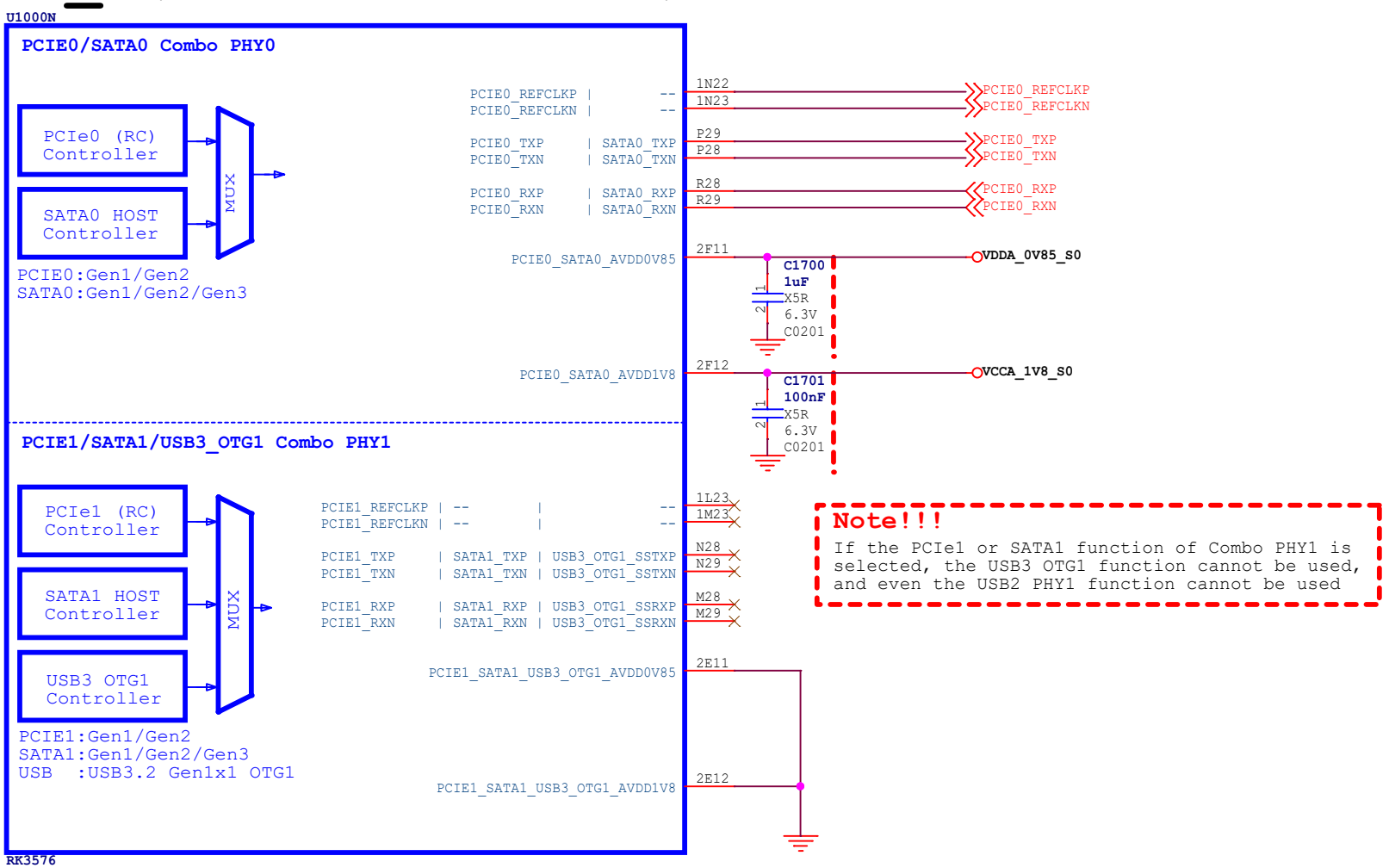


Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	16.RK3576-HDMI/eDP				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	17 of 50

RK3576_N(PCIE/SATA/USB3)



Note!!!

If the PCIe1 or SATA1 function of Combo PHY1 is selected, the USB3 OTG1 function cannot be used, and even the USB2 PHY1 function cannot be used

Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	17.RK3576-PCIE/SATA/USB3				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	18 of 50

RK3576_F(VCCIO2)

U1000F

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

PWM2_CH5_M0	--	--	--	--	AUPLL_CLK_IN_M2	SAI4_MCLK_M0	SAI1_MCLK_M0	GPIO4_A2_d
PWM2_CH4_M1	--	I2C2_SCL_M2	UART5_RTSN_M1	SPI3_CSN0_M2	FLEXBUS1_CSN_M4	--	SAI1_SCLK_M0	GPIO4_A3_d
CAN0_TX_M2	--	I2C4_SCL_M1	UART6_TX_M0	SPI3_MOSI_M2	FLEXBUS0_D13_M1	PDM1_SDI3_M1	SAI4_SCLK_M0	GPIO4_A4_d
--	PCIE1_CLKREQN_M2	I2C2_SDA_M2	UART5_CTSN_M1	SPI4_CSN1_M2	FLEXBUS1_D12_M1	--	SAI1_LRCK_M0	GPIO4_A5_d
CAN0_RX_M2	--	I2C4_SDA_M1	UART6_RX_M0	SPI3_MISO_M2	FLEXBUS0_D14_M1	PDM1_CLK0_M1	SAI4_LRCK_M0	GPIO4_A6_d
PWM2_CH6_M0	--	--	--	SPI3_CLK_M2	--	--	SAI4_SDI_M0	SAI1_SDO0_M0	GPIO4_A7_d
--	UART2_RTSN_M1	UART6_RTSN_M0	UART5_TX_M1	SPI4_CLK_M2	FLEXBUS1_D13_M1	PDM1_CLK1_M1	SAI1_SDI3_M0	SAI1_SDO1_M0	GPIO4_B0_d
--	UART2_CTSN_M1	UART6_CTSN_M0	UART5_RX_M1	SPI4_MOSI_M2	FLEXBUS1_D14_M1	PDM1_SDI2_M1	SAI1_SDI2_M0	SAI1_SDO2_M0	GPIO4_B1_d
--	--	MIPI_TE_M0	--	SPI4_MISO_M2	FLEXBUS1_D15_M1	PDM1_SDI1_M1	SAI1_SDI1_M0	SAI1_SDO3_M0	GPIO4_B2_d
PWM2_CH7_M0	--	--	SPI3_CSN1_M2	SPI4_CSN0_M2	--	PDM1_SDI0_M1	SAI4_SDO_M0	SAI1_SDI0_M0	GPIO4_B3_d
CAN1_RX_M2	--	I2C3_SDA_M0	UART2_RX_M1	--	FLEXBUS0_CSN_M4	--	--	SPDIF_RX0_M0	GPIO4_B4_d
CAN1_TX_M2	PCIE0_CLKREQN_M2	I2C3_SCL_M0	UART2_TX_M1	--	FLEXBUS0_D15_M1	--	--	SPDIF_TX0_M0	GPIO4_B5_d

1D6 SAI1_MCLK_M0
1C6 SAI1_SCLK_M0
1C5 HP_DET_L
1B6 SAI1_LRCK_M0
1B5 PDM1_CLK0_M1
A7 SAI1_SDO0_M0

1A5
B7 SPK_CTL_H
B6 PDM1_SDI1_M1
1A6 SAI1_SDI0_M0
B8 I2C3_SDA_M0_Audio
1A4 I2C3_SCL_M0_Audio

VCCIO_1V8_S0
R1800 2.2K R0201
R1801 2.2K R0201
I2C3_SDA_M0_Audio
I2C3_SCL_M0_Audio

VCCIO2_VCC 2A2 C1800 100nF X5R 6.3V C0201 VCCIO_1V8_S0

RK3576
BGA698_16R1X17R2X1R08

RK3576_G(VCCIO3)

U1000G

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH0_M1	PCIE1_CLKREQN_M1	SPI1_CLK_M0	I2C9_SDA_M1	--	--	SAI3_SCLK_M1	--	SDMMC1_D0_M0	ETH1_RXD2_M1	GPIO1_B4_d
PWM1_CH1_M1	--	SPI1_MOST_M0	I2C9_SCL_M1	--	--	SAI3_LRCK_M1	--	SDMMC1_D1_M0	ETH1_RXD3_M1	GPIO1_B5_d
--	PCIE0_CLKREQN_M1	SPI1_MISO_M0	--	UART3_CTSN_M2	--	SAI3_SDO_M1	--	SDMMC1_D2_M0	ETH1_RXCLK_M1	GPIO1_B6_d
--	--	SPI1_CSN0_M0	--	UART3_RTSN_M2	--	SAI3_SDI_M1	--	SDMMC1_D3_M0	ETH1_TXD2_M1	GPIO1_B7_d
PWM0_CH0_M1	--	SPI1_CSN1_M0	--	UART3_TX_M2	--	PDM0_SDI2_M2	--	--	SDMMC1_CMD_M0	ETH1_TXD3_M1	GPIO1_C0_d
--	--	--	--	UART3_RX_M2	--	PDM0_CLK0_M2	SAI3_MCLK_M1	--	SDMMC1_CLK_M0	ETH1_TXCLK_M1	GPIO1_C1_d
PWM1_CH2_M1	--	SPI2_CSN1_M1	I2C6_SCL_M1	UART4_RTSN_M1	--	--	FSPI1_CSN1_M1	FSPI1_RSTN_M1	SDMMC1_PWREN_M0	ETH1_PPSCLK_M1	GPIO1_C2_d
--	--	SPI2_CSN0_M1	I2C6_SDA_M1	UART4_CTSN_M1	--	--	--	FSPI1_CSN0_M1	SDMMC1_DETN_M0	ETH1_PPSTRIG_M1	GPIO1_C3_d
--	PCIE0_BUTTONRSTN	SPI2_MOSI_M1	UART2_RTSN_M0	UART4_TX_M1	--	--	--	FSPI1_D0_M1	--	ETH1_RXD0_M1	GPIO1_C4_d
--	PCIE1_BUTTONRSTN	SPI2_MISO_M1	UART2_CTSN_M0	UART4_RX_M1	--	--	--	FSPI1_D1_M1	--	ETH1_RXD1_M1	GPIO1_C5_d
--	SATA_CPPOD	--	I2C8_SCL_M1	UART2_TX_M0	--	PDM0_SDI0_M2	--	FSPI1_D2_M1	--	ETH1_RXCTL_M1	GPIO1_C6_d
--	SATA_CPDET	--	I2C8_SDA_M1	UART2_RX_M0	--	PDM0_SDI1_M2	--	FSPI1_D3_M1	--	ETH1_RXD0_M1	GPIO1_C7_d
--	--	--	--	UART10_TX_M1	--	--	SAI2_SDO_M0	--	--	ETH1_RXD1_M1	GPIO1_D0_d
--	--	--	I3C0_SDA_PU_M1	UART10_RX_M1	--	--	SAI2_SCLK_M0	--	--	ETH1_RXCTL_M1	GPIO1_D1_d
PWM1_CH3_M1	--	--	I3C0_SCL_M1	--	--	--	SAI2_LRCK_M0	--	--	ETH1_MDC_M1	GPIO1_D2_d
PWM1_CH4_M1	--	--	I3C0_SDA_M1	--	--	--	SAI2_SDI_M0	--	--	ETH1_MDIO_M1	GPIO1_D3_d
--	--	--	I2C5_SCL_M1	UART10_RTSN_M1	SPDIF_RX1_M2	PDM0_SDI3_M2	SAI2_MCLK_M0	--	--	ETH1_MCLK_M1	GPIO1_D4_d
CLK1_32K_OUT	SATA_MPSWIT	SPI2_CLK_M1	I2C5_SDA_M1	UART10_CTSN_M1	SPDIF_TX1_M2	PDM0_CLK1_M2	--	FSPI1_CLK_M1	--	ETH_CLK1_25M_OUT_M1	GPIO1_D5_d

A28
B27
1A23 PCIE0_CLKREQn_M1
A27 PCIE0_WAKEn_M1

B26
1B22 PCIE0_PERSTn_M1
B29 UART4_RTSN_M1
1C23 UART4_CTSN_M1
1B23 UART4_TX_M1 For BT
B28 UART4_RX_M1
A26 WIFI_REG_ON_H
1C22 BT_REG_ON_H

C29
1D22 SAI2_SDO_M0
1A24 SAI2_SCLK_M0 For BT
C28 SAI2_LRCK_M0
1E21 SAI2_SDI_M0
1E22 HOST_WAKE_BT_H

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

VCCIO3_VCC 2B10 C1801 100nF X5R 6.3V C0201 VCCIO_WL

RK3576
BGA698_16R1X17R2X1R08

RK3576_J(VCCIO6)

U1000J

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH5_M1	UART11_TX_M2	SPI4_CSN1_M0	I2C7_SCL_M3	--	HDMI_TX_CEC_M0	--	SAI4_MCLK_M2	DSM_AUD_LP_M1	GPIO4_C0_d
PWM0_CH1_M1	UART11_RX_M2	EDP_TX_HPDIN_M0	I2C7_SDA_M3	PCIE1_CLKREQN_M3	HDMI_TX_HPDIN_M0	--	--	DSM_AUD_LN_M1	GPIO4_C1_d
PWM2_CH0_M1	UART9_TX_M2	CAN0_TX_M1	I2C2_SCL_M3	--	HDMI_TX_SCL	--	--	DSM_AUD_RP_M1	GPIO4_C2_d
PWM2_CH1_M1	UART9_RX_M2	CAN0_RX_M1	I2C2_SDA_M3	--	HDMI_TX_SDA	--	--	DSM_AUD_RN_M1	GPIO4_C3_d
PWM2_CH6_M1	UART6_TX_M3	SPI4_CSN0_M0	I2C3_SCL_M3	DP_HPDIN_M0	--	--	SAI4_LRCK_M2	ISP_PRELIGHT_TRIG_M1	GPIO4_C4_d
PWM2_CH5_M1	UART6_RX_M3	SPI4_MOSI_M0	I2C3_SDA_M3	SATA1_ACTLED_M1	--	VP0_SYNC_OUT	SAI4_SDO_M2	ISP_FLASH_TRIGOUT_M1	GPIO4_C5_d
PWM2_CH2_M1	CAN1_TX_M1	SPI4_MISO_M0	I2C6_SCL_M3	SATA0_ACTLED_M1	PCIE0_CLKREQN_M3	VP1_SYNC_OUT	SAI4_SDI_M2	--	GPIO4_C6_d
PWM2_CH3_M1	CAN1_RX_M1	SPI4_CLK_M0	I2C6_SDA_M3	--	--	VP2_SYNC_OUT	SAI4_SCLK_M2	--	GPIO4_C7_d

AK3
AK2
AL2 2024.5.27 HP_CTL_H
1AE2
AL3 TYPEC_DPTX_AUX_PUPDCTL1
AK1 TYPEC_DPTX_AUX_PUPDCTL2
1AE1 I2C6_SCL_M3_CC_RTC
AJ1 I2C6_SDA_M3_CC_RTC

VCC_3V3_S0
R1802 2.2K R0201
R1803 2.2K R0201
I2C6_SCL_M3_CC_RTC
I2C6_SDA_M3_CC_RTC

VCCIO6_VCC 2N3 C1802 100nF X5R 6.3V C0201 VCC_3V3_S0

RK3576
BGA698_16R1X17R2X1R08

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_TABLET_DEMO1_RK3576_LP4X		
File:	18.RK3576-GPIO VCCIO2/3/6		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:	Sheet: 19 of 50

RK3576_H(VCCIO4)

U1000H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

--	--	I2C4_SCL_M2	SPI4_CSN1_M3	UART8_TX_M1	--	SAI0_SDO0_M0	ETH0_RXD0_M1	SDMMC1_D0_M1	VI_CIF_D15	GPIO2_A6_d	B22	
--	--	I2C4_SDA_M2	--	UART8_RX_M1	--	SAI0_SDO1_M0	ETH0_TXCTL_M1	SDMMC1_D1_M1	VI_CIF_D14	GPIO2_A7_d	B20	
--	--	--	--	--	UART1_TX_M1	PDM0_SDI3_M3	SAI0_SDI0_M0	ETH0_TXD1_M1	SDMMC1_D2_M1	VI_CIF_D13	GPIO2_B0_d	B19
--	--	--	--	--	UART1_RX_M1	PDM0_SDI2_M3	SAI0_SDI1_M0	ETH0_TXD0_M1	SDMMC1_D3_M1	VI_CIF_D12	GPIO2_B1_d	1A18
--	--	PCIE0_CLKREQN_M0	SPI4_CSN0_M3	UART1_CTSN_M1	PDM0_SDI1_M3	SAI0_SDI2_M0	ETH0_TXD3_M1	SDMMC1_CMD_M1	VI_CIF_D11	GPIO2_B2_d	1A17	
--	--	PCIE1_CLKREQN_M0	SPI4_CLK_M3	UART1_RTSN_M1	PDM0_CLK1_M3	SAI0_SDO2_M0	ETH0_TXCLK_M1	SDMMC1_CLK_M1	VI_CIF_D10	GPIO2_B3_d	1B16	SPI4_CSN0_M3
--	SATA0_ACTLED_M0	--	SPI4_MOSI_M3	UART9_CTSN_M0	PDM0_SDI0_M3	SAI0_SDI3_M0	ETH0_TXD2_M1	SDMMC1_PWREN_M1	VI_CIF_D9	GPIO2_B4_d	A19	SPI4_CLK_M3
--	SATA1_ACTLED_M0	--	SPI4_MISO_M3	UART9_RTSN_M0	PDM0_CLK0_M3	SAI0_MCLK_M0	ETH0_RXCLK_M1	SDMMC1_DETN_M1	VI_CIF_D8	GPIO2_B5_d	1C18	SPI4_MOSI_M3
--	--	I2C8_SCL_M2	UART8_RTSN_M1	UART7_TX_M0	--	SAI0_SCLK_M0	ETH0_RXD3_M1	ETH1_PTP_REFCLK_M1	VI_CIF_D7	GPIO2_B6_d	A21	SPI4_MISO_M3
--	--	I2C8_SDA_M2	UART8_CTSN_M1	UART7_RX_M0	--	SAI0_LRCK_M0	ETH0_RXD2_M1	--	VI_CIF_D6	GPIO2_B7_d	B21	
PWM1_CH0_M2	--	--	--	UART9_RX_M0	PDM1_SDI1_M0	--	ETH0_PTP_REFCLK_M1	ETH1_RXD2_M0	VI_CIF_D5	GPIO2_C0_d	A17	
PWM1_CH1_M2	--	--	SPI1_CSN1_M1	UART9_TX_M0	PDM1_CLK1_M0	SAI2_MCLK_M1	ETH0_PPSCLK_M1	ETH1_RXD3_M0	VI_CIF_D4	GPIO2_C1_d	1A15	
PWM1_CH2_M2	--	--	SPI1_MOSI_M1	UART11_CTSN_M1	PDM1_SDI2_M0	SAI2_SCLK_M1	ETH0_PPSTRIG_M1	ETH1_RXCLK_M0	VI_CIF_D3	GPIO2_C2_d	1D15	
PWM0_CH0_M2	--	--	SPI1_MISO_M1	UART11_RTSN_M1	PDM1_SDI3_M0	SAI2_LRCK_M1	--	ETH1_TXD2_M0	VI_CIF_D2	GPIO2_C3_d	A15	
PWM1_CH3_M2	--	--	SPI1_CSN0_M1	UART11_TX_M1	PDM1_SDI0_M0	SAI2_SDO_M1	--	ETH1_TXD3_M0	VI_CIF_D1	GPIO2_C4_d	1A13	
PWM1_CH4_M2	--	--	SPI1_CLK_M1	UART11_RX_M1	PDM1_CLK0_M0	SAI2_SDI_M1	--	ETH1_TXCLK_M0	VI_CIF_D0	GPIO2_C5_d	1C15	
PWM1_CH5_M2	--	I2C5_SCL_M2	--	UART11_CTSN_M0	--	SAI3_SCLK_M3	--	ETH1_RXD0_M0	--	GPIO2_C6_d	1A14	
PWM0_CH1_M2	--	I2C5_SDA_M2	--	UART4_RTSN_M0	--	SAI3_LRCK_M3	--	ETH1_TXD1_M0	--	GPIO2_C7_d	B15	OTG_EN_H
PWM2_CH0_M2	--	I2C6_SCL_M2	--	UART4_TX_M0	--	SAI4_SDI_M3	--	ETH1_TXCTL_M0	--	GPIO2_D0_d	B16	
PWM2_CH1_M2	--	I2C6_SDA_M2	--	UART4_RX_M0	--	SAI4_SDO_M3	--	ETH1_RXD0_M0	--	GPIO2_D1_d	1A16	
PWM2_CH2_M2	I3C1_SCL_M0	--	--	UART6_TX_M1	--	SAI4_MCLK_M3	--	ETH1_RXD1_M0	CAM_CLKU_OUT_M1	GPIO2_D2_d	B17	
PWM2_CH3_M2	I3C1_SDA_M0	--	--	UART6_RX_M1	--	--	--	ETH1_RXCTL_M0	--	GPIO2_D3_d	B18	
PWM2_CH4_M2	--	I2C9_SDA_M2	--	UART6_RTSN_M1	--	--	--	ETH1_MDC_M0	ISP_PAELIGHT_TRIG_M0	GPIO2_D4_d	1B13	
PWM2_CH5_M2	--	I2C9_SCL_M2	--	UART6_CTSN_M1	--	--	--	ETH1_MDIO_M0	ISP_FLASH_TRIGOUT_M0	GPIO2_D5_d	B15	FLASH_LED_EN
PWM2_CH6_M2	I3C1_SDA_PU_M0	--	--	UART9_RTSN_M0	SPDIF_RX0_M2	SAI3_MCLK_M2	ETH0_MCLK_M1	ETH_CLK1_25M_OUT_M0	CAM_CLK1_OUT_M1	GPIO2_D6_d	1D18	PROX_INT
PWM2_CH7_M2	--	--	SPI3_CSN1_M0	UART9_CTSN_M0	SPDIF_TX0_M2	SAI3_SDO3_M0	ETH_CLK0_25M_OUT_M1	ETH1_MCLK_M0	CAM_CLK2_OUT_M1	GPIO2_D7_d	1E15	
--	--	I2C7_SCL_M1	SPI3_CLK_M0	UART3_TX_M0	--	SAI3_SCLK_M2	ETH0_MDIO_M1	--	VI_CIF_HREF	GPIO3_A0_d	1D16	
--	--	I2C7_SDA_M1	SPI3_MOSI_M0	UART3_RX_M0	--	SAI3_LRCK_M2	ETH0_MDC_M1	ETH1_PPSTRIG_M0	VI_CIF_VSYNC	GPIO3_A1_d	1B18	
--	MIPI_TE_M1	CAN1_RX_M3	SPI3_MISO_M0	UART9_CTSN_M0	SPDIF_RX1_M1	SAI3_SDO_M2	ETH0_RXCTL_M1	ETH1_PPSCLK_M0	VI_CIF_CLKO	GPIO3_A2_d	1A20	
--	--	CAN1_RX_M3	SPI3_CSN0_M0	UART9_RTSN_M0	SPDIF_TX1_M1	SAI3_SDI_M2	ETH0_RXD1_M1	ETH1_PTP_REFCLK_M0	VI_CIF_CLKI	GPIO3_A3_d	1A19	LCD_RESET_L

VCCIO4_VCC — 2A7 — C1901 1uF X5R 6.3V C0201 — VCCIO_1V8_S0

RK3576
BGA698_16R1X17R2X1R08

RK3576_I(VCCIO5)

U1000I

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH0_M3	--	SPI2_CLK_M2	UART1_CTSN_M2	FLEXBUS0_CSN_M0	--	FLEXBUS1_D11	DSMC_RDYN	SAI4_SDI_M1	ETH_CLK0_25M_OUT_M0	VO_EBC_SDSHR	VO_LCDC_D23	GPIO3_A4_d	1D13	LED_CTRL_R
PWM1_CH1_M3	--	SPI2_CSN1_M2	UART1_RTSN_M2	--	--	FLEXBUS0_D7	DSMC_DATA15	PDM1_SDI3_M2	ETH0_MDIO_M0	VO_EBC_GDSP	VO_LCDC_D22	GPIO3_A5_d	A9	LED_CTRL_G
PWM1_CH2_M3	--	UART10_CTSN_M0	UART1_RX_M2	--	--	FLEXBUS0_D6	DSMC_DATA14	PDM1_SDI2_M2	ETH0_MDC_M0	VO_EBC_GDOE	VO_LCDC_D21	GPIO3_A6_d	1A7	MIPI_DPHY_CSI0_RST_L
--	--	UART10_RTSN_M0	UART1_TX_M2	--	--	FLEXBUS0_D5	DSMC_DATA13	PDM1_CLK1_M2	ETH0_RXCTL_M0	VO_EBC_VCOM	VO_LCDC_D20	GPIO3_A7_d	B13	MIPI_DPHY_CSI3_RST_L
PWM0_CH0_M3	--	SPI2_MOSI_M2	UART10_RX_M0	--	--	FLEXBUS0_D8	DSMC_CSN1	SAI4_MCLK_M1	ETH0_MCLK_M0	VO_EBC_SDCE3	VO_LCDC_D19	GPIO3_B0_d	B14	
PWM1_CH3_M3	--	SPI4_CSN0_M1	UART10_TX_M0	--	--	FLEXBUS0_D4	DSMC_DATA12	PDM1_CLK0_M2	ETH0_RXD1_M0	VO_EBC_SDCE2	VO_LCDC_D18	GPIO3_B1_d	1A11	LED_CTRL_B
--	I2C8_SDA_M3	--	UART9_RX_M1	--	--	FLEXBUS0_D3	DSMC_DATA11	PDM1_SDI1_M2	ETH0_RXD0_M0	VO_EBC_SDCE1	VO_LCDC_D17	GPIO3_B2_d	A13	
--	I2C8_SCL_M3	--	UART9_TX_M1	--	--	FLEXBUS0_D2	DSMC_DATA10	PDM1_SDI0_M2	ETH0_TXCTL_M0	VO_EBC_SDCE0	VO_LCDC_D16	GPIO3_B3_d	A11	
PWM1_CH4_M3	--	--	UART9_RTSN_M1	--	--	FLEXBUS0_D1	DSMC_DATA9	SPDIF_RX1_M0	ETH0_TXD1_M0	VO_EBC_SDDO15	VO_LCDC_D15	GPIO3_B4_d	B10	
PWM1_CH5_M3	--	--	UART9_CTSN_M1	--	--	FLEXBUS0_D0	DSMC_DATA8	SPDIF_TX1_M0	ETH0_TXD0_M0	VO_EBC_SDDO14	VO_LCDC_D14	GPIO3_B5_d	1A9	
PWM0_CH1_M3	--	SPI3_CSN0_M1	--	--	--	FLEXBUS0_CLK	DSMC_DQS1	--	ETH0_TXCLK_M0	VO_EBC_SDDO13	VO_LCDC_D13	GPIO3_B6_d	B11	
--	I2C4_SDA_M3	UART3_CTSN_M1	UART2_RX_M2	FLEXBUS1_CSN_M0	--	FLEXBUS1_D10	DSMC_DQS0	SAI1_SDI0_M1	ETH0_PPSTRIG_M0	VO_EBC_SDDO12	VO_LCDC_D12	GPIO3_B7_d	1D12	I2C4_SDA_M3_MIPI_CSI0
--	I2C4_SCL_M3	UART3_RTSN_M1	UART2_TX_M2	--	--	FLEXBUS1_D9	DSMC_DATA7	SAI1_SDO3_M1	ETH0_PPSCLK_M0	VO_EBC_SDDO11	VO_LCDC_D11	GPIO3_C0_d	1E9	I2C4_SCL_M3_MIPI_CSI0
CAN0_RX_M3	I2C5_SDA_M3	SPI2_MISO_M2	UART11_RX_M0	--	--	FLEXBUS1_D8	DSMC_DATA6	SAI1_SDO2_M1	ETH0_PPS_REFCLK_M0	VO_EBC_SDDO10	VO_LCDC_D10	GPIO3_C1_d	1B10	I2C5_SDA_M3_MIPI_CSI3
CAN0_TX_M3	I2C5_SCL_M3	SPI4_MISO_M1	UART11_RTSN_M0	--	--	FLEXBUS1_D9	DSMC_DATA5	SAI1_SCLK_M2	ETH0_TXD3_M0	VO_EBC_SDDO9	VO_LCDC_D9	GPIO3_C2_d	B9	
PWM2_CH1_M3	I2C9_SDA_M3	SPI4_MOSI_M1	UART11_CTSN_M0	FLEXBUS0_CSN_M2	--	FLEXBUS1_D10	DSMC_INT3	SAI2_LRCK_M2	ETH0_TXD2_M0	VO_EBC_SDDO8	VO_LCDC_D8	GPIO3_C3_d	A8	
CAN0_TX_M3	I2C5_SCL_M3	SPI2_CSN0_M2	UART11_TX_M0	--	--	FLEXBUS1_D7	DSMC_DATA4	SAI1_SDO1_M1	--	VO_EBC_SDDO7	VO_LCDC_D7	GPIO3_C4_d	1D9	I2C5_SCL_M3_MIPI_CSI3
PWM2_CH2_M3	--	SPI1_MISO_M2	UART8_RX_M0	--	--	FLEXBUS1_D6	DSMC_DATA3	SAI1_LRCK_M1	--	VO_EBC_SDDO6	VO_LCDC_D6	GPIO3_C5_d	1B9	
--	--	SPI1_MOSI_M2	UART8_TX_M0	--	--	FLEXBUS1_D5	DSMC_DATA2	SAI1_LRCK_M1	--	VO_EBC_SDDO5	VO_LCDC_D5	GPIO3_C6_d	1D7	MIPI_DPHY_CSI_PWREN_H
--	--	SPI1_CLK_M2	UART8_RTSN_M0	--	--	FLEXBUS1_D4	DSMC_DATA2	SAI1_SCLK_M1	--	VO_EBC_SDDO4	VO_LCDC_D4	GPIO3_C7_d	1C7	MIPI_DPHY_CSI0_PDN_H
PWM2_CH3_M3	--	SPI1_CSN0_M2	UART8_CTSN_M0	--	--	FLEXBUS1_D3	DSMC_DATA1	SAI1_MCLK_M1	--	VO_EBC_SDDO3	VO_LCDC_D3	GPIO3_D0_d	1C12	
--	I3C1_SDA_PU_M2	SPI4_CLK_M1	--	FLEXBUS1_CSN_M2	--	FLEXBUS1_D11	DSMC_CSN2	SAI2_MCLK_M2	ETH0_RXCLK_M0	VO_EBC_SDDO2	VO_LCDC_D2	GPIO3_D1_d	1A12	
PWM2_CH4_M3	I3C1_SDA_M2	SPI4_CSN1_M1	UART12_RTSN_M2	FLEXBUS0_CSN_M3	FLEXBUS1_D15_M0	FLEXBUS1_D12	DSMC_CSN3	SAI2_SDI_M2	ETH0_RXD3_M0	VO_EBC_SDDO1	VO_LCDC_D1	GPIO3_D2_d	1A10	
PWM2_CH5_M3	I3C1_SCL_M2	--	UART12_CTSN_M2	--	--	FLEXBUS1_D2	DSMC_CSN0	SAI2_SDO_M2	ETH0_RXD2_M0	VO_EBC_SDDO0	VO_LCDC_D0	GPIO3_D3_d	B12	
--	I2C3_SCL_M2	SPI3_CLK_M1	UART5_RX_M0	--	--	FLEXBUS1_D1	DSMC_DATA0	SAI1_SDI1_M1	--	VO_EBC_SDLE	VO_LCDC_DEN	GPIO3_D4_d	1E12	
--	I2C3_SDA_M2	SPI3_MISO_M1	UART5_TX_M0	--	--	FLEXBUS1_D0	DSMC_CLKP	SAI1_SDI2_M1	--	VO_EBC_GDCLK	VO_LCDC_HSYNC	GPIO3_D5_d	1D10	MIPI_DPHY_CSI3_PDN_H
PWM2_CH6_M3	--	SPI3_MOSI_M1	UART5_CTSN_M0	--	--	FLEXBUS1_CLK	DSMC_CLKN	SAI1_SDI3_M1	--	VO_EBC_SDCLK	VO_LCDC_VSYNC	GPIO3_D6_d	1C10	
PWM2_CH7_M3	--	SPI3_CSN1_M1	UART5_RTSN_M0	FLEXBUS1_CSN_M1	FLEXBUS1_D12_M0	FLEXBUS1_D15_M0	DSMC_RESETN	SAI4_SCLK_M1	CAM_CLK0_OUT_M0	VO_EBC_SDOE	VO_LCDC_CLK	GPIO3_D7_d	1E7	MIPI_DPHY_CSI0_CAM_CLKOUT
MIPI_TE_M2	I2C7_SCL_M2	SPI1_CSN1_M2	UART3_TX_M1	FLEXBUS1_CSN_M3	FLEXBUS1_D14_M0	FLEXBUS1_D13_M0	DSMC_INT0	SAI4_LRCK_M1	CAM_CLK1_OUT_M0	SPDIF_RX0_M1	--	GPIO4_A0_d	1B12	
--	I2C7_SDA_M2	--	UART3_RX_M1	FLEXBUS0_CSN_M1	FLEXBUS1_D13_M0	FLEXBUS0_D14_M0	DSMC_INT2	SAI4_SDO_M1	CAM_CLK2_OUT_M0	SPDIF_TX0_M1	VO_POST_EMPTY	GPIO4_A1_d	1B7	MIPI_DPHY_CSI3_CAM_CLKOUT

VCCIO5_VCC_0 / VCCIO5_VCC_1 — 2A4 / 2A5 — C1903 1uF X5R 6.3V C0201 — VCCIO_1V8_S0

RK3576
BGA698_16R1X17R2X1R08

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

VCCIO_1V8_S0 — R1926 2.2K R0201 — I2C4_SDA_M3_MIPI_CSI0
VCCIO_1V8_S0 — R1927 2.2K R0201 — I2C4_SCL_M3_MIPI_CSI0
VCCIO_1V8_S0 — R1934 2.2K R0201 — I2C5_SDA_M3_MIPI_CSI3
VCCIO_1V8_S0 — R1935 2.2K R0201 — I2C5_SCL_M3_MIPI_CSI3

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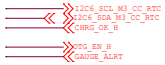
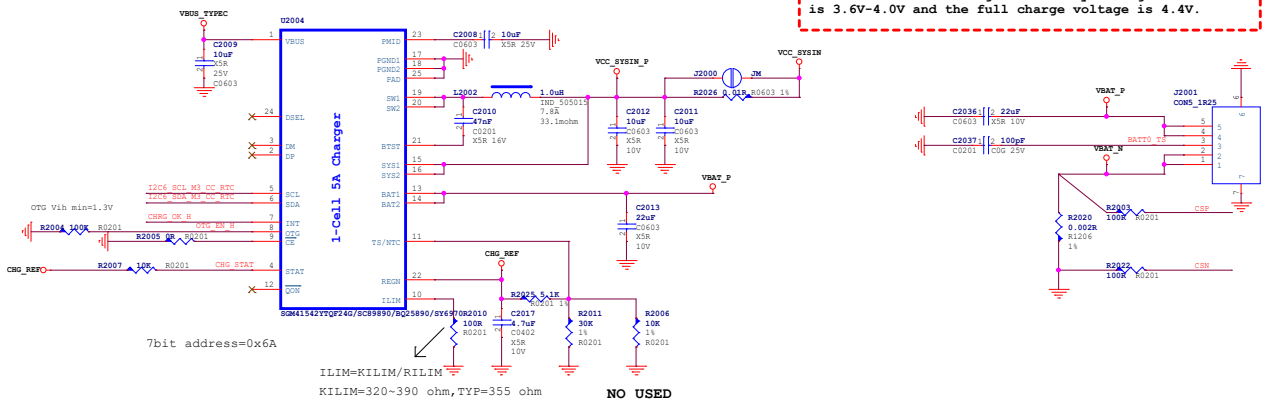
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_TABLET_DEMO1_RK3576_LP4X		
File:	19.RK3576-GPIO VCCIO4/5		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:	Sheet: 20 of 50

Power_1Cell_QC



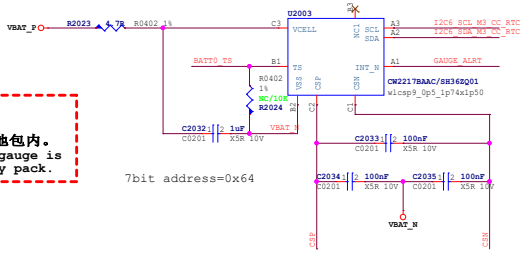
Charger IC

Note:
电池内阻小于80mR,满充电压4.4V，电池在3.6V—4.4V时最大充电电流10A。
The internal resistance of battery is less than 80mR, The maxium charging current no more then 10A during the battery voltage is 3.6V-4.0V and the full charge voltage is 4.4V.

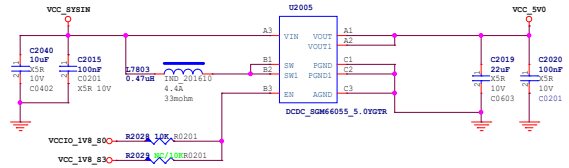


Gas Gauge

Note:
电量计建议放在电池包内。
Suggest the fuel gauge is built in the battery pack.



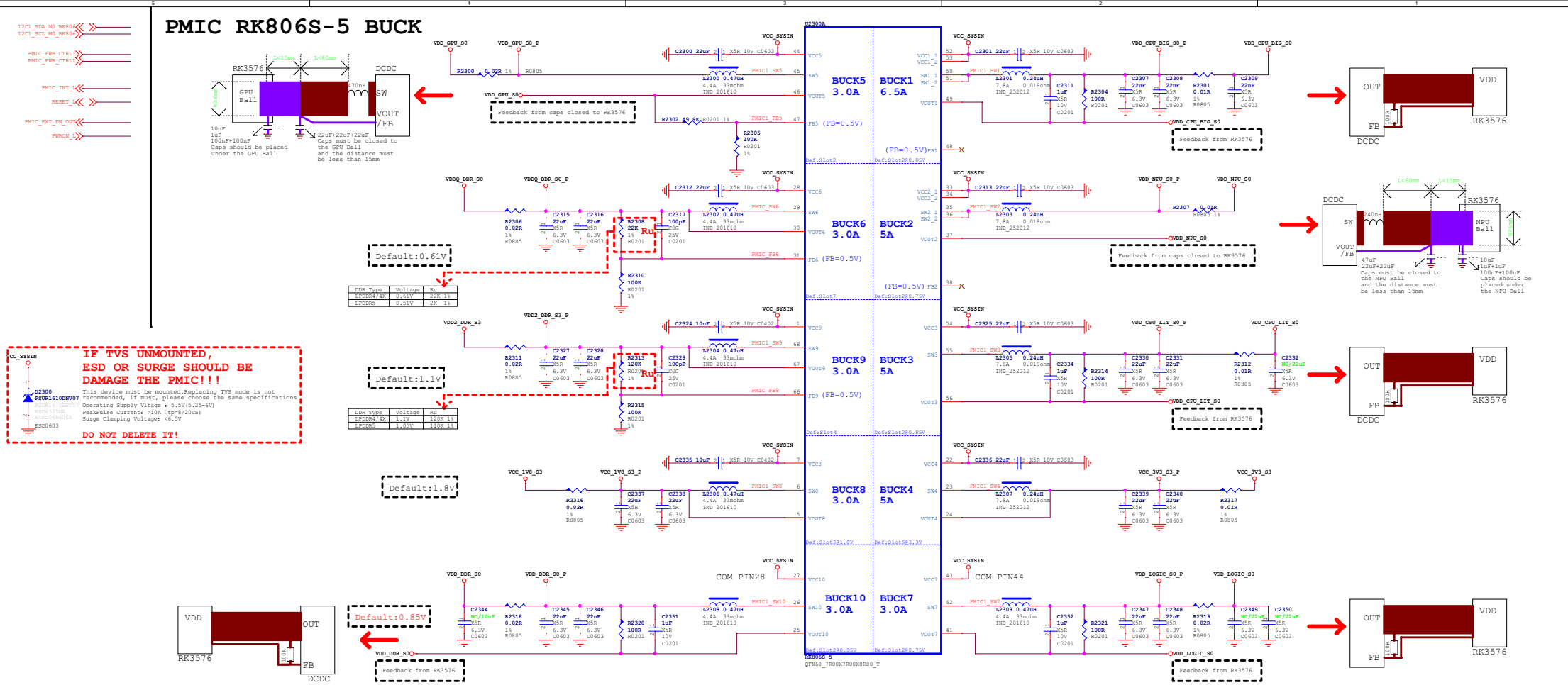
BOOST:VCC_5V0



Rockchip Confidential

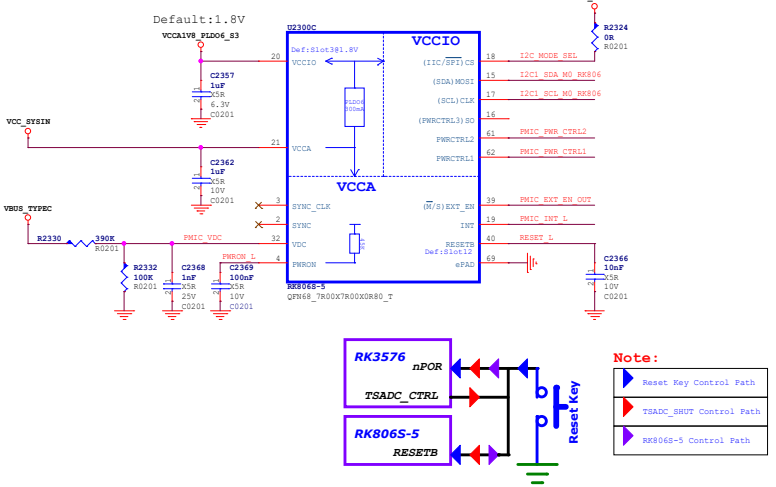
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_TABLET_DEMO1_RK3576_LP4X
File:	20.Power_1Cell_QC
Date:	Thursday, May 30, 2024
Rev:	V1.2
Designed by:	Mark Ye
Reviewed by:	
Sheet:	21 of 50

PMIC RK806S-5 BUCK



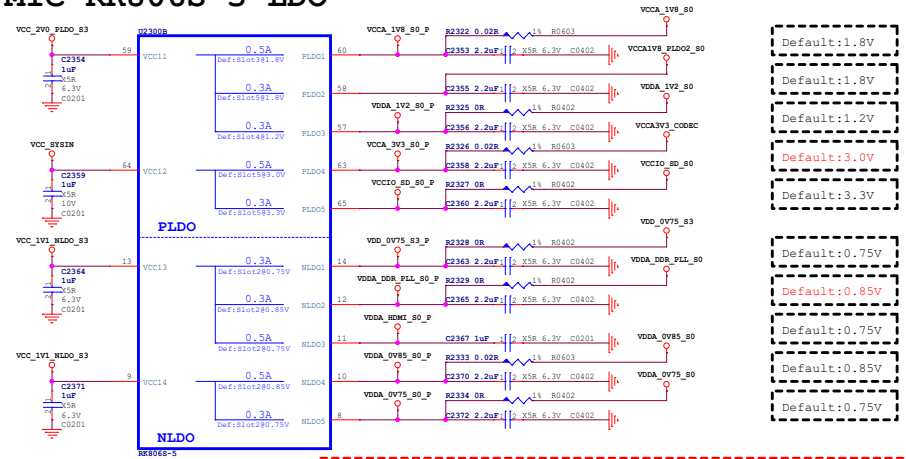
PMIC RK806S-5 Managerment

Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND



Note:
- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806S-5 Control Path

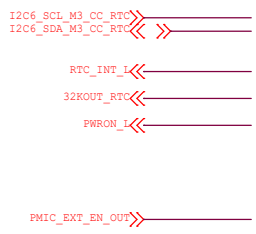
PMIC RK806S-5 LDO



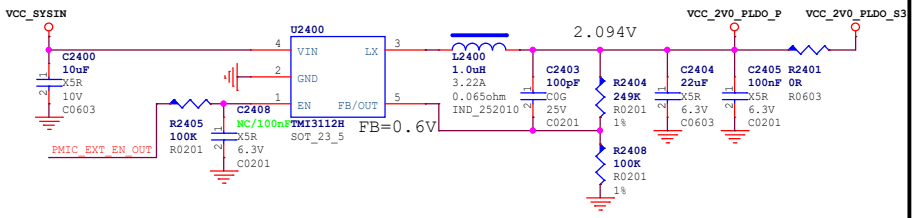
Default:1.8V
Default:1.8V
Default:1.2V
Default:3.0V
Default:3.3V
Default:0.75V
Default:0.85V
Default:0.75V
Default:0.85V
Default:0.75V

Note:
The RK806S-5 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

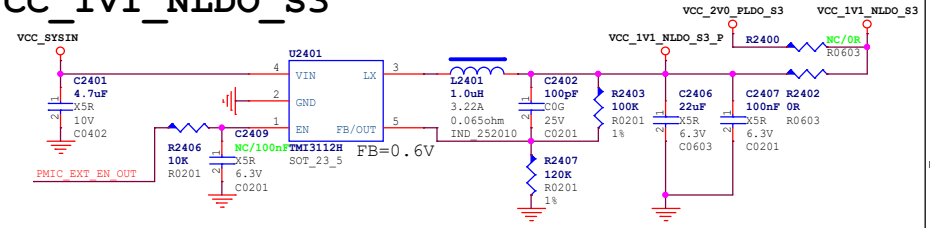
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_TABLET_DEMO1_RK3576_LP4X
File:	23.Power-PMIC RK806S-5
Date:	Thursday, May 30, 2024
Rev:	V1.2
Designed by:	Mark Ye
Reviewed by:	
Sheet:	22 of 50



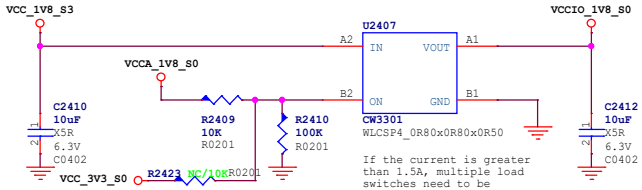
VCC_2V0_PLDO_S3



VCC_1V1_NLDO_S3



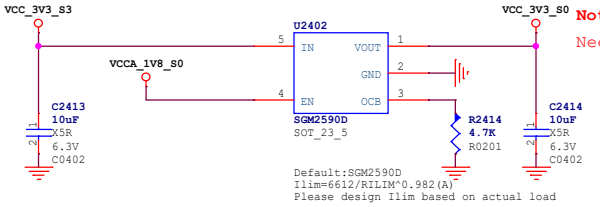
VCCIO_1V8_S0



Note:

1.8V Load switch!
Need quick output discharge!

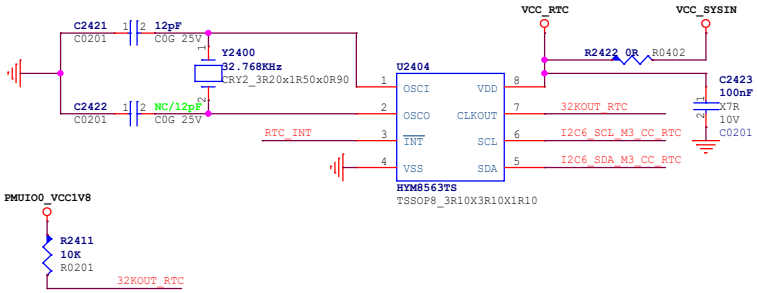
VCC_3V3_S0



Note:

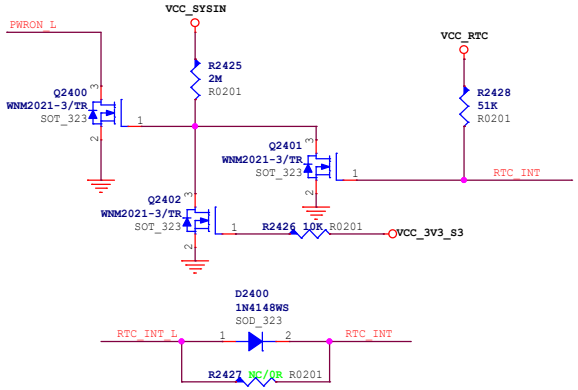
Need quick output discharge

RTC



WIFI/BT Power

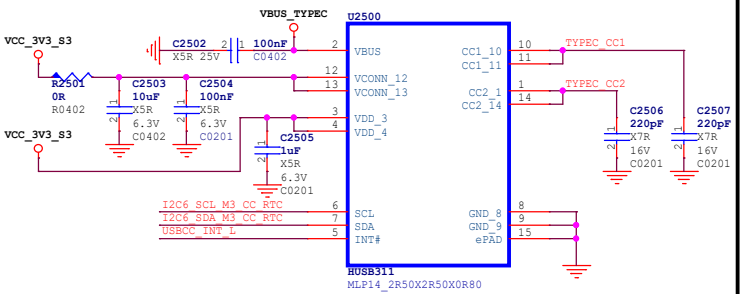
RTC POWERON



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	24.Power-Ext Discrete/RTC				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	23 of 50

CC

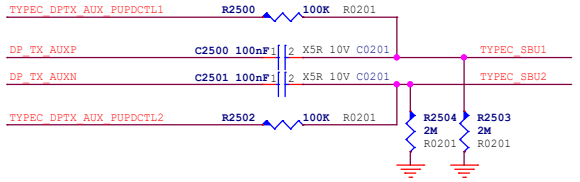


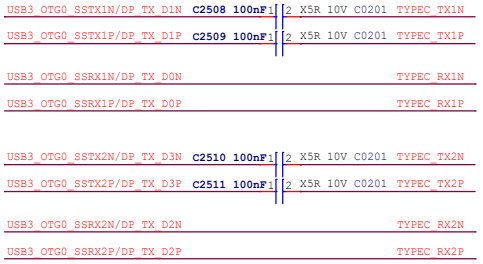
Note:
7bit address=0x22

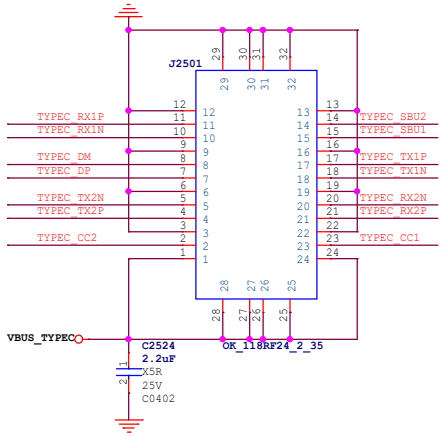
VBUS of FUSB302BMPX: 4 to 21 TYP = 5V
VDD of FUSB302BMPX: 3 to 5.5 TYP = 3.3V
VCONN of FUSB302BMPX: 3 to 5.5

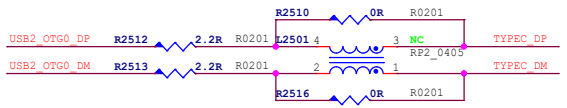
TYPEC

With Displayport Alt Mode
This is also the firmware download interface



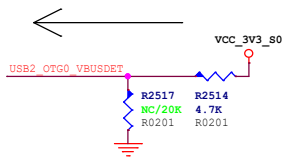




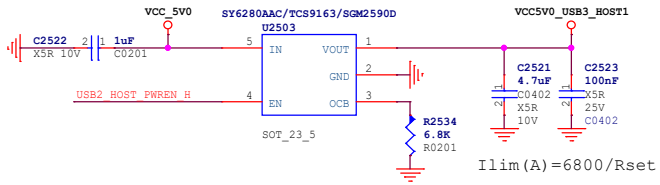


Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability

ESD on SUB board



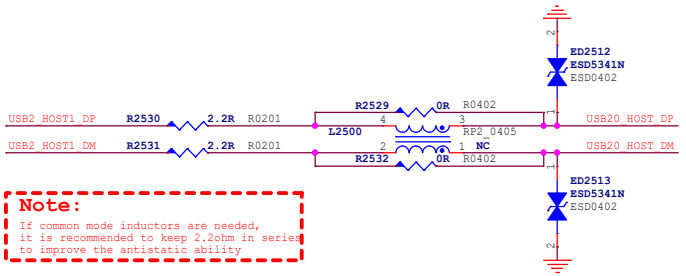
USB POWER



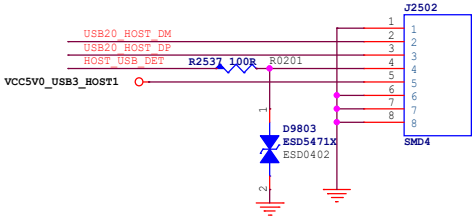
Ilim(A)=6800/Rset

USB20_HOST1

Note:
USB3信号的ESD不能随便换掉
如需换那么必须选择相同的规格。
Cj<=0.4pF



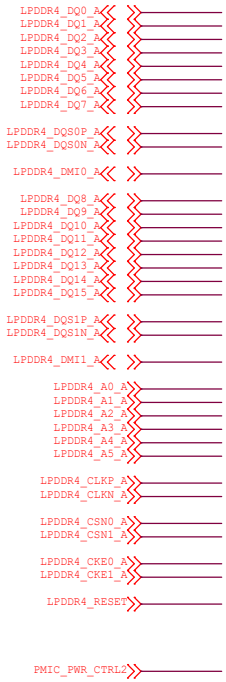
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability

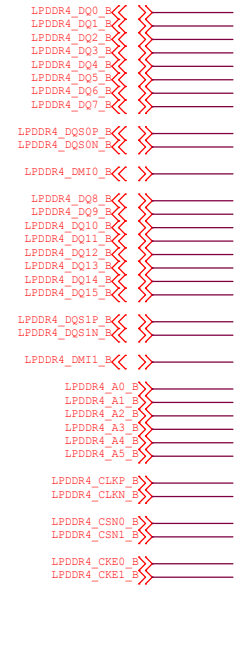


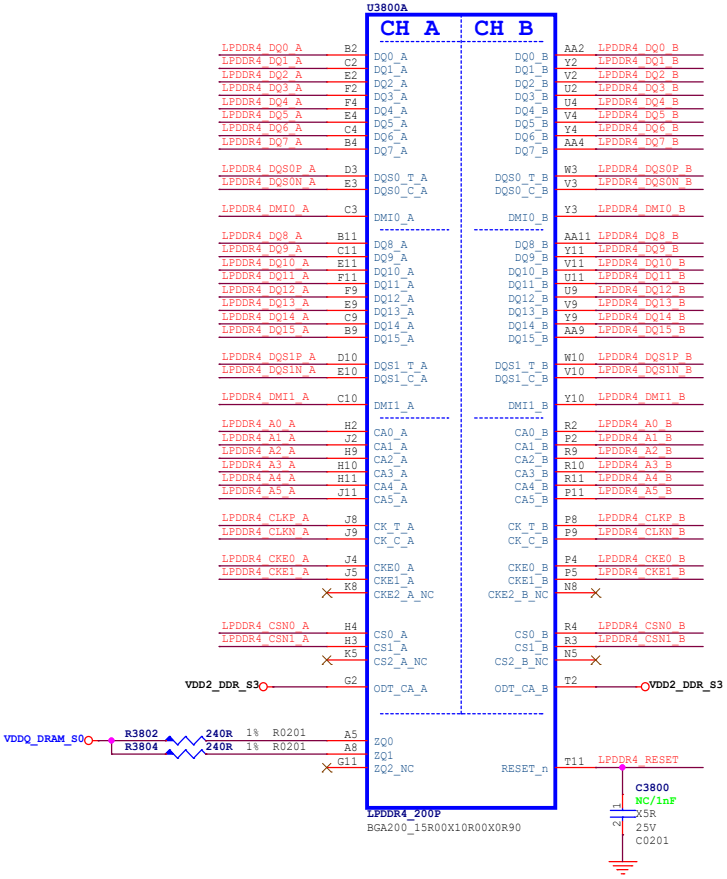
Rockchip Confidential

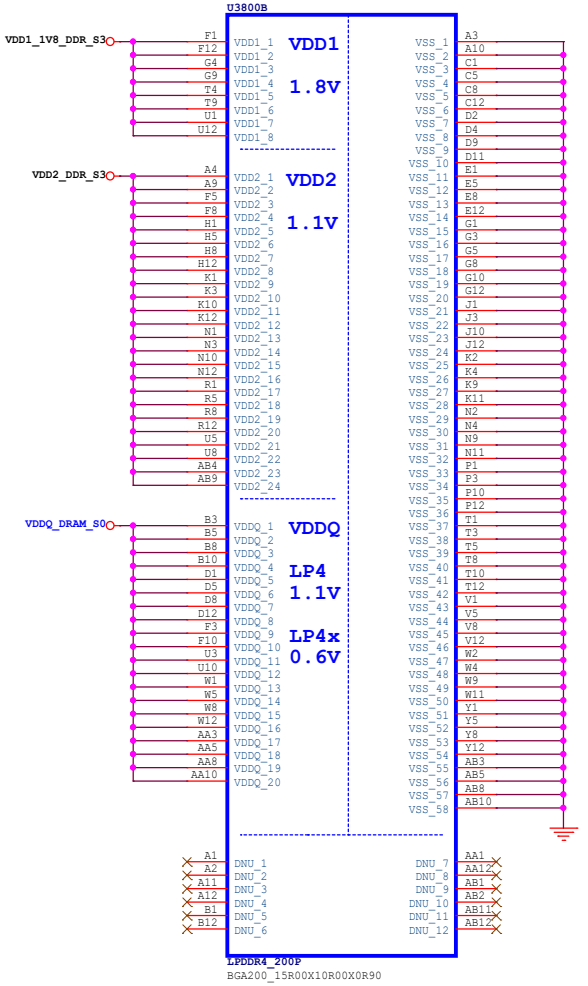
Rockchip Electronics Co., Ltd					
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	25.USB/TypeC Port				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	24 of 50

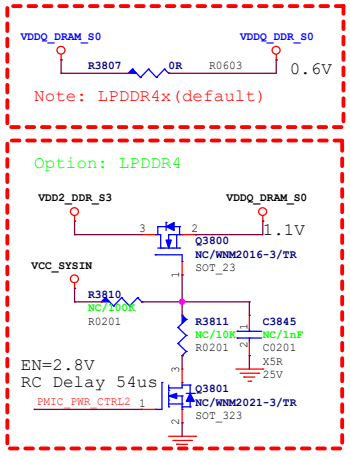
LPDDR4/4X

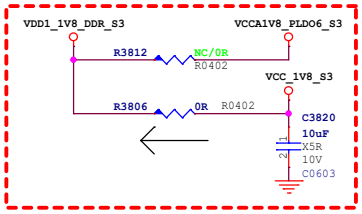


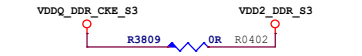








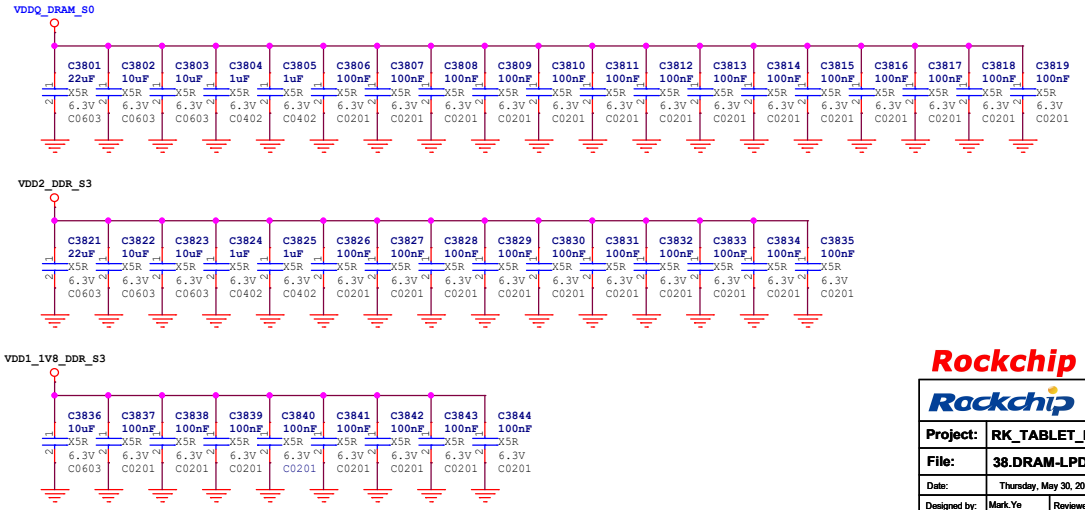




Note:

Sequence:VDD1-VDD2-VDDQ

	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65



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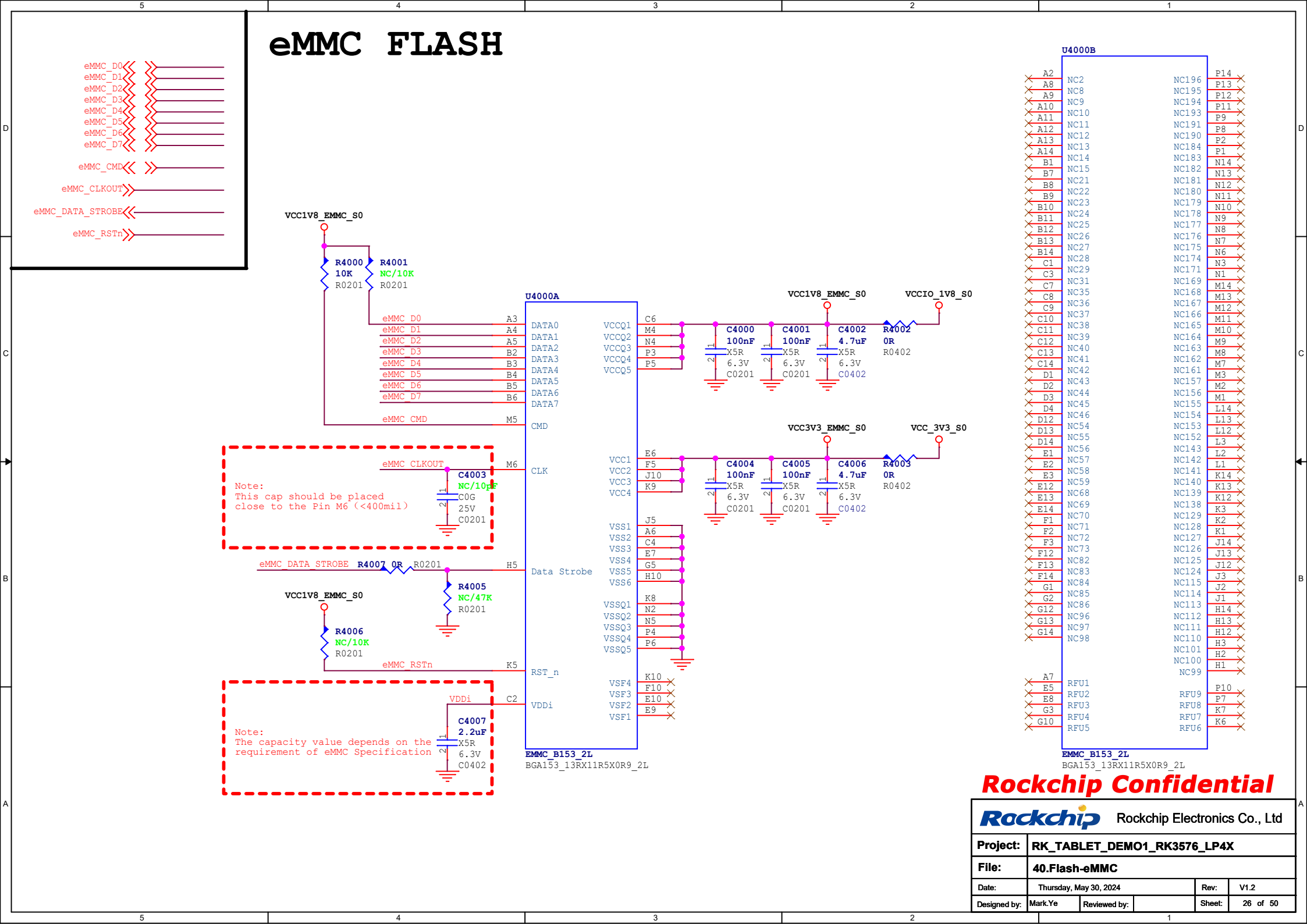
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_TABLET_DEMO1_RK3576_LP4X
File:	38.DRAM-LPDDR4X_1X32bit_200P
Date:	Thursday, May 30, 2024
Rev:	V1.2
Designed by:	Mark.Ye
Reviewed by:	
Sheet:	25 of 50

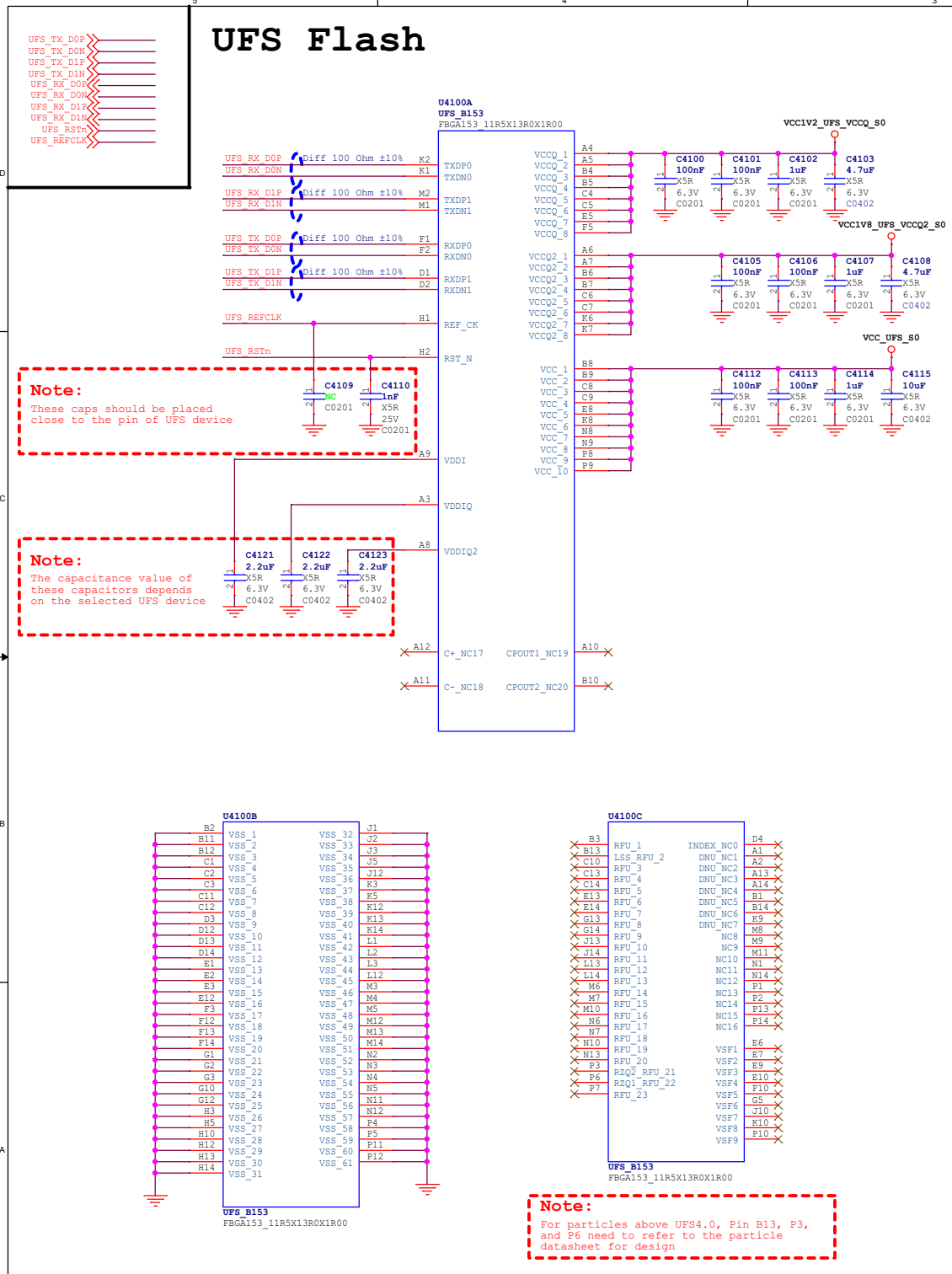
eMMC FLASH



Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	40.Flash-eMMC				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	26 of 50

UFS Flash



Note:
These caps should be placed close to the pin of UFS device

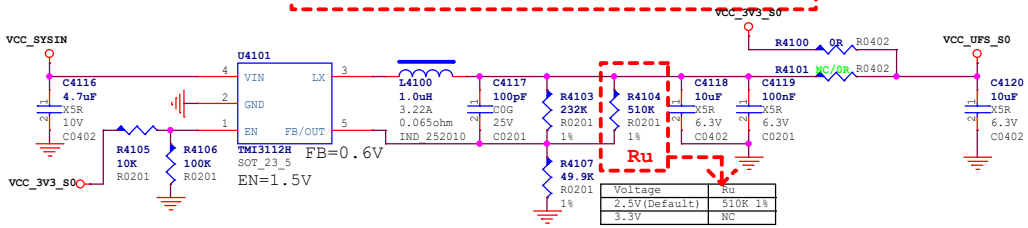
Note:
The capacitance value of these capacitors depends on the selected UFS device

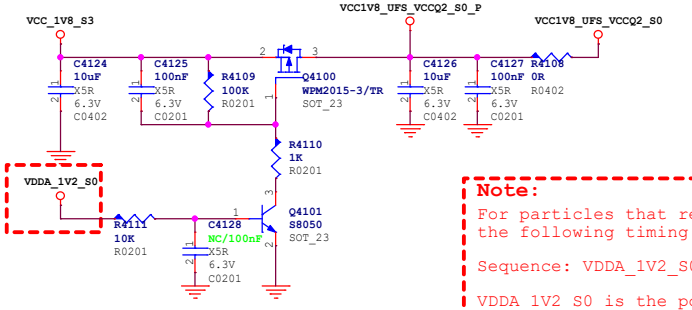
Note:
For particles above UFS4.0, Pin B13, P3, and P6 need to refer to the particle datasheet for design

UFS POWER

	VCCQ	VCCQ2	VCC	
UFS2.1	No Connect	1.8V	3.3V	Default UFS device: UFS2.2
UFS2.2	No Connect	1.8V	3.3V	
UFS3.0	1.2V	No Connect	2.5V/3.3V	
UFS3.1	1.2V	No Connect	2.5V/3.3V	
Sequence:VCCQ2->VCCQ, VCC is independent				

Note:
The power ball that is not used at the particle must be kept floating.

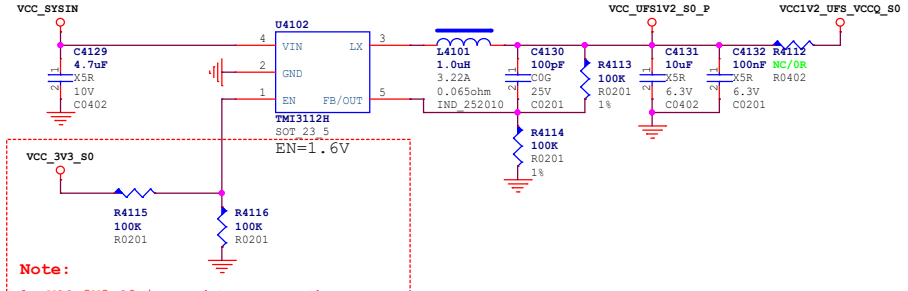




Note:
For particles that require VCCQ and VCCQ2, the following timing needs to be met:

Sequence: VDDA_1V2_S0->VCCQ2->VCCQ

VDDA_1V2_S0 is the power of REF_CK & RST_N in RK SOC, which needs to be powered on before UFS particles



Note:
1. VCC_3V3_S0 is used to ensure the power supply timing of the UFS chip;
2. The resistance voltage division value needs to be designed based on the EN pin threshold of DCDC.

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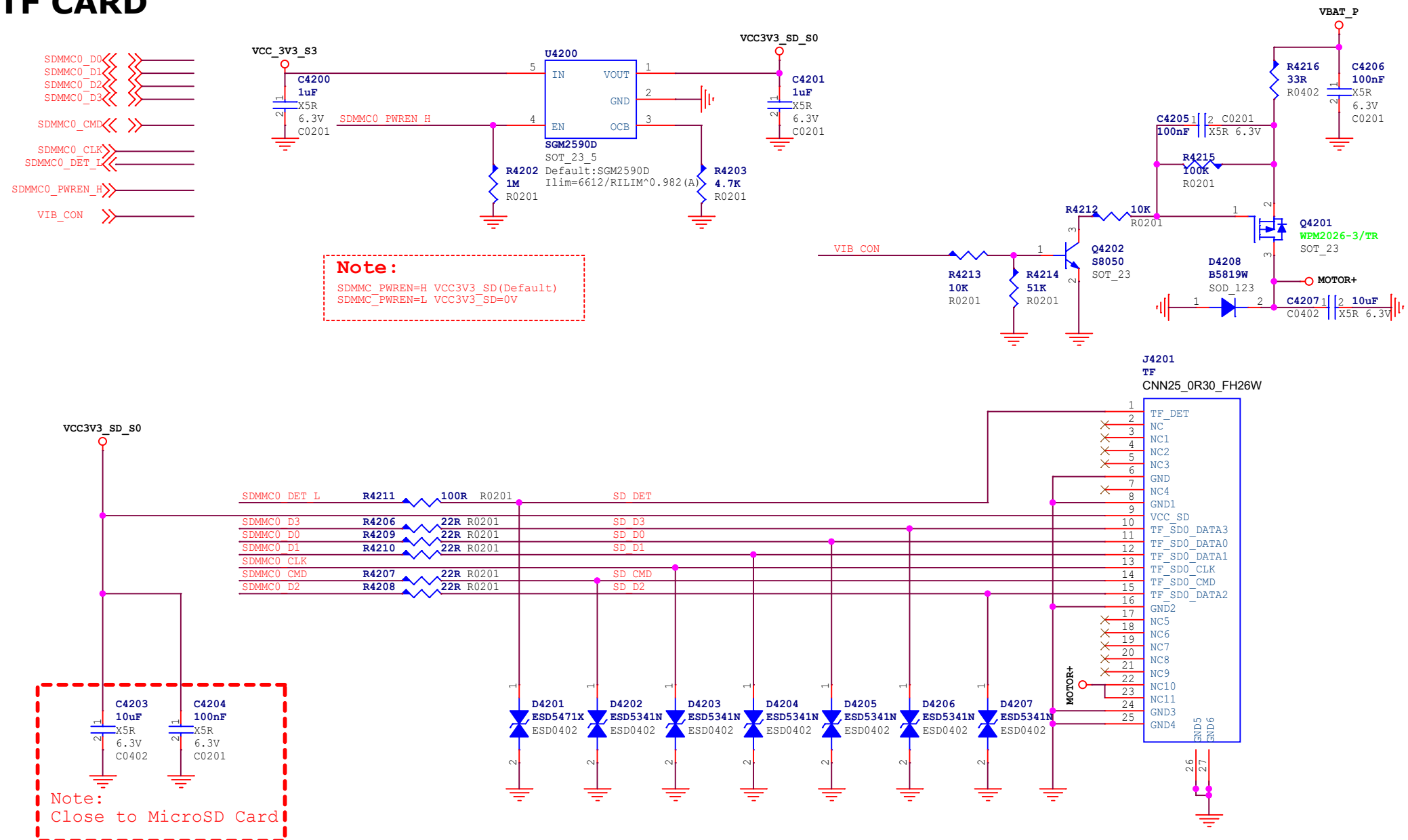
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	41.Flash-UFS				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	27 of 50

TF CARD



Note:
SDMMC_DET_L:
SDCARD PLUG: Pull-down to GND
SDCARD UNPLUG: Pull-up to PMUIO0_VCC1V8.

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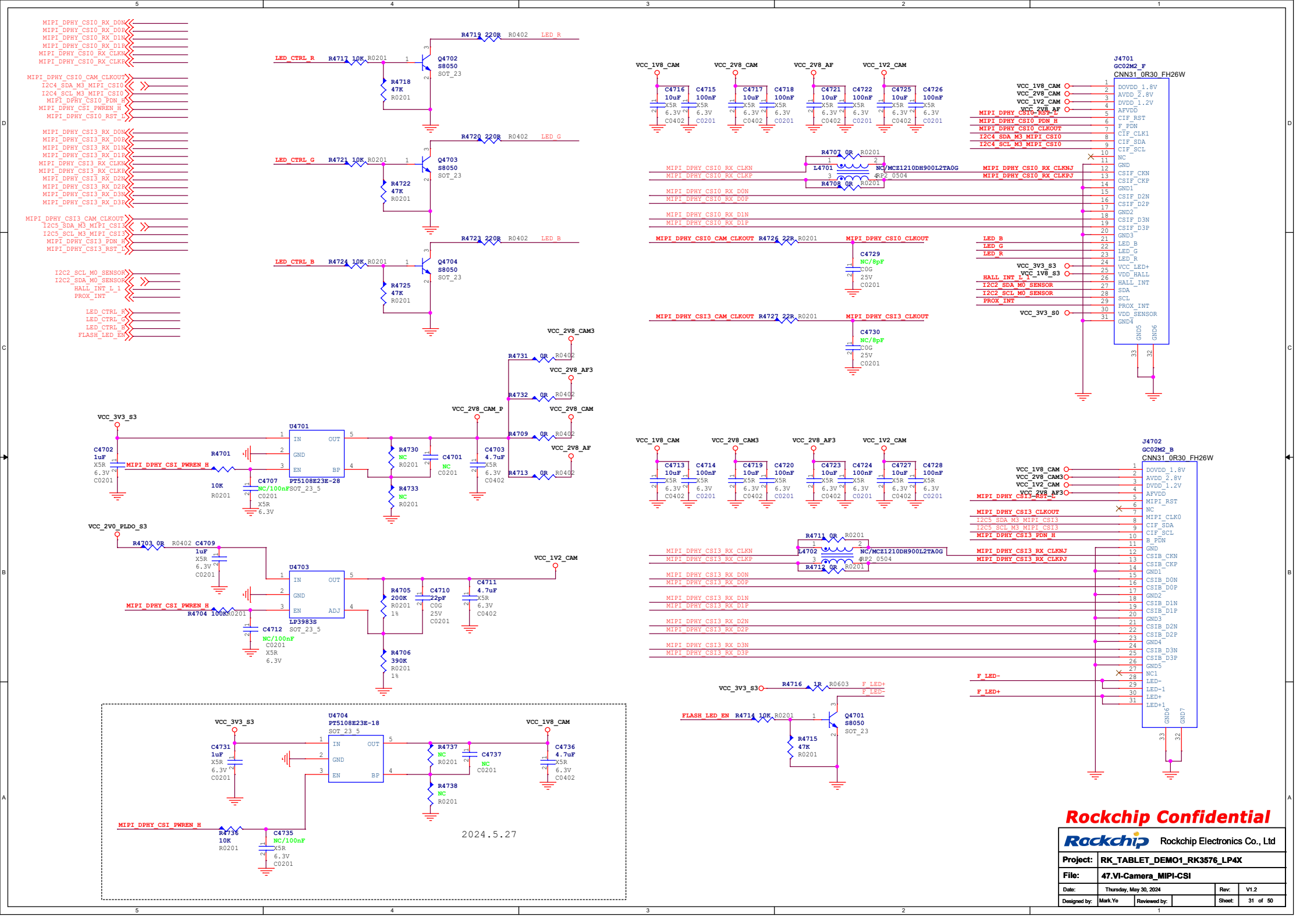
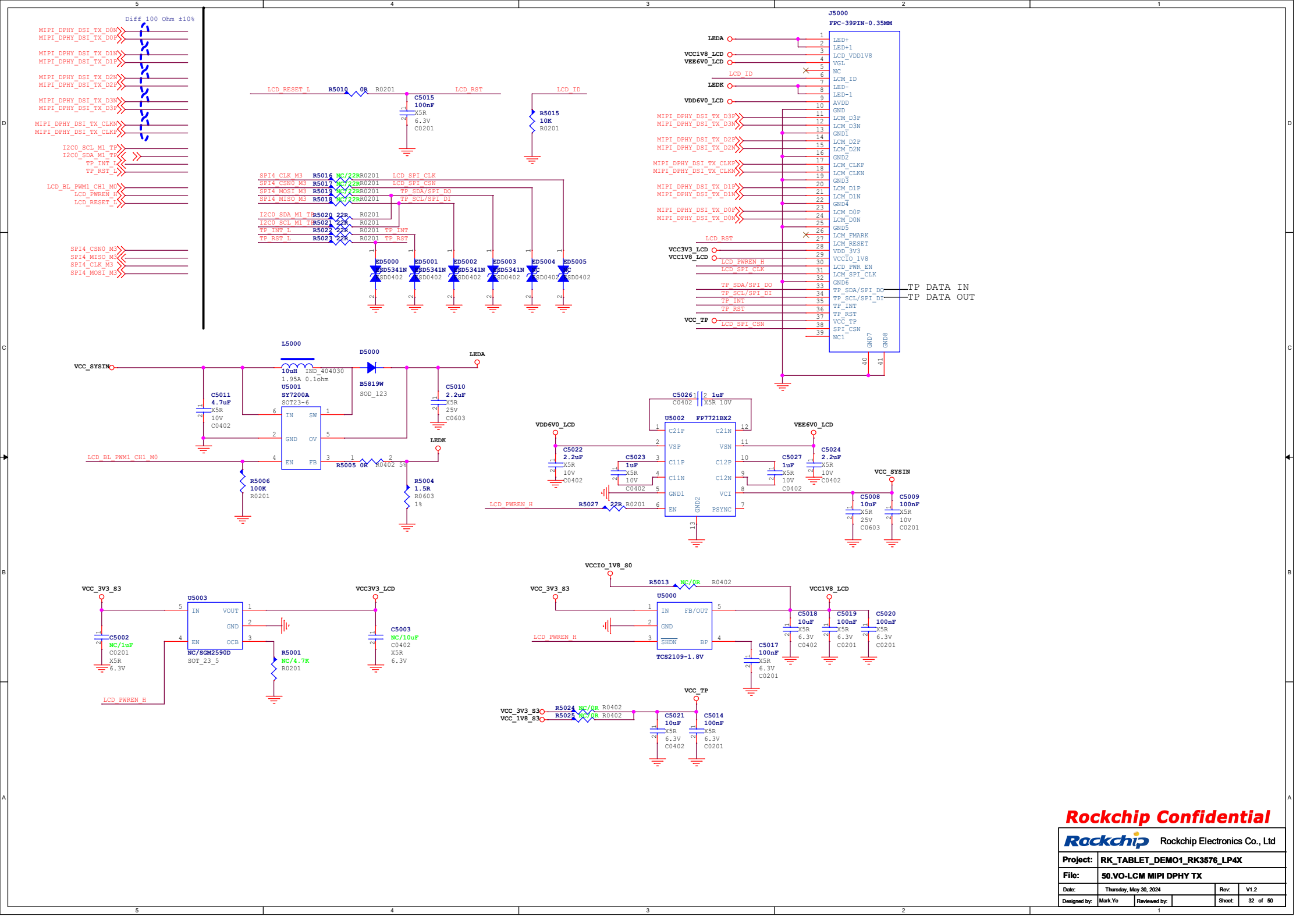
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_TABLET_DEMO1_RK3576_LP4X		
File:	42.Flash-MicroSD Card		
Date:	Thursday, May 30, 2024	Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:	Sheet: 28 of 50


MIPI_DPHY_CSI0_RX_D0N
MIPI_DPHY_CSI0_RX_D0P
MIPI_DPHY_CSI0_RX_D1N
MIPI_DPHY_CSI0_RX_D1P
MIPI_DPHY_CSI0_RX_CLKN
MIPI_DPHY_CSI0_RX_CLKP
MIPI_DPHY_CSI0_CAM_CLKOUT
I2C4_SDA_M3_MIPI_CSI0
I2C4_SCL_M3_MIPI_CSI0
MIPI_DPHY_CSI0_PDN_H
MIPI_DPHY_CSI_PWREN_H
MIPI_DPHY_CSI0_RST_L
MIPI_DPHY_CSI3_RX_D0N
MIPI_DPHY_CSI3_RX_D0P
MIPI_DPHY_CSI3_RX_D1N
MIPI_DPHY_CSI3_RX_D1P
MIPI_DPHY_CSI3_RX_CLKN
MIPI_DPHY_CSI3_RX_CLKP
MIPI_DPHY_CSI3_RX_D2N
MIPI_DPHY_CSI3_RX_D2P
MIPI_DPHY_CSI3_RX_D3N
MIPI_DPHY_CSI3_RX_D3P
MIPI_DPHY_CSI3_CAM_CLKOUT
I2C5_SDA_M3_MIPI_CSI3
I2C5_SCL_M3_MIPI_CSI3
MIPI_DPHY_CSI3_PDN_H
MIPI_DPHY_CSI3_RST_L
I2C2_SCL_M0_SENSOR
I2C2_SDA_M0_SENSOR
HALL_INT_L_1
PROX_INT
LED_CTRL_R
LED_CTRL_G
LED_CTRL_B
FLASH_LED_EN
R4719 220R R0402 LED_R
LED_CTRL_R R4717 10K R0201
Q4702 S8050 SOT_23
R4718 47K R0201
R4720 220R R0402 LED_G
LED_CTRL_G R4721 10K R0201
Q4703 S8050 SOT_23
R4722 47K R0201
R4723 220R R0402 LED_B
LED_CTRL_B R4724 10K R0201
Q4704 S8050 SOT_23
R4725 47K R0201
VCC_1V8_CAM
VCC_2V8_CAM
VCC_2V8_AF
VCC_1V2_CAM
C4716 10uF X5R 6.3V C0402
C4715 100nF X5R 6.3V C0201
C4717 10uF X5R 6.3V C0402
C4718 100nF X5R 6.3V C0201
C4721 10uF X5R 6.3V C0402
C4722 100nF X5R 6.3V C0201
C4725 10uF X5R 6.3V C0402
C4726 100nF X5R 6.3V C0201
J4701
GC02M2_F
CNN31_0R30_FH26W
DOVDD_1.8V
AVDD_2.8V
DVDD_1.2V
AFVDD
CIF_RST
F_PDN
CIF_CLK1
CIF_SDA
CIF_SCL
NC
GND
CSIF_CKN
CSIF_CKP
GND1
CSIF_D2N
CSIF_D2P
GND2
CSIF_D3N
CSIF_D3P
GND3
LED_B
LED_G
LED_R
VCC_LED+
VDD_HALL
HALL_INT
SDA
SCL
PROX_INT
VDD_SENSOR
GND4
GND5
GND6
R4707 0R R0201
L4701 NC/MCZ1210DH900L2TA0G
R4708 0R R0201
RP2 0504
C4729 NC/8pF C0G 25V C0201
C4730 NC/8pF C0G 25V C0201
VCC_2V8_CAM3
VCC_2V8_AF3
VCC_2V8_CAM_P
R4731 0R R0402
R4732 0R R0402
R4709 0R R0402
R4713 0R R0402
VCC_3V3_S3
U4701
PT5108E23E-28
SOT_23_5
C4702 1uF X5R 6.3V C0201
R4701 10K R0201
C4707 NC/100nF C0201 X5R 6.3V
R4730 NC R0201
R4733 NC R0201
C4701 NC C0201
C4703 4.7uF X5R 6.3V C0402
VCC_2V0_PLDO_S3
R4703 0R R0402
C4709 1uF X5R 6.3V C0201
U4703
LP3983S
SOT_23_5
R4704 100K R0201
C4712 NC/100nF C0201 X5R 6.3V
R4705 200K R0201 1%
R4706 390K R0201 1%
C4710 22pF C0G 25V C0201
C4711 4.7uF X5R 6.3V C0402
U4704
PT5108E23E-18
SOT_23_5
C4731 1uF X5R 6.3V C0201
R4736 10K R0201
C4735 NC/100nF X5R 6.3V C0201
R4737 NC R0201
R4738 NC R0201
C4737 NC C0201
C4736 4.7uF X5R 6.3V C0402
2024.5.27
VCC_1V8_CAM
VCC_2V8_CAM3
VCC_2V8_AF3
VCC_1V2_CAM
C4713 10uF X5R 6.3V C0402
C4714 100nF X5R 6.3V C0201
C4719 10uF X5R 6.3V C0402
C4720 100nF X5R 6.3V C0201
C4723 10uF X5R 6.3V C0402
C4724 100nF X5R 6.3V C0201
C4727 10uF X5R 6.3V C0402
C4728 100nF X5R 6.3V C0201
J4702
GC02M2_B
CNN31_0R30_FH26W
DOVDD_1.8V
AVDD_2.8V
DVDD_1.2V
AFVDD
MIPI_RST
NC
MIPI_CLK0
CIF_SDA
CIF_SCL
B_PDN
GND
CSIB_CKN
CSIB_CKP
GND1
CSIB_D0N
CSIB_D0P
GND2
CSIB_D1N
CSIB_D1P
GND3
CSIB_D2N
CSIB_D2P
GND4
CSIB_D3N
CSIB_D3P
GND5
NC1
LED-
LED-1
LED+
LED+1
GND6
GND7
R4711 0R R0201
L4702 NC/MCZ1210DH900L2TA0G
R4712 0R R0201
RP2 0504
R4716 1R R0603
R4714 10K R0201
Q4701 S8050 SOT_23
R4715 47K R0201
F_LED+
F_LED-
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK_TABLET_DEMO1_RK3576_LP4X
File: 47.VI-Camera_MIPI-CSI
Date: Thursday, May 30, 2024
Rev: V1.2
Designed by: Mark.Ye
Reviewed by:
Sheet: 31 of 50



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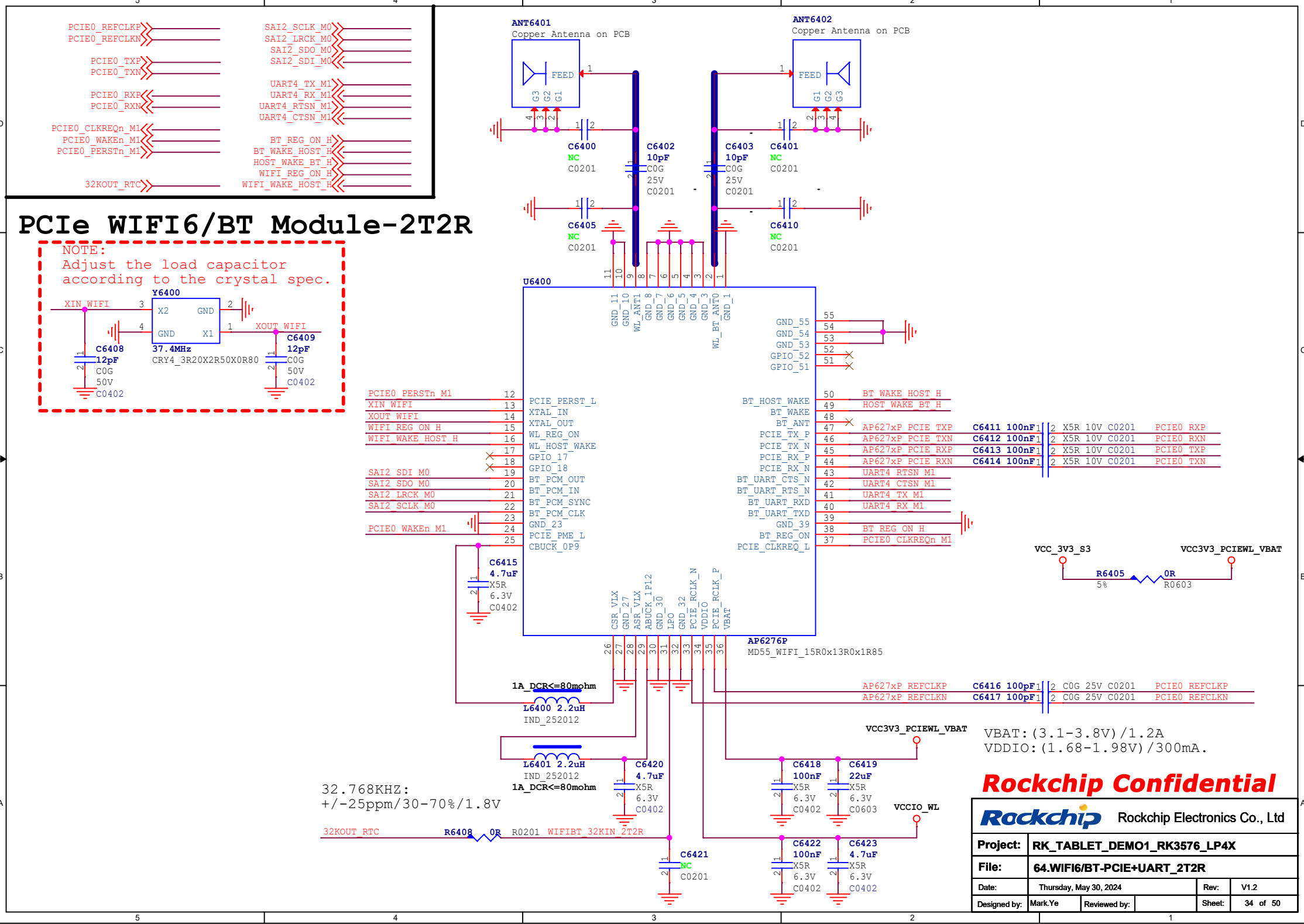
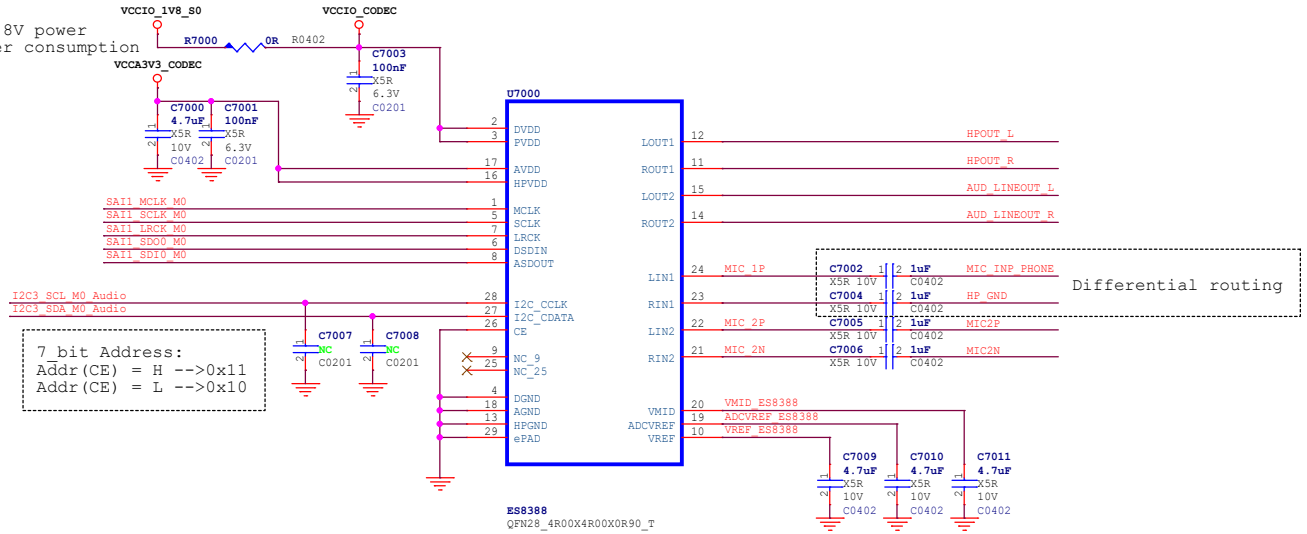
Rockchip Electronics Co., Ltd					
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	50.VO-LCM MIPI DPHY TX				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	32 of 50

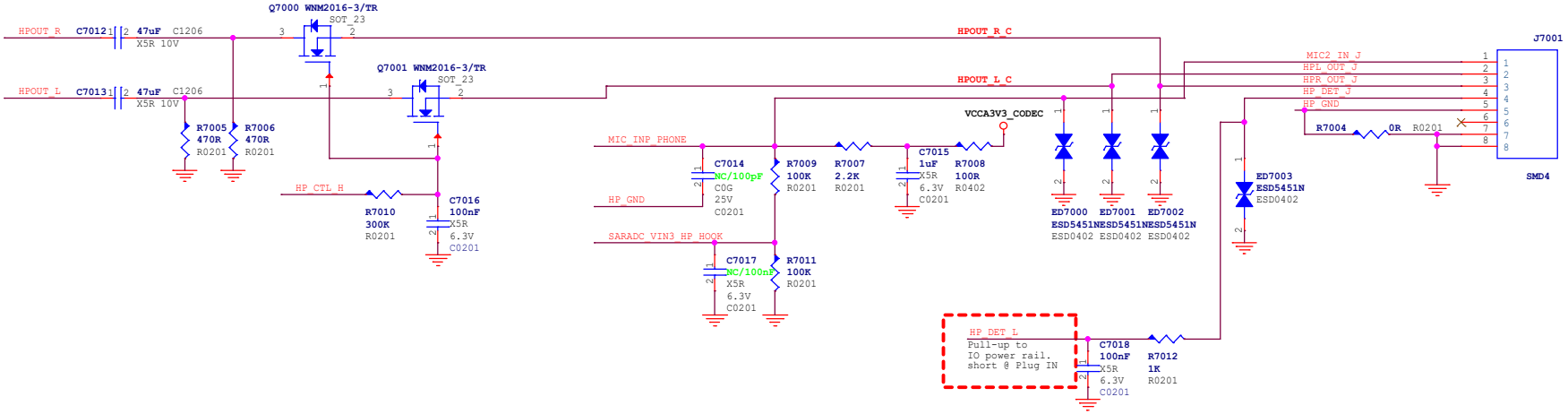

PCIE0_REFCLKP
PCIE0_REFCLKN
PCIE0_TXP
PCIE0_TXN
PCIE0_RXP
PCIE0_RXN
PCIE0_CLKREQn_M1
PCIE0_WAKEn_M1
PCIE0_PERSTn_M1
32KOUT_RTC
SAI2_SCLK_M0
SAI2_LRCK_M0
SAI2_SDO_M0
SAI2_SDI_M0
UART4_TX_M1
UART4_RX_M1
UART4_RTSN_M1
UART4_CTSN_M1
BT_REG_ON_H
BT_WAKE_HOST_H
HOST_WAKE_BT_H
WIFI_REG_ON_H
WIFI_WAKE_HOST_H
PCIe WIFI6/BT Module-2T2R
NOTE:
Adjust the load capacitor
according to the crystal spec.
Y6400
37.4MHz
CRY4_3R20X2R50X0R80
C6408 12pF C0G 50V C0402
C6409 12pF C0G 50V C0402
ANT6401
Copper Antenna on PCB
ANT6402
Copper Antenna on PCB
FEED
C6400 NC C0201
C6401 NC C0201
C6402 10pF C0G 25V C0201
C6403 10pF C0G 25V C0201
C6405 NC C0201
C6410 NC C0201
U6400
AP6276P
MD55_WIFI_15R0x13R0x1R85
PCIE_PERST_L
XTAL_IN
XTAL_OUT
WL_REG_ON
WL_HOST_WAKE
GPIO_17
GPIO_18
BT_PCM_OUT
BT_PCM_IN
BT_PCM_SYNC
BT_PCM_CLK
GND_23
PCIE_PME_L
CBUCK_0P9
BT_HOST_WAKE
BT_WAKE
BT_ANT
PCIE_TX_P
PCIE_TX_N
PCIE_RX_P
PCIE_RX_N
BT_UART_CTS_N
BT_UART_RTS_N
BT_UART_RXD
BT_UART_TXD
GND_39
BT_REG_ON
PCIE_CLKREQ_L
GND_55
GND_54
GND_53
GPIO_52
GPIO_51
C6411 100nF X5R 10V C0201
C6412 100nF X5R 10V C0201
C6413 100nF X5R 10V C0201
C6414 100nF X5R 10V C0201
C6415 4.7uF X5R 6.3V C0402
R6405 0R 5% R0603
VCC_3V3_S3
VCC3V3_PCIEWL_VBAT
1A_DCR<=80mohm
L6400 2.2uH IND_252012
L6401 2.2uH IND_252012
C6416 100pF C0G 25V C0201
C6417 100pF C0G 25V C0201
C6418 100nF X5R 6.3V C0402
C6419 22uF X5R 6.3V C0603
C6420 4.7uF X5R 6.3V C0402
C6421 NC C0201
C6422 100nF X5R 6.3V C0402
C6423 4.7uF X5R 6.3V C0402
VCCIO_WL
32.768KHZ:
+/-25ppm/30-70%/1.8V
32KOUT_RTC
R6408 0R R0201 WIFIBT_32KIN_2T2R
VBAT:(3.1-3.8V)/1.2A
VDDIO:(1.68-1.98V)/300mA.
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK_TABLET_DEMO1_RK3576_LP4X
File: 64.WIFI6/BT-PCIE+UART_2T2R
Date: Thursday, May 30, 2024
Rev: V1.2
Designed by: Mark.Ye
Reviewed by:
Sheet: 34 of 50

CODEC

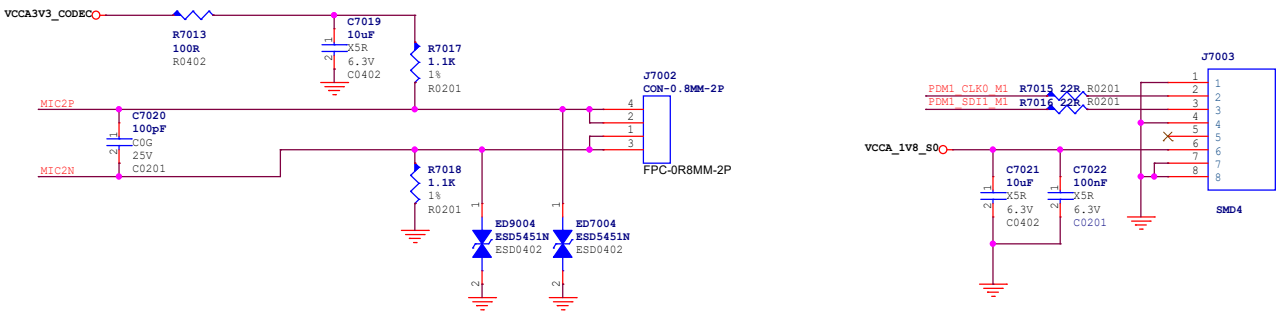
The chip can adopt 1.8V power supply to reduce power consumption



Headphone Jack(4-pole with DET & MIC)



MIC



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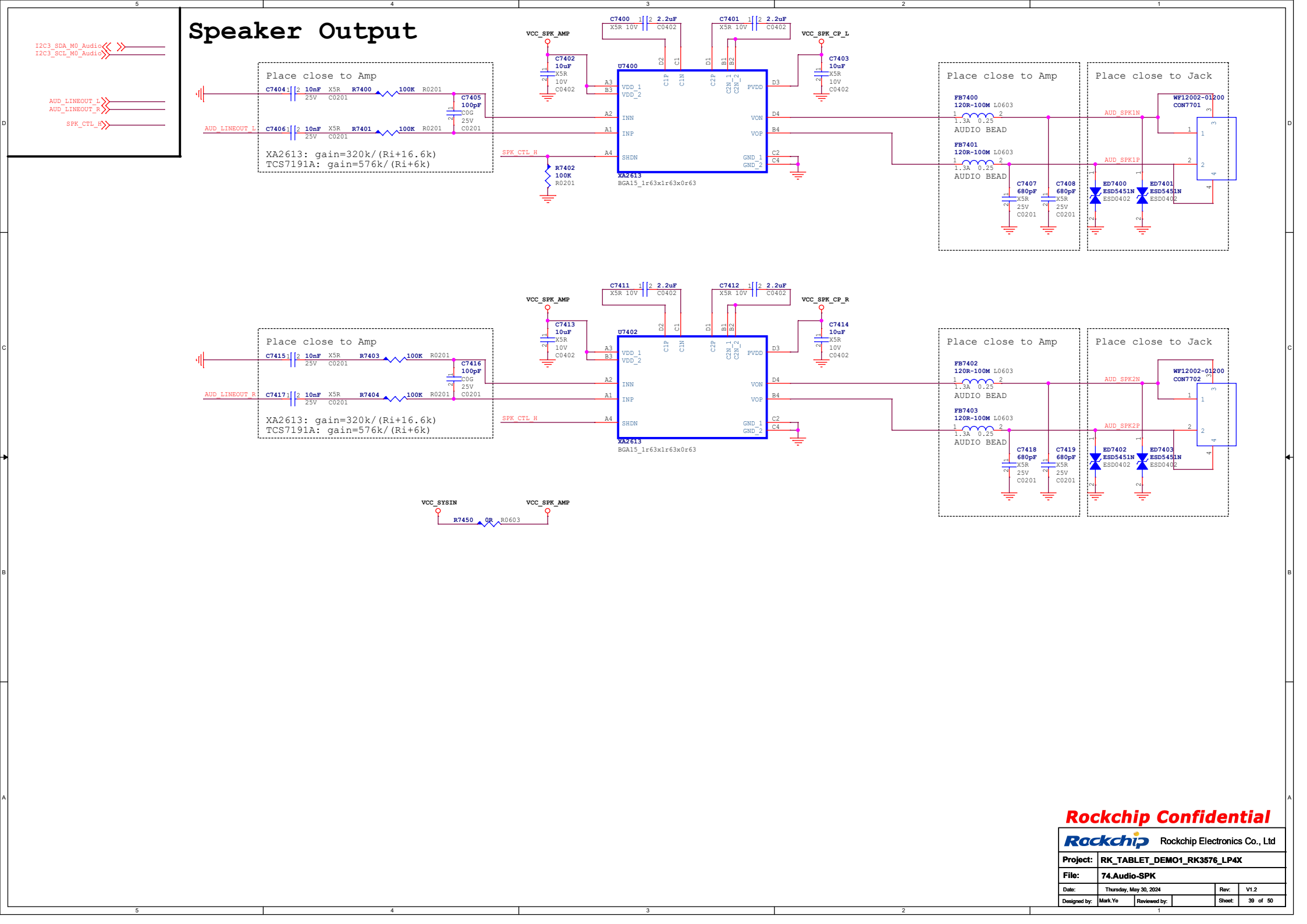
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	70.Audio-CODEC(ES8388)				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	38 of 50

Speaker Output



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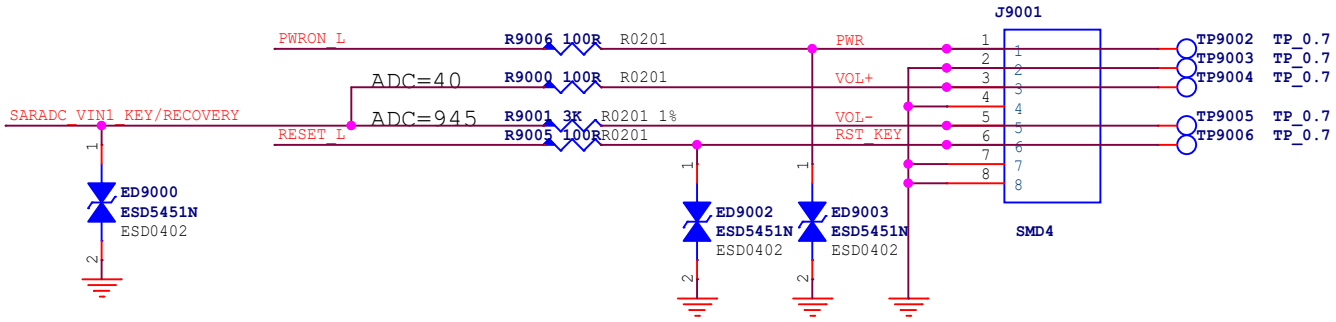
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	74.Audio-SPK				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	39 of 50

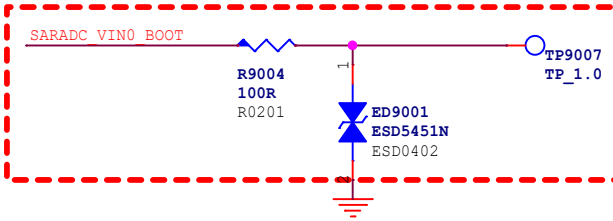
KEY

SARADC_VIN1_KEY/RECOVERY
RESET_L
PWRON_L

SARADC_VIN0_BOOT

Note:
Please reserve this circuit
if the RECOVERY_Key is not kept





Note:
Please reserve this circuit
if the BOOT_Key is not kept

Note:
If BOOT_SARADC_IN0=0V after power-on reset,
then system will enter into Maskrom mode.

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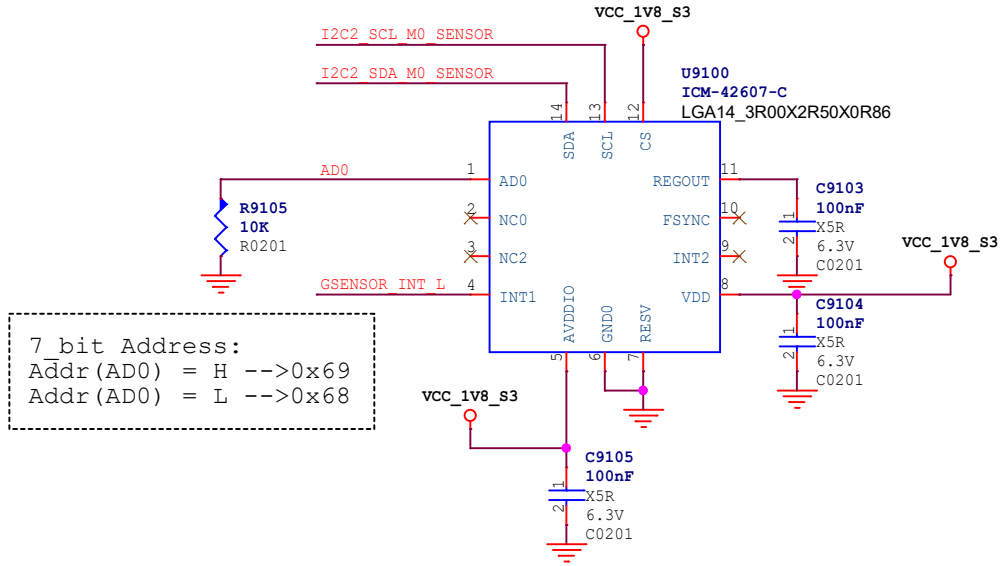
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	90.Key				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	43 of 50

I2C2_SCL_M0_SENSOR
I2C2_SDA_M0_SENSOR
GSENSOR_INT_L

Gyroscope+G-sensor



HALL

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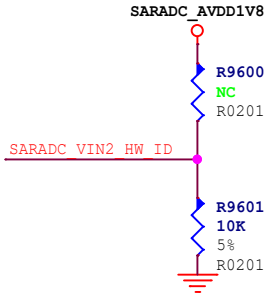
Rockchip Electronics Co., Ltd					
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	91.Sensors				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	44 of 50

HW_ID

SARADC_VIN2_HW_ID

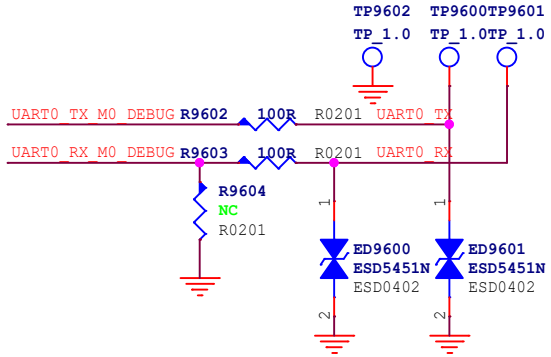
UART0_TX_M0_DEBUG

UART0_RX_M0_DEBUG



Config Table for SARADC_VIN2_HW_ID

Item	Rup	Rdown	ADC Value	VERSION
HW_ID1	DNP	10K	0	RESERVE
HW_ID2	100K	11.3K	416	RESERVE
HW_ID3	100K	24.9K	816	RESERVE
HW_ID4	100K	43K	1231	RESERVE
HW_ID5	100K	68K	1658	RESERVE
HW_ID6	100K	100K	2048	RESERVE
HW_ID7	68K	100K	2438	RESERVE
HW_ID8	43K	100K	2864	RESERVE
HW_ID9	24.9K	100K	3279	RESERVE
HW_ID10	11.3K	100K	3679	RESERVE
HW_ID11	10K	DNP	4095	RESERVE



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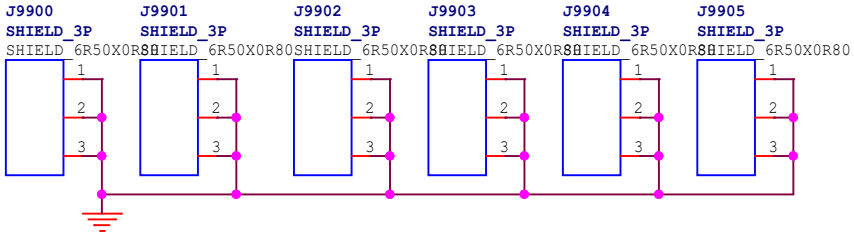
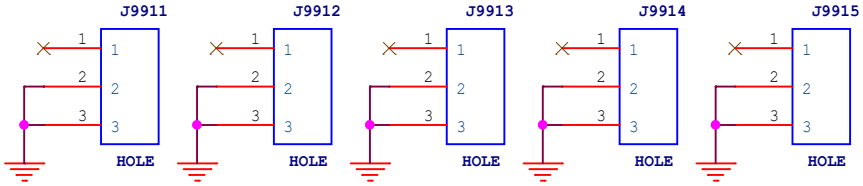
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	96.HW_ID				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	47 of 50



Hole



Mark

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_TABLET_DEMO1_RK3576_LP4X				
File:	99.Mark/Hole				
Date:	Thursday, May 30, 2024			Rev:	V1.2
Designed by:	Mark.Ye	Reviewed by:		Sheet:	50 of 50