

Lab 3 – Buffer Insertion

- Due: 23:59pm, May 6 (Thu)
- How to submit
 - **Zip all the files and upload it in the blackboard “Lab 3” page.**
 - **Email submission will not be accepted.**

Lab 3

- Download the following file.
 - `wget https://eecs.wsu.edu/~ee434/Labs/lab3.tar.gz`
- Unzip it.
 - `tar xvfz lab3.tar.gz`
- Source
 - `ictools_generic.sh`
 - `cadence_innovus17.sh`
- Run Innovus
 - `innovus`

Lab 3

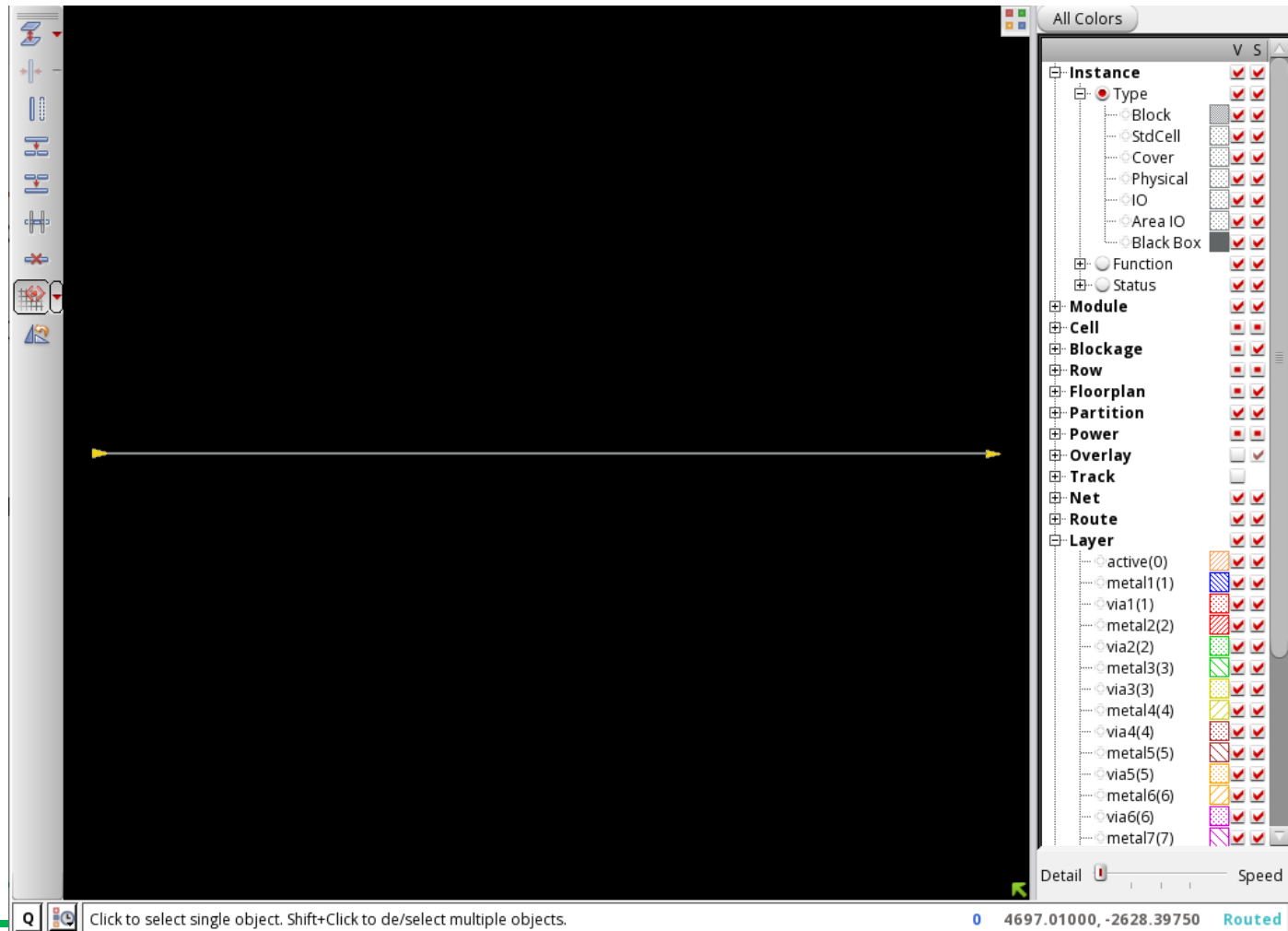
- Click “File” → “Import Design...”.
- In the “Design Import” window, click “Load...” and select “bi.globals”. This will fill up the “Design Import” window. Click “OK”.
- Now, you have imported the netlist. Let’s also import a layout. In the terminal window, run the following command.
 - `defIn bi.def`

```
innovus l>  
innovus l> defIn bi.def
```

- Press “f” to refresh the window.

Lab 3

- You can see this window.



User Interface

- Mouse left button: select an object.
- Mouse right button: click → hold → drag → release (zoom-in)

Timing

- The design has a two-input NAND gate.
- $g_out = \sim(g_in[0] \text{ AND } g_in[1])$
- Timing constraint: 500ps
- Layout width: 5,000um
 - The two input pins are on the left side of the layout.
 - The output pin is on the right side.
 - The NAND gate is on the left side.
 - Thus, the distance between the output of the NAND gate and the output pin g_out is almost 5,000um.
 - You are supposed to minimize the delay.

Timing

- Use “report_timing -net” to get a timing report.

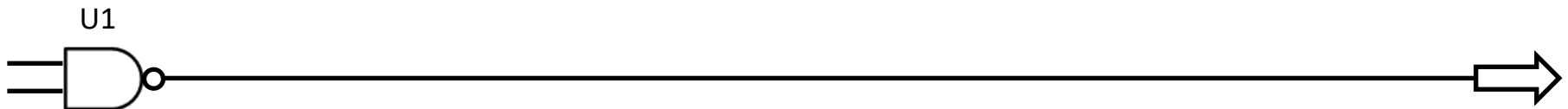
```
Path 1: VIOLATED Path Delay Check
Endpoint: g_out (^)
Beginpoint: g_in[1] (v) triggered by leading edge of '@'
Path Groups: {default}
Analysis View: NG_view_typ
- External Delay          0.000
+ Path Delay              0.500
= Required Time          0.500
- Arrival Time           2.323
= Slack Time             -1.823

  Clock Rise Edge          0.000
+ Input Delay              0.000
= Beginpoint Arrival Time  0.000
```

Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
g_in[1]	v	g_in[1]			0.000	-1.823
U1/A2	v	g_in[1]	NAND2_X1	0.000	0.000	-1.823
U1/ZN	^	g_out	NAND2_X1	0.475	0.475	-1.348
g_out	^	g_out	VBI	1.848	2.323	0.500

Gate internal delay

Net delay




Buffer Types



- BUF_X1
- BUF_X2
- BUF_X4
- BUF_X8
- BUF_X16
- BUF_X32

How to Insert a Buffer

- Click “ECO” → “Interactive ECO...”
- Click the “Add Repeater” tab.
- Type the name of the target net (“g_out” in this example) or click the net in the GUI window with your mouse left button and click “get selected” in the ECO window.
- In the “New Cell” box, select “BUF_X8”.
- Click the “Location” bullet.
- You can enter the target coordinate or click the icon beside the “First Buf/Inv” coordinates and click a target buffer insertion location in the layout.


 Interactive ECO


Add RepeaterAdd InstanceChange CellDel RepeaterDisplay Buffer Tree

Net: g_out  

Terminals:

☒ All Terminals


☐ Listed Terminals 


New Cell: BUF_X8 

Place Mode

☐ Default

☐ Don't Place Cells


☒ Location: First Buf/Inv X: 2740.499 Y: 1.5515 

☐ Second Inv X: Y: 



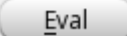

☐ Relative distance wire cut to the sink (%): 0.5

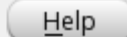
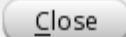

☐ Offload:

☒ By Slack (ns):

☐ By Location: X: Y: 

☐ Radius (um):





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How to Insert a Buffer

- Click “Apply”. This will insert a buffer into the target location.
- In the Innovus terminal, reroute the design (you should reroute the design after you insert a buffer.)
 - globalDetailRoute
- Then, run “report_timing -net”.
- The slack increased from -1.823ns to -0.851ns.

```
Path 1: VIOLATED Path Delay Check
Endpoint: g_out (v)
Beginpoint: g_in[1] (^) triggered by leading edge of '@'
Path Groups: {default}
Analysis View: NG_view_typ
- External Delay          0.000
+ Path Delay              0.500
= Required Time          0.500
- Arrival Time           1.351
= Slack Time              -0.851

Clock Rise Edge          0.000
+ Input Delay             0.000
= Beginpoint Arrival Time 0.000
```

Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
g_in[1]	^	g_in[1]			0.000	-0.851
U1/A2	^	g_in[1]	NAND2_X1	0.000	0.000	-0.851
U1/ZN	v	FE_ECON0_g_out	NAND2_X1	0.234	0.234	-0.618
FE_ECOC0_g_out/A	v	FE_ECON0_g_out	BUF_X8	0.620	0.854	0.002
FE_ECOC0_g_out/Z	v	g_out	BUF_X8	0.185	1.039	0.187
g_out	v	g_out	VBI	0.313	1.351	0.500

Note

- If you insert a buffer into a net, it splits the net into two nets. The names of the nets will change, so it would be better to select a net and click “Get Selected” in the “Add Repeater” window.

Goal

- Satisfy the given timing constraint.
- Minimize the total buffer size (the sum of BUF_X#).
- Submit
 - Final DEF file (see the next slide)
 - Final timing report (a screenshot or copy&paste)
 - Total buffer size
 - A brief description of the optimization methodology you used.

How to Generate DEF

- In the Innovus terminal, type
 - `defOut -floorplan -netlist -routing <filename>`
 - For example
 - `defOut -floorplan -netlist -routing Kim.def`

Play with Buffers

- If you want to delete a buffer, go to the “Del Repeater” tab.
 - Select the target buffer in the layout.
 - Click “Get Selected”.
 - Click “Apply”.
- If you want to replace a buffer with a different buffer, go to the “Change Cell” tab.
 - Select the target buffer in the layout.
 - Click “Get Selected”.
 - Select the new buffer type (e.g., BUF_X16) in the “specified cell”.
 - Click “Apply”.
- Don’t forget to reroute the design whenever you modify the layout.
 - globalDetailRoute