Lab 2 – Full-Custom Design

- Due: 2pm, Apr. 26 (Mon)

- How to submit
  - **Zip all the files and upload it in the blackboard "Lab 2" page.**
  - **Email submission will not be accepted.**

- Read the "tutorial_virtuoso.pdf" in the "Labs" page carefully.

Target Design and Specification

- Two-input XOR gate (use the static CMOS design methodology)

- Specification
  - Input ports: A, B, VDD, VSS
  - Output port: Y
  - Layout dimension: Width (2um), Height (2um)
  - Input vector: (A,B) = (0,0) → (1,0) → (0,0) → (0,1) → (0,0) → (1,1) → (1,0) → (1,1) → (0,1) → (1,1)
  - Worst-case rise and fall delays (for a 10fF load cap): < ~200ps

  - Do not use M2~M10 layers.

Target Design and Specification

- Submit (zip the files and upload it in the Labs submission page)
  - A screenshot of your layout with two rulers shown (width and height)
  - A snapshot of your transistor-level schematic (you can draw it on paper and take a photo of it). Show the width of each TR.
  - DRC and LVS reports
    - drc.results and drc.summary generated by nmDRC.
    - lvs.report generated by nmLVS.
  - Input and output waveforms for pre-layout simulation (show A, B, Y, and some data points showing the delay values).
  - Input and output waveforms for post-layout simulation (show A, B, Y, and some data points showing the delay values).
  - Pre-layout simulation files (LVS.sp and pre.sp)
  - Post-layout simulation files (post.sp and PEX HSpice files)
  - A summary report. Just show the following numbers.
    - Layout width and height
    - Rise delays for (0,0) → (1,0), (0,0) → (0,1), (1,1) → (1,0), and (1,1) → (0,1)
    - Fall delays for (1,0) → (0,0), (0,1) → (0,0), (1,0) → (1,1), and (0,1) → (1,1)

Procedure

Step	Date	Points	What to do
0	3/12		Announcement
1	3/22	10	A rough layout of the inverter in the tutorial
2	3/29	10	DRC, LVS, PEX, and post-layout simulation of the inverter
3	4/5	10	TR-level schematic design, TR sizing, pre-layout simulation of the XOR gate
4	4/14	10	A rough layout of the XOR gate
5	4/23	10	DRC, LVS, PEX, and post-layout simulation of the XOR gate

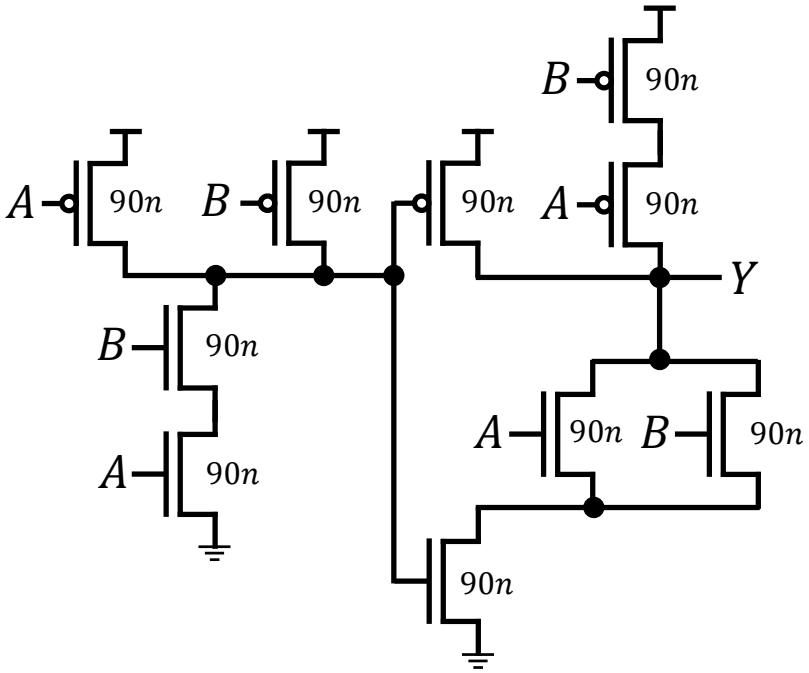
Grading Criteria

- Completion of Lab 2: 100 points
  - Even if you can't complete your work by the deadline, you can still submit your work so that you can get some partial credits.
- If you meet the following deadlines, you will get some extra points.

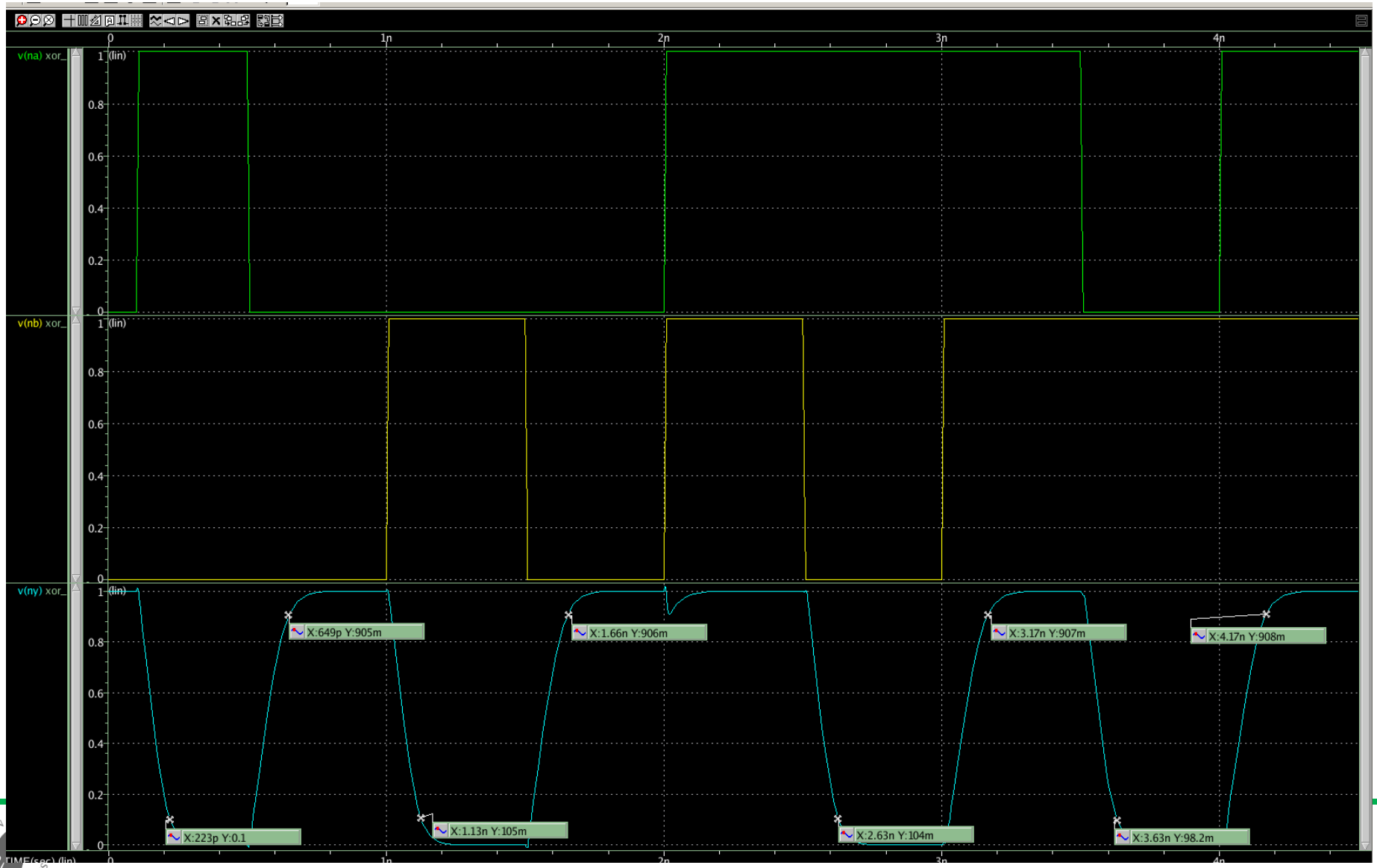
Step	Date	Points	What to do
1	3/22	10	A rough layout of the inverter in the tutorial (Submit a layout screenshot) (The layout should look like an inverter. Some DRC errors are accepted. Some LVS errors are accepted, but it shouldn't have noticeable LVS errors.)
2	3/29	10	DRC, LVS, PEX, and post-layout simulation of the inverter (Submit drc.results, drc.summary, lvs.report, and a screenshot of the I/O waveforms. Show the data points in the waveform snapshot.) (No DRC error, no LVS error.)
3	4/5	10	TR-level schematic design, TR sizing, pre-layout simulation of the XOR gate (Submit a snapshot of your schematic with TR width shown, pre-layout simulation files (LVS.sp, pre.sp), and a screenshot of the I/O waveforms. Show the data points in the waveform snapshot) (The worst-case rise and fall delays of the pre-layout simulation should be < 180ps.)
4	4/14	10	A rough layout of the XOR gate (Submit a layout screenshot) (The layout should look like an XOR. Some DRC errors are accepted. Some LVS errors are accepted, but it shouldn't have noticeable LVS errors.)
5	4/23	10	DRC, LVS, PEX, and post-layout simulation of the XOR gate (Submit drc.results, drc.summary, lvs.report, and a screenshot of the I/O waveforms. Show the data points in the waveform snapshot.) (No DRC error, no LVS error, the worst-case rise and fall delays of the post-layout simulation should be < 220ps.)

Sample Report: XNOR2 (Schematic)

- TR-level schematic



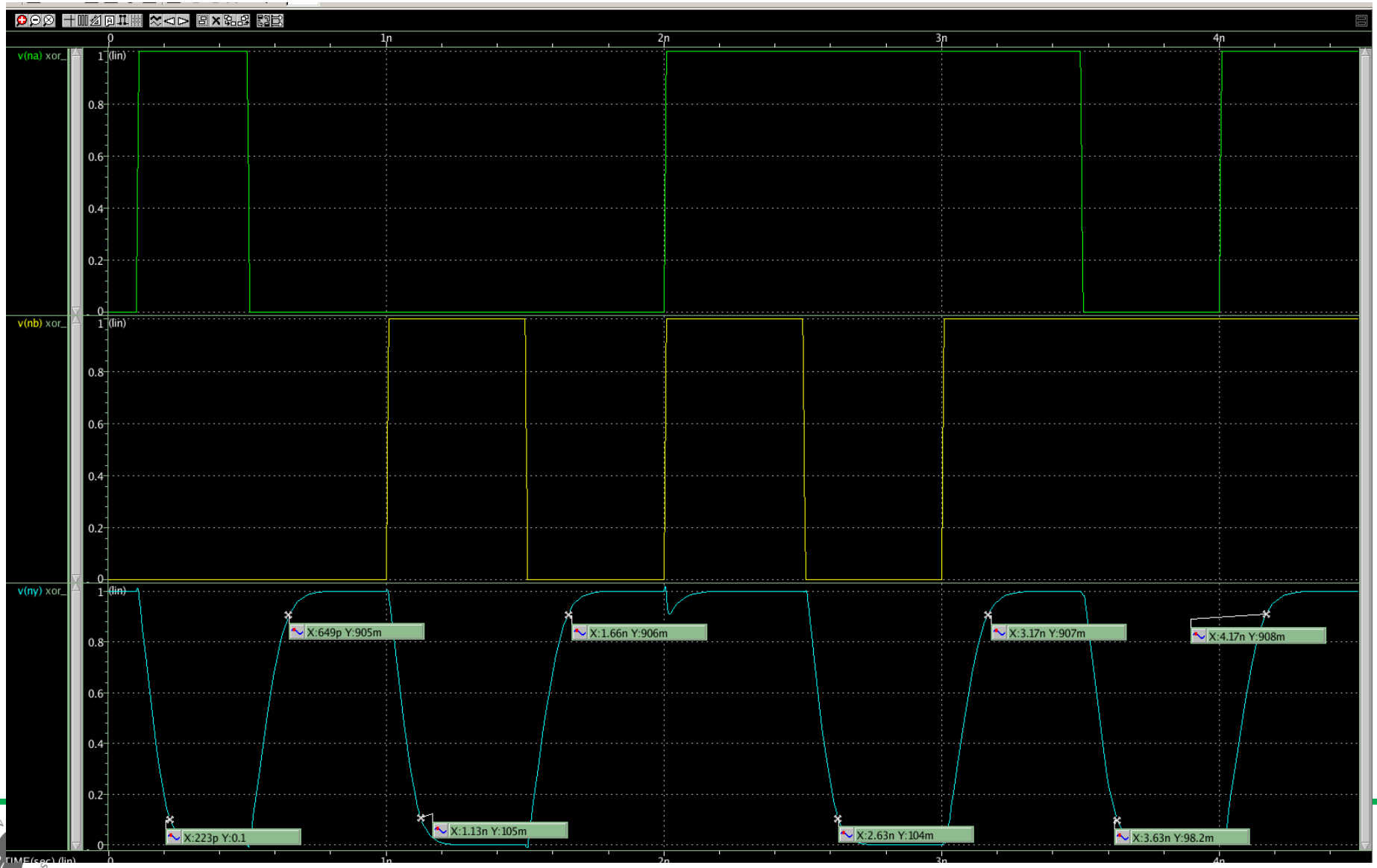
Sample Report: XNOR2 (Pre-layout sim)



Sample Report: XNOR2 (Layout)

- A layout

Sample Report: XNOR2 (Post-layout sim)



Sample Report: XNOR2 (Delays)

- Layout width: 1.8um
- Layout height: 1.8um
- Rise delays

Input (A,B)	Delay
(0,0) → (0,1)	100ps
(0,0) → (1,0)	100ps
(1,1) → (0,1)	100ps
(1,1) → (1,0)	100ps

- Fall delays

Input (A,B)	Delay
(1,0) → (0,0)	100ps
(0,1) → (0,0)	100ps
(1,0) → (1,1)	100ps
(0,1) → (1,1)	100ps