EE 586

Course Project

Project Report Due on 9th December 2021

Demo Due by 9th December 2021

Comparative performance evaluation of dynamic and static flip-flops

This design project consists of following specific goals.

(1) Performance evaluation of semi dynamic flip-flops: consider the following three types of semi dynamic flip-flops: (a) implicit-pulsed, data-close-to-output, semi dynamic hybrid flip-flop (*ip-DCO*) [1], (b) hybrid latch-flip-flop [2] and (c) semi dynamic edge-triggered flip-flop [3]. First, obtain the energy vs. delay characteristics of these three semi dynamic flip-flops. Then obtain the energy*delay product as a function of delay. Establish a detailed comparative evaluation in terms of D-Q delay, minimum E*D product point, total device width and total energy. Please undertake this analysis in 65 nm technology node.

(2) Implicit-pulsed static flip-flops: In the next step you are required to design a time-borrowing master-slave flip-flop (*tb-SMS*) [1]. Compare the performance of this static flip-flop with the best of the above mentioned semi dynamic flip-flops. Once again, you need to undertake the design and the analysis in the 65 nm technology node.

(3) Among all the above flip-flops which one is the fastest? Is the fastest design most energy efficient? Which one you should use in high-speed operation? Which one should be used for majority of the data paths?

(4) You need to submit a detailed report in the form of an IEEE 6-page conference paper. You need to explain operation of each circuit clearly and justify your claim with suitable experimental results. The questions asked in the point (3) above need to be answered in the paper. You are welcome to add any new reference you want to add to enhance the quality of your work.

Please follow the following references for this project:

1. J. Tschanz et al., “Comparative Delay and Energy of Single Edge-Triggered & Dual Edge-Triggered Pulsed Flip-Flops for High-Performance Microprocessors”, ISLPED’01, August 6-7, 2001, Huntington Beach, Califomia, USA.

2. H. Partovi et al., “Flow-Through Latch and Edge-Triggered Flip-flop Hybrid Elements” 1996 IEEE International Solid-state Circuits Conference (ISCC).
3. Fabian Klass et al., “A New Family of Semi dynamic and Dynamic Flip-Flops with Embedded Logic for High-Performance Processors” IEEE Journal of Solid-State Circuits, vol. 34, no. 5, may 1999.