Evaluation of Semi-Dynamic Flip-Flops and Static Flip-Flop based on Delay and Power

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***Abstract*— This paper provides a comparative analysis of various flip-flop topologies including implicit-pulsed semi-dynamic flip-flop (ip-DCO), Hybrid latch-flip-flop (HLFF), semi-dynamic edge-triggered flip-flop (SDFF), and Time-borrowing static master-slave (tb-SMS) flip-flops in terms of Delay and Energy. As a result of the comparative analysis, ip-DCO has the lowest Data to Q delay, while tb-SMS is the most power-efficient flip-flop.**

Keywords—Flip-flop, power-efficiency, delay, energy and power product

I. INTRODUCTION

Low power consumption and high speed have become very important design issues in VLSI. As integrated circuits' transistor density is associated with Moore's law, power consumption, area saving and performance has always been a big concern when we do VLSI design. In this case, Flip flop's power-speed performance and size are the fundamental elements. The trade-off within the power, speed, and total size of any flip-flop is significantly important for a design engineer.

In this paper, we introduce three semi-dynamic flip-flops and one static flip-flop and also briefly explain their operation. In order to find the best flip-flop according to their speed, sizing, and power consumption, we first determine the best one within the three semi-dynamic and secondly compared it with the static flip-flop based on their D to Q and energy-delay characteristics, energy and delay produce results.

The paper is organized as follows. Section 2 describes the simulation environment and the method that results in experiment results. Section 3 clearly presents the operating process of each flip-flop. Section 4 gives a detailed comparison between each semi-dynamic flip-flop and also the static flip-flop. Finally, we concluded the paper in Section 5.

II. SIMULATION PROCESS

All simulations presented in this paper are performed on TSMC 65nm transistor models using Cadence Spectre. The temperature and other settings are set as default settings. Also, all the experiment results are under 3Ghz clock pulse, 1.0v Vdd.

We measured D to Q delay by measuring the time between the rise of the clock and the change of Q at Vdd/2. During the simulation, we measured the delay and power of each flip-flop on the premise of successfully running the flip-flops, no matter latching "1" or latching "0". We only measure the D to Q delay of Q's rising time, for the convenience of comparison.

As for the input D, we set it to be stable right before the CLK edges come in order to transfer stable input data. This assumes that the clock triggering edge and pulse has enough time to capture the data input change. Since we provide stable inputs before the CLK edge, we measure the CLK to Q delay as the D to Q delay.

There are several basic performance metrics that are used to qualify a flip-flop and compare it to other designs. We use D to Q delay and energy-delay product to measure the performance of flip-flops.

Similar to the energy-delay product, the power–delay product (PDP) is a figure of merit correlated with the energy efficiency of a logic gate or logic family. Also known as switching energy, it is the product of power consumption P (averaged over a switching event) times the input-output delay or duration of the switching event D. It has the dimension of energy and measures the energy consumed per switching event [1]. Since we can obtain average power in Cadence Spectre, we can calculate the energy per-cycle through the function that E/cycle= average Pwr * one cycle period.

Clock-to-Q delay is also called propagation delay from the clock terminal to the output Q terminal. This is assuming that the data input D is set early enough with respect to the effective edge of the clock input signal [2].

Furthermore, there is a constant load capacitance for each flip flop, which is 10f F. The design of an explicit clocking pulse should make sure that the pulse width is large enough, such that the data will be correctly captured [3]. The typical pulse is 55ps to 60ps which is less than half of the clock period for 3Ghz in order to guarantee the pass the data from input to Q. We use the same pulse for ip-DCO, HLFF, and tb-SMS, while for SDFF is different. We would illustrate it on the related part.

III. Operation of Each Circuit

A. Implicit pulse semi-dynamic flip-flop

Semi-dynamic flip-flop composes of a dynamic state coupled to a pseudo-static state is appropriate for the application of high-speed needing and less concern on the power [2]. Figure 1 is an implicit pulsed semi-dynamic flip-flop as it donates a combination of dynamic part and static part. The two back-to-back inverters are used to avoid the dynamic nodes and the three inverters linked to the Clk are for generation delay pulse. The final inverter is a buffer that isolates the previous semi-dynamic node from the output.

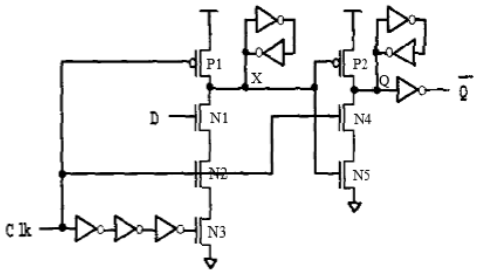

Figure 1: Implicit pulsed semi-dynamic flip-flop (ip-DCO) [3].

As the falling edge of the Clk comes, N2 is off while P1 is on; so the flip-flop enters the pre-charge state. X node would be pre-charged to logic"1". At this moment, N4 and P2 are both off, so the Q node holds its previous value with the help of back to back inverter.

When Clk comes to its rising edge, then the circuit is under evaluation period. Since the circuit has delayed pulse generation by the three inverters after the Clk signal when Clk reaches the rising, the input signal of N3 has a delay compared to Clk and it still remains high. In this case, N2 and N3 are on while P1 is off. Therefore, the voltage level of X depends on the value of D; If the voltage level of D is logic "0", N1 off, such that X would remain high. Because X and Clk are high now, N4 and N5 are on leading to a path from Q to ground, Q will be flop to logic "0". Similarly, During the evaluation period, if D is logic "1", N1, N2, and N3 would be on. Then, there would be a path from X to GND. X changed to level high, so N5 is off and P2 would be on. In this case, Q would be charged to logic “1”. The evaluation period depends on the delay of the three inverters. Remind that the evaluation period should be long enough to latch data from D to Q.

B. Hybrid latch-flip-flop

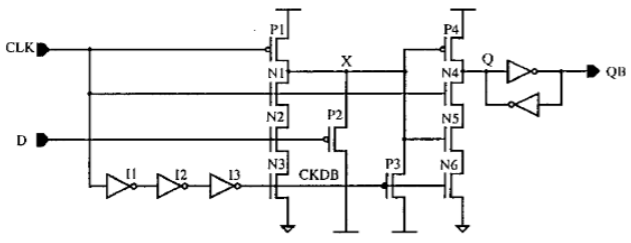

Figure 2: Hybrid latch-flip-flop (HLFF) [4]

HLFF sample the data at one edge of the clock, and this can eliminate the retardation of data flow on the opposite side edge, which is similar to a latch that can minimize the effect s of clock skew on cycle time [4]. To introduce the circuit, I1, I2, and I3 inverters are set to delay CLK to CKDB for generating a suitable pulse. The back-to-back inverter near output is to keep the circuit to be semi-dynamic.

When the falling edge of the CLK signal comes, the circuit reaches the pre-charge state; P1 is on while N2 is off, X node would be pre-charged to a voltage high. Moreover, since both N4 and P4 are off at the moment, Q would keep its voltage level with back-to-back inverters.

As the rising edge of CLK comes, CKDB would still remain at a high voltage level due to the delay of I1, I2, and I3. At the state, N1, N3, N4, and N6 are all on. X's voltage level would be depended on the input D, the circuit would be at the evaluate state. If D is logic “0”, N2 would be turned off, and P2 would be turned on, X node would be charged by the path containing P2. Such that, N2 would be turned on, which activates a path from Q to ground. Hence, it would latch a logic "0" from D to Q. If D is logic 1 during the evaluation period, N2 would be turned on, so X would be discharged to a low level. Because X is low, N5 is off while P4 would be turned on, Q would be a charge to logic "1". After this process, D is latched to Q no matter logic "1" or logic "0".

The designs on I1, I2, and I3 are important for the operation of HLLF because, during the evaluation period, data D and Q are transparent; the latency of the three inverters determines the evaluation period length should be large enough to transfer D to Q.

C. Semidynamic edge-triggered flip-flop

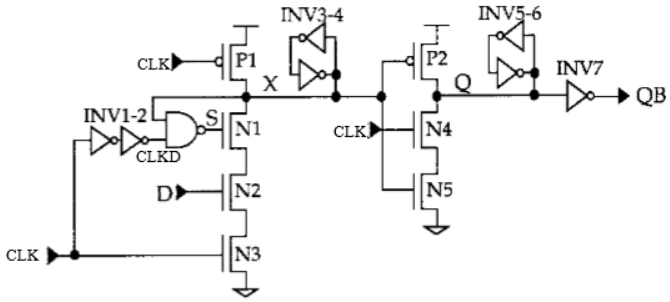

Figure 3: Semidynamic edge-triggered flip-flop (SDFF) [5]

As we have introduced the previous two kinds of semi-dynamic flip-flops, they are both have the same shortcoming in terms of the evaluation period. The timing of the evaluation period which is also called the sampling window is critical for those two flip-flops. A short sampling window can lead to metastability or functional failure while a long sampling window may affect the hold time would be increased [5]. Figure 3 is a Semi-dynamic edge-triggered flip-flop that is more robust. Inverter 3-4 and Inverter 5-6 are used to reduce dynamic factors keeping Q to be stable. A NAND gate is introduced to form conditional shutoff related to input D.

Introducing inverter 1-2 is to delay the CLK. Inverter 7 is a buffer that generates a stable complement signal from Q to QB.

When the clock comes to its falling edge, N3 is turned off while P1 is on. X node would be pre-charged to a high voltage level. Q would hold its previous voltage level since P4 and N6 are both off.

As the rising edge of CLK comes, the evaluation period begins; since there is a delay on CLKD because of INV1-2, CLKD still remains low. S is high, and N1is still turned on. If D is latching a logic "0" and such N2 off, X will be remained at a high keeping value by INv3-4. In this case, Q will be pulled down to GND since N4 and N5 are both turned on. If D is latching a logic "1", there is a path from X node to GND, pulling down the voltage level of X. P2 will be turned on resulting in Q being charged to logic high, and INV7 would drive QB to low. Notice that once the X node is pulled down to logic 0, the S node would be forced to stay at a high voltage level, such that the path of INV1-3 would remain active. The introduction of NAND can reduce the sampling window and yield a shorter time than the previous two circuits. We design the same delay from CLK to S as the typical pulse, which is close to 60ps.

D. Time-borrowing static master master-slave flip-flop

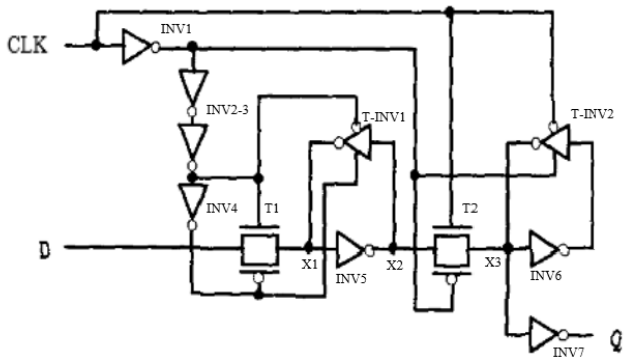

Figure 4: Time-borrowing static master master-slave flip-flop (tb-DCO) [3]

The most commonly used static flip-flop is the time-borrowing static master master-slave flip-flop [3]. The flip-flop implements two inverters which are INV2 and INV3 to generate a delay pulse in order to latch D to X3 within the pulse period. Also, it has two tristate inverters that are controlled by CLK and its delay signals in order to keep logic high or low level for nodes X1, X2, and X3. Compared to the signal to the previous semi-dynamic circuit, the flip can provide a statable output signal without adding a complement state QB. Follow will describe the operation process of the circuit.

Before the arrival of CLK rising edge, Pass-transistor T1 and T-INV2 are both on. T-INV2, INV6, and INV7 help X3 and Q hold their previous voltage level. Also, D can pass its voltage level to X1 and pass its complement signal to X2 because T1 is on. If D arrives before CLK's rising edge, D can definitely be transferred to X2.

As the CLK rising edge comes while the delay CLK signal after INV4 is still at low, pass-transistor T2 would be turned on while T1 is still on T2 can pass the Date from D or X2 to X3. X3 also would latch the data to Q. After the delay of INV1-4, the pass-transistor T1 would be turned off. Node X2 and X1 would keep their previous high or low voltage level because T-INV1 is off at the moment. This operating process is the same no matter what the input signal that D passes. Remind that if D is arriving before the CLK rising edge, D can latch to X2 in advance, which would drive the circuit faster. Also, the path from X1, X2, and X3 did not have a conditional path to the ground leading to leakage; it means that the circuit doesn't need a keeper to hold those nodes' voltage levels. This could reduce much energy than those semi-dynamic flip-flops.

IV. COMPARISON BETWEEN FLIP-FLOPS

In the previous section, we briefly introduced the character of the flip-flops and their operation process. In order to find the best semi-dynamic flip-flop regarding power consumption and delay, we evaluate their energy and delay characteristics and energy& power products for each semi-dynamic flipflop. After we got the best circuit within the semi-dynamic flip-flop, we compared it with the static flip-flop.

A. Comparison between semi-dynamic flip-flops

The energy versus delay characteristic of the three flip-flops including ip-DCO, HLFF, and SDFF is shown in Figure 4(a), while Figure 4(b) presents the energy*delay product as a function of delay.

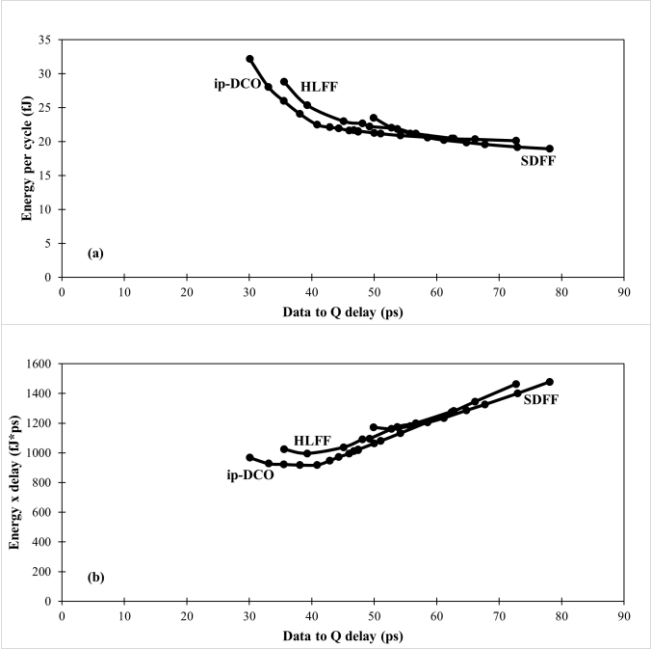

Figure 4: Comparison of semi-dynamic flip-flops. (a) Energy versus delay. (b) Energy * Delay product

As we can see from Figure 4(a), ip-DCO can provide a much smaller D to Q delay, while HLFF's D to Q delay can only reach around 35ps. Furthermore, SDFF can only reach 49ps, which is the worst one according to the smallest D to Q

delay. In this case, ip-DCO is much more suitable for high-performance processors since it can provide low latency D to Q delay.

Regarding Figurer 4(b), the energy*delay product can indicate the power and speed performance of a circuit. As we can see from the figure, during low D to Q x-axis, such as 40ps to 55ps, ip-DCO still provides the smallest energy*delay product compared to HLFF. Moreover, when the D to Q delay is around 58ps to 70ps, all the three circuits' results are close, but ip-DCO has the largest energy*delay product value.

Table I shows the comparison of D to Q delay for equal energy at 25fJ per cycle, minimizing energy*delay product point. Also, it shows a comparison of the energy*delay point, total width, and total E when the D to Q delay is 60 ps.

Table I presents that both HLFF F and ip-DCO are better than SDFF in terms of D to Q delay when energy per-cycle is 25fJ, energy*delay point, total width and energy when D to Q delay is 60ps. SDFF can not be placed high-speed processor because SDFF can not reach the same D to Q delay as low as HLFF and ip-DCO.

TABLE I. COMPARISON BETWEEN SEMI-DYNAMIC FLIP-FLOPS

	D-Q ***(E=25fJ)***	***Min-E*D***	***E*D*** ***(D-Q=60ps)***	***Total Width*** ***(D-Q=60ps)***	***Total E*** ***(D-Q=60ps)***
SDFF	49.89ps	1162.8	1235.2	13.8u	20.2fJ
HLFF	39.25ps	996.21	1174.8	12.6u	21.8fJ
Ip-DCO	35.51ps	918.3	1274.4	11.52u	20.4fJ
SDFF	*ref*	*ref*	*ref*	*ref*	*ref*
HLFF	21.3% better	14.3% better	4.8% better	8.6% better	7.9% better
Ip-DCO	49.1% better	21.0% better	3% worse	16% better	0.9% better

Based on the experiment results, ip-DCO has the best performance of D to Q delay and energy*delay product. Also, its total width is also less than both HLFF and SDFF. Among all the above flip-flops, ip-DCO is the fastest one. Also, the fastest design is most energy-efficient in regards to the minimum energy*delay product. However, as we can see in Figure 4(b) when we consider the delay from 60ps to 70ps, SDFF is the most power-efficient circuit, so we should trade off this characteristic. In high-speed operation, we can use ip-DCO as a flip-flop since it can reach much less D to Q delay than the other two. When we consider power consumption as the priority factor, SDFF produces the smallest energy per cycle at 60ps to 70ps delay. Therefore, SDFF can be used for the majority of the data paths when we only consider the three semi-dynamic circuits.

B. Comparison between ip-DCO and tb-SMS

As the D to Q delay decreases, the power consumption could be significantly increased especially when the D to Q delay is initially set to low. We can see that all the three semi-dynamic flip-flops present the characteristic. Large power consumption may be caused by the pre-charge and evaluation period due to the dynamic characteristic when the input is held constant [1]. Previously, considering the above-mentioned semi-dynamic flip-flops, we choose ip-DCO as the best one regarding energy*delay product. In this part, we compare the performance of semi-dynamic flip-flop ip-DCO and the static flip-flop tb-SMS.

Figure 5(a) shows the energy versus delay characteristic of the two flip-flops including semi-dynamic flip-flop ip-DCO and the static flip-flop tb-SMS. Also, the energy*delay product as a function of delay is presented in Figure 5(b).

As we can see from Figure 5(a), tb-SMS always provides a lower Energy consumption when we consider the same D to Q delay. Moreover, the energy*delay product has a significant gap. As a result, tb-SMS's power efficiency is better than ip-DCO.

Semi-Dynamic Flip-Flop ip-DCO is a high-performance flip-flop because of its small delay and simple topology, while tb-SMS is much more energy efficient because it consumes less power when they are at the same D to Q delay.

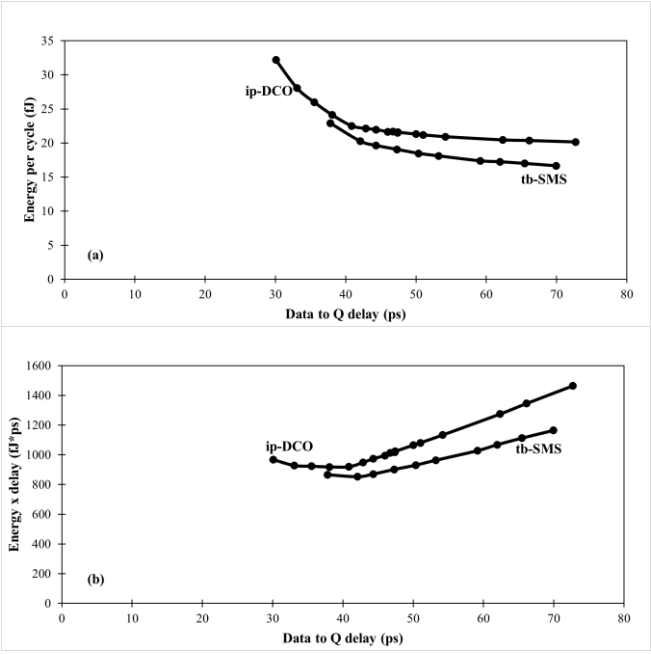

Figure 5: Comparison of semi-dynamic flip-flops ip-DCO and static flip-flop tb-SMS. (a) Energy versus delay. (b) Energy * Delay product

Among all the above flip-flops ip-DCO is the one that has the faster D to Q delay. However, the power consumption increases significantly as it designs to have low latency. The main reason for this might be the dynamic power

consumption during the evaluation period. This has determined that it cannot be the most energy-efficient circuit when it is compared to static flip-flops. Since there is no dynamic part inside tb-SMS, tb-SMS results in less power consumption.

Table II shows the comparison of the minimum energy*delay product points. Also, it shows a comparison of the energy*delay point, total width, and total E when the D to Q delay is 60ps. Based on the table, we can easily detect that tb-SMS is more power-efficient than ip-DCO since its energy*delay product (D-Q=60ps) is more than 40 percent better than ip-DCO. Furthermore, due to the result that can reach the same D to Q delay with less total size, tb-SMS is more saving at the area when they perform in the same speed processor. Therefore, when we consider the highest speed, ip-DCO is the best choice. However, Tb-SMS can be used for the majority of the data paths because it's power efficiency.

TABLE II. COMPARISON BETWEEN IP-DCO AND TB-SMS

	Min-E*D	***E*D*** ***(D-Q=60ps)***	***Total Width*** ***(D-Q=60ps)***	***Total E*** ***(D-Q=60ps)***
Ip-DCO	918.3	1274.4	11.52u	20.4fJ
Tb-SMS	852.6	1027.7	7.92u	17.3fJ
Ip-DCO	*ref*	*ref*	*ref*	*ref*
Tb-SMS	7% better	19% better	31% better	15% better

V. CONCLUSIONS

In order to find the best flip-flop in terms of power performance among ip-DCO, HLFF, SDFF, and tb-SMS, we measure energy vs. delay characteristics of these three semi-dynamic flip-flops as well as the static flip-flop. Furthermore, we obtain the energy*delay product as a function of delay according to the energy vs. delay characteristics.

As a result of the comparison among the three semi-dynamic flip-flops provides the lowest D to Q delay and the best power efficiency when they were both compared at high speed. However, when performing speed is secondly concerned, SDFF consumes less power than ip-DCO when they both have the same latency at high. Moreover, as D to Q delay reduce, all the flip-flops would definitely have higher power consumption. The trade-off is between energy-consuming and latency. After the trade-off, we determine that ip-DCO is the best flip flop among the three semi-dynamic flip-flops.

Compared to ip-DCO and the static flip-flop tb-SMS, tb-SMS has the lowest energy*power product at all the D to Q delay regions, which indicates that it is the most power-efficient. As tb-SMS can reach the same D to Q latency with lower total size, tb-SMS is more area-efficiency. However, ip-DCO provides smaller D to Q latency. By considering these factors, we can use ip-DCO in high-speed operations or critical paths. We can use tb-SMS for the majority of the data paths for reducing power consumption and area.

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