Latest Specifications:

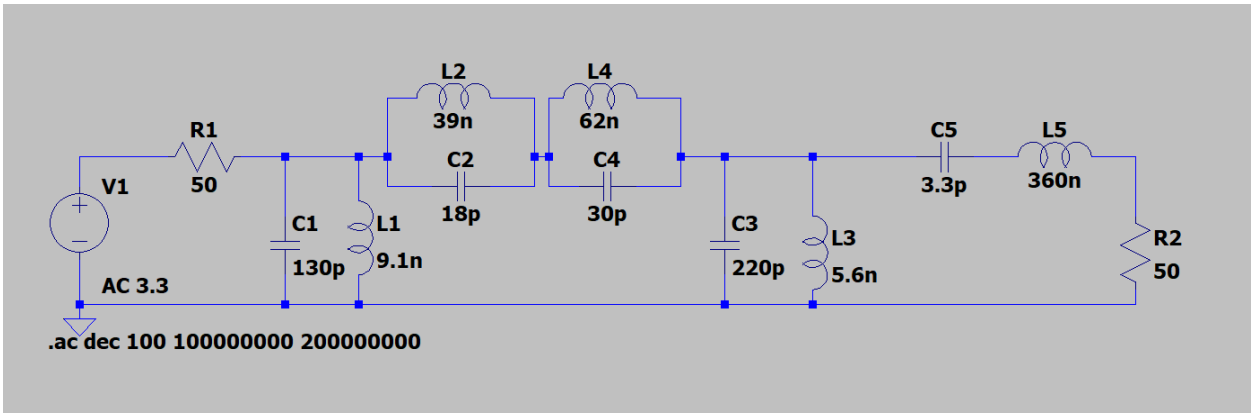
- The transmitter is **FM**. Specifically, we will use **FSK** (frequency shift keying), a type of FM transmission, to push telemetry data into the antenna
    - https://www.youtube.com/watch?v=ogJB5fiQ9kM&ab_channel=RohdeSchwarz
- Allowable frequency ranges are **144.90MHz-145.10MHz** (200kHz bandwidth) or **145.50MHz-145.80MHz** (300kHz bandwidth)
- The output power on the module should be between **30dBm and 33dBm** (1W to 2W)
- The output impedance on the antenna (both transmitting and receiving) should be about **50 ohms**
    - If not, we need to design a matching network (specifically a **pi-type match**)
- Radio Module PCB dimensions: **77mm x 47mm**

Current Goals:

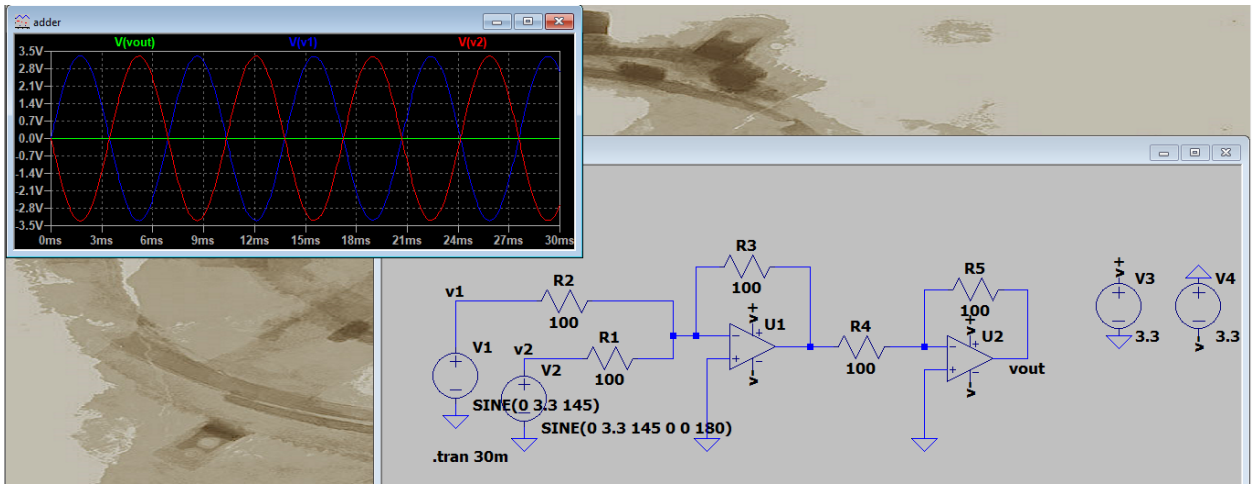
- Understand how FSK works and determine local oscillator/carrier frequencies for FSK
    - https://www.tutorialspoint.com/digital_communication/digital_communication_frequency_shift_keying.htm
    - https://www.researchgate.net/figure/A-block-diagram-of-frequency-shift-keying-FSK-modulation_fig1_264591517
    - 13_fsk.dvi (uct.ac.za)
        - This document helped us determine our equation to figure out the distance between our frequencies based on the bandwidth and bit rate.
    - chap6-5to6-11 (nctu.edu.tw)

- This document includes equations and methods for determining bit error of the FSK signals.

- Design a system block diagram for our transmitter with FSK
    - Pick a mixer, local oscillator, power amplifier
- Design a circuit schematic for transmitter
    - Design bandpass filter:

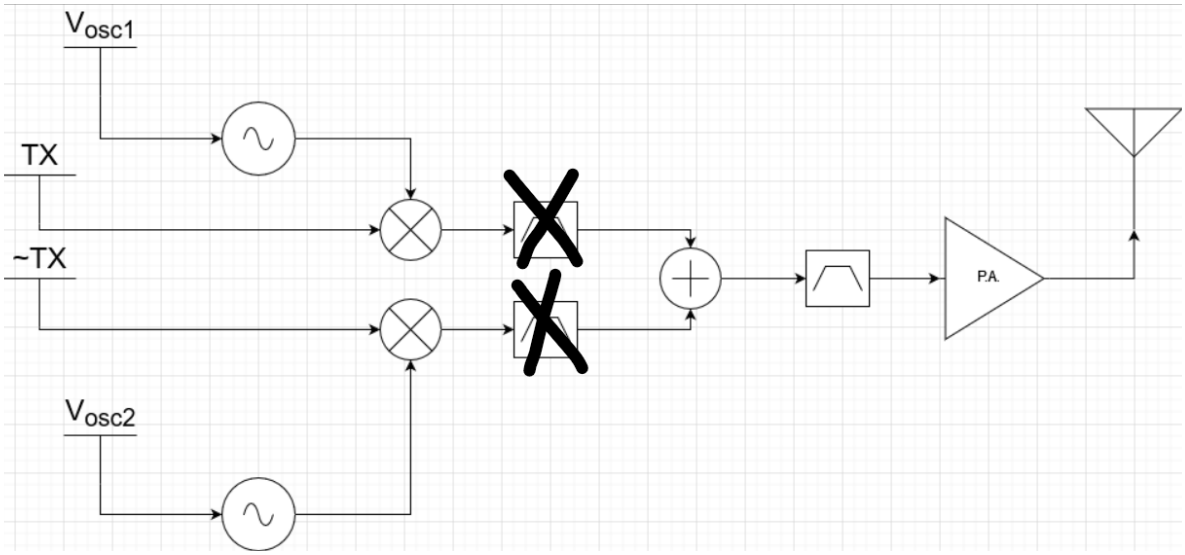


- Design signal adder:



- Make parts list with prices
- Test voltage output on Teensy 4.1 for signal noise and HIGH/LOW thresholds
- We can start with the straightforward transmitter system architecture in this article:
    - https://eng.libretexts.org/Bookshelves/Electrical_Engineering/Electronics/Microwave_and_RF_Design_I_-_Radio_Systems_(Steer)/03%3A_Transmitters_and_Receivers/3.04%3A_Receiver_and_Transmitter_Architectures
    - The goal is to have >1W transmission (within 30dBm to 33dBm) in our assigned VHF range (141.1MHz - 148.0 MHz).
    - >1W transmission tends to generate heat, so we may want to cool the transmission antenna with a heat sink
    - We can continue adding on features to the architecture after we finish the main transmission architecture.

Block Diagram:



Shopping List:

2 Local Oscillators

- https://www.digikey.com/en/products/filter/oscillators/172 (use this to look for LOs)
- We need to determine FSK separation frequencies before choosing specific carriers

2 Mixers

- https://www.nxp.com/docs/en/data-sheet/SA612A.pdf

1 Power Amplifier

- https://www.digikey.com/en/products/detail/cml-microcircuits/CMX902QT8/9698678

1 Band-Pass Filter

- **We designed this ourselves**
- **https://rf-tools.com/lc-filter/ (use for elliptic filter design)**

Testing Antenna

- **QWB144 TE Connectivity Laird | RF/IF and RFID | DigiKey**

2 Op-Amps

- https://www.mouser.com/datasheet/2/609/AD8017-1502182.pdf

Lots of Capacitors, Inductors and Resistors to create Adders

VHF:

141.1MHz - 148.0 MHz

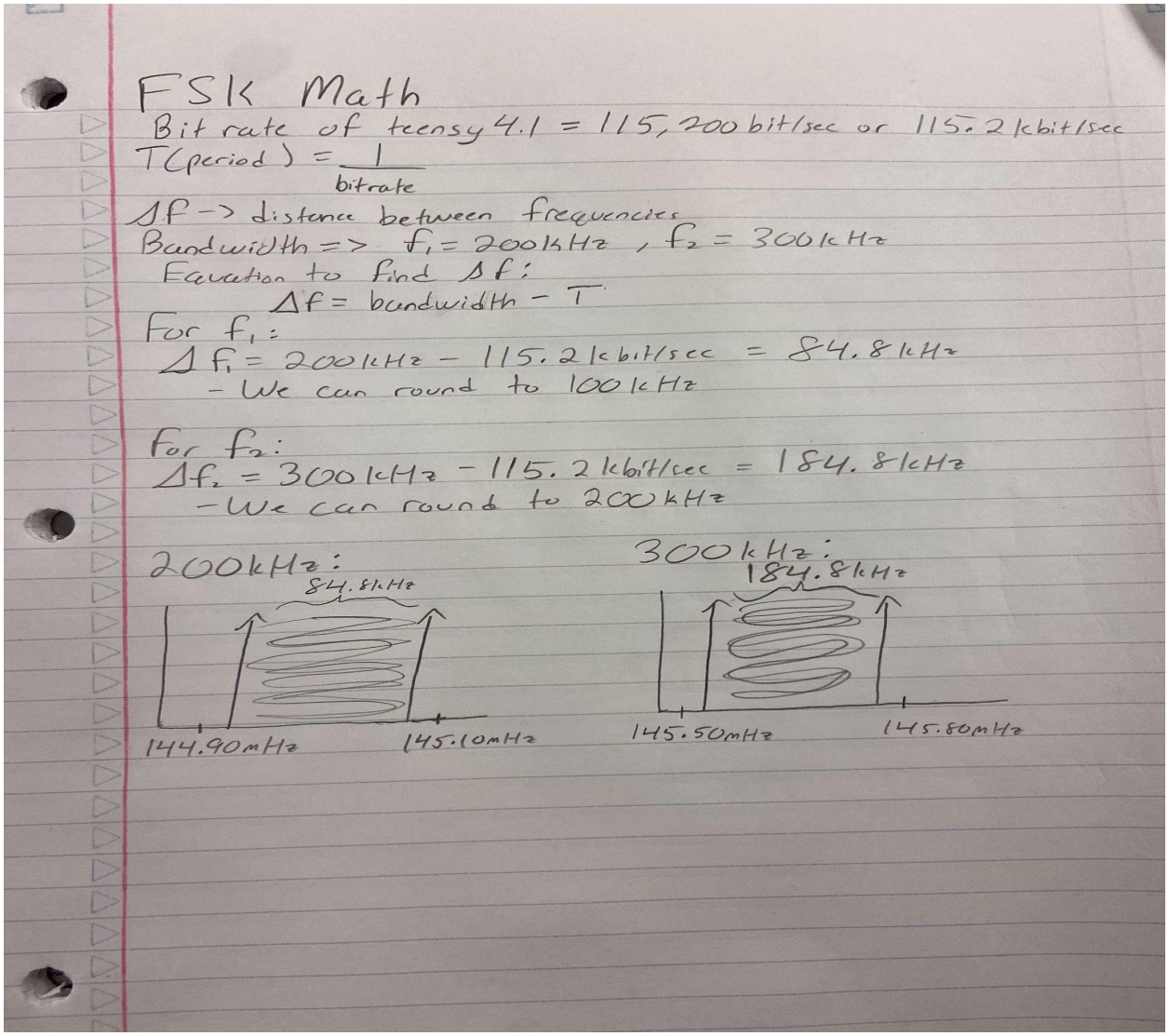
Bandpass design: After the signal frequency is ramped up on the output of the mixer, a bandpass in series with a power amplifier will push the signal out of the transmitting antenna at >1W. To meet VHF requirements, the bandpass filter will have the following specifications:

- The center frequency will be 144.55MHz. We can round this to 144.6Mhz
- Our assigned bandwidth is 6.9MHz
    - **Cutoff range:** 144.1MHz to 148MHz
    - For all passive designs, try to use around 100 ohms
        - **Use this article for the passive bandpass filter design:** Radio Frequency Filter Design: Vhf Bandpass Filter Using Discrete Components And Distributed Elements. [k546xkpkrw48] (idoc.pub)
        - Similar to article above https://www.electronics-notes.com/articles/radio/rf-filters/constant-k-simple-bandpass-lc-rf-filter-design-calculations.php
        - Many Bandpass filter designs using LC only: https://rf-tools.com/lc-filter/
    - For all active designs, most preferably a second order filter, use a thevenin equivalent of 100 ohms, or <1K ohms at most

- Therefore, the projected quality factor will be: 144.55MHz / 6.9Mhz = 20.95
- NOTE: resistors add current noise to the signal. We will want to use **carbon film or metal film resistors** to minimize this noise at ~146MHz
- Resistor voltage noise: $v_{noise} = \sqrt{4KTBR}$, where T is temperature, K is Boltzmann's constant, B is bandwidth
- We want low power resistors, so T should be low, R should also be low. Let's say R is 100 ohms and the temperature on the resistor is 40 deg C. Then:

$$v_{noise} = 1.234 * 10^{-7}\sqrt{R}$$

FSK Calculations:



(144.95MHz - 145.05MHz) and (145.55MHz - 145.75MHz)

- As shown, we have derived an equation that uses the Δf (distance between the frequencies), bandwidth, and the period which is found by taking 1/(bit rate). The bit rate is given from the teensy 4.1 in bits per second.
- The drawings show the frequency ranges for each bandwidth, the arrows drawn represent the epsilon value which is the distance in between the lower frequency and the arrow and the upper frequency and the arrow.

- Our next task is to determine the bit error and figure out how to make it as low as possible. This requires much more complex equations and calculations, there is a document posted under current goals that shows some of these equations.

Antenna: We will need to match the output impedance of the module to the ground antenna's impedance. Preferably 50 ohms for max power transfer. We will conduct testing with a network analyzer. If impedances don't end up matching, we will need to design a matching network. Article for matching examples and how to make a matching filter. It also tells you what they do: https://www.electronicdesign.com/technologies/communications/article/21801154/back-to-basics-impedance-matching-part-3

- Pi match is preferred. We can configure our own bandwidth (max of 6.9MHz), and we will minimize parasitic capacitance between the inductor and GND

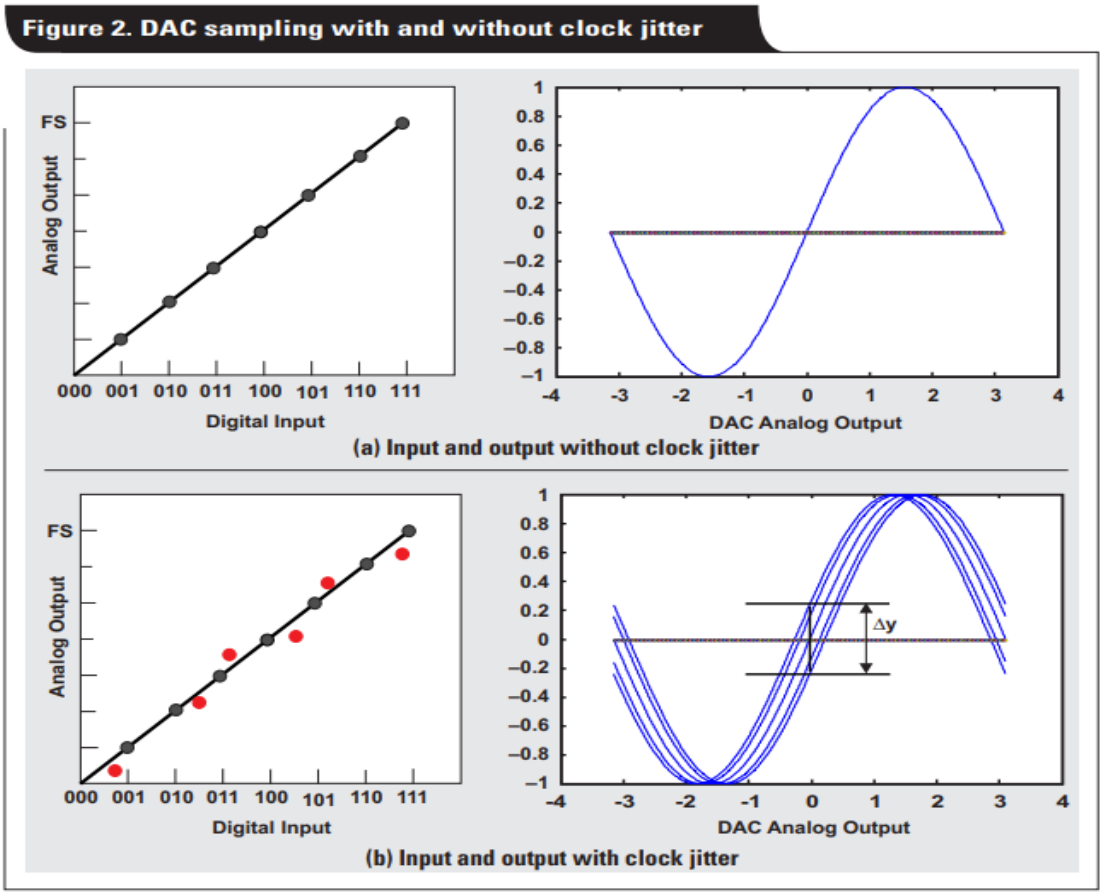
Useful Documents:

- Impact of Clock Noise
  - Analyzing the impact of clock noise on an RF-sampling DAC system (ti.com)
  - When testing the clock output focus on the jitter
    - Increase the slew rate (maximum rate of change of an op amps output voltage, aka dV/dT) to decrease jitter.
    - Buffer attached to the output of the clock
      - Say gain is 1, upping the dV/dT will decrease jitter. This could potentially increase the noise slightly as it would be

an RL System (Resistor-Inductor) and resistors create noise. However, this can be fixed by using a small resistance and band-pass filter to get rid of unwanted noise.

- Causes for clock jitter include trace attenuation and reflection. Lossy trace material of a PCB behaves like a low pass filter and will attenuate the clock signal; the attenuation will get worse as the trace length and frequency increase. Secondly, the clock signal overshoots or undershoots due to reflections in the trace. These reflections usually originate from unterminated traces and impedance mismatches.
    - To counter attenuation we choose a high swing mode
    - Since we are focusing on transmitters we should focus on series termination for the trace

Example of clock jitter:



In fig. a, the sine wave has a steady period of 6. But in fig. B, the jitter is causing the period to "vibrate" between periods of $6 \pm t_{\Delta y}$, where $t_{\Delta y}$ is the time induced by jitter. As a result, a region in the y-direction, Δy, is added as an offset.

- Basic Receiver and Transmitter Architecture
    - 3.4: Receiver and Transmitter Architectures - Engineering LibreTexts