RUTHVIK REDDY ANTHIREDDIGARI

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SUMMARY

I am a graduate with a strong foundation in digital design and FPGA development seeking an entry level role at your organization. With experience in Verilog and C for circuit design and implementation, I can develop and optimize circuits for performance, generate timing diagrams and smooth collaboration with others to complete projects.

EDUCATION

Manipal Institute of Technology, MAHE, Manipal Oct 2020 - July 2024

Bachelors in Technology, Major in Electrical and Electronics Engineering.

Relevant coursework : Basic Electronics, Analog System Design & LAB, Digital System Design & LAB, FPGA Design.

SKILLS

- **Languages**: Verilog, VHDL, Arduino, C, Assembly.
- **Tools**: LT SPICE, MATLAB/SIMULINK, PROTEUS, LABVIEW, Kiel uvision, KI-CAD.
- **RTL design tools**: Questa Sim/Model Sim, Xilinx Vivado, and Xilinx Vitis.
- **Hardware:** Altera Max V/10, Xilinx Zynq 7000, Artix-7, Arduino,ESP-32, 8051 uc, Analog and Digital IC's.

INTERNSHIP EXPERIENCE

Delta IOT Solutions Private limited, Hyderabad, India Mar 2025 – July 2025

Intern – Embedded

- Developed and implemented Embedded C code for Arduino and ESP32-based IoT projects.
- Assisted in designing custom PCBs based on existing schematics, supporting prototyping and hardware development.
- Helped in hardware testing, troubleshooting, and circuit board development, contributing to debugging processes.

Research Centre Imarat, DRDO , Hyderabad, India Feb 2024 – June 2024

Student/Project Intern

- Engineered a low-latency power-efficient video data streaming system using AXI4-Stream and AMBA protocols, reducing latency by 15% and power consumption by 10%.
- Designed and verified RTL using Verilog, implementing FSM-based control logic for fast and reliable data transfer on Xilinx FPGAs.
- Utilized Vivado and Vitis for code synthesis, implementation, testing, and timing validation to ensure design robustness.

Boeing India Private Limited , Bengaluru , India Jun 2023 – Aug 2023

Electrical Design and Analysis Engineer Intern.

- Developed UART interface with FIFO buffers using FSMs in Verilog, enabling reliable communication for FPGA-based systems.
- Used Intel Quartus and ModelSim for simulation, debugging, and verification, achieving timing and functional correctness.
- Contributed to 15% size reduction of product and 25% cost savings through code optimization and in-house product development

ACADEMIC RESEARCH

***Rectifier based buck converter prototype for charging* applications (Link)** Aug 2022 – May 2023

- Conducted research on diode rectifier based buck converters for efficient DC-DC voltage regulation, analyzing performance under varying input conditions and simulated models in LTspice and Simulink to optimize parameters.
- Achieve 10% improvement in charging efficiency and voltage stability, suits compact and low-cost, energy efficient application.

ACADEMIC PROJECTS

Emergency vehicle traffic clearing device using LabVIEW (Link) Aug 2022 – Nov 2022

- Developed a device that automatically changes the traffic lights in the direction of an emergency vehicle travelling to provide it with a hassle-free journey. Usage of Arduino Uno and NI LabView systems.

LPG Gas leakage detection system using 8051uc and Keil software (Link) Mar 2022 – May 2022

- Developed a system that will sound an alarm to alert nearby people about gas leakage and automatically switch off the electrical supply of the house to prevent the threat from sparks in the power supply.

CERTIFICATIONS

- Introduction to FPGA Design for Embedded Systems, Coursera – University of Colorado Boulder.(Link)
- Hardware Description Languages for FPGA Design, Coursera – University of Colorado, Boulder (Link)
- VLSI Design Flow : RTL to GDS, NPTEL – IIIT, Delhi (Link).