Indian Institute of Technology Indore
Computer Science & Engineering
Final-Semester Examination (CS 206)
April 25, 2017

Full Marks: 60/ Duration: 3 hrs
(Answer all)

Q1. Derive the circuit of a 8: 3 encoder. **(4 MARKS)**

Q2. Draw the design abstraction levels of digital system design. **(4 MARKS)**

Q3. Using T-FF, design a counter that counts in the following sequence: 000 →100→010→101→111 and then repeats. **(10 MARKS)**

Q4. Implement the following using only 2:1 multiplexers: F = AB + AC + A'. **(6 MARKS)**

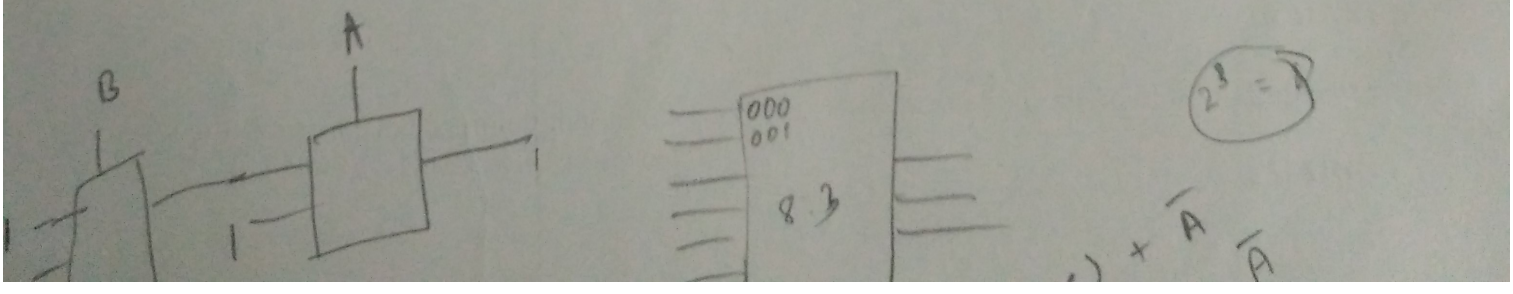
Q5. Design a synchronous gray code counter using J-K FFs. **(10 MARKS)**

Q6. Mention the various phases of synthesis, implementation, simulation and emulation of a Xilinx logic CAD tool with a flowchart. **(6MARKS)**

Q7. Design the circuit of a 3 bit odd parity generator. **(5 MARKS)**

Q8. Derive the Boolean expression of a 3 bit odd parity checker. **(5 MARKS)**

Q9. Design a decoder with three input lines but with only six output lines. If the value of the input corresponds to 6 or 7, then all output lines should be asserted to signal an error. **(10 MARKS)**



(5 MARKS)

Indian Institute of Technology Indore
Computer Science & Engineering
Mid-Semester Examination: Digital Logic Design (CS 206)
March 10, 2017

Full Marks: 40 / Duration: 2 hrs
(Answer all)

Instructor: Dr. Anirban Sengupta

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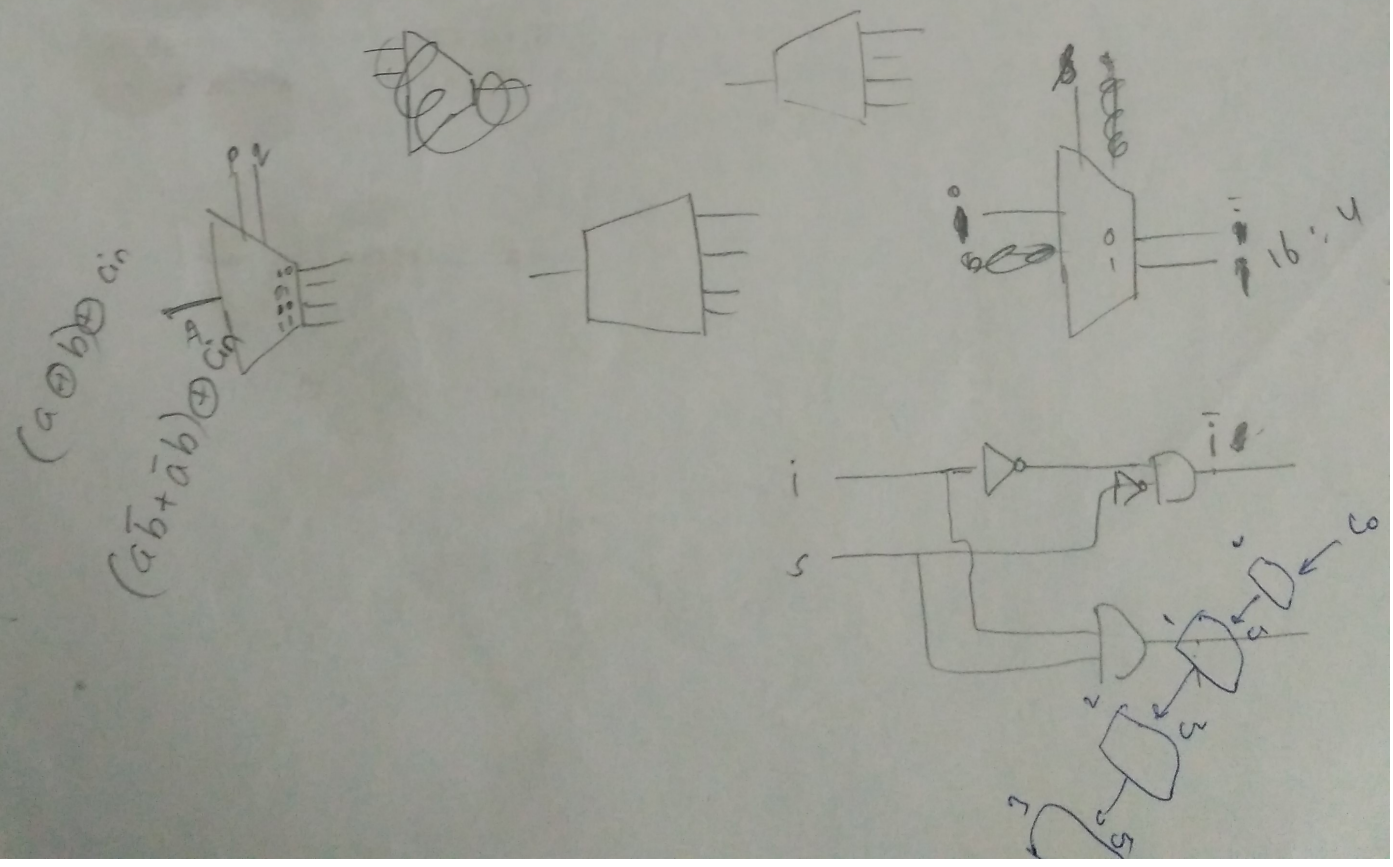
b) Write the structural VHDL code of a 4-bit FA. **(6 MARKS)**

Q5. Design a BCD adder using decoder which produces an output which is plus three of the input. **(5 MARKS)**

Q6. Realize the following function using one 8:1 Multiplexer (IC 74152).
$F(A, B, C, D) = \sum_m (2,4,6,7,9,10,11,12,15)$ **(3 MARKS)**

Q7 Use NAND gates only to derive a Full Adder circuit and Full Subtractor circuit. **(7 MARKS)**

Q8. Draw the circuit of a 1-4 demux using gates. **(4 MARKS)**

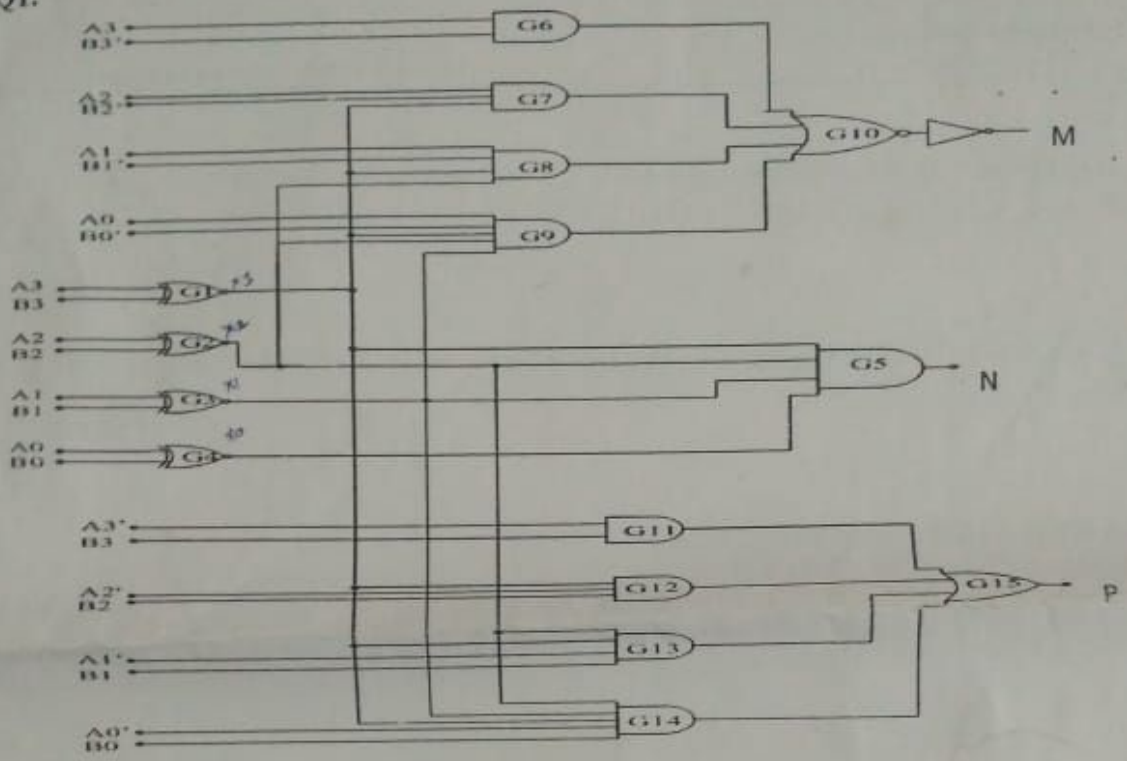


Mid-Semester Examination: Digital Logic Design (CS 206)
March 15, 2016

Full Marks: 50/ Duration: 2 hrs
(Answer all)

Instructor: Dr. Anirban Sengupta

Q1.



Consider the digital circuit above. Assume the outputs of G1, G2, G3 and G4 are x3, x2, x1 and x0 respectively. Design the truth table for the above circuit (by showing the derived Boolean expressions clearly for three outputs M, N and P).

(5 MARKS)

Q2. a) Write the VHDL code of a 2 bit Adder-Subtractor unit using XOR gate.

(5 MARKS)

Q3. Design the circuit of a 2 digit BCD adder.

(5 MARKS)

Q4. Show the process of evolution of JK flip flop from SR NAND Latch

(10 MARKS)

Q5. Derive expressions and circuit for priority encoder.

(5 MARKS)

Full Marks: 50/ Duration: 2 hrs
(Answer all)

Instructor: Dr. Anirban Sengupta

Q6. Realize the following function using one 8:1 Multiplexer (IC 74152).
$F(A, B, C, D) = \sum_m (2,4,6,7,9,10,11,12,15)$

(5 MARKS)

Q7. $F = AB + AC + BC$. Design a circuit using three multiplexers where A and B act as select lines.

(5 MARKS)

Q8. a) Write VHDL code for 4bit RCA.
b) Draw diagram of 4 bit CLA

(10 MARKS)