NE310H2
Hardware Design Guide

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APPLICABILITY TABLE

PRODUCTS

- NE310H2-W1

Contents

1. INTRODUCTION

1.1. Scope

This document introduces the Telit NE310H2 modules and presents possible and recommended hardware solutions for developing a product based on this module. All the features and solutions detailed in this document are applicable to all NE310H2 variants, where NE310H2 refers to the variants listed in the applicability table.

Obviously, this document cannot embrace every hardware solution or every product that can be designed. Where the suggested hardware configurations need not be considered mandatory, the information given should be used as a guide and a starting point for properly developing your product with the Telit module.

1.2. Audience

This document is intended for Telit customers, especially system integrators, about to implement their applications using the Telit module.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.5. Related Documents

- SIM Holder Design Guides, 80000NT10001a
- AT Commands User Guide, 1VV0301611
- xE310 TLB Documentation, 1VV0301617

2. GENERAL PRODUCT DESCRIPTION

2.1. Overview

The NE310H2 is part of a new generation of modules in Telit's NBIoT module portfolio.

With its compact LGA footprint, it is designed for those m2m applications requiring miniature foot print.

It is a multi band LTE NBIoT communication product based on the market' latest NBIoT core which allows integrators to plan on availability for even the longest lifecycle applications, highly recommended for new designs specified for NBIoT coverage worldwide.

It is highly recommended for new designs requiring NBIoT coverage in a small and robust LGA package, which implies easy integration and low impact on final application size and costs. Ease of production and small foot print makes it the ideal solution for applications in security alarms, automated meter reading, and pos terminals.

The NE310H2 operates with 1.8 V GPIOs, minimizing power consumption and making it even more ideally suited for battery powered and wearable device applications.

2.2. Product Variants and Frequency Bands

Product	2G Band (MHz)	3G Band (MHz)	4G Band (MHz)	Region
NE310H2-W1	-	-	B1, B2, B3, B4, B5, B8, B12, B13, B17, B18, B19, B20, B25, B26, B28, B66, B71, B85	Worldwide

Refer to "RF Section" for details information about frequencies and bands.

2.3. Target market

The NE310H2 enables enterprises to deploy new small footprint designs across many application areas including:

- Utility metering
- Home and commercial security
- POS devices
- Logistics terminals

2.4. Main features

Function	Features
Modem	• 3GPP Rel.14 LTE Cat.NB2 • SMS support (text and PDU) • Real Time Clock
Interfaces	• 3 UARTs (Main and secondary with flow control and Auxiliary with RX TX only) • USB 2 (debug only) • SPI • I2C • 6 GPIOs • Antenna pad

2.5. TX Output Power

Band	Power class
All Bands	Class 3 (23dB)

2.6. Mechanical specifications

2.6.1. Dimensions

The overall dimensions of NE310H2 family are:

- Length: 15 mm
- Width: 18 mm
- Thickness: 2.3 mm

2.7. Temperature Range

Condition	Range	Note
Operating Temperature Range	-20°C to +55°C	The module is fully functional(*) within this 3GPP temperature range and meets 3GPP specifications.
Extended Temperature Range	-40°C to +85°C	The module is fully functional(*) within this temperature range. The RF Performance may deviate from 3GPP requirements in this extended range. For example: receiver sensitivity or maximum output power may deviate by a few dB due to limitations of physics like higher thermal noise floor at high temperature.
Storage Temperature Range	-40°C to +85°C	-

(*) Functional: if applicable, the module is able to make and receive data calls, send and receive SMS and data traffic.

3. PINS ALLOCATION

3.1. Pin-out

Pin	Signal	I/O	Function	Type	Comment
Asynchronous Serial Port (USIF0) – Prog. / Data + HW Flow Control					
Y16	TXD0	I	Serial data input (TXD) from DTE	CMOS 1.8	
AA15	RXD0	O	Serial data output (RXD) to DTE	CMOS 1.8	
Y18	RTS0	I	Input for Request to send signal (RTS) from DTE	CMOS 1.8	
AA17	CTS0	O	Output for Clear to send signal (CTS) to DTE	CMOS 1.8	
Asynchronous Serial Port (USIF1)					
Y12	TXD1	I	Serial data input (TXD) from DTE	CMOS 1.8	
AA11	RXD1	O	Serial data output (RXD) to DTE	CMOS 1.8	
AA13	RTS1	I	Input for Request to send signal (RTS) from DTE	CMOS 1.8	
Y14	CTS1	O	Output for Clear to send signal (CTS) to DTE	CMOS 1.8	
USB 1.1 (Debug Port)					
U19	USB_D+	I/O	USB differential Data (+)		
V18	USB_D-	I/O	USB differential Data (-)		
T18	USB_VBUS	-	Power sense for the internal USB transceiver		Compliant to VUSB from USB2.0 specification (from 4.4 V to 5.5V)
Auxiliary UART					
Y10	TX_AUX	O	AUX UART (TX Data to DTE)	CMOS 1.8	
AA9	RX_AUX	I	AUX UART (RX Data from DTE)	CMOS 1.8	

SIM card interface					
L1	SIM_CLK	O	External SIM signal – Clock	1.8 V	
M2	SIM_RST	O	External SIM signal – Reset	1.8 V	
N1	SIM_DAT	I/O	External SIM signal – Data I/O	1.8 V	
P2	SIM_VCC	-	External SIM signal – Power supply for the SIM	1.8 V	
X	SIMIN	I	Presence SIM input	CMOS 1.8	See next chapters
DIGITAL IO					
V11	IO1	I/O	Configurable GPIO01 Alternate 1: I2C_SDA Alternate 2: SIMIN	CMOS 1.8	Using AT commands
V13	IO2	I/O	Configurable GPIO02 Alternate 1: I2C_SCL Alternate 2: SIMIN	CMOS 1.8	Using AT commands
D7	IO3	I/O	Configurable GPIO03 Alternate 1: I2C_SDA Alternate 2: SIMIN	CMOS 1.8	Using AT commands
D9	IO4	I/O	Configurable GPIO04 Alternate 1: I2C_SCL Alternate 2: SIMIN	CMOS 1.8	Using AT commands
D11	IO5	I/O	Configurable GPIO05 Alternate 1: SIMIN	CMOS 1.8	Using AT commands
D13	IO6	I/O	Configurable GPIO06 Alternate 1: SIMIN	CMOS 1.8	Using AT commands
ADC					
B18	ADC	I	Analog To Digital converter Input	A/D	10-bit range
RF Section					

A5	MAIN ANTENNA	I/O	Main Antenna (50 ohm)	RF	Main Antenna (50 ohm)
Miscellaneous Functions					
B2	S_LED	O	Status LED	CMOS 1.8V	
N16	ON_OFF*	I	Input Command for Power ON/OFF	CMOS 1.8V	Active LOW
R19	RST*	I	Reset	CMOS 1.8V	Active LOW
L16	WAKE*	O	Input Command to Wake from PSM	CMOS 1.8V	Active Low
R1	VAUX	O	Supply Output for external accessories / Power ON Monitor	Power	Max10mA
Audio Section					
C1	DVI_WA0	I/O	Digital Audio Interface I2S (WA0)	CMOS 1.8V	
D2	DVI_RX	I	Digital Audio Interface I2S (RX)	CMOS 1.8V	
E1	DVI_TX	O	Digital Audio Interface I2S (TX)	CMOS 1.8V	
F2	DVI_CLK	I/O	Digital Audio Interface I2S (BCLK)	CMOS 1.8V	
L4	DVI_MCLK	I/O	Digital Audio Interface I2S (MCLK)	CMOS 1.8V	
Bus SPI Master					
Y6	SPI_CS	O/I	SPI - Circuit Select	CMOS 1.8V	
AA7	SPI_CLK	O/I	SPI - Clock	CMOS 1.8V	
AA5	SPI_MOSI	O/I	SPI - MOSI	CMOS 1.8V	
Y8	DVI_MCLK	I/O	SPI - MISO	CMOS 1.8V	
Power Supply					
W1	VBATT_PA	-	Main power supply (Radio PA)	Power	
AA3	VBATT	-	Main power supply (Baseband)	Power	

A3	GND	-	RF Ground	Power
A7	GND	-	RF Ground	Power
A9	GND	-	RF Ground	Power
A13	GND	-	RF Ground	Power
A17	GND	-	RF Ground	Power
B4	GND	-	RF Ground	Power
B6	GND	-	RF Ground	Power
B10	GND	-	RF Ground	Power
B12	GND	-	RF Ground	Power
B14	GND	-	RF Ground	Power
B16	GND	-	RF Ground	Power
C19	GND	-	RF Ground	Power
D18	GND	-	RF Ground	Power
F8	GND	-	Thermal Ground	Power
F12	GND	-	Thermal Ground	Power
F18	GND	-	Thermal Ground	Power
G19	GND	-	Thermal Ground	Power
H6	GND	-	Thermal Ground	Power
H14	GND	-	Thermal Ground	Power
J19	GND	-	Thermal Ground	Power
K18	GND	-	Thermal Ground	Power

M18	GND	-	Thermal Ground	Power
N19	GND	-	Thermal Ground	Power
P6	GND	-	Thermal Ground	Power
P14	GND	-	Thermal Ground	Power
T8	GND	-	Thermal Ground	Power
T12	GND	-	Thermal Ground	Power
U1	GND	-	Power Ground	Power
V2	GND	-	Power Ground	Power
W19	GND	-	Power Ground	Power
Y2	GND	-	Power Ground	Power
Y4	GND	-	Power Ground	Power
RESERVED				
G1	RESERVED	-	RESERVED	
H2	RESERVED	-	RESERVED	
J1	RESERVED	-	RESERVED	
K2	RESERVED	-	RESERVED	
J4	RESERVED	-	RESERVED	
G4	RESERVED	-	RESERVED	
L19	RESERVED	-	RESERVED	
A11	RESERVED	-	RESERVED	
N4	RESERVED	-	RESERVED	

R4	RESERVED	-	RESERVED
E4	RESERVED	-	RESERVED
E16	RESERVED	-	RESERVED
U4	RESERVED	-	RESERVED
U16	RESERVED	-	RESERVED
V7	RESERVED	-	RESERVED
V9	RESERVED	-	RESERVED
P18	RESERVED	-	RESERVED
AA13	RESERVED	-	RESERVED
T2	RESERVED	-	RESERVED
E19	RESERVED	-	RESERVED
R16	RESERVED	-	RESERVED
H18	RESERVED	-	RESERVED
G16	RESERVED	-	RESERVED
J16	RESERVED	-	RESERVED
B8	RESERVED	-	RESERVED

WARNING

Reserved pins must not be connected.

If not used, almost all pins should be left disconnected. The only exceptions are the following pins:

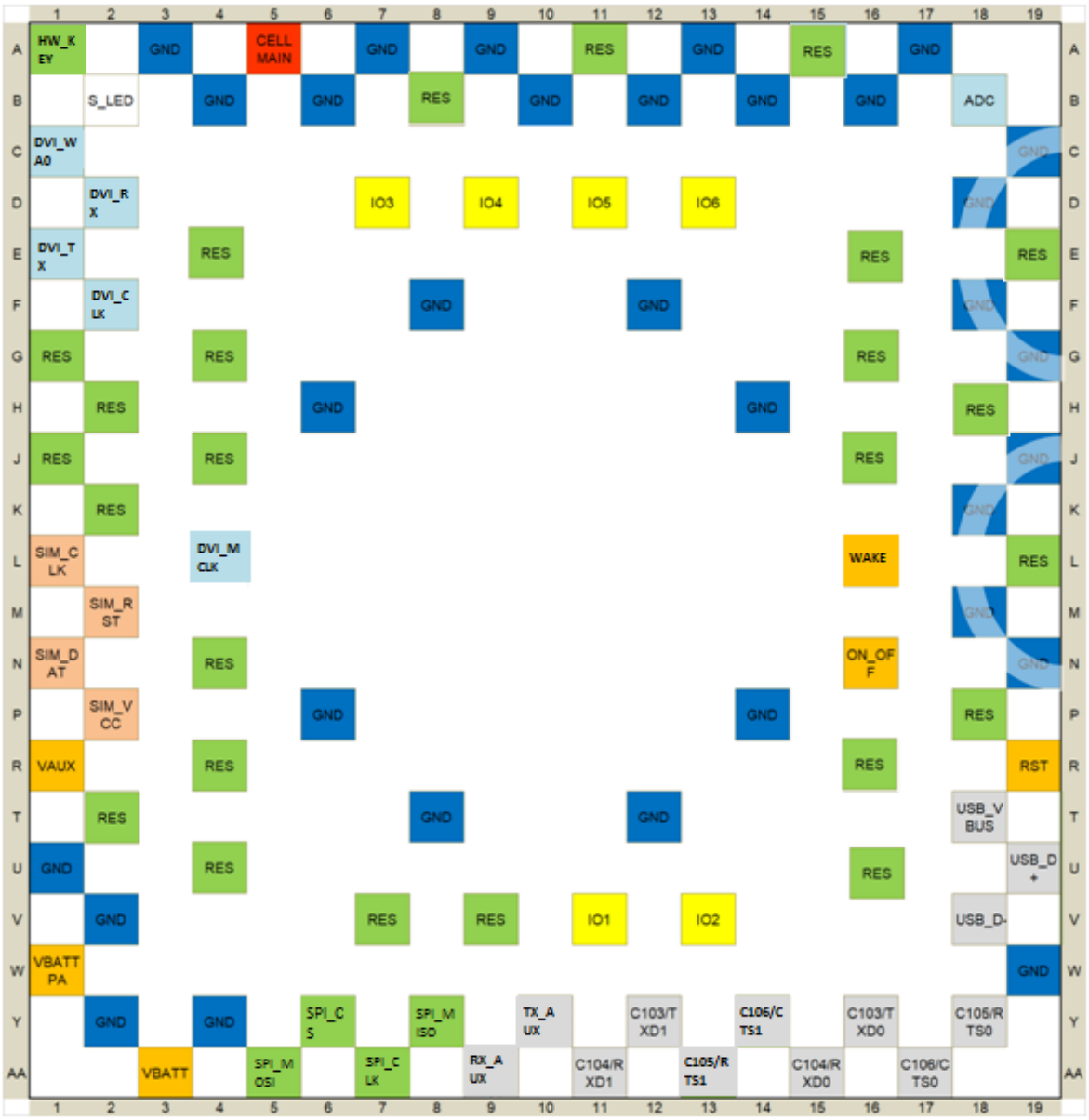
Pad	Signal	Note
W1	VBATT_PA	
AA3	VBATT	
A3, A7, A9, A13, A17, B4, B6, B10, B12, B14, B16, C19, D18, F8, F12, F18, G19, H6, H14, J19, K18, M18, N19, P6, P14, T8, T12, U1, V2, W19, Y2, Y4	GND	
A5	MAIN ANTENNA	
Y16	C103/TXD0	
AA15	C104/RXD0	
Y18	C105/RTS0	
AA17	C106/CTS0	
N16	ON_OFF*	
R19	RST*	
R1	VAUX	
L16	WAKE*	
L1	SIM_CLK	
M2	SIM_RST	
N1	SIM_DAT	
P2	SIM_VCC	
U19	USB_D+	On TP or a Connector

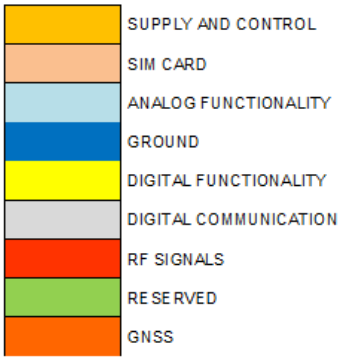
V18	USB_D-	On TP or a Connector
T18	USB_VBUS	On TP or a Connector

RTS pin should be connected to the GND (on the module side) if flow control is not used.
The above pins are also necessary to debug the application when the module is assembled on it so we recommend connecting them also to dedicated test point.

3.2. LGA Pads Layout

TOP VIEW





4. POWER SUPPLY

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

4.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfil the following requirements:

Power Supply	Value
Nominal Supply Voltage	3.3V
Operating Voltage Range	3.00 V÷ 3.60 V
Extended Voltage Range	2.10 V÷ 3.63 V
$VBAT_{min}$	2.10V

Battery powered application	Value
Operating Voltage Range (Li-MnO2)	2.10 V÷ 3.00 V
Operating Voltage Range (LiSoCl2)	2.80 V÷ 3.63 V

NOTE:
The Operating Voltage Range MUST never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop.
If the voltage drop is exceeding the limits it could cause a Power Off of the module. Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded.

4.2. Power Consumption

Mode	Average	Mode Description
Module OFF	3.2uA	Module switched OFF
PSM	4.2uA	T3412 Ext Unit=60s, T3412 Ext Value=2
AT+CFUN=1	520uA	Paging period=1.28s
Data Call Active B1 (Max Power)	126mA	Central channel, VBATT=3.3V
Data Call Active B1 (10dBm)	41mA	Central channel, VBATT=3.3V
Data Call Active B1 (0dBm)	28mA	Central channel, VBATT=3.3V
Data Call Active B2 (Max Power)	120mA	Central channel, VBATT=3.3V
Data Call Active B2 (10dBm)	40mA	Central channel, VBATT=3.3V
Data Call Active B2 (0dBm)	28mA	Central channel, VBATT=3.3V
Data Call Active B3 (Max Power)	111mA	Central channel, VBATT=3.3V
Data Call Active B3 (10dBm)	39mA	Central channel, VBATT=3.3V
Data Call Active B3 (0dBm)	27,6mA	Central channel, VBATT=3.3V
Data Call Active B4 (Max Power)	111mA	Central channel, VBATT=3.3V
Data Call Active B4 (10dBm)	39mA	Central channel, VBATT=3.3V
Data Call Active B4 (0dBm)	27,7mA	Central channel, VBATT=3.3V
Data Call Active B5 (Max Power)	108mA	Central channel, VBATT=3.3V
Data Call Active B5 (10dBm)	41mA	Central channel, VBATT=3.3V
Data Call Active B5 (0dBm)	29,5mA	Central channel, VBATT=3.3V
Data Call Active B8 (Max Power)	119mA	Central channel, VBATT=3.3V
Data Call Active B8 (10dBm)	42mA	Central channel, VBATT=3.3V
Data Call Active B8 (0dBm)	29,6mA	Central channel, VBATT=3.3V
Data Call Active B12 (Max Power)	122mA	Central channel, VBATT=3.3V
Data Call Active B12 (10dBm)	41mA	Central channel, VBATT=3.3V
Data Call Active B12 (0dBm)	29mA	Central channel, VBATT=3.3V
Data Call Active B13 (Max Power)	115mA	Central channel, VBATT=3.3V
Data Call Active B13 (10dBm)	41mA	Central channel, VBATT=3.3V
Data Call Active B13 (0dBm)	29mA	Central channel, VBATT=3.3V
Data Call Active B17 (Max Power)	118mA	Central channel, VBATT=3.3V
Data Call Active B17 (10dBm)	41mA	Central channel, VBATT=3.3V
Data Call Active B17 (0dBm)	29mA	Central channel, VBATT=3.3V
Data Call Active B18 (Max Power)	116mA	Central channel, VBATT=3.3V

Data Call Active B18 (10dBm)	42mA	Central channel, VBATT=3.3V
Data Call Active B18 (0dBm)	29,5mA	Central channel, VBATT=3.3V
Data Call Active B19 (Max Power)	117,5mA	Central channel, VBATT=3.3V
Data Call Active B19 (10dBm)	41mA	Central channel, VBATT=3.3V
Data Call Active B19 (0dBm)	29,5mA	Central channel, VBATT=3.3V
Data Call Active B20 (Max Power)	115mA	Central channel, VBATT=3.3V
Data Call Active B20 (10dBm)	42mA	Central channel, VBATT=3.3V
Data Call Active B20 (0dBm)	29,6mA	Central channel, VBATT=3.3V
Data Call Active B25 (Max Power)	120mA	Central channel, VBATT=3.3V
Data Call Active B25 (10dBm)	41mA	Central channel, VBATT=3.3V
Data Call Active B25 (0dBm)	28mA	Central channel, VBATT=3.3V
Data Call Active B26 (Max Power)	120mA	Central channel, VBATT=3.3V
Data Call Active B26 (10dBm)	41,4mA	Central channel, VBATT=3.3V
Data Call Active B26 (0dBm)	29,5mA	Central channel, VBATT=3.3V
Data Call Active B26 (Max Power)	125,6mA	Central channel, VBATT=3.3V
Data Call Active B26 (10dBm)	42mA	Central channel, VBATT=3.3V
Data Call Active B26 (0dBm)	29,3mA	Central channel, VBATT=3.3V
Data Call Active B28 (Max Power)	115,6mA	Central channel, VBATT=3.3V
Data Call Active B28 (10dBm)	41,8mA	Central channel, VBATT=3.3V
Data Call Active B28 (0dBm)	29,3mA	Central channel, VBATT=3.3V
Data Call Active B66 (Max Power)	109mA	Central channel, VBATT=3.3V
Data Call Active B66 (10dBm)	39mA	Central channel, VBATT=3.3V
Data Call Active B66 (0dBm)	28mA	Central channel, VBATT=3.3V
Data Call Active B71 (Max Power)	127mA	Central channel, VBATT=3.3V
Data Call Active B71 (10dBm)	42mA	Central channel, VBATT=3.3V
Data Call Active B71 (0dBm)	30mA	Central channel, VBATT=3.3V
Data Call Active B85 (Max Power)	121,6mA	Central channel, VBATT=3.3V
Data Call Active B85 (10dBm)	41,5mA	Central channel, VBATT=3.3V
Data Call Active B85 (0dBm)	29mA	Central channel, VBATT=3.3V

NOTE:

The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 200mA.

4.3. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout.

4.3.1. Electrical Design Guidelines

The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

4.3.1.1. +5V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.3V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the module, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the module from power polarity inversion.

4.3.2. +12V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.3V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.

- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.
- A protection diode should be inserted close to the power input, in order to save the module from power polarity inversion. This can be the same diode as for spike protection.

4.3.2.1. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.3V and the maximum voltage allowed is 3.65V.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the NE310H2 from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The suggested battery capacity is from 500mAh to 1000mAh.

WARNING:

The three cells Ni/Cd or Ni/MH 3,6 V Nom. Battery types or 4V PB types *MUST NOT BE USED DIRECTLY* since their maximum voltage can rise over the absolute maximum voltage for the NE310H2 and damage it.

NOTE:

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with NE310H2. Their use can lead to overvoltage on the NE310H2 and damage it. USE ONLY Li-MnO2 or LiSoCl2 batteries.

4.3.3. Thermal Design Guidelines

The thermal design for the power supply heat sink should be done considering the values described in the “Power Consumption” chapter.

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

For the heat generated by the module, you can consider it to be during transmission TBD W max during Data call.

This generated heat will be mostly conducted to the ground plane under the module; you must ensure that your application can dissipate it.

NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

4.3.4. Power Supply PCB layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performance.

- The Bypass low ESR capacitor must be placed close to the Telit NE310H2 power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the NE310H2 is wide enough to ensure a dropless connection even during the 2A current peaks.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces connecting the Switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually)
- The use of a good common ground plane is suggested.
- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.
- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines.
- A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

4.4. RTC Bypass out

The NE310H2 module is provided by an internal RTC section but its reference supply is VBATT. So, in order to maintain active the RTC programming, VBATT should not be removed

4.5. VAUX Power Output

A regulated power supply output is provided in order to supply small devices from the module. The signal is in common with the PWRMON (module powered ON indication) function. This output is always active when the module is powered ON. The operating range characteristics of the supply are:

Item	Min	Typical	Max
Output voltage	1.62V	1.80V	1.98V
Output current	-	-	10mA
Output bypass capacitor		0.1uF	

NOTE:
The Output Current MUST never be exceeded; care must be taken when designing the application section to avoid having an excessive current consumption.
If the Current is exceeding the limits it could cause a Power Off of the module.

NOTE:
VAUX max output current is shared with the other GPIOs for a maximum load of 10mA.

Warning:
The current consumption from VAUX_PWRMON increases the modem temperature.

5. DIGITAL SECTION

5.1. Logic Levels

ABSOLUTE MAXIMUM RATINGS:

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) with respect to ground	-0.3V	2.1V

OPERATING RANGE – INTERFACE LEVELS (1.8V CMOS):

Parameter	Min	Max
Input high level	1.35V	1.98V
Input low level	-0.3V	0.63V
Output high level	1.35 V	1.98V
Output low level	0	0.45

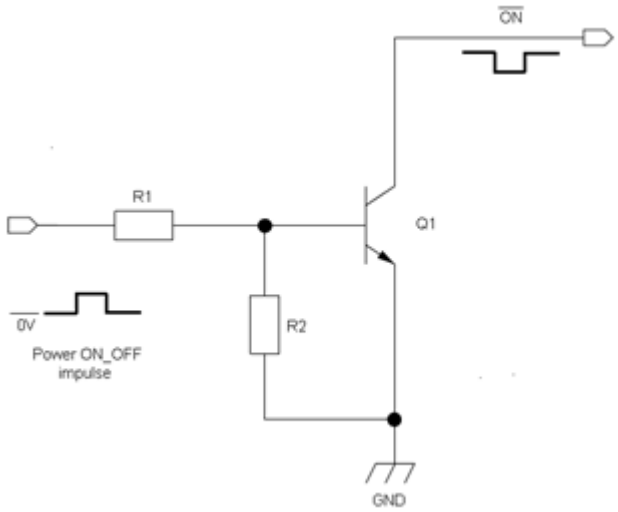
CURRENT CHARACTERISTICS:

Parameter	AVG	Max
Input Current	5 uA	80uA (if Pull Down is active)

5.2. Power On

To turn on the NE310H2 the pad ON_OFF* must be tied low for at least 200 millisecondsand then released.

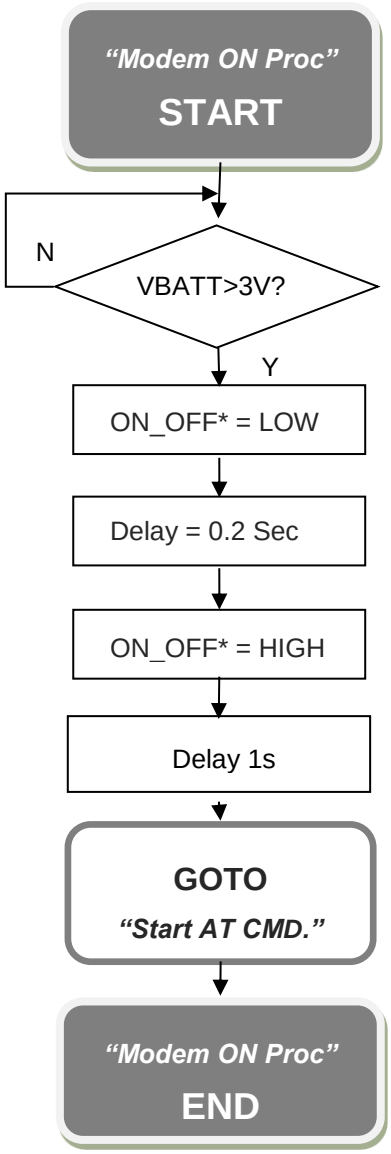
A simple circuit to do it is:



NOTE:

Don't use any pull up resistor on the ON_OFF* line, it is internally pulled up. Using pull up resistor may bring to latch up problems on the NE310H2 power regulator and improper power on/off of the module. The line ON_OFF* must be connected only in open collector or open drain configuration.

A flow chart showing the proper turn on procedure is displayed below:

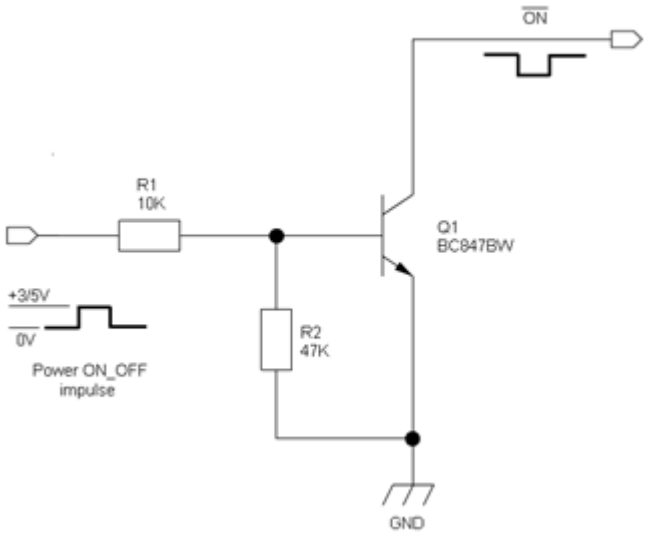


NOTE:

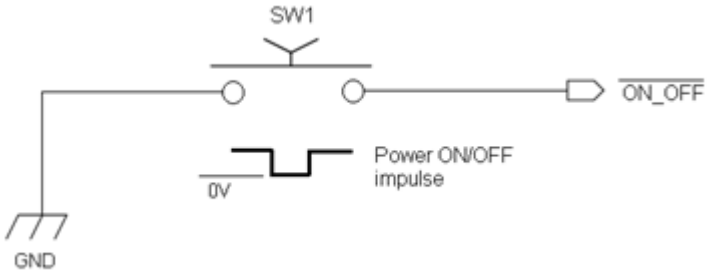
In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NE310H2 when the module is powered off or during an ON/OFF transition

For example:

1- Let's assume you need to drive the ON_OFF* pad with a totem pole output of a +3/5 V microcontroller (uP_OUT1):



2- Let's assume you need to drive the ON_OFF* pad directly with an ON/OFF button:



5.3. Power Off

The device could be turned off using the ON_OFF* pin

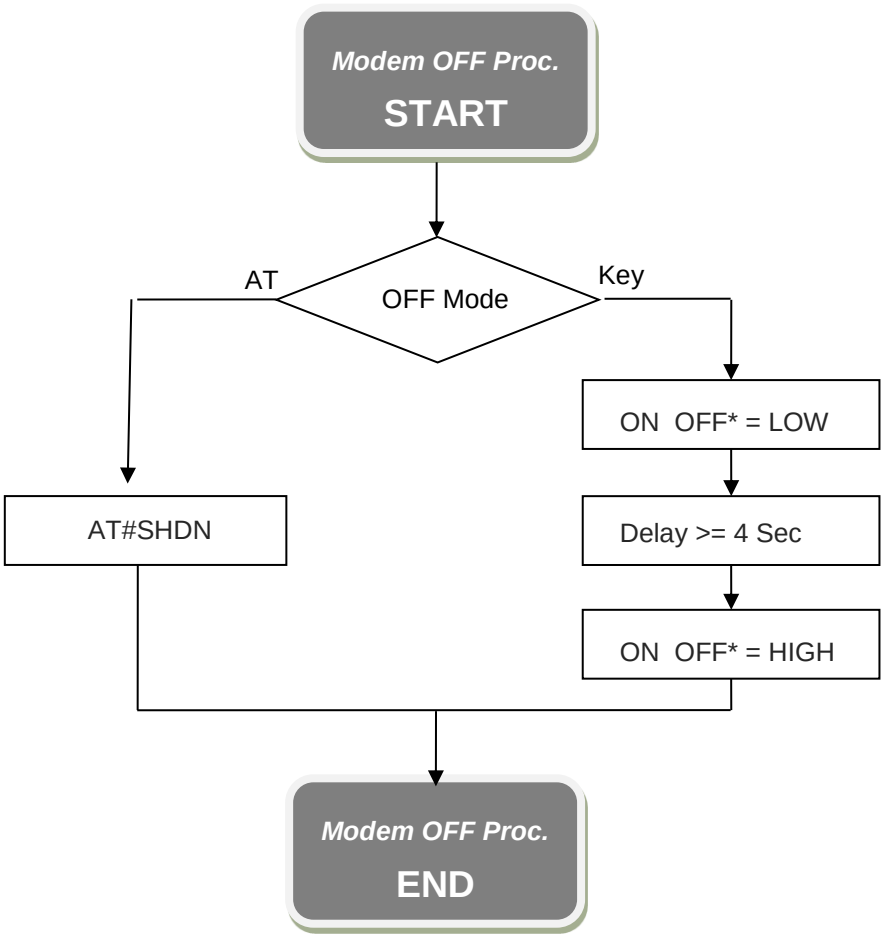
When the procedure is activated, the device issues a detach request to network informing that the device will not be reachable any more.

To turn OFF the NE310H2 the pad ON_OFF* must be tied low for at least 4 seconds and then released.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NE310H2 when the module is powered off or during an ON/OFF transition.

The following flow chart shows the proper turn off procedure:



5.4. Unconditional Restart

To unconditionally restart the NE310H2, the pad RST* must be tied low for at least 400 milliseconds and and then released.
The hardware unconditional Restart must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure to be done in the rare case that the device gets stuck waiting for some network or SIM responses.

Do not use any pull up resistor on the RST line nor any totem pole digital output. Using pull up resistor may bring to latch up problems on the NE310H2 power regulator and improper functioning of the module.
The line RST must be connected only in open collector configuration; the transistor must be connected as close as possible to the RST pin.

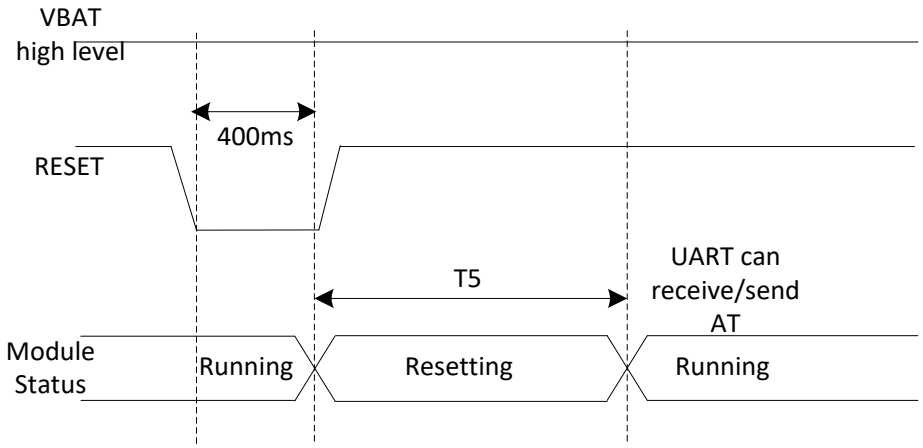
The unconditional hardware restart must always be implemented on the boards and the software must use it as an emergency exit procedure.

5.4.1. PIN DESCRIPTION

Signal	Function	I/O	Pad
RST*	Unconditional Reset of the Module	I	R19

There are two way to reset the module you can choose:
1：Through AT command
2：Reset the module through RESET pin
When the software stops response, you can pulled down RESET for 400ms to reset the module's system.

The RESET timing are shown in the following figure below:



T5：the RESET process until the AT port can communicate spend time

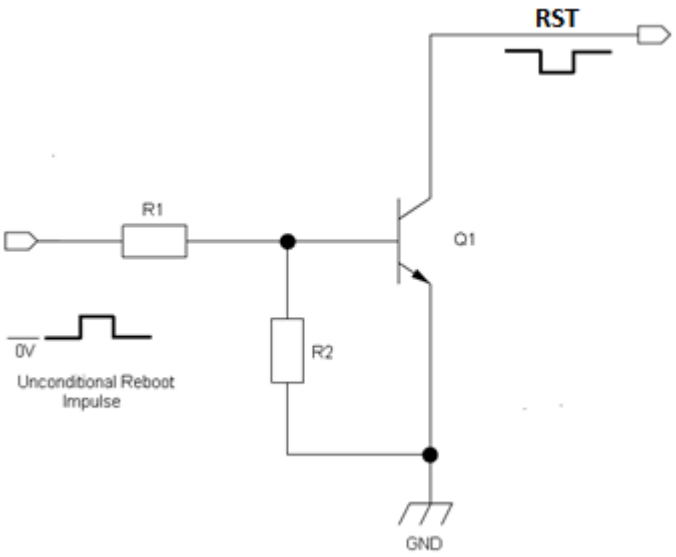
5.4.2. Operating levels

The RST* line is connected to VBATT with a Pull Up so the electrical levels on this pin are aligned to the main supply level.

WARNING:

The hardware unconditional Reset must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure.

A typical circuit is the following:



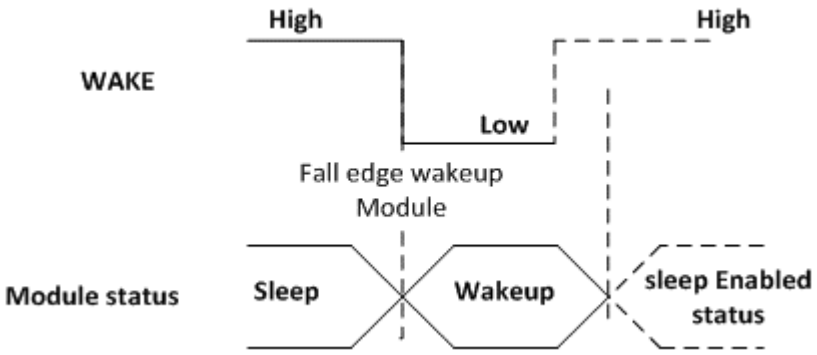
NOTE:
In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NE310H2 when the module is powered off or during a reboot transition.

NOTE:
Do not use any pull up resistor on the RST line nor any totem pole digital output. Using pull up resistor may bring to latch up problems on the NE310H2 power regulator and improper functioning of the module.
To proper power on again the module please refer to the related paragraph (“Power ON”)
The unconditional hardware reboot must always be implemented on the boards and should be used only as an emergency exit procedure.

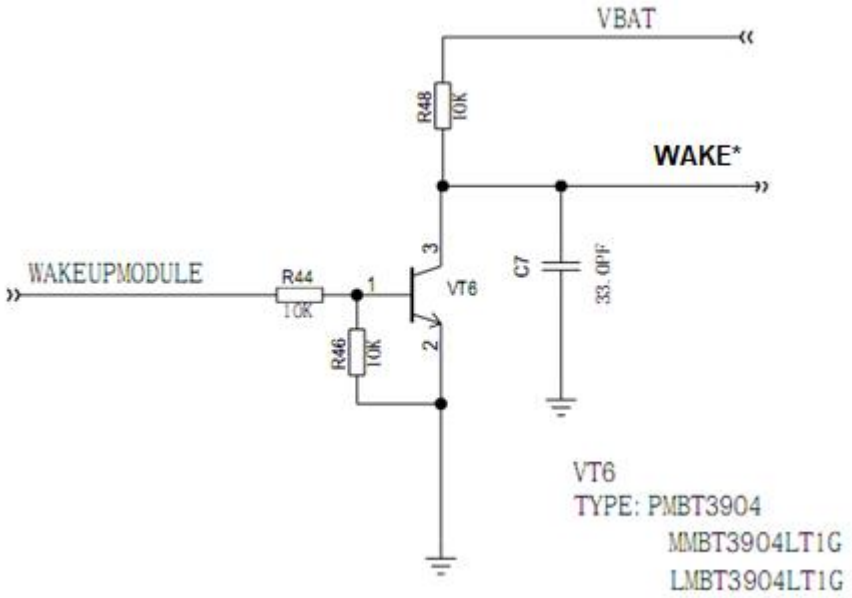
5.1. WAKEUP from PSM

5.1.1. Pin Description

The module is provided by an input line named WAKE* used to wakeup the module from the deep power saving state (PSM). The signal is active LOW.
The following figure is the signal waveform:



5.1.2. Application Example



The resistors R44, R46 and R48 in Figure are only the recommended value and they need to be tuned according to the specific customer's application.

5.2. SPI

The module is supporting one SPI port (Master Only).

The signals are available on the following pads:

Pad	Name	I/O	Descriprtion	Type	Notes
Y6	SPI_CS	O/I	SPI - Circuit Select	CMOS 1.8V	
AA7	SPI_CLK	O/I	SPI - Clock	CMOS 1.8V	
AA5	SPI_MOSI	O/I	SPI - MOSI	CMOS 1.8V	
Y8	DVI_MCLK	I/O	SPI - MISO	CMOS 1.8V	

5.3. Communication ports

5.3.1. Serial Ports

The NE310H2 module is provided with by 2 Asynchronous serial ports:

- MODEM SERIAL PORT 0 (Main)
- MODEM SERIAL PORT 1

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 2.8V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 5V or other voltages different from 2.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work.

On the NE310H2 the ports are CMOS 1.8.

5.3.1.1. MODEM SERIAL PORT 0 (USIF0)

The main serial port on the NE310H2 is a +2.8V UART with two flow control signals (CTS, RTS).

It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

The following table is listing the available signals:

RS232 pin	Signal	PAD	Name	Usage
2	C104/RXD0	AA15	Transmit line *see Note	Output transmit line of NE310H2 UART
3	C103/TXD0	Y16	Receive line *see Note	Input receive of the NE310H2 UART
5	GND	A3, A7, A9, A13, A17, B4, B6, B10, B12, B14, B16, C19, D18, F8, F12, F18, G19, H6, H14, J19, K18, M18, N19, P6, P14, T8, T12, U1, V2, W19, Y2, Y4	Ground	Ground
7	C106/CTS0	AA17	Clear to Send	Output from the NE310H2 that controls the Hardware flow control
8	C105/RTS0	Y18	Request to Send	Input to the NE310H2 that controls the Hardware flow control

NOTE:
According to V.24, some signal names are referred to the application side, therefore on the NE310H2 side these signal are on the opposite direction:
TXD on the application side will be connected to the receive line (here named C103/TXD0)
RXD on the application side will be connected to the transmit line (here named C104/RXD0)

For a minimum implementation, only the TXD, RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NE310H2 when the module is powered off or during a reboot transition.

5.3.1.2. MODEM SERIAL PORT 1 (USIF1)

The secondary serial port on the NE310H2 is a +1.8V UART

It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

The following table is listing the available signals:

RS232 pin	Signal	PAD	Name	Usage
2	RXD1	AA11	Transmit line *see Note	Output transmit line of NE310H2 UART
3	TXD1	Y12	Receive line *see Note	Input receive of the NE310H2 UART
5	GND	A3, A7, A9, A13, A17, B4, B6, B10, B12, B14, B16, C19, D18, F8, F12, F18, G19, H6, H14, J19, K18, M18, N19, P6, P14, T8, T12, U1, V2, W19, Y2, Y4	Ground	Ground
7	C106/CTS1	Y14	Clear to Send	Output from the NE310H2 that controls the Hardware flow control
8	C105/RTS1	AA13	Request to Send	Input to the NE310H2 that controls the Hardware flow control

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NE310H2 when the module is not supplied or during a reboot transition.

NOTE:
According to V.24, some signal names are referred to the application side, therefore on the NE310H2 side these signal are on the opposite direction:
TXD on the application side will be connected to the receive line (here named C103/TXD1)
RXD on the application side will be connected to the transmit line (here named C104/RXD1)
In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NE310H2 when the module is powered off or during a reboot transition.

5.3.1.3. MODEM SERIAL PORT 3 (Auxiliary)

The third serial port on the NE310H2 is a +1.8V UART
The following table is listing the available signals:

Signal	PAD	Name	Usage
TX_AUX	Y10	Transmit line	Output transmit line of NE310H2 UART
RX_AUX	AA9	Receive line	Input receive of the NE310H2 UART

5.3.1.4. RS232 LEVEL TRANSLATION

In order to interface the module with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must:

- invert the electrical signal in both directions;
- change the level from 0/1.8V to +15/-15V .

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.
The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).
By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.

In order to translate the whole set of control lines of the UART you will need:

- 2 drivers
- 2 receivers

NOTE:
The digital input lines working at 1.8V CMOS have an absolute maximum input voltage of 3.0V; therefore the level translator IC shall not be powered by the +3.8V supply of the module. Instead, it must be powered from a +2.7V / +2.9V (dedicated) power supply.
This is because in this way the level translator IC outputs on the module side (i.e. module's inputs) will work at +3.8V interface levels, damaging the module inputs

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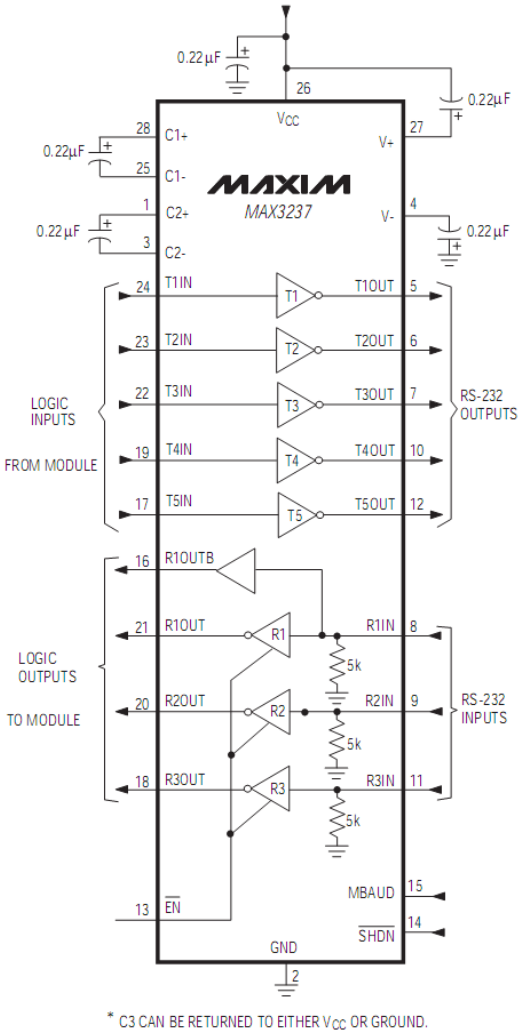
An example of level translation circuitry of this kind is:

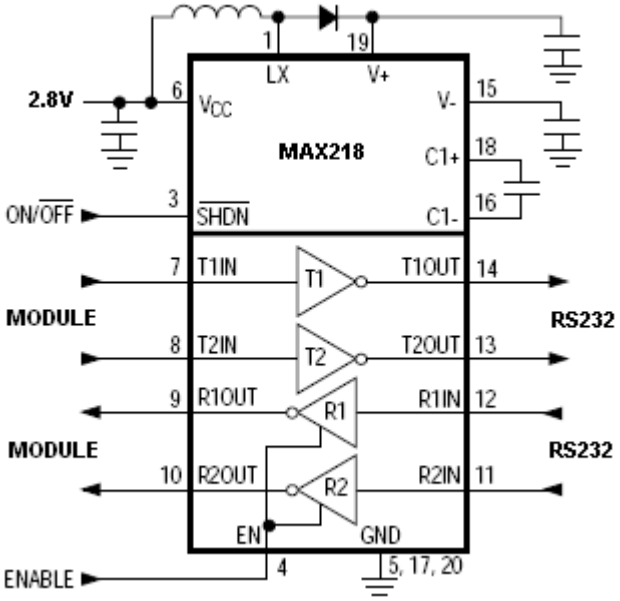


The example is done with a MAXIM MAX3237 Transceiver that could accept supply voltages of 3V DC. Not exceeded with supply voltage higher then 3.1VDC because this is the higher voltage limit of module's inputs.

NOTE:

In this case Vin has to be set with a value compatible with the logic levels of the module. (Max 3.1V DC)

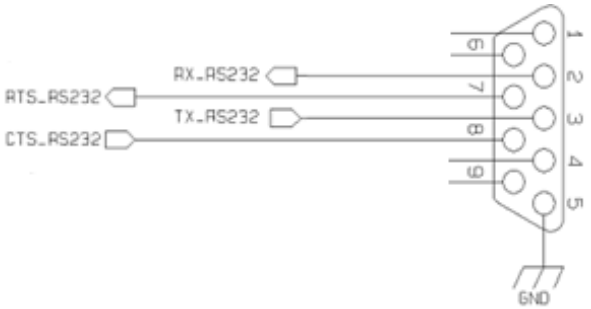
Second solution could be done using a MAXIM transceiver (MAX218) In this case the compliance with RS232 (+-5V) is possible.



Another level adapting method could be done using a standard RS232 Transceiver (MAX3237EAI) adding some resistors to adapt the levels on the module's Input lines.

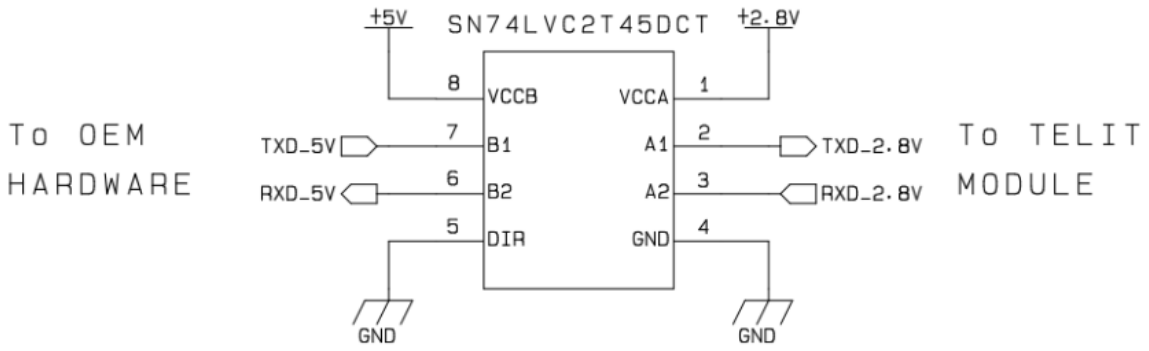
NOTE:
In this case has to be taken in account the length of the lines on the application to avoid problems in case of High-speed rates on RS232.

The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



5.3.1.5. 5V UART level translation

If the OEM application uses a microcontroller with a serial port (UART) that works at a voltage different from 2.8 - 3V, then a circuitry has to be provided to adapt the different levels of the two set of signals. As for the RS232 translation there are a multitude of single chip translators. For example a possible translator circuit for a 5V TRANSMITTER / RECEIVER can be:



NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the module when the module is powered OFF or during an ON/OFF transition.

5.4. General purpose I/O

The NE310H2 module is provided by a set of Configurable Digital Input / Output pins (CMOS 1.8)

Input pads can only be read; they report the digital value (high or low) present on the pad at the read time. Output pads can only be written or queried and set the value of the pad output. An alternate function pad is internally controlled by the NE310H2 firmware and acts depending on the function implemented.

The following table shows the available GPIO on the NE310H2:

PAD	Signal	I/O	Default State	Note
V11	GPIO_01	I/O	INPUT	
V13	GPIO_02	I/O	INPUT	
D7	GPIO_03	I/O	INPUT	
D9	GPIO_04	I/O	INPUT	
D11	GPIO_05	I/O	INPUT	
D13	GPIO_06	I/O	INPUT	

NOTE:
The internal GPIO's pull up/pull down could be set to the preferred status for the application using the specific AT command.
Please refer for the AT Commands User Guide for the detailed command Syntax.

WARNING:
During power up the GPIOs may be subject to transient glitches.

5.4.1. Using a GPIO as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO. If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 1.8V CMOS, then it can be buffered with an open collector transistor with a 47K pull up to VAUX.

NOTE:
In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NE310H2 when the module is powered off or during a reboot transition.
The VAUX pin can be used for input pull up reference or/and for ON monitoring.

5.4.2. Using a GPIO as OUTPUT

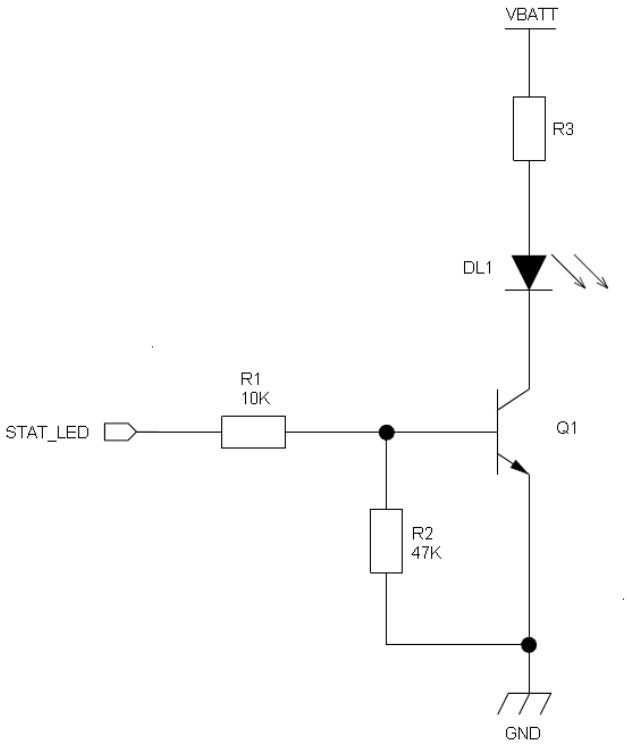
The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

5.4.3. Indication of network service availability

The SLED pin status shows information on the network service availability and Call status. In the NE310H2 modules, the SLED needs an external transistor to drive an external LED. Therefore, the status indicated in the following table is reversed with respect to the pin status.

Device Status	Led Status
Device off	Permanently off
Offline	Frequency 1Hz, Duty cycle 50%
Online	Frequency 0.3Hz, Duty cycle 10%
Data Sending	Frequency 10Hz, Duty cycle50%

A schematic example could be:



5.5. External SIM Holder

Please refer to the related User Guide (SIM Holder Design Guides, 80000NT10001a).

5.1. ADC

The module provides one ADC to digitize the analog signal to 10-bit digital data such as battery voltage,temperature and so on.

Using a specific AT command (ref. to AT user guide) can read the voltage value on ADC pin. The read value is expressed in mV.

In order to improve the accuracy of ADC, the related PCB line should be surrounded by ground.

6. RF SECTION

6.1. Antenna requirements

6.1.1. Main Antenna

The antenna connection and board layout design are the most important aspect in the full product design as they strongly affect the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.

The antenna and antenna transmission line on PCB for a Telit NE310H2 device shall fulfil the following requirements:

Item	Value
Frequency range	617-2200MHZ
Gain	TBD
Impedance	50 Ohm
Input power	23dBm
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfil all regulatory requirements)

6.1.2. PCB Design guidelines

When using the NE310H2, since there's no antenna connector on the module, the antenna must be connected to the NE310H2 antenna pad by means of a transmission line implemented on the PCB.

In the case the antenna is not directly connected at the antenna pad of the NE310H2, then a PCB line is needed in order to connect with it or with its connector.

This transmission line shall fulfil the following requirements:

Item	Value
Characteristic Impedance	50 ohm
Max Attenuation	0,3 dB
Coupling	Coupling with other signals shall be avoided
Ground Plane	Cold End (Ground Plane) of antenna shall be equipotential to the NE310H2 ground pins

The transmission line should be designed according to the following guidelines:

- Ensure that the antenna line impedance is 50 ohm;
- Keep the antenna line on the PCB as short as possible, since the antenna line loss shall be less than 0,3 dB;
- Antenna line must have uniform characteristics, constant cross section; avoid meanders and abrupt curves;
- Keep, if possible, one layer of the PCB used only for the Ground plane;
- Surround (on the sides, over and under) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line track;
- The ground around the antenna line on PCB has to be strictly connected to the Ground Plane by placing vias every 2mm at least;
- Place EM noisy devices as far as possible from NE310H2 antenna line;
- Keep the antenna line far away from the NE310H2 power supply lines;
- If you have EM noisy devices around the PCB hosting the NE310H2, such as fast switching Ics, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.

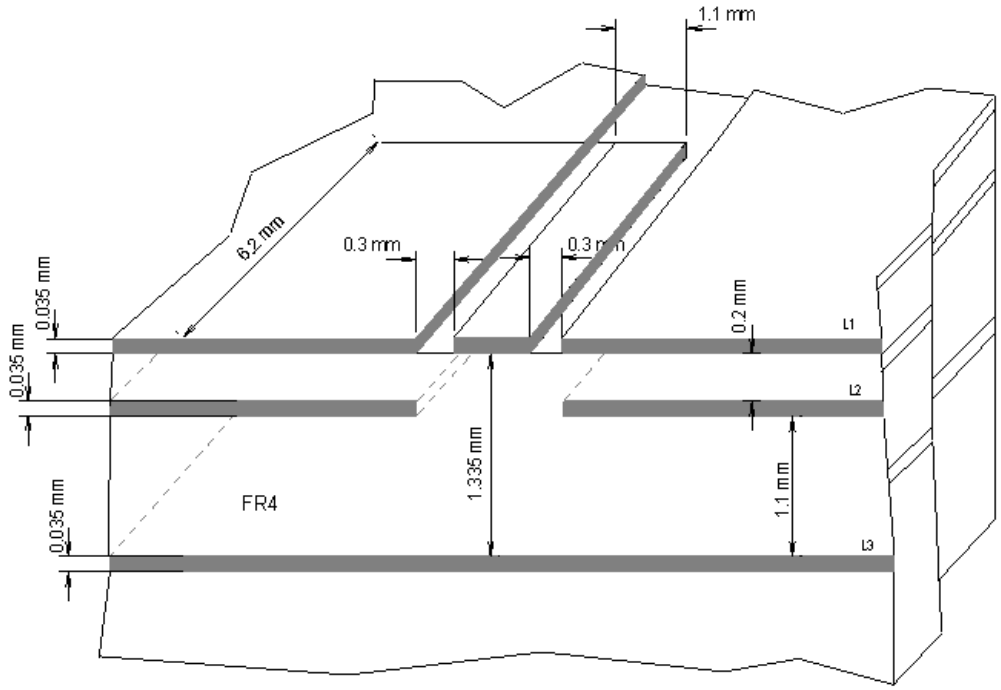
- If you don’t have EM noisy devices around the PCB of NE310H2, by using a micro strip on the superficial copper layer for the antenna line, the line attenuation will be lower than a buried one;

6.1.2.1. Transmission line design

During the design of the NE310H2 interface board, the placement of components has been chosen properly, in order to keep the line length as short as possible, thus leading to lowest power losses possible. A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.

The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity ε_r = 4.6 ± 0.4 @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.

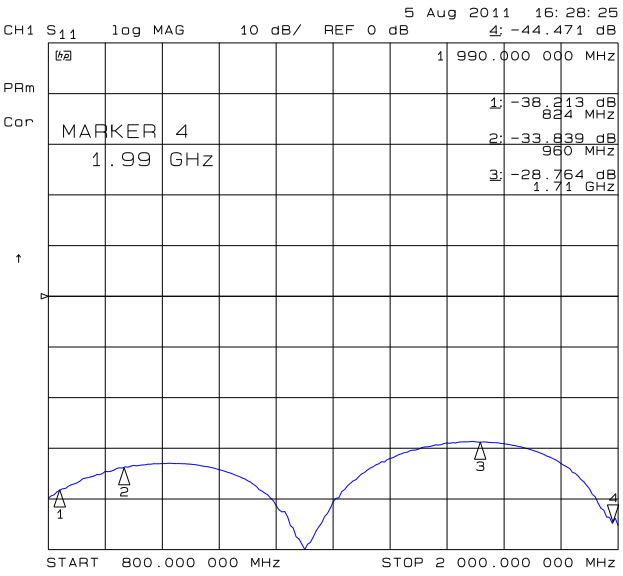
A characteristic impedance of nearly 50 Ω is achieved using trace width = 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of trace above ground plane is 1.335 mm. Calculated characteristic impedance is 51.6 Ω, estimated line loss is less than 0.1 dB. The line geometry is shown below:



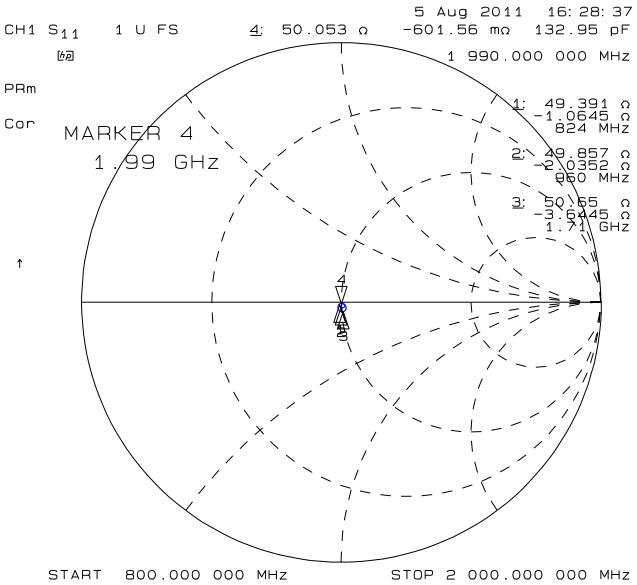
6.1.2.2. Transmission Line Measurements

An HP8753E VNA (Full-2-port calibration) has been used in this measurement session. A calibrated coaxial cable has been soldered at the pad corresponding to RF output; a SMA connector has been soldered to the board in order to characterize the losses of the transmission line including the connector itself. During Return Loss / impedance measurements, the transmission line has been terminated to 50 Ω load.

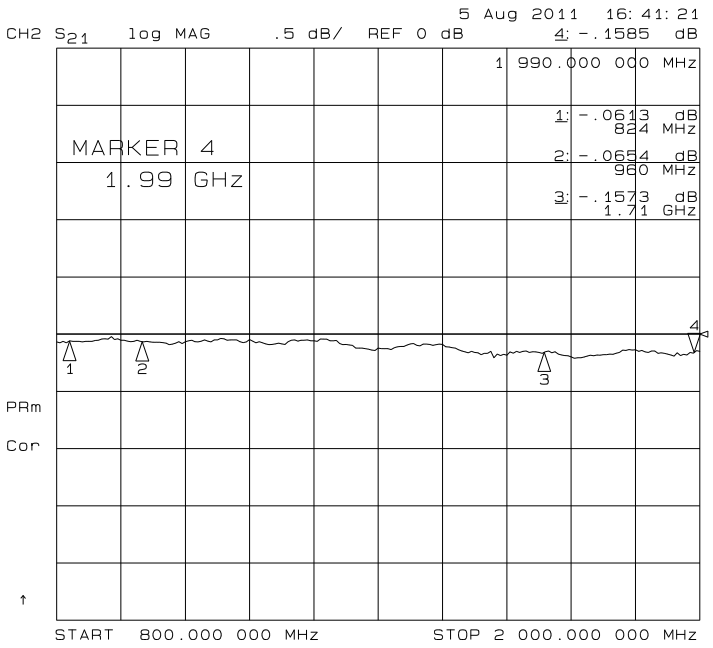
Return Loss plot of line under test is shown below:



Line input impedance (in Smith Chart format, once the line has been terminated to 50 Ω load) is shown in the following figure:



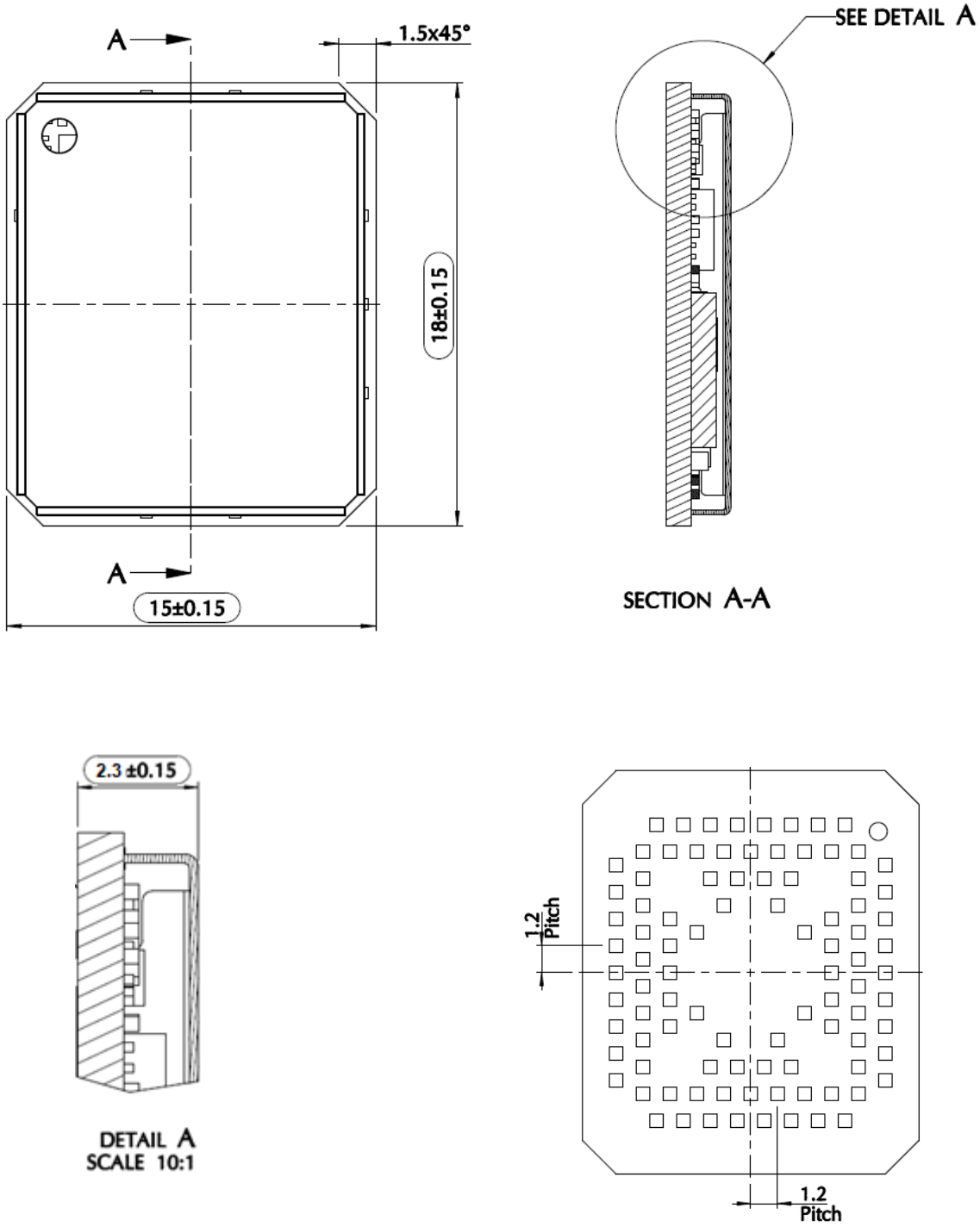
Insertion Loss of G-CPW line plus SMA connector is shown below:



6.1.2.3. Antenna Installation Guidelines

- Install the antenna in a place covered by the LTE signal.
- The Antenna must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter;
- Antenna shall not be installed inside metal cases
- Antenna shall be installed also according Antenna manufacturer instructions.

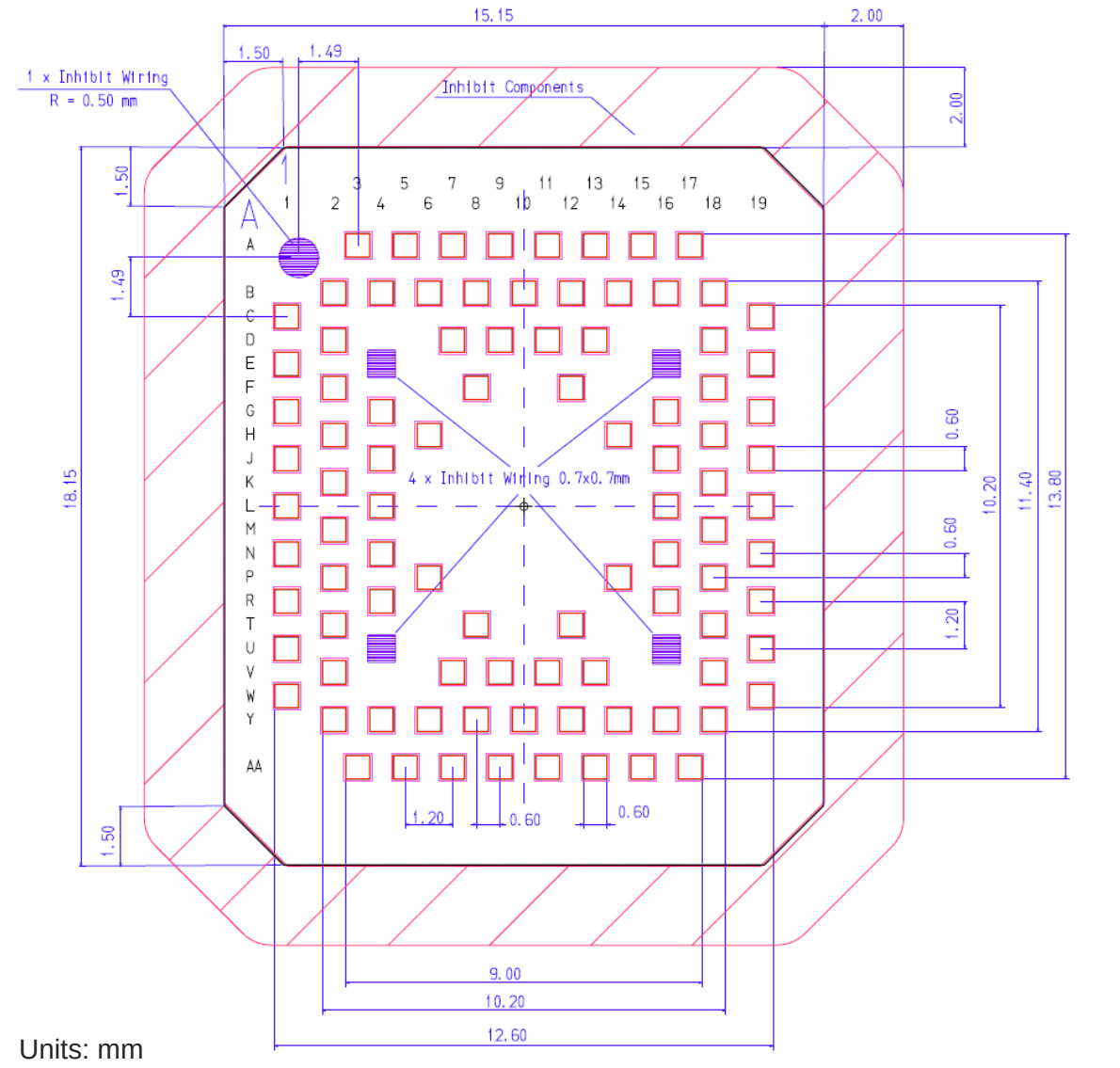
7. MECHANICAL DESIGN



NOTE: The dimensions are in mm

8. APPLICATION PCB DESIGN

The NE310H2 modules have been designed in order to be compliant with a standard lead-free SMT process.



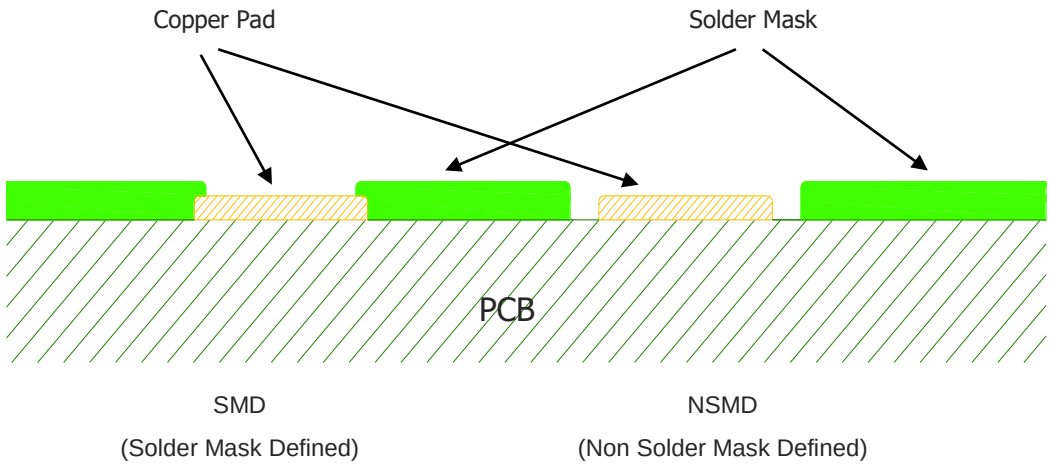
Units: mm

In order to easily rework the NE310H2 is suggested to consider on the application a 1.5 mm placement inhibit area around the module. It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

NOTE:
In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

8.1. PCB pad design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



8.2. PCB pads

It is not recommended to place via or micro-via not covered by solder resist in an area of 0,3 mm around the pads unless it carries the same signal of the pad itself.
Holes in pad are allowed only for blind holes and not for through holes.
Recommendations for PCB pad surfaces:

Finish	Layer Thickness (um)	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.05 – 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.
It is not necessary to panel the application's PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

8.3. Stencil

Stencil's apertures layout can be the same of the footprint (1:1), we suggest a thickness of stencil foil ≥ 120 µm.

8.4. Solder paste

Item	Lead Free
Solder Paste	Sn/Ag/Cu

We recommend using only "no clean" solder paste in order to avoid the cleaning of the modules after assembly.

8.5. Solder Reflow

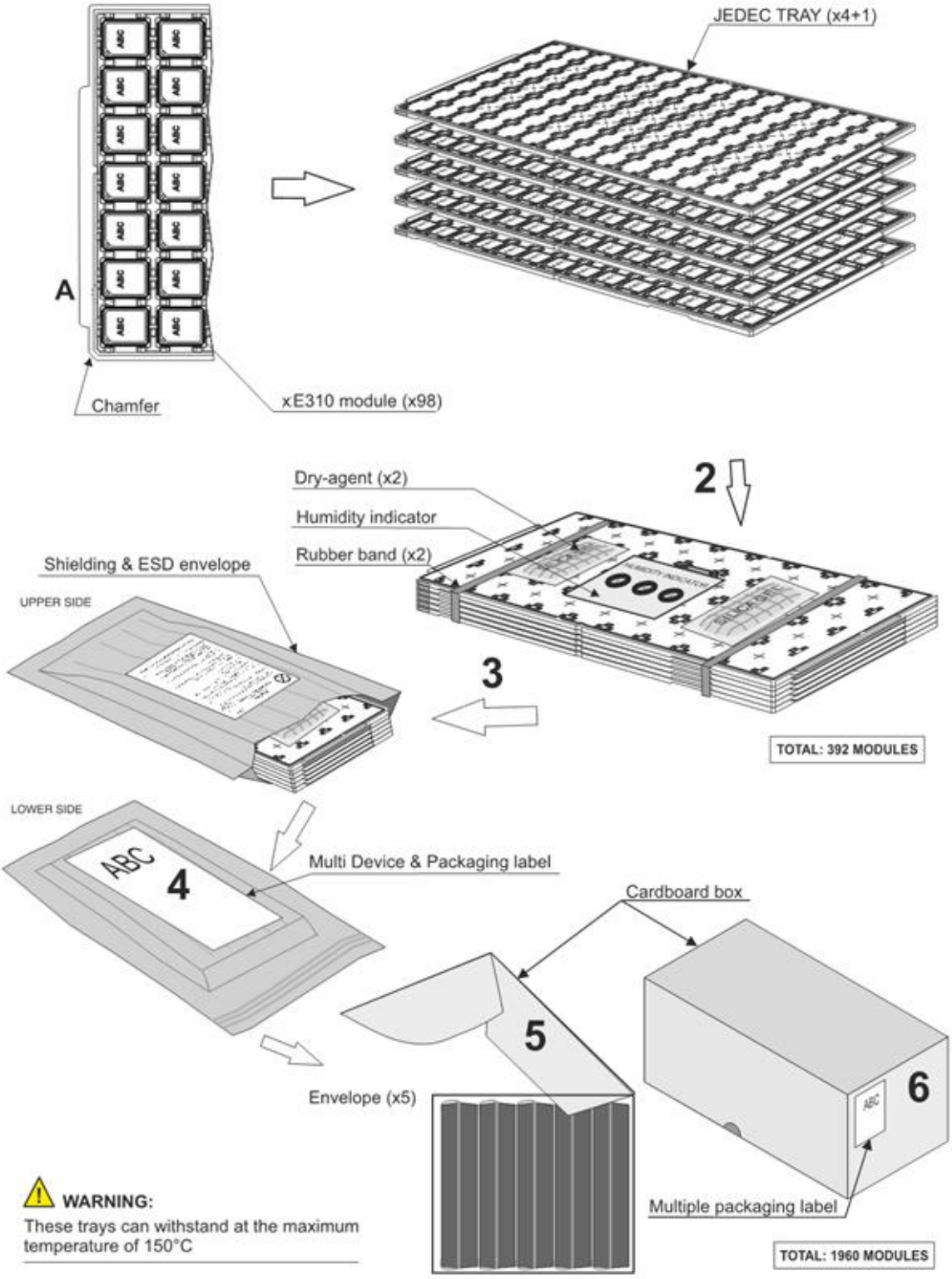
WARNING:
THE NE310H2 MODULE WITHSTANDS ONE REFLOW PROCESS ONLY.

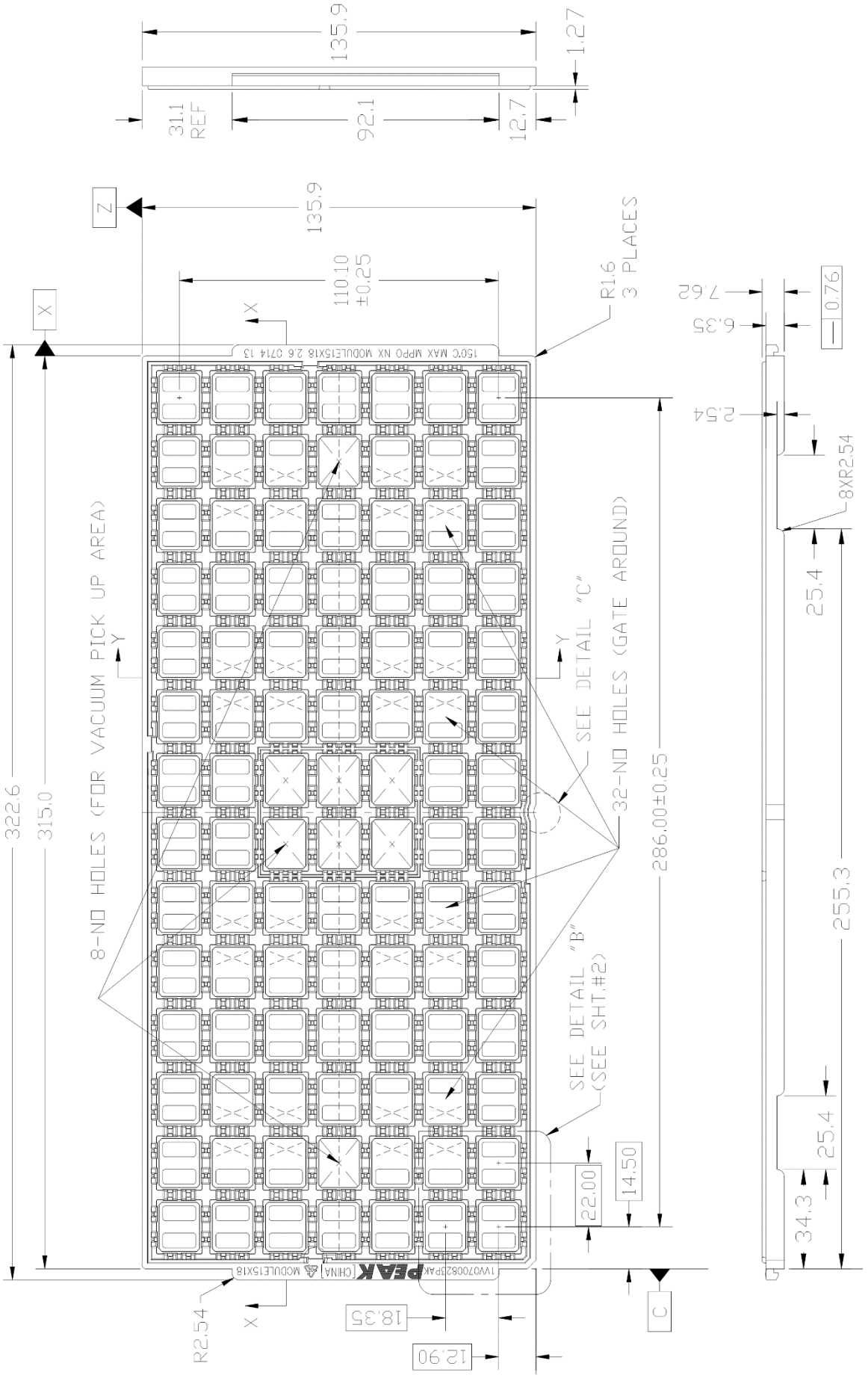
9. PACKAGING

9.1. Tray

The NE310H2 modules are packaged on trays.

These trays can be used in SMT processes for pick & place handling.




135.9
1.27
31.1
REF
92.1
12.7
Z
135.9
110.10
±0.25
X
R1.6
3 PLACES
150C MAX MPPO NX MODULE15X18 2.6 0714 13
7.62
6.35
0.76
2.54
8XR2.54
25.4
322.6
315.0
8-NO HOLES (FOR VACUUM PICK UP AREA)
Y
SEE DETAIL "C"
32-NO HOLES (GATE AROUND)
286.00±0.25
255.3
SEE DETAIL "B"
(SEE SHT #2)
22.00
14.50
25.4
34.3
PEAK
CHINA
MODULE15X18
R2.54
18.35
12.90
C

9.2. Moisture sensitivity

The NE310H2 is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5.

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

10. CONFORMITY ASSESSMENT ISSUES

10.1. Approvals

- GCF
- RED
- RoHS and REACH

10.2. Declaration of Conformity

The DoC will be available here: https://www.telit.com/RED/

11. SAFETY RECOMMENDATIONS

11.1. READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as any project or installation issue, because the risk of disturbing the LTE network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

http://ec.europa.eu/enterprise/sectors/rtte/documents/

The text of the Directive 99/05 regarding telecommunication equipment is available,

while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/

12. REFERENCE TABLE OF RF BANDS CHARACTERISTICS

Band	Freq. Tx (MHz)	Freq. Rx (MHz)
B1	1920 MHz – 1980 MHz	2110 MHz – 2170 MHz
B2	1850 MHz – 1910 MHz	1930 MHz – 1990 MHz
B3	1710 MHz – 1785 MHz	1805 MHz – 1880 MHz
B4	1710 MHz – 1755 MHz	2110 MHz – 2155 MHz
B5	824 MHz – 849 MHz	869 MHz – 894 MHz
B8	880 MHz – 915 MHz	925 MHz – 960 MHz
B12	699 MHz – 716 MHz	729 MHz – 746 MHz
B13	777 MHz – 787 MHz	746 MHz – 756 MHz
B17	704 MHz – 716 MHz	734 MHz – 746 MHz
B18	815 MHz – 830 MHz	860 MHz -875 MHz
B19	830 MHz – 845 MHz	875 MHz – 890 MHz
B20	832 MHz – 862 MHz	791 MHz -821 MHz
B25	1850 MHz – 1915 MHz	1930 MHz -1995 MHz
B26	814 MHz – 849 MHz	859 MHz – 894 MHz
B28	703 MHz – 748 MHz	758 MHz – 803 MHz
B66	1710 MHz – 1780 MHz	2110 MHz – 2200 MHz
B71	663 MHz – 698 MHz	617 MHz – 783 MHz
B85	698 MHz – 716 MHz	728 MHz – 746 MHz

13. ACRONYMS

TTSC	Telit Technical Support Centre
USB	Universal Serial Bus
HS	High Speed
DTE	Data Terminal Equipment
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multiple Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
UART	Universal Asynchronous Receiver Transmitter
HSIC	High Speed Inter Chip
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
I/O	Input Output
GPIO	General Purpose Input Output
CMOS	Complementary Metal – Oxide Semiconductor
MOSI	Master Output – Slave Input

MISO	Master Input – Slave Output
CLK	Clock
MRDY	Master Ready
SRDY	Slave Ready
CS	Chip Select
RTC	Real Time Clock
PCB	Printed Circuit Board
ESR	Equivalent Series Resistance
VSWR	Voltage Standing Wave Radio
VNA	Vector Network Analyzer
TTFF	Time to First Fix

14. DOCUMENT HISTORY

Revision	Date	Changes
0	2019-06-26	First emission – Preliminary
1	2019-08-14	Updated overall document
2	2019-08-20	Updated 5.3, 5.3.1.3 chapters
3	2019-08-30	Updated chapters 2.1, 2.3, 2.4, 9, 10.2 Updated mechanical dimensions Added Temperature range
4	2019-09-30	Updated Chapter 3.1, 4.1, 4.2, 5.1, 6.1.1

SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

www.telit.com

Telit Communications S.p.A.
Via Stazione di Prosecco, 5/B
I-34010 Sgonico (Trieste), Italy

Telit IoT Platforms LLC
5300 Broken Sound Blvd, Suite 150
Boca Raton, FL 33487, USA

Telit Wireless Solutions Inc.
3131 RDU Center Drive, Suite 135
Morrisville, NC 27560, USA

Telit Wireless Solutions Co., Ltd.
8th Fl., Shinyoung Securities Bld.
6, Gukjegeumyung-ro8-gil, Yeongdeungpo-gu
Seoul, 150-884, Korea

Telit Wireless Solutions Ltd.
10 Habarzel St.
Tel Aviv 69710, Israel

Telit Wireless Solutions
Technologia e Servicos Ltda
Avenida Paulista, 1776, Room 10.C
01310-921 São Paulo, Brazil

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