library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity full\_adder is

Port ( A, B, C\_in : in STD\_LOGIC;

S, C\_out : out STD\_LOGIC);

end full\_adder;

architecture Behavioral of full\_adder is

component half\_adder is

Port ( A, B : in STD\_LOGIC;

Sum , Carry : out STD\_LOGIC);

end component half\_adder;

SIGNAL S1, C1, C2 : STD\_LOGIC;

begin --Behavioral

HA1: half\_adder port map (A => A, B => B, Sum => S1, Carry => C1);

HA2: half\_adder port map (A => S1, B => C\_in , Sum => S, Carry => C2);

C\_out <= C1 or C2;

end Behavioral;