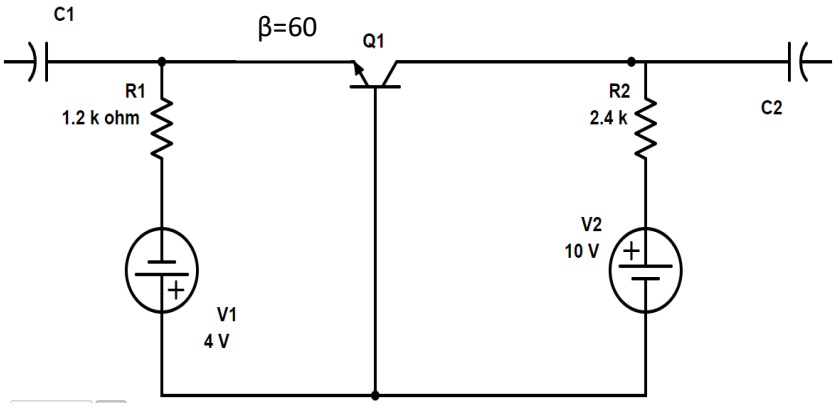
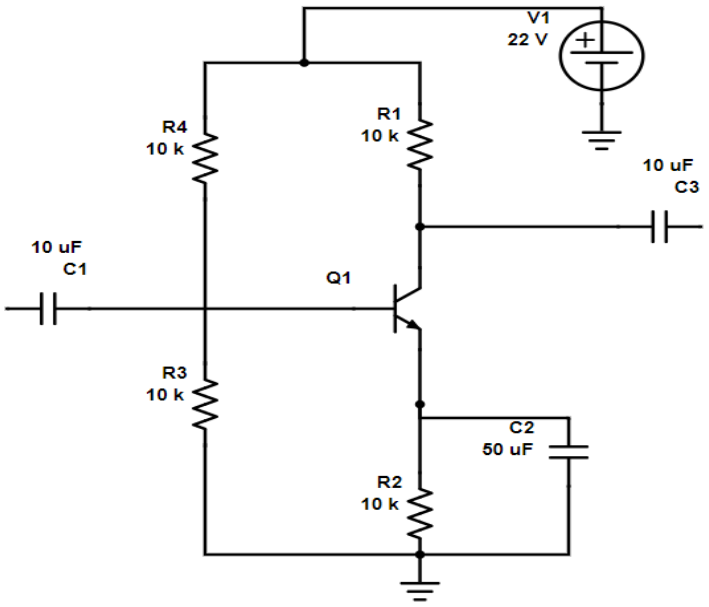
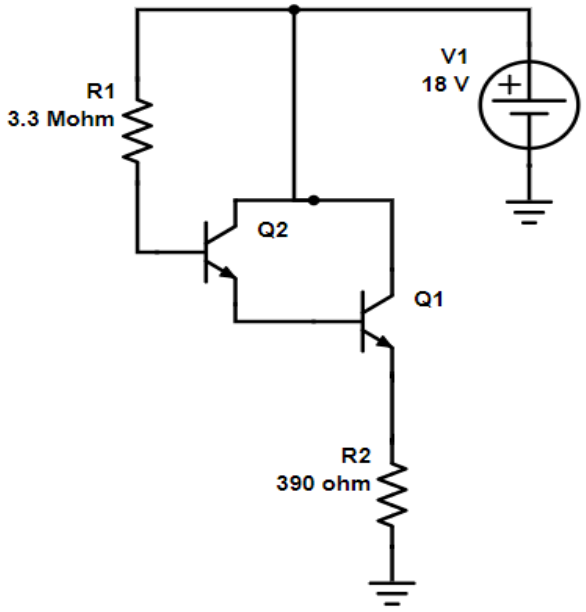
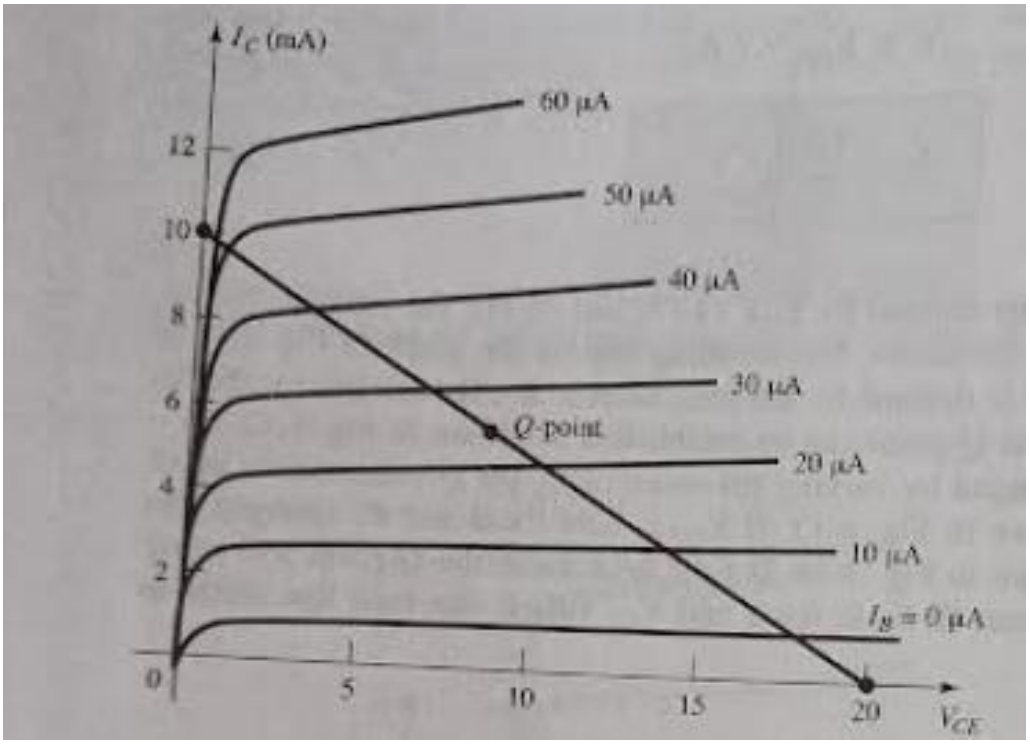
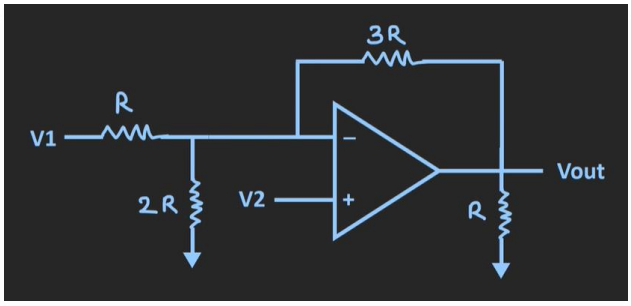
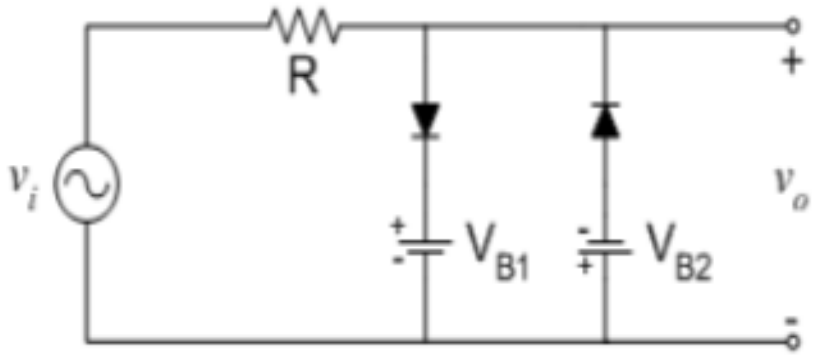
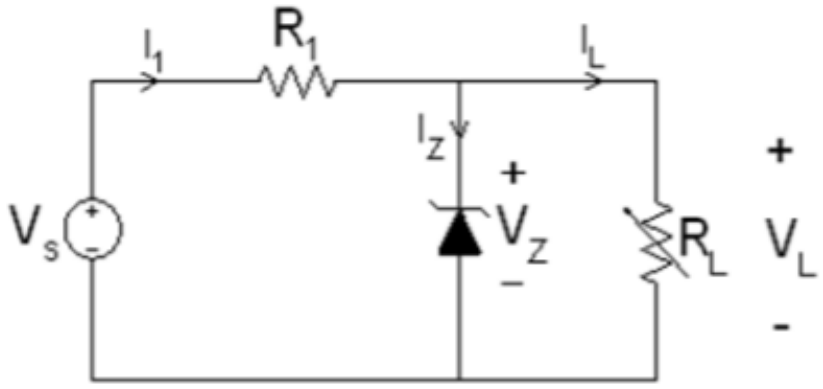
TUTORIAL TEST I **Session: 2021**

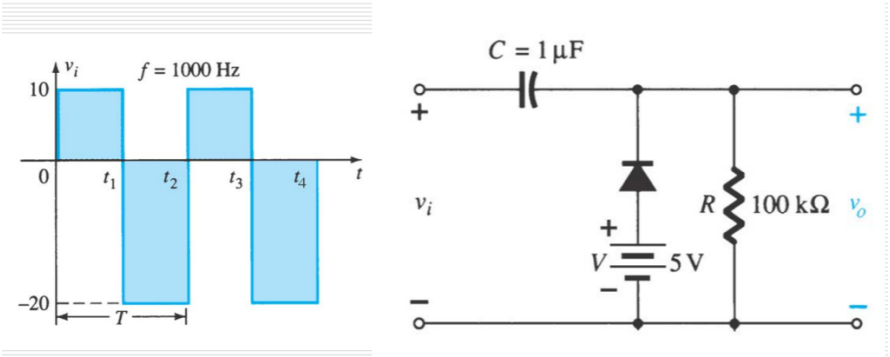
Subject: Digital Electronics & Logic Design **Duration:** 45 min

Instructions: 1. It is mandatory to attempt all the questions sequentially
2. Mention your complete admission number and name on all the pages of answer sheet
3. Take the clear scan copy of your answer sheet. Combine it in a single PDF file.
4. Rename your PDF with your Admission number and then upload it in the assignment.

1	Determine the values of V_{CB} and current I_B for the common base configuration shown in Fig1  Fig. 1	(2 M)
2	Determine the bias voltage V_{CE} and current I_C for the voltage divider configuration in Fig 2.  Fig. 2	(2 M)

3	Sketch the transfer characteristics for the n-channel depletion type MOSFET with I_{DSS}=10 mA, and V_P = - 4V.	(2 M)
4	Calculate the dc voltages (V_C, V_B, V_E) and currents (I_B, I_E, I_C) in the circuit of the Fig. 3  Fig.3	(3 M)
5	Given the load line of the Fig. 4 and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.  Fig. 4	(2 M)

6	Find the expression of the output voltage in terms of V_1 and V_2  Fig. 5	(3 M)
7	Op-Amp has Gain Bandwidth product of 1 MHz. Find the bandwidth of non-inverting Op-amp which has gain of 20 dB.	(3 M)
8	For the circuit shown below, find the output for a sinusoidal input Vi(t)=Vm.Sin(2πt/T) where (V_{B1}, V_{B2}) < V_m  Fig. 6	(2 M)
9	In the Fig 7 , Vs is the unregulated voltage that varies between 6 V and 7 V while the zener diode voltage is V_Z= 5V. The load resistor R_L can have a value from 100 Ω to ∞ (i.e. open circuit) I_{Zmin}=0 A. Find the maximum value of R_1 that the load voltage V_L would be still kept constant at 5V for all values of R_L and Vs.  Fig. 7	(3 M)

10	Determine V_0 for the following clamper circuit with the input shown. Consider an ideal diode.  Fig.8	(3 M)
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