Experiment No.: 2

Diode Clamper Circuits

Date: 13/08/2021
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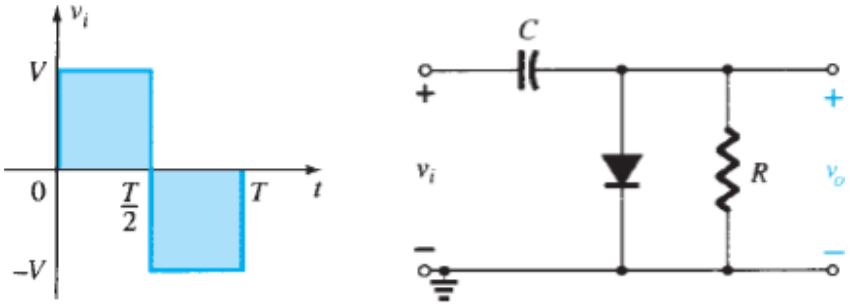
Admission No.: U20CS110

Aim: To study, design and plot the various Clamper Circuits.

SOFTWARE TOOLS / OTHER REQUIREMENTS:
Multisim Simulator/Circuit Simulator

Theory:
A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal. Additional shifts can also be obtained by introducing a dc supply to the basic structure. The resistor and capacitor of the network must be chosen such that the time constant determined by t=RC is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is not conducting. Throughout the analysis we assume that for all practical purposes the capacitor fully charges or discharges in five time constants.

The simplest of clamper networks is shown in figure below. It is important to note that the capacitor is connected directly between input and output signals and the resistor and the diode are connected in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.



Analysis

Step 1: Start the analysis by examining the response of the portion of the input signal that will forward bias the diode.

Step 2: During the period that the diode is in the "ON" state, assume that the capacitor will charge up instantaneously to a voltage level

determined by the surrounding network.

For the network shown above the diode will be forward biased for the positive portion of the applied signal. For the interval 0 to *T*/2 the network will appear as shown in **Fig. a** below. The short-circuit equivalent for the diode will result in *Vo*=0 V for this time interval. During this same interval of time, the time constant determined by t=*RC* is very small because the resistor *R* has been effectively "shorted out" by the conducting diode and the only resistance present is the inherent (contact, wire) resistance of the network. The result is that the capacitor will quickly charge to the peak value of *V* volts as shown in **Fig. a** with the polarity indicated in the figure below.

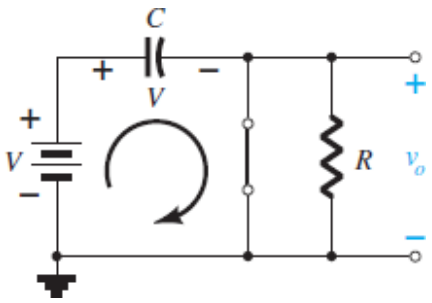


Fig. a

Step 3: Assume that during the period when the diode is in the "off" state the capacitor holds on to its established voltage level.

Step 4: Throughout the analysis, maintain a continual awareness of the location and defined polarity for Vo to ensure that the proper levels are obtained.

When the input switches to the -*V* state, the network will appear as shown in **Fig.b**, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that *R* is back in the network the time constant determined by the *RC* product is sufficiently large to establish a discharge period 5t, much greater than the period *T*, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since $V = Q/C$) during this period.

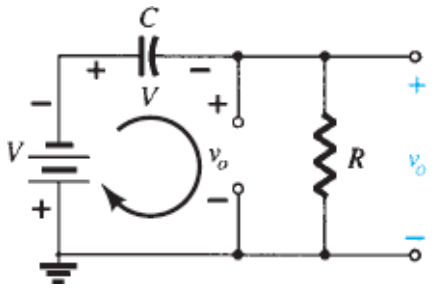


Fig. b

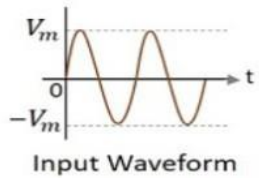
Since *Vo* is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig.b . Applying Kirchhoff's voltage law around the input loop results in

The negative sign results from the fact that the polarity of 2 *V* is opposite to the polarity defined for *Vo.*

Step 5: Check that the total swing of the output matches that of the input.

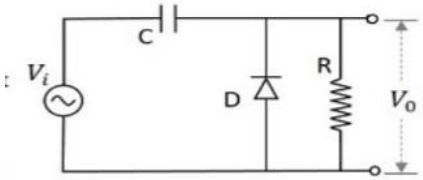
This is a property that applies for all clamping networks, giving an excellent check on the results obtained.

Few Clamper Configurations

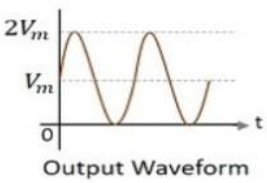


Input Waveform

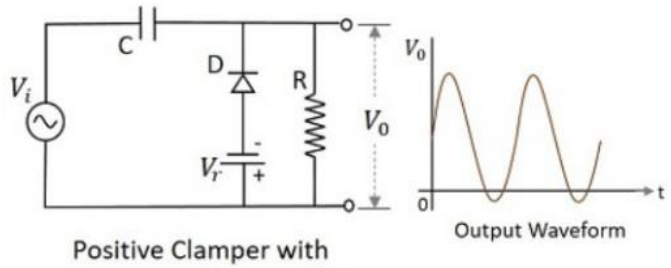
Common Input for all below circuits



Positive Clamper circuit

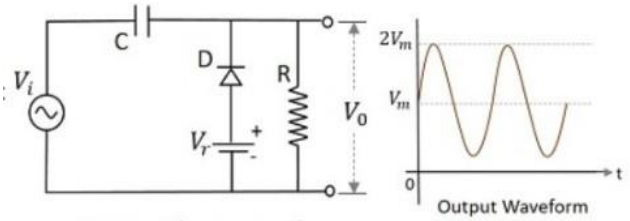


Output Waveform



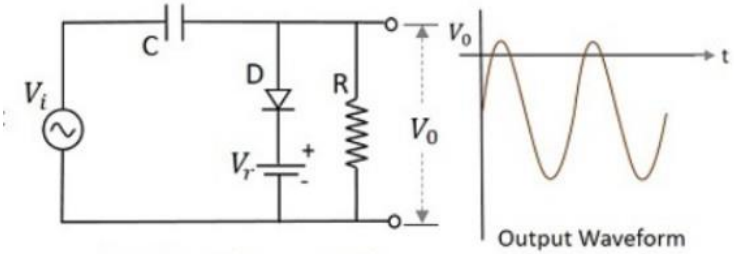
Output Waveform

Positive Clamper with negative reference V_r



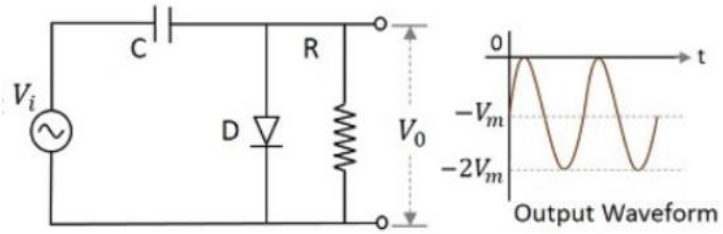
Output Waveform

Positive Clamper with positive reference V_r



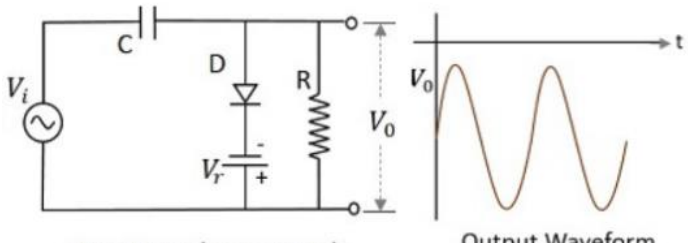
Output Waveform

Negative Clamper with positive reference V_r



Output Waveform

Negative Clamper circuit

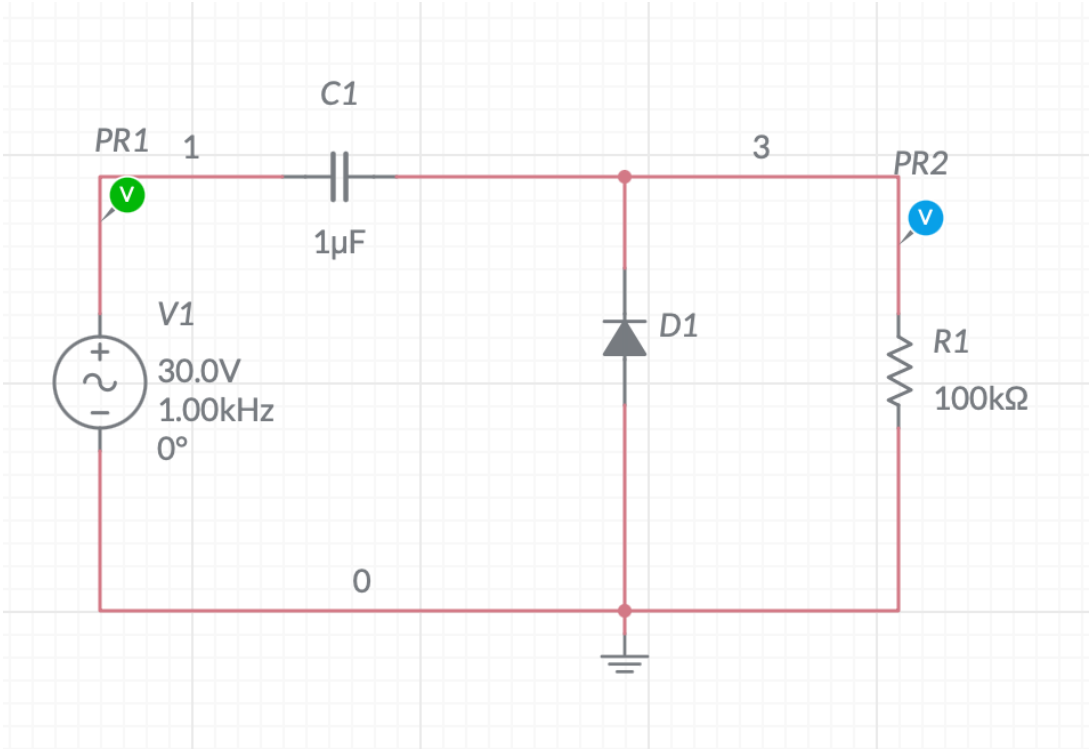


Output Waveform

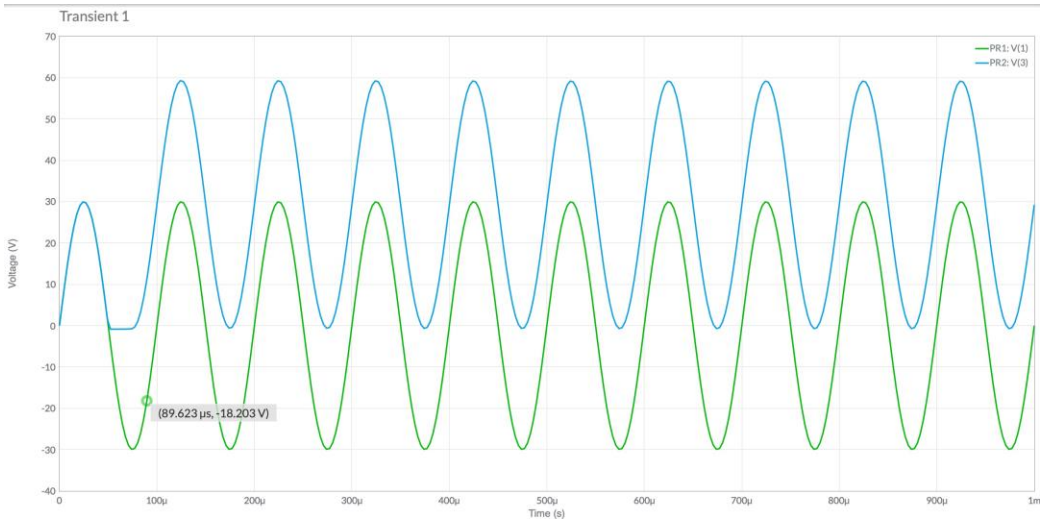
Negative Clamper with negative reference V_r

Positive Clamper

Circuit/Connection diagrams (from MultiSim)

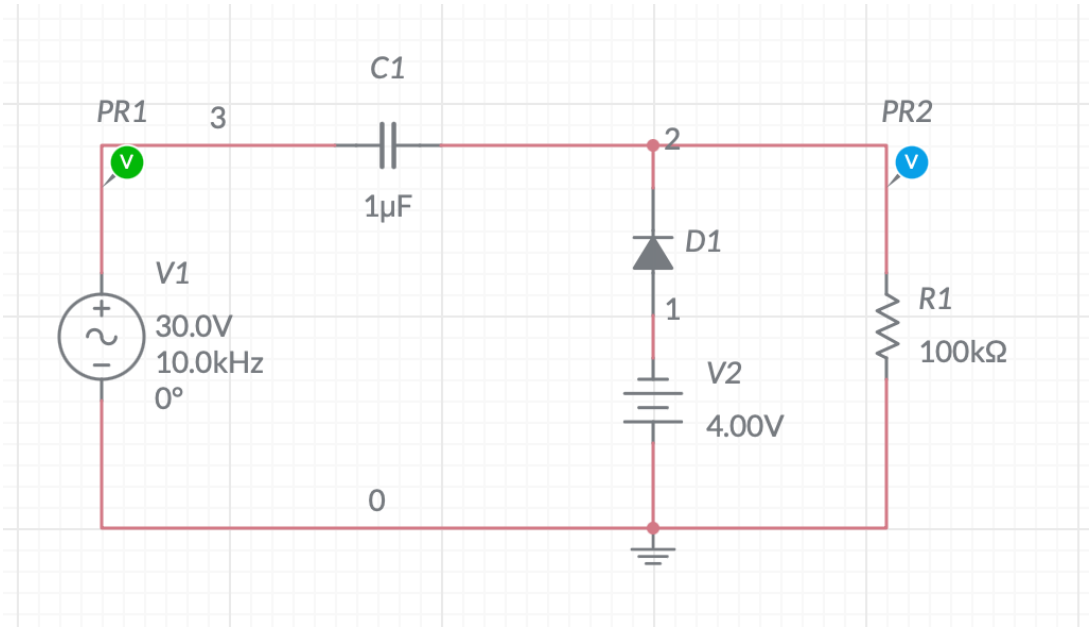


Waveforms (from MultiSim)

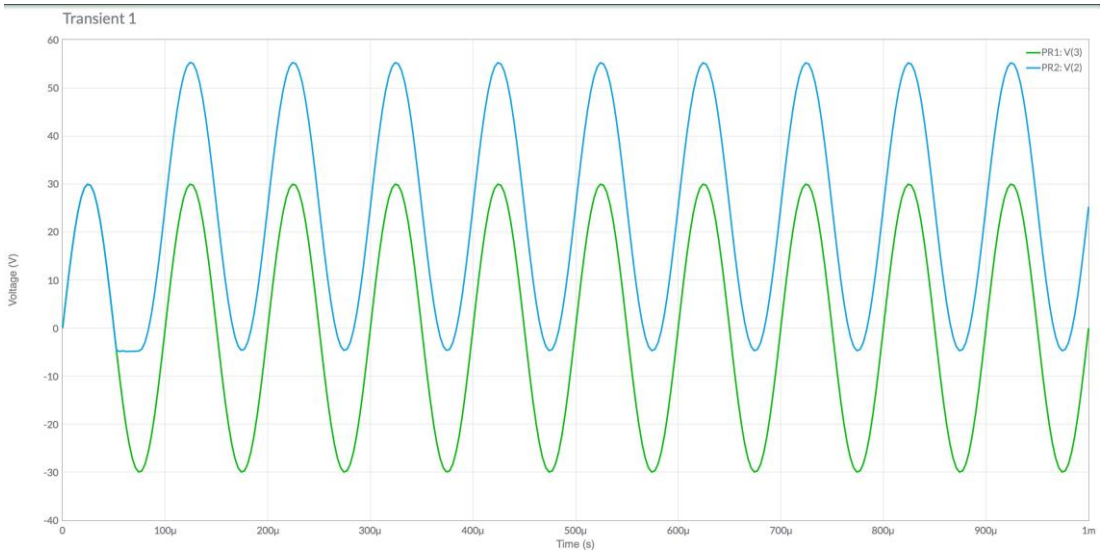


Positive Clamper with negative reference

Circuit/Connection diagrams (from MultiSim)

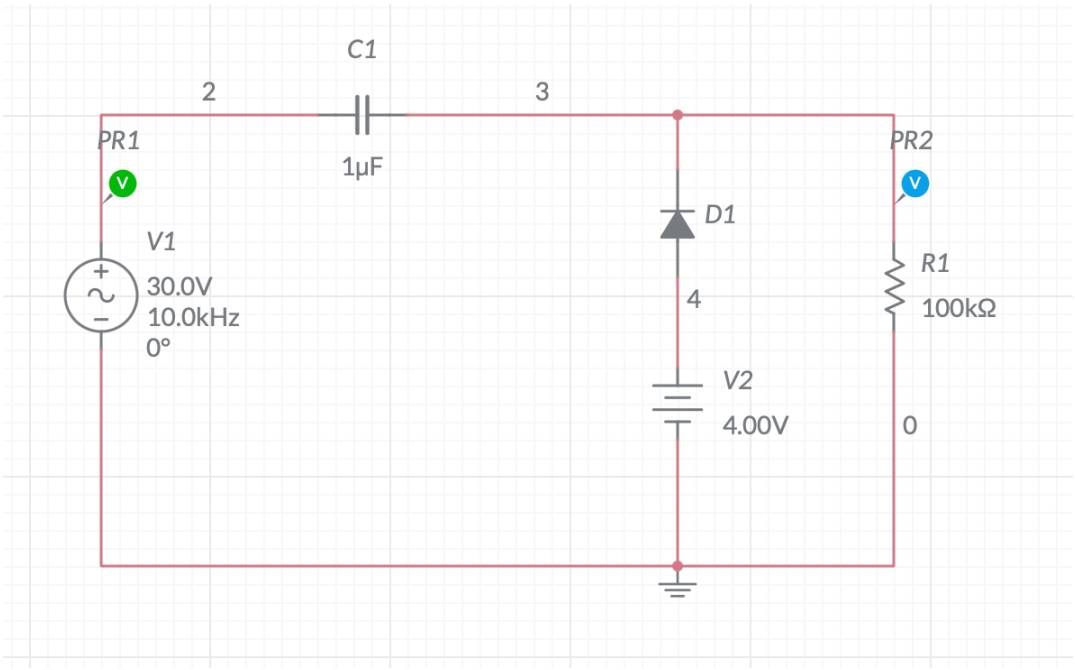


Waveforms (from MultiSim)



Positive Clamper with positive reference

Circuit/Connection diagrams (from MultiSim)



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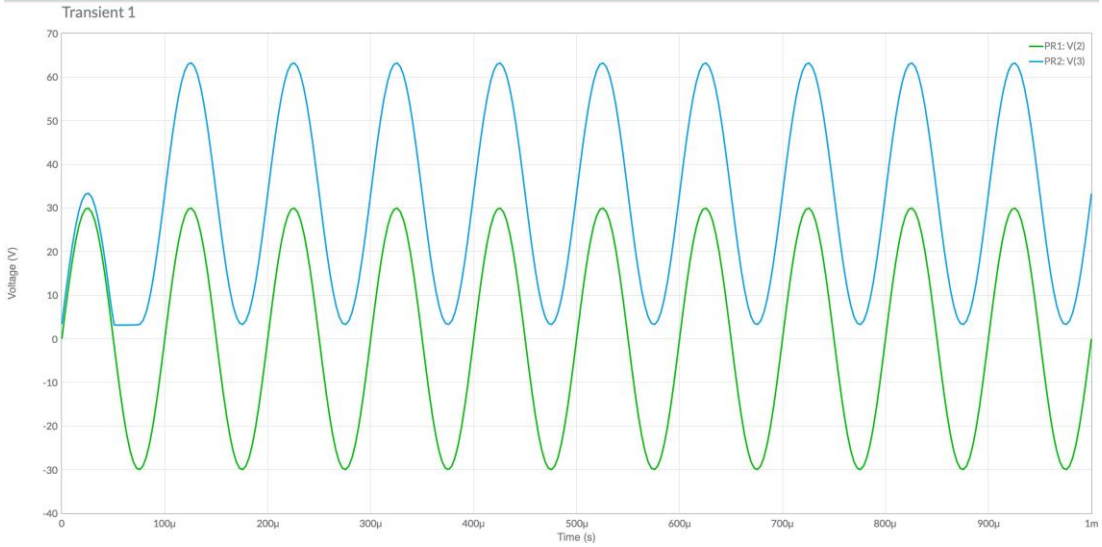
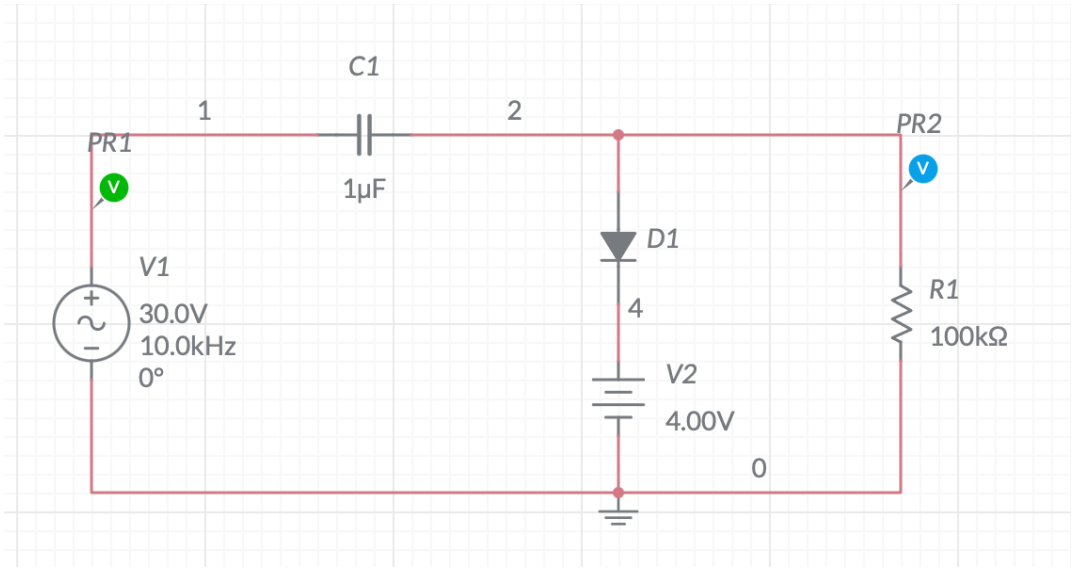


Negative Clamper with positive reference

Circuit/Connection diagrams (from MultiSim)



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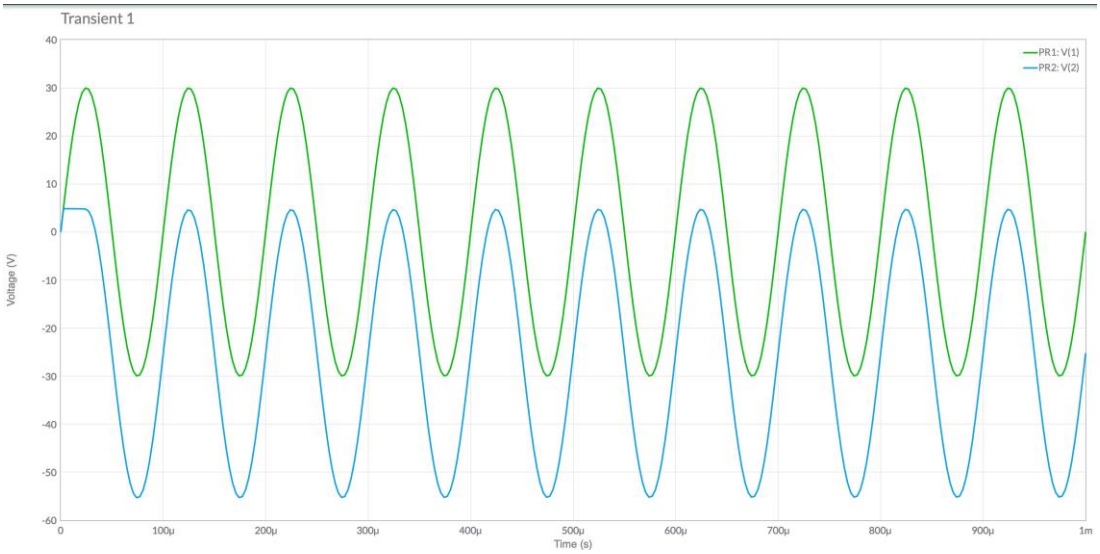
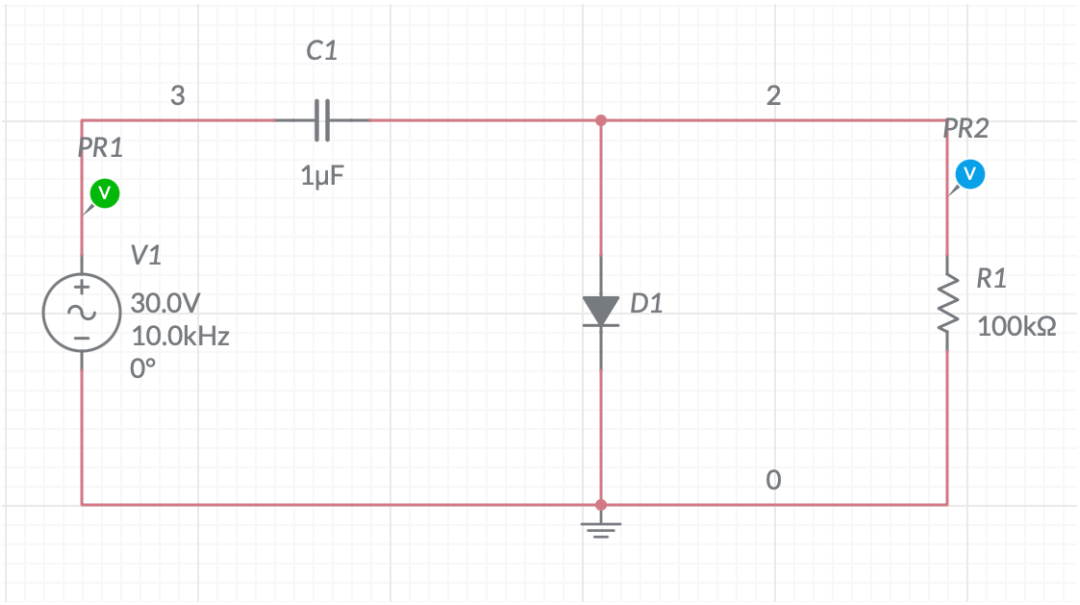


Negative Clamper

Circuit/Connection diagrams (from MultiSim)



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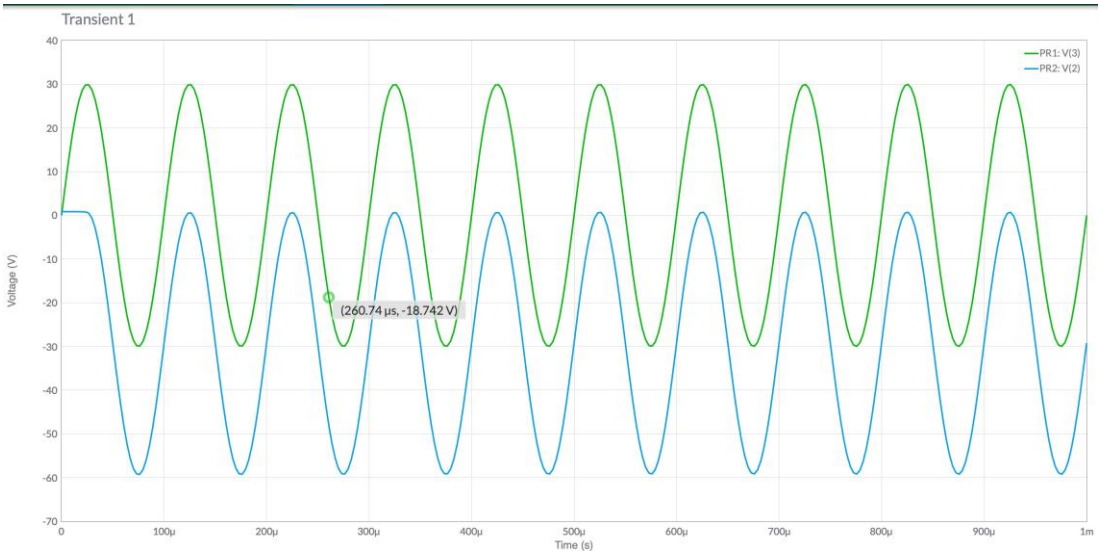

Negative Clamper with negative reference

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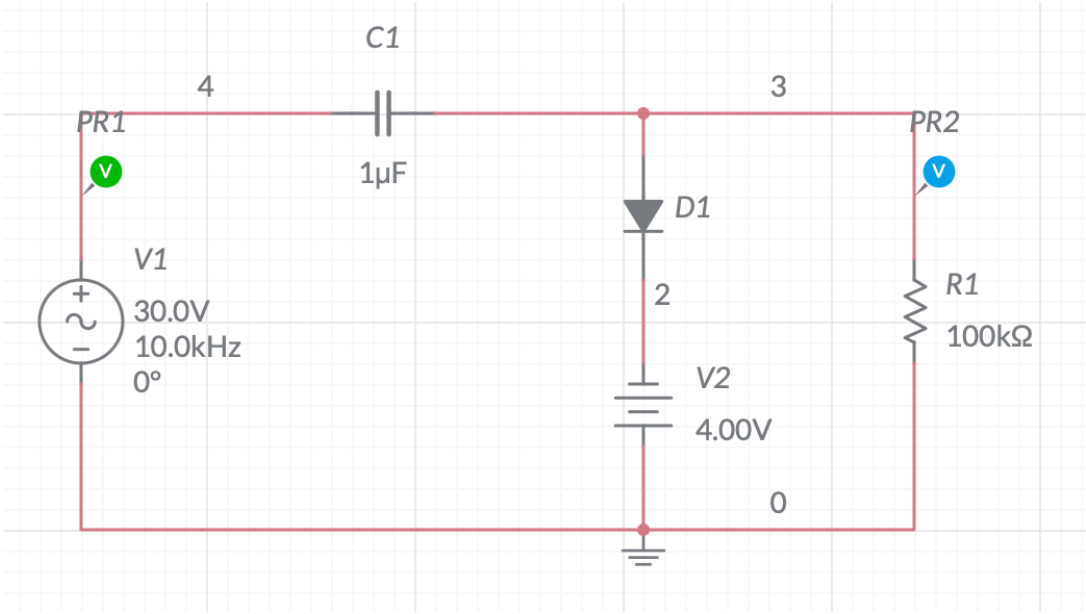

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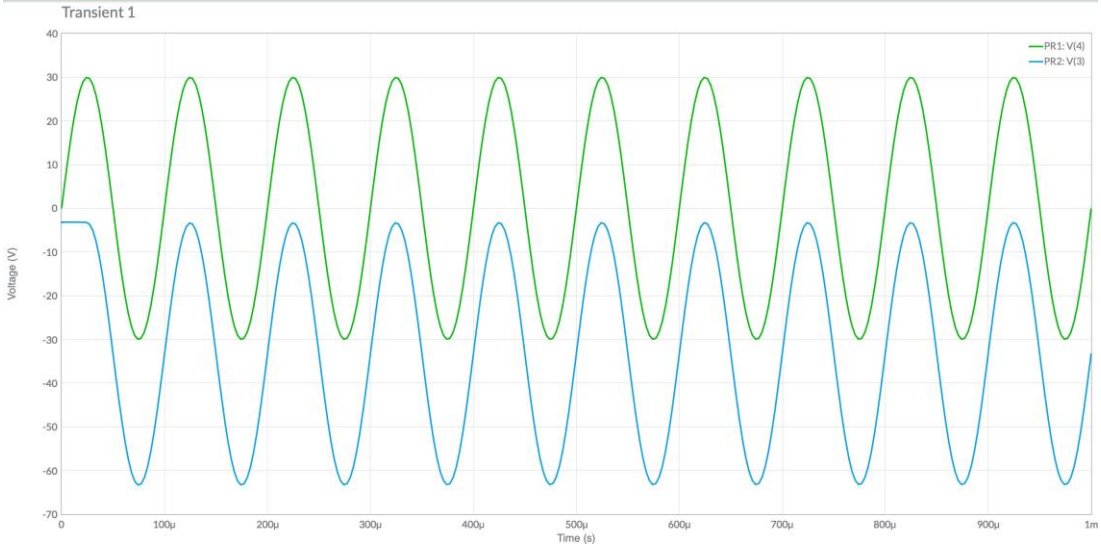
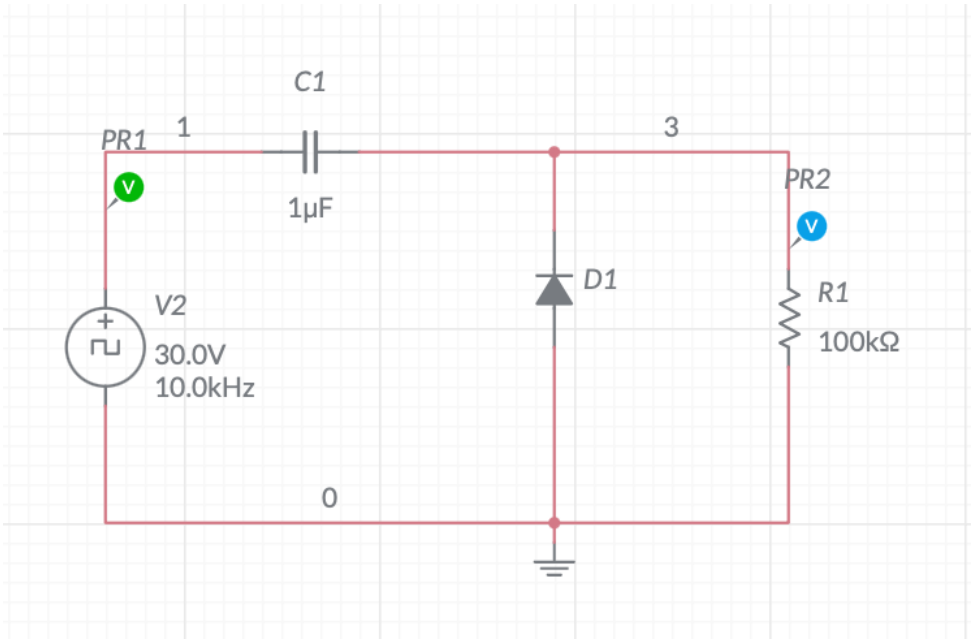


Conclusions: -

HERE, THE PRACTICAL AND THEORITICAL CHARACTERISTICS OF VERIOUS NEGATIVE AND POSITIVE CLAMPER (WITH AND WITHOUT BIAS) CIRCUITS ARE SAME. HENCE VERIFIED.

Assignment

Circuit/Connection diagrams (from MultiSim)



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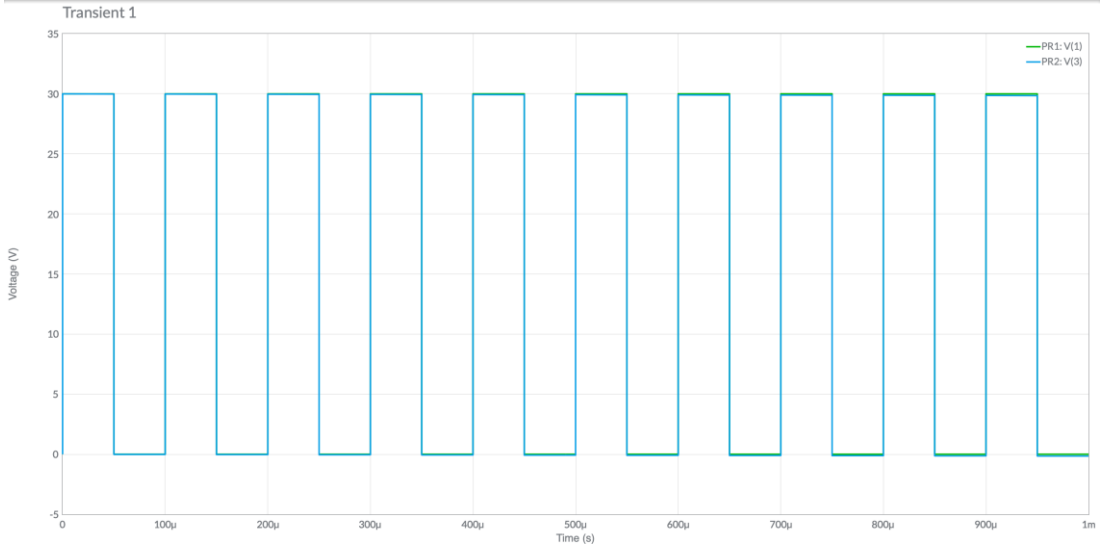

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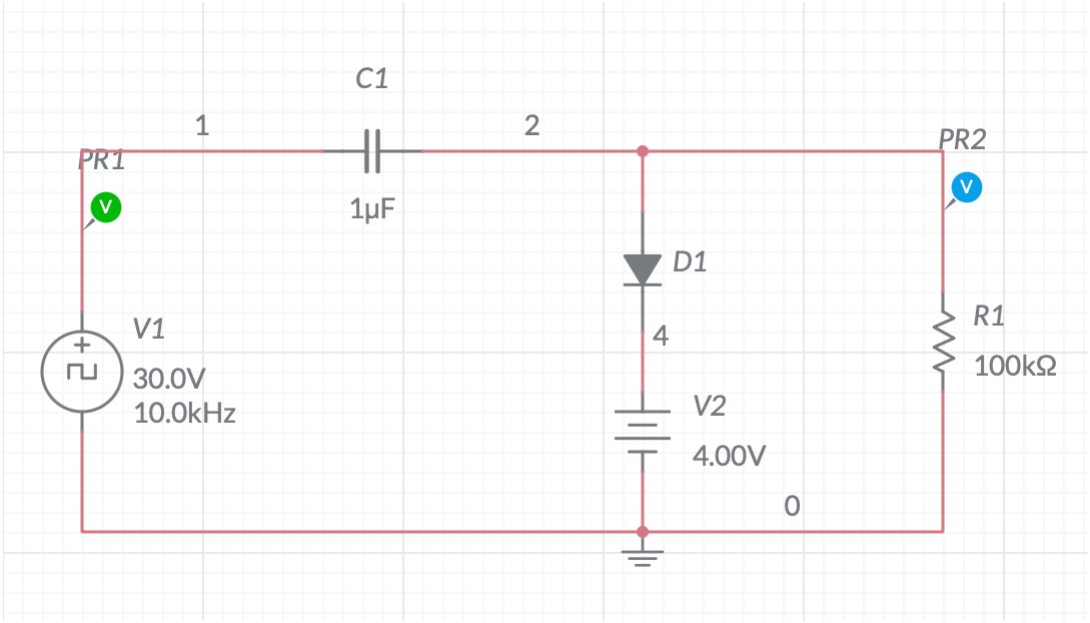

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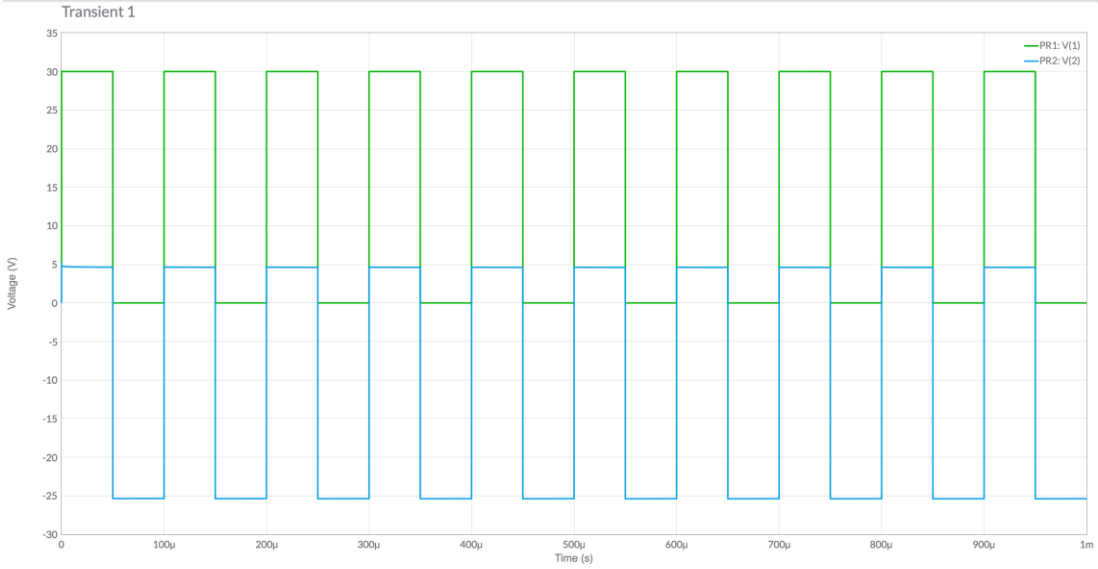

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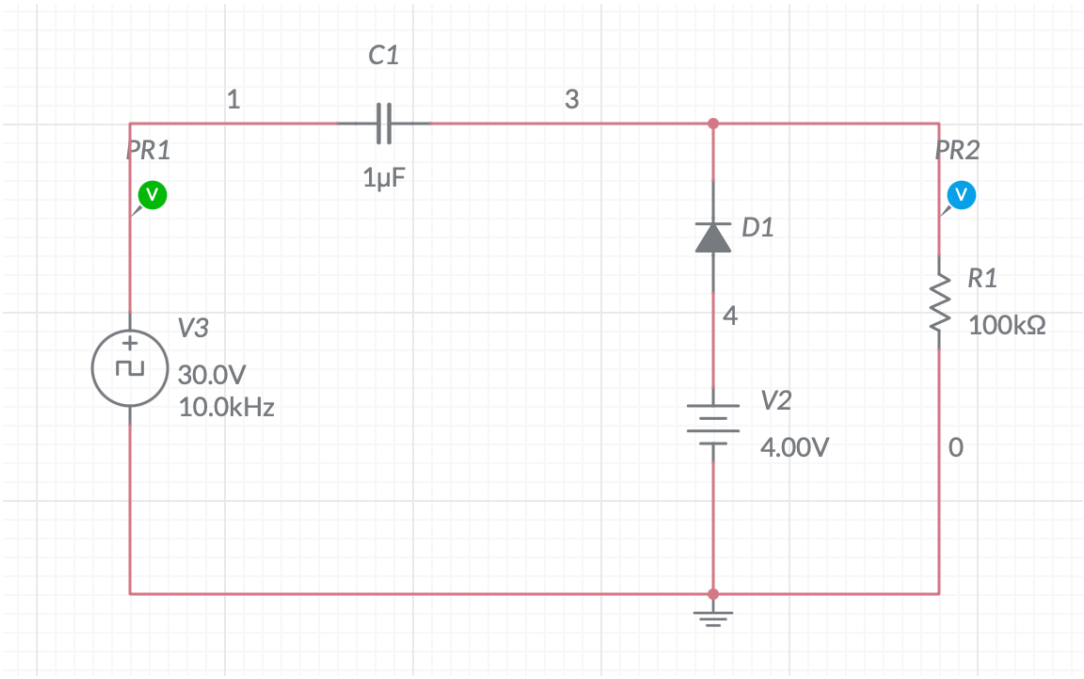

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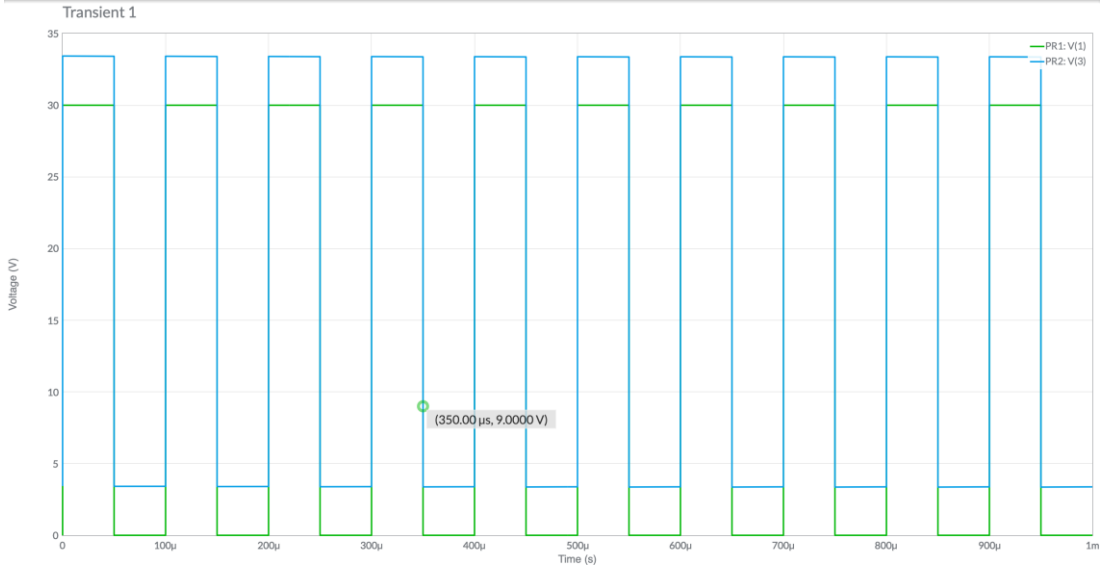

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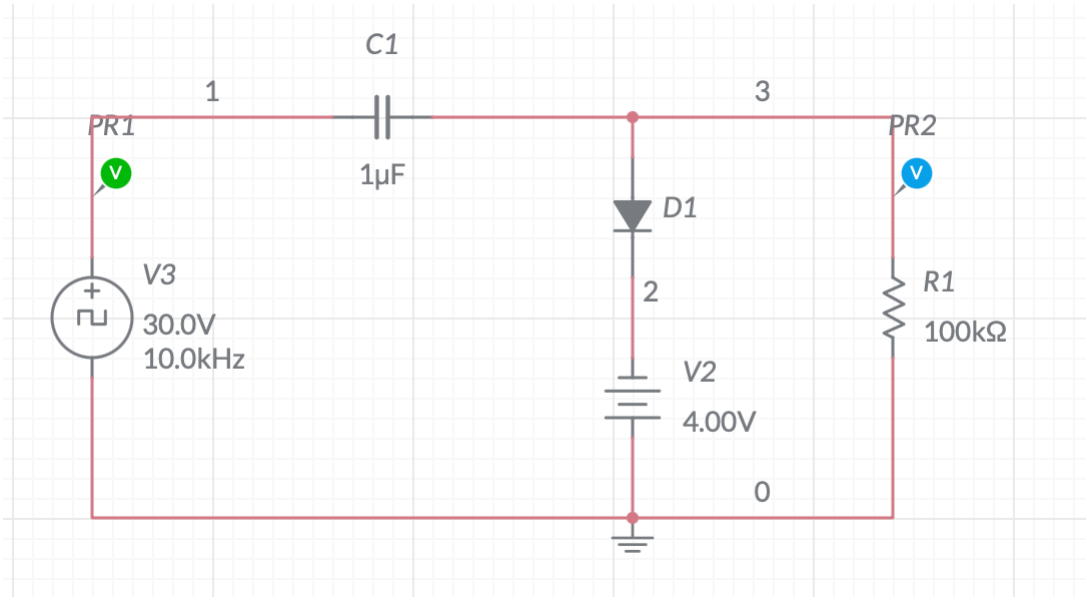

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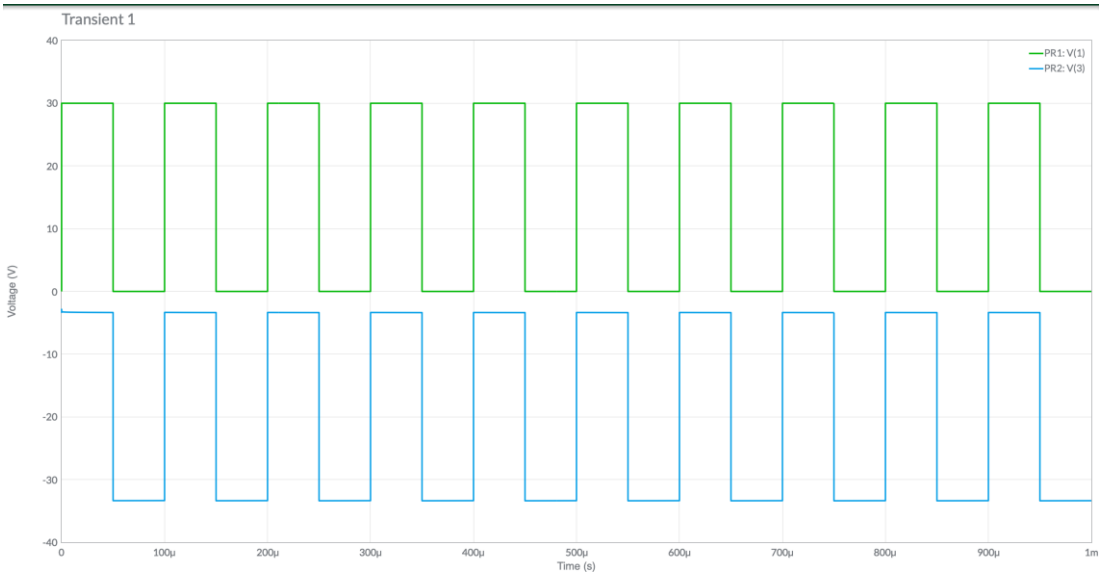

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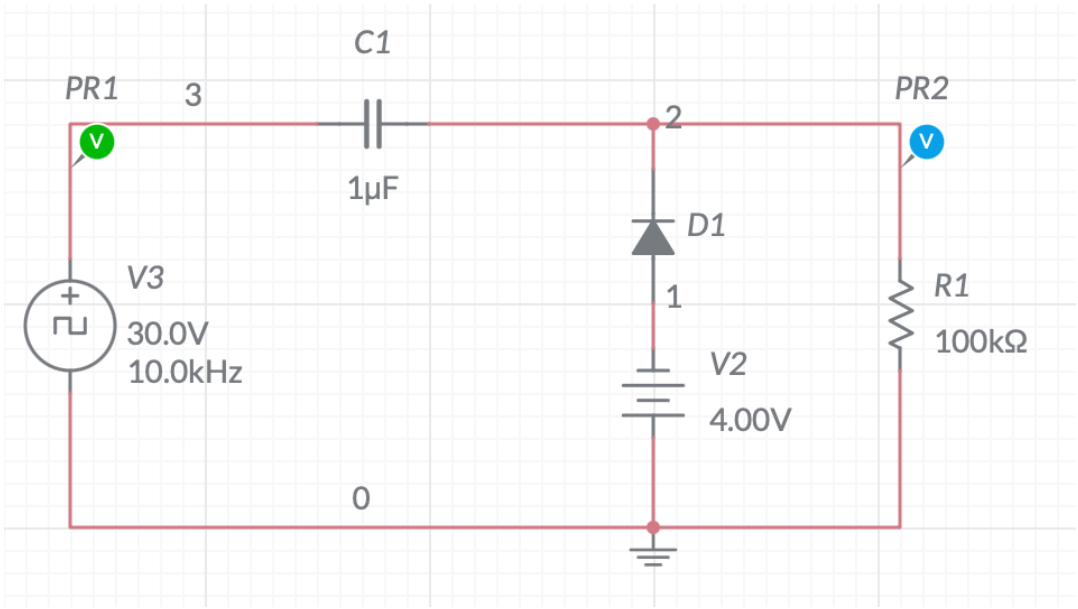

Waveforms (from MultiSim)