DIGITAL ELECTRONICS AND LOGIC DESIGN [EC - 207]

SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT ELECTRONICS ENGINEERING DEPARTMENT

SR AND JK FLIP FLOP USING NAND AND NOR GATE

AIM :- To Design and Implement SR and JK flip flop using NAND and NOR gate using Multi-sim Software.

SOFTWARE TOOLS / OTHER REQUIREMENTS:

(1). Multisim Simulator.

THEORY :-

- SR Flip Flop :-

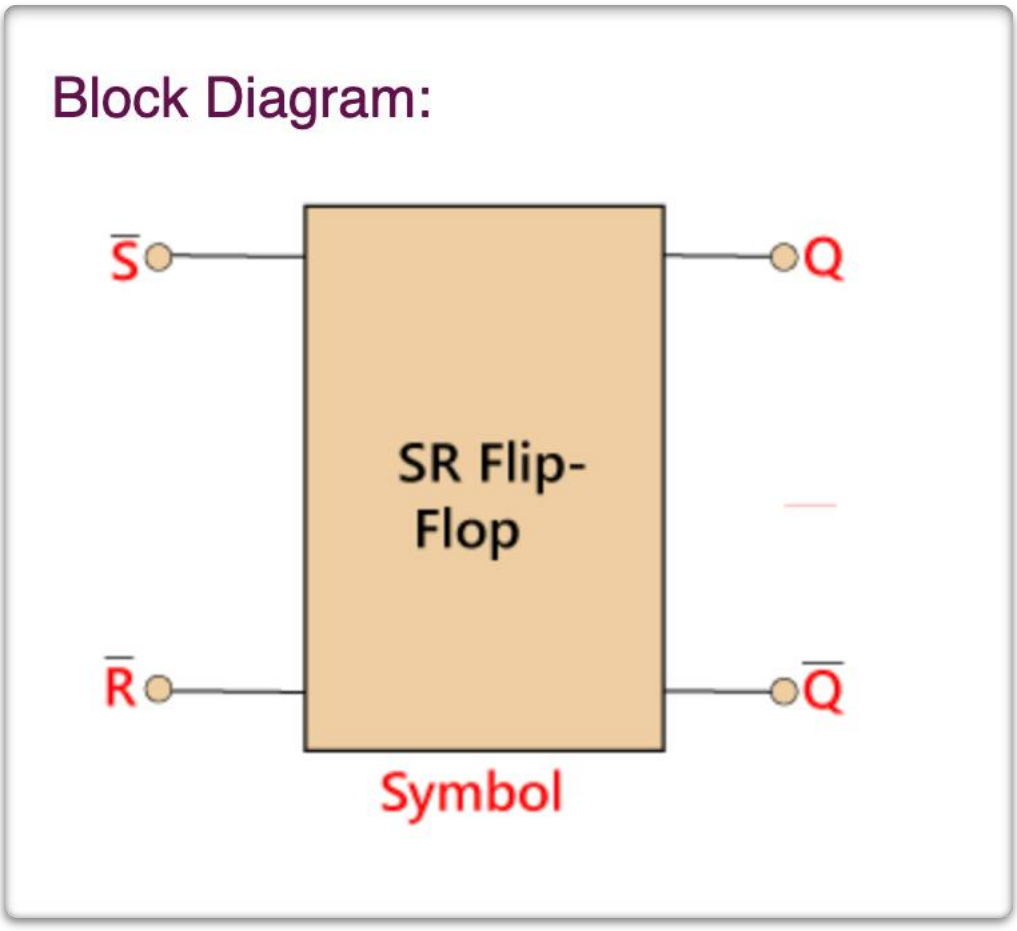
The SR flip flop is a 1-bit memory bistable device having two inputs, i.e., SET and RESET. The SET input 'S' set the device or produce the output 1, and the RESET input 'R' reset the device or produce the output 0. The SET and RESET inputs are labeled as **S** and **R**, respectively.

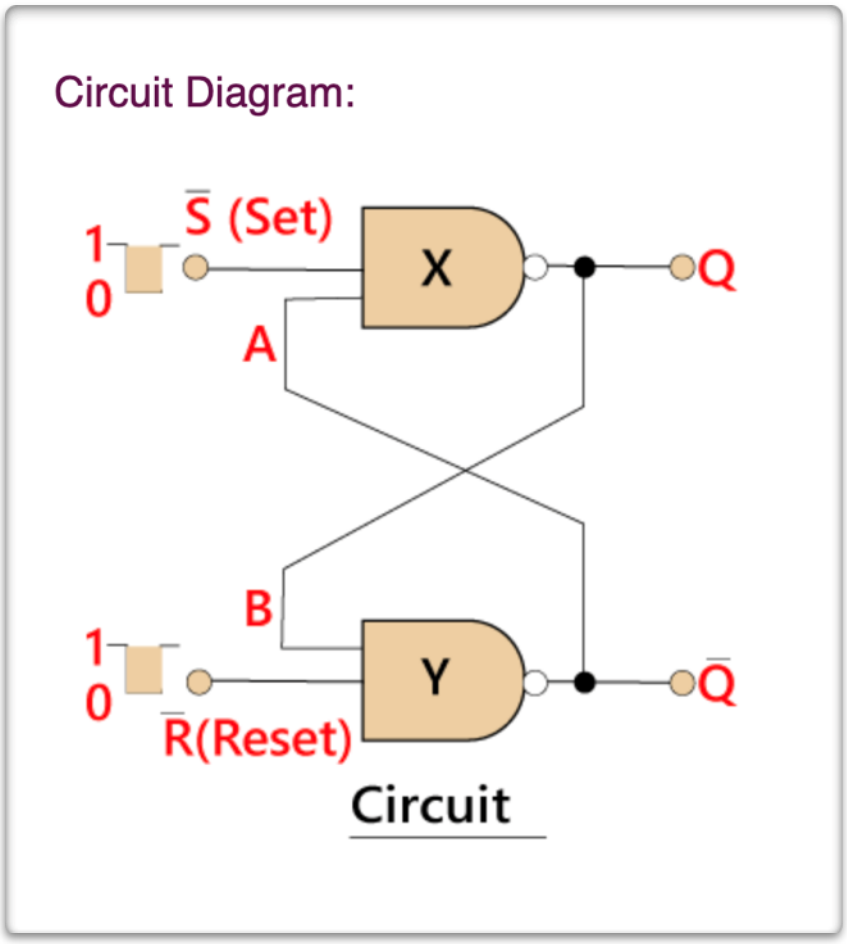
The SR flip flop stands for "Set-Reset" flip flop. The reset input is used to get back the flip flop to its original state from the current state with an output 'Q'. This output depends on the set and reset conditions, which is either at the logic level "0" or “1".

The NAND gate SR flip flop is a basic flip flop which provides feedback from both of its outputs back to its opposing input. This circuit is used to store the single data bit in the memory circuit. So, the SR flip flop has a total of three inputs, i.e., 'S' and 'R', and current output 'Q'. This output 'Q' is related to the current history or state. The term "flip-flop" relates to the actual operation of the device, as it can be "flipped" to a logic set state or "flopped" back to the opposing logic reset state.

- The NAND Gate SR Flip-Flop :-

We can implement the set-reset flip flop by connecting two cross-coupled 2-input NAND gates together. In the SR flip flop circuit, from each output to one of the other NAND gate inputs, feedback is connected. So, the device has two inputs, i.e., Set 'S' and Reset 'R' with two outputs Q and Q' respectively. Below are the block diagram and circuit diagram of the S-R flip flop.





- The Set State :-

In the above diagram, when the input R is set to false or 0 and the input S is set to true or 1, the NAND gate Y has an input 0, which will produce the output Q' 1. The value of Q' is faded to the NAND gate 'X' as input 'A', and now both the inputs of the NAND gate 'X' are 1(S=A=1), which will produce the output 'Q' 0.

Now, if the input R is changed to 1 with 'S' remaining 1, the inputs of NAND gate 'Y' is R=1 and B=0. Here, one of the inputs is also 0, so the output of Q' is 1. So, the flip flop circuit is set or latched with Q=0 and Q'=1.

- Reset State :-

The output Q' is 0, and output Q is 1 in the second stable state. It is given by R =1 and S = 0. One of the inputs of NAND gate 'X' is 0, and its output Q is 1. Output Q is faded to NAND gate Y as input B. So, both the inputs to NAND gate *Y* are set to 1, therefore, Q' = 0.

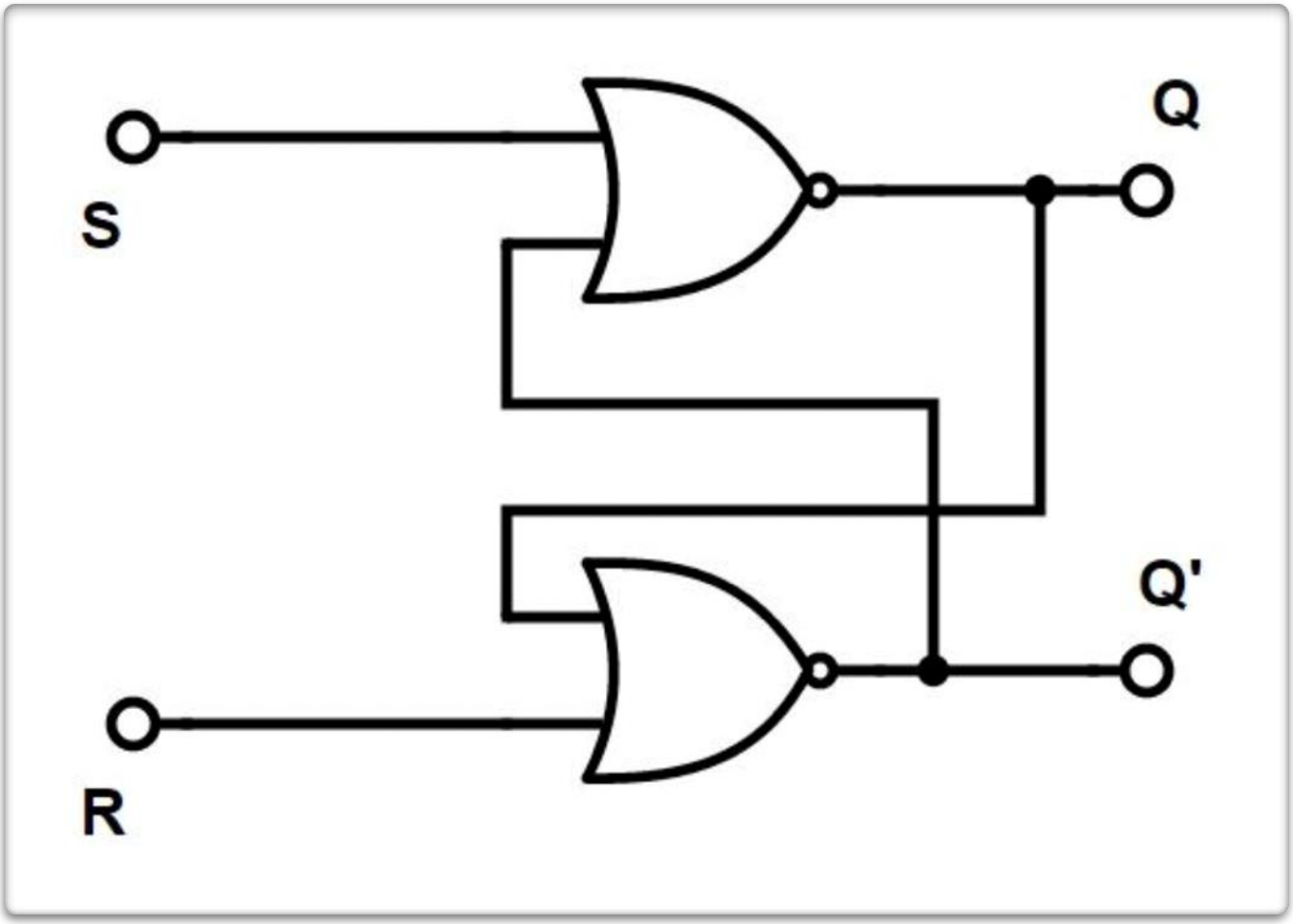
Now, if the input S is changed to 0 with 'R' remaining 1, the output Q' will be 0 and there is no change in state. So, the reset state of the flip flop circuit has been latched, and the set/reset actions are defined in the following truth table:

State	S	R	Q	Q’	Description
Set	1	0	0	1	Set Q’>>1
	1	1	0	1	No change
Reset	0	1	1	0	Reset Q’>>0
	1	1	1	0	No change
Invalid	0	0	1	1	Invalid Condition

From the above truth table, we can see that when set 'S' and reset 'R' inputs are set to 1, the outputs Q and Q' will be either 1 or 0. These outputs depend on the input state S or R before the input condition exist. So, when the inputs are 1, the states of the outputs remain unchanged.

The condition in which both the inputs states are set to 0 is treated as invalid and must be avoided.

- The NOR Gate SR Flip-Flop :-



- JK Flip Flop :-

The SR Flip Flop or Set-Reset flip flop has lots of advantages. But, it has the following switching problems:

- When Set 'S' and Reset 'R' inputs are set to 0, this condition is always avoided.
- When the Set or Reset input changes their state while the enable input is 1, the incorrect latching action occurs.

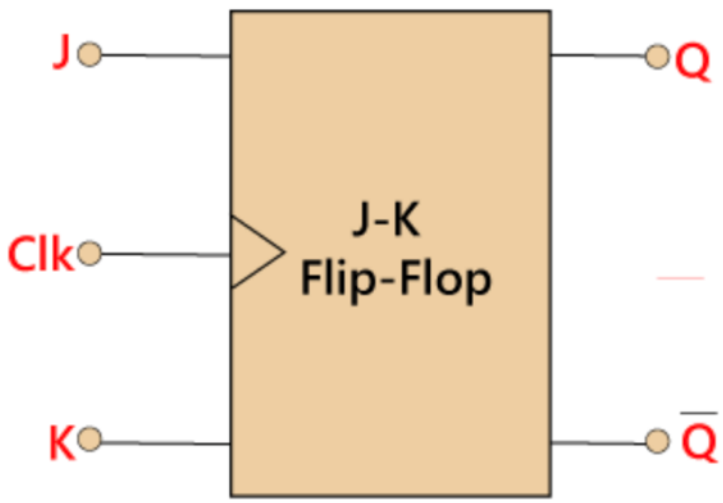
The JK Flip Flop removes these two drawbacks of SR Flip Flop.

The JK flip flop is one of the most used flip flops in digital circuits. The JK flip flop is a universal flip flop having two inputs 'J' and 'K'. In SR flip flop, the 'S' and 'R' are the shortened abbreviated letters for Set and Reset, but J and K are not. The J and K are themselves autonomous letters which are chosen to distinguish the flip flop design from other types.

The JK flip flop work in the same way as the SR flip flop work. The JK flip flop has 'J' and 'K' flip flop instead of 'S' and 'R'. The only difference between JK flip flop and SR flip flop is that when both inputs of SR flip flop is set to 1, the circuit produces the invalid states as outputs, but in case of JK flip flop, there are no invalid states even if both 'J' and 'K' flip flops are set to 1.

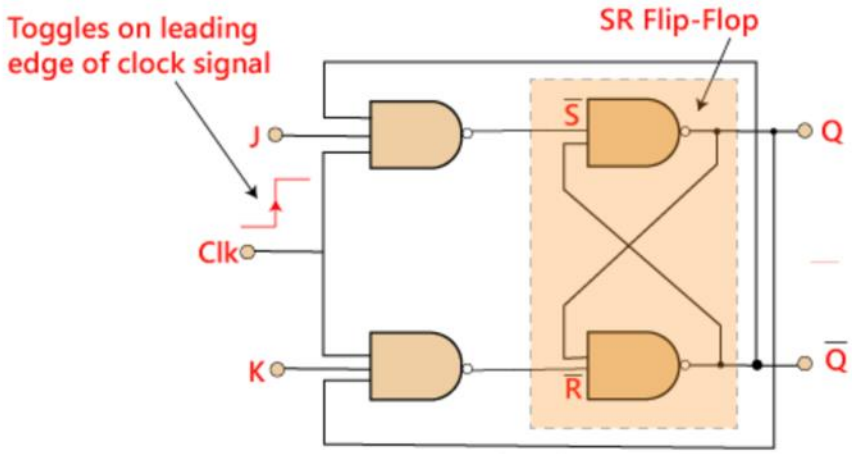
The JK Flip Flop is a gated SR flip-flop having the addition of a clock input circuitry. The invalid or illegal output condition occurs when both of the inputs are set to 1 and are prevented by the addition of a clock input circuit. So, the JK flip-flop has four possible input combinations, i.e., 1, 0, "no change" and "toggle". The symbol of JK flip flop is the same as **SR Bistable Latch** except for the addition of a clock input.

Block Diagram:



Symbol

Circuit Diagram:



Circuit

In SR flip flop, both the inputs 'S' and 'R' are replaced by two inputs J and K. It means the J and K input equates to S and R, respectively.

The two 2-input AND gates are replaced by two 3-input NAND gates. The third input of each gate is connected to the outputs at Q and Q'. The cross-coupling of the SR flip-flop permits the previous invalid condition of (S = "1", R = "1") to be used to produce the "toggle action" as the two inputs are now interlocked.

If the circuit is "set", the J input is interrupted from the "0" position of Q' through the lower NAND gate. If the circuit is "RESET", K input is interrupted from 0 positions of Q through the upper NAND gate. Since Q and Q' are always different, we can use them to control the input. When both inputs 'J' and 'K' are set to 1, the JK toggles the flip flop as per the given truth table.

Truth Table:

Same as for SR Latch	Clock	Input		Output		Description
	Clk	J	K	Q	Q'	
	X	0	0	1	0	Memory no change
	X	0	0	0	1	
	¯↓_	0	1	1	0	Reset Q>>0
	X	0	1	0	1	
	¯↓_	1	0	0	1	Set Q>>1
	X	1	0	1	0	
Toggle action	¯↓_	1	1	0	1	Toggle
	¯↓_	1	1	1	0	

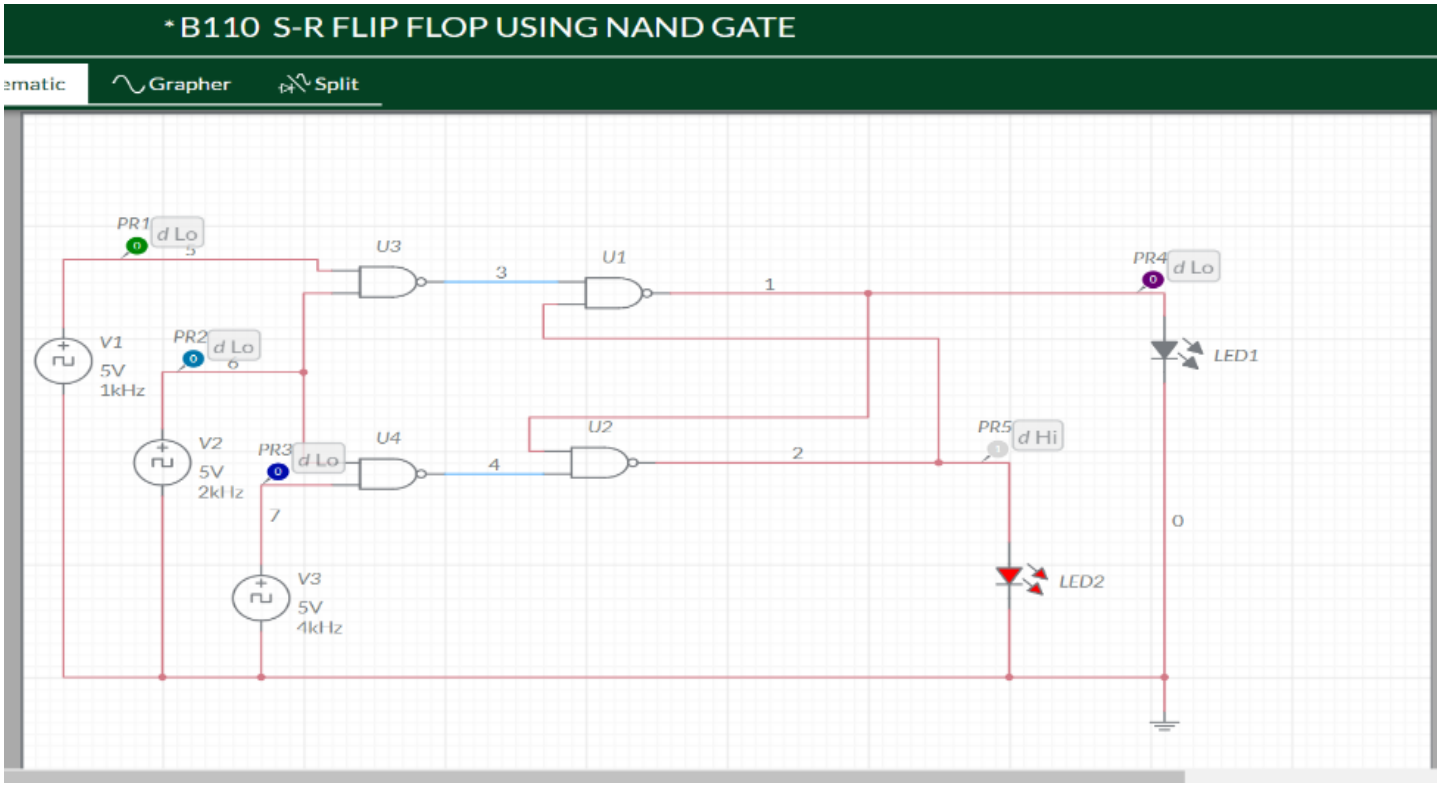
When both of the inputs of JK flip flop are set to 1 and clock input is also pulse "High" then from the SET state to a RESET state, the circuit will be toggled. The JK flip flop work as a T-type toggle flip flop when both of its inputs are set to 1.

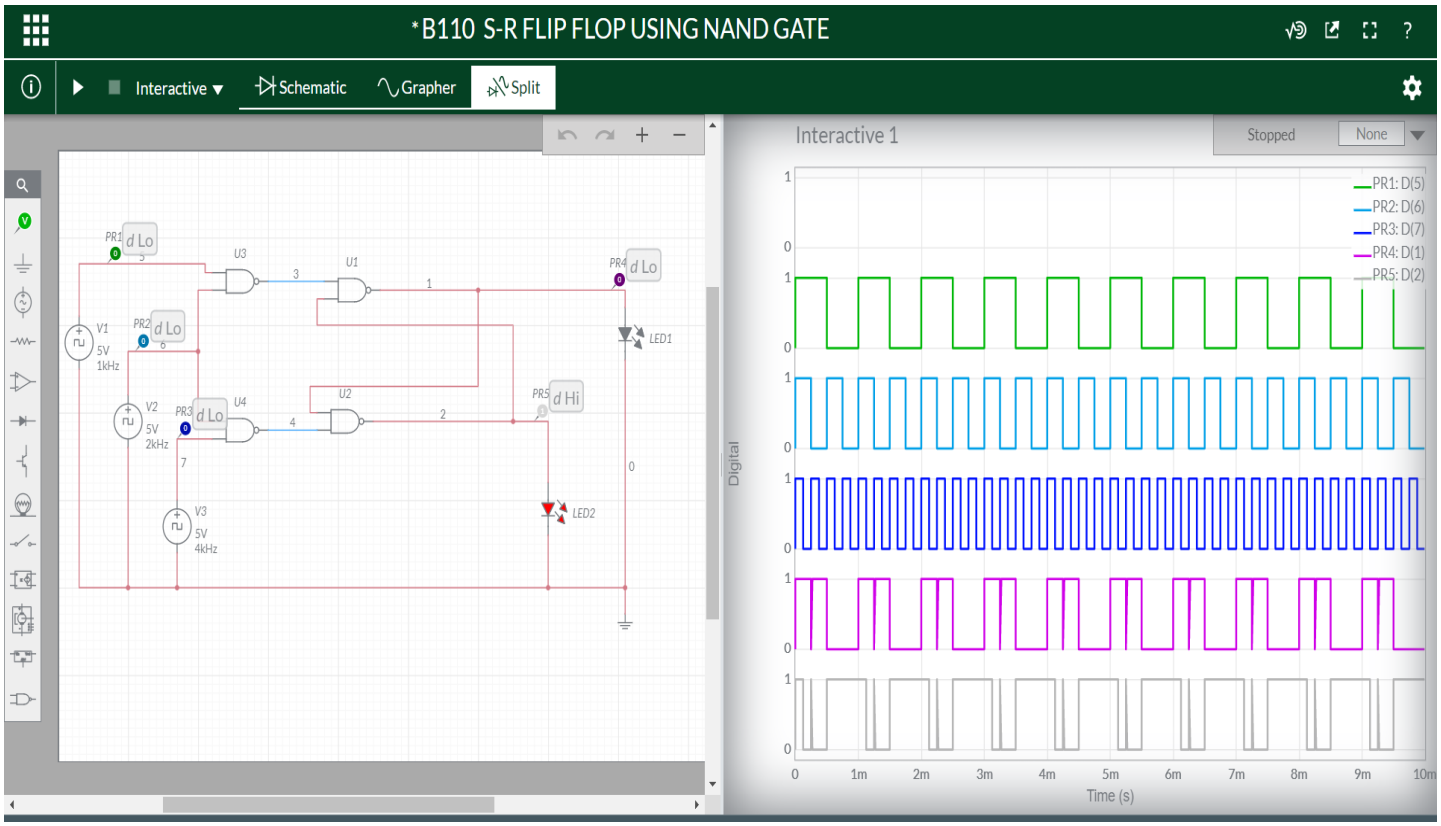
The JK flip flop is an improved clocked SR flip flop. But it still suffers from the **"race"** problem. This problem occurs when the state of the output Q is changed before the clock input's timing pulse has time to go **"Off"**. We have to keep short timing plus period (T) for avoiding this period.

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)

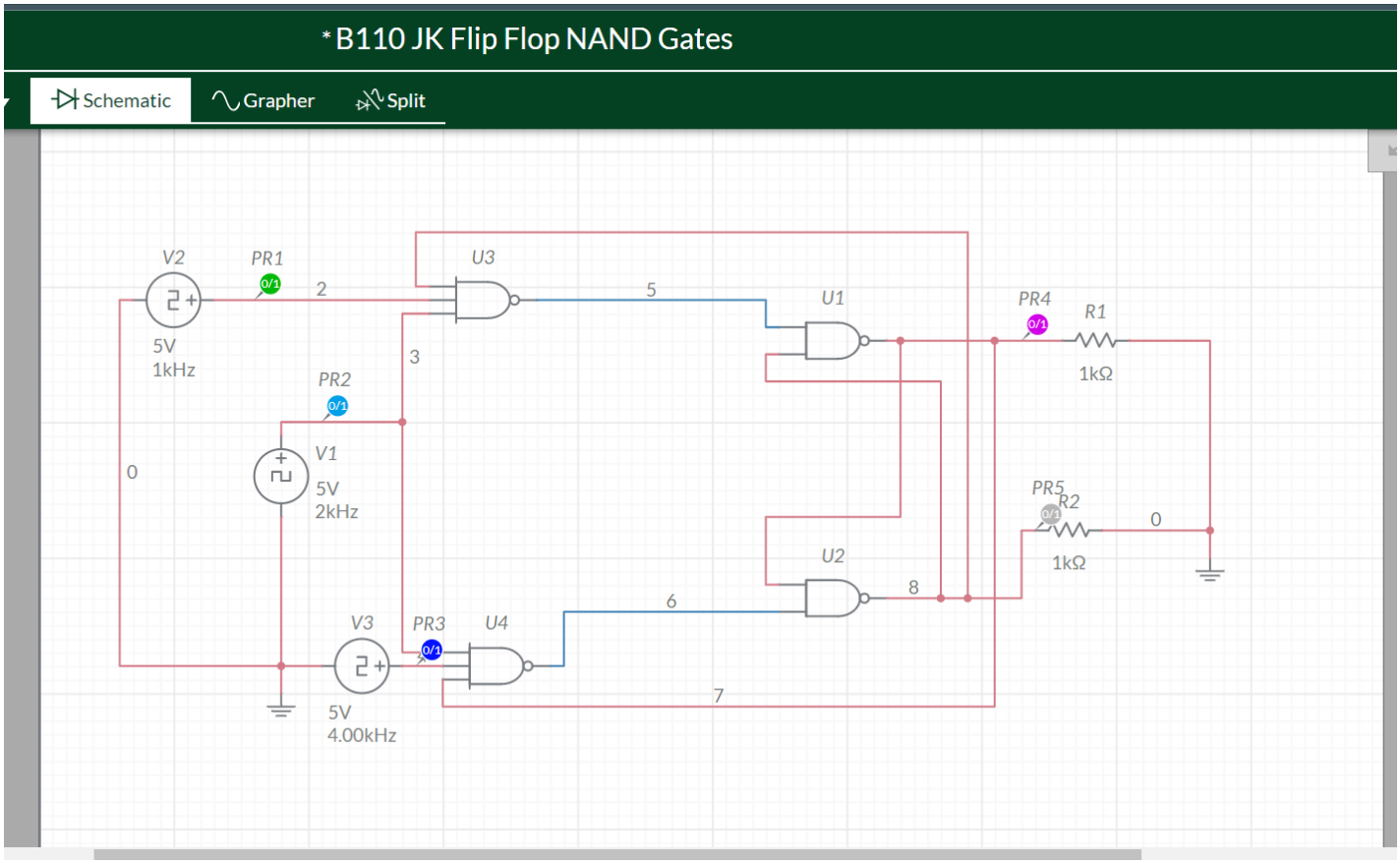
ALONG WAVEFORMS (FROM MULTISIM)

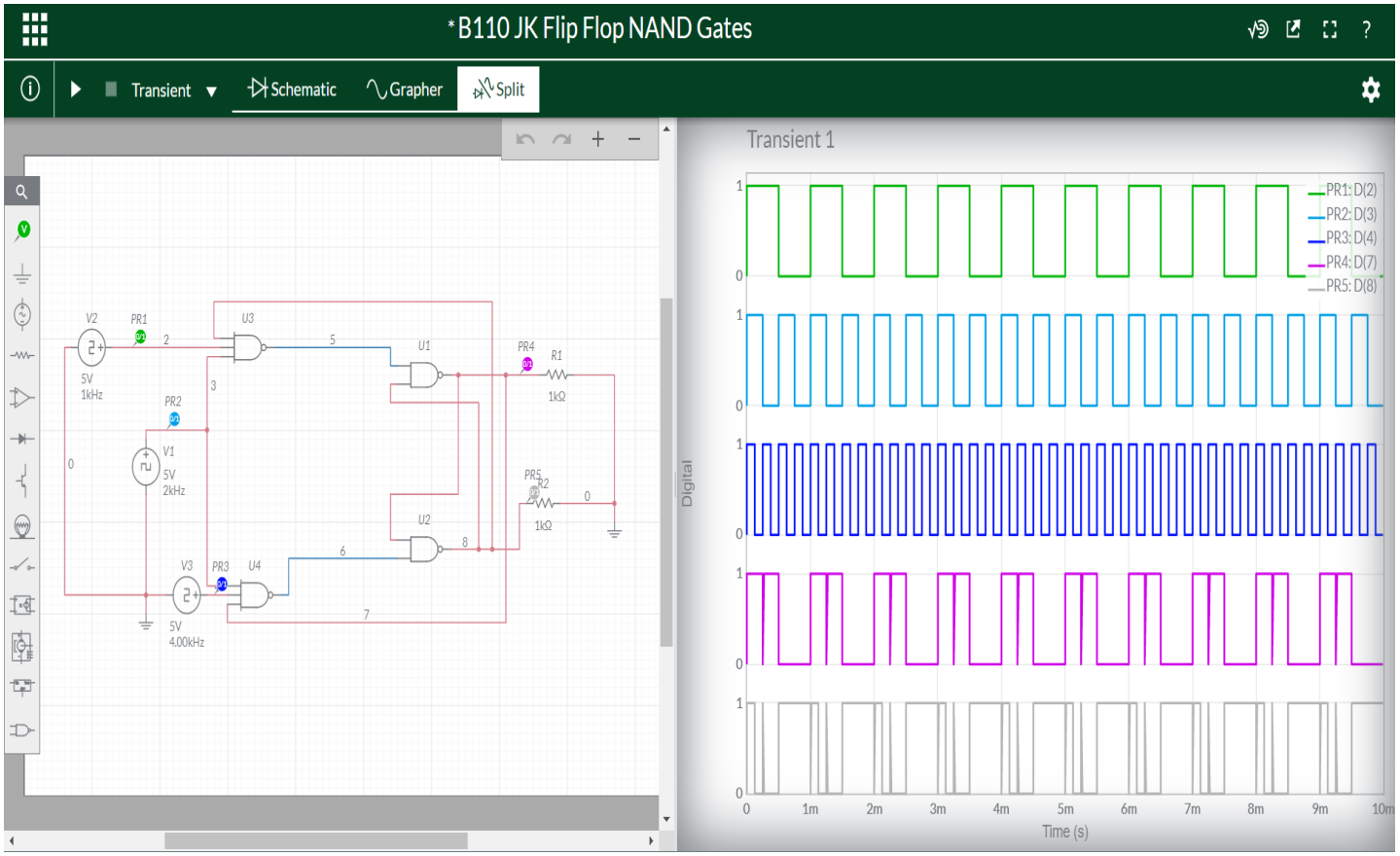
SR FLIP-FLOP USING NAND GATE CIRCUIT :-



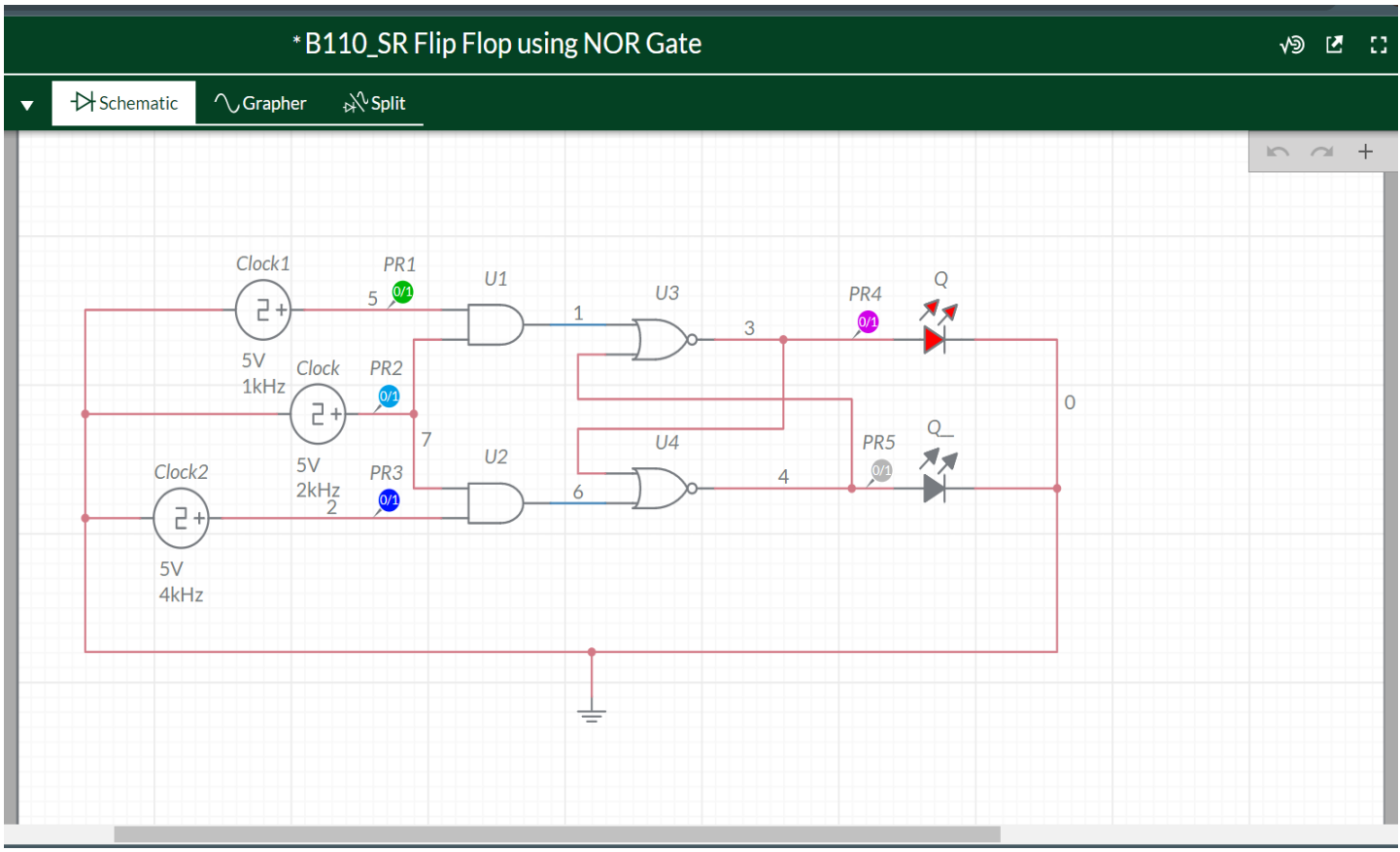


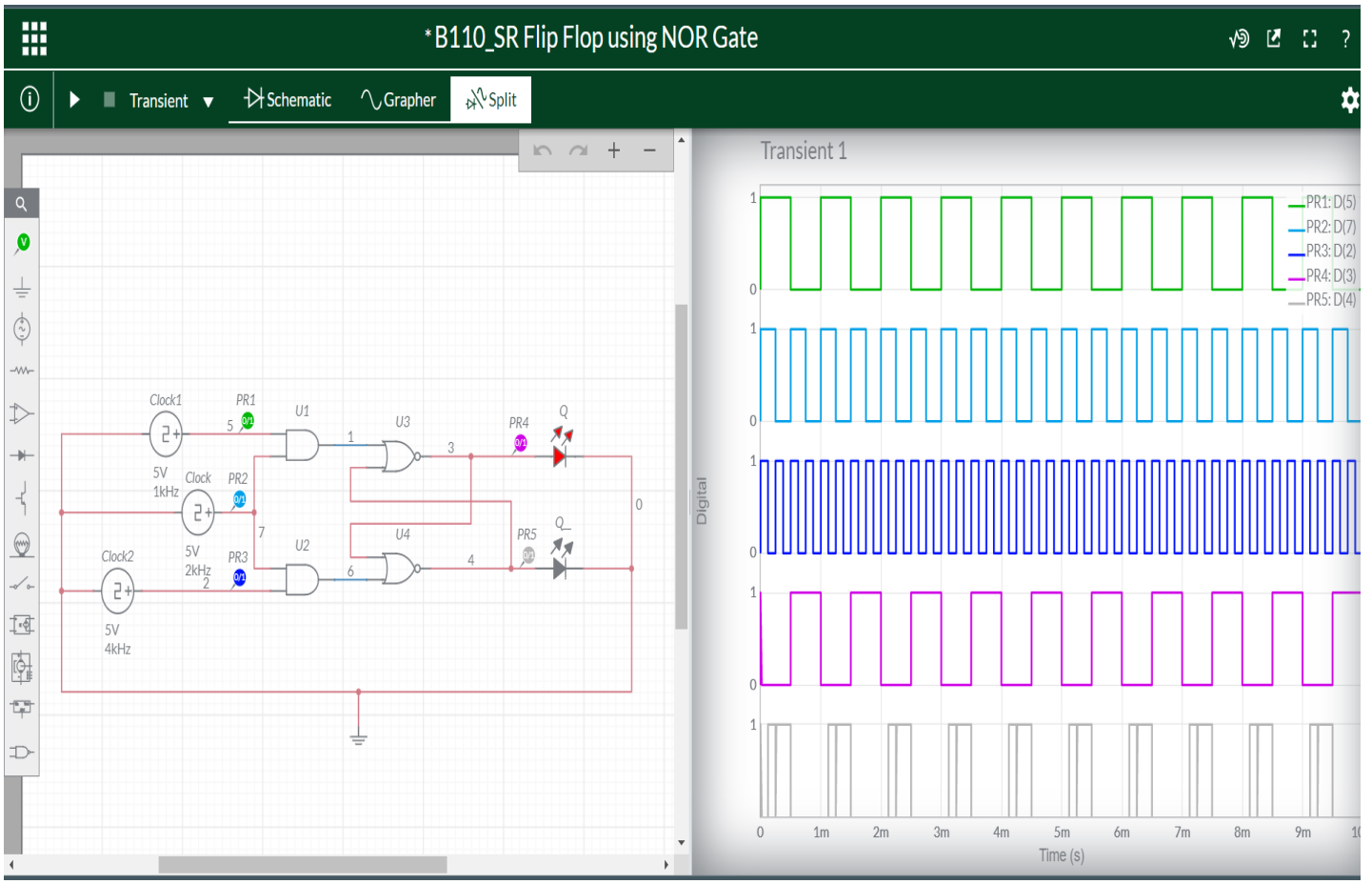
JK FLIP-FLOP USING NAND GATE CIRCUIT :-



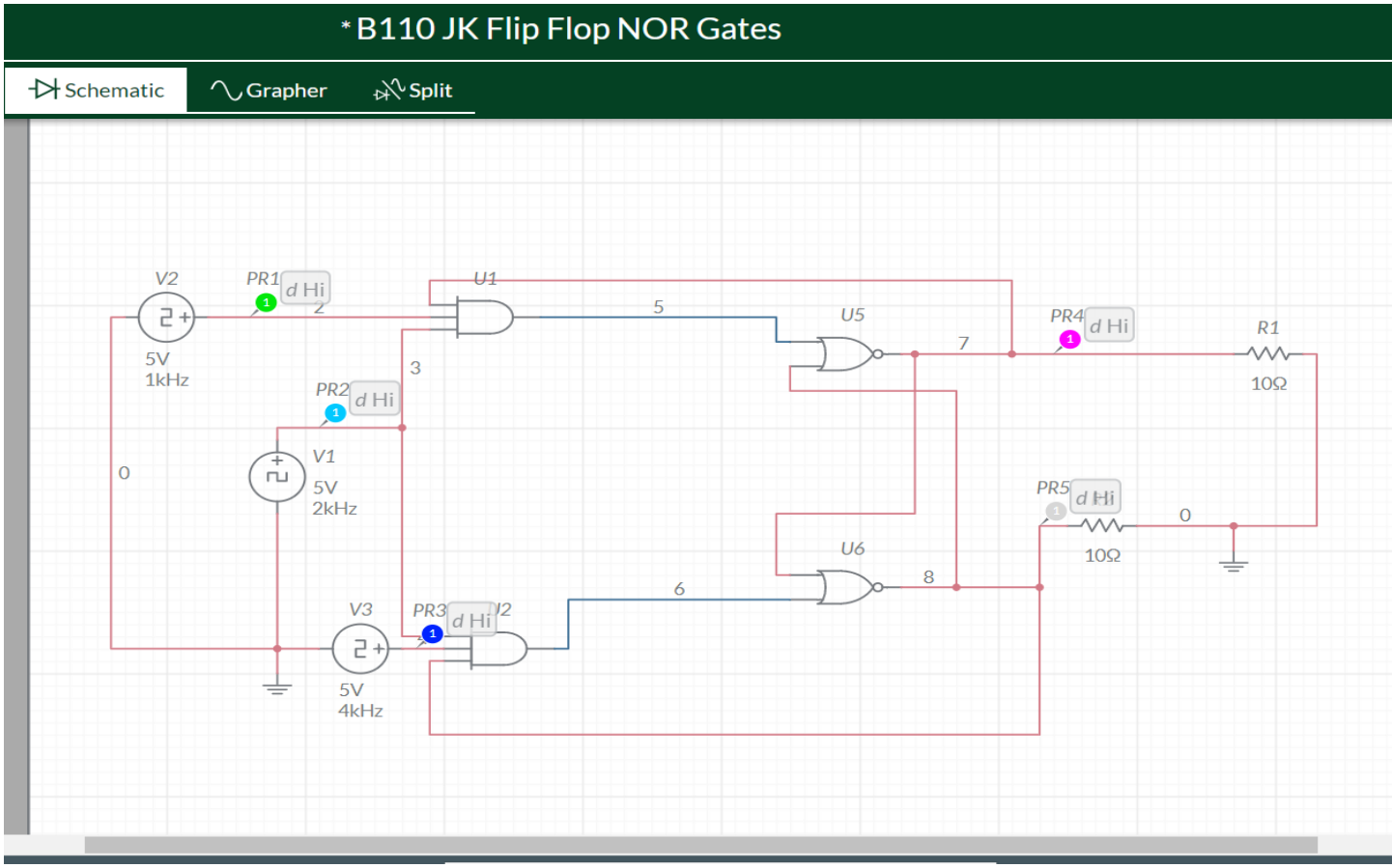


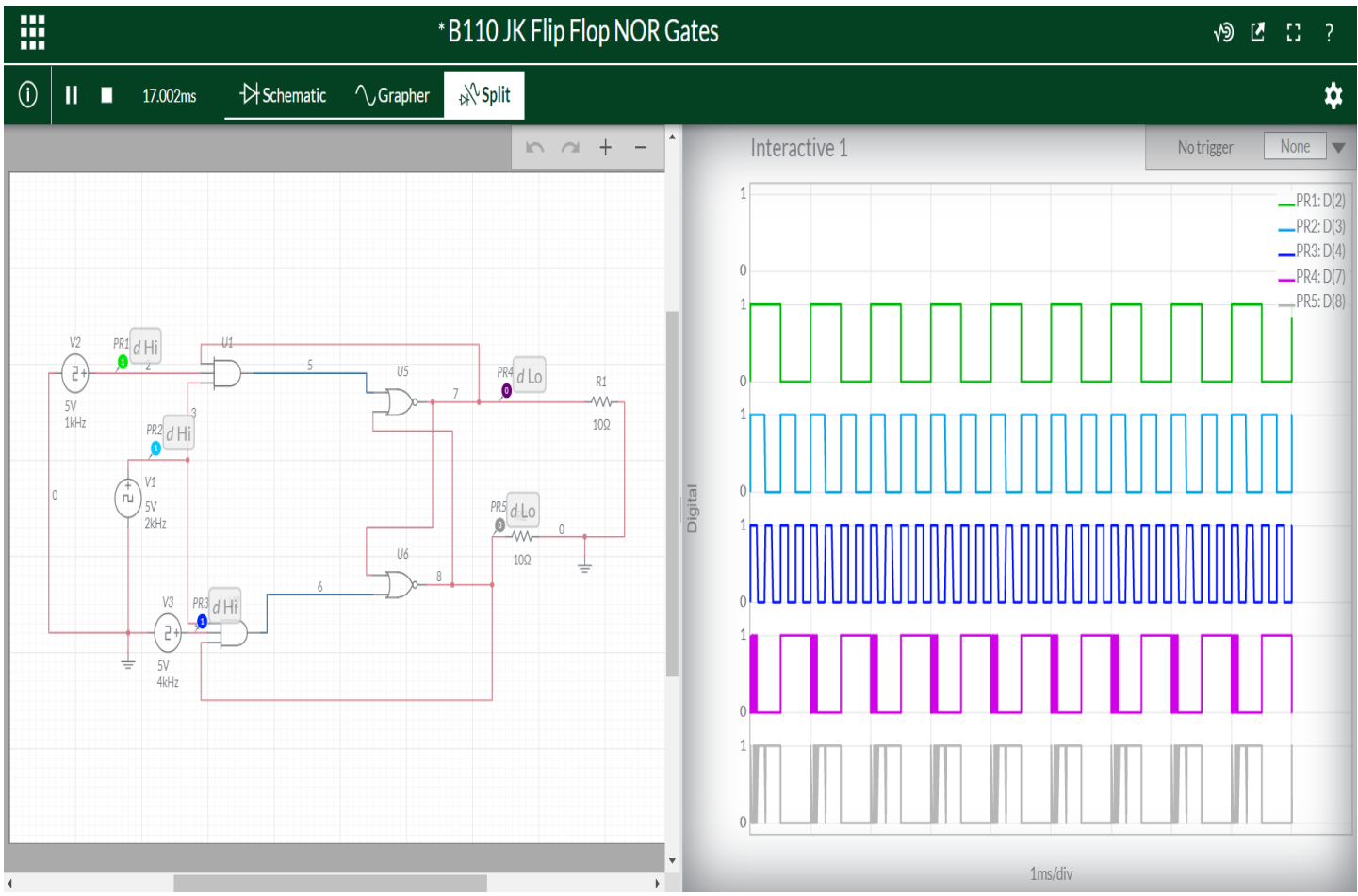
SR FLIP-FLOP USING NOR GATE CIRCUIT :-





JK FLIP-FLOP USING NOR GATE CIRCUIT :-





• CONCLUSIONS :-

The Truth Table In Theory and Simulation of SR and JK Flip Flop with NAND and NOR gate using Multi Sim Live are equal .Hence Verified….