MIT (CS-202) TUTORIAL-QUIZ-22-04-2022

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* Required

Untitled Section

*

```
LXI SP,8007H
XRA A
CPI 0AH
RC
INR C
ADD B
STAX B
MVI B,FFH
STA 9000H
HLT
```

The value stored at the location 9000H after execution of the above 8085 program is:

(a) 00H
(b) FFH
(c) 0AH
(d) 90H

- [ ] A
- [x] B
- [ ] C
- [ ] D

*

Match the following:

Column I	*Column II*
(a) POP	(i) to save data in the strack
(b) PUSH	(ii) to read data from stack
(c) STACK	(iii) a portion of memory reserved for return address and data
(d) MASK	(iv) a byte used with an ANI instruction to blank out certain bits

(a) a -i, b-ii, c-iii, d- iv
(b) a -iv, b-iii, c-ii, d- i
(c) a -ii, b-i, c-iii, d- iv
(d) a -iii, b-i, c-ii, d- iv
(e) none of the above

- ○ A
- ○ B
- ◉ C
- ○ D
- ○ E

*

For 8086, which of the following signals indicates a/an upper 8-bit data transfer?
(a) A0 = 0 and BHE=0
(b) A0 = 1 and BHE=1
(c) A0 = 0 and BHE=1
(d) A0 = 1 and BHE=0

- ○ A
- ○ B
- ○ C
- ◉ D

*

Let the content of different registers in 8086 be as follows: DS=1000H, SS=2000H, CS=3000H, BX=4000H, SI=5000H, DI= 6000H and BP=7000H. Find the memory address/addresses from where the 8086 accesses the data while executing MOV BX,[BP+DI+5] instruction

(a) 1D005H and 1D006H
(b) 2D005H and 2D006H
(c) 3D005H and 3D006H
(d) 33005H and 33006H

- ○ A
- ○ B
- ○ C
- ○ D

*

The interrupt not disabled by 8085 DI instruction is
(a) TRAP (b) RST 7.5 (c) RST 6.5 (d) RST 5.5 (e) INTR (f) none of the above

- ◉ A
- ○ B
- ○ C
- ○ D
- ○ E
- ○ F

*

In 8085, RLC instruction is equivalent to
(a) STC
(b) CMC
(c) DAD H
(d) ADC C
(e) none of the above

- A
- B
- C
- D
- E

*

The 8085 microprocessor enters into bus idle machine cycle whenever
(a) INTR interrupt is recognized
(b) RST x.5 is recognised
(c) DAD rp instruction is executed
(d) b and c
(e) a and c

- A
- B
- C
- D
- E

*

If the crystal frequency is 5MHz, then the clock frequency of 8085 microprocessor is
(a) 5 MHz (b) 10 MHz (c) 2.5 MHZ (d) 3.54 MHZ

- A
- B
- C
- D

*

The mnemonic for the shift instruction which shifts A towards right once and retains the most significant bit to be same as before is
(a) SAL A,1 (b) SHL A,1 (c) SAR A, 1 (d) SHR A, 1

- A
- B
- C
- D

*

Let the contents of AL, DL registers be 31H, 37H respectively. After executing the 8086 instruction SUB AL,DL and AAS ,the content of AL register is
(a) FAH (b) 68H (c) 37H (d) 07H (e) 06H

- A
- B
- C
- D
- E

*

The most relevant addressing mode to write position independent code is
(a) direct mode
(b) indirect mode
(c) relative mode
(d) indexed mode

- A
- B
- C
- D

*

Let the content of different registers in 8086 be as follows: DS=1000H, SS=2000H, ES=3000H, BX=4000H, SI=5000H, DI= 6000H and BP=7000H. Find the memory address/addresses from where the 8086 accesses the data while executing the (i) MOV BX,[SI-5] is
(a) 14995H (b) 4FFBH (c) 49995H (D) 14FFBH

- A
- B
- C
- D

*

Give content of A register after executing following 8085 microprocessor:

MVI A,55h
MVI C,25h
ADD C
DAA

(a) 7AH
(b) 80H
(c) 50H
(d) 22H

- A
- B
- C
- D

*

_____ generate interrupt signal to microprocessor and receive acknowledge
(a) priority resolver
(b) arithmetic unit
(c) control logic
(d) interrupt request register
(e) interrupt register

- A
- B
- C
- D
- E

*

In 8085, Interrupt caused by RST 5 is called _____ interrupt.
(a) nonmaskable (b) software (c) hardware (d) priority (e) none of these

- A
- B
- C
- D
- E

*

Before the execution of the instruction LHLD 2200H, the contents of H register, L registers and locations 2200H and 2201H were 23, 26, 45, and 85 respectively. After the execution of the instruction LHLD 2200H, the contents of the locations 2200H and 2201H are
(a) 85,45 (b) 45,85 (c) 22,00 (d) 00,22 (e) 23,26

- A
- B
- C
- D
- E

*

In 8086 the overflow flag is set when
(a) The sum is more than 16 bits
(b) Signed numbers go out of their range after an arithmetic operation
(c) Carry and sign flags are set
(d) During subtraction

- A
- B
- C
- D

*

What is the output of the following 8086 code:
AX = 37D7H, BH = 151 decimal , DIV BH
(a) AL = 65H, AH= 94 decimal (b) AL= 5EH, AH= 101 decimal
(c) AH= E5H, AL= 5EH (d) AL= 56H, AH= 5EH

- A
- B
- C
- D

*

MVI B,00
MVI A, 1CH
DCR B
DAA
STA TEMP
HLT

The content of TEMP location after the execution of the above 8085 program is:
(a) 1CH
(b) 22H
(c) 82H
(d) 12H

- A
- B
- C
- D

*

From the following select the incorrect:
for a microprocessor system using I/O mapped I/O
(a) memory space available is greater
(b) not all data transfer instructions are available
(c) I/O and memory address spaces are distinct
(d) I/O address is greater

- A
- B
- C
- D

*

Consider following 8085 program:

```
LXI H, 0106H
DCR L
LOOP: DCX H
JNZ LOOP
HLT
```

LOOP will be executed
(a) 105 times
(b) 0 times
(c) 261 times
(d) infinite
(e) can't say

- A
- B
- C
- D
- E

*

The HLT instruction of 8085 has the following characteristics
(a) After executing this instruction the value of PC is frozen (b) the CPU can come out of the halt state only after an interrupt or reset occurs (c) the program stored after the HLT instruction will be executed after the HLT state is quit

- A
- B
- C

*

The content of the A register, after executing the following three sequences of 8085 instructions
(1) XRA A (2) MVI A,4FH (3) DAA, is
(a) 50H (b) 4FH (c) 55H (d) 45H

- A
- B
- C
- D

*

for 8255, can "Bit Set Reset operation" change PC_0, if both Port A and Port B are in mode 0 and Port C lower is being used as output?
(a) BSR can change status of pin (b) BSR cannot change status of pin (c) BSR change PCO (d) None

- A
- B
- C
- D

*

The mnemonic for the rotate instruction which rotates the byte in location 0100H towards right once and transfers the least significant bit of this location to both most significant bit and carry flag is
(a) ROL [0100H], 1 (b) ROR [0100H], 1 (c) RCL [0100H], 1 (d) RCR [0100H], 1

- A
- B
- C
- D

Untitled Question *

The flags affected by 8085 double byte addition instruction are:
(a) all flags (b) all flags other than carry (c) only carry (d) none of above

- A
- B
- C
- D

*

From the following statements which are not Correct for 8086.
(a) It uses two stages of pipelining
(b) It is available in 3 versions based on the frequency of operation
(c) Fetch stage can pre-fetch up to 6 bytes of instructions
(d) It has 512 vectored interrupts.

- A
- B
- C
- D

*

Consider following 8085 instructions:
(1) PUSH PSW (2) CALL ADDR (3) XTHL (4) RST n. The stack pointer will be affected by the instruction/s
(a) 1 only
(b) 1 nad 2 only
(c) 1,2, and 4 only
(d) 1,2, and 3 only

- A
- B
- C
- D

*

The 8086 instruction, JMP 2000H:1000H; is an example of
(a) intrasegment direct mode
(b) intersegment direct mode
(c) intrasegment indirect mode
(d) intersegment indirect mode
(e) invalid jump

- A
- B
- C
- D
- E

*

When the operand required for an instruction is stored outside the MPU, the addressing mode used by the instruction is
(a) Register (b) Direct (c) Register indirect (d) Implicit (e) Immediate

- A
- B
- C
- D
- E

*

Which of the following are typical features of a RISC machine?
(a) Instruction taking multiple cycles
(b) highly pipelined
(c) instructions interpreted by microprograms
(d) multiple register sets
(e) a and c
(f) b and d

- A
- B
- C
- D
- E
- F

*

For the following requirements, ICW1 and OCW1 of 8259 will be:
vector location is 2000H, Edge triggered input, Address interval of 4 bytes, Single 8259, No ICW4. Also interrupt requests are allowed only through IR0, Ir3, Ir5, IR6.
(a) 86H, 96H
(b) 16H, 96H
(c) 1BH, 69H
(d) 16H,69H

- A
- B
- C
- D

*

Consider following 8085 program:

```
DELAY: LXI H, 0100H
LOOP: DCX H
      MOV A,L
      ORA H
      XRA A
      JNZ LOOP
      RET
```

The number of times LOOP will be executed is

(a) 16
(b) infinite
(c) 10
(d) 1

- A
- B
- C
- D

*

for 8086,assume that the DS and CS registers are initialized to be 0000H. Let the content of the location 4500H and 4501H be 25 and 35 respectively. After executing the instruction MOV CX, [4500H] , the contents of the registers CH,CL are

(a) 45H, 00H (b) 00H,45H (c) 25H, 35H (d) 35H, 25H

- A
- B
- C
- D

*

Which of the following 8086 instructions is not valid?
(a) MOV AX, BX
(b) MOV AX, 5000H
(c) MOV DS, 5000H
(d) PUSH AX

- A
- B
- C
- D

*

For the following requirements, decide the control word for 8253:
Counter 2, 8-bit count BCD placed at most significant byte, mode 3.
(a) 97H
(b) B7H
(c) B6H
(d) 96H

- A
- B
- C
- D

*

Let the content of Ah, Al, Ch registers be 00H, 03H and 08H respectively. After executing the 8086 instruction MUL Ch, the content of AX register is

(a) 0018H (b) 1800H (c) 0024H (d) 2400H (e) 0003H

- A
- B
- C
- D
- E

*

The PC contains 8452H and SP contains 88D6H. What will be the content of PC and SP following CALL to subroutine at the location 82AFH?

(a) 82AFH, 88D4H (b) 82AFH, 8450H (c) 8450H, 88D4H (d) 82AFH, 8452H

- A
- B
- C
- D

*

What is the output of the following 8086 code
AL= 00110100 BL= 00111000
ADD AL, BL
AAA
(a) AL = 6CH (b) 12H (c) 12 (d) C6H

- A
- B
- C
- D

*

After reset 8255 will be in
(a) mode 0, all ports are input
(b) mode 0, all ports are output
(c) mode 2
(d) unchanged condition
(e) can't say

- A
- B
- C
- D
- E

*

Which of the following 8086 instruction affects carry flag
(a) RCR (b) MUL (c) JZ (d) INC AX

- A
- B
- C
- D

*

When INTR is encountered, the processor branches to the memory location, which is
(a) 0024H
(b) determined by the 'call address' instruction issued by I/O device
(c) determined by the 'RST n' instruction issued by I/O device
(d) a and b
(e) b and c
(f) all of the above

- A
- B
- C
- D
- E
- F

*

The 8085 instructions which make a program ir-relocatable are
(a) Absolute JMP and CALL instruction which branch to location inside to program area being relocated (b) All CALL and JMP instructions (c) Only JMP instructions (d) The instruction which use the memory space to which the program is to be relocated as data area

- A
- B
- C
- D

*

Consider the following 8085 program
MVI A,45H
MOV B,A
NOP
MVI A,35H
ADD B
DAA
RST 1
If the 3rd ,5th instructions of the program are changed to STC and ADC B respectively, the content of A register after execution of the new program is
(a) 80H (b) 80 (c) 7A (d) 81H

- A
- B
- C
- D

*

In 8086, index register are used to hold _____

(a) memory register
(b) offset address
(c) segment memory
(d) offset memory

- A
- B
- C
- D

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