SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT
ELECTRONICS ENGINEERING DEPARTMENT

Expt. No:	2	Diode Clipper Circuits
Date:		

Name: Aarti Otari
Admission No: U20CS095

AIM: To implement various diode clamper circuits and verify its performance using Multi-Sim software.

SOFTWARE TOOLS / OTHER REQUIREMENTS:

1. Multisim Simulator/Circuit Simulator

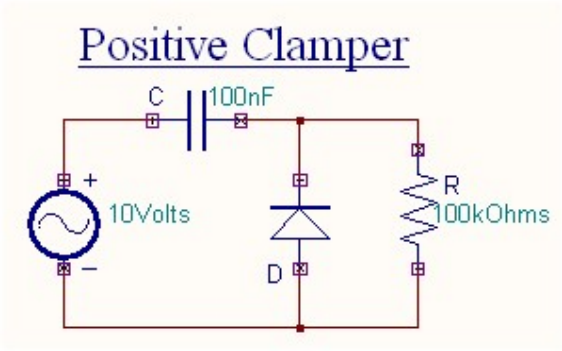
THEORY:

A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

It prevents a signal from exceeding a certain defined magnitude by shifting its DC value. The clamper does not restrict the peak-to-peak excursion of the signal, but moves it up or down by a fixed value. A diode clamp (a simple, common type) relies on a diode, which conducts electric current in only one direction; resistors and capacitors in the circuit are used to maintain an altered dc level at the clamper output. The different types of clampers are positive negative and biased clampers. A positive clamp circuit outputs a purely positive waveform from an input signal; it offsets the input signal so that all of the waveform is greater than 0 V. A negative clamp is the opposite of this - this clamp outputs a purely negative waveform from an input signal. A clamping network must have a capacitor, a diode and a resistive element. The magnitude R and C must be chosen such that the time constant RC is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non- conducting.

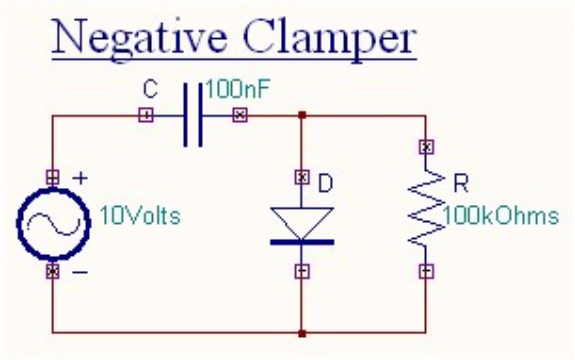
Positive Clamper

The circuit for a positive clamper is shown in the figure. During the negative half cycle of the input signal, the diode conducts and acts like a short circuit. The output voltage $V_o = 0V$. The capacitor is charged to the peak value of input voltage V_m. And it behaves like a battery. During the positive half of the input signal, the diode does not conduct and acts as an open circuit. Hence the output voltage $V_o = V_m + V_m$. This gives a positively clamped voltage.



Neagtive Clamper

During the positive half cycle the diode conducts and acts like a short circuit. The capacitor charges to peak value of input voltage V_m. During this interval the output $V_o$which is taken across the short circuit will be zero. During the negative half cycle, the diode is open.



Six type of clamper circuits are as follows:

1. POSITIVE CLAMPER

2. POSITIVE CLAMPER WITH POSITIVE VT

3. POSITIVE CLAMPER WITH NEGATIVE VT

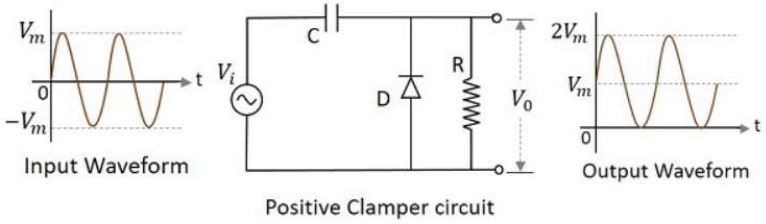
4. NEGATIVE CLAMPER

5 NEGATIVE CLAMPER WITH POSITIVE VT

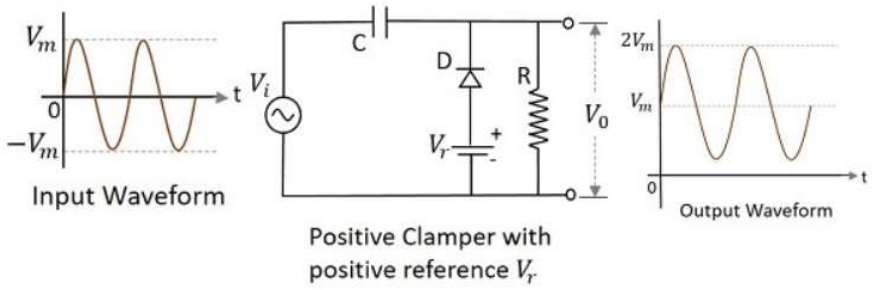
6 NEGATIVE CLAMPER WITH NEGATIVE VT

CIRCUIT DIAGRAMS:

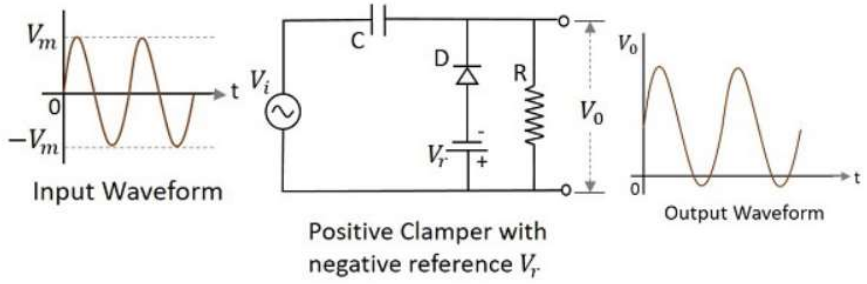
1. POSITIVE CLAMPER CIIRCUIT:



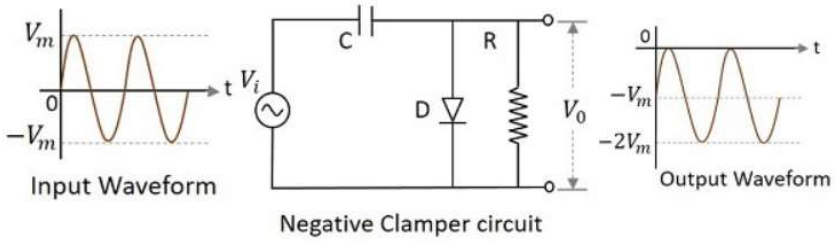
2. POSITIVE CLAMPER WITH POSITIVE VT



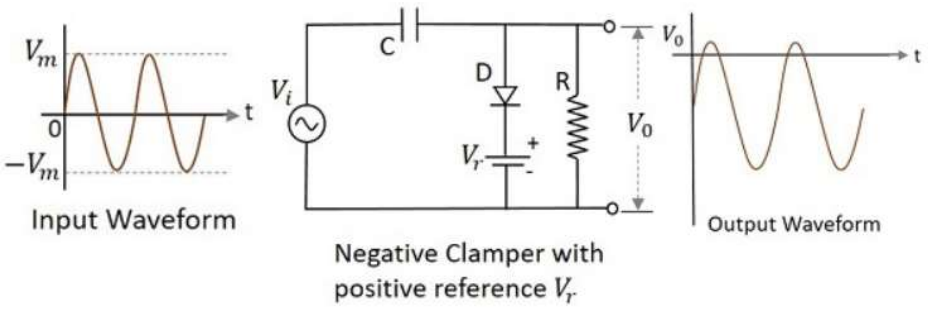
3. POSITIVE CLAMPER WITH NEGATIVE VT



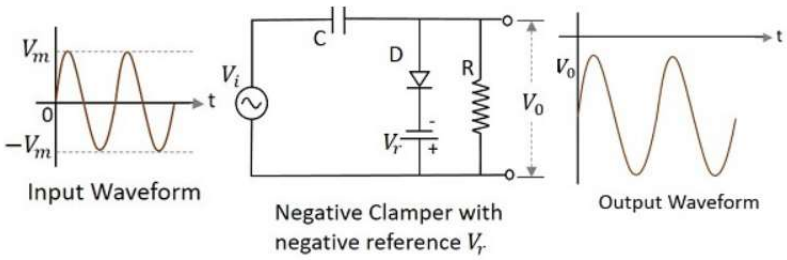
4. NEGATIVE CLAMPER



5 NEGATIVE CLAMPER WITH POSITIVE VT

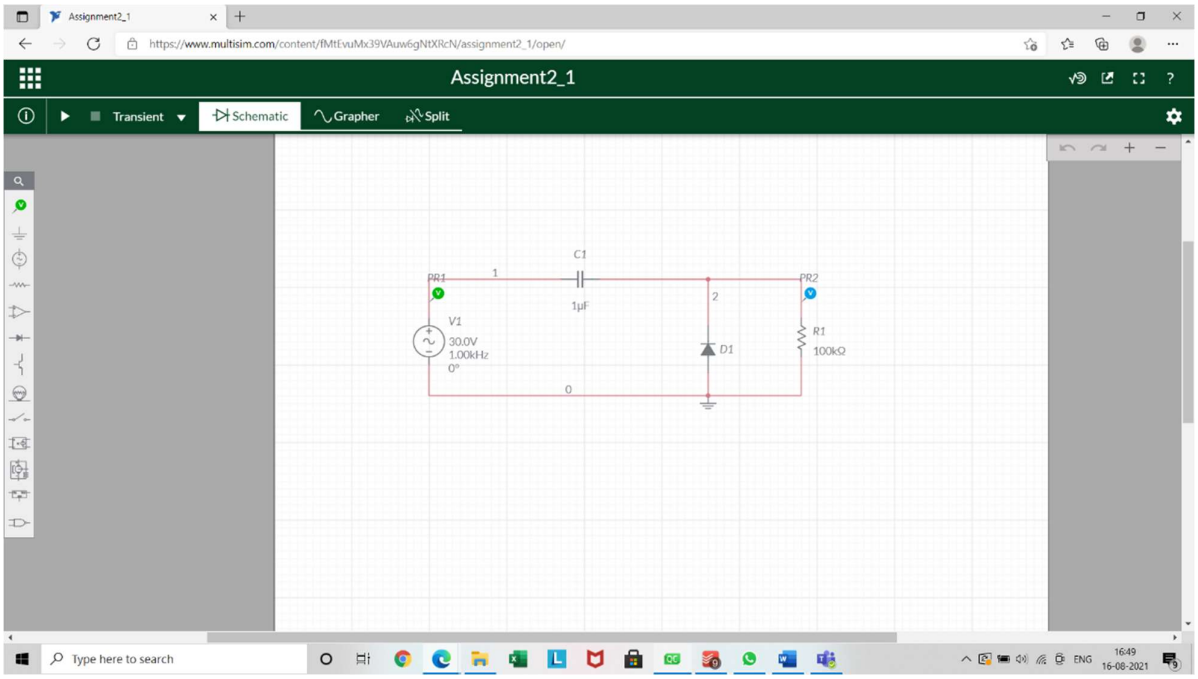


6 NEGATIVE CLAMPER WITH NEGATIVE VT

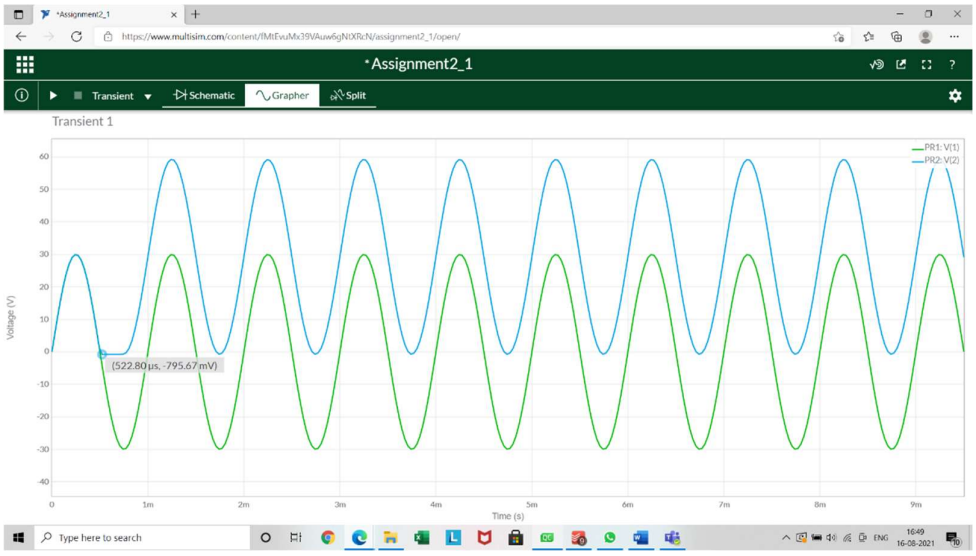


1) POSITIVE CLAMPER

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)

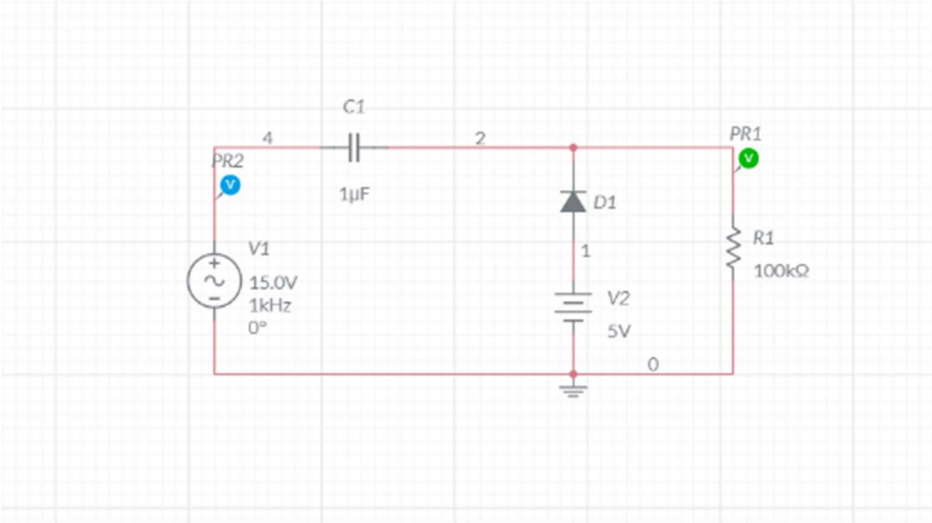


WAVEFORMS (FROM MULTISIM)

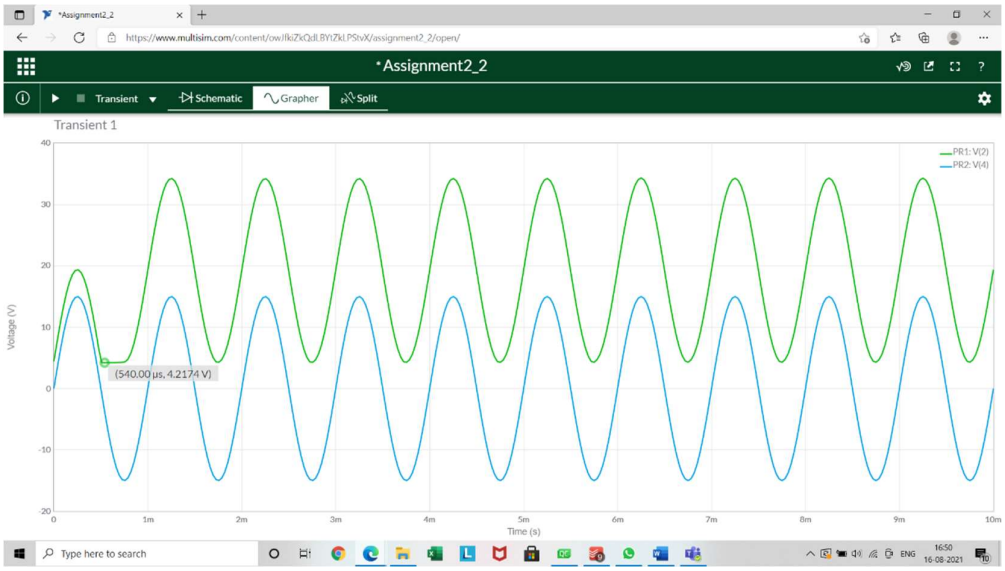


2) POSITIVE CLAMPER CIRCUIT WITH POSITIVE REFERENCE

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)

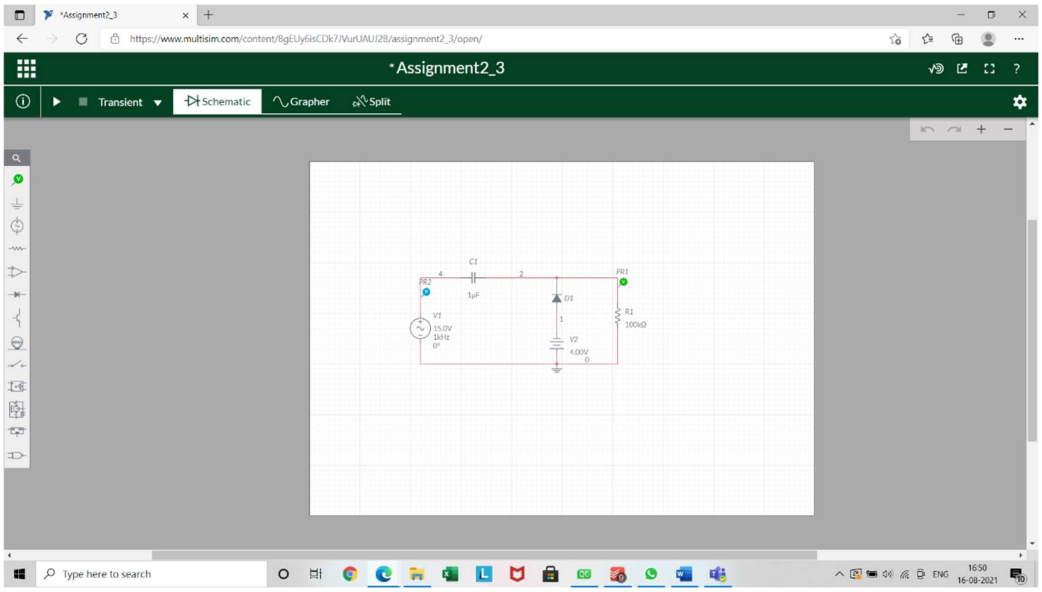


WAVEFORMS (FROM MULTISIM)

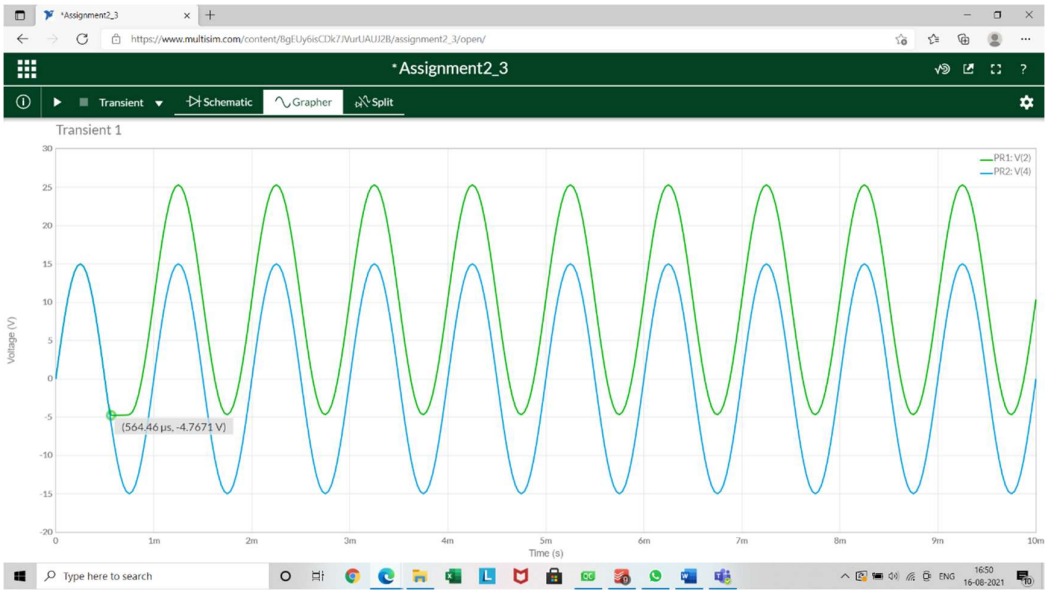


3) POSITIVE CLAMPER CIRCUIT WITH NEGATIVE REFERENCE

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)

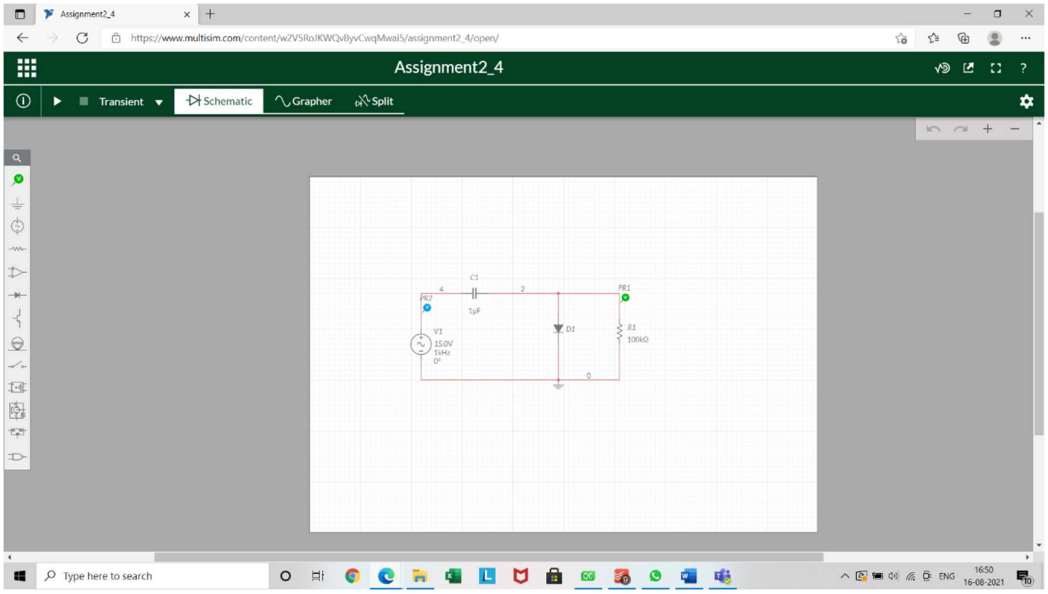


WAVEFORMS (FROM MULTISIM)

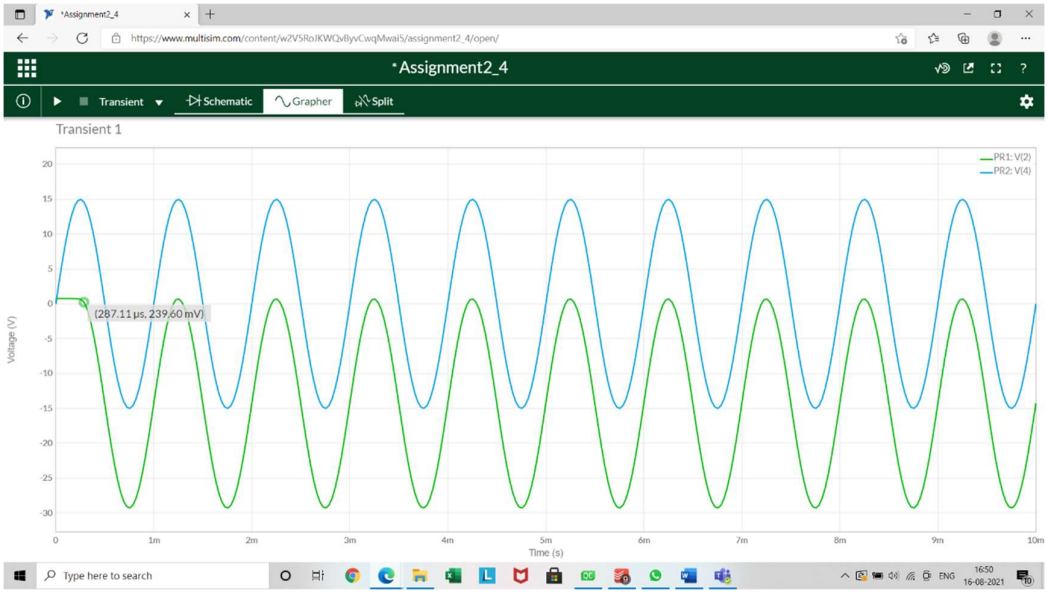


4) NEGATIVE CLAMPER

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)

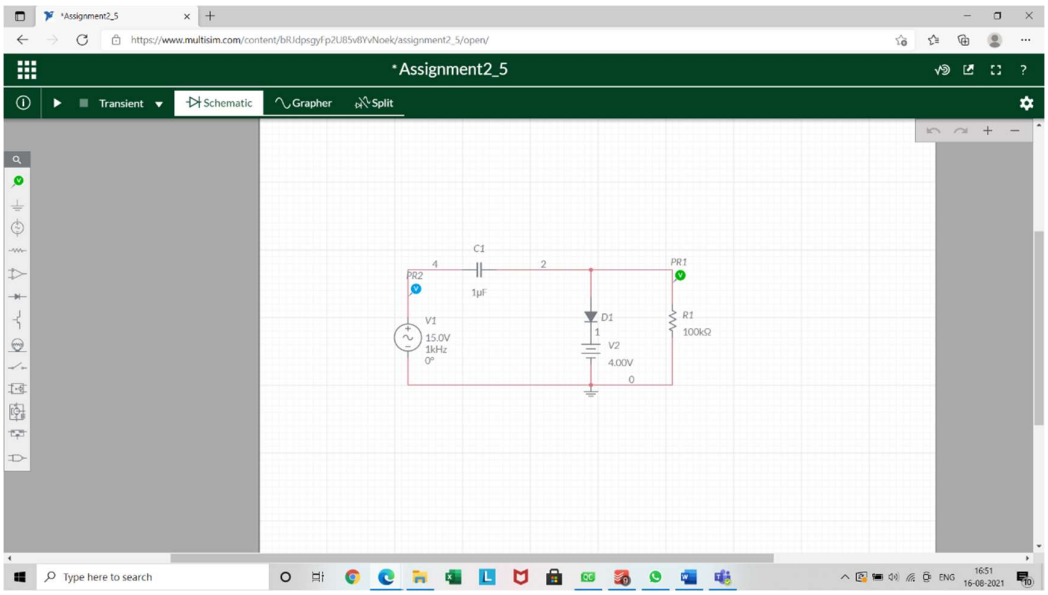


WAVEFORMS (FROM MULTISIM)

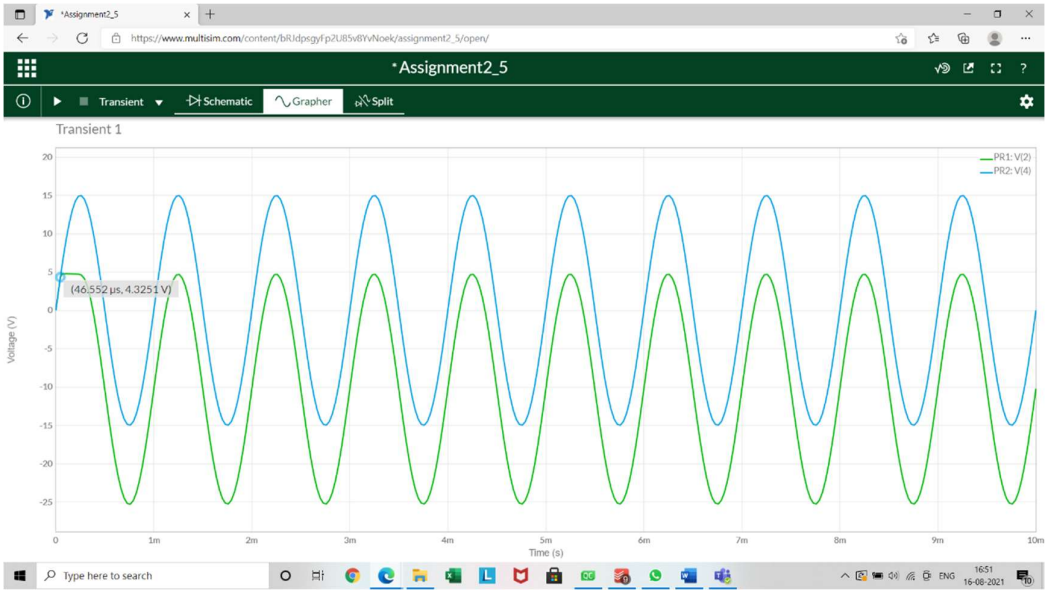


5) NEGATIVE CLAMPER CIRCUIT WITH POSITIVE REFERENCE

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)

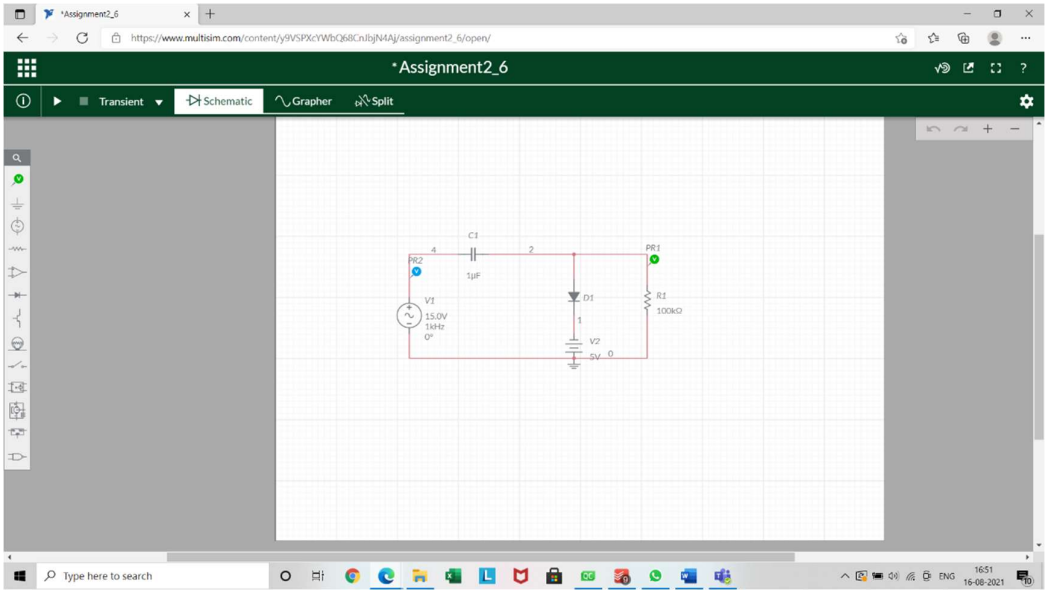


WAVEFORMS (FROM MULTISIM)

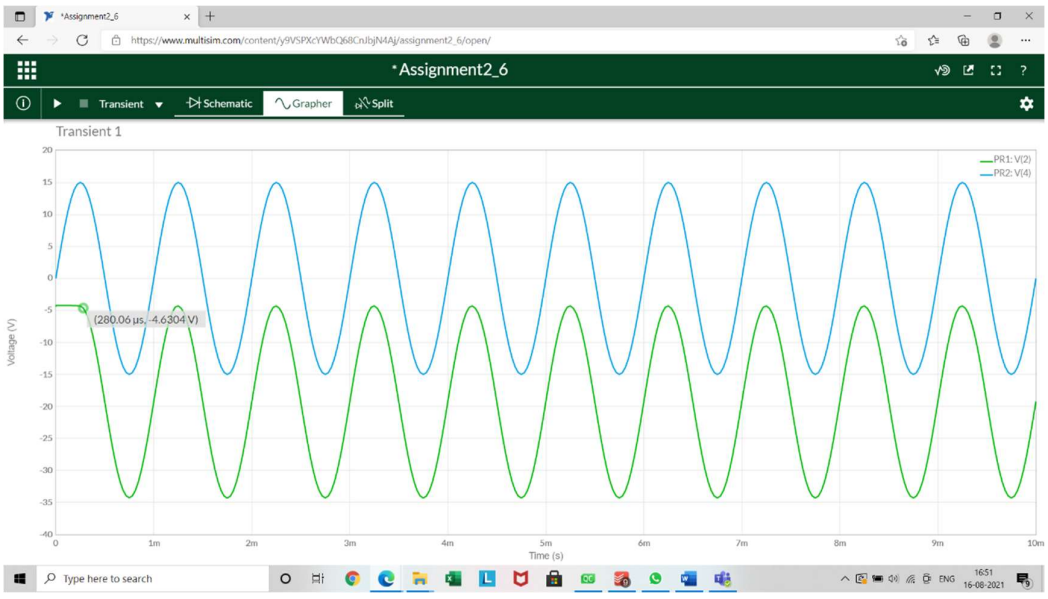


6) NEGATIVE CLAMPER CIRCUIT WITH NEGATIVE REFERENCE

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



WAVEFORMS (FROM MULTISIM)

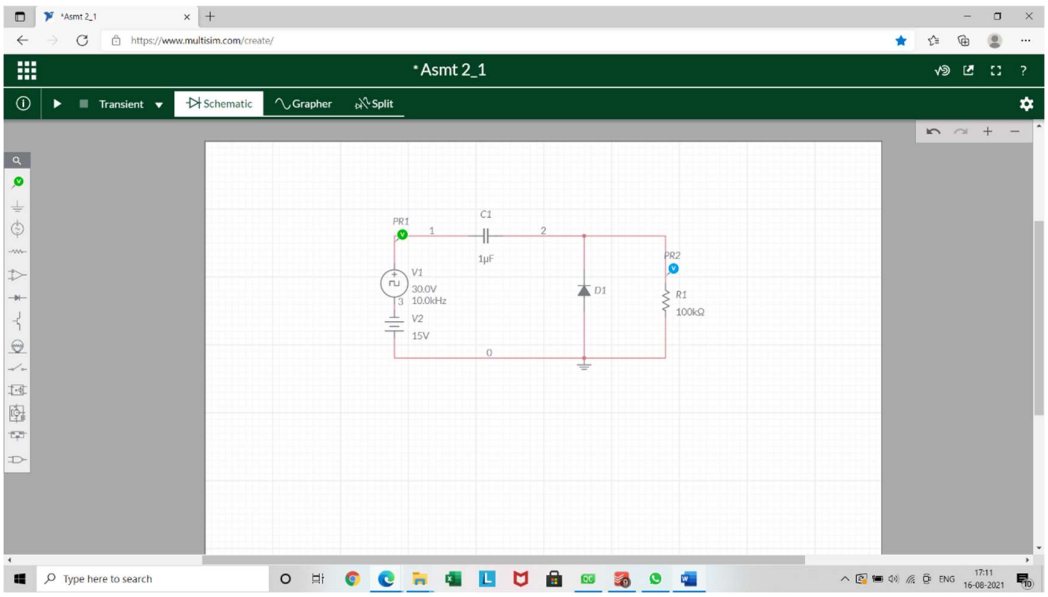


CONCLUSIONS Here, the practical and theoretical characteristics of various negative and positive clamper (with and without bias) are same. Hence verified.

ASSIGNMENT

QUESTION 1:

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



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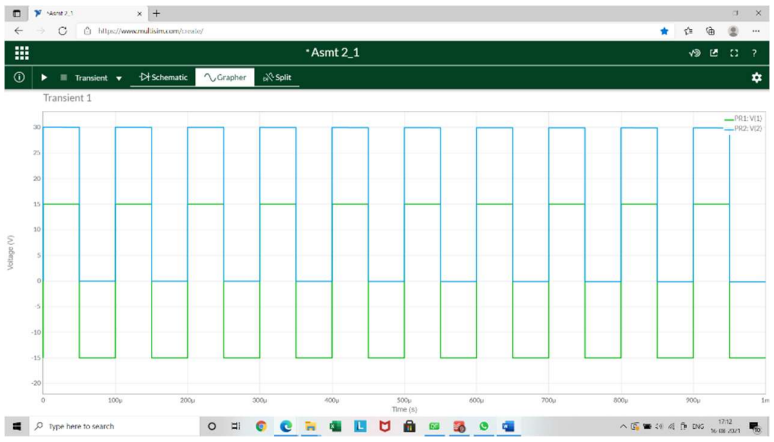
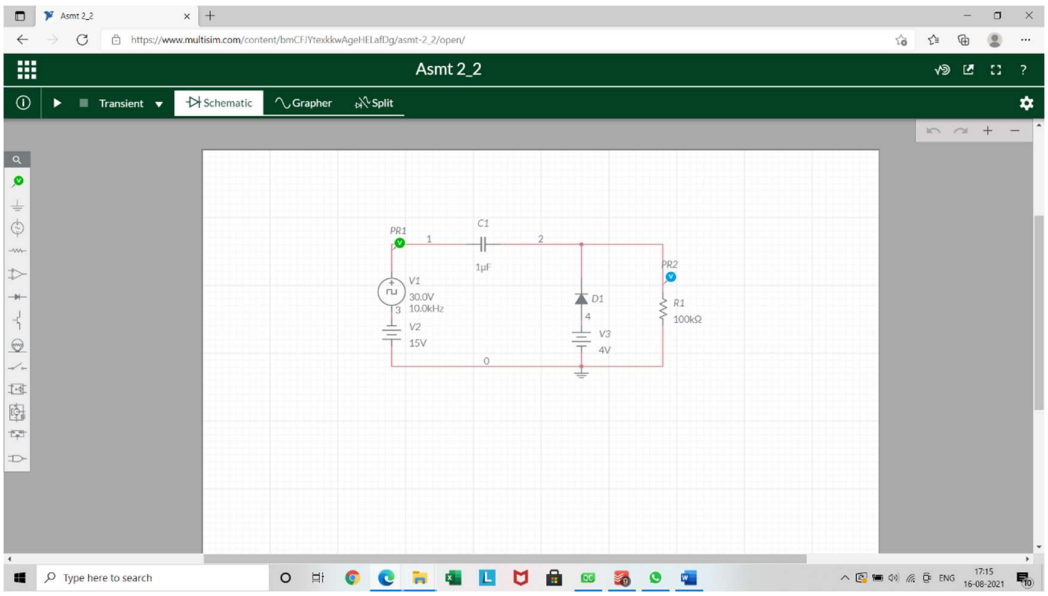
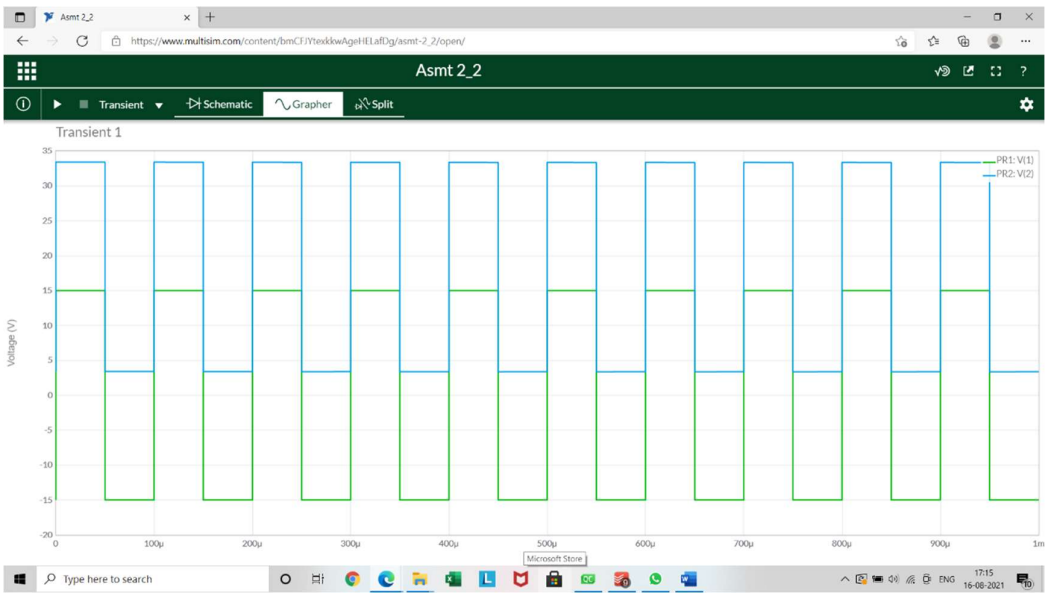


QUESTION 2:

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)

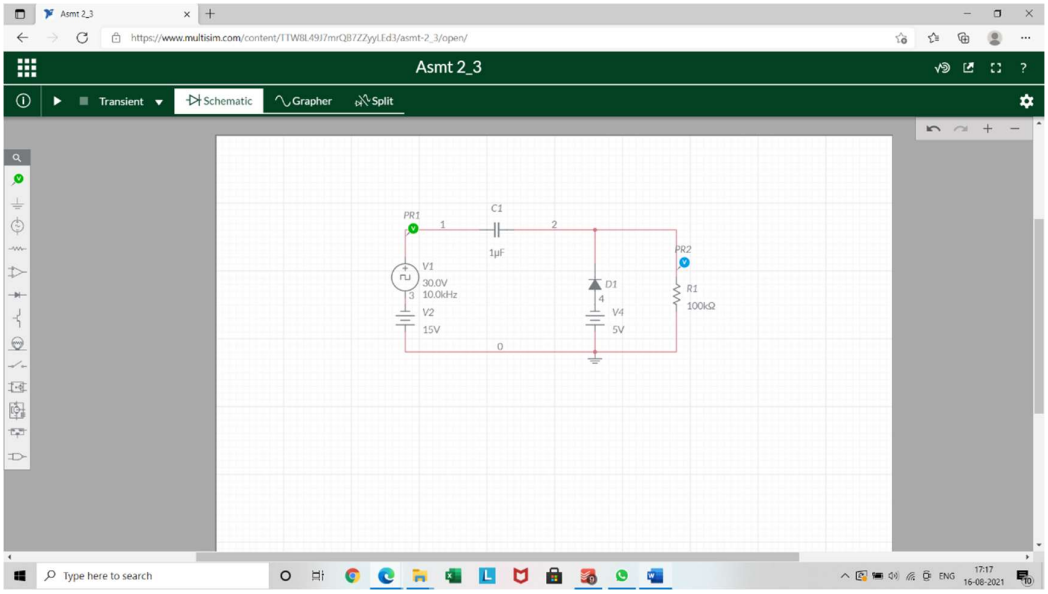


WAVEFORMS (FROM MULTISIM)



QUESTION 3:

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



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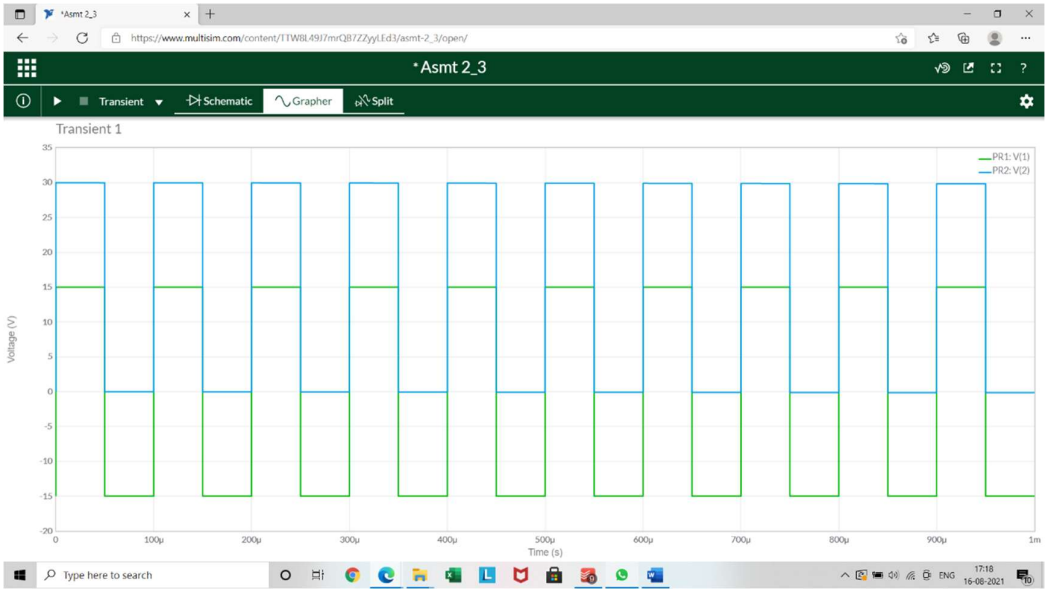
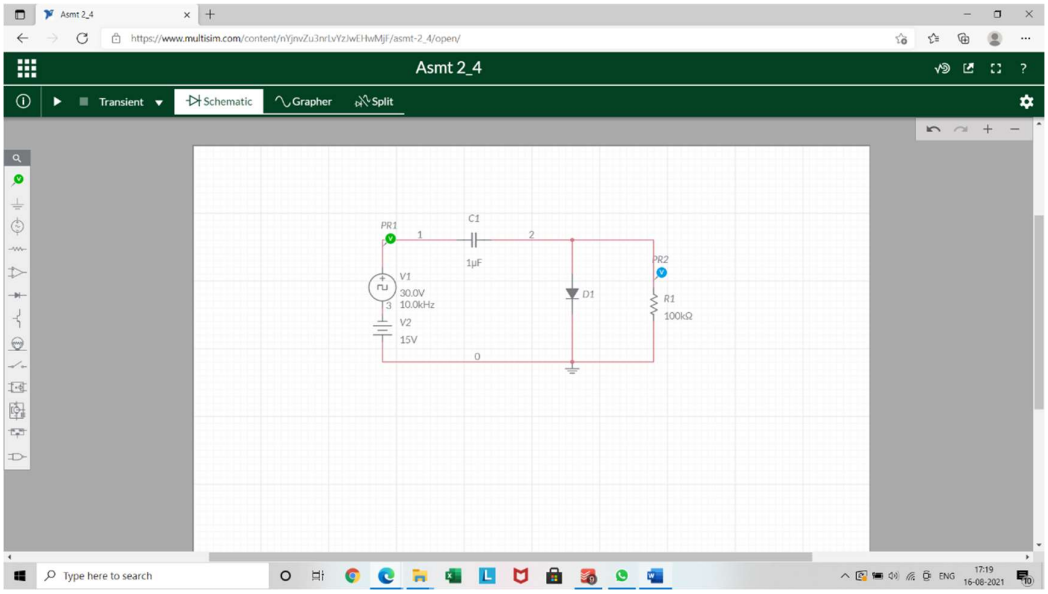
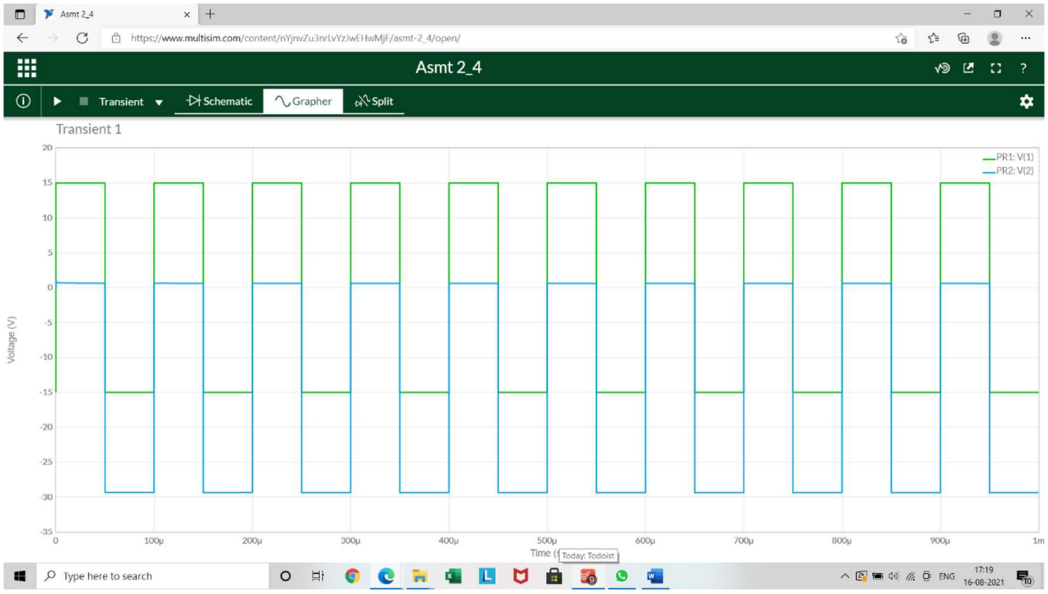


QUESTION 4:

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)

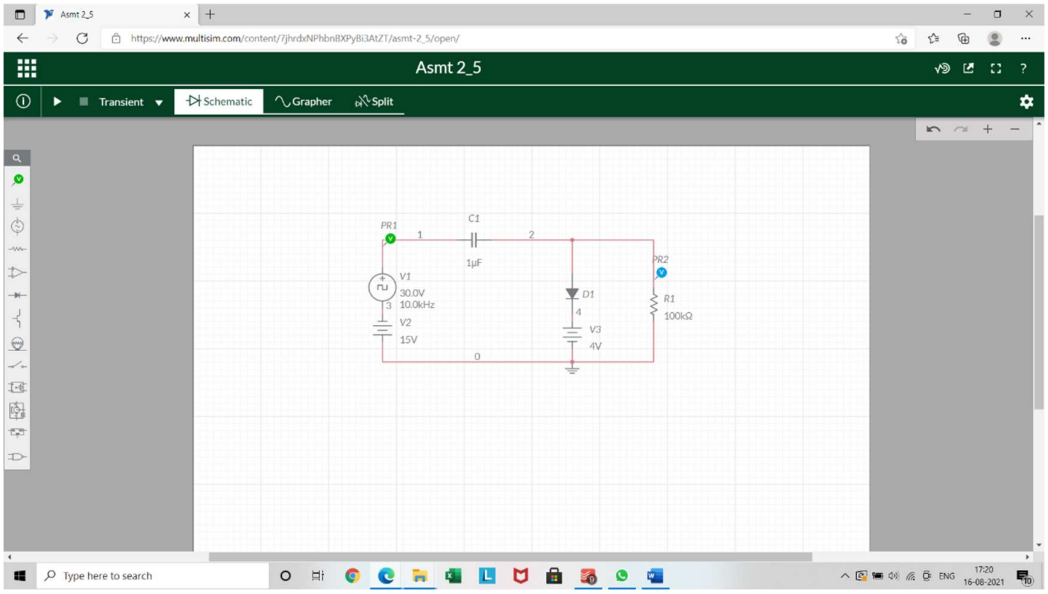


WAVEFORMS (FROM MULTISIM)



QUESTION 5:

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



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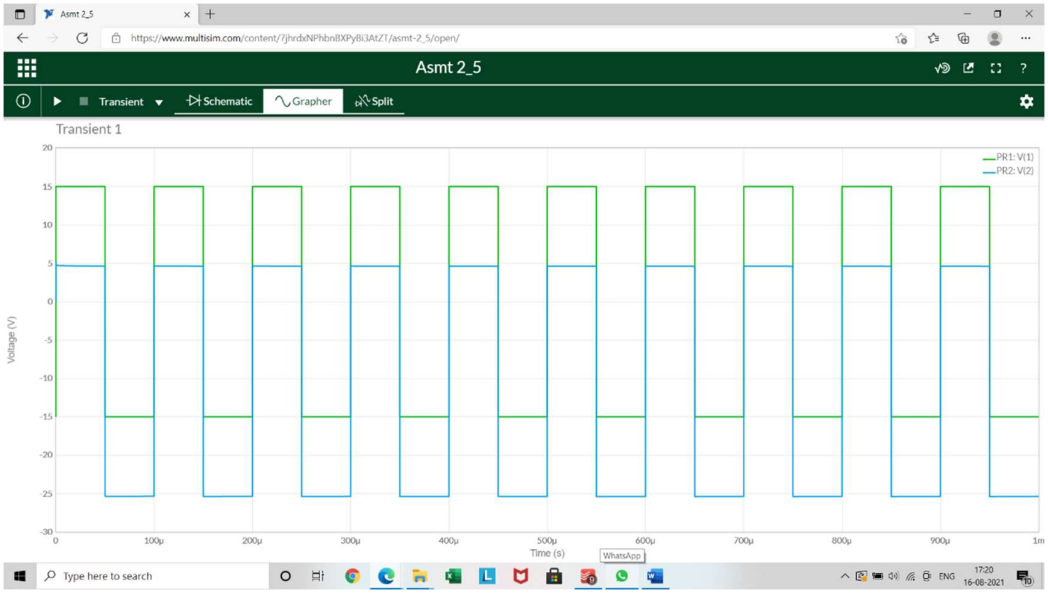
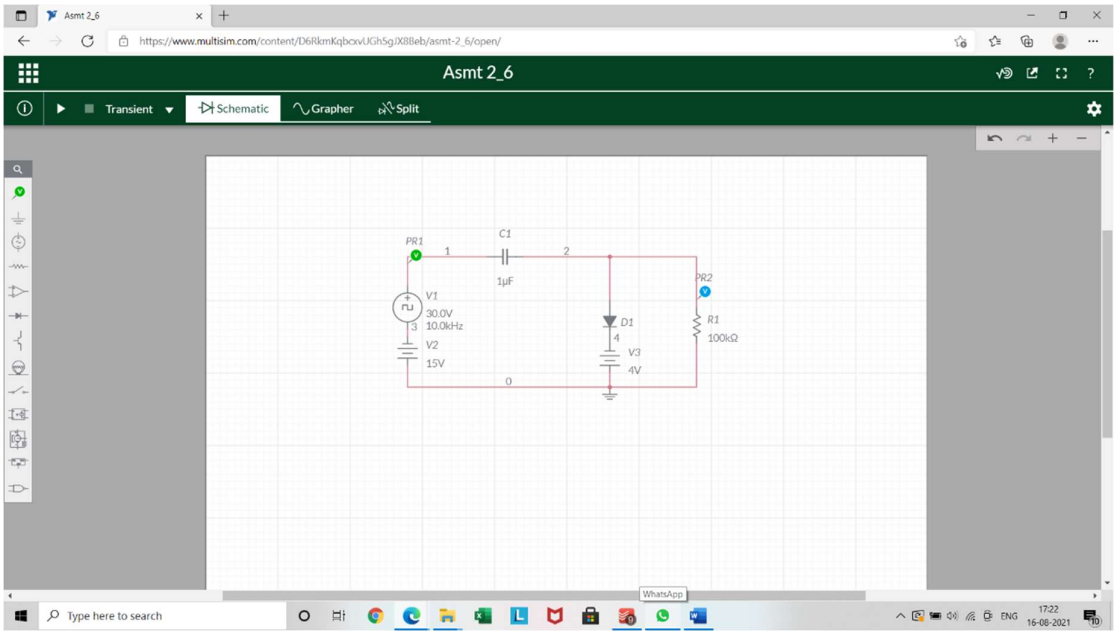


QUESTION 6:

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



WAVEFORMS (FROM MULTISIM)