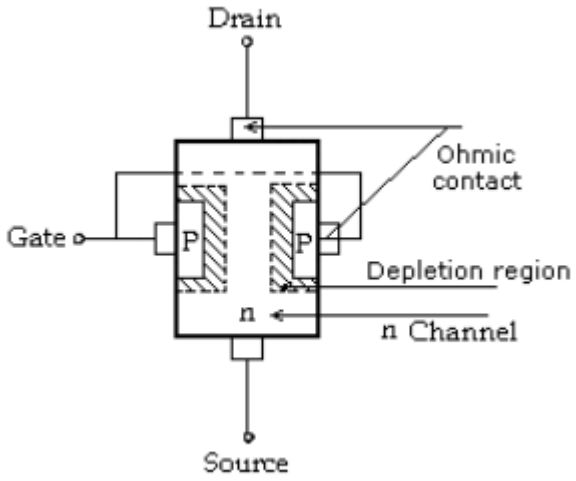
AIM: To study output and transfer characteristics of an n-channel Junction field effect Transistor (JFET) Amplifier

APPARATUS: JFET (BFW-10), Resistor (1KΩ, 100KΩ), Multisim Software.

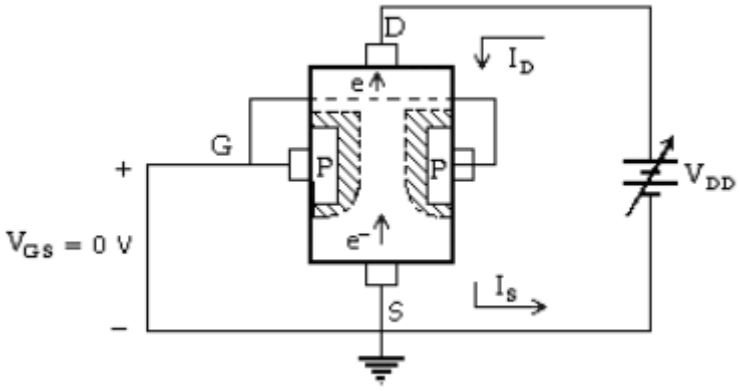
Theory:



The basic construction of n-channel FET is as shown in figure. The major part of JEET is the channel between embedded P types of material. The top of the n-channel is connected to an ohmic contact called as 'Drain' (D) & lower end of Channel is called as 'Source' (S). The two p types of materials are connected together & to the 'Gate' terminal (G).

Characteristic:-

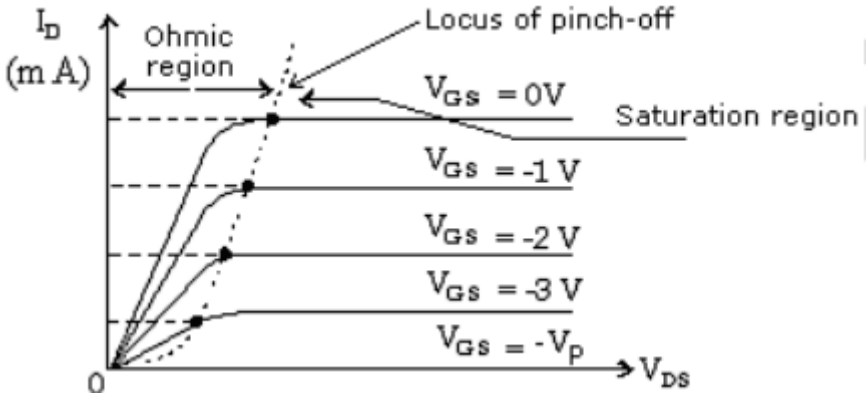
1. VGS = 0V, VDS - Some +ve Value:-



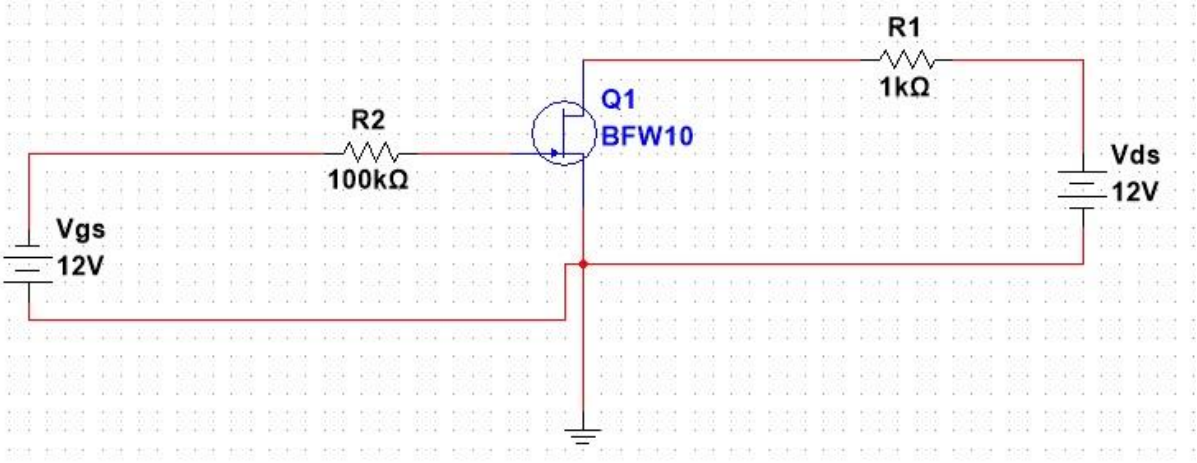
As shown in the figure the gate is directly connected to source to achieve VGS = 0V, this is similar to no bias condition. The instant the voltage VDD (=VDS) is applied, the electrons will be drawn to the drain terminal, causing ID & IS to flow (i.e. ID = IS). Under this condition the flow of charge is limited solely by resistance of the n channel between drain & source. It is important to note that the depletion region wider at the top of both p type of material. Since the upper terminal is more R .B. than the lower terminal (source - S). As voltage VDS is increased from 0 to few volts, the current will increase as determined by ohm's law. If still VDS is increased & approaches a level referred as VP, the depletion region will widen, causing a noticeable reduction in channel width. The reduced path of conduction causes the resistance to increase. The more the horizontal curve, the higher resistance. If VDS is increase to a level where it appears that the two depletion region would touch each other, the condition referred as 'pinch–off' will result. The level of VDS that establish this condition is called as 'pinch off voltage' (VP). At VP, ID should be zero, but practically a small channel still exists & very high density current still flows through the channel. As VDS is increased beyond VP, the saturation current will flow through the channel (i.e IDSS). IDSS – Drain to source current with short cut connection from source to Gate.

2. VGS < 0V:-

If a –ve bias is applied between gate and source, the effect of the applied –ve bias VGS is to establish depletion region similar to those obtained with VGS = 0V but at lower level of VDS. As VGS will become more & more –ve biased, the depletion layer pinch off occur at the less & less value of VDS. Eventually, when VGS = - VP, will be sufficiently –ve to establish a saturation level, i.e. essentially 0 mA & for all practical purpose the device has been 'turned OFF'



CIRCUIT DIAGRAM:



PROCEDURE:

OUTPUT CHARACTERISTICS:

1. Connect the circuit as per given diagram properly.
2. Keep VGS = 0V
3. Vary VDS in step of 0.5V up to 10 volts and measure the drain current ID. Tabulate all the readings.
5. Repeat the above procedure for VGS as -0.5, -1V, -1.5V, -2V.

TRANSFER CHARACTERISTICS:

1. Connect the circuit as per given diagram properly.
2. Keep VDS constant at 2V.
3. Plot the transfer characteristics VGS vs. ID.
4. Repeat the above procedure for VDS as 3, 4V.

Observation Table:

OUTPUT CHARACTERISTICS

Vgs = 0V		**Vgs = -0.5 V**		**Vgs = -1 V**		**Vgs = -1.5V ….upto 2V**	
Vds (V)	**Id (mA)**						
0							
1							
10							

Transfer Characteristics

Vds (2V)		**Vds (3V)**	**Vds (4V)**
Vgs (V)	**Id (mA)**		
0			
-0.2			
-0.4			
-2			

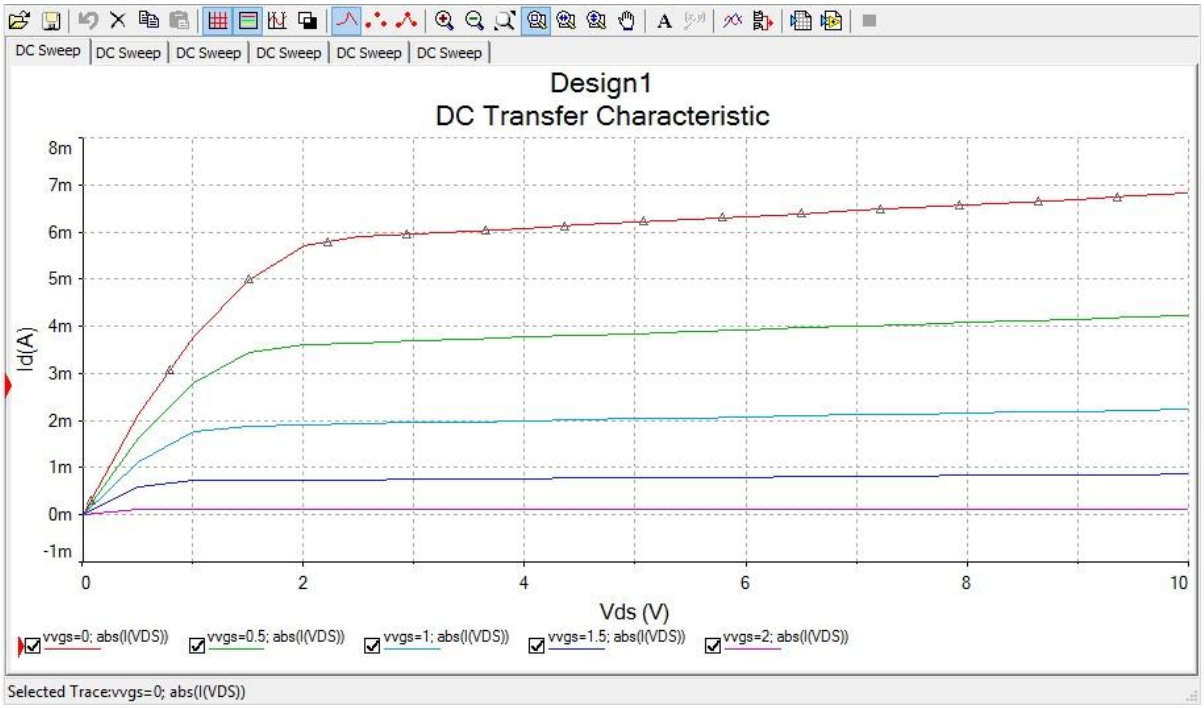
CALCULATION:

1. Transconductance gm: Ratio of small change in drain current (Δ ID) to the corresponding change in gate to source voltage (ΔVGS) for a constant VDS.
   gm = Δ ID / ΔVGS at constant VDS

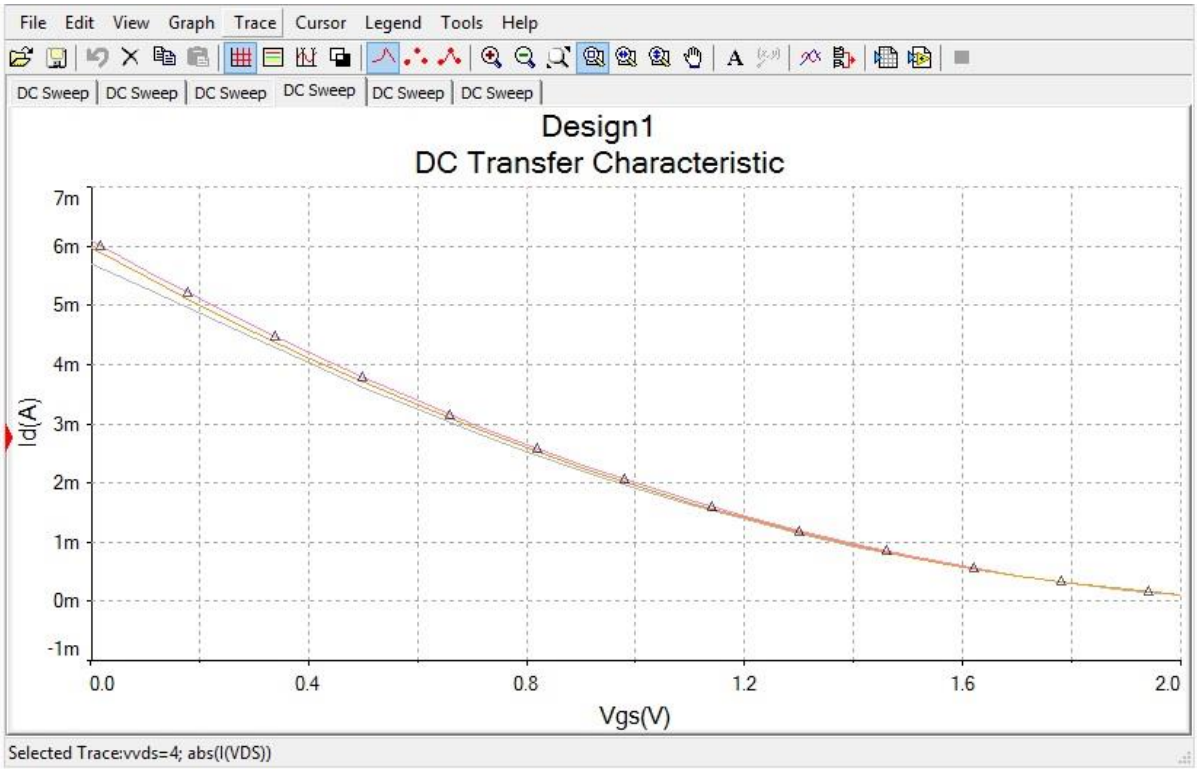
2. Output resistance: It is given by the relation of small change in drain to source voltage (Δ VDS) to the corresponding change in Drain Current (Δ ID) for a constant VGS, when the JFET is operating in pinch-off region.
   rd or ro = ΔVDS / Δ ID at a constant VGS

Result:

OUTPUT CHARACTERISTICS



TRANSFER CHARACTERISTICS



Conclusion: