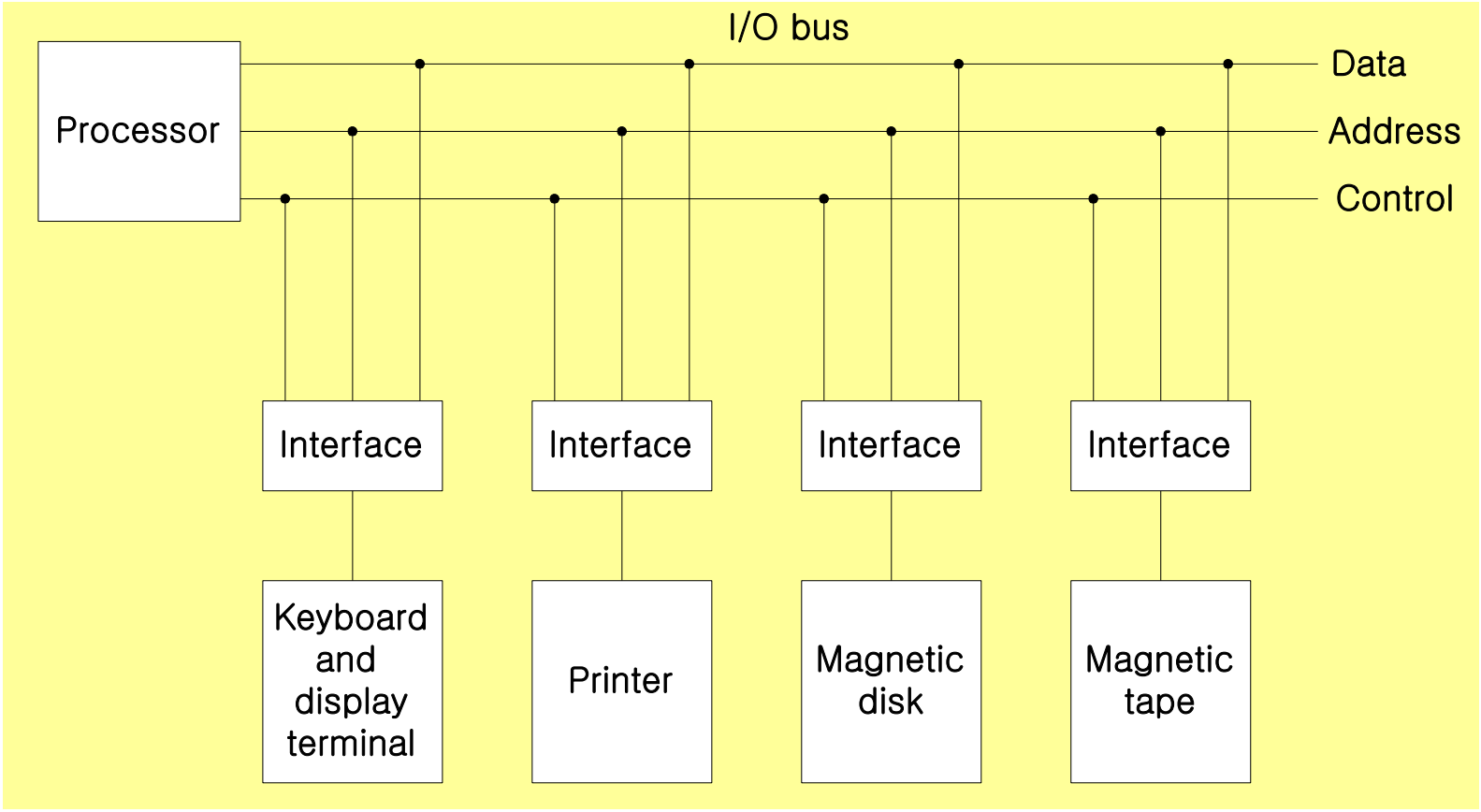
Input Output Organization

- **Peripheral Devices :**
  - I/O Subsystem
    - Provides an efficient mode of communication between the central system and the outside environment
  - Peripheral (or I/O Device)
    - Input or Output devices attached to the computer
      - Monitor (Visual Output Device) : CRT, LCD
      - KBD (Input Device) : light pen, mouse, touch screen, joy stick, digitizer
      - Printer (Hard Copy Device) : Dot matrix (impact), thermal, ink jet, laser (non-impact)
      - Storage Device : Magnetic tape, magnetic disk, optical disk

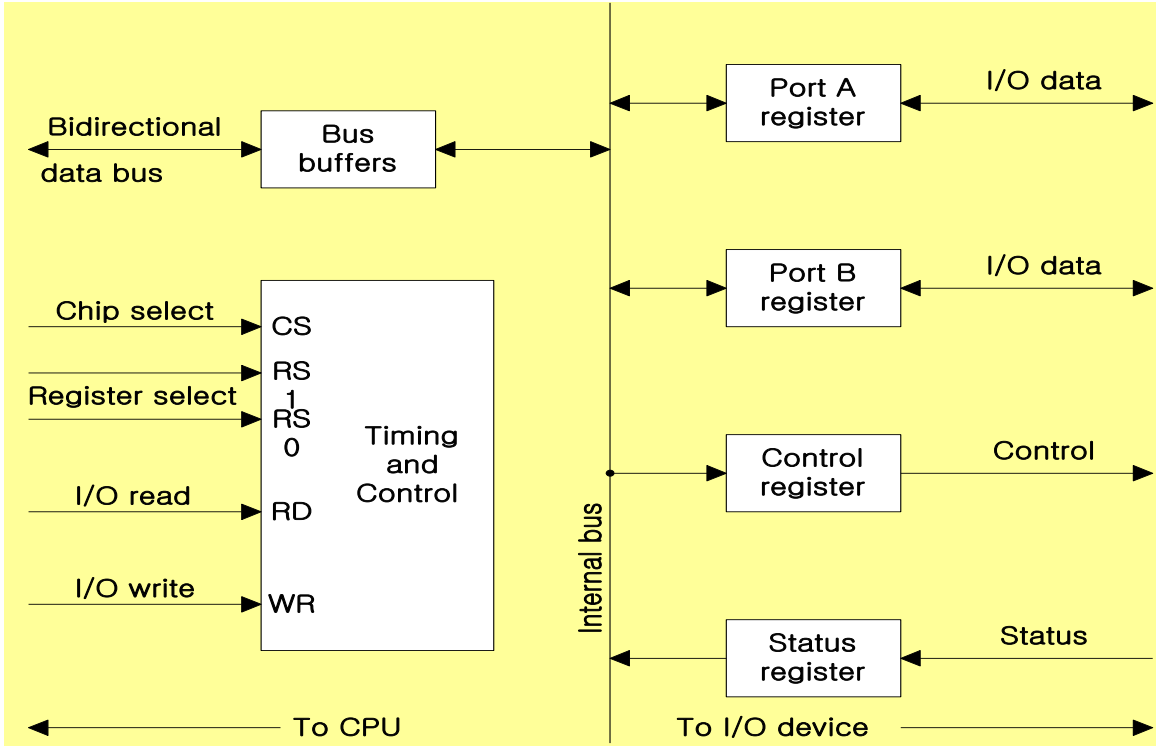
- **Input-Output Interface**
  - Provides method for transferring information between internal storage and external I/O devices.
  - Special communication link require for interfacing peripherals with CPU
  - Differences between Peripherals and CPU
    - 1) A conversion of signal values may be required
    - 2) A synchronization mechanism may be needed
      - The data transfer rate of peripherals is usually slower than the transfer rate of the CPU
    - 3) Data codes and formats in peripherals differ from the word format in the CPU and Memory
    - 4) The operating modes of peripherals are different from each other
      - Each peripherals must be controlled so as not to disturb the operation of other peripherals connected to the CPU

- Interface :
  - Special hardware components between the CPU and peripherals
  - Supervise and Synchronize all input and output transfers
- I/O Bus and Interface Modules :
  - I/O Bus
    - Data lines
    - Address lines
    - Control lines
  - I/O command :
    - Control Command
    - Status Command
    - Input Command
    - Output Command


I/O bus
Processor
Data
Address
Control
Interface
Interface
Interface
Interface
Keyboard and display terminal
Printer
Magnetic disk
Magnetic tape

- I/O Bus versus Memory Bus :
  - Computer buses can be used to communicate with memory and I/O
  - 1) Use two separate buses, one for memory and the other for I/O :
    - Computer has individual sets of data, address, and control buses
    - Done in computer which have separate I/O Processor (IOP)
  - 2) Use one common bus for both memory and I/O but have separate control lines for each : ***Isolated I/O*** or ***I/O Mapped I/O***
    - Distinction between memory transfer and I/O transfer made through separate read write lines
    - **IN**, **OUT** : I/O Instruction
    - **MOV** or **LD** : Memory read/write Instruction
    - Isolated I/O method isolate memory and I/O addresses

- 3) Use one common bus for memory and I/O with common control lines : ***Memory Mapped I/O***
  - **MOV** or **LD** : I/O and Memory read/write Instruction
  - Employ only one set of read and write signals and do not distinguish memory and I/O addresses.
  - Segment of total address space is reserved for interface register



CS	RS 1	RS 0	Register selected
0	×	×	None : data bus in high-impedance
1	0	0	Port A register
1	0	1	Port B register
1	1	0	Control register
1	1	1	Status register

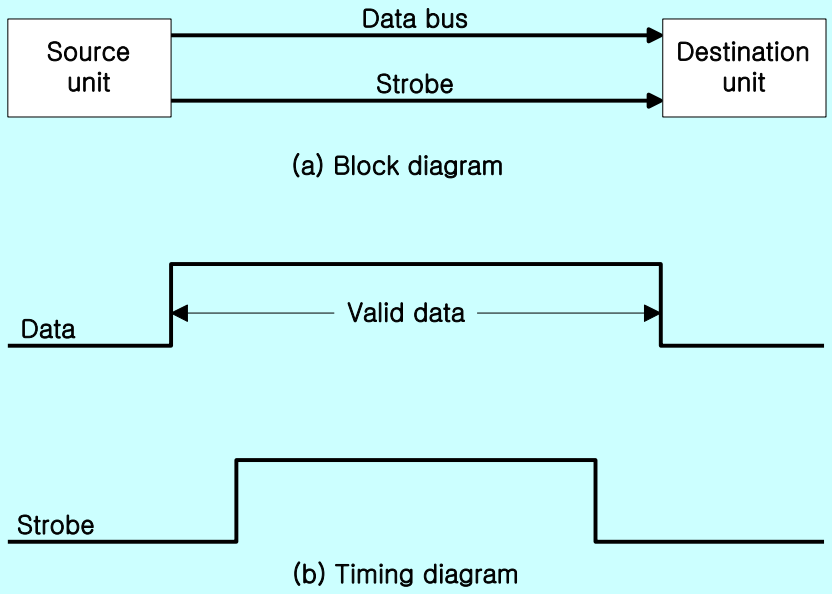
Example of I/O Interface :

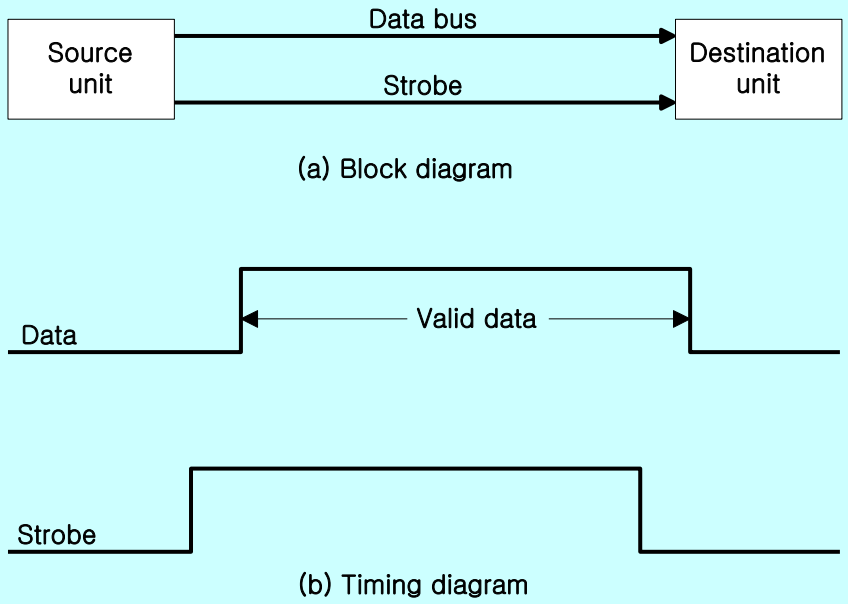
- 4 I/O port : Data port A, Data port B, Control, Status
- Address Decode : CS, RS1, RS0

- Asynchronous Data Transfer :
  - Synchronous Data Transfer
    - All data transfers occur simultaneously during the occurrence of a clock pulse
    - Registers in the **interface** share a common clock with **CPU** registers
  - Asynchronous Data Transfer
    - Internal timing in each unit (*CPU and Interface*) is independent
    - Each unit uses its own private clock for internal registers

- Strobe : Control signal to indicate the time at which data is being transmitted
  - 1) Source-initiated strobe :
  - 2) Destination-initiated strobe :

  - Disadvantage of strobe method
    - Source will never know the receipt of data at destination
    - Destination that initiate transfer has no way to know whether source has placed data on the bus



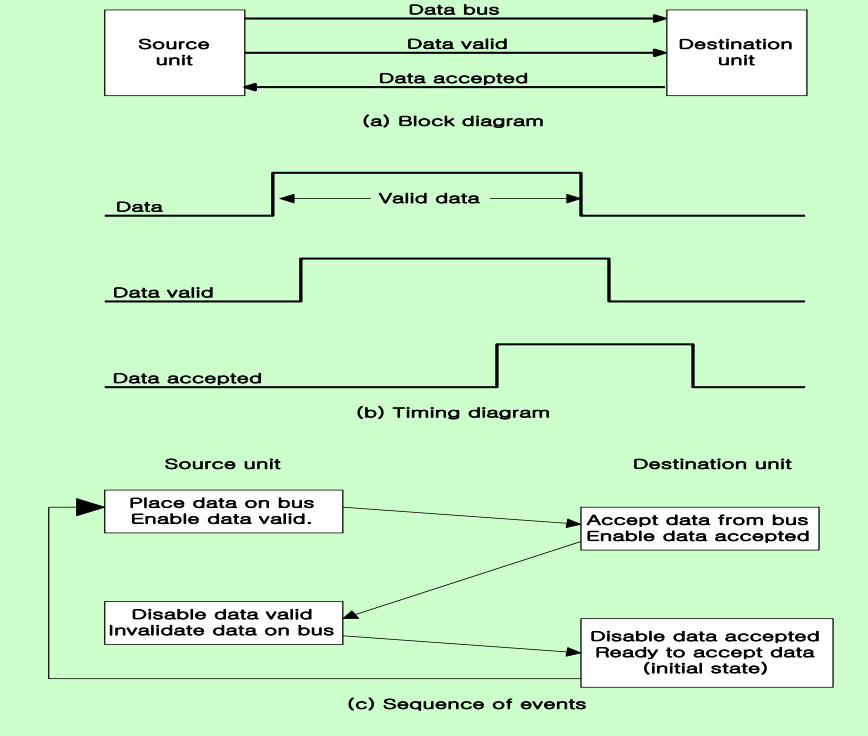


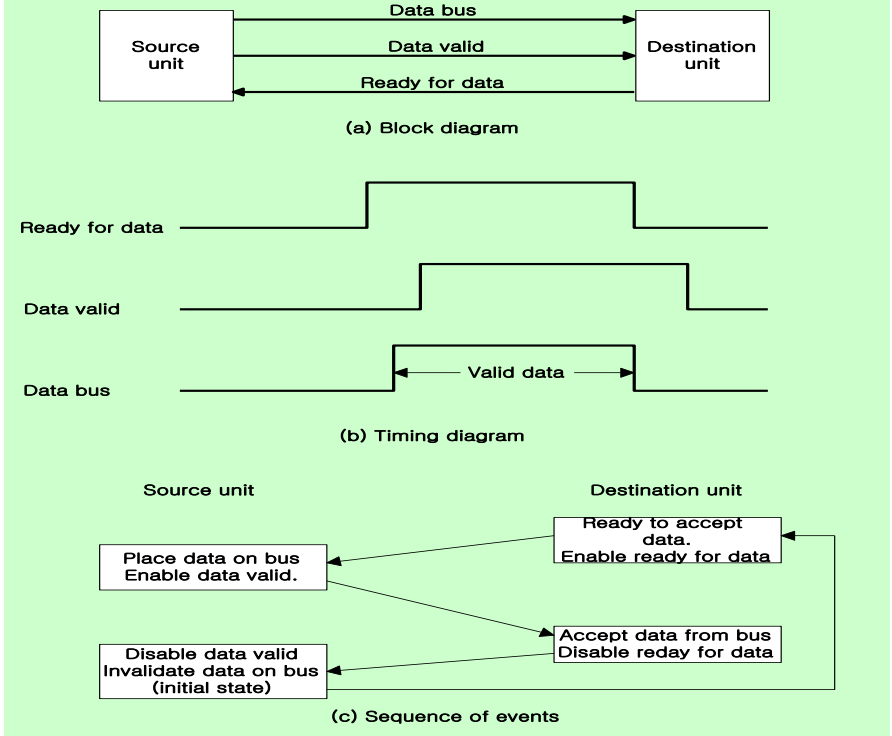
Source-initiated strobe & Destination initiated Strobe

- Handshake : Agreement between two independent units
  - 1) Source-initiated handshake :
  - 2) Destination-initiated handshake :

  Timeout : If the return handshake signal does not respond within a given time period, the unit assumes that an error has occurred.

- Modes of Transfer :
  - Data transfer to and from peripherals
    - 1) Programmed I/O :
    - 2) Interrupt-initiated I/O :
    - 3) Direct Memory Access (**DMA**) :
    - 4) I/O Processor (**IOP**) :

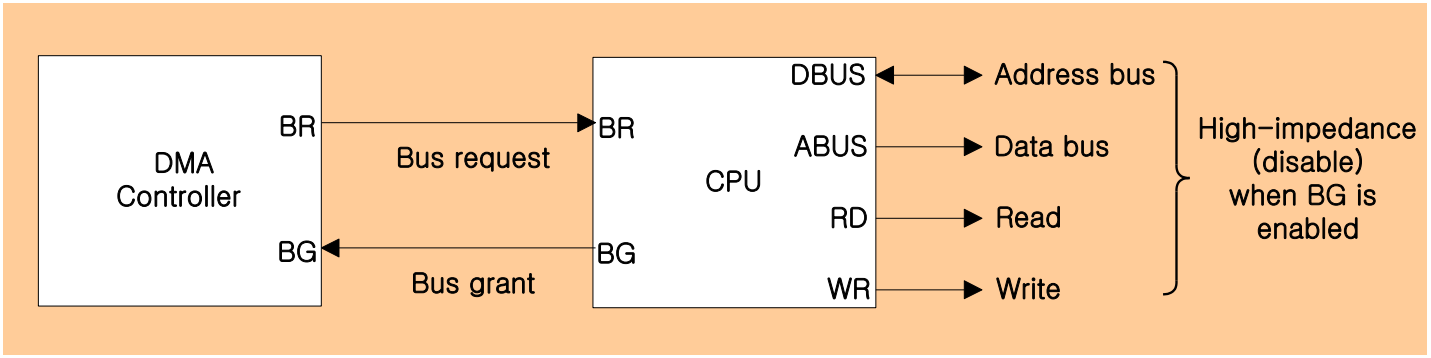


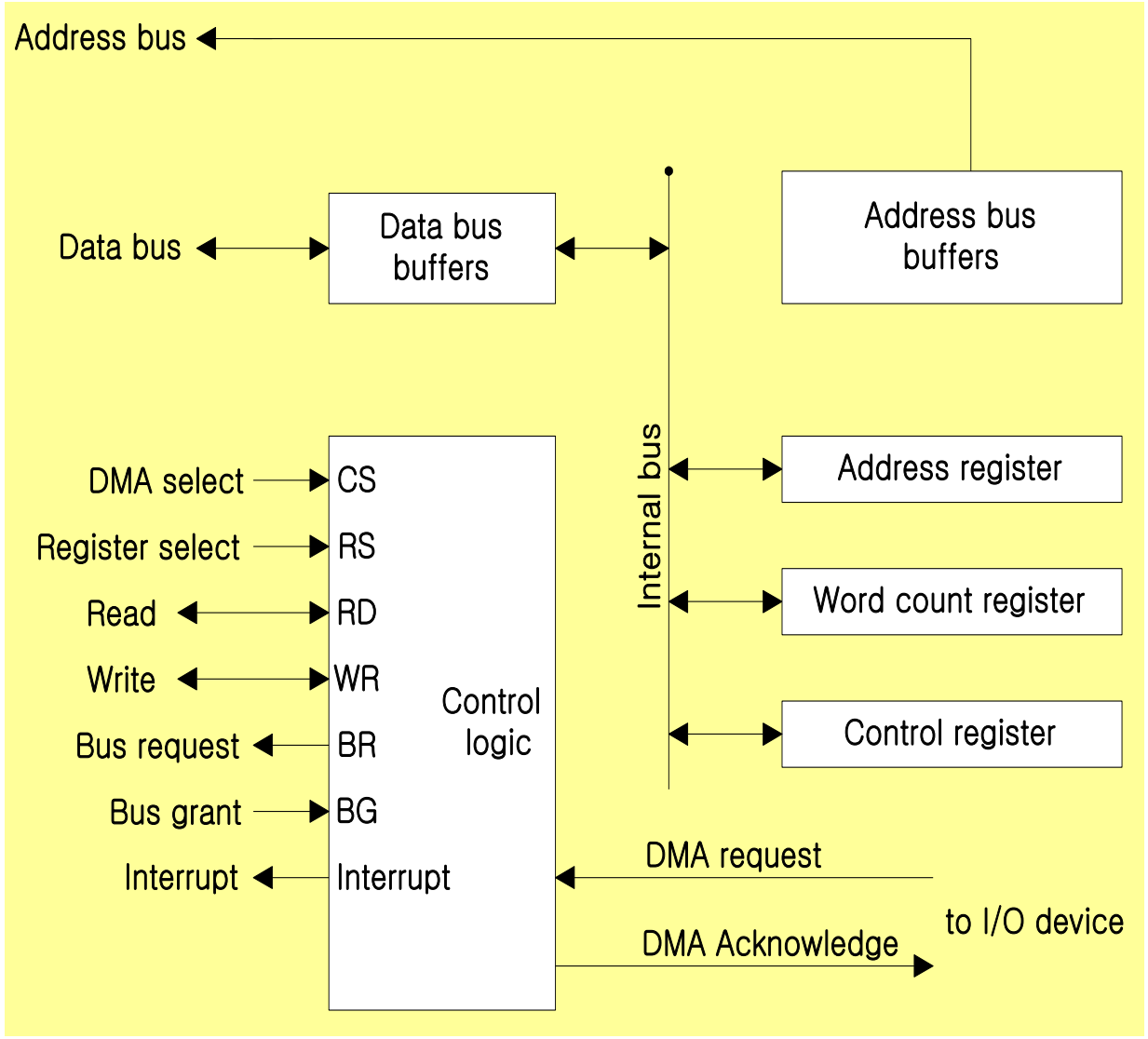


Source-initiated handshake & Destination initiated handshake

- Asynchronous Serial Transfer :
  - Synchronous transmission :
    - The two unit share a common clock frequency
    - Bits are transmitted continuously at the rate dictated by the clock pulses
  - Asynchronous transmission :
    - Special bits are inserted at both ends of the character code
    - Each character consists of three parts :
      - » 1) start bit : always “0”, indicate the beginning of a character
      - » 2) character bits : data
      - » 3) stop bit : always “1”

- Direct Memory Access (DMA) :
  - DMA
    - DMA controller takes over the buses to manage the transfer directly between the **I/O device** and **memory** *(**Bus Request/Grant**)*




Address bus
Data bus
Data bus buffers
Address bus buffers
Internal bus
DMA select
CS
Register select
RS
Read
RD
Write
WR
Bus request
BR
Bus grant
BG
Interrupt
Interrupt
Control logic
Address register
Word count register
Control register
DMA request
to I/O device
DMA Acknowledge

- Transfer Modes :
  - 1) Burst transfer : Block sequence of memory word transferred in cont. burst
  - 2) Cycle stealing transfer : data word transfer 1 at time. Bus control return to cpu

- DMA Controller (Intel 8237 DMAC) :
  - DMA Initialization Process
    - **1)** Set Address register :
      - » memory address for read/write
    - **2)** Set Word count register :
      - » the number of words to transfer
    - **3)** Set transfer mode :
      - » read/write,
      - » burst/cycle stealing,
    - 4) DMA transfer start :
    - 5) EOT (End of Transfer) :
      - » Interrupt