9/14/2023

ASSIGNMENT 2: PROGRESS REPORT 1
EEE3098S 2023

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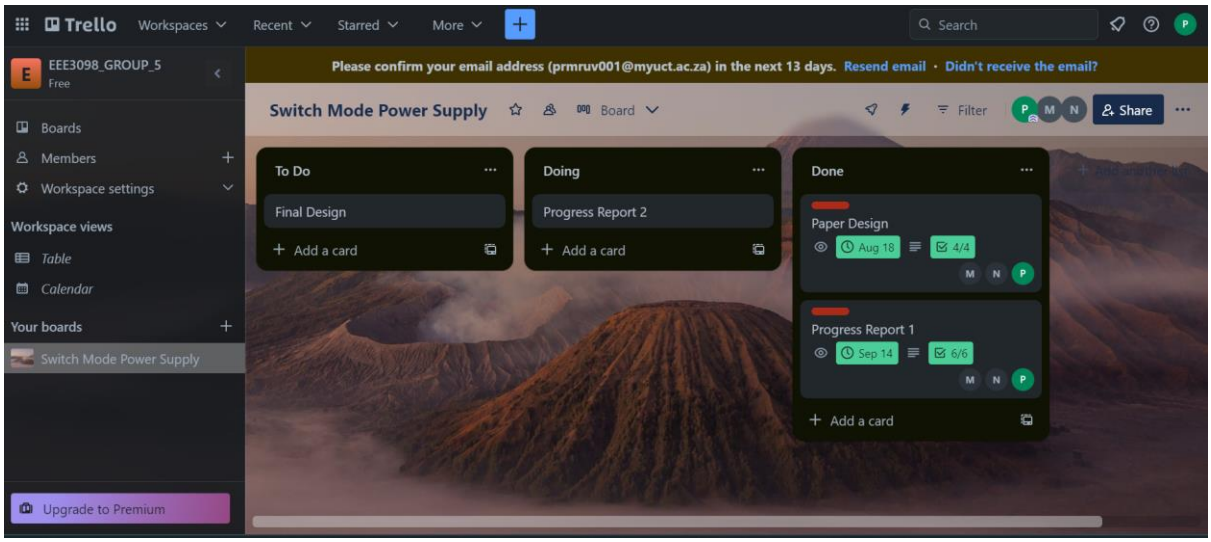
Contents

Admin Documents

Table of contributions:

Name	Contribution
Steve Muhilane – MHLSTE012	Project management tool, github, simulation setup, simulation results and analysis, system design and implementation, simulation setup, ATPs, conclusion.
Ruviel Perumal – PRMRUV001	Project management tool, github, simulation setup, simulation results and analysis, system design and implementation, simulation setup, ATPs, conclusion.
Sivuyile Nose – NSXSIV001	Project management tool, github, simulation setup, simulation results and analysis, system design and implementation, simulation setup, ATPs, conclusion.

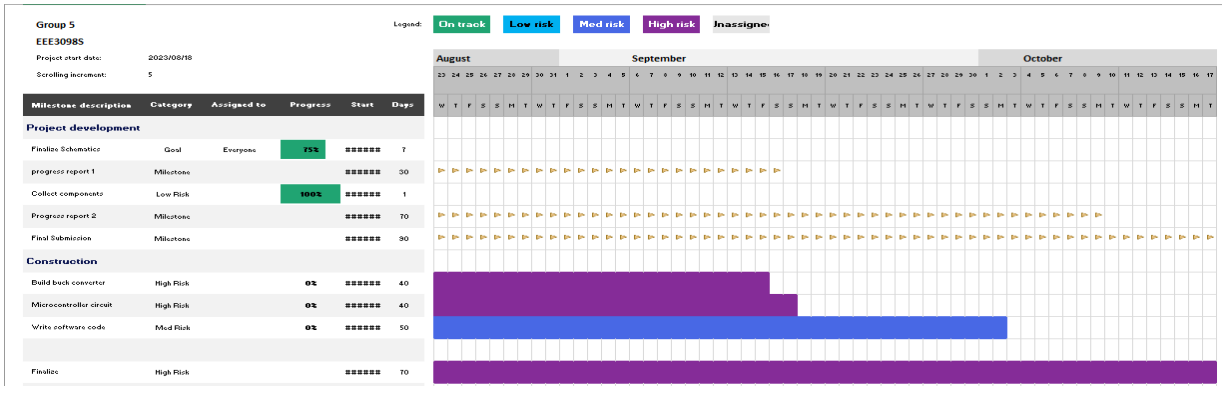
Project Management Tool:



GitHub repository link:

https://github.com/RuvielP/EEE3098S_GROUP_5_2023.git

Timeline:



Simulation Setup

Simulation environment:

LTspice is a widely used electronics and electrical circuit simulation software with a number of features some of the features below were use in the process of simulating the circuits, main LTSpice features are as follows:

Schematic Editor: It allows you to create circuit schematics using various components.

Component Library: Offers an extensive library of electronic components.

Simulation Controls: Supports various simulation types like transient, AC, and DC analysis.

Waveform Viewer: Allows visualization of simulation results in voltage and current waveforms.

Parameter Sweeps: Enables analysis of circuit behavior with varying component values.

Monte Carlo Analysis: Assesses component tolerance effects and generates statistical data.

Symbol Editor: Lets you create custom symbols and models for components.

Hierarchical Design: Supports nested schematics for modeling complex systems.

Simulation Control Panel: Provides a user interface for configuring simulation settings.

Error Console: Reports issues with the circuit and aids in troubleshooting.

Scripting: Offers scripting capabilities for automation and batch simulations.

Integration: Can be integrated with external tools for advanced analysis.

LTspice provides a versatile environment for designing, simulating, and analysing electrical circuits, making it the better choice for the simulation.

LTSPICE was used to simulate the design of the Buck converter as well as the Integrated circuit required to control the buck converter and the digital I^2C wattmeter.

LTSPICE circuit:

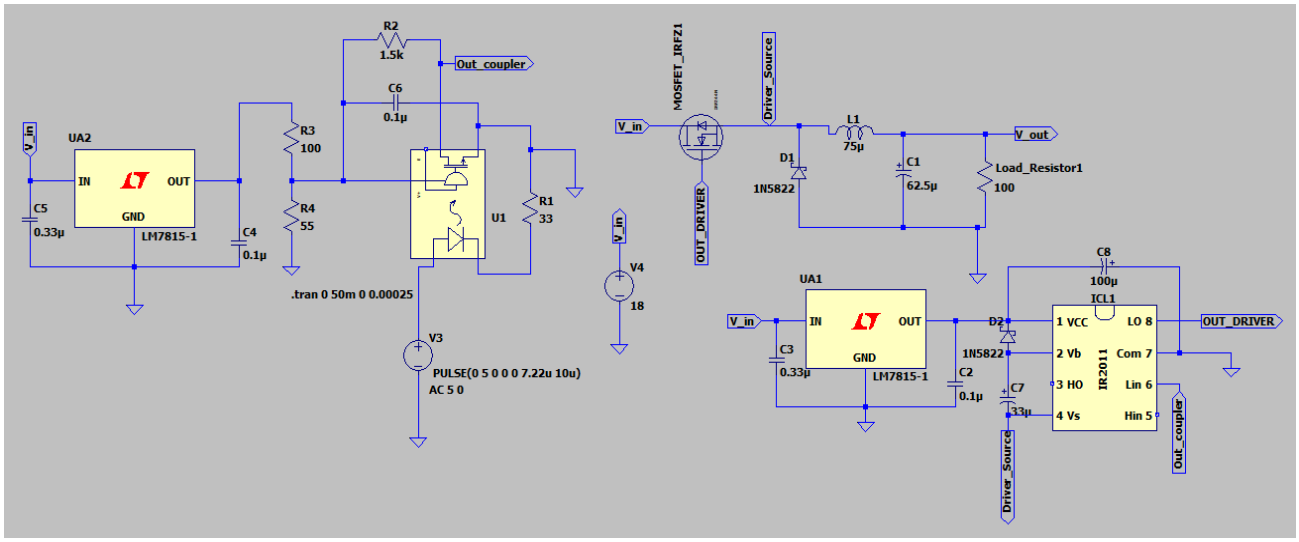


Figure 1:Overall Circuit

LTSPICE models used:

We had to import models for components which were not part of the standard. We used the IRFZ44N model, two LM7815 models for the voltage regulator. Instead of the ICL7667 MOSFET gate driver we used the IR2011 MOSFET driver which has the same characteristics as the ICL7667 MOSFET gate driver.

Part no.	Name	Quantity	LTSpice Model
ICL7667	MOSFET gate driver IC	1	IR2011
EKR FROLYT 100uF 63V	Capacitor	1	Ideal Capacitor
6N137	High Speed Optocouplers	1	6N137
IRFZ44N	N-CHANNEL POWER MOSFET	1	IRZ44N
UA7815UC	Fixed Positive Voltage Regulator	2	LM7815
10W 6.8 OMH [J]	RESISTOR	1	Ideal Resistor
IN5822	DIODE	1	IN5822
100uF 35V	Capacitor	2	Ideal Capacitor
INA219	I2C DIGITAL WATTMETER	2	IN219

System Design and Implementation

Voltage regulator:

The voltage regulator takes in an input voltage of 18V and regulates that voltage to 15V. A fixed positive voltage regulator was used to perform this regulation, with a part number UA7815UC. Two decoupling capacitors were used to achieve a constant voltage regulation of 15V as suggested by the part data sheet. To test the voltage regulator, we simulated the circuit. The circuit diagram of the voltage regulator is shown below.

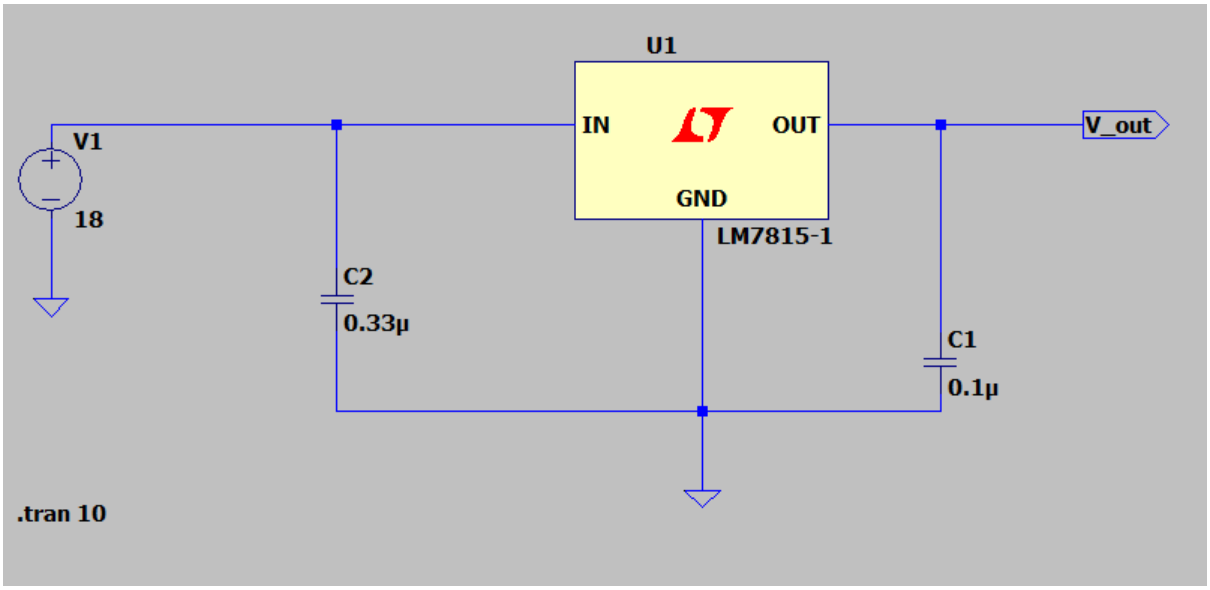


Figure 2:Voltage Regulator Circuit Diagram

Optocoupler circuit:

The optocoupler circuit serves as a portal between the trigger and the switching circuit. The main component of the optocoupler circuit is the optocoupler. The optocoupler takes in a 5V PWM signal from the microcontroller, which represented by a pulse voltage source. To test this circuit, we took the output of the voltage regulator, passed it through a voltage divider to produce a 5V that is fed into V_{dd} of the optocoupler. We then observe the output voltage of the optocoupler circuit through the load. Transient simulations of the circuit are then run. The circuit diagram of the optocoupler is shown below.

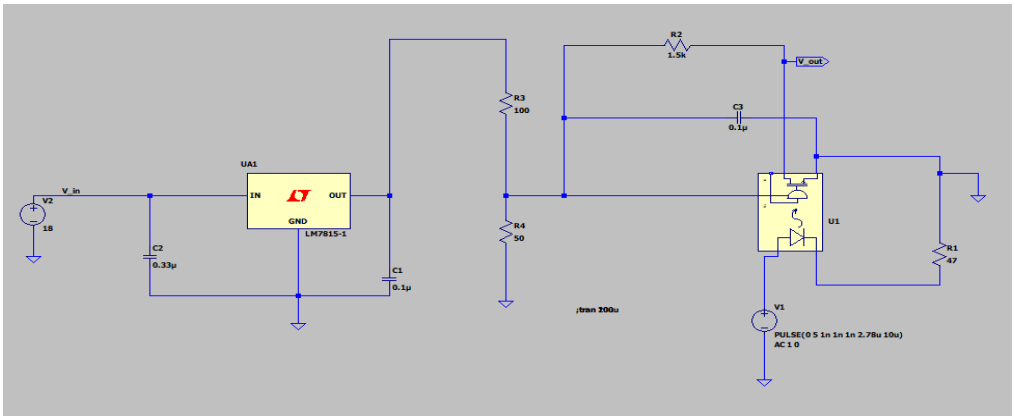


Figure 3:Optocoupler Circuit

MOSFET driver circuit:

The MOSFET driver circuit is a specialized circuit that is used to drive the gate of the power MOSFET effectively and efficiently as it has low output impedance in high-speed switching operations. The MOSFET driver circuit takes in the output of the optocoupler circuit and supply's its output to the buck converter circuit. The circuit diagram of the MOSFET driver circuit is shown below.

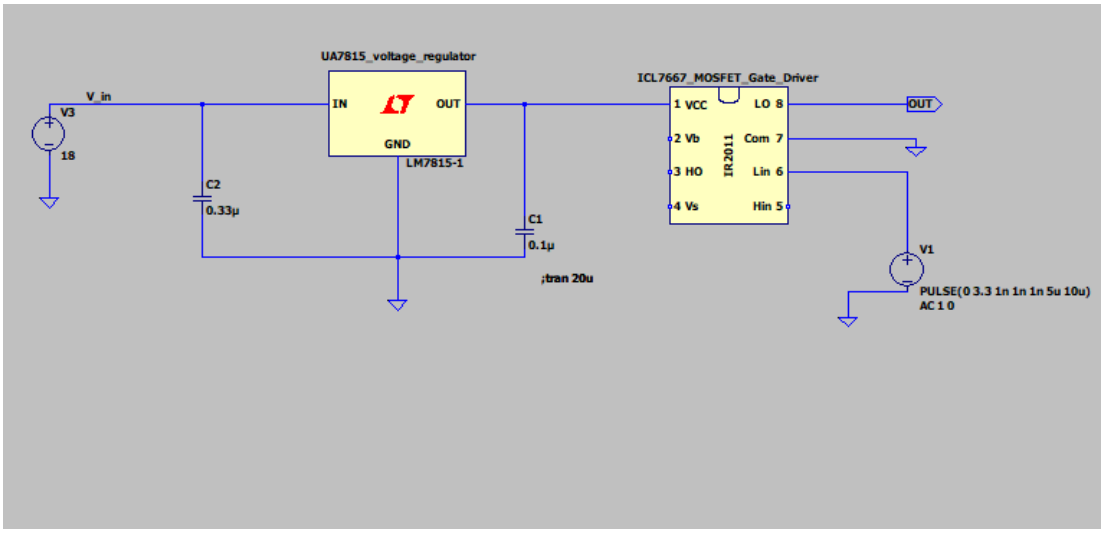


Figure 4:MOSFET driver circuit

Buck converter circuit:

The Buck converter is the DC-DC converter that ultimately steps down the voltage to the desired 5V. It takes in the output of the MOSFET driver circuit into the MOSFET gate. The circuit consists of an inductor, capacitor, diode and MOSFET. Transient simulations were performed to determine the output voltage and output current in relation to the input. The circuit diagram of the buck converter is shown below.

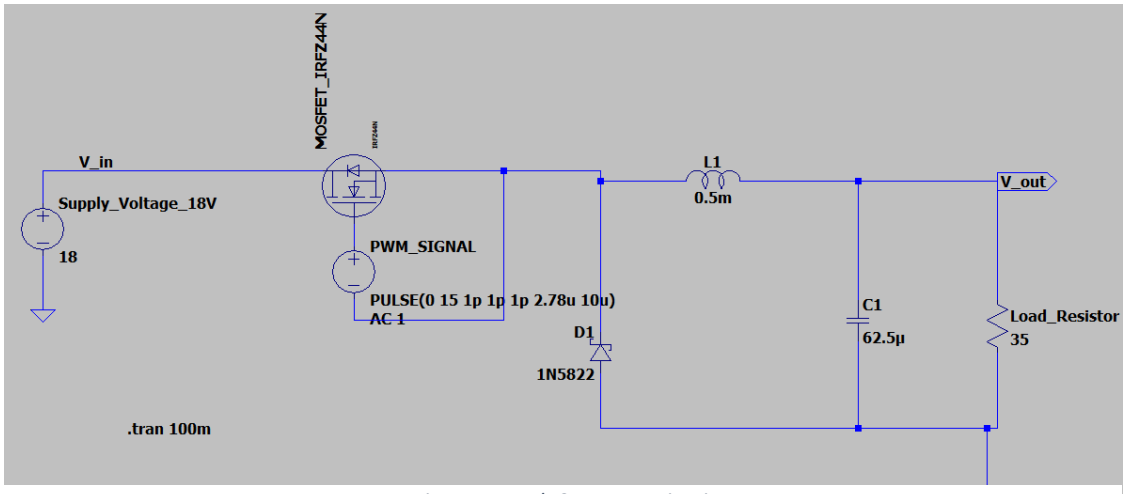


Figure 5: Buck Converter circuit

Overall system:

The switch mode power supply relies on varies submodules to be integrated as one in order to efficiently operate. This includes all the submodules mentioned above. After AC-DC rectification, the voltage supplied to the SMPS is 18V. This voltage is fed into the voltage regulator which regulates the voltage to 15V. This voltage is then fed into the optocoupler through a voltage divider. The output of the optocoupler is fed into the MOSFET driver circuit. At this stage the MOSFET driver circuit feeds the signal into the MOSFET of the buck converter to implement switching of the buck converter. The buck converter finally steps down the voltage to the desired 5V voltage.

The microcontroller, which is represented by the pulse voltage source at the optocoupler, is connected to the overall design. The role of the microcontroller is to change the duty cycle of the circuit depending on the desired step-down voltage, either 5V at an 0.28 duty cycle or 9V at a 0.5 duty cycle. To change the duty cycle, two of the built in buttons on the UCT Dev board will be configured such that the above-mentioned operation can be performed.

The digital I^2C wattmeter will be connected to the output and the input of the buck converter in order for the microcontroller to calculate the efficiency and display it on the LCD screen.

The overall system circuit diagram is shown below.

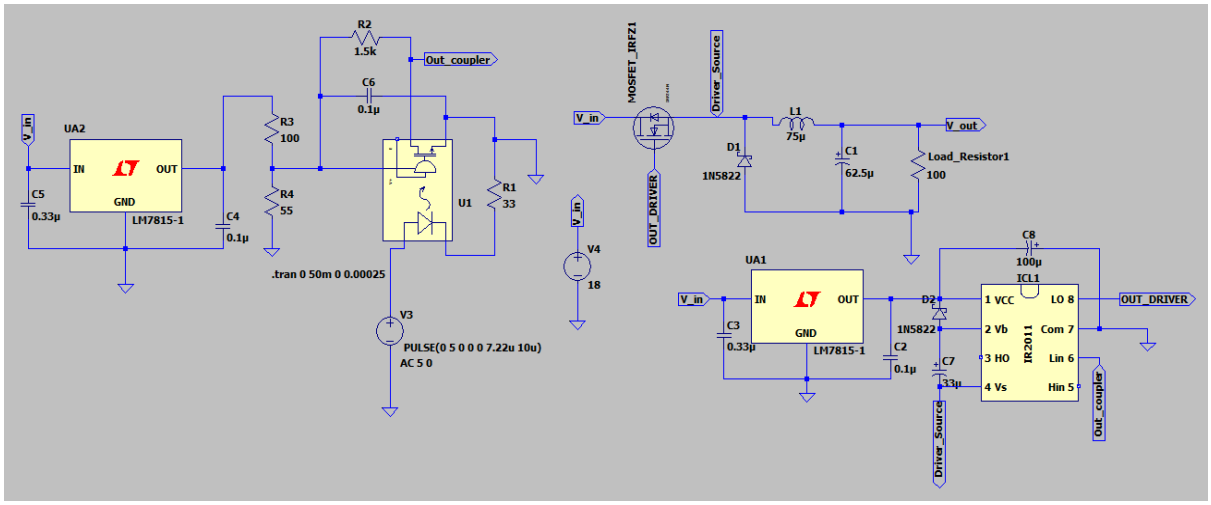


Figure 6: Overall System

Revised theoretical calculations:

We aim to design an SMPS that converts an 18V DC input into a stable output voltage ranging from 5V to 9V DC. We have selected a switching frequency of 100 kHz for this design. In our resistor selection process, we opted for a minimum value of 10 ohms. Additionally, to maintain continuous conduction mode for the inductor current, we need to determine the minimum inductor value.

To calculate the Inductor Value:

$$L = \frac{R(1-D)}{2f_s}$$

$Where$:

$V_0 = 5V, 9V$

$for\ 5V$:

$$D = \frac{V_o}{V_{in}} = \frac{5}{18} = 0.28$$

$for\ 9V$:

$$D = \frac{V_o}{V_{in}} = \frac{9}{18} = 0.5$$

$$f_s = 100kHz$$

Therefore, the minimum inductor values for different output voltages are as follows:

$$\boldsymbol{For\ output\ of\ 5V}:$$

$$L\_min = \frac{10(1-0.28)}{(1000000)(2)} = 36\mu H$$

$$\boldsymbol{for\ output\ of\ 9V}:$$

$$L\_min = \frac{10(1-0.5)}{(1000000)(2)} = 25\mu H$$

Based on these calculations, it is advisable to select an inductor value greater than 36 µH. After conducting simulations, a 75 µH inductor was found to provide the best response while exceeding the minimum required inductor value. To ensure optimal performance, a voltage ripple of 10 mV is desired.

$$Capacitor\ value\ is\ calculated\ using:$$

$$C = \frac{1-D}{8L\left(\frac{\Delta V_o}{V}\right)f^2} = \frac{1-0.28}{8(75\mu)\left(\frac{0.01}{5}\right)(100000)^2} = 62.5\mu F$$

Now our selection:

- Inductor value $75\ \mu H$
- Capacitor value $68\ \mu F (aligned\ with\ standard\ E12\ value)$

Embedded software used:

1. **Header Files Inclusion:**

The software includes the necessary STM32 HAL and CMSIS header files. These files provide functions and definitions required for STM32 development.

2. **Global Variables:**

This variable stores the configuration settings for Timer 2, which is used to generate the PWM signal. These arrays store the GPIO port and pin configurations for two buttons used to adjust the duty cycle.

3. **Main Function:**

The main function initializes the system, GPIO pins, and Timer 2 for PWM generation.

It starts the PWM generation using **HAL_TIM_PWM_Start**.

The main loop contains the application code and continuously runs the microcontroller.

4. **Timer Configuration (TIM2 - PWM):**

Initializes Timer 2 for PWM generation with a frequency of 100 kHz and an initial duty cycle of 0.28.

The TIM2 peripheral is enabled and configured to generate PWM on Channel 1 (PA6).

5. **GPIO Configuration:**

Configures GPIOA pins:

PA6 is configured as an alternate function (AF1) with push-pull output for PWM output.

PA0 and PA1 are configured as input pins for the two buttons.

6. **Button Callback Function:** This function is called when a button press is detected (falling edge).

It checks which button was pressed and adjusts the **duty cycle,** accordingly, ensuring it stays within the range of 0.28 to 0.5.

The PWM pulse is updated based on the new duty cycle.

Simulation Results and Analysis

The simulation parts will be broken into the voltage regulator simulation, MOSFET driver circuit simulation, optocoupler circuitry simulation, PWM simulation (software simulations), buck converter simulations and I2C wattmeter simulations.

Voltage regulator simulation:

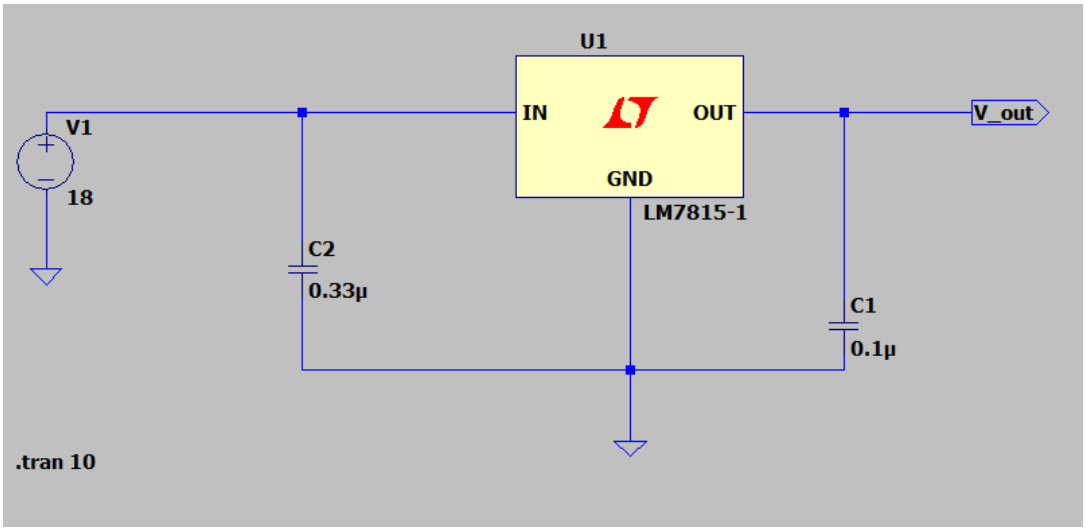


Figure 6: Voltage Regulator Circuit

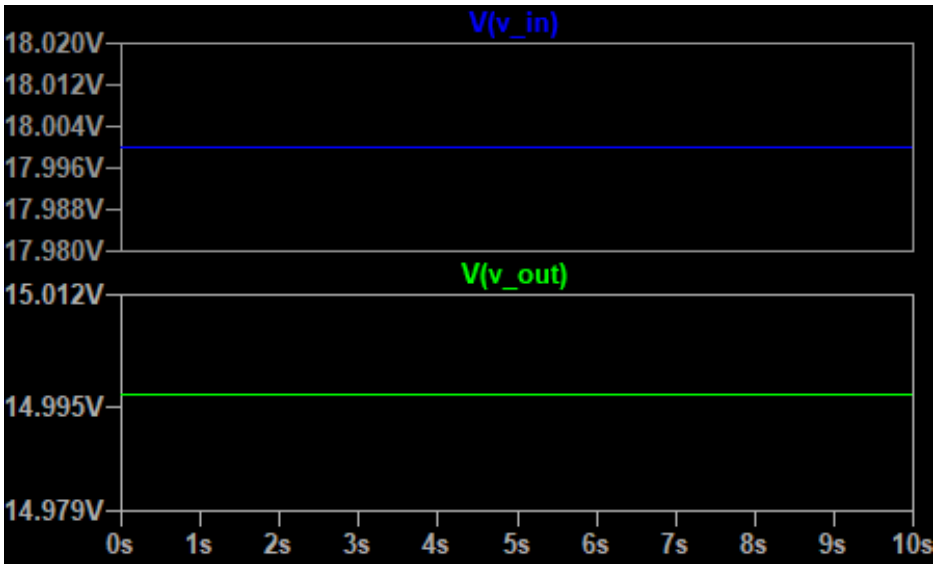


Figure 7: Voltage waveform of voltage regulator

The waveform above describes the input and output of the voltage regulator. The blue line represents the input voltage into the voltage regulator and the output voltage is represented by the green waveform. It is clear to see that the voltage is regulated from 18V to the desired 15V that will be fed into the optocoupler.

Optocoupler circuit simulation:

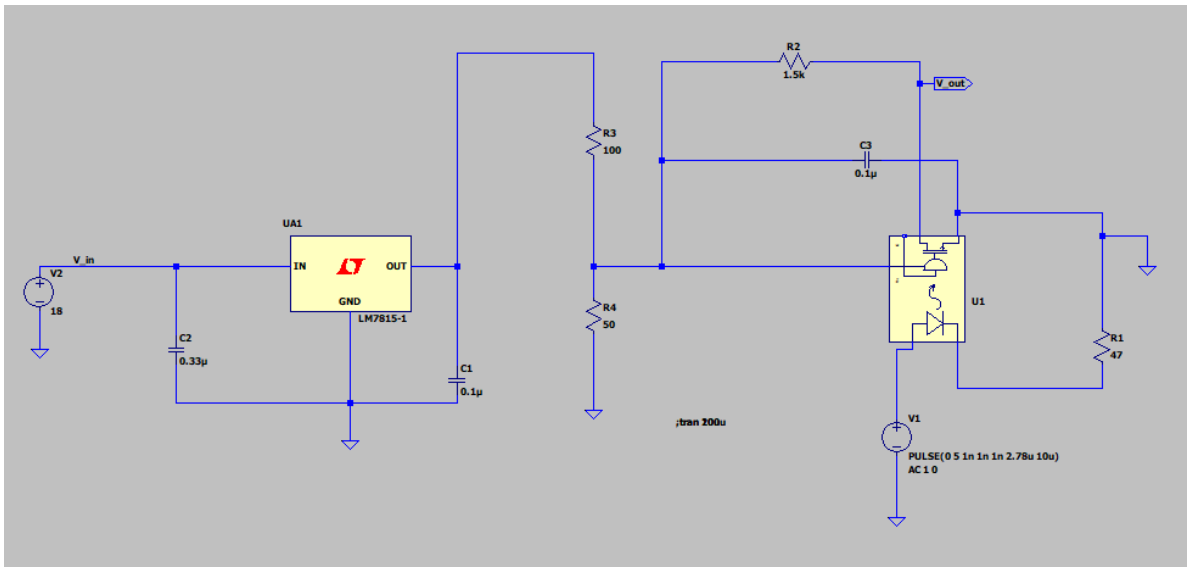


Figure 8: Optocoupler circuit

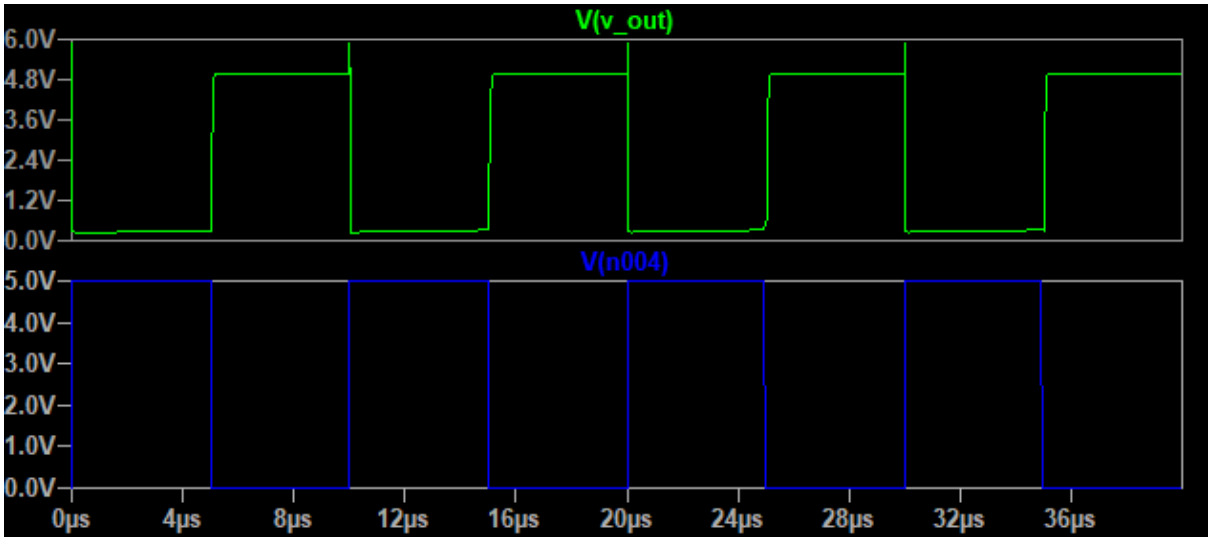


Figure 9: Voltage waveform of optocoupler

The optocoupler employed in this setup has an inverted output characteristic. To align with this behaviour and attain the desired duty cycle, it's necessary to apply an input signal that is itself inverted. The voltage waveform in green accurately represents the output generated by the optocoupler circuit, providing a pulse with the specified duty cycle. On the other hand, the input signal to the optocoupler, represented by the blue waveform, consists of a pulse with a duty cycle of 1 minus D (1-D). It's important to note that the green waveform reaches a peak magnitude of 5V, corresponding to the maximum output voltage, since the input voltage from the optocoupler's Vdd is set at 5V.

MOSFET driver circuit simulation:

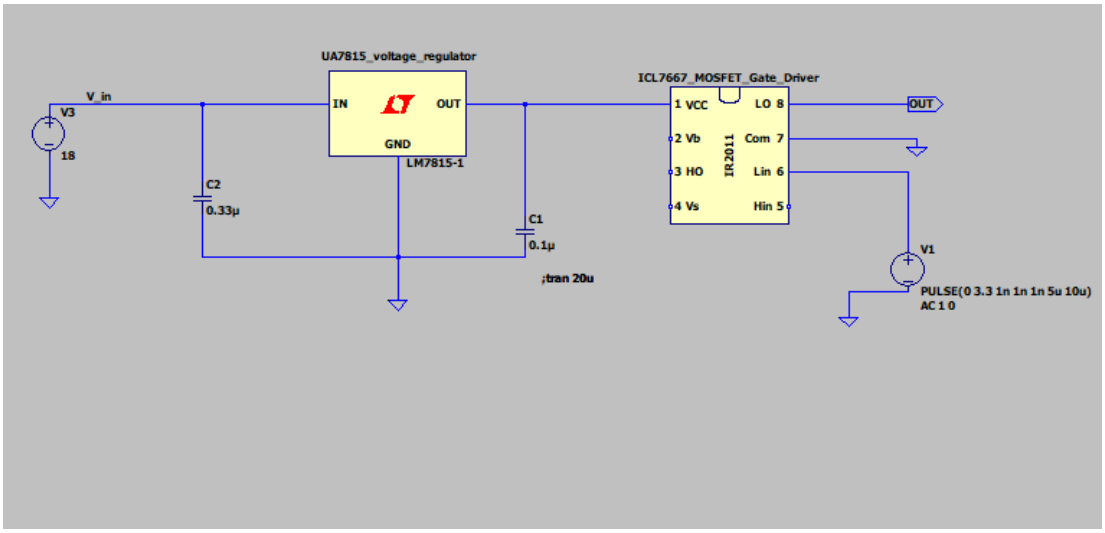


Figure 10: MOSFET driver circuit

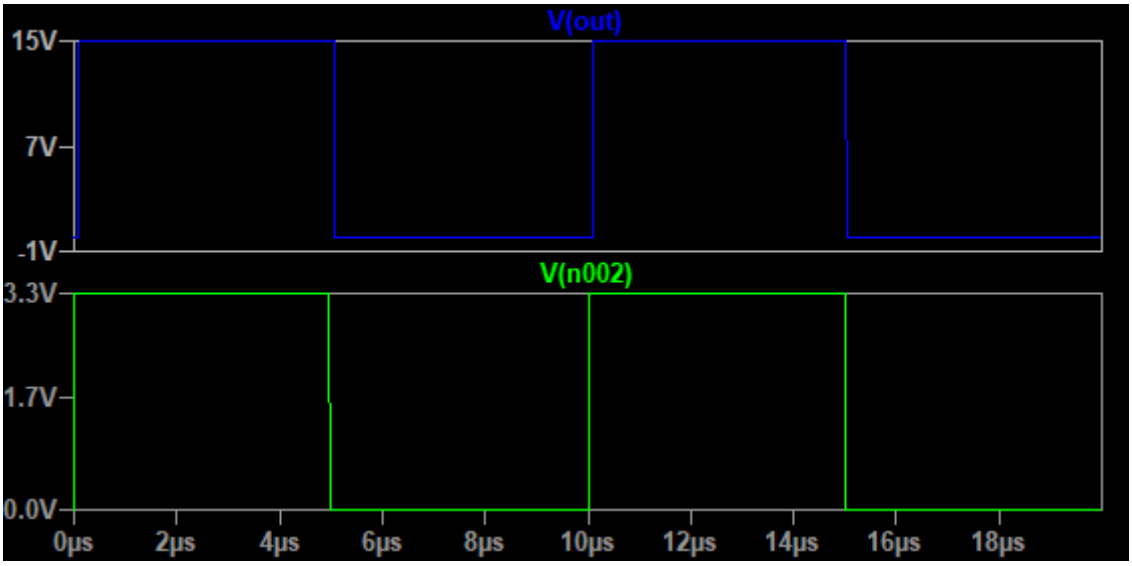


Figure 11: Voltage waveform of mosfet driver circuit

The depicted figures illustrate the input and output characteristics of the MOSFET driver circuit. The signal originating from the optocoupler serves as the input to the MOSFET driver circuit and is simulated as a 3.3V pulse waveform, as denoted by the green waveform in the figures. The output voltage from the MOSFET driver circuit, observed at 15V, is represented by the blue waveform. This 15V output, generated by the MOSFET driver circuit, is subsequently directed to the MOSFET's gate terminal. It's worth noting that this 15V signal is more than sufficient to effectively drive the MOSFET.

Buck converter simulations:

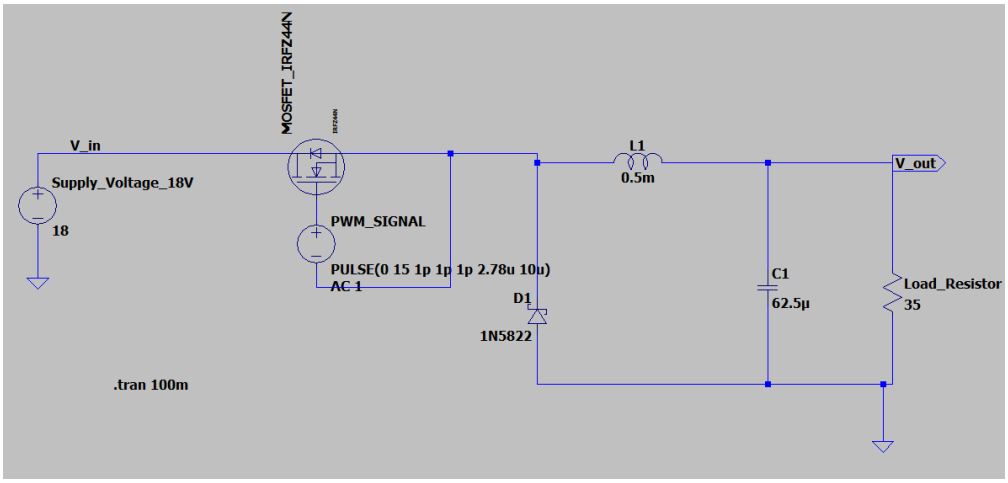


Figure 12: Buck converter circuit

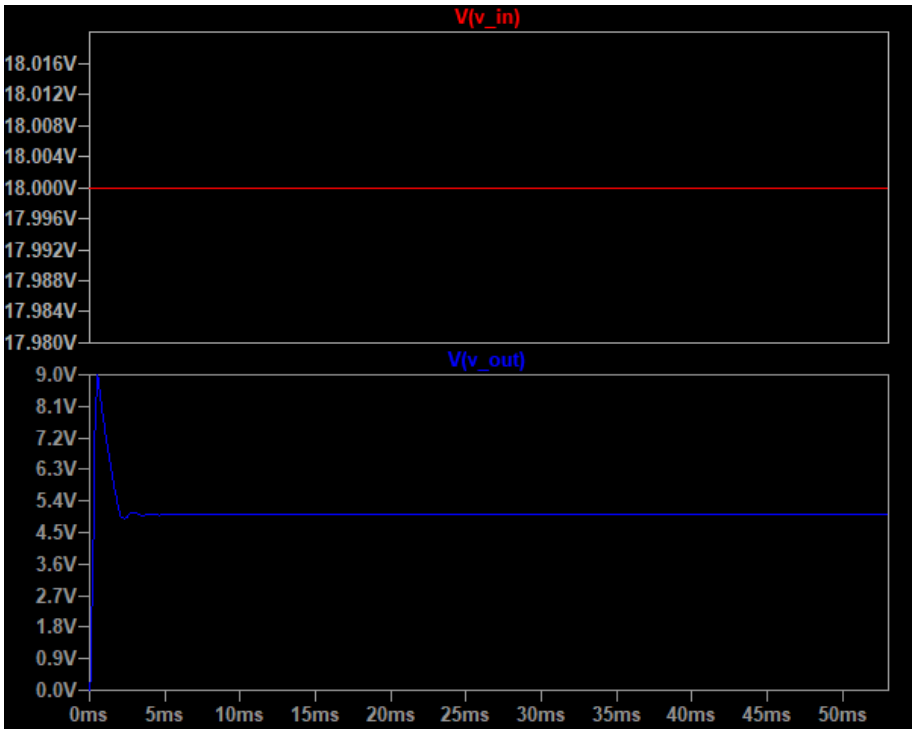


Figure 13: Voltage waveform of buck converter

The above figures resemble the Buck converter circuit diagram as well as the voltage waveforms of the buck converter. The red voltage waveform represents the input voltage of 18V that is being fed into the buck converter. The blue voltage waveform represents the step-down output voltage of the buck converter. As seen above in figure 13, the output voltage is stepped down to approximately 5V, which is the desired voltage from the buck converter.

Overall system:

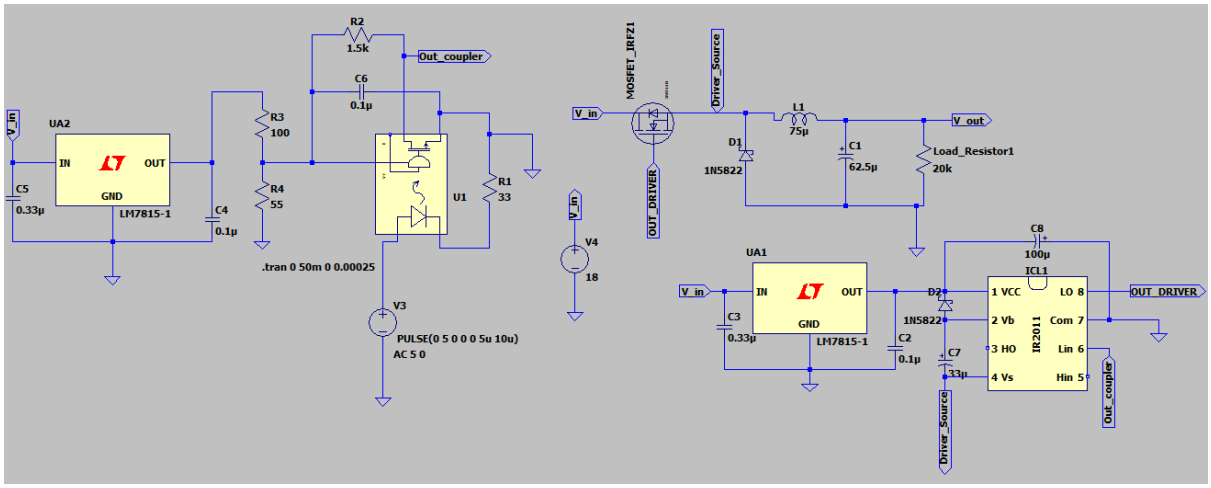


Figure 14: Overall system circuit

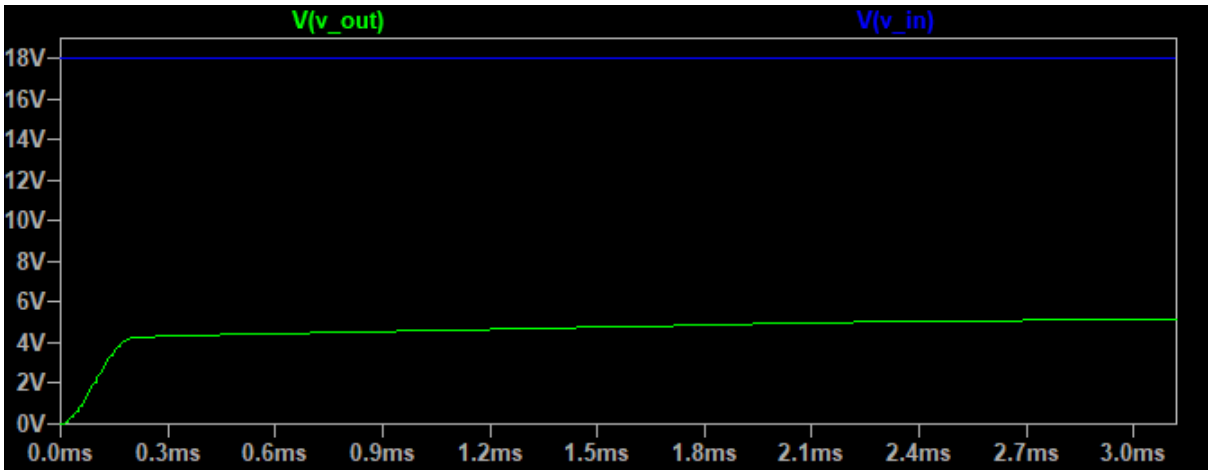


Figure 15: Voltage waveform of 5V step-down

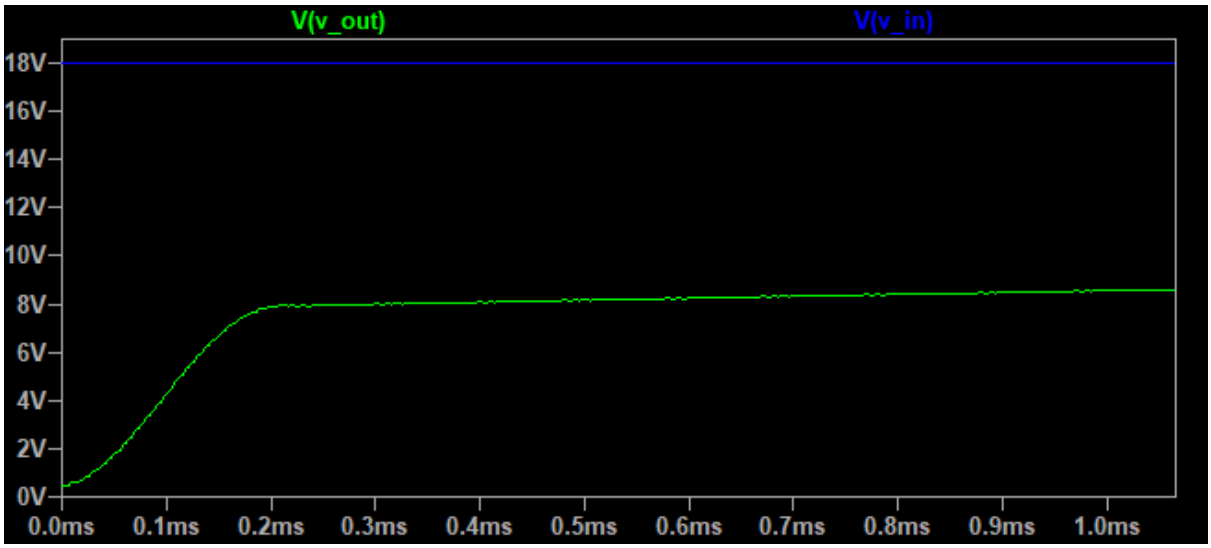


Figure 16: Voltage waveform of 9V step-down

Figure 14 depicts the overall system circuit. Figure 15 represents the voltage waveform with a duty cycle of 0.28. The blue waveform represents the input voltage of 18V, and the green waveform represents the step-down voltage. In this figure it is clear to see that the system approaches and steadies out at approximately 4.3V. This could be due to the losses in the circuit as well as the tolerances of components. Figure 16 represents the voltage waveform with a duty cycle of 0.5. The blue waveform represents the input voltage of 18V, and the green waveform represents the step-down voltage. In this figure it is clear to see that the system approaches and steadies out at approximately 8.4V. Again, this could be due to the losses in the circuit as well as the tolerances of components. Overall, the design comes very close to the desired outcome.

Challenges and Limitations:

1. **Component Models**: One of the initial challenges we encountered during the simulation process was the availability of accurate models for the specific components we were using in our design. While LTspice provides an extensive library of component models, there were instances where we couldn't find exact matches for the components we were using in our real-world circuit. To address this, we had to identify and use substitute models available in LTspice that closely matched the electrical characteristics of our components. This introduced an element of approximation, which required careful consideration and validation to ensure the simulation results were still representative of our actual circuit.
2. **Complex Circuit:** Our SMPS design's complexity led to setup difficulties, increased error risks, and challenges in diagnosing simulation issues. We tackled this complexity by systematically testing smaller subcircuits before integrating them into the complete design.
3. **Simulation Speed:** The circuit's complexity caused significant LTspice simulation slowdowns, hindering extensive testing and rapid design iterations. We optimized our setup, reducing the simulation time span, increasing time steps, and selectively disabling non-essential outputs. Parameter sweeping and efficient resource use aided in overcoming these time constraints.

Evaluation (ATPs)

The acceptance test procedure will ensure that the design meets its intended performance. The procedure involves defining figures of merit, designing experiments to evaluate these metrics, and establishing acceptable performance standards.

Figures of merit:

ATP ID	ATP name	Figures of merit
ATP001	Voltage Regulation	This is about making sure the output voltage stays steady even when things change. We want to know if the SMPS can keep the voltage where we want it, no matter what's happening.
ATP002	Efficiency	This tells us how good the SMPS is at turning the input power into useful output power. It's like checking if we're not wasting too much energy during the conversion process.
ATP003	Transient Response	This checks how quickly the SMPS can handle sudden changes in power demand. We want to see if the output voltage behaves well even when there's a sudden shift in the load.
ATP004	Switching Frequency Stability	We're looking at how consistent the switching of the SMPS is. It's like making sure the rhythm of the system stays steady.

Experiment Design:

ATP ID	ATP name	Test
ATP001-T1	Voltage Regulation	We'll suddenly change the load to see if the SMPS can keep the output voltage steady. We'll watch the output voltage closely and check if it stays within a certain range of the desired voltage.

ATP002-T2	Efficiency	We'll change the load (the power being drawn) from low to high and see how the SMPS handles it. We'll calculate the efficiency for different load levels and see if it's at least 80% efficient, as we planned.
ATP003-T3	Transient Response	We'll quickly change the load and see how the output voltage reacts. We want to make sure the voltage doesn't swing around too much during these quick changes.
ATP004-T4	Switching Frequency Stability	We'll change the input voltage and the load and see how the switching frequency behaves. We'll see if the switching speed stays pretty consistent no matter what we do.

Acceptable Performance Definitions:

ATP ID	ATP name	Acceptable Performance
ATP001-A1	Voltage Regulation	We consider it good if the output voltage stays within a small range (±5%) of what we want, no matter how much power we need.
ATP002-A2	Efficiency	We're happy if the efficiency is 80% or more across different power levels.
ATP003-A3	Transient Response	The response is great if the voltage doesn't jump around more than a little bit (±2%) during load changes.

ATP004-A4	Switching Frequency Stability	We're good if the switching speed doesn't change much (±2%) from the normal rate, even when we change things around.

By running these tests and comparing the results to what we think is good performance, we'll be able to say whether our SMPS design works the way we planned. The results and evaluations of the tests are tabulated below.

Evaluation of ATP's:

ATP ID	ATP name	Evaluation
ATP001-E1	Voltage Regulation	After performing simulations at various loads in our buck converter we notice that the voltage is regulated to around 4.3V. This indicates that the buck converter operates as not quite as we expect and the Test performed falls just out of the acceptable performance, ATP001-A1.
ATP002-E2	Efficiency	After performing simulations at various loads in our SMPS we measure the output power and calculate the efficiency of the system. We can see that the efficiency remains around about the same and the test falls within the acceptable performance, ATP002-A2.
ATP003-E3	Transient Response	For this test we quickly changed the load and we notice the output voltage. We notice that the voltage does not swing around too much. The voltage doesn't jump around more than a little bit (±2%) during load changes. This matches the acceptable performance, ATP003-A3

ATP004-E4	Switching Frequency Stability	We change the input voltage and the load and see how the switching frequency behaves. We notice that the switching speed doesn't change much (±2%) from the normal rate. This falls within the acceptable performance, ATP004-A4.

Improvements and modifications to design:

ATP ID	ATP name	Improvements/Modifications
ATP001	Voltage Regulation	We can increase the capacitance of the boot strap which will make sure that the voltage of the MOSFET driver is high.

Next steps for project:

1. Correct schematic with above mentioned improvements and modifications.
2. Test individual components.
3. Build circuit prototype on breadboard.
4. Test prototype using lab equipment.

Conclusion

After completing tests to our system design, we have deduced various findings that can assist us in improving the design of the overall system. It was clear to see that each submodule performed exactly as expected on their own. However, when the submodules are cascaded together, the output voltage is not exactly as expected as seen in the analysis. This could be due to loading effects of the circuit.

Furthermore, there has been some improvements suggested in order to improve the overall design to make sure that the overall design is in accordance with the Acceptable performance that was tabulated in the ATP section.

Many lessons were learnt during this report. Such as accounting for external factors such as component tolerances, loading effects and power losses within a circuit.

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