Chapter 11: Field effect Transistors: Operation, Circuit, Models, and Applications – Instructor Notes

Chapter 11 introduces field-effect transistors. **Should the instructor choose to only teach field-effect devices (or to cover FETs before BJTs), Section 10.1 can be used as an introductory section prior to starting Chapter 11.**

Section 11.1 briefly reviews the classification and symbols for the major families of field-effect devices. Section 11.2 introduces the fundamental ideas behind the operation of N-channel field-effect enhancement-mode transistors. A brief explanation of P-channel devices is also presented in this section. Section 11.3 , illustrates the calculation of the state and operating point of basic field-effect transistor circuits. Section 11.4 outlines the operation of MOSFET large-signal amplifiers, and presents two practical examples (11.6 and 11.7), rfelated to a battery charging circuit and a DC motor drive circuit. These examples are analogous to those presented in Chapter 10 for BJT large-signal amplifiers, giving the instructor the opportunity to make a comparison of the two technologies, if so desired. Finally, Section 11.5 introduces the analysis of MOSFET switches and presents CMOS gates. The box *Focus on Measurements: MOSFET bidirectional analog gate* (pp. 572-573) presents ananalog application of CMOS technology.

The end-of-chapter problems are straightforward applications of the concepts illustrated in the chapter. The 5th Edition of this book includes 13 new problems; some of the 4th Edition problems were removed, increasing the end-of-chapter problem count from 23 to 35.

Learning Objectives

1. Understand the classification of field-effect transistors. *Section 11.1.*
2. Learn the basic operation of enhancement-mode MOSFETs by understanding their *i-v* curves and defining equations. *Section 11.2.*
3. Learn how enhancement-mode MOSFET circuits are biased. *Section 11.3.*
4. Understand the concept and operation of FET large-signal amplifiers. *Section 11.4*
5. Understand the concept and operation of FET switches. *Section 11.5.*
6. Analyze FET switches and digital gates. *Section 11.5.*

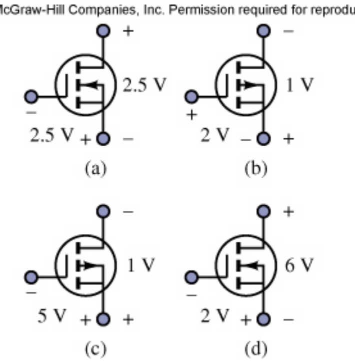
Section 11.2: n-channel MOSFET Operation

Problem 11.1

Solution:

Known quantities:

For the transistors shown in Figure P11.1, $|V_T| = 3\text{V}$.



Find:

The operating state of each transistor.

Analysis:

a) This is an n-channel enhancement MOSFET, with V_T = - 3 V. To operate in the triode region, the condition is: $v_{DS} < v_{GS} - V_T$. To operate in the saturation region, the condition is: $v_{DS} \geq v_{GS} - V_T$. To turn the transistor on, the condition is: $v_{GS} > V_T$.

We can compute: $v_{GS} = -2.5\text{ V}$ $\quad v_{DS} = 2.5\text{ V}$ $\quad v_{GS} - V_T = -2.5 + 3 = 0.5\text{ V}$

$v_{DS} = 2.5\text{ V} > \text{v}_{\text{GS}} - V_T = 0.5\text{ V}$.

Therefore, the transistor is in the saturation region.

b) This is a p-channel enhancement MOSFET, with V_T = 3 V. To operate in the triode region, the condition is: $v_{DS} > v_{GS} - V_T$. To operate in the saturation region, the condition is: $v_{DS} \leq v_{GS} - V_T$. To turn the transistor on, the condition is: $v_{GS} < V_T$.

We can compute: $v_{GS} = 2\text{ V}$ $\quad v_{DS} = -1\text{ V}$ $\quad v_{GS} - V_T = 2 - 3 = -1\text{ V}$

$v_{DS} = -1\text{ V} > \text{v}_{\text{GS}} - V_T = -1\text{ V}$.

Therefore, the transistor is in the saturation region.

c) This is a p-channel enhancement MOSFET, with V_T = - 3 V. To operate in the triode region, the condition is: $v_{DS} > v_{GS} - V_T$. To operate in the saturation region, the condition is: $v_{DS} \leq v_{GS} - V_T$. To turn the transistor on, the condition is: $v_{GS} < V_T$.

We can compute: $v_{GS} = -5\text{ V}$ $\quad v_{DS} = -1\text{ V}$ $\quad v_{GS} - V_T = -5 + 3 = -2\text{ V}$

$v_{DS} = -1\text{ V} > \text{v}_{\text{GS}} - V_T = -2\text{ V}$.

Therefore, the transistor is in the triode region.

d) This is an n-channel enhancement MOSFET, with V_T = - 3 V. To operate in the triode region, the condition is: $v_{DS} < v_{GS} - V_T$. To operate in the saturation region, the condition is: $v_{DS} \geq v_{GS} - V_T$. To turn the transistor on, the condition is: $v_{GS} > V_T$.

We have: $v_{GS} = -2\text{ V} > V_T$.

$v_{GS} - V_T = -2 + 3 = 1\text{ V}$

$v_{DS} = 6V > v_{GS} - V_T = 1\text{ V}$

Therefore, the transistor is in the saturation region.

Problem 11.2

Solution:

Known quantities:

The potentials of an n-channel enhancement-mode MOSFET (4, 5, and 10 V respectively).

Find:

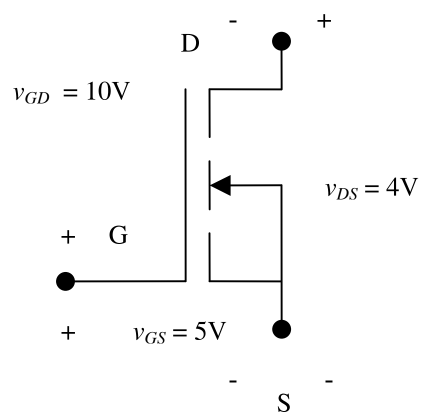
The circuit symbol, if the device is operating:

a) In the ohmic state.
b) In the active region.

Analysis:

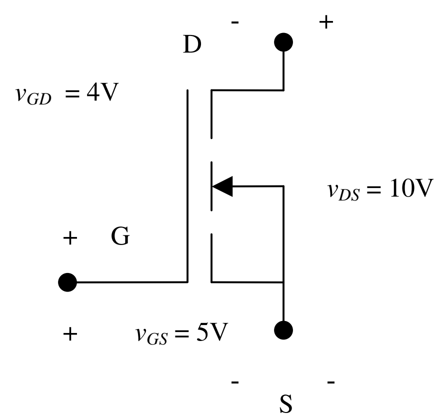
a) To operate in the ohmic region, the condition is: $v_{DS} < v_{GS} - V_T$ and $V_T > 0$, $v_{DS} > 0$.

The circuit for operation in the ohmic region is shown below.



b) To operate in the active region, the condition is: $v_{DS} \geq v_{GS} - V_T$ and $V_T > 0$, $v_{DS} > 0$.

The circuit for operation in the active region is shown below.



Problem 11.3

Solution:

Known quantities:

The threshold voltage, $V_T = 2$ V, of an enhancement-type NMOS that has its source grounded and a 3 V DC source connected to the gate.

Find:

The operating state if:

a) $v_D = 0.5\,\mathrm{V}$.

b) $v_D = 1\,\mathrm{V}$.

c) $v_D = 5\ \mathrm{V}$

Analysis:

a)
$$v_{DS} = v_D = 0.5\,\mathrm{V}$$
$$v_{GS} - V_T = 3 - 2 = 1\ \mathrm{V}$$
$$v_{DS} < v_{GS} - V_T$$

The transistor is in the triode region.

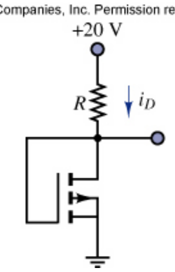
b)
$$v_{DS} = v_D = 1\,\mathrm{V}$$
$$v_{GS} - V_T = 3 - 2 = 1\ \mathrm{V}$$
$$v_{DS} = v_{GS} - V_T$$

The transistor is either in the triode or in the saturation region.

c)
$$v_{DS} = v_D = 5\,\mathrm{V}$$
$$v_{GS} - V_T = 3 - 2 = 1\ \mathrm{V}$$
$$v_{DS} > v_{GS} - V_T$$

The transistor is in the saturation region.

Problem 11.4



Solution:

Known quantities:

The threshold voltage, $V_T = 2$ V, of the p-channel transistor shown in Figure P11.4. $k = 10 \text{ mA/V}^2$.

Find:

R and v_D for $i_d = 0.4 \text{ mA}$.

Analysis:

The device shown is a p-channel enhancement mode MOSFET, with , $V_T = 2$ V and , $V_{DG} = 0$ V. To operate in the saturation region we require: $v_{DS} \geq v_{GS} - V_T$.

Since $v_{DG} = v_{DS} - v_{GS} = 0 > -V_T = -2$ V, the transistor is in the saturation region. Knowing $k = 10 \text{ mA/V}^2$, we can write: $0.4 = 10(v_{GS} - 2)^2$ and determine $v_D = v_{DS} = v_{GS} = 2.2$ V. R can be found as follows:

$$R = \frac{20 - v_D}{i_D} = \frac{20 - 2.2}{0.4 \cdot 10^{-3}} = 44.5 \text{ k}\Omega$$

Problem 11.5

Solution:

Known quantities:

The threshold voltage, $V_T = 2$ V, of an enhancement-type NMOS transistor. $i_D = 1$ mA when $v_{GS} = v_{DS} = 3$ V.

Find:

The value of i_D for $v_{GS} = 4$ V.

Analysis:

Because $v_{DS} > v_{GS} - V_T$, the transistor is in the saturation region:

$$i_D = k \cdot (v_{GS} - V_T)^2 = k \cdot (3 - 2)^2 = 0.001 \text{ A}$$

$$\Rightarrow k = 0.001.$$

For $v_{GS} = 4$ V we have:

$$i_D = 0.001 \cdot (4 - 2)^2 = 4 \text{ mA}.$$

Problem 11.6

Solution:

Known quantities:

Characteristics of an n-channel enhancement-mode MOSFET operated in the ohmic region:
v_{DS} = 0.4 V, V_T = 3.2 V. Effective resistance of the channel, given by: $R_{DS} = \dfrac{500}{(v_{GS} - 3.2)}\ \Omega$.

Find:

The value of i_D when v_{GS} = 5 V, R_{DS} = 500 Ω, and v_{GD} = 4 V.

Analysis:

Since $V_{DS} = 0.4 < v_{GS} - V_T = 5 - 3.2 = 1.8\text{ V}$,the transistor is operating in the ohmic region. The effective resistance is: $R_{DS} = \dfrac{500}{(5-3.2)} = 277.78\,\Omega$. Since $R_{DS} = \dfrac{V_{DS}}{i_D}$, we have: $i_D = \dfrac{V_{DS}}{R_{DS}} = 1.44\text{ mA}$.

Problem 11.7

Solution:

Known quantities:

The threshold voltage, V_T = 2.5 V, of an enhancement-type NMOS that has its source grounded and a 4 V DC source connected to the gate.

Find:

The operating state if:
a) $v_D = 0.5\text{ V}$
b) $v_D = 1.5\text{ V}$

Analysis:

a) v_{DS} = 0.5 < v_{GS} - V_T = 4 – 2.5 = 1.5 V, therefore the transistor is in the triode region.
b) v_D = 1.5 V = v_{DS} , therefore the transistor is at the border of the saturation and triode regions.

Problem 11.8

Solution:

Known quantities:

The threshold voltage, $V_T = 4$ V, of an enhancement-type NMOS. $i_D = 1$ mA when $v_{GS} = v_{DS} = 6$ V.

Find:

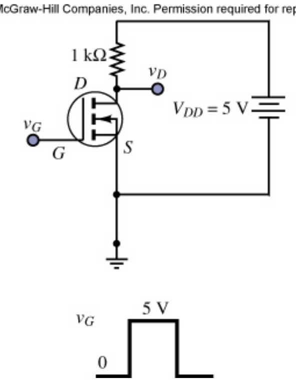
The value of i_D when $v_{GS} = 5$ V.

Analysis:

From $0.001 = k(6 - 4)^2$, we have $k = 0.25\times10^{-3}$

For $v_{GS} = 5$ V, and assuming active operation: $i_D = 0.25\times10^{-3}(5 - 4)^2 = 0.25$ mA.

Problem 11.9



Solution:

Known quantities:

The threshold voltage, $V_T = 1.5$ V, of the NMOS transistor shown in Figure P11.9. $k = 0.4\,\text{mA/V}^2$.

Find:

The voltage levels of the pulse signal at the drain output, if v_G is a pulse with 0 V to 5 V.

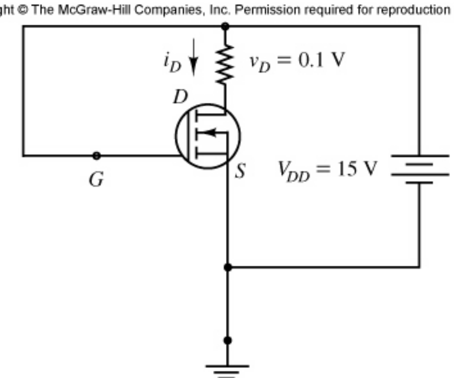
Analysis:

Since $V_T = 1.5$ V, with $v_G = 0$ V, $v_{GS} < V_T$, the transistor is cut off. Therefore, $v_D = 5$ V.

When $v_G = 5$ V, and assuming that the transistor is in the active region:

$i_D = k\,(v_{GS} - V_T)^2 = 0.4\,(5 - 1.5)^2 = 4.9$ mA. Therefore, $v_D = 5 - 4.9\times1 = 0.1$ V.

Problem 11.10



Solution:

Known quantities:

Circuit shown in Figure 11.10.

Find:

Find the current i_D.

Analysis:

In the circuit of Figure P11.10,

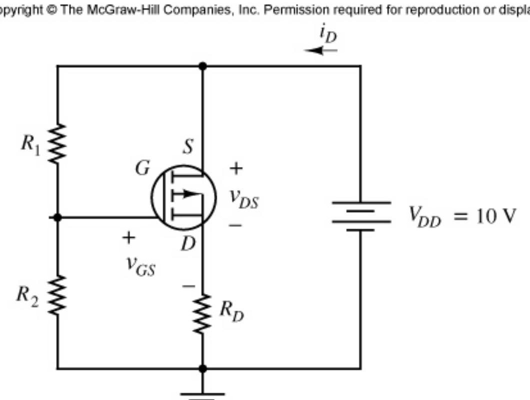
$v_{DS} = 0.1 < v_{GS} - V_T = 14V$,

therefore the transistor is in the ohmic region. We can compute the drain current to be:

$$i_D = K\left[2(v_{GS} - V_T)v_{DS} - v_{DS}^2\right]$$

$$= \ 0.5 \times 10^{-3}\left[2(15\ \text{-}1)\times 0.1\text{-}(0.1)^2\right] = 1.395 \text{ mA}$$

Problem 11.11



Solution:

Known quantities:

In the circuit shown in Figure P11.11, the MOSFET operates in the active region.

Find:

a) R_D

b) The largest allowable value of R_D for the MOSFET to remain in the saturation region.

Analysis:

Since the transistor is in the saturation region and $i_D = 0.5$ mA , we have

$$i_D = K(v_{GS} - V_T)^2$$

$$0.5 = 0.5(v_{GS} + 1)^2$$

and $v_{GS} = -2$ V; $v_{GS} < V_T = -1$. Since the source is at 10 V, the gate voltage must be 8 V. Thus, we can select $R_1 = 1$ MΩ and $R_2 = 4$ MΩ to obtain this operating condition.

(a) R_D can be found to be

$$R_D = \frac{V_D}{i_D} = \frac{8 \text{ V}}{0.5 \text{ mA}} = 16 \text{ k}\Omega$$

(b) Saturation region operation would be maintained when V_D exceeds V_G by $|V_T|$,

$V_{D\max} = 8 + 1 = 9$ V

Therefore,

$$R_{D\max} = \frac{V_{D\max}}{0.5} = 18 \text{ k}\Omega$$

Problem 11.12

Solution:

Known quantities:

An enhancement-type MOSFET has the parameters $K = 0.5 \text{ mA/V}^2$ and $V_T = 1.5 \text{ V}$, and the transistor is operated at $v_{GS} = 3.5 \text{ V}$.

Find:

a) The drain current obtained at $v_{DS} = 3 \text{ V}$.
b) The drain current obtained at $v_{DS} = 10 \text{ V}$.

Analysis:

(a) $V_{DS} = 3 > V_{GS}\text{-}V_T = 3.5\text{-}1.5 = 2 \text{ V}$

$$i_D = K(V_{GS}\text{-}V_T)^2 = 0.5\times10^{-3}\times4 = 2 \text{ mA}$$

(b) $V_{DS} = 10 > V_{GS}\text{-}V_T = 2 \text{ V}$

$$i_D = K(V_{GS}\text{-}V_T)^2 = 0.5\times10^{-3}\times4 = 2 \text{ mA}$$

Section 11.3: MOSFET Amplifiers

Problem 11.13

Solution:

Known quantities:

The *i-v* characteristic of Figure P11.13(a), and the circuit in Figure P11.13(b): $V_{GG} = 7\text{ V}, V_{DD} = 10\text{ V}, R_D = 5\Omega$

Find:

The current i_{DQ} the voltage v_{DSQ}, and the region of operation of the MOSFET.

Analysis:

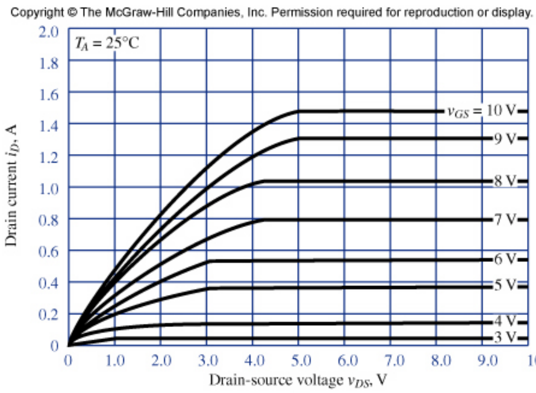
The operating point can be determined using the load line method.

$$i_D = \frac{V_{DD}}{R_D} - \frac{v_{DS}}{R_D} = 2 - 0.2\, v_{DS}$$

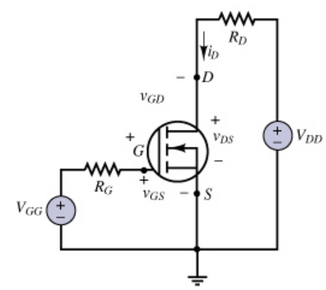
By superimposing the load line on Figure P11.13(a), and by noticing that $V_{GS} = V_{GG} = 7\text{ V}$, we obtain

$$i_{DQ} = 0.8\text{ A}, v_{DSQ} = 6\text{ V}$$

The MOSFET is in the saturation region.



(a)



(b)

Problem 11.14

Solution:

Known quantities:

The circuit in Figure P11.13(b):

$$V_{GG} = 7\text{ V}, V_{DD} = 20\text{ V}, V_T = 3\text{ V}, R_D = 5\Omega, K = 50\text{ mA/V}^2$$

Find:

The current i_{DQ} the voltage v_{DSQ}, and the region of operation of the MOSFET.

Analysis:

Assuming that the MOSFET is in the saturation region, the quiescent drain current is

$$i_{DQ} = K(v_{GSQ} - V_T)^2 = 0.05(7-3)^2 = 0.8\text{ A}$$

The drain-to-source voltage is

$$v_{DSQ} = V_{DD} - R_D i_{DQ} = 20 - 5 \cdot 0.8 = 16\text{ V}$$

Since $v_{DG} = v_{DS} - v_{GS} = 9\text{V} > V_T \Rightarrow$ hypothesis was correct

Problem 11.15

Solution:

Known quantities:

The circuit in Figure 11.9 in the text:

$V_{DD} = 36\text{ V}, V_T = 4\text{ V}, R_D = 10\text{ k}\Omega, R_1 = R_2 = 2\text{ M}\Omega, K = 0.1\text{ mA/V}^2$

Find:

The current i_{DQ}, the voltage v_{DSQ}, the resistance R_S, and the operating region of the MOSFET.

Analysis:

Using Thevenin equivalent,

$$V_{GG} = \frac{R_2}{R_1 + R_2} V_{DD} = 18\text{ V}$$

We can write the equations

$$V_{GG} = v_{GSQ} + R_S i_{DQ} = 18,$$

$$V_{DD} = (R_D + R_S) i_{DQ} + v_{DSQ} = R_D i_{DQ} + 18 - v_{GSQ} + v_{DSQ} = 36 \Rightarrow R_D i_{DQ} + v_{DSQ} = 18 + v_{GSQ}$$

Assuming saturation conditions, the current i_D can be written as

$$i_{DQ} = K(v_{GSQ} - V_T)^2 \Rightarrow v_{GSQ} + R_S K (v_{GSQ} - V_T)^2 = 18$$

and

$$R_D K (v_{GSQ} - V_T)^2 + v_{DSQ} = 18 + v_{GSQ}$$

Notice that the problem has more unknown than equations; we can impose the v_{DSQ} to ensure saturation conditions as

$$v_{DSQ} = V_{DD}/2 = 18\text{ V} \Rightarrow$$

$$(v_{GSQ} - V_T)^2 = v_{GSQ} \Rightarrow v_{GSQ}^2 - 9 v_{GSQ} + 16 = 0 \Rightarrow v_{GSQ} = 6.56\text{ V}$$

Remark: The other solution of the algebraic equation is not acceptable because $< V_T$.

The resistance R_S is given by

$$R_S = \frac{18 - v_{GSQ}}{K(v_{GSQ} - V_T)^2} = \frac{18 - 6.56}{0.1 \cdot 10^{-3}(6.56 - 4)^2} = 17.45\text{ k}\Omega$$

and the drain current

$$i_{DQ} = K(v_{GSQ} - V_T)^2 = 0.655\text{ mA}$$

Problem 11.16

Solution:

Known quantities:

The circuit in Figure P11.16:

$V_{DD} = 12\,\text{V}, V_T = 1\text{V}, R_S = R_D = 10\,\text{k}\Omega, R_1 = R_2 = 2\,\text{M}\Omega, K = 1\text{mA/V}^2$

Find:

The current i_{DQ}, the voltage v_{DSQ}, and the voltage v_{GSQ}.

Analysis:

Using Thevenin,

$$V_{GG} = \frac{R_2}{R_1 + R_2} V_{DD} = 6\text{ V}$$

We can write the equations

$$V_{GG} = v_{GSQ} + R_S i_{DQ} = 6,$$

$$V_{DD} = (R_D + R_S) i_{DQ} + v_{DSQ} = 2R_D i_{DQ} + v_{DSQ} = 12$$

Assuming saturation conditions, the current i_D can be written as

$$i_{DQ} = K(v_{GSQ} - V_T)^2 \Rightarrow v_{GSQ} + R_S K(v_{GSQ} - V_T)^2 = 6 \Rightarrow 10v_{GSQ}^2 - 19v_{GSQ} + 4 = 0 \Rightarrow$$

$$v_{GSQ} = 1.66\text{ V}$$

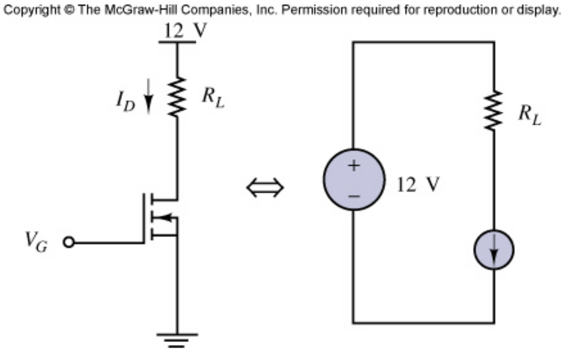
The other solution is not acceptable because less then V_T.

It follows

$$i_{DQ} = \frac{6 - v_{GSQ}}{R_S} = 0.434\text{ mA},$$

$$v_{DSQ} = 12 - 2R_D i_{DQ} = 3.32\text{ V}$$

Problem 11.17



Solution:

Known quantities:

The power MOSFET circuit shown in Figure P11.17.

Find:

a) If $V_G = 5$ V, find the range of R_L for which the VCCS will operate.
b) If $R_L = 1\,\Omega$, determine the range of V_G for which the VCCS will operate.

Analysis:

The MOSFET should be working in the saturation region, so $v_{GD} < 3 \Rightarrow V_D > V_G - 3$

a) $V_G = 5$ V, $I_D = K(v_{GS} - V_T)^2 = 1.5(5-3)^2 = 6$ A so

$V_D = 12 - R_L I_D > V_G - 3 = 2 \Rightarrow R_L < \frac{10}{6}\,\Omega$

b) $V_D = 12 - R_L I_D > V_G - 3 \Rightarrow V_G < 9 - R_L I_D = 9 - I_D$

$I_D = K(v_{GS} - V_T)^2 = K(V_G - V_T)^2$

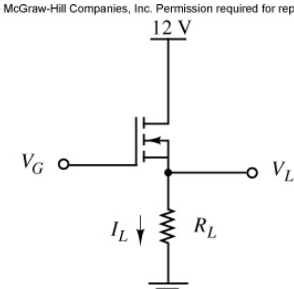
Solve the above two equations, we can have

$I_D = 8.36\ A$ or $I_D = 4.31\ A$

Obviously, the second one is reasonable, so

$V_G < 9 - I_D = 4.69$ V

Problem 11.18



Solution:

Known quantities:

The circuit in Figure P11.18:

Find:

a) Determine I_L if

$V_{DD} = 12\,\text{V}, V_G = 10\,\text{V}, V_T = 4\,\text{V}, R_L = 2\,\Omega, K = 0.5\,\text{A/V}^2$

b) If the power rating of the MOSFET is 50 W, how small can R_L be.

Analysis:

a) Since $v_{GD} = 10 - 12 < V_T = 4$ V, MOSFET is working in the saturation region

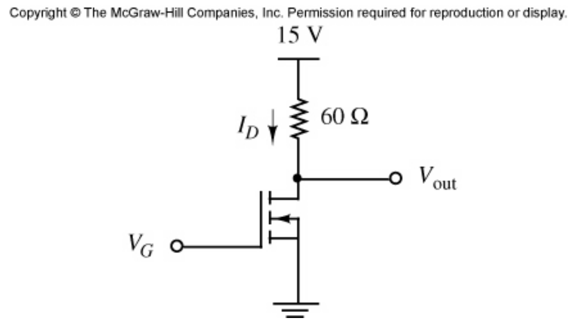
$V_L = V_G - V_T = 10 - 4 = 6$ V

So $I_L = \frac{V_L}{R_L} = \frac{6}{2} = 3$ A

b) $P_{\max} = v_{DS} I_D = 50\text{ W} \Rightarrow I_{L\max} = I_D = \frac{P_{\max}}{v_{DS}} = \frac{50}{12-6} = 8.33$ A

So, $R_{L\min} = \frac{V_L}{I_{L\max}} = \frac{6}{8.33} = 0.72\,\Omega$

Problem 11.19



Solution:

Known quantities:

The Class A amplifier shown in Figure P11.19

Find:

c) Determine the output current for the given biased audio tone input, $V_G = 10 + 0.1\cos(500t)$ V. Let $K = 2$ mA/V^2 and $V_T = 3$ V.

d) Determine the output voltage.

e) Determine the voltage gain of the $\cos(500t)$ signal.

f) Determine the DC power consumption of the resistor and the MOSFET.

Analysis:

a) The MOSFET should be working at the saturation region

So $i_D = K(v_{GS} - V_T)^2 = 0.002(10 + 0.1\cos(500t) - 3)^2 = 0.002\left(49 + 1.4\cos(500t) + 0.01\cos^2(500t)\right)$

$= 0.002(49 + 1.4\cos(500t) + 0.005\cos(1000t) + 0.005)$ A

b) $V_{out} = V_{DD} - i_D R = 15 - 60 \times 0.002(49 + 1.4\cos(500t) + 0.005\cos(1000t) + 0.005)$ V

c) $gain = \left.\dfrac{V_{out}}{V_G}\right|_{\omega=500} = \dfrac{-60 \times 0.002 \times 1.4}{0.1} = -1.68$

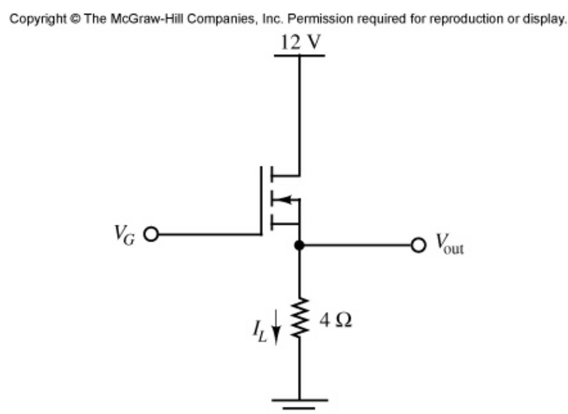
d) We can ignore the cosine part signal when calculating the DC power consumption.

$i_{D\_DC} = 0.002(49 + 0.005) = 0.098$ A

$P_R = i_{D\_DC}{}^2 \times R = 0.576$ W

$P_{MOSFET} = i_{D\_DC} \times v_{DS} = i_{D\_DC} \times (V_{DD} - i_{D\_DC} \times R) = 0.098 \times (15 - 0.098 \times 60) = 0.894$ W

Problem 11.20



Solution:

Known quantities:

The source-follower amplifier shown in Figure P11.20.

$V_G = 9 + 0.1\cos(500t)$ V, $K = 30$ mA/V^2 and $V_T = 4$ V

Find:

a) Determine the load current I_L.

b) Determine the output voltage.

c) Determine the voltage gain of the $\cos(500t)$ signal.

d) Determine the DC power consumption of the resistor and the MOSFET.

Analysis:

The MOSFET should be working at the saturation region, So the $V_{out} = V_S = v_{GS} - V_T = 5 + 0.1\cos(500t)$

a) $I_L = \dfrac{V_{out}}{R} = \dfrac{5 + 0.1\cos(500t)}{4} = 1.25 + 0.025\cos(500t)$

c) $gain = \left.\dfrac{V_{out}}{V_G}\right|_{\omega=500} = \dfrac{0.1}{0.1} = 1$

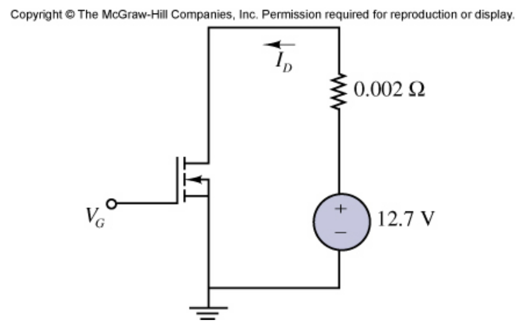
d) We can ignore the cosine part signal when calculating the DC power consumption.

$i_{D\_DC} = 1.25$ A

$P_R = i_{D\_DC}{}^2 \times R = 6.25$ W

$P_{MOSFET} = i_{D\_DC} \times v_{DS} = i_{D\_DC} \times (V_{DD} - i_{D\_DC} \times R) = 1.25 \times (12-5) = 8.75$ W

Problem 11.21



Solution:

Known quantities:

The circuit shown in Figure P11.21.

$V_G = 8$ V , $K = 4$ A/V^2 and $V_T = 3$ V

Find:

The discharging current I_D and the required MOSFET power rating.

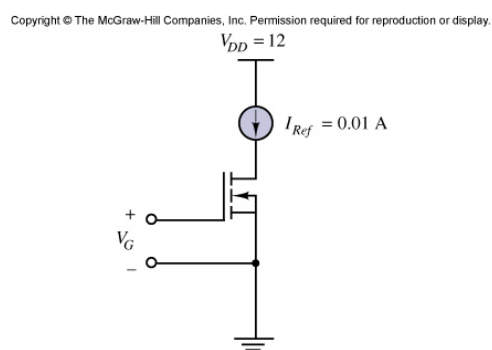
Analysis:

Obviously, the MOSFET should be working in the saturation region.

$i_D = K(v_{GS} - V_T)^2 = 4(8-3)^2 = 100$ A

$P = v_{DS} \times i_D = (12.7 - R \times i_D) \times i_D = (12.7 - 0.002 \times 100) \times 100 = 1250$ W

Problem 11.22



Note: the value of K should be 0.006 A/V^2, not mA/V^2.

Solution:

Known quantities:

The circuit shown in Figure P11.22.

Find:

Determine the output V_G .

Analysis:

Obviously, the MOSFET should be working in the saturation region.

$i_D = K(v_{GS} - V_T)^2$

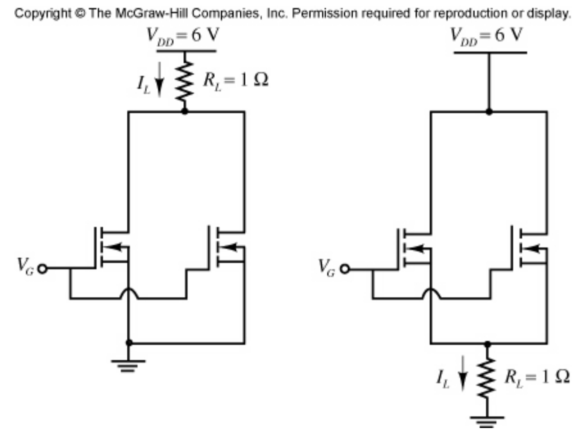
$$V_G = V_T + \sqrt{\frac{i_D}{K}} = 1.5 + \sqrt{\frac{0.01}{0.006 \times 10^{-3}}} = 1.5 + 1.29 = 2.79 \text{ V}$$

Problem 11.23

Solution:

Known quantities:

The circuit shown in Figure P11.23.



Find:

Determine the load current in each of the circuits.

Analysis:

a) In the figure of left hand side, resistance is connected to the drain

Assume that the drain current in each MOSFET is i_D, then the current through the resistance is $2i_D$

Obviously, the MOSFET is working at the saturation region, so

$i_D = K(v_{GS} - V_T)^2 = K(V_G - V_T)^2$

And $v_{GD} = V_G - V_D = V_G - V_{DD} + I_L R_L < V_T$

Solve the equations above, we can get the current

b) In the figure of right hand side, resistance is connected to the source

Assume that the drain current in each MOSFET is i_D, then the current through the resistance is $2i_D$

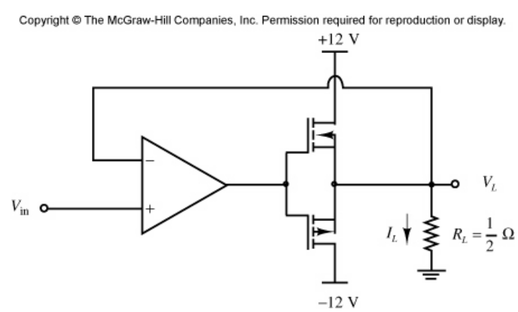
Obviously, the MOSFET is working in the saturation region, so

$i_D = K(v_{GS} - V_T)^2 = K(V_G - I_L R_L - V_T)^2$

And $v_{GD} = V_G - V_D = V_G - V_{DD} < V_T$, and $v_{GS} = V_G - V_S = V_G - I_L R_L > V_T$

Solving the equations above, we can get the current

Problem 11.24



Solution:

Known quantities:

A "push-pull amplifier" can be constructed from matched n-and-p-channel MOSFETs, shown in Figure P11.24.

Find:

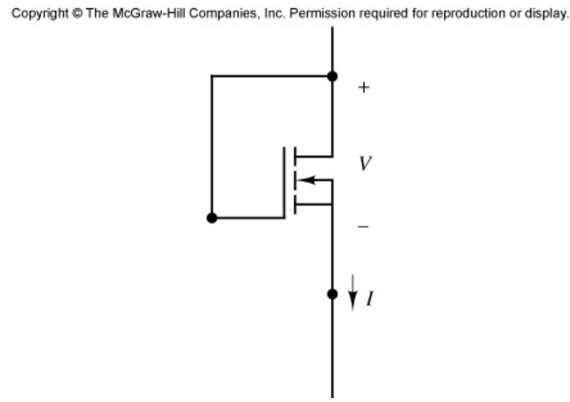
Determine V_L and I_L.

Analysis:

If $V_L < V_{in}$, the output of the operational amplifier is positive infinity, so both MOSFETs will work in the triode region and the V_L will increase, until it reaches $V_L = V_{in}$;

If $V_L > V_{in}$, the output of the operational amplifier is negative infinity, so both two MOSFET will work in cutoff region, and the V_L will increase, until it reaches $V_L = V_{in}$; So $V_L = V_{in}$ is the only equilibrium in the system, so $V_L = V_{in}$. Correspondingly, $I_L = \frac{V_L}{R_L} = 2V_L$

Problem 11.25



Solution:

Known quantities:

The circuit shown in Figure 11.25.

Find:

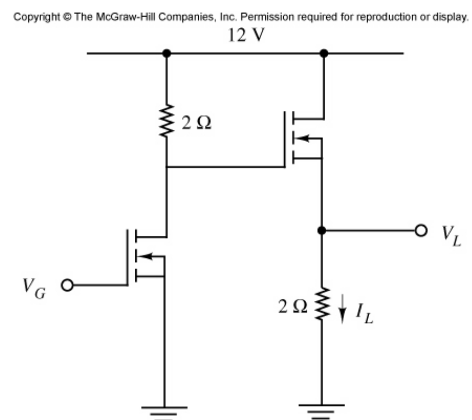
Determine the V – I characteristics of the voltage controlled resistance.

Analysis:

Since the gate is connected to the drain, the MOSFET can either work in the saturation region or cutoff region, dependant on whether $V_G \ge V_S$

So, $I = \begin{cases} K(V - V_T)^2, & V \ge V_T \\ 0, & V < V_T \end{cases}$

Problem 11.26



Solution:

Known quantities:

The two-stage amplifier shown in the circuit of Figure P11.26.

Find:

a) Determine the V_L and I_L for $V_G = 4$ V
b) Determine the V_L and I_L for $V_G = 5$ V
c) Determine the V_L and I_L for $V_G = 4 + 0.1\cos(750t)$ V

Analysis:

Assume the drain current in the MOSFET in the left hand side is i_{D1} and in the right hand side i_{D2}. Obviously, both MOSFET are working in saturation region.

a) $i_{D1} = K(v_{GS1} - V_T)^2 = K(V_{G1} - V_T)^2 = 1$ A

$V_{G2} = V_{D1} = V_{DD} - R \times i_{D1} = 12 - 2 \times 1 = 10$ V

$i_{D2} = K(v_{GS2} - V_T)^2 = K(V_{G2} - R \times i_{D2} - V_T)^2$

Solve it and we can have $i_{D2} = 2.68$ or 4.57 A

Obviously, the first solution is reasonable, so $I_L = i_{D2} = 2.68$ A and $V_L = R \times I_L = 5.36$ V

b) $i_{D1} = K(v_{GS1} - V_T)^2 = K(V_{G1} - V_T)^2 = 4$ A $\quad V_{G2} = V_{D1} = V_{DD} - R \times i_{D1} = 12 - 2 \times 4 = 4$ V

$i_{D2} = K(v_{GS2} - V_T)^2 = K(V_{G2} - R \times i_{D2} - V_T)^2$ Solve it and we can have $i_{D2} = 0.25$ or 1 A

Obviously, the first solution is reasonable, so $I_L = i_{D2} = 0.25$ A and $V_L = R \times I_L = 0.5$ V

c) Basically, the signal in c) part is a comparably small cosine signal superposed by the signal the in a) part. If we ignore the harmonics larger than 1st order, we can approximately have the following solution

$i_{D1} = 1 - 0.2\cos(750t)$ A $\qquad V_{G2} = 10 + 0.4\cos(750t)$ V

$I_L = i_{D2} = 2.68 - 1.31\cos(750t)$ A $\qquad V_L = 5.36 - 2.62\cos(750t)$ V

Section 11.4: MOSFET Switches

Problem 11.27

Solution:

Known quantities:

The CMOS NAND gate of Figure 11.23 in the text.

Find:

Identify the state of each transistor for $v_1 = v_2 = 5$ V.

Analysis:

The two transistors at the top are cut off and the two at the bottom are on.

Problem 11.28

Solution:

Known quantities:

The CMOS NAND gate of Figure 11.23 in the text.

Find:

Identify the state of each transistor for v_1=5V, v_2=0V.

Analysis:

The transistor at the bottom and the first on the top are off, the other two are on.

Problem 11.29

Solution:

Find:

Draw the schematic diagram of a two-input CMOS OR gate.

Analysis:

The output of the circuit of Figure 11.18 is connected as an input to the circuit of Figure 11.14.

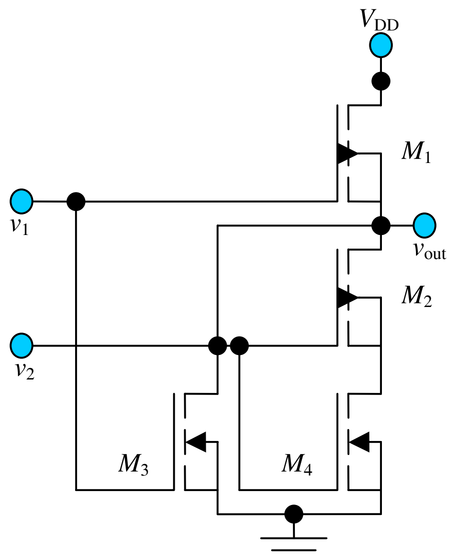


Figure 11.18

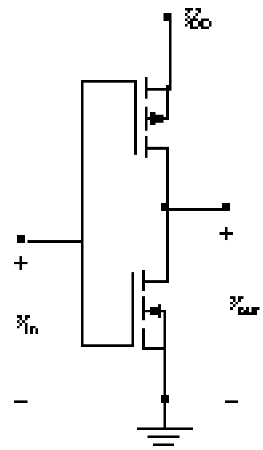


Figure 11.14

Problem 11.30

Solution:

Find:

Draw the schematic diagram of a two-input CMOS AND gate.

Analysis:

The output of the circuit of Figure 11.21 in the text is connected as an input to the circuit of Figure 11.14.

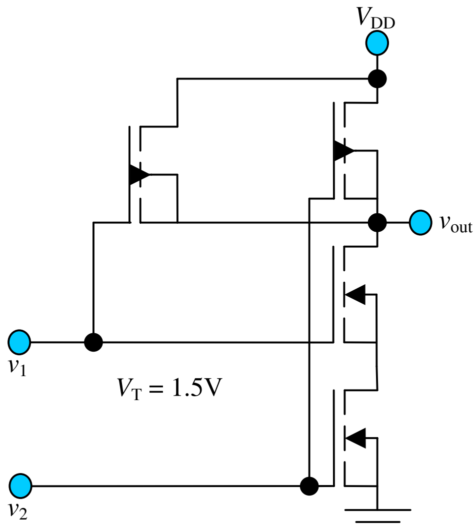


Figure 11.21

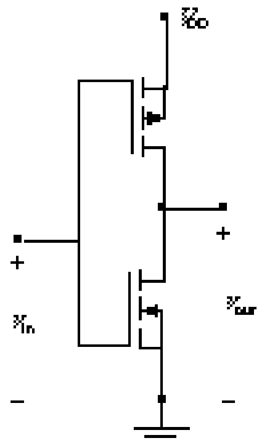


Figure 11.14

Problem 11.31

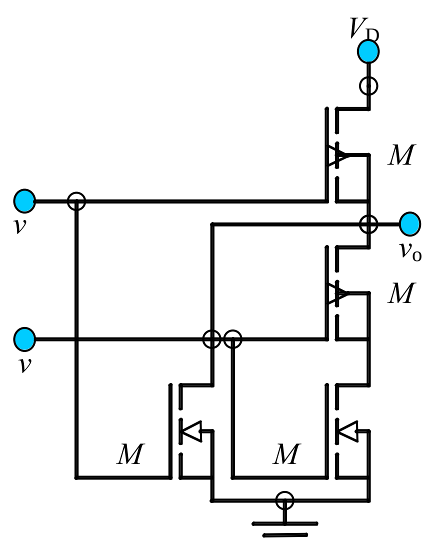
Solution:

Find:

Draw the schematic diagram of a two-input CMOS NOR gate.

Known quantities:

The circuit of Figure 11.18



Figure

Problem 11.32

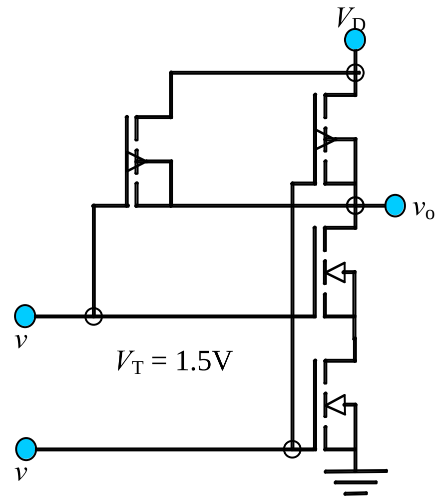
Solution:

Find:

Draw the schematic diagram of a two-input CMOS NAND gate.

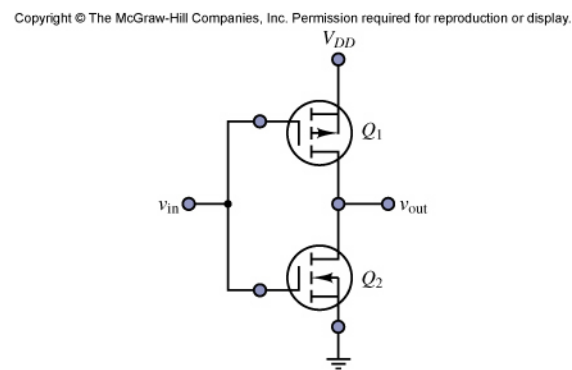
Known quantities:

The circuit of Figure 11.21, in the text.



Figure

Problem 11.33



Solution:

Known quantities:

The circuit of Figure P11.33.

Find:

Show that the given circuit functions as a logic inverter.

Analysis:

Construct a state table:

v_{in}	Q_1	Q_2	v_{out}
low	resistive	open	high
high	open	resistive	low

This table clearly describes an inverter.

Problem 11.34

Solution:

Known quantities:

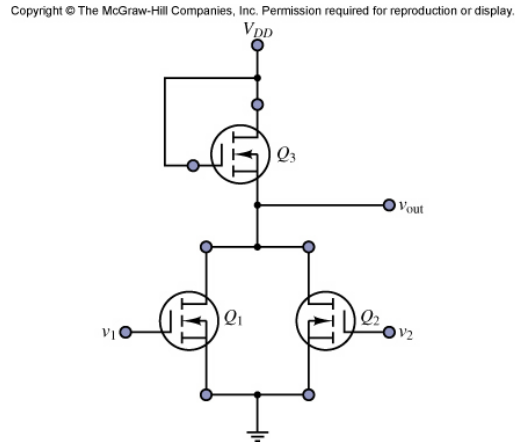
The circuit of Figure P11.34.

Find:

Show that the given circuit functions as a NOR gate.

Analysis:

Construct a state table:



v_1	v_2	Q_1	Q_2	v_{out}
0	0	off	off	high
0	high	off	on	low
high	0	on	off	low
high	high	on	on	low

This table clearly describes a NOR gate.

Problem 11.35

Solution:

Known quantities:

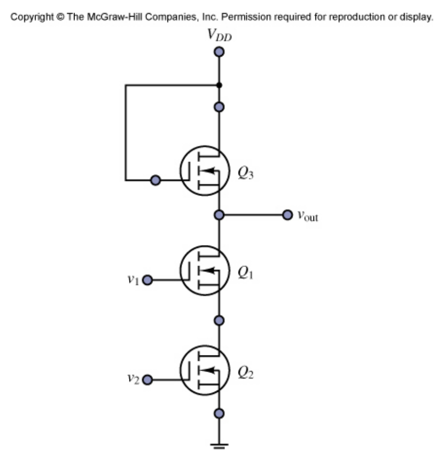
The circuit of Figure P11.35.

Find:

Show that the given circuit functions as a NAND gate.

Analysis:

Construct a state table:



v_1	v_2	Q_1	Q_2	v_{out}
0	0	off	off	high
0	high	off	on	high
high	0	on	off	high
high	high	on	on	low

This table clearly describes a NAND gate.