the temperature is (a) 310 K, (b) 316 K, and (c) 284 K.

6.23 A germanium diode is forward biased at 0.5 A and 0.3 V at 300 K. Find the saturation current of the diode for the case that the temperature is (a) 300 K, (b) 310 K, (c) 324 K, and (d) 276 K.

6.24 A germanium diode with a saturation current of 4 μA at 300 K has a forward-bias current of 0.5 A. Find the voltage across the diode for the case that the temperature is (a) 310 K, (b) 324 K, and (c) 276 K.

6.25 For the diode circuit shown in Fig. P6.25, $V_S = 2$ V and the silicon diode has a saturation current of 1 nA at 300 K. Given that $v = 0.7$ V, find (a) R_2 when $R_1 = 1$ kΩ, and (b) R_1 when $R_2 = 1$ kΩ.

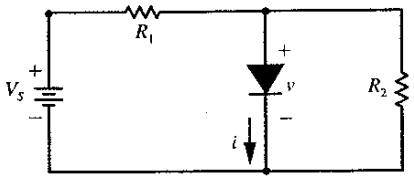


Fig. P6.25

6.26 For the diode circuit shown in Fig. P6.25, $V_S = 2$ V and the silicon diode has a saturation current of 1 nA at 300 K. Given that $i = 0.5$ mA, find (a) R_2 when $R_1 = 1$ kΩ, and (b) R_1 when $R_2 = 1$ kΩ.

6.27 For the diode circuit shown in Fig. P6.27, $V_S = 1.5$ V and the silicon diodes have a temperature of 300 K. Given that $v_2 = 0.7$ V, find (a) I_{S1} when $R = 100$ Ω and $I_{S2} = 1$ nA, and (b) R when $I_{S1} = I_{S2} = 1$ nA.

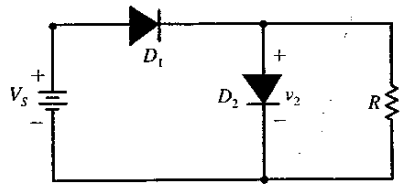


Fig. P6.27

6.28 For the diode circuit shown in Fig. P6.28, $V_S = 3$ V and the silicon diodes have a saturation current of 10 nA at 300 K. (a) Find R_1 for the case that $R_2 = 850$ Ω and $i_2 = 2$ mA. (b) Find R_2 for the case that $R_1 = 1$ kΩ and $i_1 = 5$ mA.

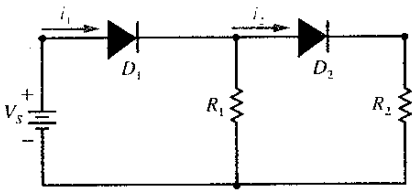


Fig. P6.28

6.29 For the diode circuit shown in Fig. P6.29, $V_S = 6$ V and the silicon diodes have a saturation current of 1 nA at 300 K. (a) Find R_2 for the case that $R_1 = 10$ kΩ and $v_1 = 0.66$ V. (b) Find R_1 for the case that $R_2 = 100$ Ω and $v_2 = 0.66$ V. (c) Find R_1 and R_2 for the case that $v_1 = 0.68$ V and $v_2 = 0.66$ V.

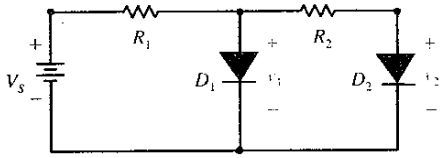


Fig. P6.29

6.30 For the diode circuit given in Fig. 6.17, on p. 371, D_1 is silicon with a saturation current of 5 nA and D_2 is germanium with a saturation current of 10 μA. Find v_1 and v_2 at 300 K.

6.31 For the diode circuit shown in Fig. P6.31, D_1 and D_2 are silicon diodes with saturation currents of 5 nA and 10 nA, respectively, at 300 K. Given that both diodes are reverse biased, find v_1 and v_2.

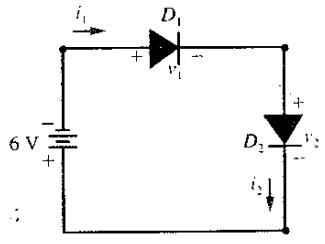


Fig. P6.31

6.32 For the diode circuit shown in Fig. P6.32, D_1 and D_2 are silicon diodes having saturation currents of 5 nA and 10 nA, respectively, at 300 K. Given that both diodes are forward biased, find the value of R for which the current is 15 mA.

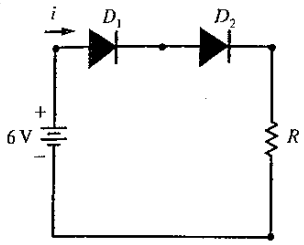


Fig. P6.32

6.33 A germanium diode has a saturation current of 20 μA at 300 K.
(a) Plot an i-v characteristic curve on a piece of graph paper.
(b) Suppose that this diode is used in the circuit given in Fig. 6.16*a*, on p. 368, where $v_1 = 1$ V and $R = 0.5$ Ω. Use the i-v curve obtained in part (a) to graphically determine i and v.

6.34 A germanium diode has a saturation current of 20 μA at 300 K. Suppose that this diode is used in the circuit given in Fig. 6.16*a* on p. 368, where $v_1 = 1$ V and $R = 0.5$ Ω. Use the numerical method described in Example 6.7 on p. 369 to find i and v. (Begin with $v = 0.2$ V.)

6.35 A silicon diode has a saturation current of 10 nA at 300 K.
(a) Plot an i-v characteristic curve on a piece of graph paper.
(b) Suppose that this diode is used in the circuit given in Fig. 6.16*a*, on p. 368, where $v_1 = 1$ V and $R = 100$ Ω. Use the i-v curve obtained in part (a) to determine graphically i and v.

6.36 A silicon diode has a saturation current of 10 nA at 300 K. Suppose that this diode is used in the circuit given in Fig. 6.16*a*, on p. 368, where $v_1 = 1$ V and $R = 100$ Ω. Use the numerical method described in Example 6.7 on p. 369 to find i and v. (Begin with $v = 0.5$ V.)

6.37 Given that the input voltage is $v_S = A \sin \omega t$ V, sketch the resulting output voltage v_o for the ideal-diode circuit shown in Fig. P6.37.

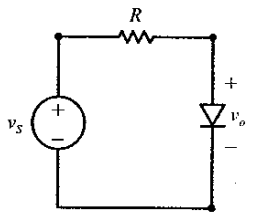


Fig. P6.37

6.38 The input voltage to the clipper circuit shown in Fig. P6.38 is $v_S = 12 \sin \omega t$ V. Determine the output voltage v_o and sketch this function.

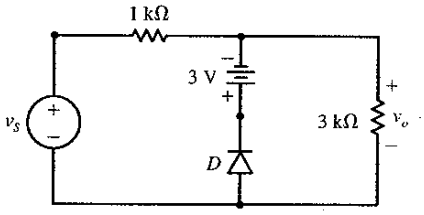


Fig. P6.38

6.39 For the ideal-diode circuit given in Fig. P6.38, reverse the polarity of the 3-V source. The input voltage to the resulting clipper circuit is $v_S = 12 \sin \omega t$ V. Determine the output voltage v_o and sketch this function.

6.40 The input voltage to the clipper circuit shown in Fig. P6.40 is $v_S = 6 \sin \omega t$ V. Determine the output voltage v_o and sketch this function.

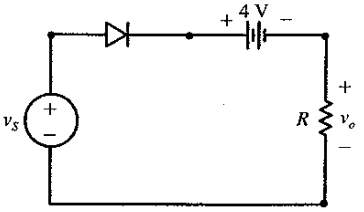


Fig. P6.40

$$v = \eta V_T \ln\left(\frac{i}{I_S} + 1\right) = 2\left(\frac{316}{11{,}586}\right) \ln\left(\frac{7.42 \times 10^{-3}}{30.3 \times 10^{-9}} + 1\right)$$

$$= 0.677 \approx 0.66 \text{ V}$$

Drill Exercise 6.6

Given that the current through a 1N4153 silicon diode is 10 mA, find the voltage across the diode when the temperature is (a) 290 K, (b) 310 K, (c) 320 K.

ANSWER (a) 0.726 V; (b) 0.70 V; (c) 0.687 V

Diode Circuits

Now let us look at the diode circuit shown in Fig. 6.16*a*. We can attempt to analyze this circuit by writing some equations, and begin with the equation relating the current and voltage for the diode:

$$i = I_S(e^{v/\eta V_T} - 1) \tag{6.21}$$

where it is assumed that I_S, η, and T are given. By KVL, we can also write

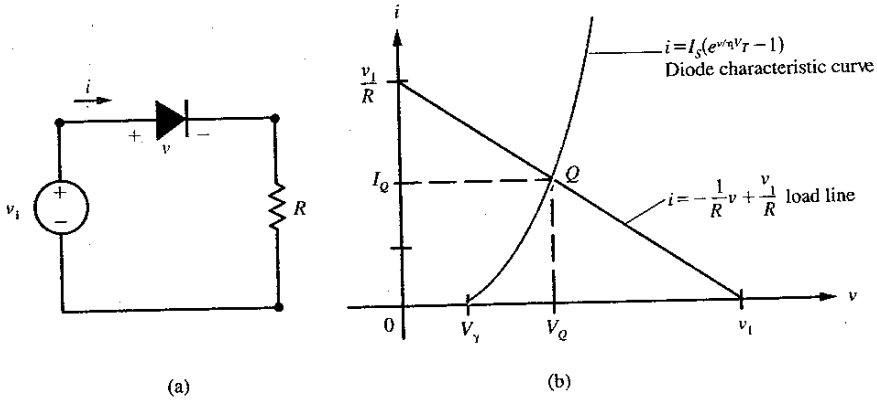


Fig. 6.16 (*a*) Diode circuit, and (*b*) graphical analysis of given diode circuit.

6.51 Sketch the i-v characteristic of the ideal-diode circuit shown in Fig. P6.51 for the case that that $I_S > 0$ A, $R_f = 0\ \Omega$, and $V_\gamma = 0$ V.

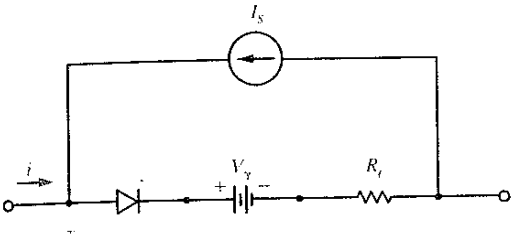


Fig. P6.51

6.52 Sketch the i-v characteristic of the ideal-diode circuit shown in Fig. P6.51 for the case that $I_S > 0$ A, $R_f > 0\ \Omega$, and $V_\gamma = 0$ V.

6.53 Sketch the i-v characteristic of the ideal-diode circuit shown in Fig. P6.51 for the case that $I_S > 0$ A, $R_f = 0\ \Omega$, and $V_\gamma > 0$ V.

6.54 Sketch the i-v characteristic of the ideal-diode circuit shown in Fig. P6.51 for the case that $I_S > 0$ A, $R_f > 0\ \Omega$, and $V_\gamma > 0$ V.

6.55 Sketch the i-v characteristic of the ideal-diode circuit shown in Fig. P6.55 for the case that $V_Z > 0$ V and $R_Z = 0\ \Omega$.

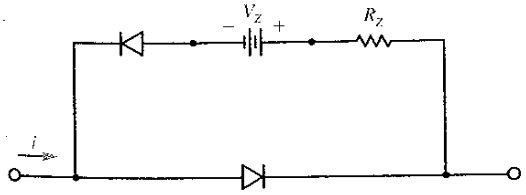


Fig. P6.55

6.56 Sketch the i-v characteristic of the ideal-diode circuit shown in Fig. P6.55 for the case that $V_Z > 0$ V and $R_Z > 0\ \Omega$.

6.57 For the DL AND gate given in Fig. 6.48, on p. 391, suppose that $R_2 = 10$ kΩ, the low voltage is 2 V, and the high voltage is 8 V. Assume that a forward-biased diode has a voltage of 0.7 V, and determine the range of values of R_1 required for proper operation.

6.58 The circuit shown in Fig. P6.58 is a DL OR gate. Suppose that $R_2 = 2$ kΩ, the low voltage is 2 V, and the high voltage is 8 V. Assume that a forward-biased diode has a voltage of 0.7 V, and determine the range of values of R_1 required for proper operation.

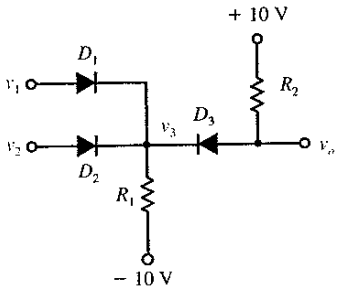


Fig. P6.58

6.59 The circuit shown in Fig. P6.58 is a DL OR gate. Suppose that $R_1 = 2$ kΩ, the low voltage is 2 V, and the high voltage is 8 V. Assume that a forward-biased diode has a voltage of 0.7 V, and determine the range of values of R_2 required for proper operation.

6.60 For the half-wave rectifier circuit given in Fig. 6.20, on p. 373, replace the ideal diode with a diode having $R_f = 20\ \Omega$ and $V_\gamma = 0.6$ V (see Fig. 6.42 on p. 388). Sketch the output voltage v_o, labeling it sufficiently, for the case that the input voltage is $v_S = 6 \sin \omega t$ V and $R = 100\ \Omega$.

6.61 For the diode circuit shown in Fig. P6.61, D_1 is germanium with $R_f = 10\ \Omega$ and $V_\gamma = 0.2$ V whereas D_2 is silicon with $R_f = 10\ \Omega$ and $V_\gamma = 0.6$ V. Find the range of values of v_S for which (a) D_1 and D_2 are both OFF; (b) D_1 and D_2 are both ON; and (c) D_1 is ON and D_2 is OFF.

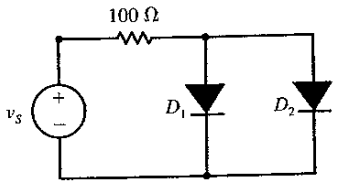


Fig. P6.61

Example 6.9

Given the ideal-diode circuit shown in Fig. 6.20, let us first consider the case of a positive input voltage, that is, $v_S > 0$ V. Since current goes through a resistor from a given potential to a lower potential, let us assume that D is ON. Replacing D by a short circuit, we get the circuit shown in Fig. 6.21. By Ohm's law, we have that $i = v_S/R$. Since $v_S > 0$ V, then $i > 0$ A, and the assumption that D is ON is confirmed.

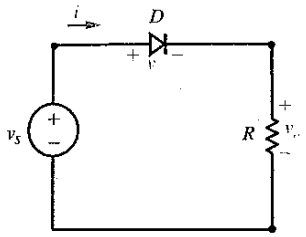


Fig. 6.20 An ideal-diode circuit.

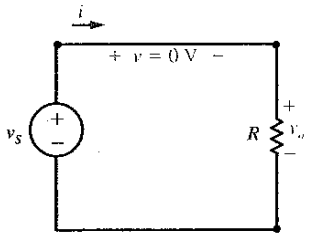


Fig. 6.21 Ideal-diode circuit with D assumed ON.

Next consider the case that $v_S \leq 0$ V. For this situation, let us assume that D is OFF. Replacing D by an open circuit yields the circuit shown in Fig. 6.22. Since $i = 0$ A, by KVL, $v = v_S - Ri = v_S$. Since $v_S \leq 0$ V, then $v \leq 0$ V and our assumption that D is OFF is confirmed.

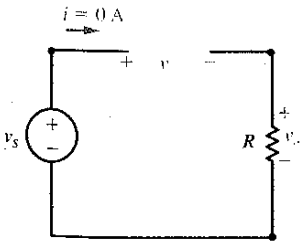


Fig. 6.22 Diode circuit with D assumed OFF.

From this discussion, $v_S > 0$ V, then the output voltage is $v_o = v_S$. When $v_S \leq 0$ V, then $v_o = Ri = 0$ V. Therefore, the output voltage v_o is given by

$$v_o = \begin{cases} 0 \text{ V} & \text{for } v_S \leq 0 \text{ V} \\ v_S & \text{for } v_S > 0 \text{ V} \end{cases}$$

tional purposes.) The equation of the solid line has the form $i = mv + b$, where m is the slope (i.e., $m = 1/R_f$) and b is the vertical-axis intercept (i.e., $b = -a$). Thus we have

$$i = \frac{1}{R_f} v - a \tag{6.33}$$

However, from Fig. 6.40, we see that the slope is $1/R_f = a/V_\gamma$. Thus, $a = V_\gamma/R_f$, and substituting this fact into Eq. 6.33 yields

$$i = \frac{1}{R_f} v - \frac{V_\gamma}{R_f} \quad \Rightarrow \quad v = V_\gamma + R_f i \tag{6.34}$$

It is easy to see that these equivalent relationships between current i and voltage v are realized by the series connection shown in Fig. 6.41. In other words, a forward-biased diode behaves approximately as a series connection of a battery V_γ and a resistance R_f, where V_γ is the cut-in voltage of the diode and R_f is a typical ac resistance of the diode. If the diode is reverse biased, it behaves approximately as an open circuit. Thus a diode model more accurate than the one shown in Fig. 6.38*b* is the one shown in Fig. 6.42*b*—it consists of an ideal diode, a battery V_γ, and a resistance R_f. For this situation, however, the diode is OFF if $v \leq V_\gamma$. As before, though, the diode is ON if $i > 0$ A. (For an even more accurate model, see Problem 6.54 at the end of this chapter.)

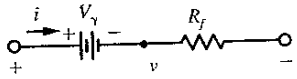
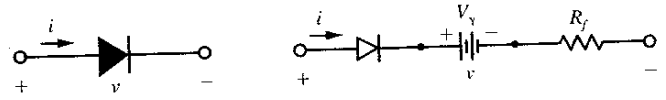


Fig. 6.41 Realization of $v = V_\gamma + R_f i$.



(a) Diode (b) Diode model using battery

Fig. 6.42 A diode and an accurate model.

Example 6.12

Let us demonstrate that the i-v characteristic of the ideal-diode connection shown in Fig. 6.43*a*, where $V_Z > 0$ V, is depicted in Fig. 6.43*b*. We shall solve this problem by considering all possibilities for the states of the diodes.

6.62 For the circuit given in Fig. 6.50, on p. 395, reverse D_1. The identical silicon Zener diodes have saturation currents of 10 nA at 300 K. Find i, v_1, and v_2 when $V_S = 6$ V and the breakdown voltage of the diodes is (a) 9 V and (b) 5 V.

6.63 For the Zener diode circuit shown in Fig. P6.63, at 300 K the germanium diodes D_1 and D_2 have saturation currents of 1 μA and 2 μA, respectively. If both diodes have a breakdown voltage of 10 V, find v_1 and v_2 when V_S is (a) 6 V and (b) 12 V.

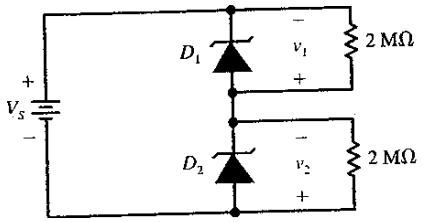


Fig. P6.63

6.64 The Zener diode in the voltage-regulator circuit given in Fig. 6.51 on p. 396 has a breakdown voltage of 9 V and is to operate with a reverse current between 10 and 100 mA. Given that $R = 200\ \Omega$,
(a) Find the range of the load resistance R_L that results in a 9-V load voltage when $v_S = 24$ V.
(b) Find the range of the supply voltage v_S that results in a 9-V load voltage when $R_L = 600\ \Omega$.

6.65 The Zener diode in the voltage-regulator circuit given in Fig. 6.51 on p. 396 has a breakdown voltage of 12 V. Suppose that the diode (reverse) current is to be 10 mA.
(a) If $v_S = 24$ V and $R_L = 2$ kΩ, find R.
(b) If $R = 2$ kΩ and $R_L = 2$ kΩ, find v_S.
(c) If $v_S = 24$ V and $R = 300\ \Omega$, find R_L.

6.66 Repeat Problem 6.65 using the Zener diode model given in Fig. 6.52*c*, on p. 398, where $R_Z = 200\ \Omega$.

6.67 The circuit shown in Fig. P6.67 contains a 6-V Zener diode, that is, a diode with a breakdown voltage of 6 V. Suppose that the supply voltage v_S is a half-wave rectified sine wave (see Fig. 6.23*b* on p. 374) with an amplitude of 12 V. (a) Use the ideal Zener diode model given in Fig. 6.52*b* on p. 398 to obtain a sketch of v_L. (b) Use the model given in Fig. 6.52*c* with $R_Z = 100\ \Omega$ to obtain a sketch of v_L.

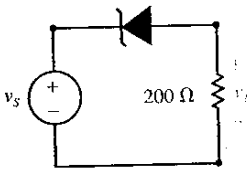


Fig. P6.67

6.68 The Zener diode in the voltage-regulator circuit given in Fig. 6.51 on p. 396 has a breakdown voltage of 9 V. Suppose that the diode has a resistance of 100 Ω in the breakdown state and the diode is to operate with a reverse current between 10 and 100 mA. Find the range of v_S for the case that $R = 200\ \Omega$ and $R_L = 600\ \Omega$.

6.69 The Zener diode in the voltage-regulator circuit given in Fig. 6.51 on p. 396 has a breakdown voltage of 9 V. Suppose that the diode has a resistance of 100 Ω in the breakdown state and the diode is to operate with a reverse current between 10 and 100 mA. Find the range of R_L for the case that $R = 200\ \Omega$ and $v_S = 24$ V.

6.70 Sketch the i-v characteristic for each connection of elements shown in Fig. P6.70, where the breakdown voltage of an ideal Zener diode is V_Z. (See p. 415.)

6.71 For the circuit shown in Fig. 6.54, on p. 399, replace the ideal Zener diode D_1 with an (ordinary) ideal diode having the same orientation. Given that the breakdown voltage for D_2 is 12 V, sketch v_o for the case that $v_S = 24 \sin \omega t$ V.

6.72 For the half-wave rectifier given in Fig. 6.56, on p. 401, reverse the diode. Sketch the output voltage v_o of the resulting circuit when the input is $v_S = A \sin \omega t\ u(t)$ V and $RC >> T = 2\pi/\omega$.

6.73 For the full-wave rectifier given in Fig. P6.44, connect a capacitor C in parallel with the

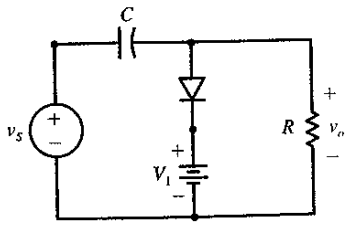


Fig. P6.77

6.78 Reverse the diode in the clamping circuit shown in Fig. P6.77. For the resulting circuit, given that the input voltage is $v_S = A \sin \omega t$ V and that $RC >> T = 2\pi/\omega$, sketch the output voltage v_o for the case that (a) $V_1 = A/2$, and (b) $V_1 = -A/2$.

6.79 For the clamping circuit shown in Fig. P6.79, the Zener diode has a breakdown voltage of 6 V. Sketch the output voltage v_o when the input voltage is $v_S = 24 \sin \omega t$ V and $RC >> T = 2\pi/\omega$.

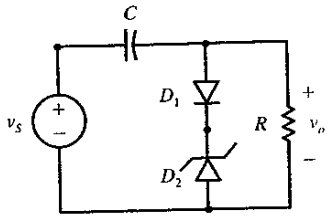


Fig. P6.79

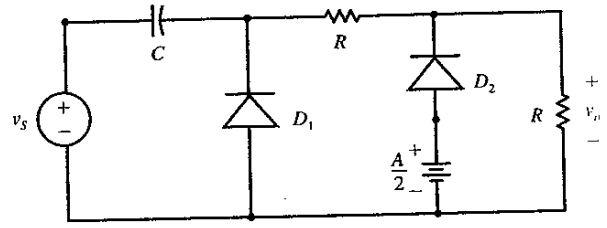


Fig. P6.81

6.80 Reverse the directions of both diodes in the clamping circuit shown in Fig. P6.79, and sketch the output voltage v_o when the input voltage is $v_S = 24 \sin \omega t$ V, $RC >> T = 2\pi/\omega$, and the Zener diode has a breakdown voltage of 6 V.

6.81 For the ideal-diode circuit shown in Fig. P6.81, sketch the output voltage v_o when the input is $v_S = A \sin \omega t$ V and $RC >> T = 2\pi/\omega$.

6.82 A silicon diode that has a permittivity of 1.04×10^{-10} F/m is reverse biased such that the depletion region has a width of 4×10^{-6} m. (a) If the cross section of the diode is a square measuring 1 mm on a side, what is the value of the transition capacitance? (b) What cross-sectional area would result in a transition capacitance of 15 pF?

6.83 A silicon diode with a saturation current of 16 nA at 300 K has a forward-bias voltage of 0.7 V and a mean carrier lifetime of 25 μs. (a) Find the diffusion capacitance. (b) Find the voltage that will result in a diffusion capacitance of 10 μF.

Verify that the transistor is biased in the active region by finding (a) i_B, (b) i_C, and (c) v_{CE}.

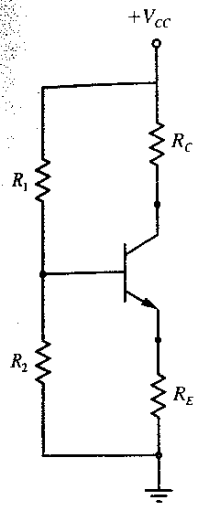


Fig. P7.10

7.11 The BJT in the circuit shown in Fig. P7.10 has $\beta = 100$. Suppose that $R_1 = 60$ kΩ, $R_2 = 30$ kΩ, $R_C = 1$ kΩ, $R_E = 100$ Ω, and $V_{CC} = 6$ V. Verify that the transistor is biased in the active region by finding (a) i_B, (b) i_C, and (c) v_{CE}.

7.12 The BJT in the circuit shown in Fig. P7.10 has $\beta = 100$. Suppose that $R_1 = 60$ kΩ, $R_2 = 30$ kΩ, $R_C = 1$ kΩ, and $V_{CC} = 6$ V. Find the minimum value of R_E such that the transistor will be in the active mode.

7.13 The BJT in the circuit shown in Fig. P7.10 has $\beta = 100$. Suppose that $R_1 = 60$ kΩ, $R_2 = 30$ kΩ, and $V_{CC} = 6$ V. Find R_E and R_C such that the transistor is biased in the active region at $i_C = 2$ mA and $v_{CE} = 2.1$ V.

7.14 The BJT in the circuit shown in Fig. P7.10 has $\beta = 100$. Suppose that $R_1 = 90$ kΩ, $R_2 = 10$ kΩ, and $V_{CC} = 20$ V. Find R_E and R_C such that the transistor is biased in the active region at $i_C = 2$ mA and $v_{CE} = 14.5$ V.

7.15 The BJT in the circuit shown in Fig. P7.10 has $\beta = 100$. Suppose that $R_1 = 150$ kΩ, $R_2 = \infty$, $R_C = R_E = 1$ kΩ, and $V_{CC} = 12$ V. Verify that the transistor is biased in the active region by finding (a) i_B, (b) i_C, and (c) v_{CE}.

7.16 The BJT in the circuit shown in Fig. P7.10 has $\beta = 100$. Suppose that $R_1 = 300$ kΩ, $R_2 = \infty$, and $V_{CC} = 12$ V. Find R_E and R_C such that the transistor is biased in the active region at $i_C = 2$ mA and $v_{CE} = 2.5$ V.

7.17 The BJT in the circuit shown in Fig. P7.10 has $\beta = 100$. Suppose that $R_1 = 120$ kΩ, $R_2 = \infty$, $R_C = 0$ Ω, $R_E = 1$ kΩ, and $V_{CC} = 6$ V. Verify that the transistor is biased in the active region by finding (a) i_B, (b) i_C, and (c) v_{CE}.

7.18 The BJT in the circuit shown in Fig. P7.10 has $\beta = 100$. Suppose that $R_C = 0$ Ω, $R_2 = \infty$, and $V_{CC} = 6$ V. Find R_E and R_1 such that the transistor is biased in the active region at $i_C = 2$ mA and $v_{CE} = 2$ V.

7.19 The BJT in the circuit shown in Fig. P7.19 has $\beta = 100$. Suppose that $R_B = 22$ kΩ, $R_C = 0$ Ω, $R_E = 2$ kΩ, $V_{BB} = V_{CC} = 0$ V, and $V_{EE} = 5$ V. Verify that the transistor is biased in the active region by finding (a) i_B, (b) i_C, and (c) v_{CE}.

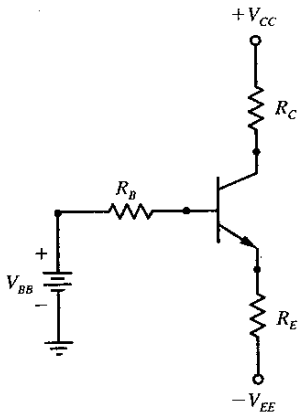


Fig. P7.19

7.20 The BJT in the circuit shown in Fig. P7.19 has $\beta = 100$. Suppose that $R_C = 0$ Ω, $V_{BB} = V_{CC} = 0$ V, and $V_{EE} = 5$ V. Find R_B and R_E such that the transistor is biased in the active region at $i_C = 2$ mA and $v_{CE} = 2.7$ V.

7.21 For the circuit shown in Fig. P7.19, suppose that $R_B = 180\ \text{k}\Omega$, $R_C = R_E = 1\ \text{k}\Omega$, $V_{BB} = 0$ V, and $V_{CC} = V_{EE} = 5$ V. Given that the BJT has $\beta = 100$, verify that the transistor is in the active region by finding (a) i_B, (b) i_C, and (c) v_{CE}.

7.22 For the circuit shown in Fig. P7.19 suppose that $R_B = 165\ \text{k}\Omega$, $R_C = R_E = 1\ \text{k}\Omega$, and $V_{CC} = V_{EE} = 5$ V. Given that the BJT is in the active region such that $i_B = 50\ \mu\text{A}$ and $i_C = 4.25$ mA, find (a) β, (b) V_{BB}, and (c) v_{CE}.

7.23 The BJT in the circuit shown in Fig. P7.19 has $\beta = 100$. Given that $R_B = 500\ \text{k}\Omega$, $R_E = 5\ \text{k}\Omega$, $V_{BB} = 0$ V, and $V_{CC} = V_{EE} = 10$ V, determine the value of R_C such that the transistor is in the active region and $v_{CE} = 10$ V.

7.24 For the circuit shown in Fig. P7.24, suppose that $R_B = 250\ \text{k}\Omega$, $R_{C1} = 2.2\ \text{k}\Omega$, $R_{C2} = 100\ \Omega$, $R_E = 0\ \Omega$, and $V_{BB} = V_{CC} = 5$ V. Given that the BJTs have $\beta = 100$, verify that the transistors are in the active region by finding i_{C1}, v_{CE1}, i_{C2}, and v_{CE2}.

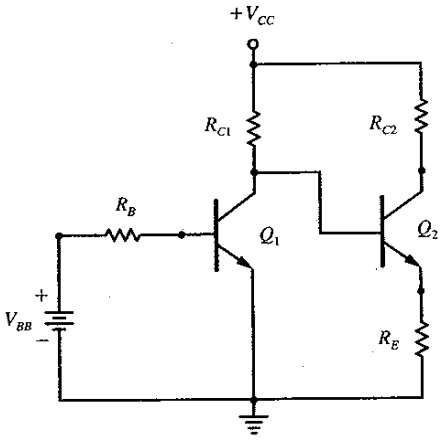


Fig. P7.24

7.25 For the circuit shown in Fig. P7.24, suppose that $R_B = 230\ \text{k}\Omega$, $R_{C1} = 1\ \text{k}\Omega$, $R_{C2} = 0\ \Omega$, $R_E = 2\ \text{k}\Omega$, $V_{BB} = 3$ V, and $V_{CC} = 6$ V. Given that the BJTs have $\beta = 100$, verify that the transistors are in the active region by finding i_{C1}, v_{CE1}, i_{C2}, and v_{CE2}.

7.26 The BJTs in the circuit shown in Fig. P7.24 have $\beta = 100$. Suppose that $V_{BB} = 4$ V and $V_{CC} = 6$ V. Find R_B, R_{C1}, R_E, and R_{C2} such that the transistors are biased in the active region at $i_{C1} = 1$ mA, $v_{CE1} = 3.5$ V, $i_{C2} = 4$ mA, and $v_{CE2} = 2$ V.

7.27 For the circuit shown in Fig. P7.27, suppose that $R_B = 230\ \text{k}\Omega$, $R_{E1} = 400\ \Omega$, $R_{E2} = 0\ \Omega$, $R_C = 100\ \Omega$, and $V_{CC} = 6$ V. Given that the BJTs have $\beta = 100$, verify that the transistors are in the active region by finding i_{C1}, v_{CE1}, i_{C2}, and v_{CE2}.

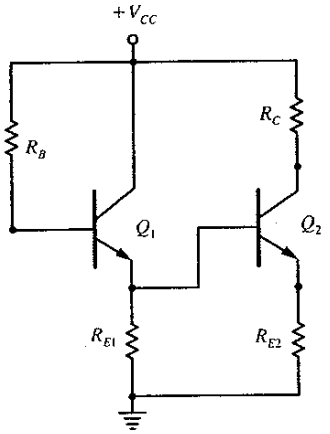


Fig. P7.27

7.28 For the circuit shown in Fig. P7.27, suppose that $R_B = 65\ \text{k}\Omega$, $R_{E1} = 500\ \Omega$, $R_{E2} = 1\ \text{k}\Omega$, $R_C = 1\ \text{k}\Omega$, and $V_{CC} = 6$ V. Given that the BJTs have $\beta = 100$, verify that the transistors are in the active region by finding i_{C1}, v_{CE1}, i_{C2}, and v_{CE2}.

7.29 The BJTs in the circuit shown in Fig. P7.27 have $\beta = 100$. Suppose that $V_{CC} = 6$ V. Find R_B, R_{E1}, R_{E2}, and R_C such that the transistors are biased in the active region at $i_{C1} = 1$ mA, $v_{CE1} = 2.6$ V, $i_{C2} = 13.5$ mA, and $v_{CE2} = 1.3$ V.

7.30 For the circuit given in Fig. 7.13, (p. 435), suppose that $V_{CC} = 5$ V. (a) Find the minimum value of h_{FE} required to saturate the BJT for the case that $R_B = 50\ \text{k}\Omega$, $R_C = 1\ \text{k}\Omega$, and $v_I = 5$ V. (b) Find the minimum value of R_C required to saturate the BJT for the case that $h_{FE} = 100$, $R_B = 50\ \text{k}\Omega$, and $v_I = 5$ V. (c) Find the maximum value of R_B required to saturate the BJT for the case that $h_{FE} = 100$, $R_C =$

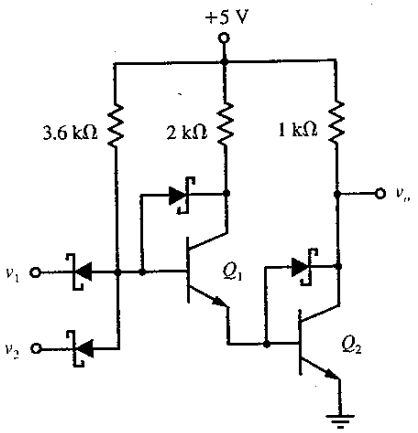


Fig. P7.77

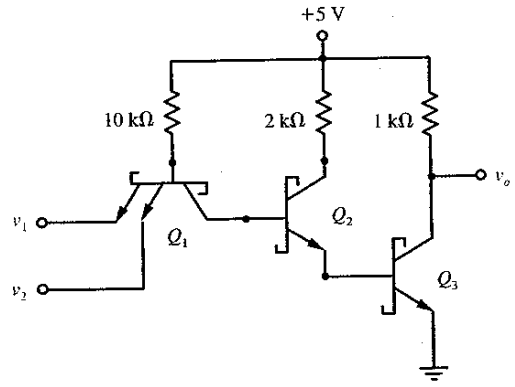


Fig. P7.80

7.82 For the Schottky TTL NAND gate shown in Fig. P7.80, suppose $h_{FER} = 0.5$ for Q_1. Find the fan-out for the case that $h_{FE} = 50$ and the high voltage is 3 V.

7.83 Find the power dissipated by the ECL gate given in Fig. 7.43 on p. 478 (see Example 7.18).

7.84 Determine the noise margins NM_L and NM_H for the ECL OR/NOR gate given in Fig. 7.43 on p. 478 (see Example 7.18).

7.85 For the ECL OR/NOR gate shown in Fig. P7.85, suppose that $R_2 = 200\ \Omega$, $V_R = 4$ V, $V_{CC} = 5$ V, and $V_{EE} = 0$ V. Neglect base currents and determine (a) the low voltage, (b) the high voltage, and (c) the value of R_1. (See p. 501.)

7.86 For the ECL OR/NOR gate shown in Fig. P7.85, suppose that $R_1 = 250\ \Omega$, $V_R = 3.7$ V, $V_{CC} = 5$ V, and $V_{EE} = 0$ V. Neglect base currents and determine (a) the high voltage, (b) the low voltage, and (c) the value of R_2.

7.87 For the ECL OR/NOR gate shown in Fig. P7.85, suppose that $R_2 = 300\ \Omega$, $V_R = 1.5$ V, $V_{CC} = V_{EE} = 2.5$ V. Neglect base currents and determine (a) the low voltage, (b) the high voltage, and (c) the value of R_1.

7.88 For the ECL OR/NOR gate shown in Fig. P7.85, suppose that the low voltage is -1.6 V, $V_R = -1.3$ V, $V_{CC} = 0$ V, and $V_{EE} = 5$ V. Neglect base currents and determine the values of R_1 and R_2.

7.89 Determine the fan-out of the RTL NOR gate in Fig. 7.44 on p. 482 for the case that the transistors have $h_{FE} = 50$.

7.90 For the RTL NOR gate given in Fig. 7.44 on p. 482, let $R_B = 20$ kΩ, $R = 5$ kΩ, and $V_{CC} = 5$ V. Suppose that this gate is loaded by 10 identical gates. Determine (a) the high voltage, and (b) the minimum value of h_{FE} for the transistors.

7.91 The RTL circuit shown in Fig. P7.91 is a NAND gate. The low voltage is 0.4 V and the high voltage is 1.2 V. Determine whether each transistor is OFF or ON, and find the minimum values of h_{FE} for (a) $v_1 = v_2 = 0.4$ V; (b) $v_1 = 0.4$ V, $v_2 = 1.2$ V; (c) $v_1 = 1.2$ V, $v_2 = 0.4$ V; and (d) $v_1 = v_2 = 1.2$ V.

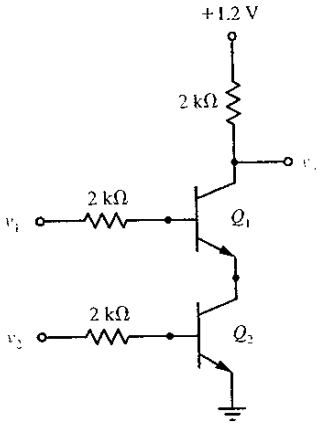


Fig. P7.91

8.9 For the circuit given in Fig. P8.2, suppose that $R_D = R_S = R$, $V_{DD} = 15$ V, and the JFET has $V_p = -3$ V. (a) Assuming active-region operation, $V_{GG} = 5$ V, and $I_{DSS} = 10$ mA, determine the value of R for which $v_{GS} = 0$ V. (b) Assuming active-region operation, find I_{DSS} given that $R = 400\ \Omega$, $V_{GG} = 5$ V, and $v_{GS} = 0$ V. (c) If I_{DSS}, R, and the region of operation are not known, what is v_{GS} when $V_{GG} = 5$ V and $v_{DS} = 1$ V? (d) If R is not known, what is the region of operation when $v_{DS} = 2$ V and $v_{GS} = -1.5$ V?

8.10 For the circuit shown in Fig. P8.10, the JFET has $I_{DSS} = 9$ mA and $V_p = -3$ V. Given that $R_1 = 150\ \text{k}\Omega$, $R_2 = 50\ \text{k}\Omega$, $R_D = R_S = 7\ \text{k}\Omega$, and $V_{DD} = 20$ V, assume active-region operation and determine (a) v_{GS}, (b) i_D, and (c) v_{DS}. (*Hint:* Use Thévenin's theorem.)

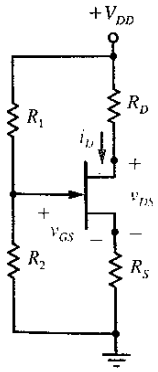


Fig. P8.10

8.11 For the circuit shown in Fig. P8.10, the JFET has $I_{DSS} = 12$ mA and $V_p = -4$ V. Given that $R_1 = 300\ \text{k}\Omega$, $R_2 = 100\ \text{k}\Omega$, $R_D = R_S = R$, $V_{DD} = 12$ V, and $v_{DS} = 6$ V, determine (a) v_{GS}, (b) i_D, and (c) R. (*Hint:* Use Thévenin's theorem.)

8.12 For the circuit shown in Fig. P8.10, the JFET has $I_{DSS} = 12$ mA and $V_p = -4$ V. Given that $R_1 = 300\ \text{k}\Omega$, $R_2 = 100\ \text{k}\Omega$, $R_D = R_S = 1\ \text{k}\Omega$, and $V_{DD} = 12$ V, determine (a) v_{GS}, (b) i_D, (c) v_{DS}, and (d) the region of operation for the JFET. (*Hint:* Use Thévenin's theorem.)

8.13 For the circuit shown in Fig. P8.10, the JFET has $I_{DSS} = 12$ mA and $V_p = -4$ V. Given that $R_1 = 300\ \text{k}\Omega$, $R_2 = 100\ \text{k}\Omega$, $R_D = R_S = 2\ \text{k}\Omega$, and $V_{DD} = 12$ V, determine (a) v_{GS}, (b) i_D, (c) v_{DS}, and (d) the region of operation for the JFET. (*Hint:* Use Thévenin's theorem.)

8.14 Both JFETs in the circuit shown in Fig. P8.14 have $I_{DSS} = 4$ mA and $V_p = -2$ V. Given that both JFETs are in the active region, $R_S = 0\ \Omega$ and $V_{DD} = V_{SS} = 10$ V, find (a) i_D, (b) v_{GS}, (c) v_{DS}, and (d) confirm the regions of operation.

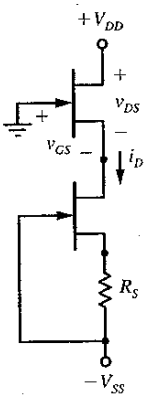


Fig. P8.14

8.15 Both JFETs in the circuit shown in Fig. P8.14 have $I_{DSS} = 4$ mA and $V_p = -2$ V. Place a 1-kΩ resistor in series with the drain of the lower JFET. Given that both JFETs are in the active region, $R_S = 1\ \text{k}\Omega$ and $V_{DD} = V_{SS} = 10$ V, find (a) i_D, (b) v_{GS}, (c) v_{DS}, and (d) confirm the regions of operation.

8.16 Both JFETs in the circuit shown in Fig. P8.14 have $I_{DSS} = 16$ mA and $V_p = -4$ V. Given that $R_S = 0\ \Omega$, $V_{DD} = 12$ V, $V_{SS} = 0$ V, the upper JFET is in the active region, and the lower JFET is in the ohmic region, find (a) v_{GS}, (b) i_D, and (c) v_{DS}.

8.17 Both JFETs in the circuit shown in Fig. P8.14 have $I_{DSS} = 16$ mA and $V_p = -4$ V. Instead of connecting the gate of the upper JFET to the reference as shown, connect a short circuit between the gate of the upper JFET and the drain of the lower JFET. Given that $R_S = 1\ \text{k}\Omega$, $V_{DD} = 6$ V, $V_{SS} =$

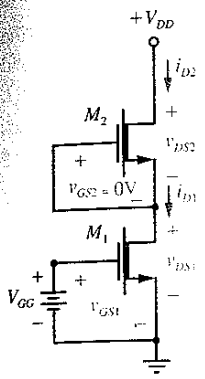


Fig. P8.26

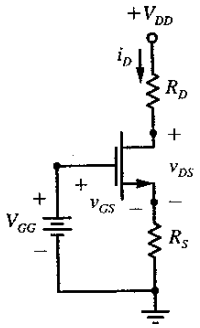


Fig. P8.32

8.28 For the depletion-MOSFET circuit shown in Fig. P8.26, M_1 has $I_{DSS} = 8$ mA and $V_p = -4$ V, whereas M_2 has $I_{DSS} = 16$ mA and $V_p = -4$ V. Given that $V_{DD} = 11$ V, find V_{GG} such that M_1 is in the active region and M_2 is on the border between the active and the ohmic regions.

8.29 For the depletion-MOSFET circuit shown in Fig. P8.26, M_1 has $I_{DSS} = 8$ mA and $V_p = -4$ V, whereas M_2 has $I_{DSS} = 16$ mA and $V_p = -4$ V. When $V_{DD} = 11$ V and $V_{GG} = 2$ V, then M_1 is in the ohmic region and M_2 is in the active region. Find (a) i_D, (b) v_{DS1}, (c) v_{DS2}, and (d) confirm the regions of operation.

8.30 For the depletion-MOSFET circuit shown in Fig. P8.26, M_1 has $I_{DSS} = 8$ mA and $V_p = -4$ V, whereas M_2 has $I_{DSS} = 16$ mA and $V_p = -4$ V. When $V_{DD} = 11$ V and $V_{GG} = 10$ V, then M_1 is in the ohmic region and M_2 is in the active region. Find (a) i_D, (b) v_{DS1}, (c) v_{DS2}, and (d) confirm the regions of operation.

8.31 An n-channel enhancement MOSFET has $K = 0.25$ mA/V^2 and $V_t = 2$ V. For small values of v_{DS}, determine the approximate drain-source resistance r_{DS} when v_{GS} is (a) 4 V, (b) 6 V, and (c) 10 V.

8.32 For the circuit given in Fig. P8.32, the enhancement MOSFET has $K = 0.15$ mA/V^2, $V_t = 2$ V, and operates in the active region. Suppose that $V_{DD} = 12$ V. (a) Find V_{GG} when $R_S = 0\ \Omega$ and $i_D = 5.4$ mA. (b) Find i_D when $v_{GS} = 4$ V. (c) Find v_{GS} when $i_D = 2.4$ mA. (d) Find R_S when $v_{GS} = 3$ V and $V_{GG} = 4.5$ V. (e) Find R_D when $v_{GS} = 3$ V, $v_{DS} = 7.5$ V, and $V_{GG} = 4.5$ V. (f) Find v_{DS} when $R_D = 4$ kΩ, $v_{GS} = 3$ V, and $V_{GG} = 4.5$ V.

8.33 For the circuit given in Fig. P8.32, the enhancement MOSFET has $K = 0.25$ mA/V^2 and $V_t = 2$ V. Given that $R_S = 0\ \Omega$ and $V_{DD} = 16$ V, determine the value of R_D for which the enhancement MOSFET will operate on the border between the active and the ohmic regions when V_{GG} is (a) 4 V and (b) 10 V.

8.34 For the circuit given in Fig. P8.32, the enhancement MOSFET has $K = 0.25$ mA/V^2 and $V_t = 2$ V. Given that $R_D = 1$ kΩ, $R_S = 0\ \Omega$, $V_{DD} = 16$ V, and $V_{GG} = 4$ V, find (a) i_D, (b) v_{DS}, and (c) the region of operation for the MOSFET.

8.35 For the circuit given in Fig. P8.32, the enhancement MOSFET has $K = 0.25$ mA/V^2 and $V_t = 2$ V. Given that $R_D = R_S = 1$ kΩ, $V_{DD} = 20$ V, and $V_{GG} = 10$ V, find (a) v_{GS}, (b) i_D, (c) v_{DS}, and (d) the region of operation for the MOSFET.

8.36 For the circuit given in Fig. P8.32, the enhancement MOSFET has $K = 0.25$ mA/V^2 and $V_t = 2$ V. Given that $R_D = R_S = 1$ kΩ, $V_{DD} = 9$ V, and $V_{GG} = 10$ V, find (a) v_{GS}, (b) i_D, (c) v_{DS}, and (d) the region of operation for the MOSFET.

8.37 For the MOSFET circuit shown in Fig. P8.37, the enhancement NMOS transistor has $K = 0.2$ mA/V^2 and $V_t = 1$ V. Given that $V_{DD} = 10$ V

and $v_{DS} = 6$ V, find (a) v_{GS}, (b) the region of operation, (c) i_D, and (d) R_D.

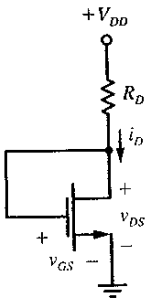


Fig. P8.37

8.38 For the MOSFET circuit shown in Fig. P8.37, the enhancement NMOS transistor has $K = 0.2$ mA/V^2 and $V_t = 1$ V. Given that $V_{DD} = 10$ V and $i_D = 3.2$ mA, find (a) the region of operation, (b) v_{GS}, (c) v_{DS}, and (d) R_D.

8.39 For the MOSFET circuit shown in Fig. P8.37, the enhancement NMOS transistor has $K = 0.2$ mA/V^2 and $V_t = 1$ V. Given that $V_{DD} = 10$ V and $R_D = 1$ kΩ, find (a) the region of operation, (b) v_{GS}, (c) v_{DS}, and (d) i_D.

8.40 For the circuit shown in Fig. P8.40, the enhancement MOSFET has $K = 0.25$ mA/V^2 and $V_t = 1$ V. Given that $R_1 = 300$ kΩ, $R_2 = 100$ kΩ, $R_D = R_S = R$, $V_{DD} = 12$ V, and $v_{DS} = 10$ V, determine (a) v_{GS}, (b) i_D, and (c) R. (*Hint:* Use Thévenin's theorem.)

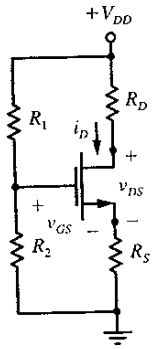


Fig. P8.40

8.41 For the circuit shown in Fig. P8.40, the enhancement MOSFET has $K = 0.25$ mA/V^2 and $V_t = 1$ V. Given that $R_1 = 300$ kΩ, $R_2 = 100$ kΩ, $R_D = R_S = 1$ kΩ, and $V_{DD} = 12$ V, find (a) v_{GS}, (b) i_D, (c) v_{DS}, and (d) the region of operation for the MOSFET. (*Hint:* Use Thévenin's theorem.)

8.42 For the MOSFET circuit given in Fig. P8.37, replace the short circuit that is connected between the gate and the drain with a 1-MΩ resistor. In addition, place another 1-MΩ resistor between the gate and the reference. Given that $K = 0.25$ mA/V^2, $V_t = 2$ V, $R_D = 500$ Ω, and $V_{DD} = 12$ V, find (a) the region of operation for the MOSFET, (b) v_{GS}, (c) v_{DS}, and (d) i_D.

8.43 The NMOS circuit shown in Fig. P8.43 is known as a **current mirror** since the current on one side equals (mirrors) the current on the other side. Given that all of the enhancement MOSFETs have $K = 0.1$ mA/V^2 and $V_t = 1$ V, $V_{DD} = 10$ V, and M_1 is in the active region, find all the currents and voltages for the circuit.

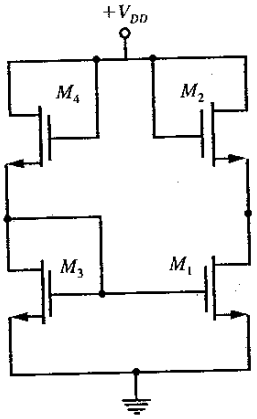


Fig. P8.43

8.44 For the NMOS circuit given in Fig. 8.2[illegible] on p. 533, suppose that $V_{DD} = 12$ V. When v_1 = 12 V, then M_1 is in the ohmic region. Given that $V_t = 2$ V for both MOSFETs and $K_1 = K_2$, find