## 1. (10 points) FoEE 7.27

**7.27** For the circuit shown in Fig. P7.27, suppose that  $R_B = 230 \text{ k}\Omega$ ,  $R_{E1} = 400 \Omega$ ,  $R_{E2} = 0 \Omega$ ,  $R_C = 100 \Omega$ , and  $V_{CC} = 6 \text{ V}$ . Given that the BJTs have  $\beta = 100$ , verify that the transistors are in the active region by finding  $i_{C1}$ ,  $v_{CE1}$ ,  $i_{C2}$ , and  $v_{CE2}$ .

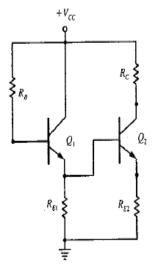


Fig. P7.27

If we are asked to veify that the transistors are on, then we can assume on and consimulated them are no contradictions.

If Q, 4 Qz one on: VBE, = 0.7V, VBEZ= 0.7V La= & LB, = 100 iB, and La= 100 iBZ

10, KUL: 6=230 K (ibi) + VBE, + VBEZ + iEZBEZ 6=230,000 ibi + 1.4

ic1 = 100 is1 : [ic1 = 2 mA]

iB2= iE1 - i3

 $i_3 = \frac{V_{BEZ}}{400R} = \frac{0.7}{400} A$  $i_{E1} = i_{B1} + i_{E1} = 2.02 \text{ mA}$ 

-. LBZ= 2.02 mA - 1.75mA = 2704A : (icl= 100.2)4A = 27 mA

By KVL: (VCE, = 6 - UBEZ = 5.3 V

By KLL: [VEZ = 6 - ia (Rc) = 3.3V

2. (10 points) FoEE 7.91

7.91 The RTL circuit shown in Fig. P7.91 is a NAND gate. The low voltage is 0.4 V and the high voltage is 1.2 V. Determine whether each transistor is OFF or ON, and find the minimum values of  $h_{FE}$  for (a)  $v_1 = v_2 = 0.4$  V; (b)  $v_1 = 0.4$  V,  $v_2 = 1.2$  V; (c)  $v_1 = 1.2$  V,  $v_2 = 0.4$  V; and (d)  $v_1 = v_2 = 1.2$  V.

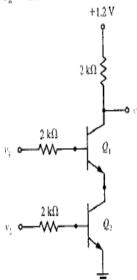


Fig. P7.91

a) By looking at V, Vi he know Qi Is off.
V=V=04V VBEI isn't high enough to turn it on.

i lgi = O, ici = O.

If ici=O iei=O.

VBE, < O.JU so Q, is off.

No coverent flows, so, Vo= 1.2V.

b)  $V_1 = 0.4 V$ ,  $V_2 = 01.2 V$ Here,  $Q_1$  is on since  $V_1 > 0.5 U$ .  $C_{R1} = \frac{V_2 - V_R E_2}{2K} = 0.2 \text{ mA}$ 

Since V, < 0.5, Q, is Off ... So, is=0,i=0

Since hfrez= Ser = D = 0. Vo=1.20

in = U, - (VBE1 + Ver) = 0.1 mb

bei= 1.2-0.4 = 0.4 mA.

h Fe = 1 = 4 hper = 100 = 2.5

AlSo, ic= 208, 1 ic, = 0.1 at +0.4 at

V= VcE, + VCE = 0.4 V.

## 3. (10 points) FoEE 8.11

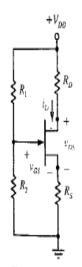


Fig. P8.10

**8.11** For the circuit shown in Fig. P8.10, the JFET has  $I_{DSS} = 12$  mA and  $V_P = -4$  V. Given that  $R_1 = 300$  k $\Omega$ ,  $R_2 = 100$  k $\Omega$ ,  $R_D = R_S = R$ ,  $V_{DD} = 12$  V, and  $V_{DS} = 6$  V, determine (a)  $V_{CS}$ . (b)  $I_D$ . and (c) R. (*Hint*: Use Thévenin's theorem.)

## 4. (0 points) FoEE 7.13

7.13 The BJT in the circuit shown in Fig. P7.10 has  $\beta = 100$ . Suppose that  $R_1 = 60 \text{ k}\Omega$ ,  $R_2 = 30 \text{ k}\Omega$ , and  $V_{CC} = 6 \text{ V}$ . Find  $R_E$  and  $R_C$  such that the transistor is biased in the active region at  $I_C = 2$  mA and  $V_{CE} = 2.1 \text{ V}$ .

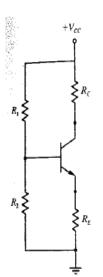
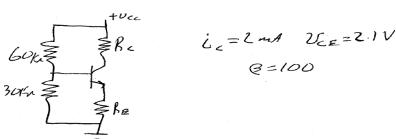
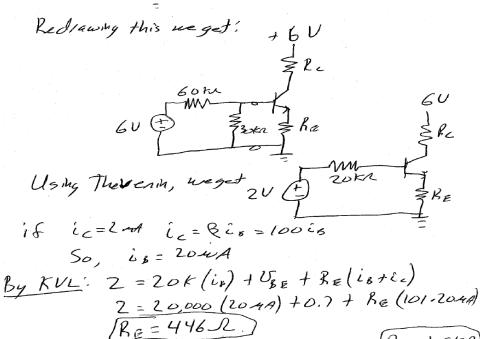


Fig. P7.10

a) 
$$V_{05}=6V$$
 by  $KUL$ ,  $12=R_{00}+U_{05}+R_{10}=2R_{10}+6$ 
 $R_{10}=3$ 
By  $KVL: 3=75K(i_6)+U_{05}+R_{10}=0+U_{05}+R_{10}$ 
 $=0+U_{05}+R_{10}$ 
 $U_{05}=0$ 

b) 
$$U_{ps} = 6V > V_{Gs} - V_{p} = 4V$$
 TFET is adive.  
So  $i_{0} = I_{pss} \left(1 - \frac{V_{us}}{V_{p}}\right)^{2} = I_{pss} = 12 \text{ nA}$ .





KVL again = icRc+Vie + CBRE=6 = (Rc=1.5KD)

(0 points) FoEE 8.33

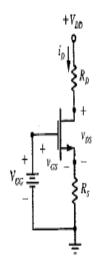


Fig. P8.32

**8.33** For the circuit given in Fig. P8.32, the enhancement MOSFET has  $K = 0.25 \text{ mA/V}^2$  and  $V_t = 2 \text{ V}$ . Given that  $R_S = 0 \Omega$  and  $V_{DD} = 16 \text{ V}$ , determine the value of  $R_D$  for which the enhancement MOSFET will operate on the border between the active and the ohmic regions when  $V_{GO}$  is (a) 4 V and (b) 10 V.

Given'  $K = 0.25 \text{ mA/v}^2$   $V_t = 2V$  $V_{pp} = 16V$ 

At the border  $V_{DS} = V_{6S} - V_{4}$ In (4)  $V_{66} = 4U$ , so  $V_{6S} = 4V$ , so  $V_{DS} = 2V$ Using  $i_{D} = K(V_{6S} - V_{4})^{2} = I_{MA}$ By KVL:  $I_{6} = R_{6}i_{0} + V_{0S} = R_{0}(I_{MA}) + 2$   $\vdots$   $R_{0} = I_{4}K_{A}$ In (4)  $V_{66} = I_{0}U$ , so  $V_{6S} = 8V$ Again  $i_{D} = K(V_{6S} - U_{4})^{2} = I_{6}M_{A}$  By KVL we sind  $K_{0} = SOO_{A}$