1. (10 points) FoEE 6.39

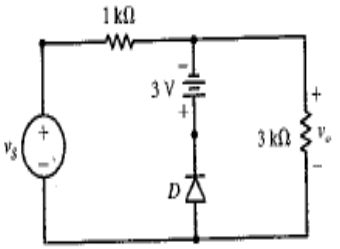


Fig. P6.38

6.39 For the ideal-diode circuit given in Fig. P6.38, reverse the polarity of the 3-V source. The input voltage to the resulting clipper circuit is $v_S = 12 \sin \omega t$ V. Determine the output voltage v_o and sketch this function.

6.44 The ideal-diode circuit shown in Fig. P6.44 is known as a **full-wave** (or **bridge**) **rectifier circuit.** Determine which diodes are ON and which are OFF when (a) $v_S > 0$ V, and (b) $v_S < 0$ V. Sketch the output voltage v_o for the case that the input voltage is $v_S = A \sin \omega t$ V.

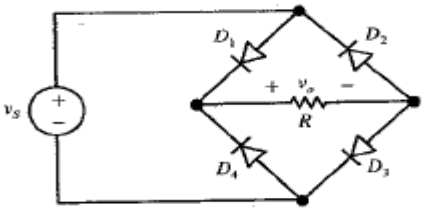
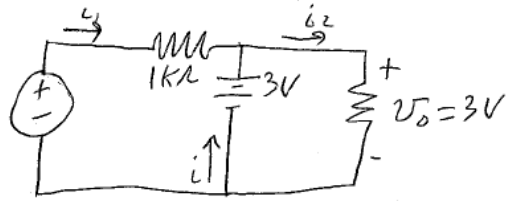


Fig. P6.44

⑥ FoEE 6.39



When diode is ON: v_S

$i_1 = \frac{v_S - 3}{1K}$

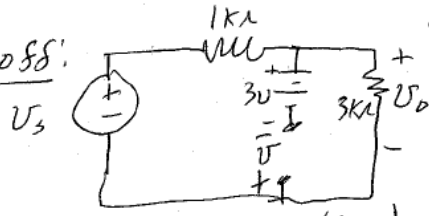
$i_2 = \frac{v_o}{3K} = 1mA$

$i = i_2 - i_1 = 1mA - \frac{v_S - 3}{1K} = \frac{3 - 3v_S + 9}{3K} = \frac{-3v_S + 12}{3K}$

This i has to be > 0 So, $-3v_S + 12 > 0$

$v_S < 4V$

When diode is off:



v_S

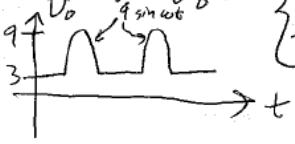
$v_o = \frac{3K}{4K} \cdot v_S = \frac{3}{4} v_S$

$v = -v_o + 3 = -\frac{3}{4} v_S + 3$

$v \leq 0, \quad -\frac{3}{4} v_S + 3 \leq 0$

So, $v_S \geq 4V$

In summary: $v_o = \begin{cases} 3 & \text{for } v_S < 4 \text{ (D.is on)} \\ \frac{3}{4} v_S & \text{for } v_S \geq 4 \text{ (D.is off)} \end{cases}$

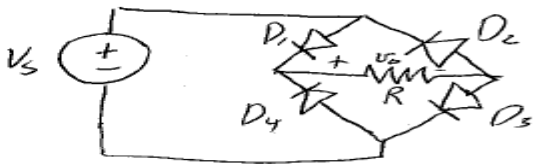


2. (10 points) FoEE 6.44

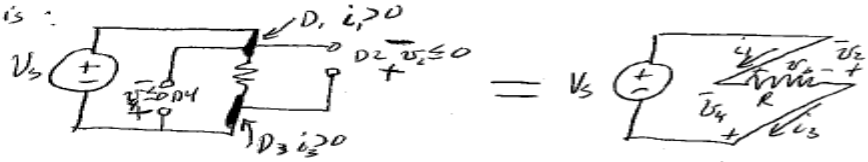
a) When $v_S > 0$ V

D_1, D_3 are on.

D_2, D_4 are off.



Ckt would look like this:



Inspection of this circuit verifies that $v_2, v_4 \leq 0$ V & $i_1 = i_3 > 0$ A.

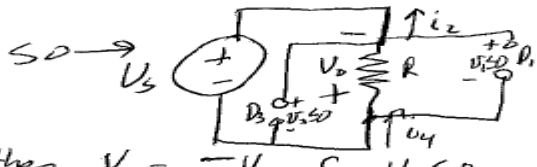
So, $v_o = +v_S$ V.

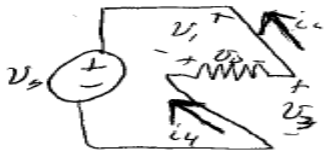
b) When $v_S < 0$

D_1, D_3 off

D_2, D_4 on

So →



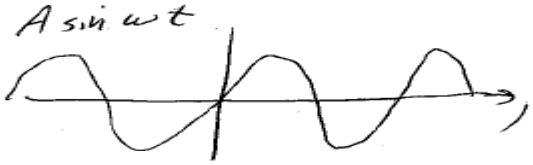


If $v_S < 0$, then $v_o = -v_S$ for $v_S < 0$

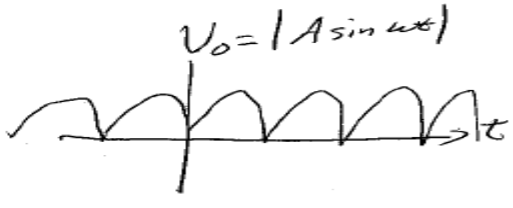
Inspection to verify D_1, D_3 off: $v_1, v_3 \leq 0$

D_2, D_4 on, $i_2, i_4 > 0$

If $v_S(t) = A \sin \omega t$



$v_o = |A \sin \omega t|$



3. (10 points) FoEE 6.35

6.35 A silicon diode has a saturation current of 10 nA at 300 K.

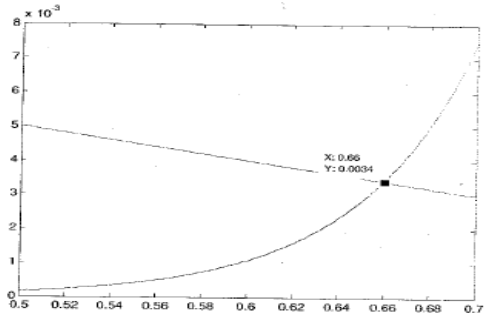
(a) Plot an i-v characteristic curve on a piece of graph paper.

(b) Suppose that this diode is used in the circuit given in Fig. 6.16*a*, on p. 368, where $v_1 = 1$ V and $R = 100\ \Omega$. Use the i-v curve obtained in part (a) to determine graphically i and v.

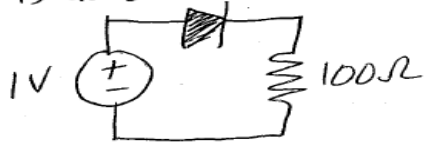
For a silicon diode we use $\eta = 2$, $V_T = \frac{\text{temperature in K}}{11,586}$

We are told that $I_S = 10\,nA$ at 300 K.

Using the equation: $i = I_s\left(e^{v/\eta V_T} - 1\right)$ we can plot i.



b) If the diode is used in this circuit:



We can add the $i = \frac{-v}{100} + \frac{1}{100}$ load line as seen in the plot above.

The crossing point tells us: $i = 3.4\,mA$, $v = 0.66\,V$

4. (15 points) FoEE 6.60

6.60 For the half-wave rectifier circuit given in Fig. 6.20, on p. 373, replace the ideal diode with a diode having $R_f = 20\ \Omega$ and $V_\gamma = 0.6$ V (see Fig. 6.42 on p. 388). Sketch the output voltage v_o, labeling it sufficiently, for the case that the input voltage is $v_S = 6 \sin \omega t$ V and $R = 100\ \Omega$.

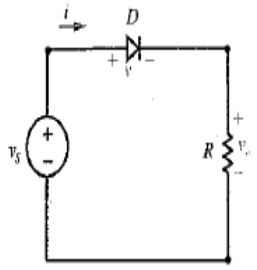
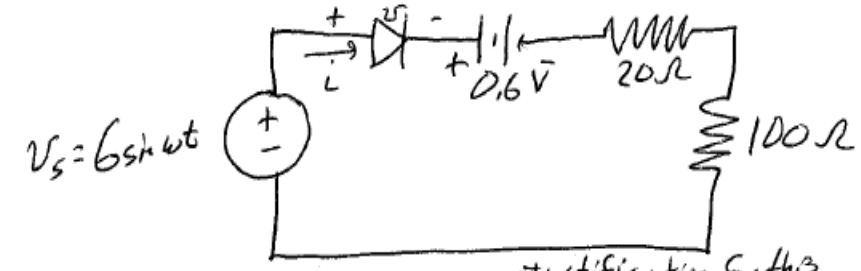


Fig. 6.20 An ideal-diode circuit.



When $v_S > 0.6$ V D is on. ← justification for this

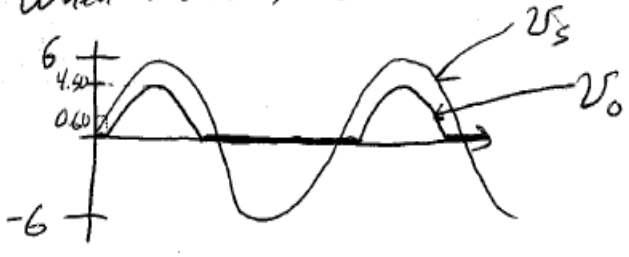
When D is on:

$v_S = 0.6 + 20i + 100i = 0.6 + 120i$

$\frac{v_S - 0.6}{120} = i$ i has to be > 0 if D is on.

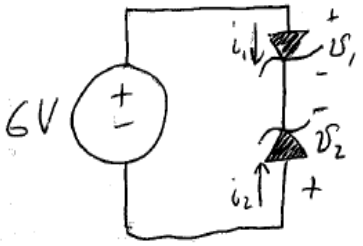
So $v_S > 0.6$. When D is on, $v_o = 100i = \frac{5}{6}v_S - 0.5$.

When D is off, $v_o = 0$.



5. (10 points) FoEE 6.62

6.62 For the circuit given in Fig. 6.50, on p. 395, reverse D_1. The identical silicon Zener diodes have saturation currents of 10 nA at 300 K. Find i, v_1, and v_2 when $V_S = 6$ V and the breakdown voltage of the diodes is (a) 9 V and (b) 5 V.



By KCL, we know $i_1 = -i_2$.

Given the orientation of the source and the diodes, we can be reasonably sure that D_1 will be on and that D_2 will either be in reverse bias or breakdown.

a) $V_z = 9V$. Since the source is well below the breakdown voltage, the logical guess of these states would be: D_1 forward bias and D_2 reverse bias.

So, i_2 is going to be forced to be at $-I_s$, $-10nA$.

This diode can allow a range of voltages, but the current is fixed. So, we can use this current to find i_1. Then use that to find v_1. And KVL to find v_2.

$i_1 = I_s\left(e^{v/\eta V_T} - 1\right)$ So,

$$v_1 = \ln\left(\frac{i_1}{I_s} + 1\right)\eta V_T$$

$i_1 = -i_2 = I_s \Rightarrow$ $\boxed{v_1 = \ln(2)\, 2\, \frac{300}{11586} = 0.036V}$

By KVL $\boxed{v_2 = -5.964V}$ $\boxed{i \text{ as originally drawn is } -10nA.}$

b) $V_z = 5V$. Now, by the same logic as above, we can say D_1 is forward bias and D_2 is likely broken down. If this is the case, v_2 will be fixed at $-5V$, but can allow a large range of negative currents.

So, by KVL $\boxed{v_1 = 1V.}$ $\boxed{v_2 = -5V.}$

And $i_1 = I_s\left(e^{v_1/\eta V_T} - 1\right) = 2.43A$

So, $\boxed{i \text{ (as drawn)} = -2.43A}$

Note that if you kept the polarity of v_1 as originally drawn instead of flipping it with the diode, your answers for v_1 would be flipped.

6. (10 points) FoEE 6.79

6.79 For the clamping circuit shown in Fig. P6.79, the Zener diode has a breakdown voltage of 6 V. Sketch the output voltage v_o when the input voltage is $v_S = 24 \sin \omega t$ V and $RC >> T = 2\pi/\omega$.

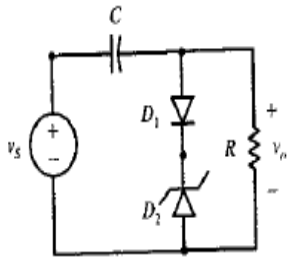
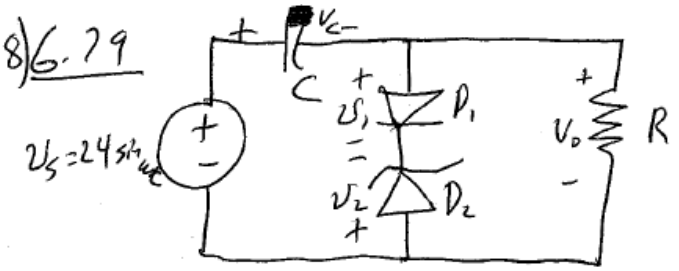


Fig. P6.79

8) 6.79



D_2: $v_z = 6$ V

$RC >> T = \frac{2\pi}{\omega}$

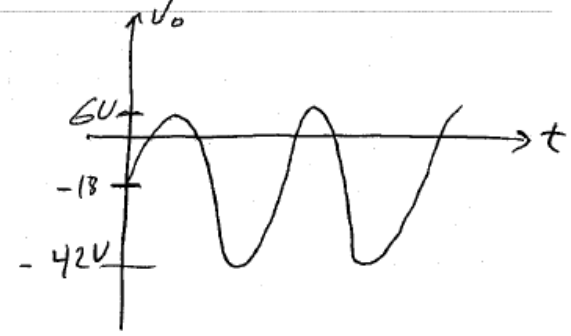
The first time v_S goes to positive 24, D_2 is in breakdown and D_1 is on. In breakdown, $v_2 = -6$ V $\therefore$ $v_o = 6$ V.

By KVL, $v_C = 18$ V.

Because the RC time constant is very high compared to the frequency of the input, the capacitor charges to 18 V and doesn't have time to discharge. Thus, this capacitor is always on.

$v_o = -v_C + v_S$ So, v_o will just be a shifted down version of v_S.

$v_o = 24 \sin \omega t - 18$



Optional Problems:

7. (0 points) FoEE 6.41

6.41 The input voltage to the clipper circuit shown in Fig. P6.41 is $v_S = 12 \sin \omega t$ V. Determine the output voltage v_o and sketch this function.

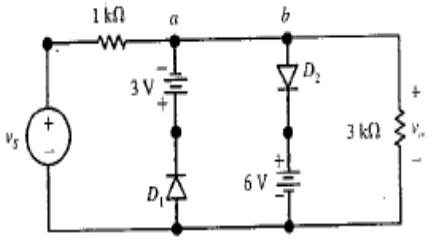
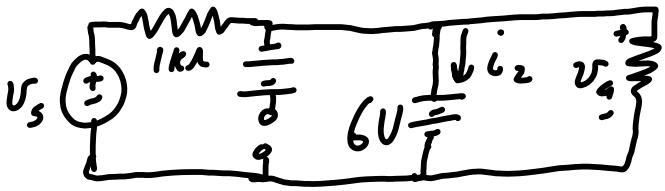


Fig. P6.41

1st get a feel for what happens in this circuit.

If D_2 is on $v_a = 6$ V and D_1 is off (I)



$v_a = 6$ V

$i_a = \frac{6}{3k} = 2$ mA

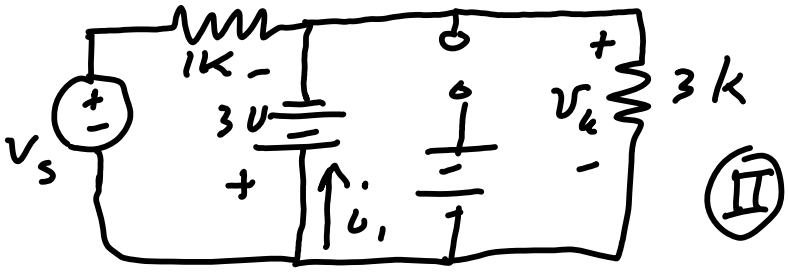
$i_2 = \frac{v_S - 6}{1k} - 2$ mA

$i_2 > 0$ when $v_S > 8$

(III)

Both can't be on...

If D_1 is on, D_2 is off



(II)

Here $v_a = -3$ V

$i_1 = \frac{-3 - v_S}{1K} + \frac{-3}{3K}$

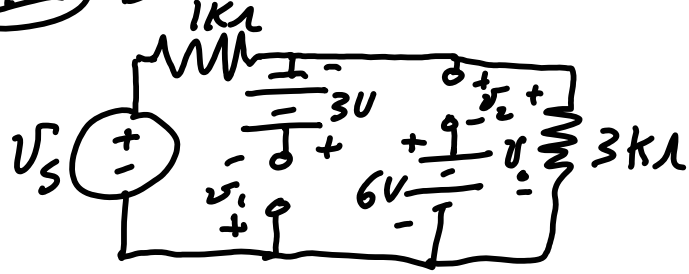
$= -3\text{mA} - \frac{v_S}{1K} - 1\text{mA} > 0$

when $\frac{-v_S}{1K} > 4$ mA

$-v_S > 4$ V

$v_S < -4$

(III) Both can be off



$v_a = \frac{3}{4} v_S$

$v_1 = -v_a - 3$

$= -\frac{3}{4} v_S - 3$

$v_1 < 0$ when $-\frac{3}{4} v_S < 3$

$v_S > -4$

$v_2 = v_a - 6$

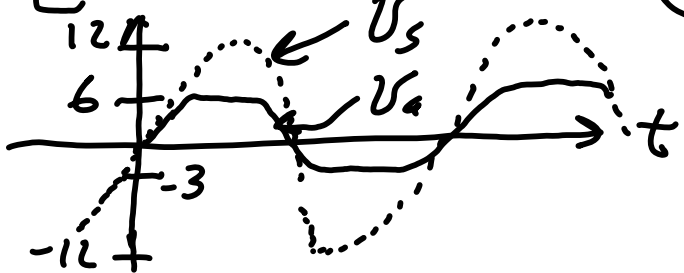
$= \frac{3}{4} v_S - 6$

$v_2 < 0$ when $\frac{3}{4} v_S - 6 < 0$

$\frac{3}{4} v_S < 6$

$v_S < 8$

So, $v_o = \begin{cases} -3 \text{ V} & v_S < -4 \\ \frac{3}{4} v_S \text{ V} & -4 \le v_S \le 8 \\ 6 \text{ V} & v_S \ge 8 \end{cases}$



8. (0 points) FoEE 6.31

6.31 For the diode circuit shown in Fig. P6.31, D_1 and D_2 are silicon diodes with saturation currents of 5 nA and 10 nA, respectively, at 300 K. Given that both diodes are reverse biased, find v_1 and v_2.

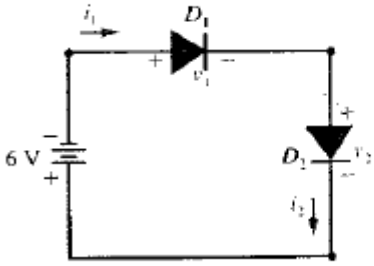
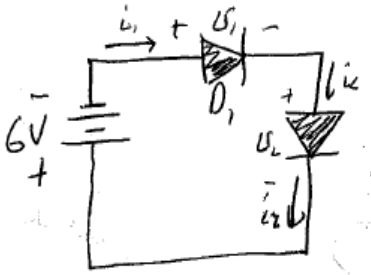


Fig. P6.31



We are given saturation currents of 5nA for D_1 and 10nA for D_2.

We know that neither diode can allow more negative current than its negative I_s.

So, $i_1 = -5\,nA$

$i_2 = -5\,nA$

$v_2 = \eta V_T \ln\left(\frac{i_2}{I_{s2}} + 1\right) = 2\,\frac{300}{11{,}586}\ln\left(\frac{-5\,nA}{10\,nA} + 1\right) = -0.036$

By KVL $v_1 = -5.964\,V$, $v_2 = -0.036\,V$

9. (0 points) FoEE 6.32

6.32 For the diode circuit shown in Fig. P6.32, D_1 and D_2 are silicon diodes having saturation currents of 5 nA and 10 nA, respectively, at 300 K. Given that both diodes are forward biased, find the value of R for which the current is 15 mA.

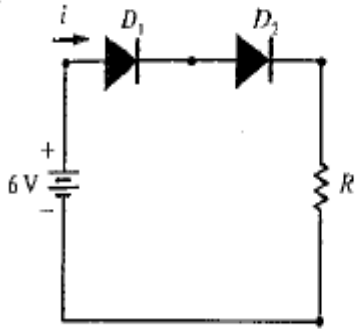
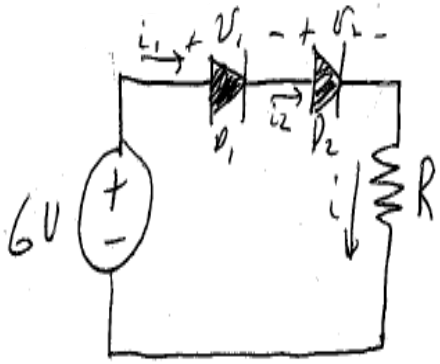


Fig. P6.32



Find R that yields the current of 15mA.

If $i = 15\,mA$, $i_1 = i_2 = 15\,mA$

$v_1 = \eta V_T \ln\left(\frac{15\,mA}{5\,nA} + 1\right) = 0.772\,V$

$v_2 = \eta V_T \ln\left(\frac{15\,mA}{10\,nA} + 1\right) = 0.736\,V$

$\therefore$ By KVL $v_R = 6 - 0.772 - 0.736 = 4.49\,V$

$R = \frac{v_R}{i} = \frac{4.49}{15\,mA} = 299\,\Omega$