Electronic Circuits

ELEC 301

Mini-Project 1

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2020-10-7

Part I

$$T(s) = \frac{V_o(s)}{V_s(s)} = 0.125\times\frac{10^5/\text{sec}}{s + 10^5/\text{sec}}\times\frac{10^6/\text{sec}}{s + 10^6/\text{sec}}\times\frac{10^7/\text{sec}}{s + 10^7/\text{sec}}$$

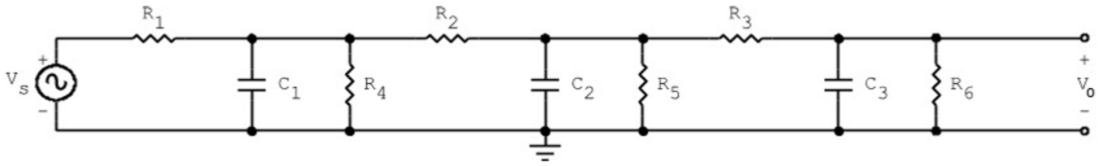

Figure 1. A three-pole low-pass filter circuit with the transfer function.

(A)

The mid-band gain is 0.125. After all the high-frequency capacitors are opened and all low-frequency capacitors are shorted, the voltage of R6 (Vo) is 0.125 pu and Vs is 1.0 pu (knowledge from ELEC 342). Thus, the resistance of R6 is 1k since the sum of the resistance is 8k. The circuit is a three cascaded voltage divider, and after KCL and KVL calculations, the resistances of two sub-branches (R4, R5) can be determined (two 2k resistors).

Given C1>C2>C3, which means C1 has the lowest frequency, C3 has the highest frequency.

$\omega_{c1} = 10^5$ rad/sec $\qquad$ $\omega_{c2} = 10^6$ rad/sec $\qquad$ $\omega_{c3} = 10^7$ rad/sec

When the frequency is 10^5 rad/sec, the open-circuit test is applied. All other high frequency capacitors are replaced bp open-circuits. The view from C1 is:

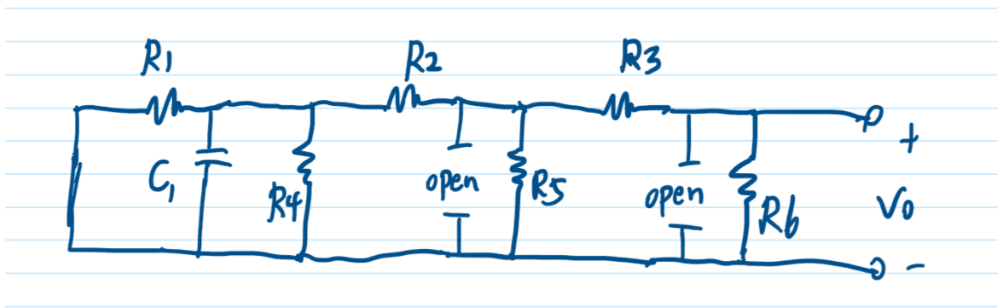

Figure 2. The view of C1 when the frequency is 10^5 rad/sec

$\tau^{oc}_{C1} = [\{(R3+R6)//(R2+R5)\}//R4\}//R1] * (C1) = 1/\omega_{c1} = 1/10^5$, C1 = $\boxed{\textbf{23.3 nF}}$

Then the frequency raises to 10^6 rad/sec, C1 is shorted and C3 is open. The view from C2 is:

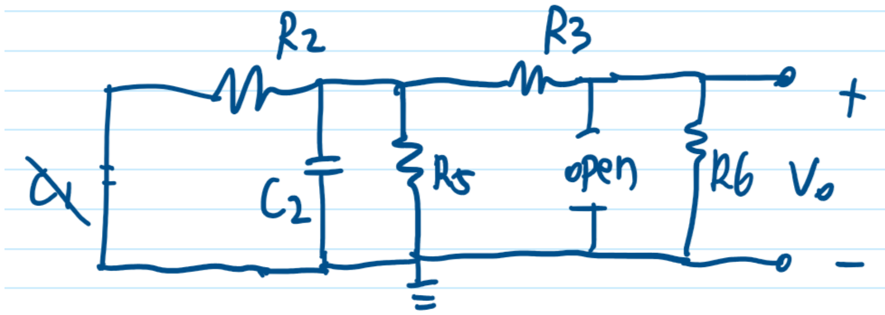

Figure 3. The view of C2 when the frequency is 10^6 rad/sec

$\tau^{oc}_{C2} = \{R2//[R5//(R3+R6)]\} *(C2) = 1/\omega_{c2} = 1/10^6$, $\boxed{\textbf{C2 = 2.0 nF}}$

The frequency then increases to the highest frequency which is 10^7 rad/sec. In this case, C1 and C2 are shorted. The view from C3 is:

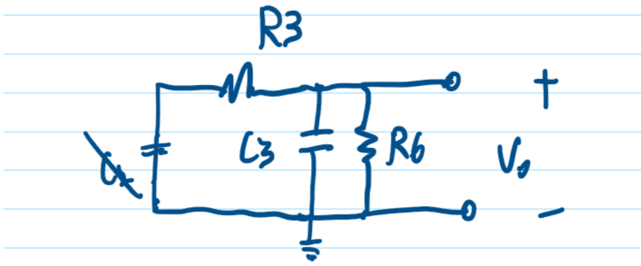

Figure 4. The view of C3 when the frequency is 10^7 rad/sec

$\tau^{oc}_{C3} = (R3//R6)*(C3) = 1/\omega_{c3} = 1/10^7$, $\boxed{\textbf{C3 = 0.20 nF}}$

The **AC Simulation** by *CircuitMaker* is:

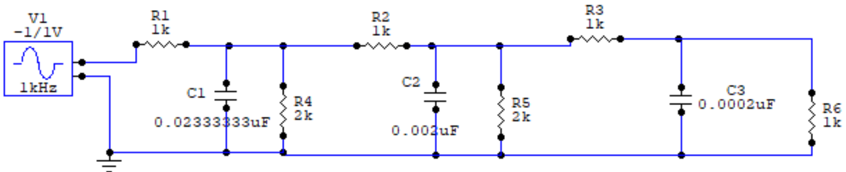

Figure 5. The AC Simulation of the designed circuit

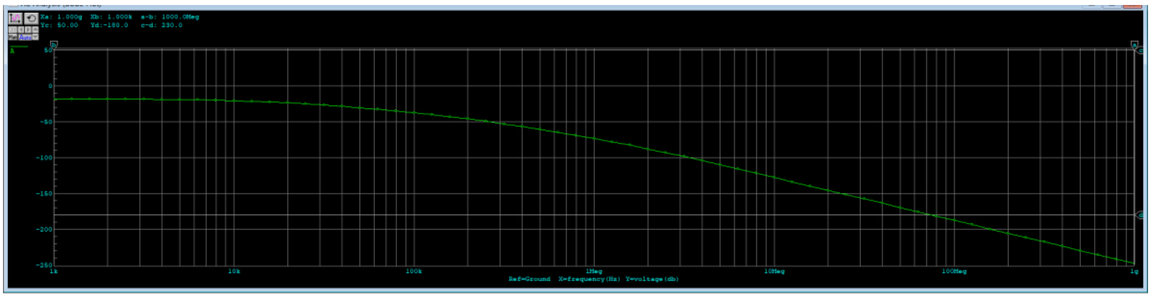

Figure 6. The magnitude of the Bode plots

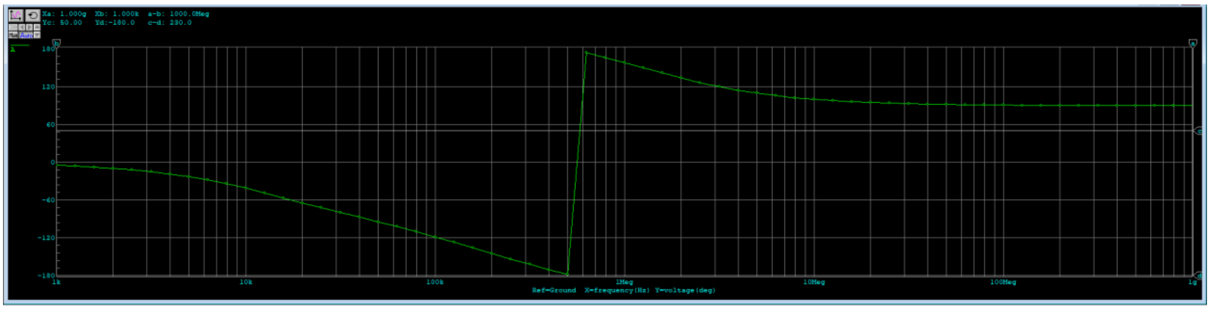

Figure 7. The phasor of the Bode plots

(B)

After factoring the transfer function:

$$T(s) = \frac{0.125 * 10^{18}}{S^3 + 1.11*10^7 *S^2 + 1.11*10^{12} *S +1.0*10^{18}}$$

The SXFER circuit is:

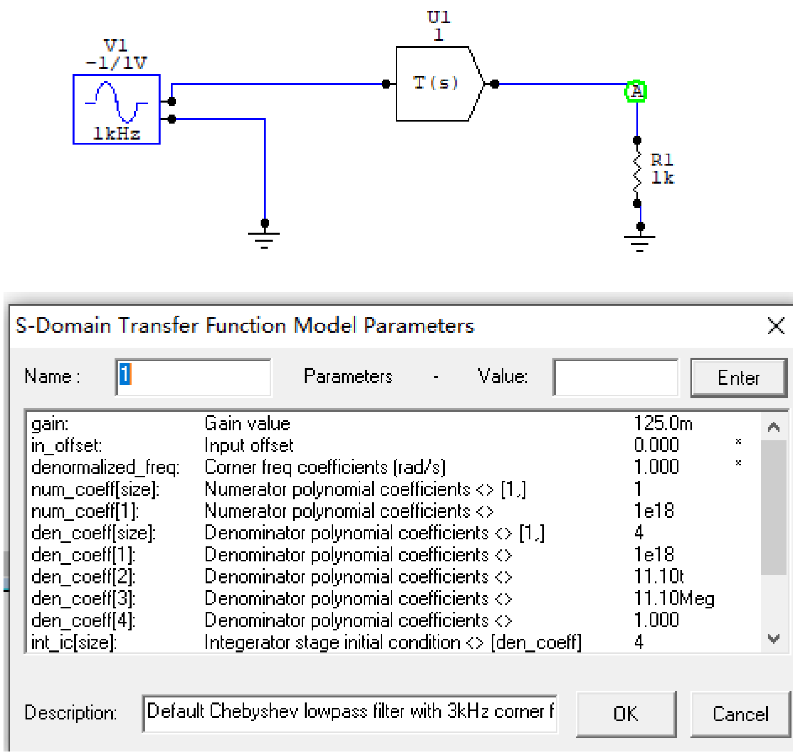

Figure 8. The SXFER circuit and the parameters

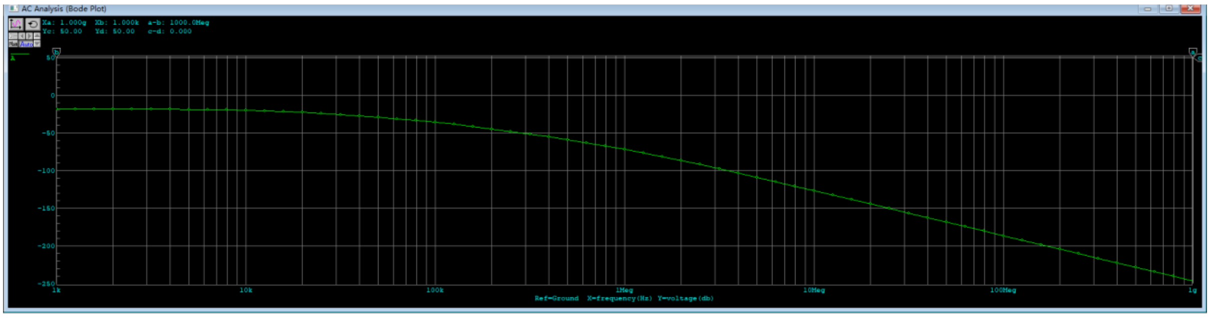

Figure 9. The magnitude of Bode plot of SXFER circuit

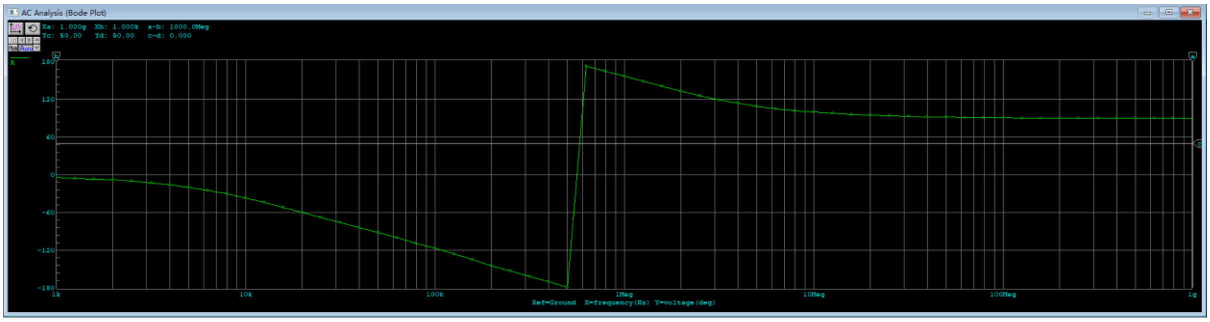

Figure 10. The phasor of Bode plot of SXFER circuit

As shown above, the Bode plots of SEFER is **the same** as the Bode plots from Part (A).

Part II

(A)

The AC Simulation in *Circuitmaker:*

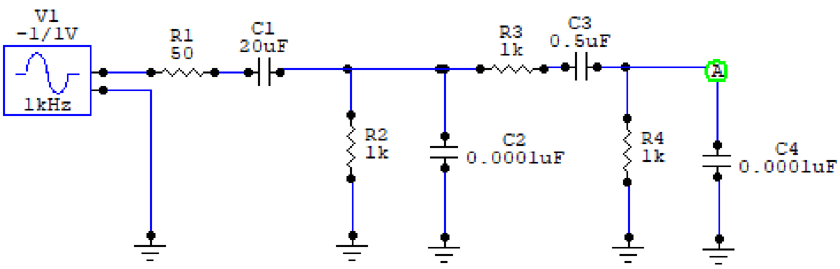

Figure 11. The simulation circuit in *circuitmaker*

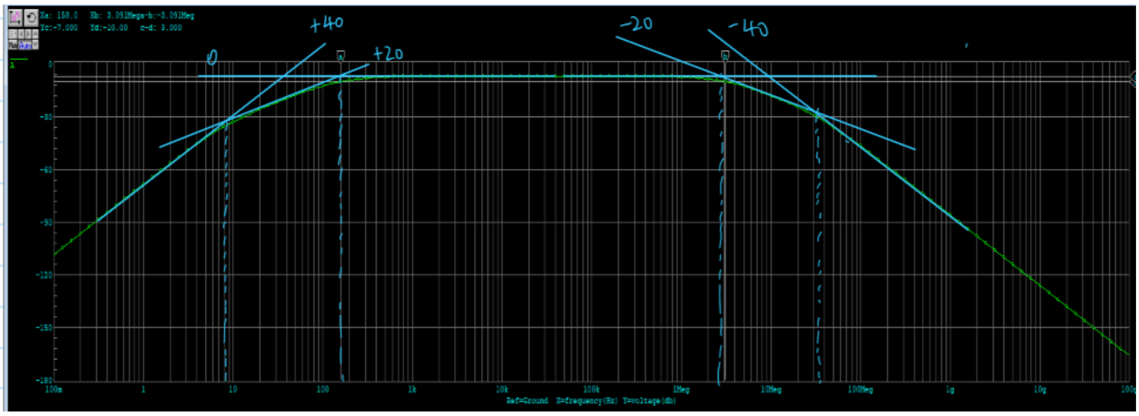

Figure 12. The magnitude of Bode plot of the 4-pole circuit

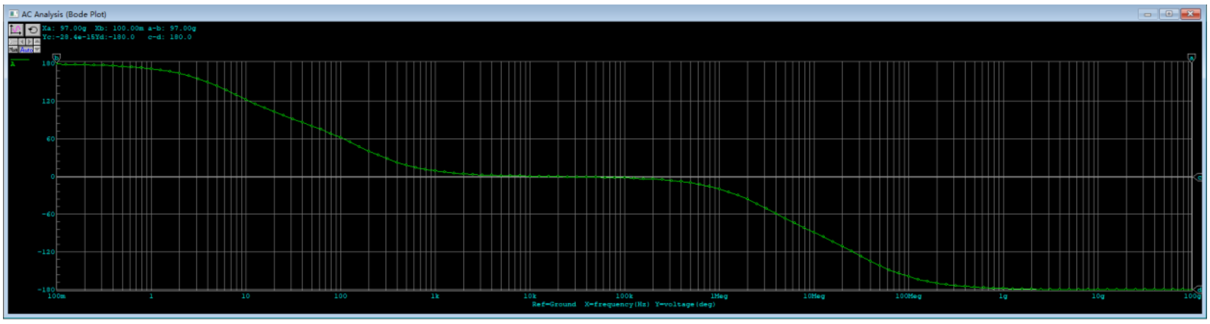

Figure 13. The phasor of Bode plot of the 4-pole circuit

From **Figure 12**, the locations of each poles are marked in the figure, and the corresponding frequencies can be graphically identified: $\boldsymbol{\omega_1}$ is the frequency at which the +40 dB/dec slope intersects with the +20 dB/dec. $\boldsymbol{\omega_2}$ is the point at which the slope becomes 0 from +20 dB/dec. ω_3 is the third pole that the slope starts to decreases to -20dB/dec. ω_4 is the fourth pole at which the slope falls to -40 dB/dec

$\omega_1 = \mathbf{8.456}$ Hz	$\omega_2 = \mathbf{167.9}$ Hz	$\omega_3 = \mathbf{2.736M}$ Hz	$\omega_4 = \mathbf{32.85M}$ Hz

(B)

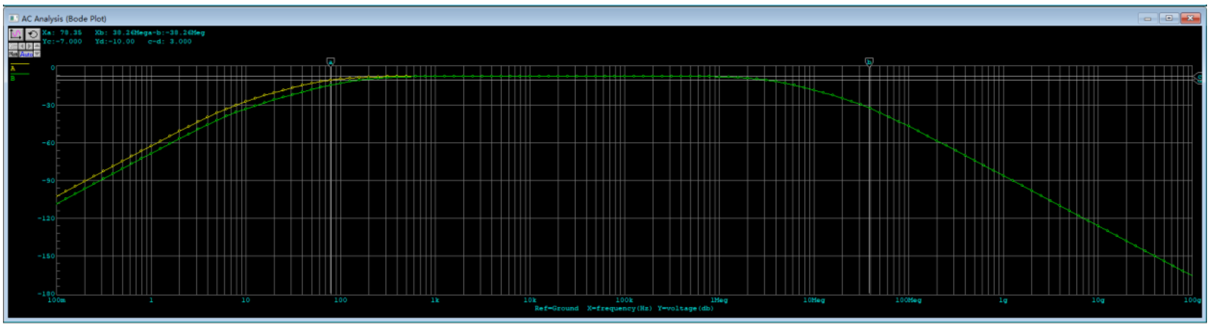

Figure 14. The magnitude of Bode plot with C3 is 500 nF (green) and 1 uF (yellow)

As Figure 14 shown, when the capacitance of C3 is increased, the low 3dB frequency is lower, which means this band-pass filter has a greater bandwidth.

From the simulations, the low 3-dB cutoff frequency is shown in the table below.

Table 1. The capacitances with the corresponding low-3dB frequencies.

C3 (uF)	0.5	1.0	2.0	5.0	10.0
ω_{L3dB} (Hz)	158.00	82.02	44.57	22.44	16.54

The relationship between capacitance of the capacitors is C1 > C3 > C2 = C4. Even though the value of C3 is increased, the relationship will not be changed. Therefore, C1 will always be the Low frequency pole 1. C2 and C4 will always be opened.

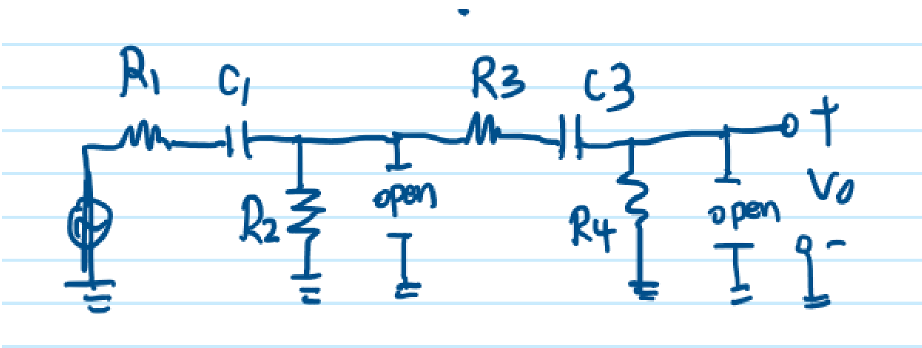

Figure 15. The diagram of open/short test circuit.

When the frequency is at the threshold of C1, all C2, C3 and C4 are opened. For C1:

τ^{sc}_{C1} = (R1 + R2)*(C1) = (1050)*(20*10^{-6}) = 0.021 s

$\omega_{Lp1} = 1/\tau^{sc}_{C1}$ = 47.62 rad/s

<u>When the frequency is for C3 = 0.5 uF, C1 is shorted, C2 and C4 are opened. For **C3 = 0.5 uF:**</u>

$$\tau^{sc}_{C3} = (R1//R2 + R3 + R4)*(C3) = (2047.62)*(0.5*10^{-6}) = 0.001024 \text{ s}$$

$$\omega_{Lp2} = 1/\tau^{sc}_{C3} = 976.74 \text{ rad/s}$$

$$\omega_{Lp3dB} = \sqrt{(\omega Lp1)^\wedge 2 + (\omega Lp2)^\wedge 2} = \sqrt{47.62^2 + 976.74^2} = \boxed{\textbf{977.90 rad/s = 155.64 Hz}}$$

$$\text{Error\%} = \frac{|Calculated - Simulated|}{Simulated} * 100\% = \frac{|155.64Hz - 158.00Hz|}{158.00\ Hz} * 100\% = \boxed{\textbf{1.49\%}}$$

When the frequency is for C3 = 1.0 uF, C1 is shorted, C2 and C4 are opened. For **C3 = 1.0 uF:**

τ^{sc}_{C3} = (R1//R2 + R3 + R4)*(C3) = (2047.62)*(1.0*10^{-6}) = 0.002048 s

$\omega_{Lp2} = 1/\tau^{sc}_{C3}$ = 488.37 rad/s

$$\omega_{Lp3dB} = \sqrt{(\omega Lp1)^\wedge 2 + (\omega Lp2)^\wedge 2} = \sqrt{47.62^2 + 488.37^2} = \boxed{\textbf{490.69 rad/s = 78.10 Hz}}$$

$$\text{Error\%} = \frac{|Calculated - Simulated|}{Simulated} * 100\% = \frac{|78.10Hz - 82.02Hz|}{82.02\ Hz} * 100\% = \boxed{\textbf{4.78\%}}$$

When the frequency is for C3 = 2.0 uF, C1 is shorted, C2 and C4 are opened. For **C3 = 2.0 uF:**

τ^{sc}_{C3} = (R1//R2 + R3 + R4)*(C3) = (2047.62)*(2.0*10^{-6}) = 0.004095 s

$\omega_{Lp2} = 1/\tau^{sc}_{C3}$ = 244.19 rad/s

$$\omega_{Lp3dB} = \sqrt{(\omega Lp1)^\wedge 2 + (\omega Lp2)^\wedge 2} = \sqrt{47.62^2 + 244.19^2} = \boxed{\textbf{248.79 rad/s = 39.60 Hz}}$$

$$\text{Error\%} = \frac{|Calculated - Simulated|}{Simulated} * 100\% = \frac{|39.60Hz - 44.57Hz|}{44.57\ Hz} * 100\% = \boxed{\textbf{11.15\%}}$$

When the frequency is for C3 = 5.0 uF, C1 is shorted, C2 and C4 are opened. For **C3 = 5.0 uF:**

τ^{sc}_{C3} = (R1//R2 + R3 + R4)*(C3) = (2047.62)*(5.0*10^{-6}) = 0.01024 s

$\omega_{Lp2} = 1/\tau^{sc}_{C3}$ = 97.67 rad/s

$$\omega_{Lp3dB} = \sqrt{(\omega Lp1)^\wedge 2 + (\omega Lp2)^\wedge 2} = \sqrt{47.62^2 + 97.67^2} = \boxed{\textbf{108.66 rad/s = 17.29 Hz}}$$

$$\text{Error\%} = \frac{|Calculated - Simulated|}{Simulated} * 100\% = \frac{|17.29Hz - 22.44Hz|}{22.44\ Hz} * 100\% = \boxed{\textbf{22.95\%}}$$

When the frequency is for C3 = 10 uF, C1 is shorted, C2 and C4 are opened. For **C3 = 10 uF:**

τ^{sc}_{C3} = (R1//R2 + R3 + R4)*(C3) = (2047.62)*(1.0*10^{-5}) = 0.02048 s

$\omega_{Lp2} = 1/\tau^{sc}_{C3}$ = 48.84 rad/s

$$\omega_{Lp3dB} = \sqrt{(\omega Lp1)^\wedge 2 + (\omega Lp2)^\wedge 2} = \sqrt{47.62^2 + 48.84^2} = \boxed{\textbf{68.21 rad/s = 10.86 Hz}}$$

$$\text{Error\%} = \frac{|Calculated - Simulated|}{Simulated} * 100\% = \frac{|10.86Hz - 16.54Hz|}{16.54\ Hz} * 100\% = \boxed{\textbf{34.34\%}}$$

Table 2. The capacitances with the corresponding low-3dB frequencies and the error %.

C3 (uF)	0.5	1.0	2.0	5.0	10.0
ω_{L3dB} (Hz) Sim	158.00	82.02	44.57	22.44	16.54
ω_{L3dB} (Hz) Cal	155.64	78.10	39.60	17.29	10.86
Error (%)	1.49	4.78	11.15	22.95	34.34

As shown in Table 2, the Low 3-dB cut-off frequency is lower when the capacitance of C3 is higher. In addition, the percent error is raised as the capacitance of C3 is increased.

Part III

(A)

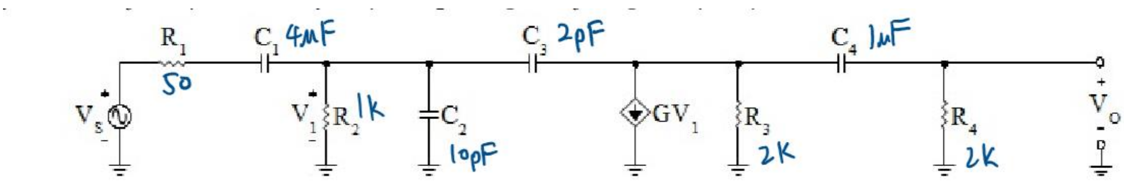

Figure 16. Basic Transconductance Amplifier

To find the mid-pass gain, all low-frequency capacitors are shorted, and all high-frequency capacitors are opened. In the circuit, C1 (4uF) and C4 (1uF) are the low-frequency capacitors. C2 (10 pF) and C3 (2 pF) are the high-frequency capacitors. For mid-pass gain, the circuit becomes:

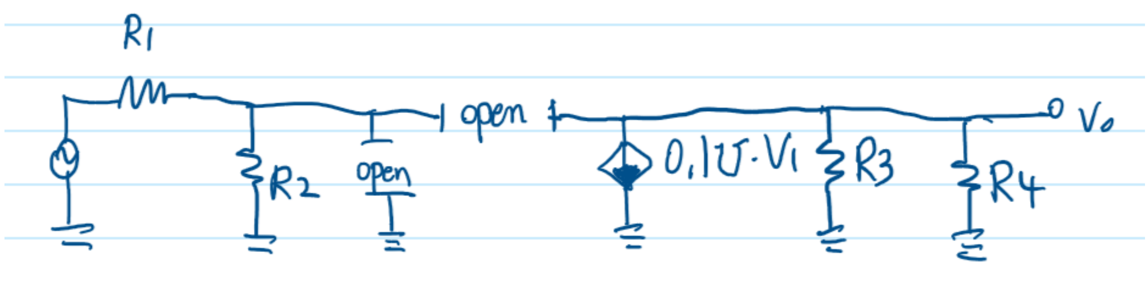

Figure 17. The mid-pass gain circuit

Applying the **Miller's Theorem** on C3, *k* is calculated by Vo/V1:

$$\frac{Vo}{V1} = \frac{-0.1\mho V1 * (\mathrm{R3//R4})}{V1} = k = -100$$

According to **Miller's Theorem**, Z1 = Z/(1-*k*), Z2 = Z**k*/(*k*-1).

$$Z1 = \frac{\frac{1}{jwC}}{1-k} = \frac{1}{jwC*(1-k)}$$, thus, C_{Z1} = C3 * (1-k) = 202.0 pF

$$Z2 = \frac{\frac{1}{jwC}}{1-1/k} = \frac{1}{jwC*(1-1/k)}$$, thus, C_{Z2} = C3 * (1-1/k) = 2.02 pF

After applying **Miller's Theorem**, the left (input) side of the circuit is:

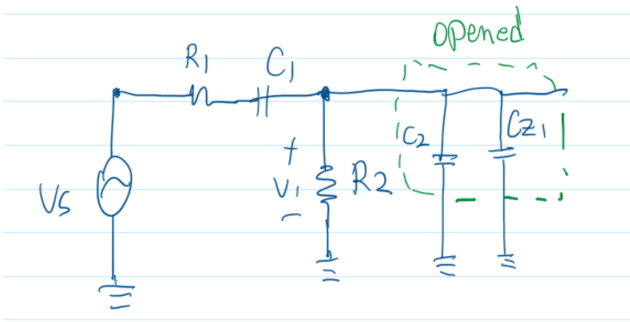

Figure 18. The input side of the circuit

In **Figure 18**, C1 is shorted because it is the low frequency capacitor. C2 and C_{Z1} are opened since they are the high frequency capacitors. To get the mid band gain:

$$Am = \frac{Vo}{Vs} = \frac{Vo}{V1} * \frac{V1}{Vs}$$

$$\frac{V1}{Vs} = \frac{R2}{R1+R2} = 1000/(1000+50) = 0.952$$

$$Am = \frac{Vo}{V1} * 0.952 = -100*0.952 = \boxed{\mathbf{-95.24}}$$

From Figure 18, C2 and C_{Z1} can be treat as a single capacitor C', C' = C2 +C_{Z1} = 212.0 pF, which is a high-frequency capacitor.

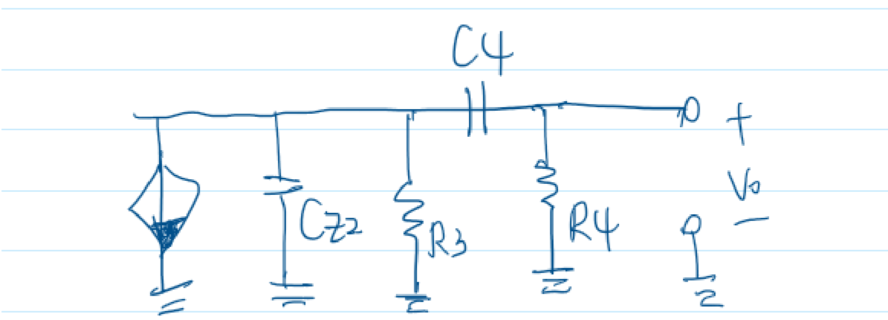

Figure 19. The output (right) side of the circuit

In **Figure 19**, C_{Z2} is a high frequency capacitor. To find poles and zeros, low or high frequency is considered.

At low frequency (for C1 in **Figure 18**), C' is opened. Therefore:

$$\omega_{Lp1} = \frac{1}{\tau = 4uF*(R1+R2)} = \boxed{238.10 \text{ rad/sec} = 37.90 \text{ Hz}}$$

for C4 in **Figure 19**, C_{Z2} is opened.

$$\omega_{Lp2} = \frac{1}{\tau = 1uF*(R3+R4)} = \boxed{250.00 \text{ rad/sec} = 39.79 \text{ Hz}}$$

At high frequency (for C' in **Figure 18**), C1 is shorted.

$$\omega_{Hp1} = \frac{1}{\tau = 212.0pF*(R1//R2)} = \boxed{9.91*10^{7} \text{ rad/sec} = 1.577*10^{7} \text{ Hz}}$$

for C_{Z2} in **Figure 19**, C4 is shorted.

$$\omega_{Hp2} = \frac{1}{\tau = 2.02pF*(R3//R4)} = \boxed{4.95*10^{8} \text{ rad/sec} = 7.878*10^{7} \text{ Hz}}$$

$$T(s) = -95.24 * \frac{s}{s+238.10} * \frac{s}{s+250.00} * \frac{9.91*10^{7}}{s+9.91*10^{7}} * \frac{4.95*10\text{^}8}{s+4.95*10\text{^}8}$$

(B)

The figures below show the AC simulation circuits using *Circuitmaker*.

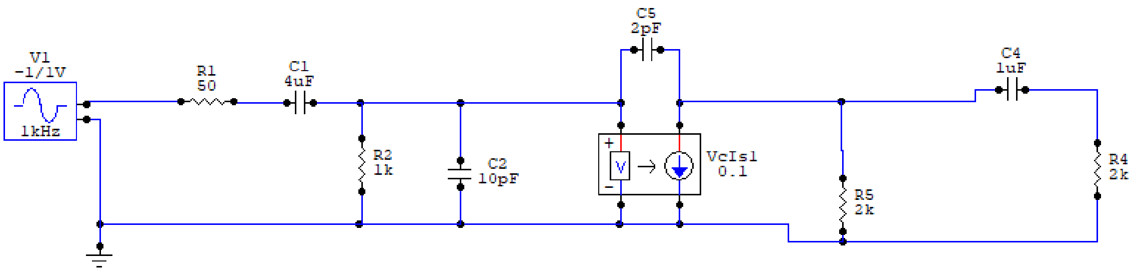

Figure 20. The circuit BEFORE applying the Miller's Theorem

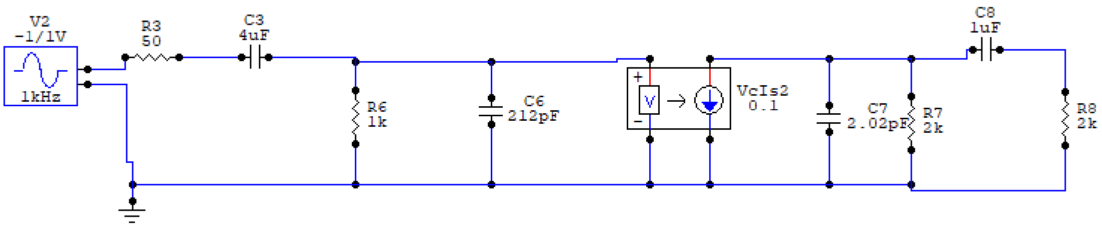

Figure 21. The circuit AFTER applying the Miller's Theorem

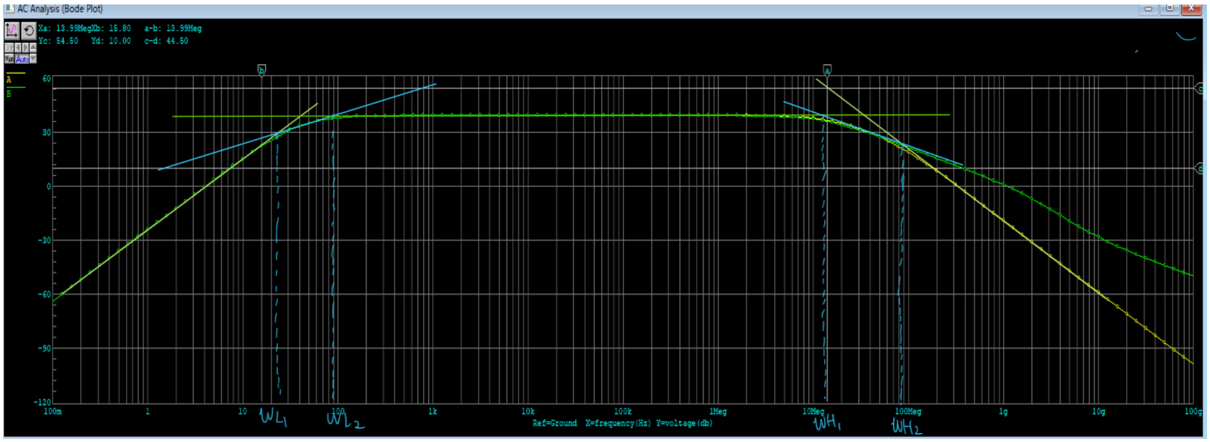

Figure 22. The magnitude of Bode Plot of the circuits

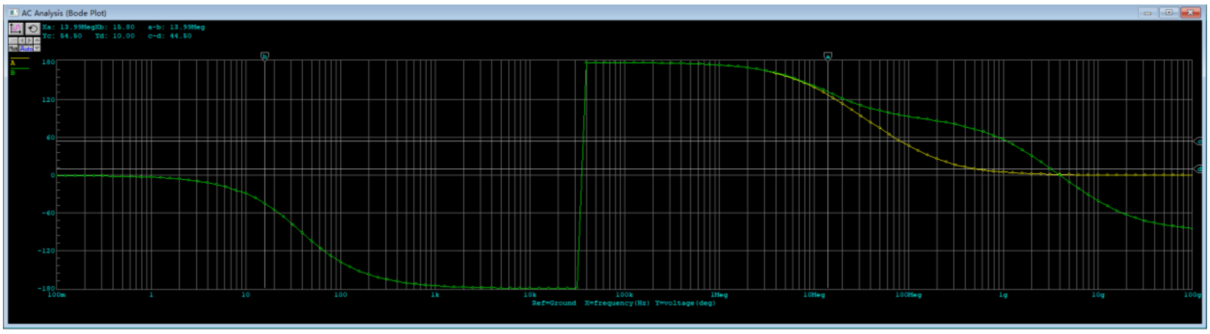

Figure 23. The phasor of Bode Plot of the circuits

In **Figure 22** and **Figure 23**, the green line represents the plot of the initial circuit. The yellow line represents the circuit after applying the **Miller's Theorem**.

As **Figure 22** shown, the simulated frequencies can be graphically got by approximation. From the approximation:

$$\boxed{\omega_{Lp1} = 33.36\ \text{Hz}}$$

$$\text{Error\%} = \frac{|Calculated - Simulated|}{Simulated} * 100\% = \frac{|37.90Hz - 33.36Hz|}{33.36\ Hz} * 100\% = \boxed{13.61\%}$$

$$\boxed{\omega_{Lp2} = 57.75 \text{ Hz}}$$

$$\text{Error\%} = \frac{|Calculated - Simulated|}{Simulated} * 100\% = \frac{|39.79Hz - 57.75Hz|}{57.75\ Hz} * 100\% = \boxed{31.10\ \%}$$

$$\boxed{\omega_{Hp1} = 13.57\text{M Hz}}$$

$$\text{Error\%} = \frac{|Calculated - Simulated|}{Simulated} * 100\% = \frac{|15.77MHz - 13.57MHz|}{13.57M\ Hz} * 100\% = \boxed{16.21\%}$$

$$\boxed{\omega_{Hp2} = 76.00\text{M Hz}}$$

$$\text{Error\%} = \frac{|Calculated - Simulated|}{Simulated} * 100\% = \frac{|78.78MHz - 76.00MHz|}{76.00M\ Hz} * 100\% = \boxed{3.66\%}$$

The Low 3-dB cut-off frequency can be calculated:

$$\omega_{Lp3dB} = \sqrt{\omega Lp1^2 + \omega Lp2^2}$$

$$\omega_{Lp3dB} = \sqrt{37.9\text{^}2 + 39.79\text{^}2} = \boxed{54.95 \text{ Hz}}$$

The calculated Low 3dB frequency and the simulated Low 3dB frequency are shown in the **Table 8** in the following.

The High 3-dB cut-off frequency can be calculated:

$$\tau_{H3dB} = \sqrt{\tau Hp1\text{^}2 + \tau Hp2\text{^}2}$$

$$\tau_{H3dB} = \sqrt{\left(\frac{1}{15.77M}\right)\text{^}2 + \frac{1}{(78.78M)}\text{^}2} = 0.06467 \text{ us}$$

$$\omega_{Hp3dB} = \frac{1}{\tau H3dB} = \boxed{15.46\text{M Hz}}$$

The calculated High 3dB frequency and the simulated High 3dB frequency are shown in the **Table 3** in the following.

Table 3. The variations between calculated values and simulated values

Poles / Zeros	Calculated (Hz)	Simulated (Hz)	Error%
ω_{Lp1}	37.90	33.36	13.61%
ω_{Lp2}	39.79	57.75	31.10%
ω_{Lp3dB}	$\boxed{54.95}$	$\boxed{66.69}$	$\boxed{17.60\%}$
ω_{Hp1}	15.77M	13.57M	16.21%
ω_{Hp1}	78.78M	76.00M	3.66%
ω_{Hp3dB}	$\boxed{15.46M}$	$\boxed{14.20M}$	$\boxed{8.87\%}$

Table 3 shows the frequency of each poles and the Low/High 3-dB frequency. The errors between the calculated values and the simulated values are shown at the last column in **Table 3**.

Conclusion

In part I, the circuit is designed by determining the resistance of resistors and the capacitance of capacitors. The designed circuit fulfills the given transfer function. In addition, SXFER transfer function block is designed and used in *Circuitmaker* to simulate the same circuit. In part II, the capacitance of one capacitor is changed. The effects of various low frequency capacitor will influence the low-3dB cut-off frequency. The higher capacitance, lower low-3dB cut-off frequency. In part III, the Miller's Theorem and open/short time constant are used to calculate the frequency of each pole. The circuit is also simulated in *Circuitmaker*. The linear approximation is used to graphically find the poles and zeros. The percent error between calculated and simulated Low/High 3-dB frequency are calculated and listed in a table. The mini-project enforces the memory of fundamental Bode Plot knowledge which will be used in the future.