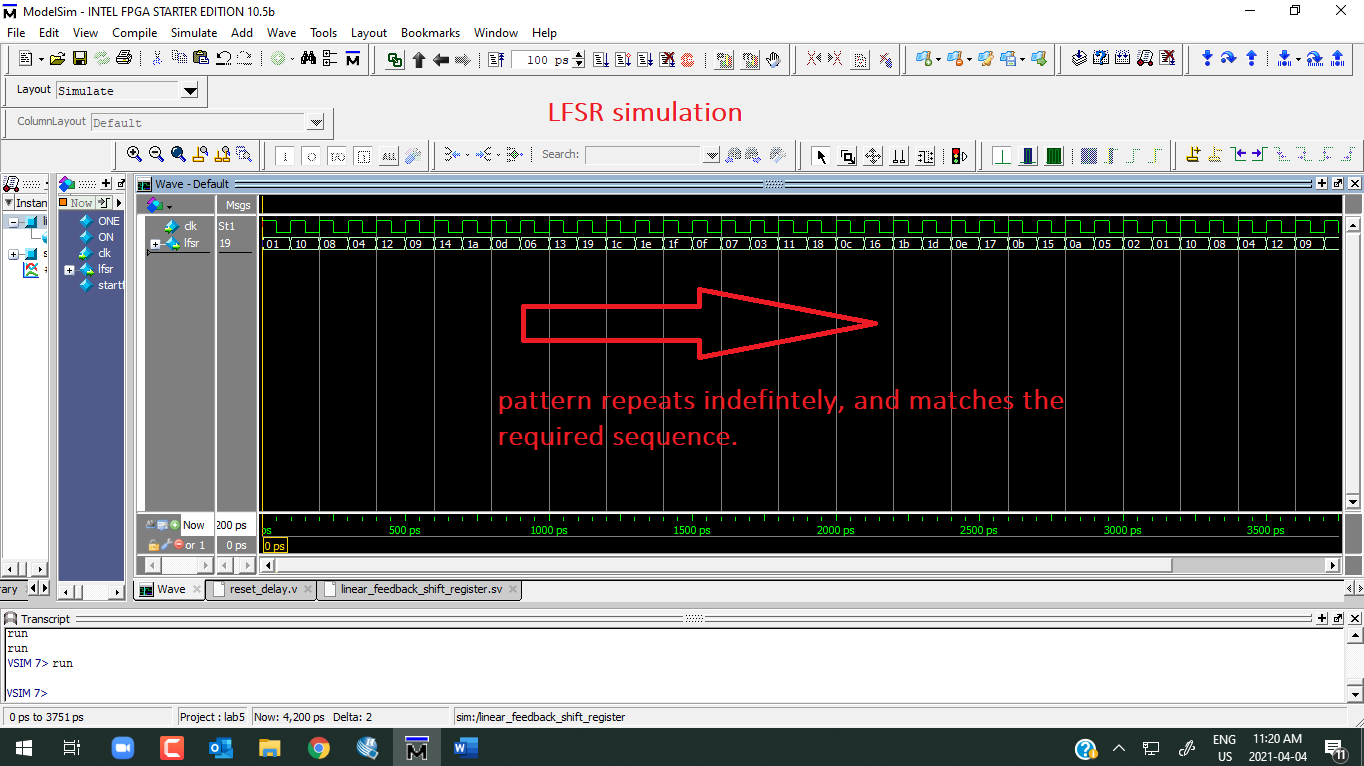
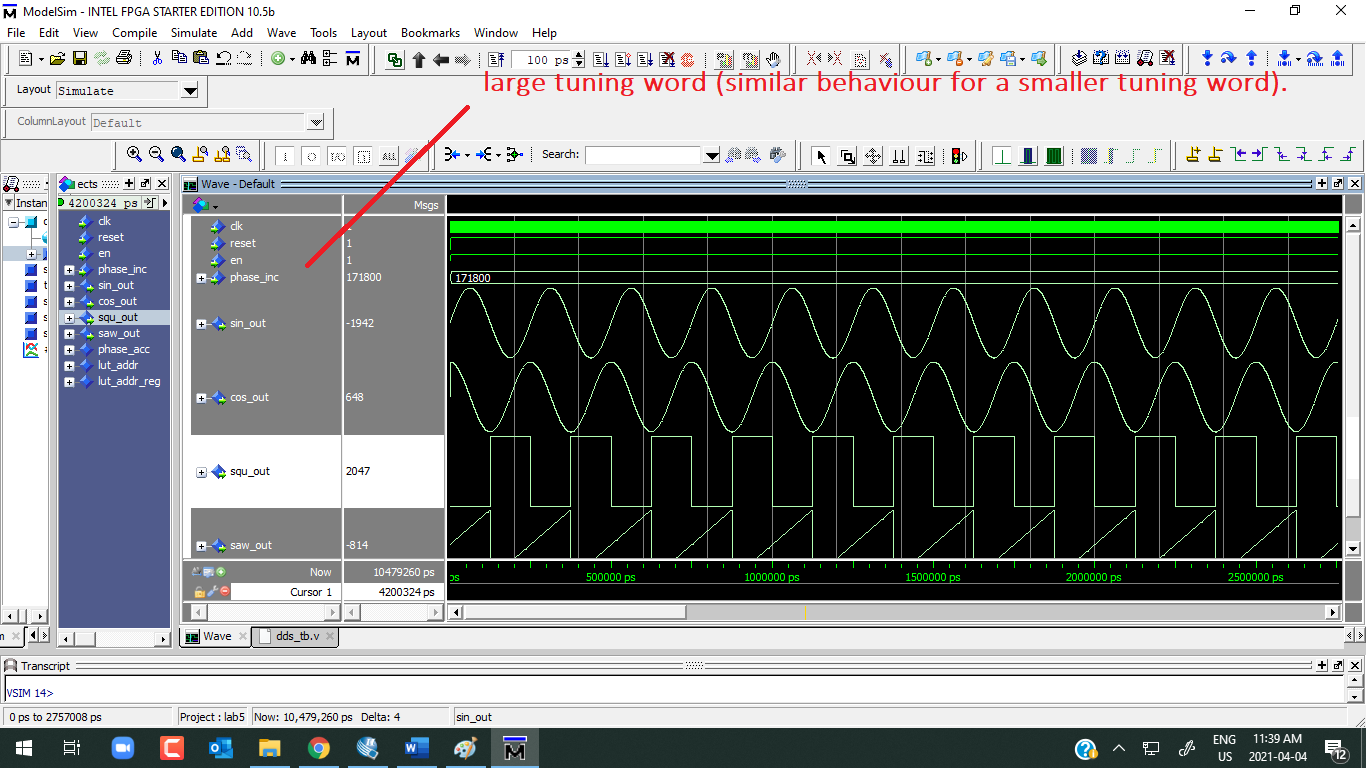
Simulations

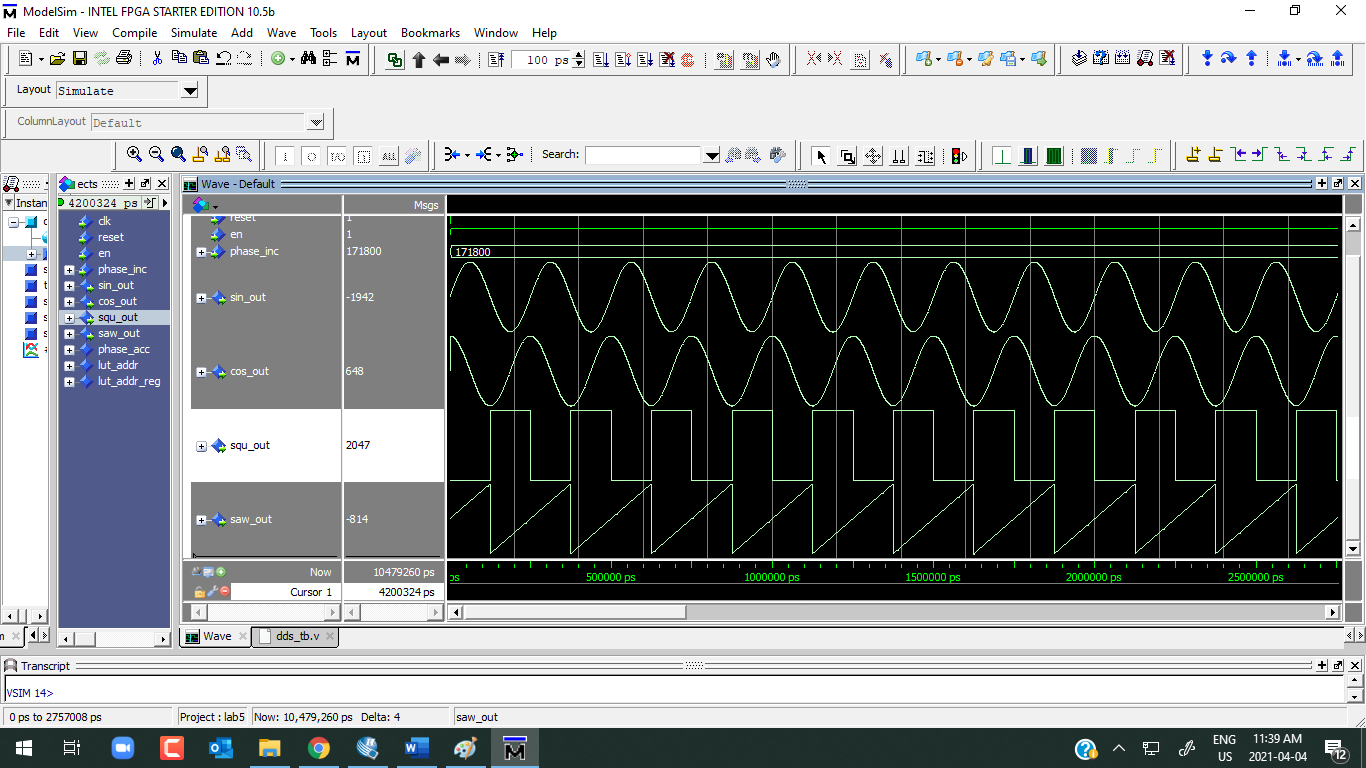
LFSR Simulations:

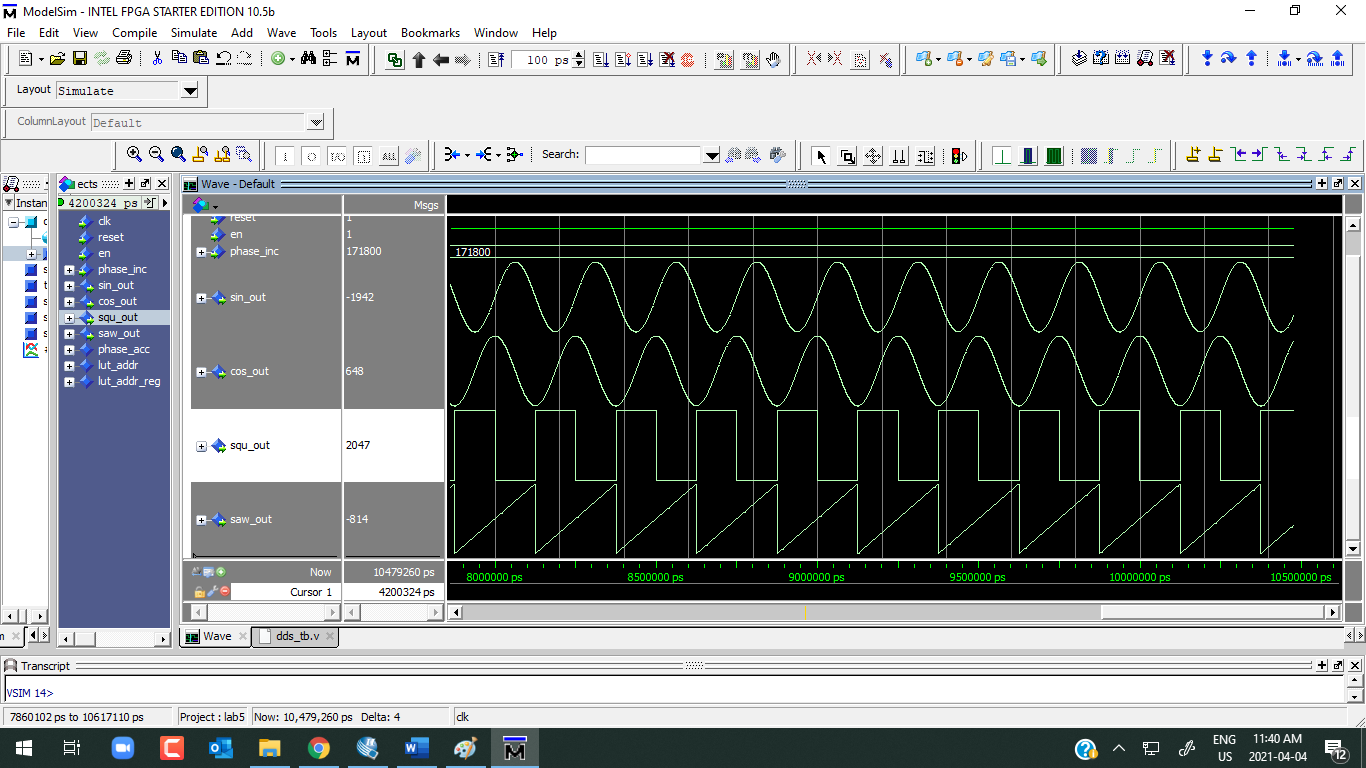


DDS:

Due to a very small tuning word, ModelSim kept crashing during simulation, as the sampled data was large, hence I chose a larger tuning word. Wave frequency: 2000 Hz





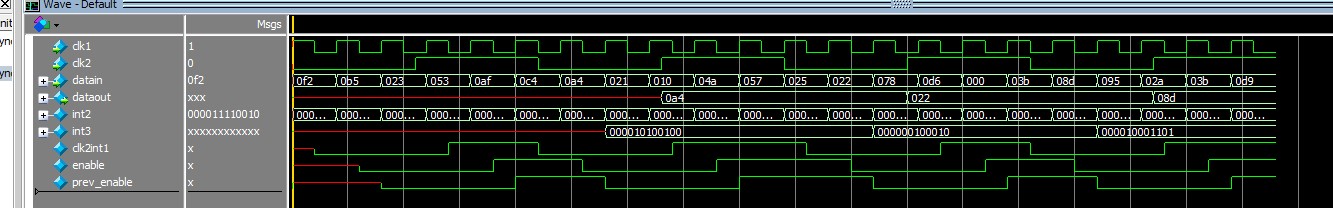


Clock Domain Crossing (Higher Frequency to lower Frequency Clock Crossing):

Module used from slides, below in a series of screenshots.

Note the screenshots below are obtained for our NEW CDC logic

CDC:



This module is used for allowing a signal from HIGH speed clock to a LOW speed clock. The module is from CPEN311 lecture 7c. It can be seen in the figure that the output data is changed when the posedge of the LOW clock. The output data depends on the enable signal. The output data got the input data when the negedge of the enable (not when enable = 1). As shown above, the first negedge of the enable captures the input data a4, then the first output data is a4. The second negedge of enable is 22, and the second output data is 22. Both input data and output data are in hex. This waveform is exactly the same as the waveform in the lecture silde.

**Note the screenshots below were obtained before for our older CDC. I decided to keep them in the slides, since they convey a very important concept, and are technically similar.**

