Assignment 5

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1 Question 1

The Finite State Machine from assignment 1/2 is called washer machine which controls the basic functions of a modern washing and drying machine. The inputs are the clock, the mode selection, the water indicator (indicating the water level in the drum) and the door lock signal (indicating the status of the drum door). The outputs include the spin signal, the in water signal, the channel open signal (controlling the channel to drain the water in the drum) and the heater signal. The more detailed explanation and description is in the assignment 1 report.

The test files are below:

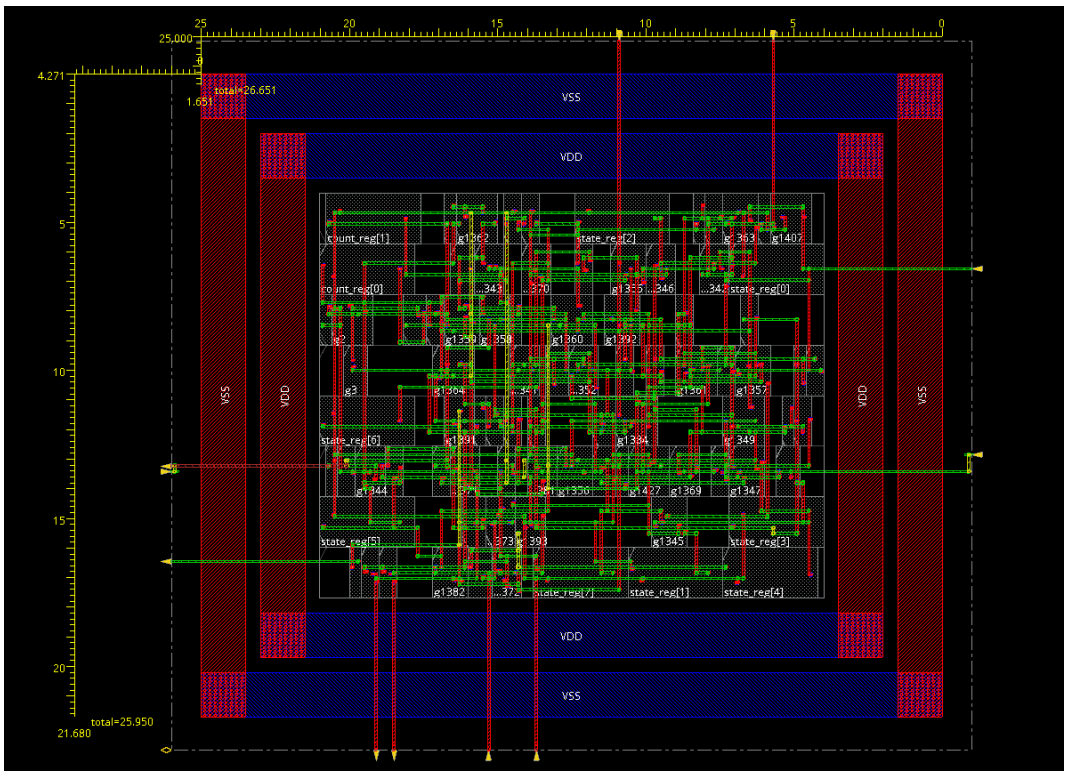

Figure 1: The synthesized circuit with dimensions.

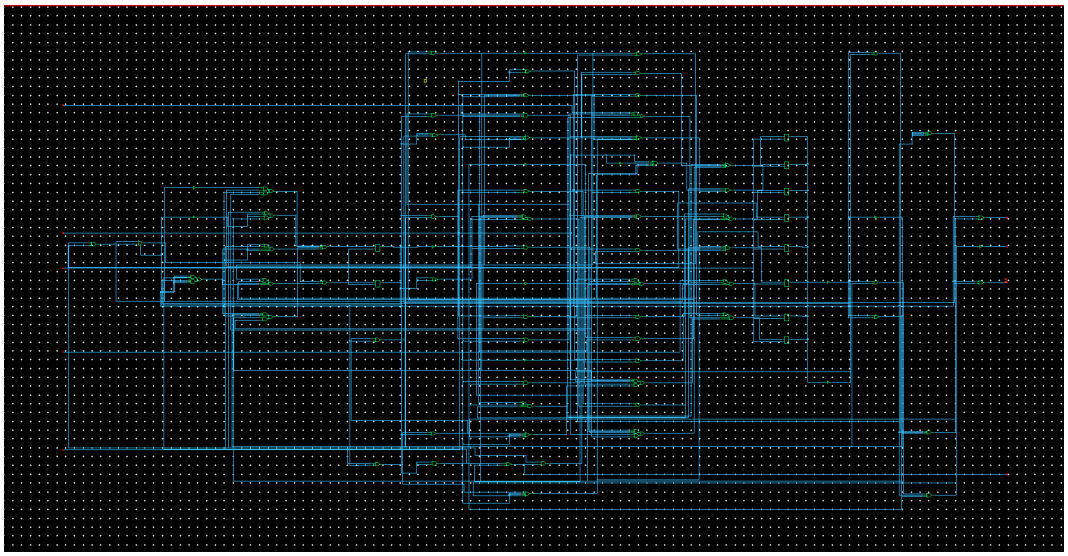

Figure 2: The gates level of the synthesized circuit.

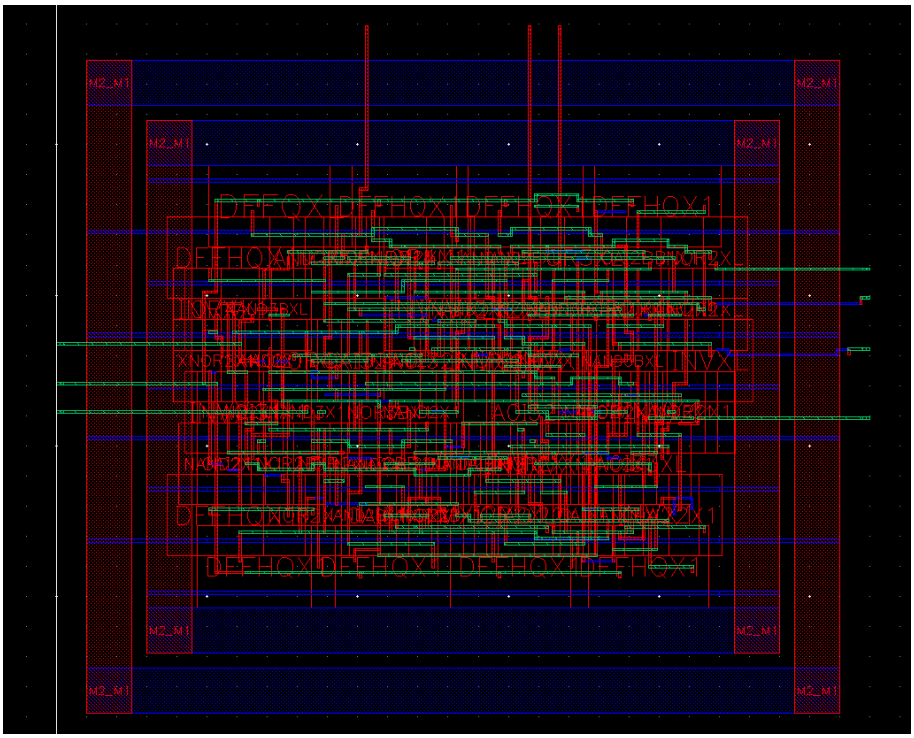

Figure 3: The sds of the synthesized circuit.

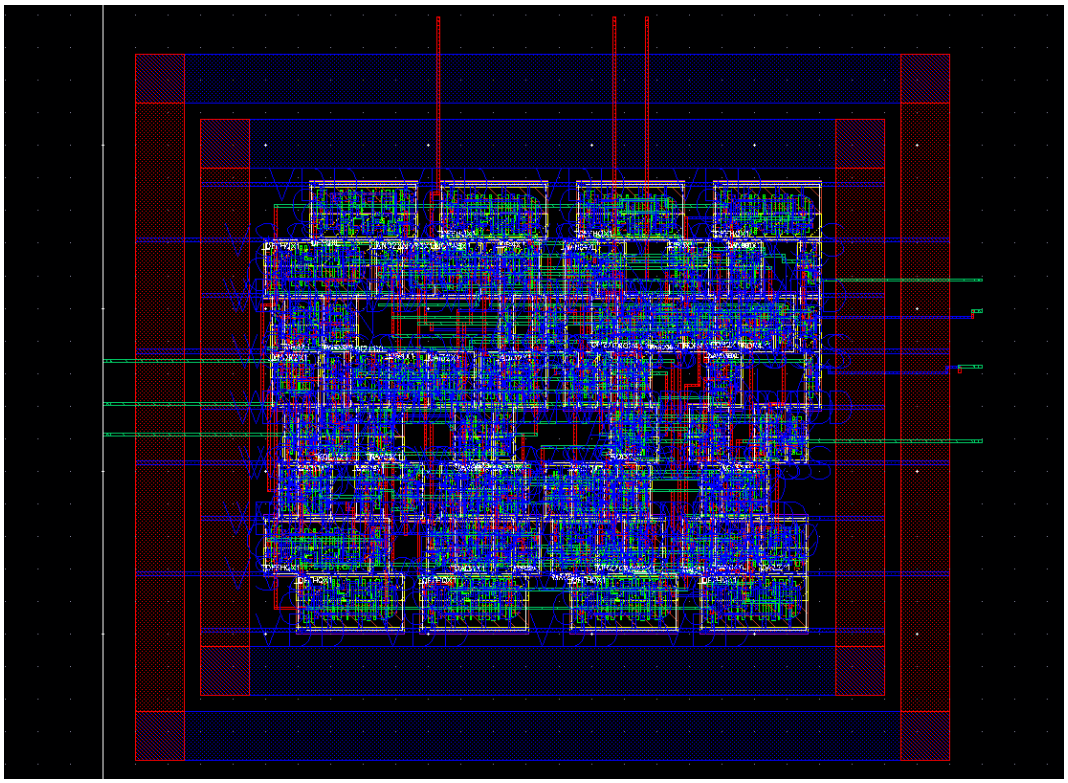

Figure 4: The transistor level 1 of the synthesized circuit.

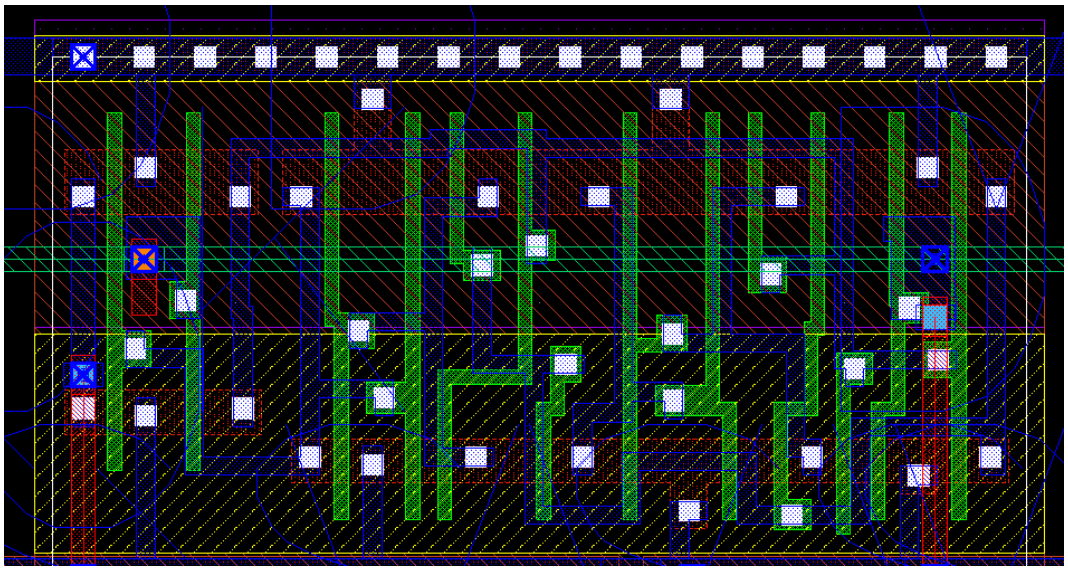

Figure 5: The transistor level 2 of the synthesized circuit.

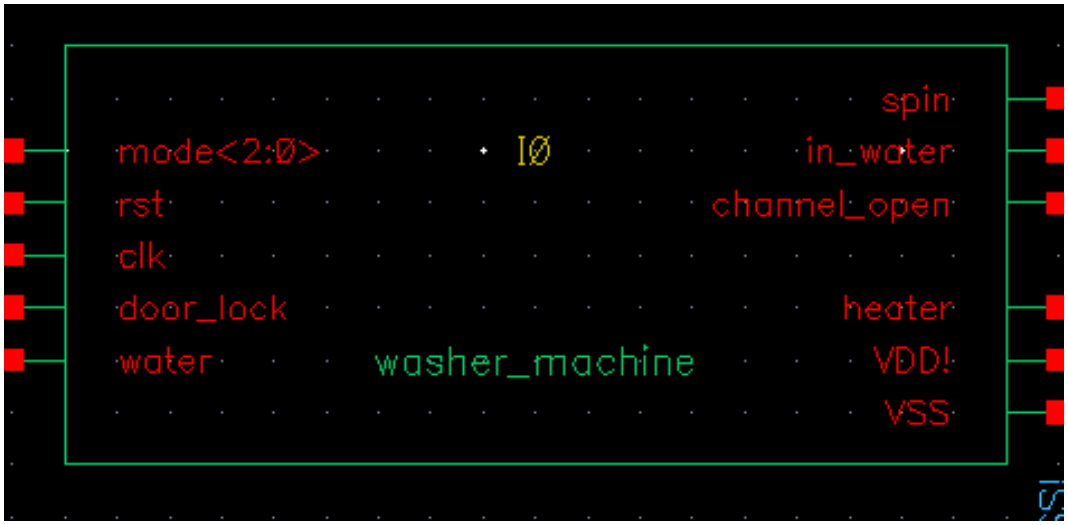

Figure 6: The testbench symbol of the synthesized circuit.

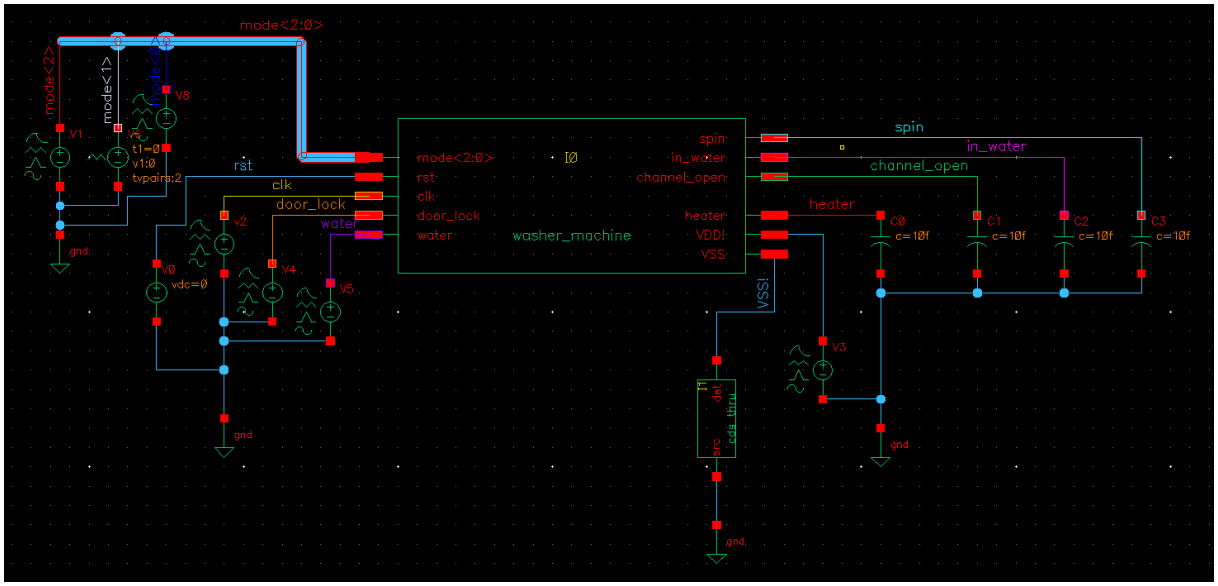

Figure 7: The testbench with the load capacitance of the synthesized circuit.

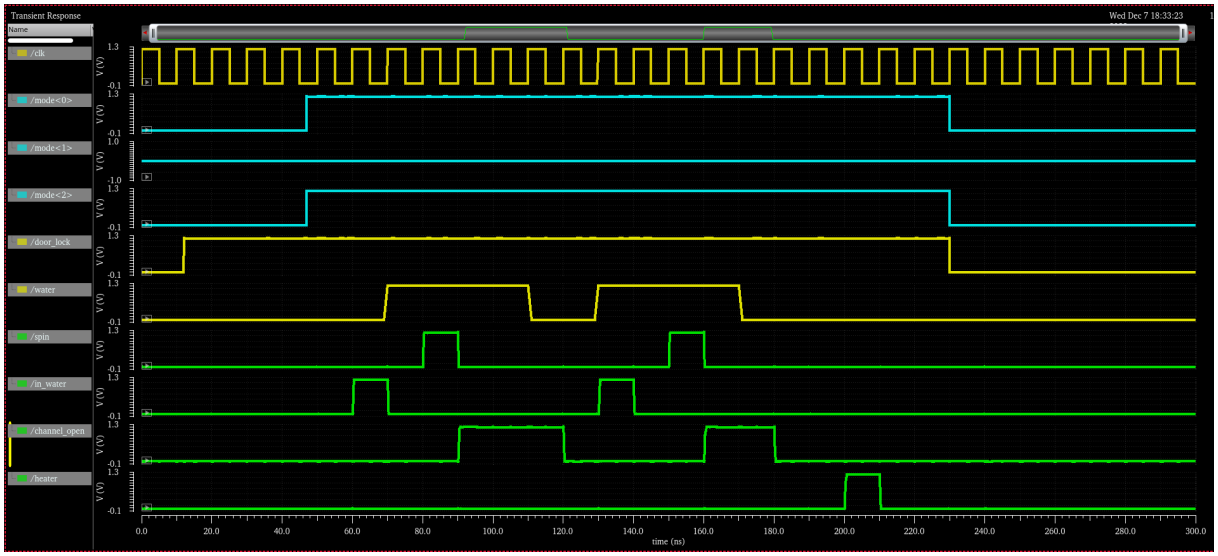

Figure 8: The simulation waveform of the testbench.

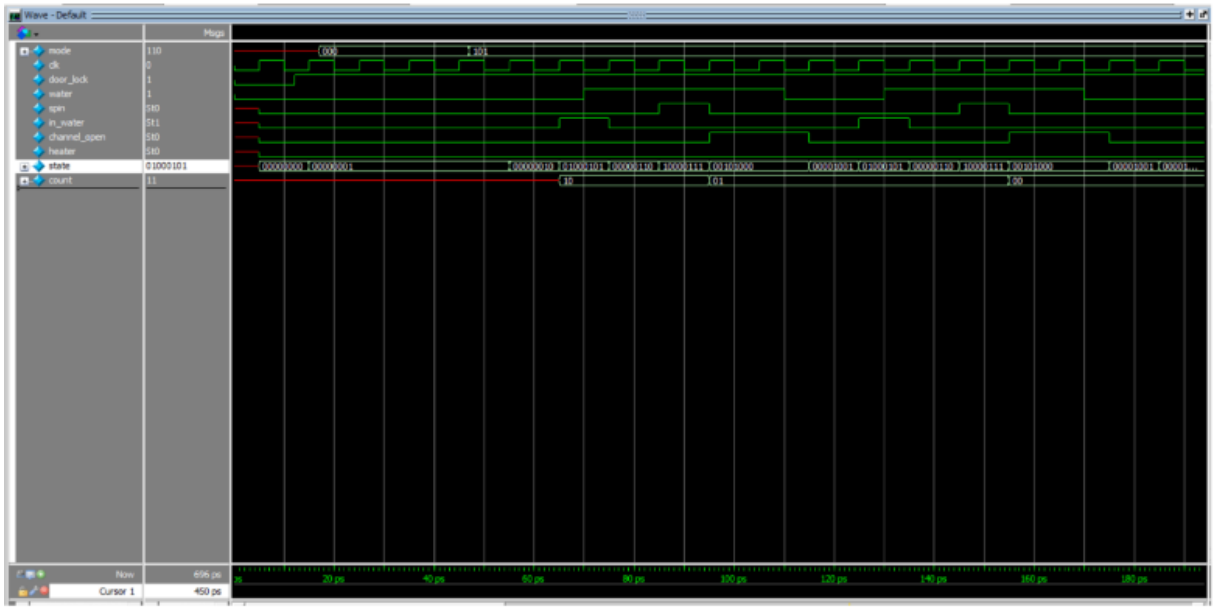

Figure 9: The original waveform from assignment 1.

As shown in Figure 8, the yellow lines represent the input signals. The green line represent the output signals. The blue lines are the bits of 'mode' signal which is 101. In this mode, the machine will spin twice and use the heating function. It can be seen that the 'water' indication is ON after the 'in water' command. Then the 'spin' signal is ON after the water in the drum reaches the desired level. Then the 'channal open' siganl is ON to drain the water and spin again. After washing, the 'heater' is ON to heat the clothes. The testbench simulation waveform exactly matches the wavefrom from assignment 1, which is expected. There is only 5 ps offset because the clock starts from 0 in assignment 1, and from 1 in the testbench. Therefore, it is safe to say the synthesized circuit works as expected.

2 Question 2

The circuit is below:

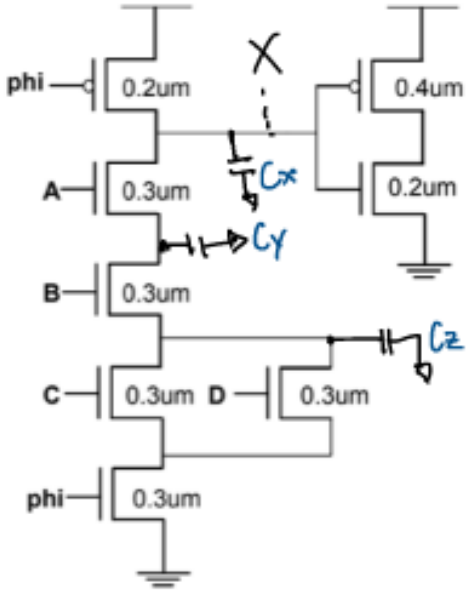

Figure 10: The circuit of question 2.

2.1 Part 1

For the Pull-Down circuit, the NMOS Gate A and B are connected in series. The Gate C and D are connected in parallel. Thus, the output logic is simply as below:

$$\boxed{OUT = F = AB \cdot (C + D)}$$

2.2 Part 2

In this question, I assumed the V_{dd} is 1.2V.
To find the worst case, I kept as many nodes as I can, and disconnected the ground. There are three node capacitors are marked in the ***Figure* 1**: C_x, C_y and C_z. The capacitances are calculated ($C_{eff} = \frac{1fF}{\mu m}$):

$$C_x = C_{eff} \times (0.2\mu m + 0.3\mu m) + C_g \times (0.4\mu m + 0.2\mu m) = 1.7fF$$

$$C_y = C_{eff} \times (0.3\mu m) = 0.3fF$$
$$C_z = C_{eff} \times (0.3\mu m + 0.3\mu m) = 0.6fF$$

At the pre-charge state, all gates A, B, C, D are at LOW (closed).The voltage at the input of the inverter is V_{dd}, 1.2V. The capacitor which shares the voltage is C_x only. Thus, the total charge is calculated:

$$Q = C_x \times V_{dd} = 1.7fF \times 1.2V = 2.04fC$$

During the evaluate state, gates A and B are HIGH and gates C and D stay LOW (0000 $\rightarrow$ 1100). Now three capacitors are sharing the charges: C_x, C_y and C_z. The new voltage is calculated:

$$V^* = \frac{Q}{C_x + C_y + C_z} = \frac{2.04fC}{1.7fF + 0.3fF + 0.6fF} = 0.785fF$$
$$Reduction\ of\ Voltage = V_{dd} - V^* = 1.2V - 0.785V = \boxed{0.4154V}$$

If no assumed V_{dd} value:

$$Q = 1.7 \cdot V_{dd}\ fC$$
$$V^* = \frac{1.7Vdd\ fC}{1.7fF + 0.3fF + 0.6fF} = 0.6538 \cdot V_{dd}$$
$$Reduction\ of\ Voltage = V_{dd} - 0.6538 \cdot V_{dd} = 0.342 \cdot V_{dd} \rightarrow \boxed{34.2\%}$$

3 Question 3

The nodes are marked in the figure below:

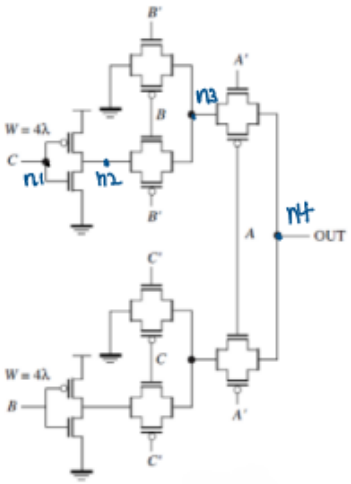

Figure 11: The circuit of question 3 with the marked nodes.

The capacitance of each node is calculated below:

***Node* 1 :**

$$C_{n1} = C_g \times (W_n + W_p) = C_g \times (4\lambda + 2\lambda) = \frac{2fF}{\mu m} \times 6 \times 0.1\mu m = \boxed{1.2\ fF}$$

Node 2 :

$$C_{n2} = C_{eff} \times (W_n + W_p) + 2 \times C_(eff) \times W + C_g \times W = C_{eff} \cdot (4\lambda + 2\lambda) + 2 \cdot 2\lambda + C_g \cdot 2\lambda = \boxed{1.4\ fF}$$

Node 3 : Two TGs are ON, one TG is OFF.

$$C_{n3} = C_{eff} \cdot 2W + 2 \cdot C_{eff} \cdot 2W + 2 \cdot C_g W = 3 \cdot \frac{1fF}{\mu m} \cdot 2 \cdot 2 \cdot 0.1\mu m + 2 \cdot \frac{2fF}{\mu m} \cdot 2 \cdot 0.1\mu m = \boxed{2.0\ fF}$$

Node 4 : One TG is ON, one TG is OFF.

$$C_{n4} = 2 \cdot C_{eff} \cdot 2W + C_g W = 2 \cdot \frac{1fF}{\mu m} \cdot 2 \cdot 2 \cdot 0.1\mu m + \frac{2fF}{\mu m} \cdot 2 \cdot 0.1\mu m = \boxed{1.2\ fF}$$

The capacitance at each nodes on the lower circuit is the same as the nodes on the upper circuit.
Now, the maximum and minimum delay can be calculated:

$$R_{inv} = R_{TG} = R_{eq} \cdot \frac{L}{W} = R_{eq} \cdot \frac{2\lambda}{2\lambda} = 12.5k\Omega.$$

The minimum-delay branch is the one from the ground to the output:

$$\tau_{min} = R_{TG} \cdot C_{n3} + 2 \cdot R_{TG} \cdot C_{n4} = 12.5k\Omega \cdot 2.0fF + 2 \cdot 12.5k\Omega \cdot 1.2fF = \boxed{55\ ps}$$

The maximum-delay branch is the one from the inverter's input to the output:

$$\tau_{max} = R_{inv} \cdot C_{n2} + (R_{inv} + R_{TG}) \cdot C_{n3} + (R_{inv} + 2 \cdot R_{TG}) \cdot C_{n4}$$

$$\tau_{max} = 12.5k\Omega \cdot 1.4fF + 25k\Omega \cdot 2.0fF + 37.5k\Omega \cdot 1.2fF = \boxed{112.5\ ps}$$

4 Question 4

The sizing parameters are measured in Cadence Virtuoso Layout using FreePDK15.

Parameters	***Size***
W_p(4 fins)	0.128 μm
W_n(10 fins)	0.368 μm
W_n(2 fins)	0.048 μm
L	0.02 μm

4.1 Static Power

The V_T is calculated from assignment 3, which is 0.3V. The V_{DD} is assumed to be 1V.
First, the current goes through the circuit, $I_{DP(sat)}$ is calculated:

$$I_{DP(sat)} = W \cdot v_{sat} \cdot C_{ox} \cdot \frac{(V_{SG} - V_T)^2}{V_{SG} - V_T + E_C \cdot L}$$

$$I_{DP(sat)} = \frac{0.128 \cdot 10^{-4}cm \cdot 8 \cdot 10^6 \frac{cm}{s} \cdot 1.6 \cdot 10^{-6} \frac{s}{\Omega cm^2} \cdot (1V - 0.3V)}{1 - 0.3V + 24\frac{V}{\mu m} \cdot 0.02\mu m} = 68.035\mu A$$

$$P_{static} = \frac{1}{2} \cdot V_{DD} \cdot I_{DP} = \frac{1}{2} \cdot 1V \cdot 68.035\mu A = \boxed{34.0176\mu W}$$

The simulation:

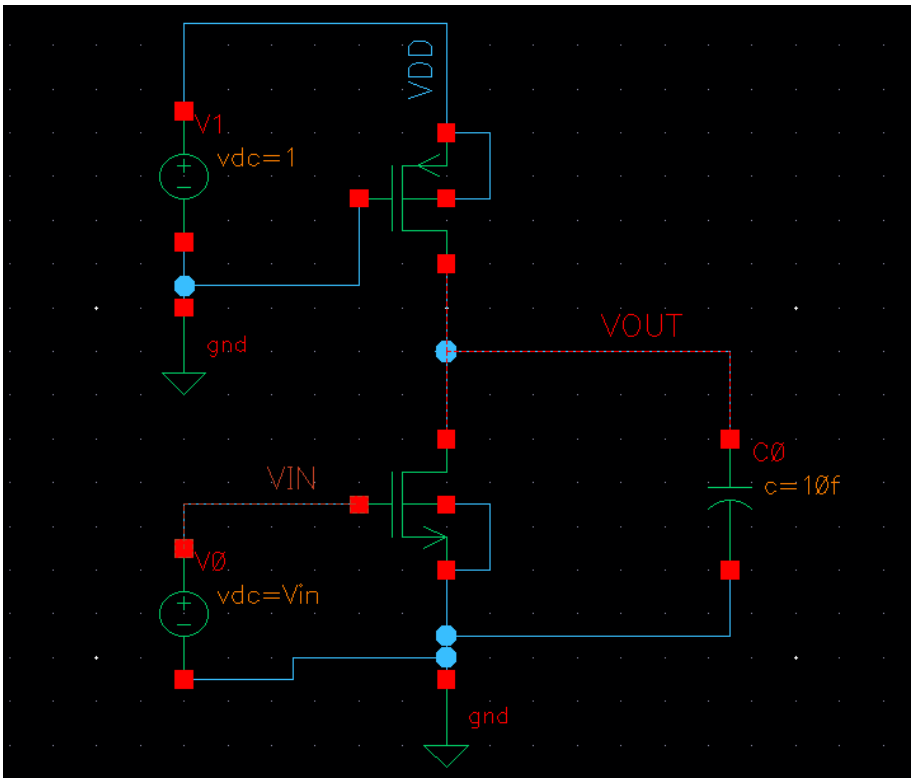

Figure 12: The pseudo circuit.

The Figure 13 shows that the total static power is 727.7 μW. However, we assume only half of the time is effective. Thus, the simulated static power is $\frac{727.7}{2} = 363.85$ μW, which is about 10 times to the calculated value.

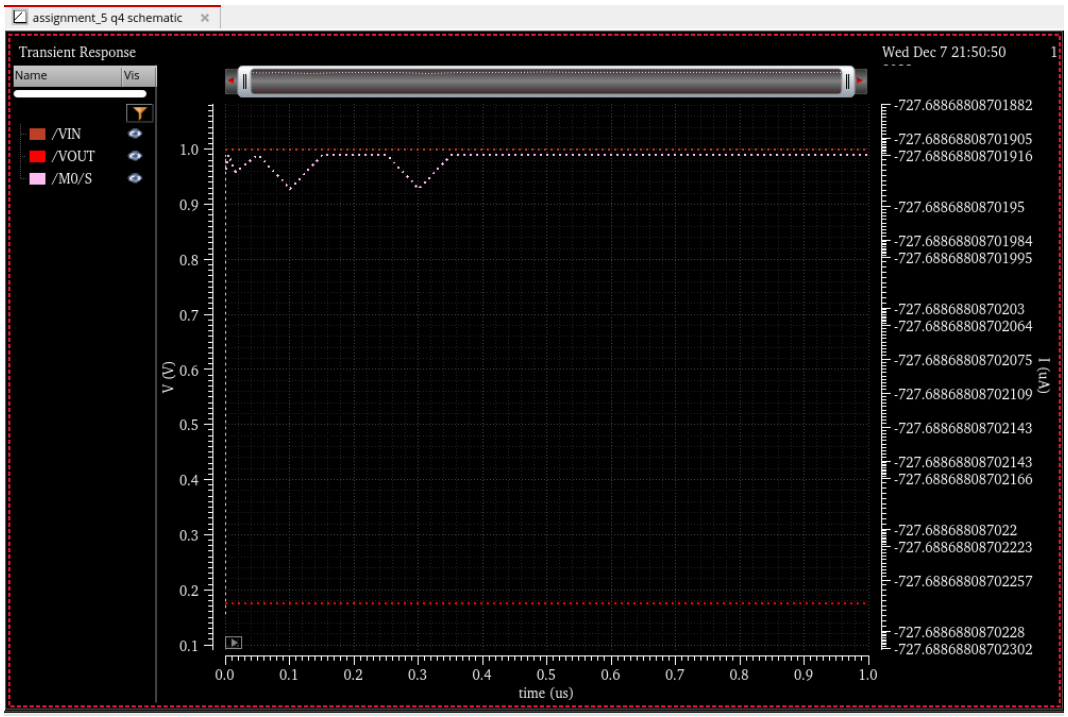

Figure 13: The simulated Vin and Vout.

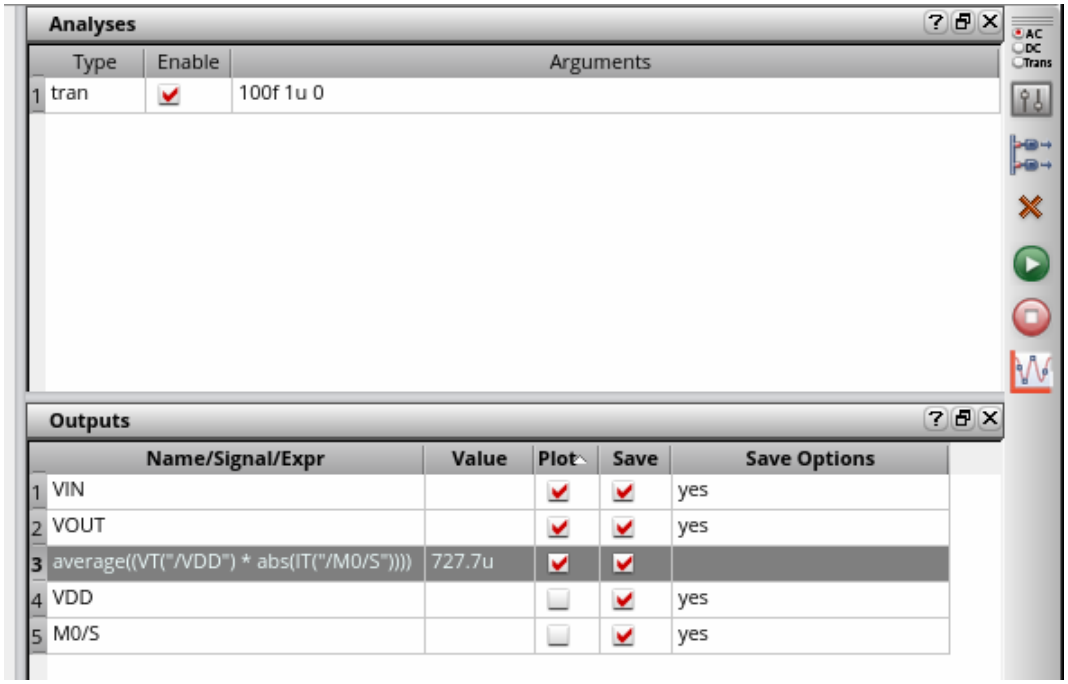

Figure 14: The simulated Vin and Vout.

4.2 Dynamic Power

4.2.1 Pseudo PMOS

The pseudo-pmos cannot pull V_{OL} all the way to 0V, thus the voltage across the capacitor is V_{DD}-V_{OL}. From Figure 13, the V_{OL} is about 174 μ V. Also, the total capacitance is calculated:

$$C_{total} = C_{self} + C_{load} = C_{eff} \cdot (W_p + W_n) + C_{load}$$

$$C_{total} = \frac{1fF}{\mu m}(0.128\mu m + 0.368\mu m) + 10fF = 10.496fF$$

Then, the dynamic power is calculated:

$$P_{dynamic} = C \cdot V^2 \cdot f = 10.496fF \cdot (1V - 0.174V)^2 \cdot 100 \cdot 10^6 Hz = \boxed{0.7161\mu W}$$

The simulation (the input is replaced by a Vpulse):

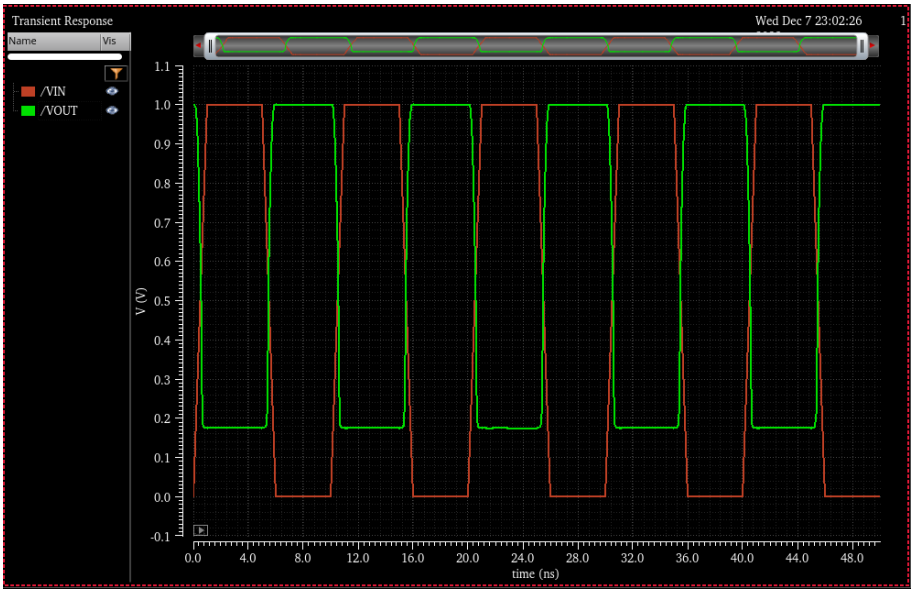

Figure 15: The simulated waveform.

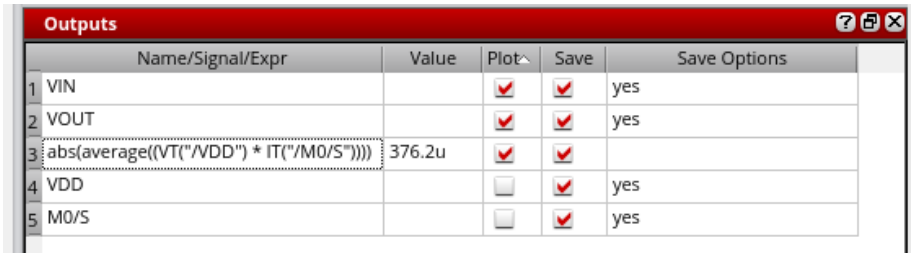

Figure 16: The simulated result.

As shown in Figure 16, the simulated P_{total} is 376.2 μ W. The simulated $P_{dynamic}$ can be calculated:

$$P_{dynamic} = P_{total} - Pstatic = 376.2\mu W - 363.85\mu W = 12.35\mu W$$

which is about 17 times larger than the calculated value.

The VTC of the Pseudo circuit is below:

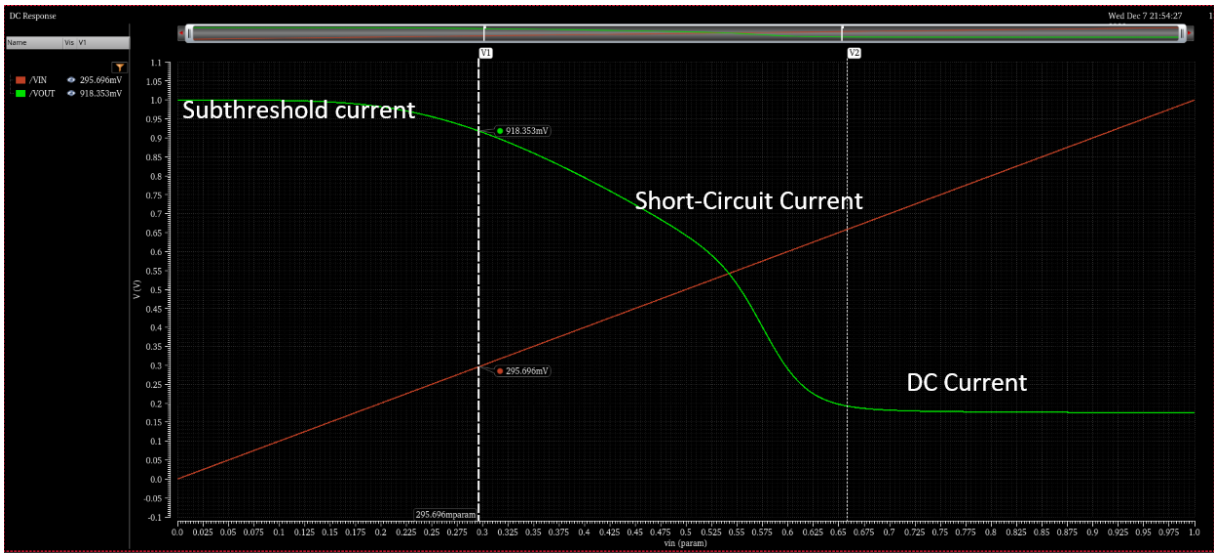

Figure 17: The simulated result.

4.2.2 CMOS

First, the capacitance is calculated:

$$C_{total} = C_{self} + C_{load} = C_{eff} \cdot (W_p + W_n) + C_{load}$$

$$C_{total} = \frac{1fF}{\mu m}(0.128\mu m + 0.048\mu m) + 10fF = 10.176fF$$

Then the dynamic power can be calculated by the same formula (The voltage can be completely drain to 0):

$$P_{dynamic} = C \cdot V^2 \cdot f = 10.176fF \cdot 1V^2 \cdot 100 \cdot 10^6 Hz = \boxed{1.0176\mu W}$$

The simulation:
As shown in Figure 20 below, the simulated dynamic power is 9.096 μW, which is about 10 times larger than the calculated value.

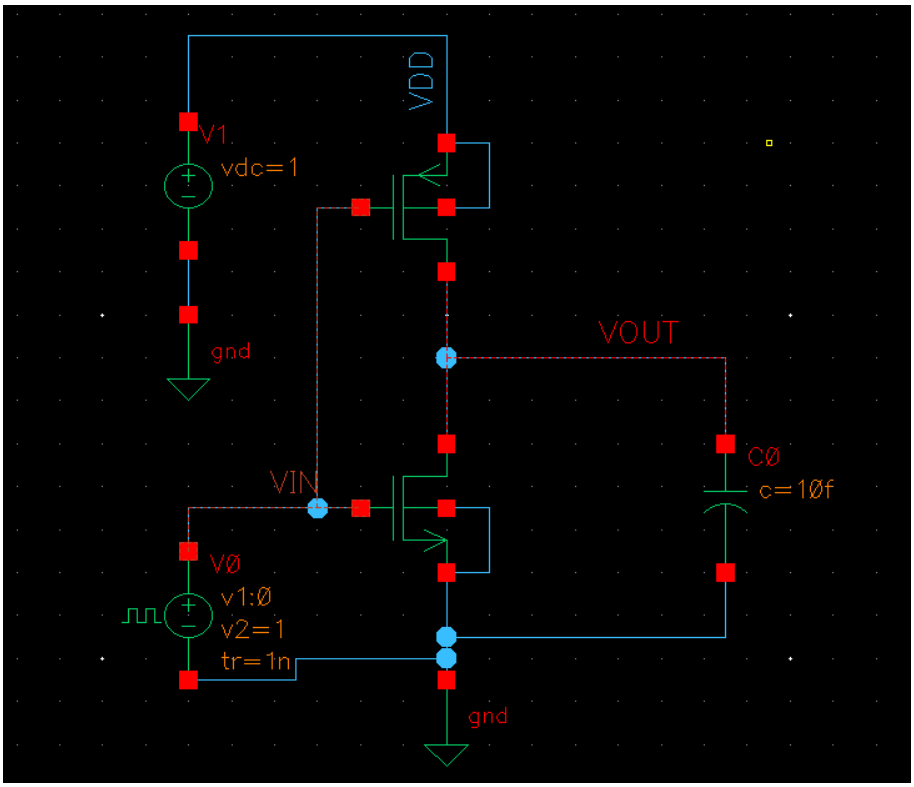

Figure 18: The simulated circuit.

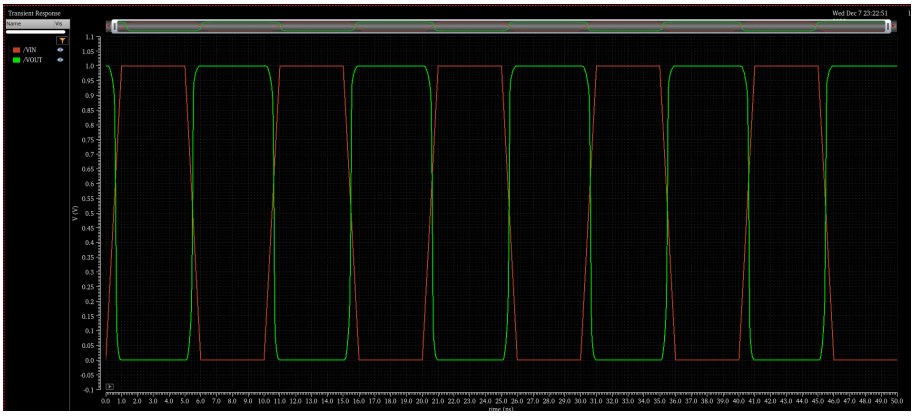

Figure 19: The simulated waveform.

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	VIN		☑	☑	yes
2	VOUT		☑	☑	yes
3	abs(average((VT("/VDD") * IT("/M0/S"))))	9.096u	☑	☑	
4	VDD		☐	☑	yes
5	M0/S		☐	☑	yes

Figure 20: The simulated result.

The VTC of the Pseudo circuit is below:

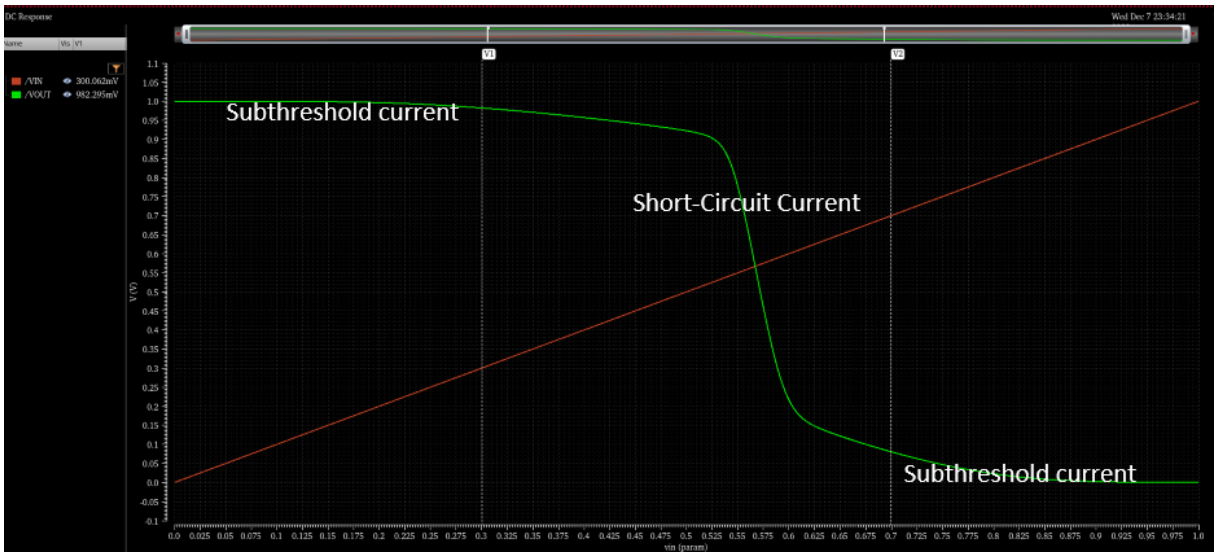

Figure 21: The VTC diagram.

5 Question 5

The defination of activity factor is the number of signal toggled divided by the number of clock toggled at a specific time slot. In this question, the number of signal toggled (transitions) is 4. The number of clock toggled (transitions) is 20. Therefore, the activity factor can be simply calculated:

$$\alpha = \frac{4}{20} = \boxed{0.2}$$

6 Question 6

The total capacitance is consist of area capacitance, lateral capacitance and the fringe capacitance. The metals are modelled below:

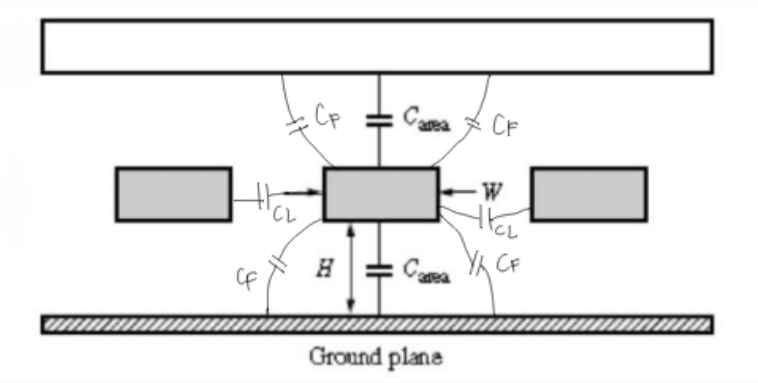

Figure 22: The model of the metals.

6.1 Part a

The resistance per unit length, r, and the capacitance per unit length c are calculated:

$$r = \frac{R}{L} = \frac{\frac{\rho L}{T \cdot W}}{L} = \frac{\rho}{TW} = \frac{0.017\ \Omega\mu m}{0.4\mu m \cdot 0.8\mu m} = \boxed{0.0531\ \frac{\Omega}{\mu m}}$$

$$C_{area} = \epsilon_{ox} \cdot \frac{W}{H} = 3 \cdot \epsilon_0 \cdot \frac{W}{H} = 3 \cdot 8.85 \cdot 10^{-12} \frac{F}{m} \cdot \frac{0.4\mu m}{0.5\mu m} = 2.124 \times 10^{-11} \frac{F}{m} = 0.02124\ \frac{fF}{\mu m}$$

$$C_{lateral} = \epsilon_{ox} \cdot \frac{T}{S} = 3 \cdot \epsilon_0 \cdot \frac{T}{S} = 3 \cdot 8.85 \cdot 10^{-12} \frac{F}{m} \cdot \frac{0.8\mu m}{2\mu m} = 1.062 \times 10^{-4} \frac{F}{m} = 0.01062 \frac{fF}{\mu m}$$

$$C_{fringe} = \epsilon_{ox} \cdot [\ln(1 + \frac{T}{H})] = 3 \cdot 8.85 \cdot 10^{-12} \frac{F}{m} \cdot \ln(1 + \frac{0.8\mu m}{0.5\mu m}) = 2.5369 \times 10^{-11} \frac{F}{m} = 0.02537\ \frac{fF}{\mu m}$$

The total capacitance per length (overestimated) is calculated:

$$c = 2 \cdot C_{area} + 2 \cdot C_{lateral} + 2 \cdot C_{fringe} = 2 \cdot 0.02124\ \frac{fF}{\mu m} + 2 \cdot 0.01062 \frac{fF}{\mu m} + 2 \cdot 0.02537\ \frac{fF}{\mu m} = \boxed{0.1145\ \frac{fF}{\mu m}}$$

6.2 Part b

The driver is a perfect voltage source and the hardware is π-modelled as below:

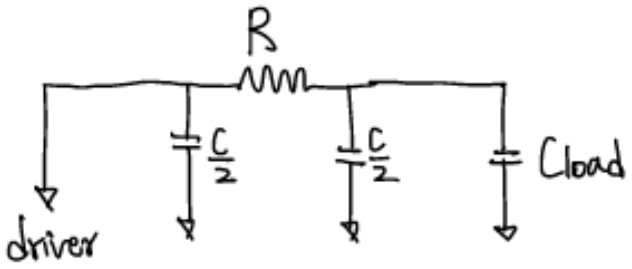

Figure 23: The model of the metals with the input source.

$$R = r \times L = 0.0531\frac{\Omega}{\mu m} \times 18mm \times \frac{1000\mu m}{1mm} = 955.8\ \Omega$$

$$C = c \times L = 0.1145\frac{fF}{\mu m} \times 18mm \times \frac{1000\mu m}{1mm} = 2061fF = 2.061\ pF$$

Since the drive is perfect voltage source. there is no input impedance. The delay can be calculated:

$$\tau = R \cdot C = R \cdot (\frac{C}{2} + C_{load}) = 955.8\Omega \cdot (\frac{2061fF}{2} + 50fF) = 1032741.9fs = \boxed{1.0327\ ns}$$

6.3 Part c

Assume the wire is being driven by a 25X inverter and using 40nm technology, $W = 2\lambda = 40nm$.
For the inverter:

$$W_n = 25 \times W = 25 \times 40\ nm = 1000\ nm = 1\ \mu m$$

$$W_p = 25 \times 2W = 25 \times 2 \times 40\ nm = 2000\ nm = 2\ \mu m$$

$$R_{inv} = R_{eq} \cdot \frac{L}{W} = 12.5k\Omega \cdot \frac{1}{25} = 0.5k\Omega = 500\Omega$$

$$C_{inv} = C_{eff} \cdot (W_n + W_p) = 1\frac{fF}{\mu m} \times (1\mu m + 2\mu m) = 3\ fF$$

The new model is below: The new delay can be calculated:

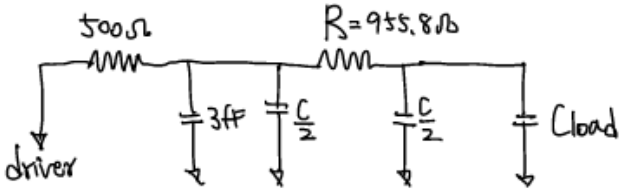

Figure 24: The new model of the metals.

$$\tau = 500\Omega \times (3fF + \frac{2061fF}{2}) + (500\Omega + 955.8\Omega) \cdot (\frac{2061fF}{2} + 50fF) = 2089741.9\ fs = \boxed{2.090\ ns}$$