

Assignment 4

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1 Question 1

The NAND3 is designed and make using Cadence. The specifications are shown below: The τ_{HL} is 26.5602ps. The τ_{LH} is 23.0161ps. The average delay is $\frac{26.5602+23.0161}{2} = 24.7882$ ps. The difference between τ_{HL} and $\tau_{LH} = 26.5602 - 23.0161 = 3.544$ ps < 5 ps

Area: 0.145533 μm^2

Delay: 24.7882 ps

Area \times Delay = $3.6074 \mu m^2 \cdot ps$

The figure below shows the schematics:

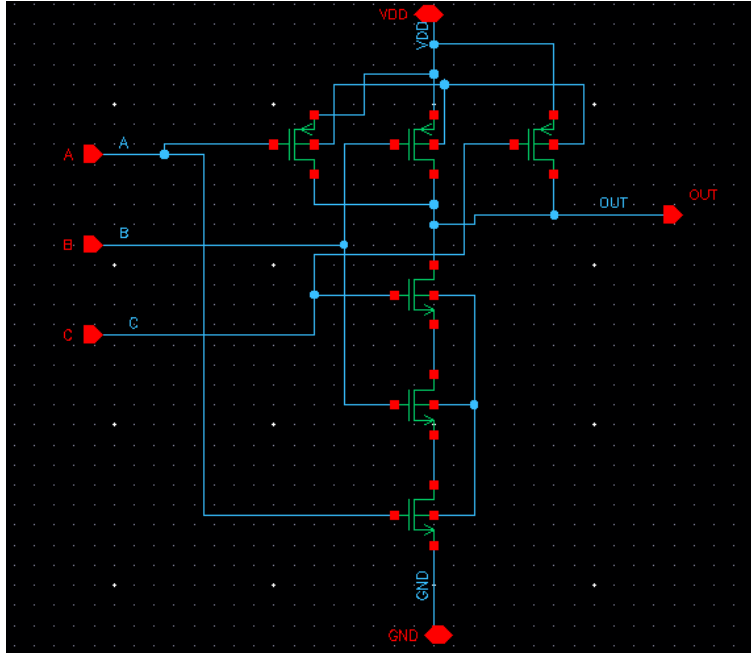


Figure 1: The schematics of the NAND3.

The figures below show the testbench with the **load capacitor**, the layout with demensions, the netlist including all parasitics, the DRC summary. The last figure shows the simulation waveform, which indicates the τ_{HL} and τ_{LH} and the 10ps clock skew rate.

In Figure 3, the area is calculated by multipling the length with width.

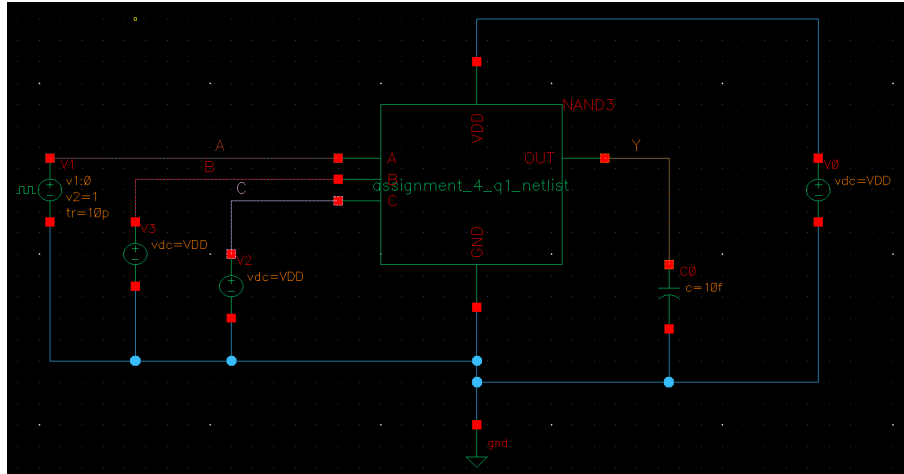


Figure 2: The testbench of the NAND3.

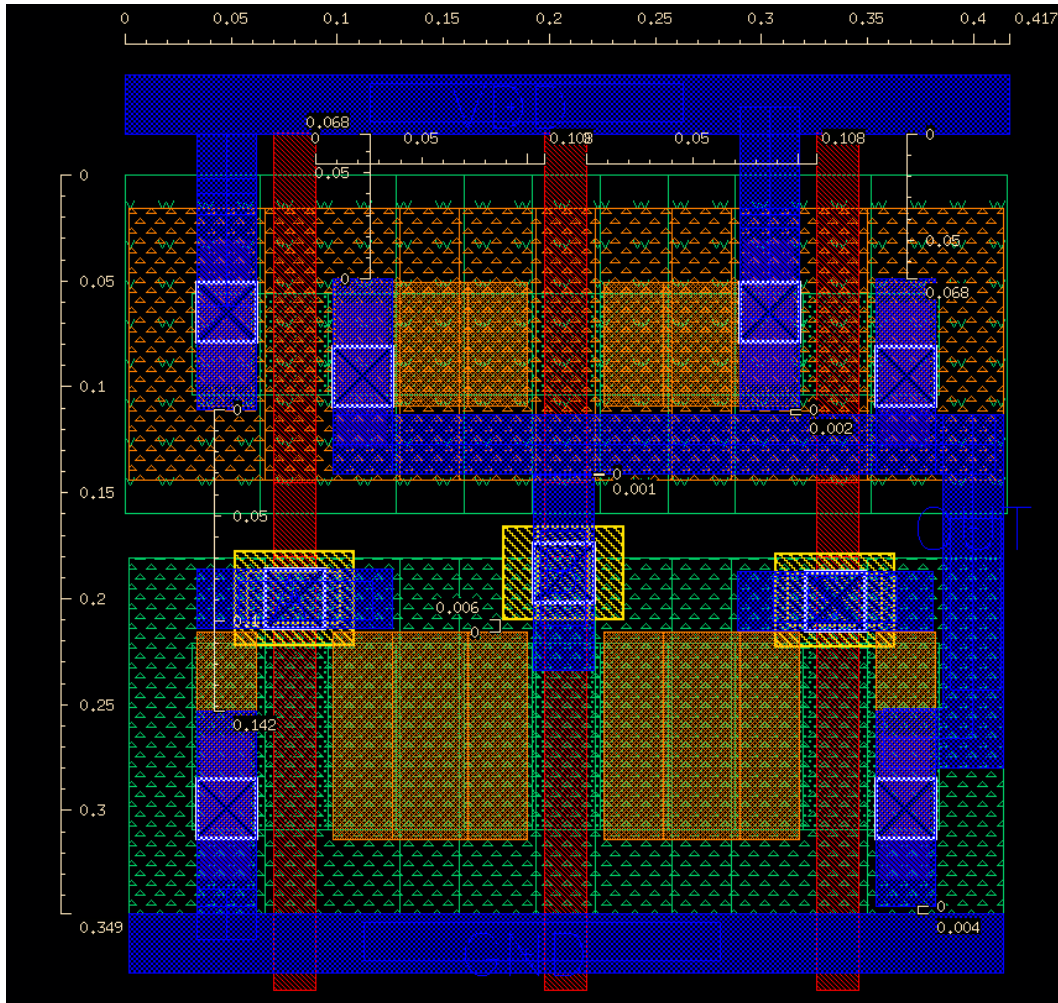


Figure 3: The layout of the NAND3.

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* File: assignment_4.q1.pex.netlist
* Created: Sun Nov 20 16:53:43 2022
* Program "Calibre xRC"
* Version "v2018.1.36.27"
*
*include "assignment_4.q1.pex.netlist.pex"
*subckt assignment_4_q1 A GND B C VDD OUT
*
* OUT OUT
* VDD VDD
* C C
* B B
* GND GND
* A A
M0_noxref noxref_14 A N_GND_M0_noxref_s noxref_20 NFET L=2e-08 W=8.8e-08 NFIN=3
+ ADEJ=5.28e-16 ASEJ=4.56e-16 PDEJ=1.32e-07 PSEJ=1.14e-07
M1_noxref noxref_15 B noxref_14 noxref_20 NFET L=2e-08 W=8.8e-08 NFIN=3
+ ADEJ=1.056e-15 ASEJ=1.056e-15 PDEJ=2.88e-07 PSEJ=2.88e-07
M2_noxref N_OUT_M2_noxref_d C noxref_15 noxref_20 NFET L=2e-08 W=8.8e-08 NFIN=3
+ ADEJ=9.12e-16 ASEJ=5.28e-16 PDEJ=2.52e-07 PSEJ=1.32e-07
M3_noxref noxref_14 noxref_17 noxref_14 noxref_20 NFET L=2e-08 W=8.8e-08 NFIN=3
+ ADEJ=1.056e-15 ASEJ=1.056e-15 PDEJ=2.88e-07 PSEJ=2.88e-07
M4_noxref noxref_15 noxref_18 noxref_15 noxref_20 NFET L=2e-08 W=8.8e-08 NFIN=3
+ ADEJ=1.056e-15 ASEJ=1.056e-15 PDEJ=2.88e-07 PSEJ=2.88e-07
MM0 N_OUT_MM0_d A N_VDD_MM0_s NET1 PFET L=2e-08 W=4.8e-08 NFIN=2 ADEJ=3.52e-16
+ ASEJ=3.04e-16 PDEJ=8.8e-08 PSEJ=7.6e-08
MM1 N_OUT_MM0_d B N_VDD_MM1_s NET1 PFET L=2e-08 W=4.8e-08 NFIN=2 ADEJ=7.04e-16
+ ASEJ=7.04e-16 PDEJ=1.92e-07 PSEJ=1.92e-07
MM2 N_OUT_MM2_d C N_VDD_MM1_s NET1 PFET L=2e-08 W=4.8e-08 NFIN=2 ADEJ=6.08e-16
+ ASEJ=3.52e-16 PDEJ=1.68e-07 PSEJ=8.8e-08
M8_noxref N_OUT_MM0_d noxref_17 N_OUT_MM0_d NET1 PFET L=2e-08 W=4.8e-08 NFIN=2
+ ADEJ=7.04e-16 ASEJ=7.04e-16 PDEJ=1.92e-07 PSEJ=1.92e-07
M9_noxref N_VDD_MM1_s noxref_18 N_VDD_MM1_s NET1 PFET L=2e-08 W=4.8e-08 NFIN=2
+ ADEJ=7.04e-16 ASEJ=7.04e-16 PDEJ=1.92e-07 PSEJ=1.92e-07
c_7 A GND 0.0118111f
c_15 B GND 0.0121583f
c_20 C GND 0.0104826f
c_44 noxref_14 GND 0.0738977f
c_49 noxref_15 GND 0.0734863f
*
*include "assignment_4.q1.pex.netlist,ASSIGNMENT_4_Q1.pxi"
*
*ends
*
*

```

Figure 4: The netlist of the NAND3.

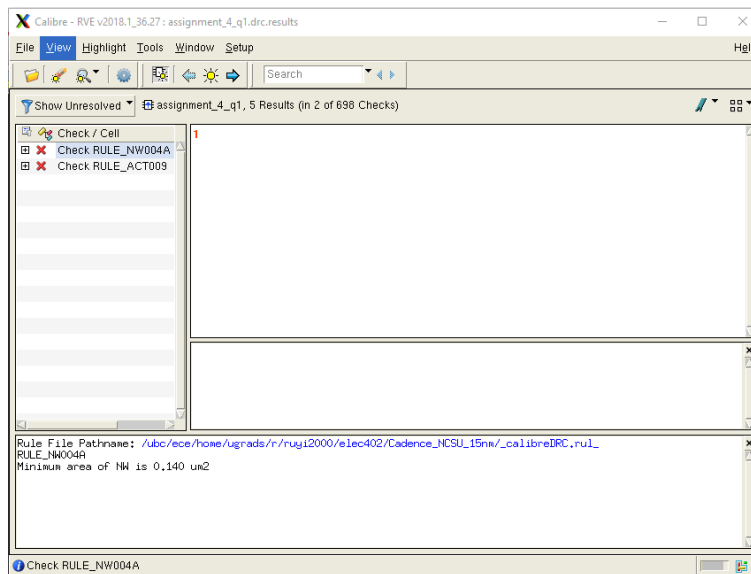


Figure 5: The part 1 of DRC report.

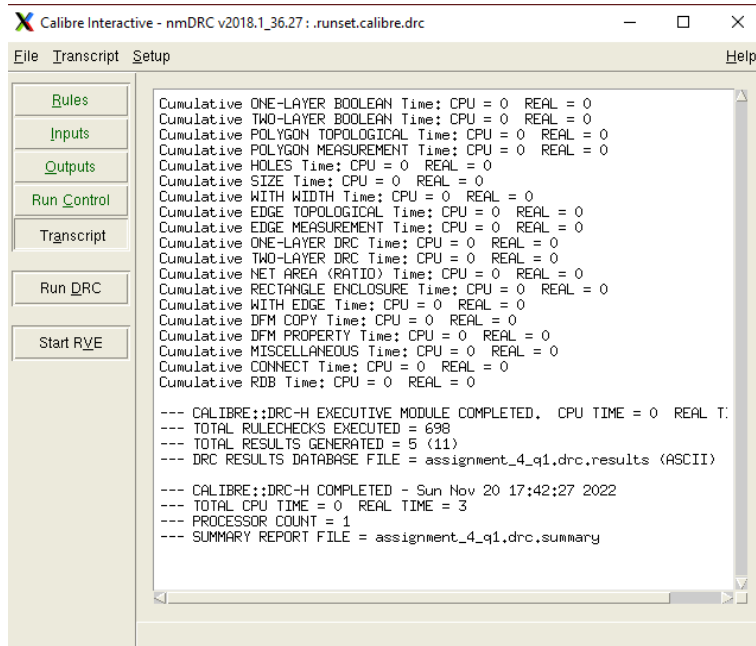


Figure 6: The part 2 of DRC report.

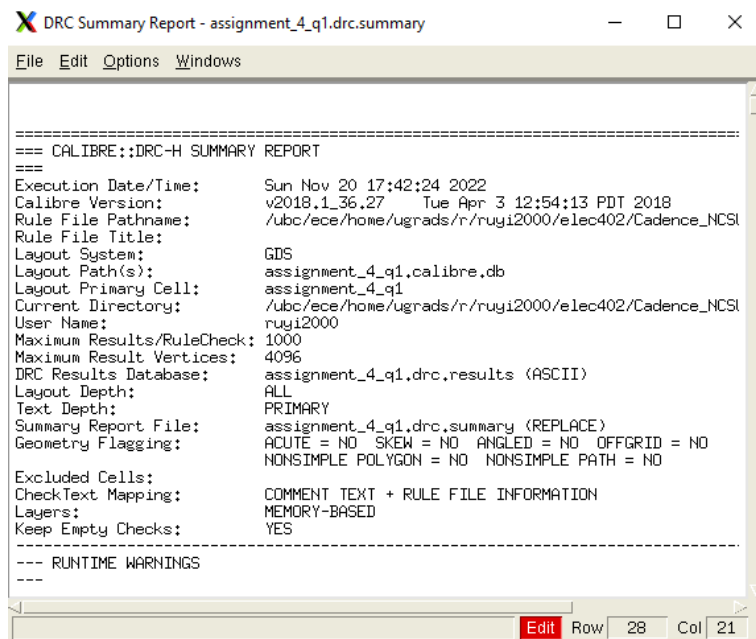


Figure 7: The part 3 of DRC report.



Figure 8: The waveform of the NAND3.

2 Question 2

The circuit is:

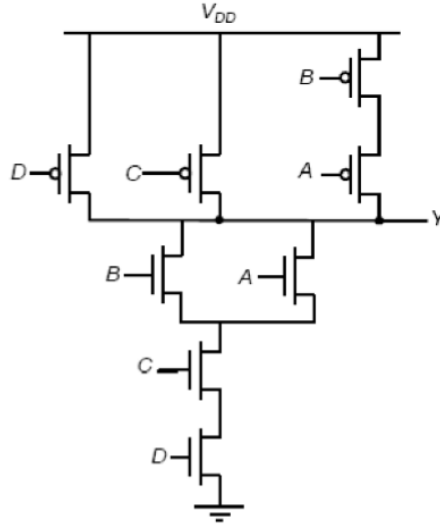


Figure 9: The circuit of question 2.

2.1 (a)

The pull-down logic function is $\overline{F} = \overline{Y} = (A + B) * CD$. The logic function of the circuit can be found by inverting the \overline{F} :

$$F = Y = \overline{\overline{F}} = \overline{(A + B) * CD} = \overline{(A + B)} + \overline{CD} = \boxed{\overline{A} * \overline{B} + \overline{C} + \overline{D}}$$

2.2 (b)

As shown in Figure 1, in the **Pull – Up** circuit, either D, C will be ON or both A and B will be ON. When D or C is ON, each branch has a single resistance of R . Thus, each D and C has a width of $2W$ or 8λ . The other branch is A and B, the worst-case because this branch has two P-MOS in series. The resistance of A and B is $\frac{1}{2}R$. The width of A and B are doubled due to the series connection. Thus, the A and B has a width of $4W$ or 16λ .

For the **Pull – Down** circuit, either A or B is ON and the C, D must be ON. The worst-case branch is either B-C-D or A-C-D. Since A and B are in parallel and each connects C,D in series, all A, B, C, D have the resistance of $\frac{1}{3}R$. Thus, the width of A, B, C, D are equal which is $3W$ or 12λ .

2.3 (c)

Pull – Up

For the τ_{LH} , in the worst case, I kept as many nodes to be LOW. Therefore B and C are always HIGH (NMOS on and PMOS off) and A is always LOW (NMOS off and PMOS on). D is HIGH to connect the ground in pull-down circuit. Since the output is pulled up, D is from HIGH to LOW to drain the current from the VDD and disconnect the ground. Therefore, the worse-case input pattern for τ_{LH} is $ABCD = 0111 \rightarrow ABCD = 0110$

Pull – Down

For the τ_{HL} , in the worst case, I kept as many nodes to be charged (HIGH). Therefore, B and C are always HIGH (NMOS on and PMOS off) and A is always LOW (NMOS off and PMOS on) (The same as pull-up). D is LOW (enable in Pull-up circuit) to connect the VDD in pull-up circuit. Since the output is pulled down, D is from LOW to HIGH to disconnect the VDD and drain the current to ground. Therefore, the worse-case input pattern for τ_{LH} is $ABCD = 0110 \rightarrow ABCD = 0111$

Simulations

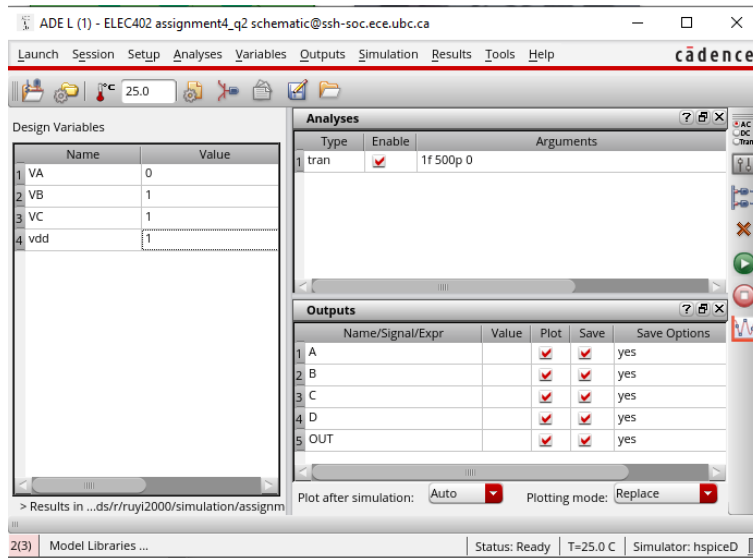


Figure 10: The parameters of the circuit.

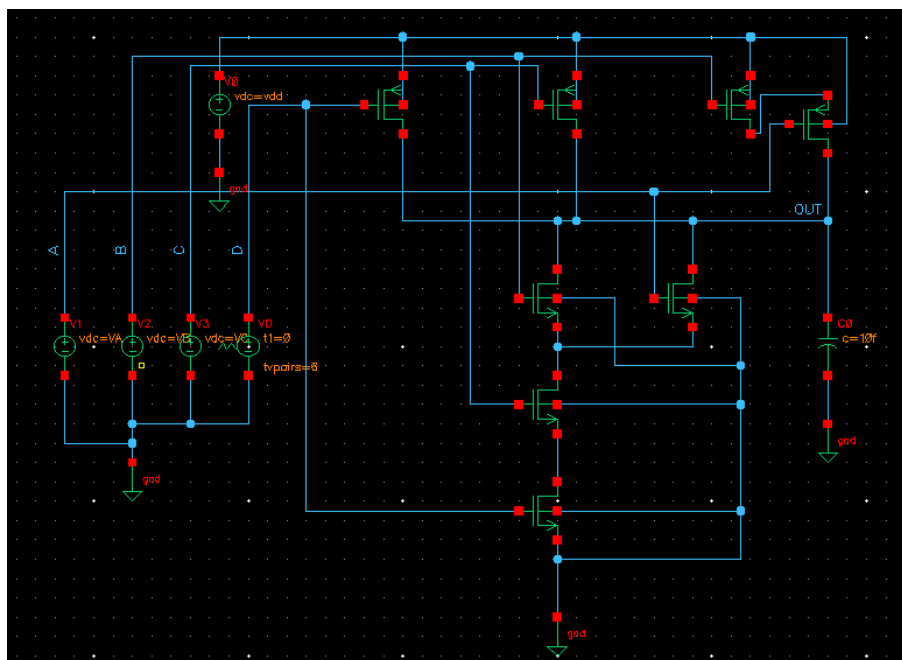


Figure 11: The schematics of the circuit.

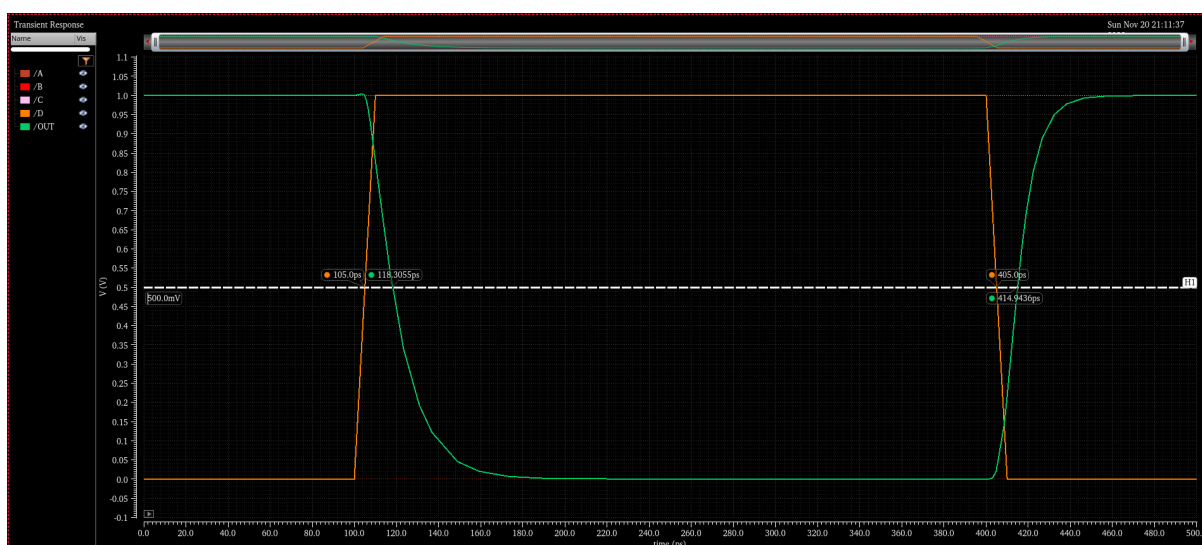


Figure 12: The waveform of the circuit.

Figure 12 shows the output waveform of switching D for pull-up and pull-down. The $\tau_{HL} = 118.3055 - 105 = 13.3055$ ps. The $\tau_{LH} = 414.9436 - 405 = 9.9436$ ps. The τ_{HL} and τ_{LH} are the highest value compared to other input patterns. Therefore, the speculated input patterns are the worst.

3 Question 3

3.1 (a)

Know that selB is \overline{sel} .

The top TG has a control signal sel to select \bar{A} . The bottom TG has a control signal \overline{sel} to select \bar{B} . When sel is 1, branch A is selected. When \overline{sel} is 1, branch B is selected. Thus,

$$C = (\bar{A} * sel) + (\bar{B} * \overline{sel})$$

$$OUT = \bar{C} = \overline{(\bar{A} * sel + \bar{B} * \overline{sel})} = \boxed{(A + \overline{sel}) * (B + sel)}$$

3.2 (b)

The equivalent Circuit:

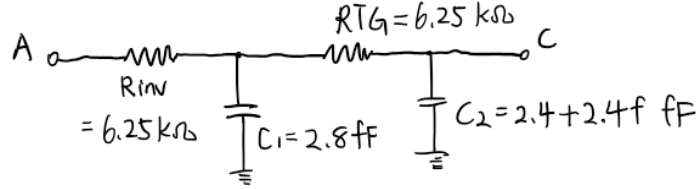


Figure 13: The equivalent circuit of the A-C path.

$$R_{inv} = R_{TG} = R_{eq} * \left(\frac{L}{W} \right) = 12.5k\Omega * \frac{2\lambda}{4\lambda} = \boxed{6.25k\Omega}$$

$$C_1 = C_{inv} + C_{TGin} = [C_{eff} * (4\lambda + 8\lambda)] + 2 * C_{eff} * 4\lambda + C_g * 4\lambda$$

$$C_1 = \frac{1fF}{um} * 12 * 0.1um + \frac{2fF}{um} * 4 * 0.1um + \frac{2fF}{um} * 4 * 0.1um = \boxed{2.8fF}$$

$$C_2 = C_{TGout} + C_{lg} + C_{TG}^{OFF} = [2 * C_{eff} * 4\lambda + C_g * 4\lambda] + f * C_g * (4\lambda + 8\lambda) + (2 * C_{eff} * 4\lambda)$$

$$C_2 = 2 * \frac{1fF}{um} * 4 * 0.1um + \frac{2fF}{um} * 4 * 0.1um + f * \frac{2fF}{um} * 12 * 0.1um + 2 * \frac{1fF}{um} * 4 * 0.1um = \boxed{(2.4 + 2.4f)fF}$$

3.3 (c)

Elmore delay is used to find the delay from A to C:

$$\tau = R_{inv} * C_1 + (R_{inv} + R_{TG}) * C_2$$

$$\tau = R_{inv} * (C_{inv} + C_{TGin}^{ON}) + (R_{inv} + R_{TG}) * (C_{TGout}^{ON} + C_{lg} + C_{TG}^{OFF})$$

$$\tau = 6.25k\Omega * 2.8fF + (6.25k\Omega + 6.25k\Omega) * (2.4 + 2.4f)fF = \boxed{(47.5 + 30f)ps}$$

3.4 (d)

The equivalent circuit from A to OUT is:

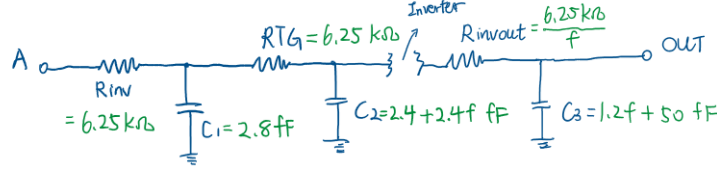


Figure 14: The equivalent circuit of the A-OUT path.

$$R_{invout} = \frac{R_{inv}}{f} = \frac{6.25k\Omega}{f}$$

$$C_3 = f * C_{eff} * (4\lambda + 8\lambda) + C_{load}$$

$$C_3 = f * \frac{1fF}{um} * 12 * 0.1um + 50fF = (1.2 * f + 50)fF$$

The τ_{out} can be calculated:

$$\tau_{out} = R_{invout} * C_3 = \frac{6.25k\Omega}{f} * (1.2 * f + 50)fF = \boxed{7.5 + \frac{312.5}{f}ps}$$

Therefore, τ_{total} can be calculated:

$$\tau_{total} = R_{inv} * C_1 + (R_{inv} + R_{TG}) * C_2 + \tau_{out}$$

$$\tau_{total} = R_{inv} * (C_{inv} + C_{TGin}^{ON}) + (R_{inv} + R_{TG}) * (C_{TGout}^{ON} + C_{lg} + C_{TG}^{OFF}) + R_{invout} * (C_{inv} + C_{load})$$

$$\tau_{total} = 6.25k\Omega * 2.8fF + (12.5k\Omega * (2.4 + 2.4 * f)fF) + 7.5 + \frac{312.5}{f}$$

$$\tau_{total} = (55 + 30f + \frac{312.5}{f})ps$$

3.5 (e)

To minimize the τ_{total} , the term $30f + \frac{312.5}{f}$ is minimized. The minimum f is calculated using derivative:

$$\text{Derivative of the term} = 30 + (\frac{-312.5}{f^2}) = 0$$

$$\boxed{f \Rightarrow 3.2275}$$

As shown in the calculation, the value of f which minimizes the delay is about 3.2275. If the f is an integer (manufactured by Finfet), it is 3.