assign3

2022年10月23日 星期日 10:48

ELEC402_prjassign3

Q1: Since EcL is NOT >> VGs, VDs, short-channel is used.

(1) Since Vout = VoL = 0.1V, Vin is ~1.2V

$V_{gs} = 1.2V - 0V = 1.2V > V_{th}(0.4V)$

$V_d = V_{out} = V_{OL} = 0.1V$, $V_{ds} = 0.1V - 0V = 0.1V$

$0.1V < 1.2V - 0.4V \Rightarrow V_{ds} < V_{gs} - V_{th}$

∴ Linear Region

$I_R = I_{DS}(lin)$

$$\Rightarrow \frac{1.2 - V_D}{10k} = \frac{W}{L}\cdot\frac{\mu_n C_{ox}}{(1+\frac{V_{DS}}{E_c L})}\cdot\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)\cdot V_{ds}$$

$$\frac{1.2-0.1}{10k} = \frac{W}{0.1um}\cdot\frac{270\ cm^2/V\cdot s \cdot 1.0\mu F/cm^2}{1+\frac{0.1V}{0.6V}}\cdot\left(1.2V - 0.4V - \frac{0.1V}{2}\right)\cdot 0.1V$$

$\Rightarrow$ **W = 0.6337 um**

(2) Since Vout = VoL = 0.1V, Vin is ~1.2V

for N2: $V_{gsN2} = 1.2 - 0.1 = 1.1V > V_{th}(0.4V)$

$V_{dsN2} = 1.2 - 0.1 = 1.1V > V_{gsN2} - V_{th} = 0.7V$

∴ N2 is in Saturation

for N1: $V_{gsN1} = 1.2 - 0V = 1.2V > V_{th}(0.4V)$

$V_{dsN1} = 0.1 - 0V = 0.1V < V_{gsN} - V_{th} = 0.8V$

∴ N1 is in Linear.

$I_{DSN2}(sat) = I_{DSN1}(lin)$

$$\Rightarrow W_{N2}\cdot v_{sat}\cdot C_{ox}\cdot\frac{(V_{gsN2}-V_t)^2}{(V_{gsN2}-V_t)+E_cL} = \frac{W_{N1}}{L}\cdot\frac{\mu_n C_{ox}}{1+\frac{V_{dsN1}}{E_cL}}\cdot\left(V_{gsN1} - V_t - \frac{V_{dsN1}}{2}\right)\cdot V_{dsN1}$$

$$0.1um\cdot 8\times10^6 cm/s\cdot\frac{(1.1V-0.4V)^2}{1.1V-0.4V+0.6V} = \frac{W_{N1}}{0.1um}\cdot\frac{270\ cm^2/V\cdot s}{1+\frac{0.1V}{0.6V}}\cdot\left(1.2V-0.4V-\frac{0.1V}{2}\right)\cdot 0.1V$$

0.37692308

$\Rightarrow$ **W_{N1} = 0.17373 um**

(3) Since Vout = VoL = 0.1V, Vin is ~1.2V

for N2: $V_{gsN2} = 1.6 - 0.1 = 1.5V > V_{th}(0.4V)$

$$V_{dsN2} = 1.2 - 0.1 = 1.1V > \frac{(V_{gsN2}-V_{th})E_cL}{(V_{gsN2}-V_{th})+E_cL} = 0.388$$

∴ N2 is saturation.

for N1: $V_{gsN1} = 1.2 - 0 = 1.2V > V_{th}(0.4V)$

$V_{dsN1} = 0.1 - 0 = 0.1V < V_{gsN1} - V_{th} = 0.8V$

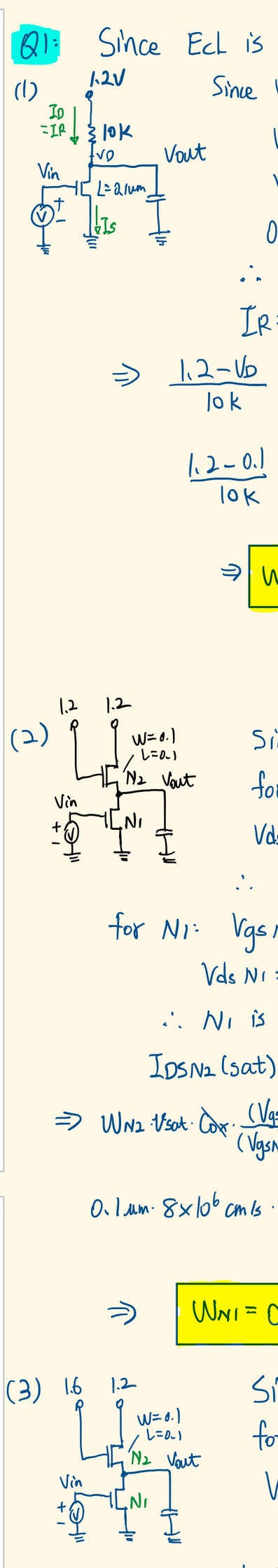
∴ N1 is Linear

$I_{DSN2}(sat) = I_{DSN1}(lin)$

$$W_{N2}\cdot v_{sat}\cdot C_{ox}\cdot\frac{(V_{gsN2}-V_t)^2}{(V_{gsN2}-V_t)+E_cL} = \frac{W_{N1}}{L}\cdot\frac{\mu_n C_{ox}}{1+\frac{V_{dsN1}}{E_cL}}\cdot\left(V_{gsN1}-V_t-\frac{V_{dsN1}}{2}\right)\cdot V_{dsN1}$$

$$0.1um\cdot 8\times10^6 cm/s\cdot\frac{(1.5-0.4)^2}{1.5-0.4+0.6} = \frac{W_{N1}}{0.1um}\cdot\frac{270\ cm^2/Vs}{1+\frac{0.1V}{0.6V}}\cdot\left(1.2-0.4-\frac{0.1}{2}\right)\cdot 0.1V$$

$\Rightarrow$ **W_{N1} = 0.3281 um**



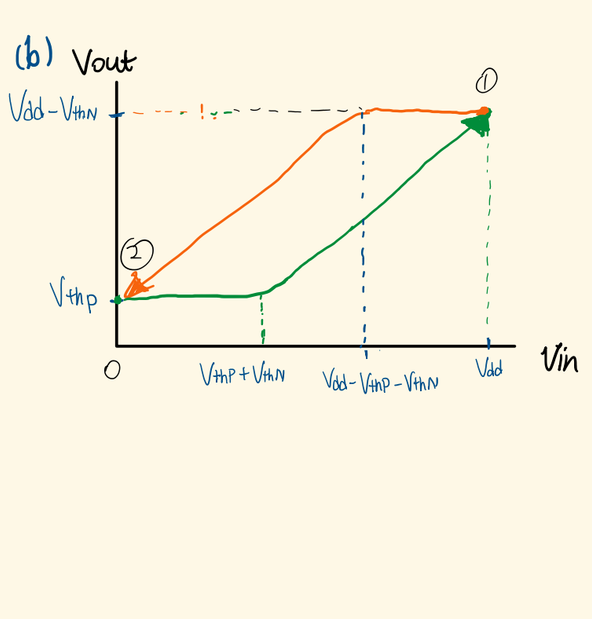
Q2 (a) The intended function of this circuit is a digital buffer in which the output voltage followes the input voltage.

Output swing: In this circuit, NMOS is the pull-up device, the max Vout is Vdd-VthN. A PMOS is a pull-down device, the minimum Vout is VthP. When a LOW voltage is applied, the NMOS is OFF and PMOS is ON. The output is LOW. When a HIGH voltage is applied, the NMOS is ON and PMOS is OFF. The output is pulled to HIGH.

Input	Output
LOW	LOW VthP
HIGH	HIGH (Vdd-Vth)

} the reason is explained in part (c)

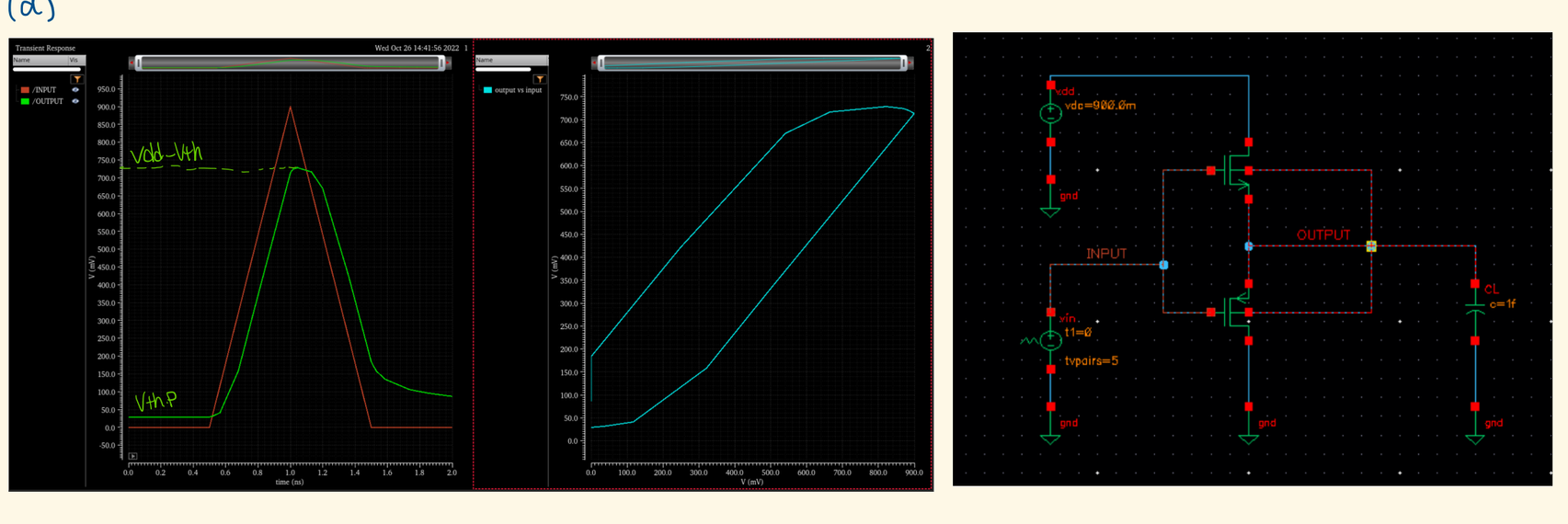
(b)



The input voltage is firstly from HIGH to LOW. (orange) The output voltage starts to drop when Vin drops to Vdd-VthP-VthN because the point and below, the PMOS is stronger and pulls Vout to VthP. Then Vin is from 0V. (green line). Vout isn't charging because PMOS is still ON and NMOS is still OFF. After Vin = VthP + VthN, the NMOS is ON and pulls the Vout up. While the Vin is increasing to Vdd, the PMOS is turned OFF and the maximum Vout is Vdd-VthN.

c) The gain for this circuit is theoretically close to 1. However, this is NOT a valid gate because for the NMOS, VGS = Vin(vdd) - Vs(vout). When Vout = Vdd-VthN, VGS = Vdd-(Vdd - VthN) = VthN. If Vout exceeds Vdd-VthN, VGS = Vdd - (Vdd - VthN + ε) = VthN - ε. So VGS < VthN. At VGS < VthN, the NMOS doesn't work. Thus the maximum logic high output is Vdd-VthN. For the PMOS, VGS = Vin(VIL) - Vs(Vout). When Vout = 0, VGS = 0-0 = 0V. 0V < |Vthp|. At VGS < |Vthp|, the PMOS doesn't work. Therefore, the minimum logic Low output is Vthp. As a result, the gain cannot be 1; it will be close to 1. In addition, the gain is higher than 1 for Low gain regions because when Vin is 0, the output is 1. According to the VTC in part (d), at the high gain regaion, the gain is lower than 1. Therefore, it is NOT a valid gate and doesn't have noise-rejection properties.

(d)



As shown above, the maximum Vout is Vdd-Vth, the minmum Vout is Vth.P, which verified the statement in part (a) (b) (c).

Q4:

(a) The oxide capacitance $= C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\times8.85\times10^{-12}F/m}{40\times10^{-10}m} = 0.00862875\ F/m^2$

$\Rightarrow 0.00862875\ \frac{F}{m^2}\times\frac{1m}{10^6um}\times\frac{1m}{10^6um}\times\frac{10^{15}fF}{1F} = 8.62875\ fF/um^2$

$C_g = C_{ox}\cdot A/W = C_{ox}\cdot W\cdot L/W = 8.62875\ fF/um^2\times180\ nm\times\frac{1um}{10^3nm} =$ **1.553175 fF/um**

Overlap C = $C_{ol} = C_{ox}\cdot A_{ol}/W_{ol} = C_{ox}\cdot L_{ol} = 8.62875\ fF/um^2\times22\times10^{-9}m = 0.1898\ fF/um$

total Gate C = $C_G = C_g\cdot W = 1.553\ fF/um\times900\ nm = 1.398\ fF$

total overlap C = $C_{orlap} = C_{ol}\cdot W = 0.1898\ fF/um\times900\ nm = 0.171\ fF$

In Linear:

$C_{GS} = \frac{1}{2}C_G + C_{orlap} = \frac{1}{2}\times1.398\ fF + 0.171\ fF =$ **0.87 fF**

$C_{GD} = \frac{1}{2}C_G + C_{orlap} = \frac{1}{2}\times1.398\ fF + 0.171\ fF =$ **0.87 fF**

$C_{GB} =$ **0 fF**

In Saturation:

$C_{GS} = \frac{2}{3}C_G + C_{orlap} = \frac{2}{3}\times1.398\ fF + 0.171\ fF =$ **1.103 fF**

$C_{GD} = C_{orlap} =$ **0.171 fF**

$C_{GB} =$ **0 fF**

In Cut-off

$C_{GS} = C_{orlap} =$ **0.171 fF** $C_{GD} = C_{orlap} =$ **0.171 fF**

$C_{GB} = C_G =$ **1.398 fF**

(b) $\phi_B = \frac{kT}{q}\cdot\ln\left|\frac{N_A\cdot N_D}{n_i^2}\right| = 2.565\times10^{-2}\times\ln\left|\frac{3\times10^{16}/cm^3\times3\times10^{19}/cm^3}{(1.45\times10^{10})^2/cm^6}\right| = 0.923\ V$

$$C_{jo} = \sqrt{\frac{\varepsilon_{si}\cdot q}{2\phi_B}\cdot\frac{N_A N_B}{N_A+N_B}} = \sqrt{\frac{11.7\times8.85\times10^{-14}\frac{F}{cm}\times1.6\times10^{-19}\times3\times10^{16}\times3\times10^{19}}{2\times0.923\times(3\times10^{16}+3\times10^{19})}} = 5.1856\times10^{-8}F/cm^2$$

$\Rightarrow 5.1856\times10^{-8}\frac{F}{cm^2}\times\frac{100cm}{1m}\times\frac{1m}{10^6um}\times\frac{100cm}{1m}\times\frac{1m}{10^6um}\times\frac{10^{15}fF}{1F} = 0.51856\ fF/um^2$

assume NO STI on side, so the side is $2x_j$.

$C_j = C_{jo}\cdot(Y+2x_j) = 0.51856\ fF/um^2\times(800+600)\ nm\times\frac{1um}{1000nm} =$ **0.7260 fF/um**

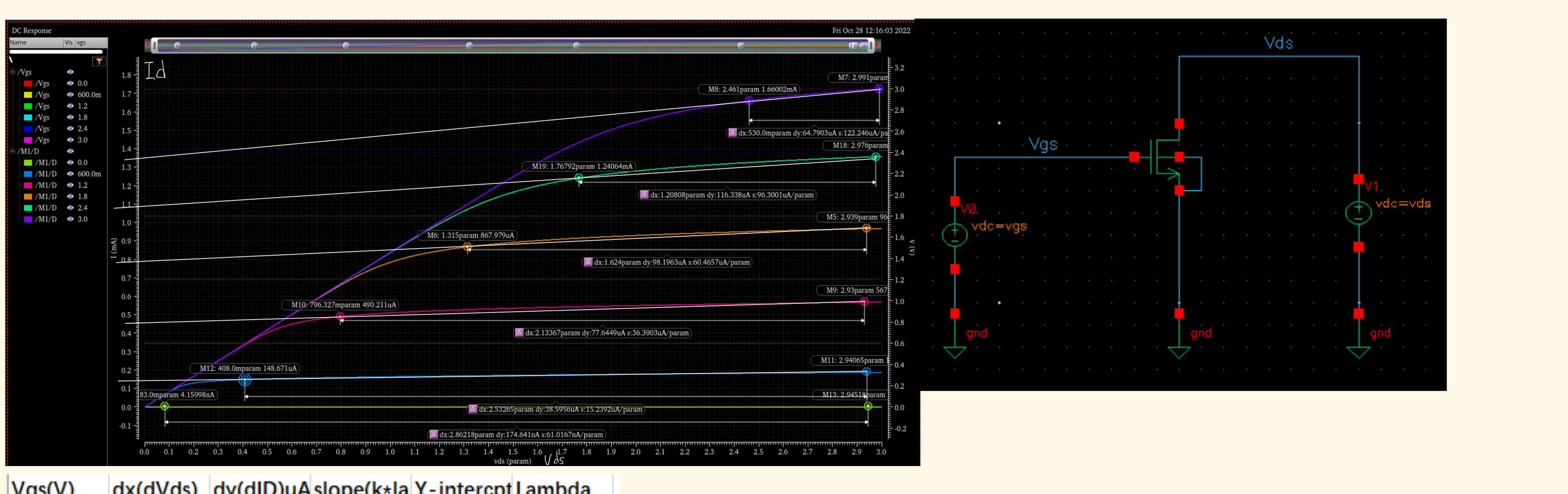
(c) i. $V_D = 1.8V$, $V_B = 0V$, $V_j = 0V - 1.8V = -1.8V$

$$C_{junc} = \frac{C_j\cdot W}{(1-\frac{V_j}{\phi_B})^m} = \frac{0.7260\ fF/um\times0.9\ um}{(1-\frac{-1.8V}{0.923V})^{0.5}} = \mathbf{0.3804\ fF}$$

ii. $V_D = 0V$, $V_B = 0V$, $V_j = 0 - 0 = 0V$

$$C_{junc} = \frac{C_j\cdot W}{(1-\frac{V_j}{\phi_B})^m} = \frac{0.7260\ fF/um\times0.9\ um}{(1-\frac{0}{\phi_B})^{0.5}} = \mathbf{0.6534\ fF}$$

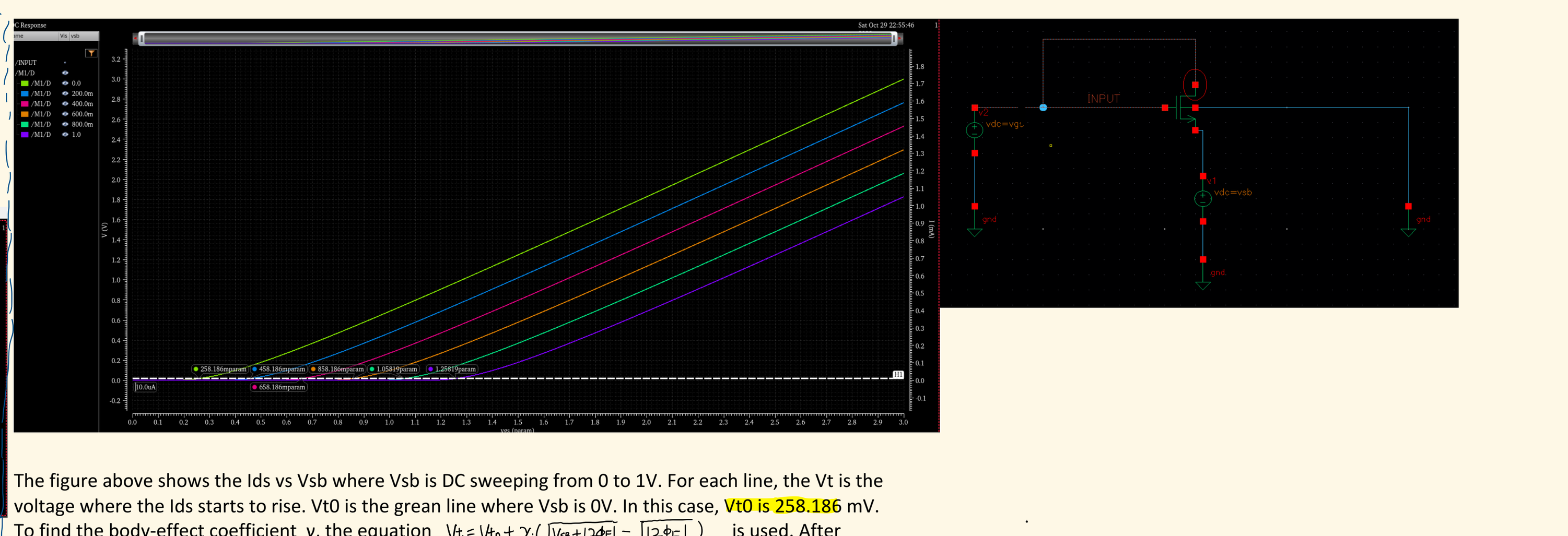
Q3

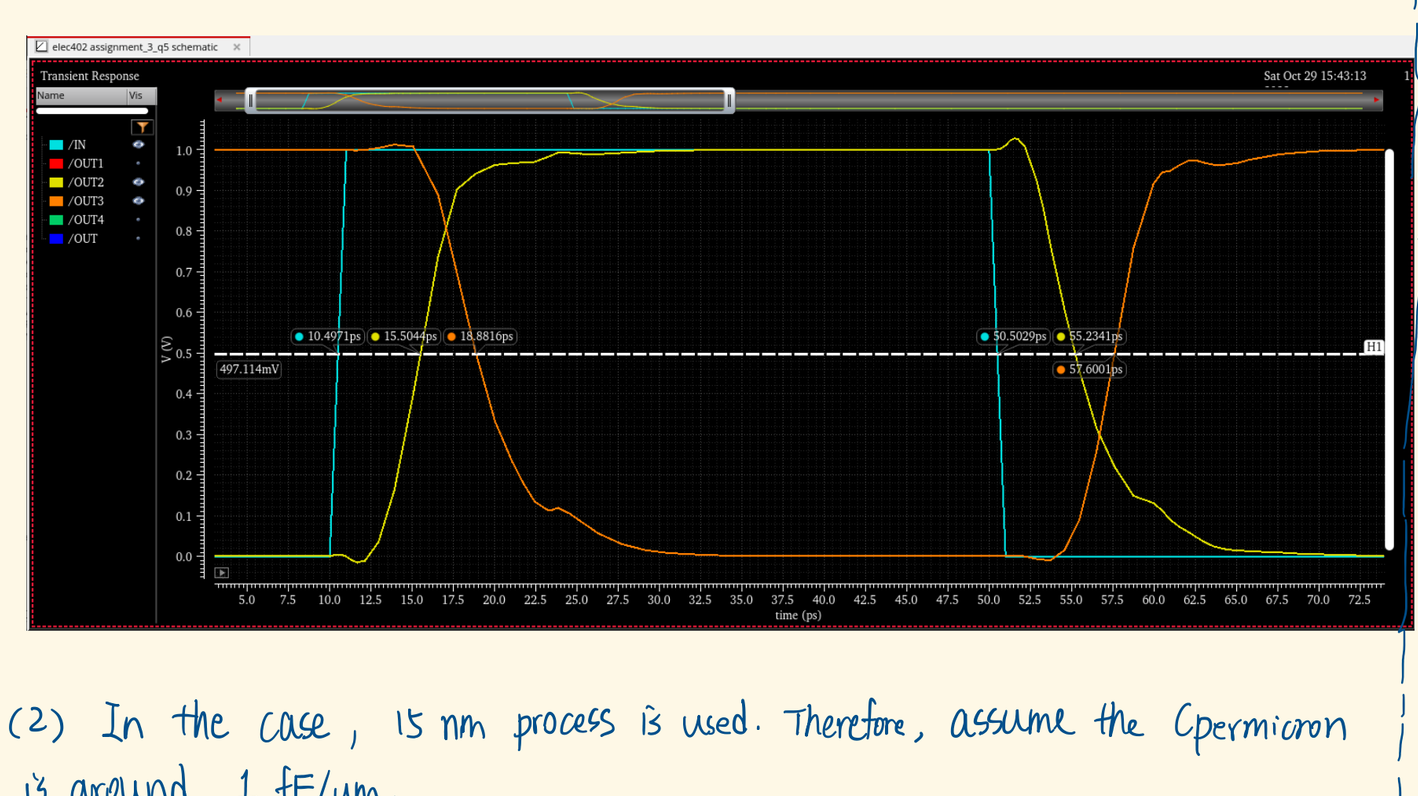


Vgs(V)	dx(dVds)	dy(dID)uA	slope(k*la	Y-intercpt	Lambda
0	/	/	/	/	/
0.6	2.53265	38.5965	1.52E-05	0.15	0.101597
1.2	2.13367	77.6449	3.64E-05	0.45	0.080867
1.8	1.624	98.1963	6.05E-05	0.78	0.07752
2.4	1.20808	116.338	9.63E-05	1.09	0.088349
3	0.53	64.7903	0.000122	1.35	0.090552
				Average:	0.087777

$$I_{DS} = \frac{\mu\cdot C_{ox}}{2}\cdot(V_{GS}-V_T)^2(1+\lambda\cdot V_{DS}) \quad \cdots\ eq.1$$

To find lambda, the eq.1 above is used. The Vgs is from 0 to 3V. For each value of Vgs,I treat the $\frac{\mu\cdot C_{ox}}{2}\cdot(V_{GS}-V_T)^2$ Part of eq.1 as a constant K. The eq.1 becomes Ids = K(1+λ*Vds) = K + Kλ*Vds, where the K is the Y-intercept (ID) and Kλ is the slope. In the figure above, the slope and the Y-intercept are obtained in Cadence. The λ is obtained using Kλ divided by K. The results are in the table above. The average λ is 0.087777 V^-1 which is in reasonable range.





Q5 (1)

The simulation result for the first testbench is below. The delay is the time different between OUT2 and OUT3 (since the third invertor is DUT) under ½ Vdd (0.5V). The Tpdr = 18.8816ps - 15.5044ps = 3.3812ps. The Tpdf = 57.6001ps - 55.234ps = 2.3661 ps. Thus the Tpd = (Tpdr+Tpdf)/2 = (3.3812 + 2.3661)/2 = 2.8735 ps.

The figure above shows the Ids vs Vsb where Vsb is DC sweeping from 0 to 1V. For each line, the Vt is the voltage where the Ids starts to rise. Vt0 is the grean line where Vsb is 0V. In this case, Vt0 is 258.186 mV.

To find the body-effect coefficient γ, the equation $V_t = V_{t0} + \gamma\cdot(\sqrt{V_{SB}+|2\phi_F|} - \sqrt{|2\phi_F|})$ is used. After transfermation, $\gamma = (V_t - V_{t0})/(\sqrt{V_{SB}+(2\phi_F)} - \sqrt{|2\phi_F|})$, where $2\phi_F$ is 0.88V.

The table below includes the Vt and Vsb for each line (Vsb from 0 to 1V).

Vsb (V)	Vt(V)	γ (V^0.5)	V2 (V)
0	0.258186	/	0.258186
0.2	0.258186	0.193401	0.458186
0.4	0.258186	0.099172	0.658186
0.6	0.258186	0.067688	0.858186
0.8	0.25819	0.051911	1.05819
1	0.25819	0.042399	1.25819
	Average	0.090914	

The data is sampled when Ids = 10 uA. In the schematic, V2 is the input voltage Vg. Also, Vsb is Vs. Therefore, Vgs = V2 - Vsb = Vt in the table.

As the table shown, after using the formula above, the body-effect coefficient is about 0.0909 V^0.5.

(2) In the case, 15 nm process is used. Therefore, assume the Cpermicron is around 1 fF/um.

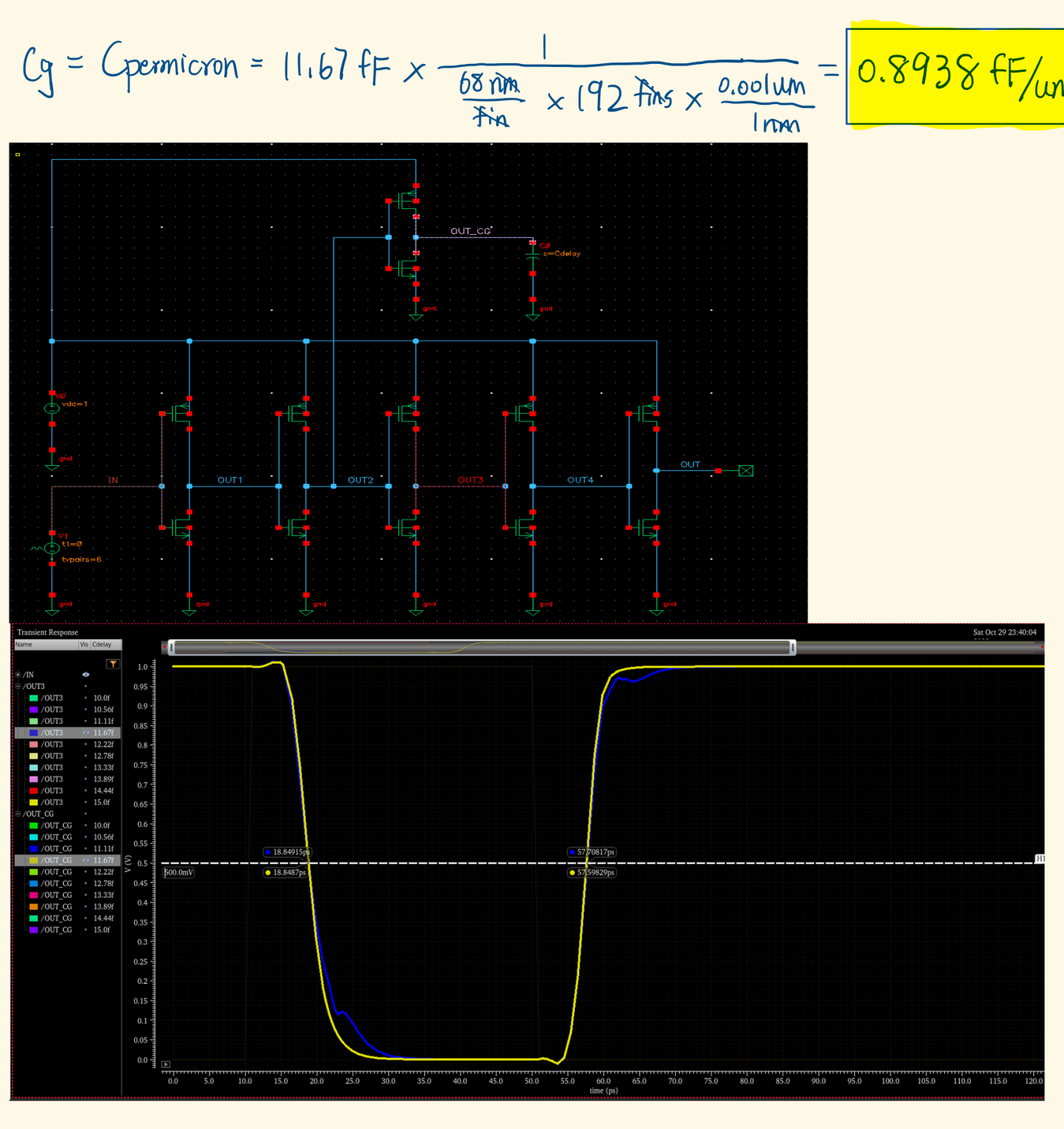
$$C_{permicron} = C_{delay}\times\frac{1}{\frac{68\ nm}{fin}\times n\ fins\times\frac{0.001um}{1nm}}$$

where n is the total fins of X4, which is 128 + 64 = 192

$$C_{gate} = C_{delay} = 1\ \frac{fF}{um}\times\frac{68\ nm}{fin}\times192\ fins\times\frac{0.001um}{1nm} = 13.056\ fF$$

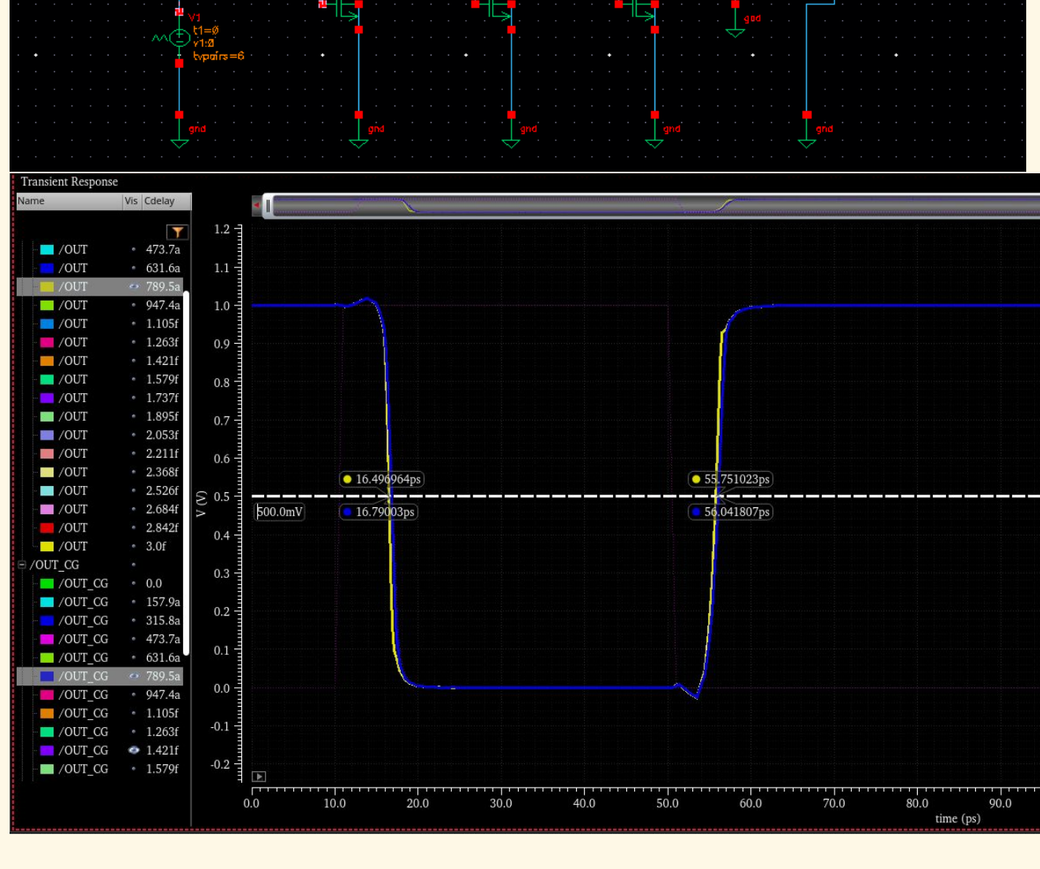
When Cpermicron = 1fF/um, Cdelay = 13.056 fF. So I sweep the Cdelay from 10 fF to 15 fF. The simulation results below shows that when Cdelay is 11.67 fF, the OUT-3 and OUT-CG matches perfectly at ½ Vdd. Therefore, the Cdelay is 11.67 fF in this case. The Cg is calculated.

$$C_g = C_{permicron} = 11.67\ fF\times\frac{1}{\frac{68\ nm}{fin}\times192\ fins\times\frac{0.001um}{1nm}} = \mathbf{0.8938\ fF/um}$$



(3) Parasitic Capacitance

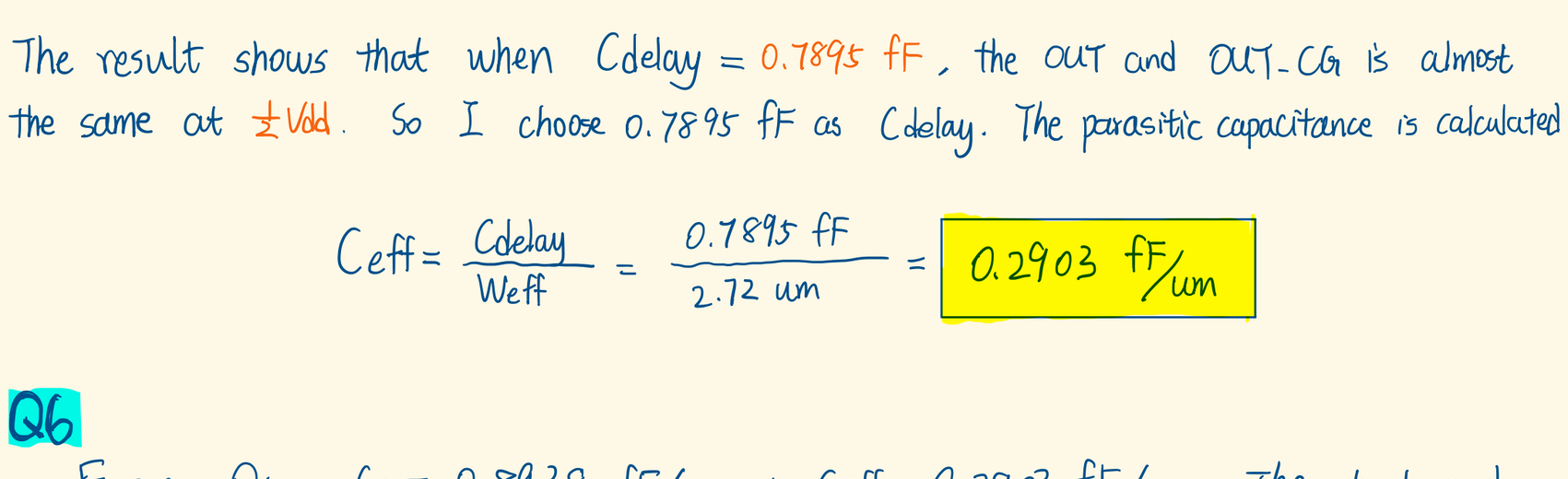
The schematic is below:



The used NMOS has 40 fins as metioned on piazza. Therefore, the Weff is calculated:

$$W_{eff} = \frac{68\ nm}{fin}\times40\ fins\times\frac{1um}{1000\ nm} = 2.72\ um.$$

When Cpermicron = 1 fF/um, Cdelay = 2.72 fF. Thus, I sweep Cdelay from 0 fF to 3 fF with 20 samples. The simulation result is below.



The result shows that when Cdelay = 0.7895 fF, the OUT and OUT-CG is almost the same at ½ Vdd. So I choose 0.7895 fF as Cdelay. The parasitic capacitance is calculated:

$$C_{eff} = \frac{C_{delay}}{W_{eff}} = \frac{0.7895\ fF}{2.72\ um} = \mathbf{0.2903\ fF/um}$$

Q6

From Q5, Cg = 0.8938 fF/um ; Ceff = 0.2903 fF/um. The tprd and tpdf are calculated. 'h' is 4 since this is Fanout 4. (1F = 1s/Ω)

$$t_{pdr} = \frac{R_P}{2}(3\cdot h\cdot C + 3C_d) = \frac{0.413\ k\Omega\cdot um}{2}\cdot\left(3\times4\times0.8938\frac{fF}{um} + 3\times0.2903\frac{fF}{um}\right)$$

$$\Rightarrow t_{pdr} = 2.3947\ k\Omega\cdot fF\times\frac{1000\Omega}{1k\Omega}\times\frac{10^{-15}F}{1fF}\times\frac{1\frac{s}{\Omega}}{1F}\times\frac{10^{12}ps}{1s} = \mathbf{2.3947ps}$$

$$t_{pdf} = R_n(3\cdot h\cdot C + 3C_d) = 0.266\ k\Omega\cdot um\cdot\left(3\times4\times0.8938\frac{fF}{um} + 3\times0.2903\frac{fF}{um}\right)$$

$$\Rightarrow t_{pdf} = 2.9123\ k\Omega\cdot fF\times\frac{1000\Omega}{1k\Omega}\times\frac{10^{-15}F}{1fF}\times\frac{1\frac{s}{\Omega}}{1F}\times\frac{10^{12}ps}{1s} = \mathbf{2.9123\ ps}$$

$$t_{pd} = (t_{pdr}+t_{pdf})/2 = (2.3947ps + 2.9123ps)/2 = \mathbf{2.6535\ ps}$$

Compared to the simulated tpd in Q5(1) which is 2.8735 ps, the calculated tpd (2.6535 ps) can be described as precise.