

# Assignment 4

Ruyi Zhou

November 2022

The NAND3 is designed and make using Cadence. The specifications are shown below: The  $\tau_{HL}$  is 26.5602ps. The  $\tau_{LH}$  is 23.0161ps. The average delay is  $\frac{26.5602+23.0161}{2} = 24.7882$ ps. The difference between  $\tau_{HL}$  and  $\tau_{LH} = 26.5602 - 23.0161 = 3.544$ ps  $< 5$ ps

Area: 0.145533  $\mu m^2$

Delay: 24.7882 ps

Area  $\times$  Delay =  $3.6074 \mu m^2 \cdot ps$

The figure below shows the schematics:

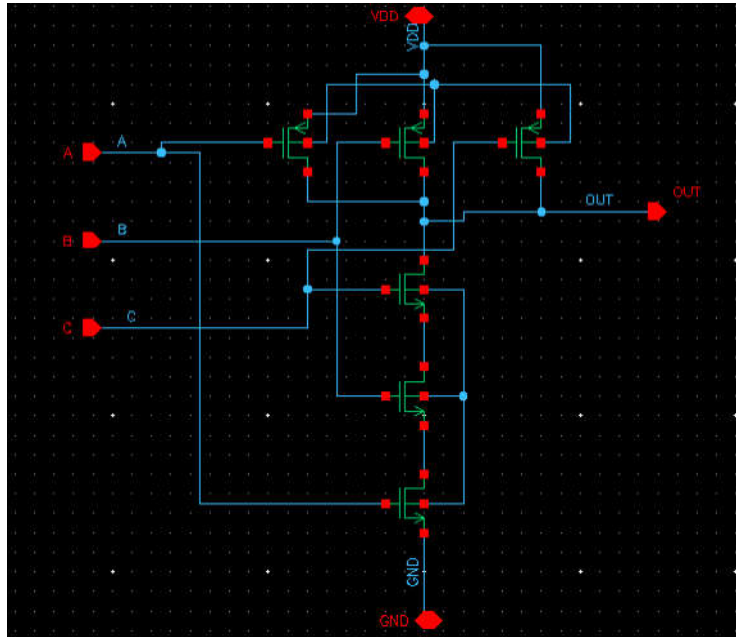


Figure 1: The schematics of the NAND3.

The figures below show the testbench with the **load capacitor**, the layout with dimensions, the netlist including all parasitics, the DRC summary. The last figure shows the simulation waveform, which indicates the  $\tau_{HL}$  and  $\tau_{LH}$  and the 10ps clock skew rate.

In Figure 3, the area is calculated by multiplying the length with width.

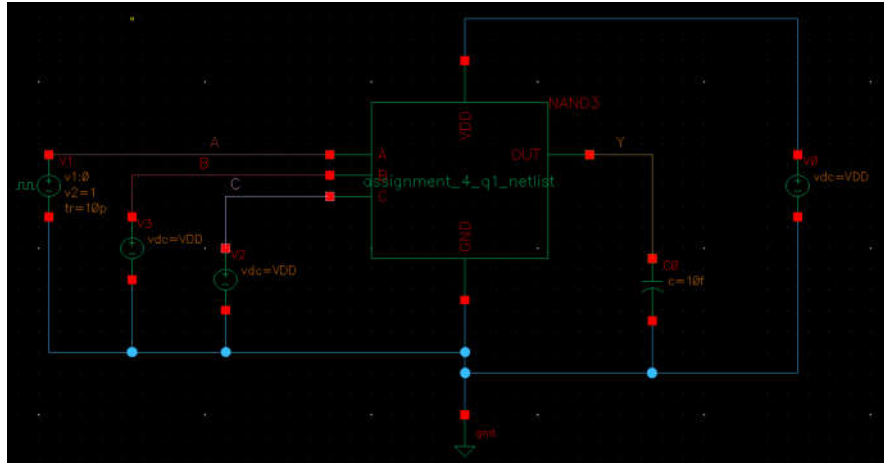


Figure 2: The testbench of the NAND3.

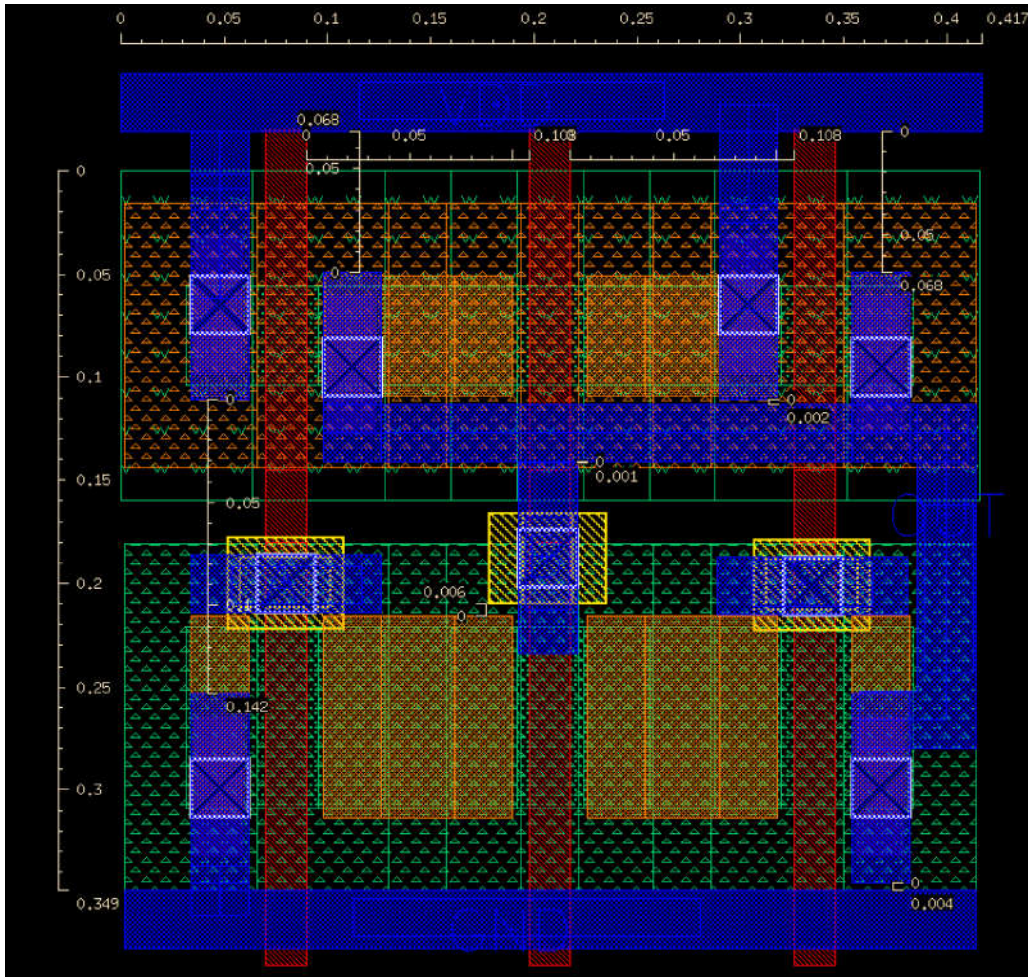


Figure 3: The layout of the NAND3.

```

PEX Netlist File - assignment_4_q1.pex.netlist
File Edit Options Windows

* File: assignment_4_q1.pex.netlist
* Created: Sun Nov 20 16:53:43 2022
* Program "Calibre xRC"
* Version "v2018.1_36,27"
*
* .include "assignment_4_q1.pex.netlist.pex"
* subckt assignment_4_q1 A GND B C VDD OUT
*
* OUT OUT
* VDD VDD
* C C
* B B
* GND GND
* A A
M0_noxref noxref_14 A N_GND_M0_noxref_s noxref_20 NFET L=2e-08 W=8.8e-08 NFIN=3
+ ADEJ=5.28e-16 ASEJ=4.56e-16 PDEJ=1.32e-07 PSEJ=1.14e-07
M1_noxref noxref_15 B noxref_14 noxref_20 NFET L=2e-08 W=8.8e-08 NFIN=3
+ ADEJ=1.056e-15 ASEJ=1.056e-15 PDEJ=2.88e-07 PSEJ=2.88e-07
M2_noxref N_OUT_M2_noxref_d C noxref_15 noxref_20 NFET L=2e-08 W=8.8e-08 NFIN=3
+ ADEJ=9.12e-16 ASEJ=9.28e-16 PDEJ=2.52e-07 PSEJ=1.32e-07
M3_noxref noxref_14 noxref_17 noxref_14 noxref_20 NFET L=2e-08 W=8.8e-08 NFIN=3
+ ADEJ=1.056e-15 ASEJ=1.056e-15 PDEJ=2.88e-07 PSEJ=2.88e-07
M4_noxref noxref_15 noxref_18 noxref_15 noxref_20 NFET L=2e-08 W=8.8e-08 NFIN=3
+ ADEJ=1.056e-15 ASEJ=1.056e-15 PDEJ=2.88e-07 PSEJ=2.88e-07
MM0_N_OUT_MM0_d A N_VDD_MM0_s NET1 PFET L=2e-08 W=4.8e-08 NFIN=2 ADEJ=3.52e-16
+ ASEJ=3.04e-16 PDEJ=9.8e-08 PSEJ=7.6e-08
MM1_N_OUT_MM0_d B N_VDD_MM1_s NET1 PFET L=2e-08 W=4.8e-08 NFIN=2 ADEJ=7.04e-16
+ ASEJ=7.04e-16 PDEJ=1.92e-07 PSEJ=1.92e-07
MM2_N_OUT_MM2_d C N_VDD_MM1_s NET1 PFET L=2e-08 W=4.8e-08 NFIN=2 ADEJ=6.08e-16
+ ASEJ=3.52e-16 PDEJ=1.68e-07 PSEJ=8.8e-08
M8_noxref N_OUT_MM0_d noxref_17 N_OUT_MM0_d NET1 PFET L=2e-08 W=4.8e-08 NFIN=2
+ ADEJ=7.04e-16 ASEJ=7.04e-16 PDEJ=1.92e-07 PSEJ=1.92e-07
M9_noxref N_VDD_MM1_s noxref_18 N_VDD_MM1_s NET1 PFET L=2e-08 W=4.8e-08 NFIN=2
+ ADEJ=7.04e-16 ASEJ=7.04e-16 PDEJ=1.92e-07 PSEJ=1.92e-07
c_7 A GND 0.018111f
c_15 B GND 0.0121583f
c_20 C GND 0.0104826f
c_44 noxref_14 GND 0.0738977f
c_49 noxref_15 GND 0.0734863f
*
* .include "assignment_4_q1.pex.netlist,ASSIGNMENT_4_Q1.pxi"
*
* .ends
*

```

Figure 4: The netlist of the NAND3.

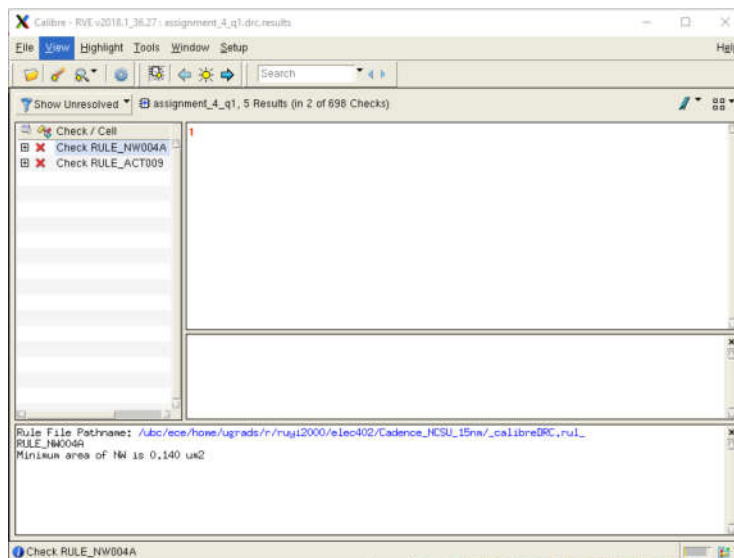


Figure 5: The part 1 of DRC report.

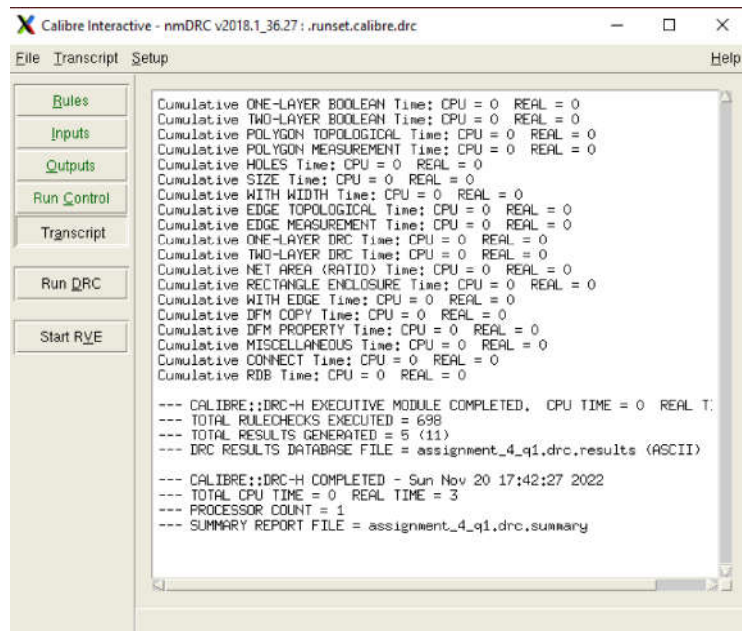


Figure 6: The part 2 of DRC report.

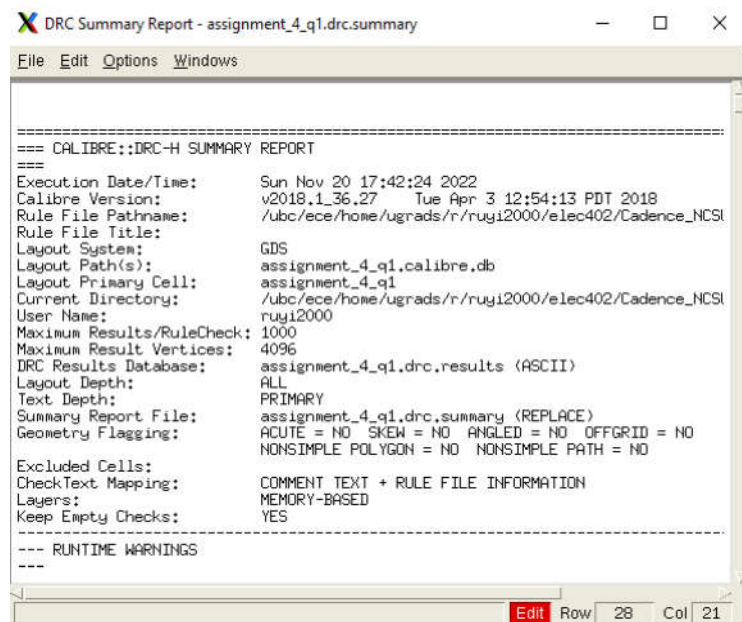


Figure 7: The part 3 of DRC report.



Figure 8: The waveform of the NAND3.