ELEC402 Introduction to VLSI System

Synthesized Washer & Dryer Machine

Assignment 2 Report

Ruyi Zhou

49581911

Mapped Verilog Generated by RTL Compiler

The figures below show the mapped Verilog file generated by the RTL compiler.

lec402 > Cadence_49581911 > synth > out > ≣ washer_machine_map.v

```
1
2   // Generated by Cadence Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
3
4   // Verification Directory fv/washer_machine
5
6   module washer_machine(mode, rst, clk, door_lock, water, spin, in_water,
7       channel_open, heater);
8     input [2:0] mode;
9     input rst, clk, door_lock, water;
10    output spin, in_water, channel_open, heater;
11    wire [2:0] mode;
12    wire rst, clk, door_lock, water;
13    wire spin, in_water, channel_open, heater;
14    wire [1:0] count;
15    wire [7:0] state;
16    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
17    wire n_8, n_9, n_10, n_12, n_13, n_14, n_15, n_16;
18    wire n_17, n_18, n_19, n_20, n_21, n_22, n_23, n_24;
19    wire n_25, n_26, n_27, n_28, n_29, n_30, n_32, n_33;
20    wire n_35, n_36, n_37, n_38, n_39, n_41, n_42, n_44;
21    wire n_45, n_47, n_48, n_49, n_50, n_51, n_52, n_53;
22    wire n_54, n_56, n_57, n_58, n_60, n_61, n_62, n_63;
23    wire n_64, n_65, n_66, n_67, n_68, n_69, n_70, n_71;
24    wire n_72, n_73, n_74, n_76, n_77, n_78, n_79, n_80;
25    wire n_81, n_82, n_83, n_84, n_85, n_87, n_89, n_91;
26    wire n_92, n_93, n_94, n_95, n_105, n_106, n_107, n_108;
27    wire n_109, n_110;
28    DFFSNQ_X1 \count_reg[0] (.SN (1'b1), .CLK (clk), .D (n_106), .Q
29        (count[0]));
30    DFFSNQ_X1 \state_reg[2] (.SN (1'b1), .CLK (clk), .D (n_95), .Q
31        (state[2]));
32    DFFSNQ_X1 \state_reg[6] (.SN (1'b1), .CLK (clk), .D (n_94), .Q
33        (state[6]));
34    DFFSNQ_X1 \count_reg[1] (.SN (1'b1), .CLK (clk), .D (n_93), .Q
35        (count[1]));
36    DFFSNQ_X1 \state_reg[3] (.SN (1'b1), .CLK (clk), .D (n_92), .Q
37        (state[3]));
38    DFFSNQ_X1 \state_reg[0] (.SN (1'b1), .CLK (clk), .D (n_89), .Q
39        (state[0]));
40    DFFSNQ_X1 \state_reg[1] (.SN (1'b1), .CLK (clk), .D (n_108), .Q
41        (state[1]));
42    NAND4_X1 g8493(.A1 (n_80), .A2 (n_60), .A3 (n_53), .A4 (n_91), .ZN
43        (n_95));
44    NAND2_X1 g8495(.A1 (n_84), .A2 (n_82), .ZN (n_94));
45    NAND2_X1 g8497(.A1 (n_78), .A2 (n_83), .ZN (n_93));
46    NAND4_X1 g8499(.A1 (n_73), .A2 (n_110), .A3 (n_56), .A4 (n_91), .ZN
47        (n_92));
48    DFFSNQ_X1 \state_reg[5] (.SN (1'b1), .CLK (clk), .D (n_87), .Q
49        (state[5]));
50    OR4_X1 g8491(.A1 (n_67), .A2 (n_81), .A3 (n_79), .A4 (n_57), .Z
51        (n_89));
52    NAND2_X1 g8506(.A1 (n_85), .A2 (n_71), .ZN (n_87));
53    DFFSNQ_X1 \state_reg[7] (.SN (1'b1), .CLK (clk), .D (n_69), .Q
54        (state[7]));
55    DFFSNQ_X1 \state_reg[4] (.SN (1'b1), .CLK (clk), .D (n_74), .Q
56        (state[4]));
57    NAND2_X1 g8503(.A1 (n_62), .A2 (count[1]), .ZN (n_83));
58    NOR2_X1 g8504(.A1 (n_70), .A2 (n_81), .ZN (n_82));
59    NOR3_X1 g8509(.A1 (n_81), .A2 (n_58), .A3 (n_79), .ZN (n_80));
60    AOI22_X1 g8510(.A1 (n_72), .A2 (n_20), .B1 (n_76), .B2 (n_65), .ZN
61        (n_78));
62    AOI22_X1 g8496(.A1 (count[0]), .A2 (n_42), .B1 (n_3), .B2 (n_76), .ZN
63        (n_77));
64    AOI21_X1 g8505(.A1 (n_4), .A2 (n_76), .B (n_72), .ZN (n_73));
65    NAND2_X1 g8511(.A1 (n_51), .A2 (water), .ZN (n_71));
66    NOR3_X1 g8515(.A1 (n_61), .A2 (n_66), .A3 (water), .ZN (n_70));
67    INV_X1 g8516(.I (n_68), .ZN (n_69));
68    OAI22_X1 g8498(.A1 (n_66), .A2 (n_28), .B1 (n_64), .B2 (n_63), .ZN
69        (n_67));
70    NOR3_X1 g8522(.A1 (n_65), .A2 (n_64), .A3 (n_63), .ZN (n_74));
71    NAND4_X1 g8523(.A1 (n_61), .A2 (n_15), .A3 (n_5), .A4 (n_54), .ZN
72        (n_62));
73    OR4_X1 g8525(.A1 (n_48), .A2 (n_66), .A3 (n_1), .A4 (mode[2]), .Z
74        (n_60));
75    INV_X1 g8537(.I (n_72), .ZN (n_85));
76    NOR2_X1 g8512(.A1 (n_56), .A2 (water), .ZN (n_57));
77    NAND3_X1 g8517(.A1 (n_79), .A2 (state[1]), .A3 (water), .ZN (n_68));
78    NAND2_X1 g8518(.A1 (n_8), .A2 (n_54), .ZN (n_84));
79    AOI21_X1 g8519(.A1 (n_38), .A2 (state[3]), .B (n_45), .ZN (n_81));
80    NOR3_X1 g8538(.A1 (n_30), .A2 (n_13), .A3 (n_50), .ZN (n_72));
81    OAI21_X1 g8513(.A1 (n_26), .A2 (n_37), .B (n_52), .ZN (n_53));
82    INV_X1 g8530(.I (n_64), .ZN (n_76));
83    INV_X1 g8532(.I (n_56), .ZN (n_51));
84    NOR3_X1 g8534(.A1 (n_33), .A2 (n_50), .A3 (state[7]), .ZN (n_58));
85    NOR3_X1 g8536(.A1 (n_32), .A2 (state[0]), .A3 (n_47), .ZN (n_79));
86    NOR4_X1 g8524(.A1 (n_48), .A2 (state[1]), .A3 (n_47), .A4 (n_21), .ZN
87        (n_49));
88    NOR2_X1 g8527(.A1 (n_50), .A2 (state[6]), .ZN (n_54));
89    NAND3_X1 g8528(.A1 (n_36), .A2 (n_41), .A3 (n_7), .ZN (n_91));
90    NAND2_X1 g8529(.A1 (n_65), .A2 (n_52), .ZN (n_66));
```

```
  NAND2_X1 g8531(.A1 (n_44), .A2 (n_52), .ZN (n_64));
  NAND3_X1 g8533(.A1 (channel_open), .A2 (n_24), .A3 (n_22), .ZN
      (n_56));
  OAI21_X1 g8535(.A1 (n_44), .A2 (state[3]), .B (n_52), .ZN (n_45));
  NAND4_X1 g8520(.A1 (n_16), .A2 (n_14), .A3 (n_41), .A4 (n_39), .ZN
      (n_42));
  NOR2_X1 g8539(.A1 (n_35), .A2 (n_29), .ZN (heater));
  NAND2_X1 g8542(.A1 (n_18), .A2 (n_39), .ZN (n_50));
  NAND2_X1 g8544(.A1 (n_27), .A2 (n_17), .ZN (n_38));
  INV_X1 g8546(.I (n_47), .ZN (n_52));
  NOR4_X1 g8548(.A1 (n_10), .A2 (state[0]), .A3 (n_23), .A4 (state[2]),
      .ZN (channel_open));
  NOR3_X1 g8555(.A1 (n_12), .A2 (state[0]), .A3 (mode[0]), .ZN (n_37));
  INV_X1 g8557(.I (n_35), .ZN (n_36));
  NOR2_X1 g8541(.A1 (n_33), .A2 (n_32), .ZN (in_water));
  NOR3_X1 g8545(.A1 (n_30), .A2 (n_32), .A3 (n_29), .ZN (spin));
  AOI22_X1 g8526(.A1 (n_27), .A2 (n_6), .B1 (n_9), .B2 (door_lock), .ZN
      (n_28));
  NOR2_X1 g8540(.A1 (state[1]), .A2 (n_25), .ZN (n_26));
  NAND3_X1 g8547(.A1 (n_24), .A2 (n_23), .A3 (n_22), .ZN (n_47));
  AOI22_X1 g8549(.A1 (n_20), .A2 (state[3]), .B1 (n_65), .B2 (mode[2]),
      .ZN (n_21));
  NAND2_X1 g8551(.A1 (n_27), .A2 (n_20), .ZN (n_19));
  NAND3_X1 g8558(.A1 (n_27), .A2 (state[3]), .A3 (state[4]), .ZN
      (n_35));
  INV_X1 g8571(.I (n_32), .ZN (n_18));
  AND2_X1 g8550(.A1 (n_23), .A2 (n_22), .Z (n_39));
  NOR2_X1 g8552(.A1 (n_20), .A2 (state[1]), .ZN (n_17));
  NAND2_X1 g8553(.A1 (n_30), .A2 (state[2]), .ZN (n_16));
  OAI21_X1 g8554(.A1 (n_29), .A2 (count[0]), .B (state[7]), .ZN (n_15));
  NAND3_X1 g8560(.A1 (state[0]), .A2 (n_29), .A3 (state[6]), .ZN
      (n_33));
  AOI21_X1 g8562(.A1 (n_0), .A2 (state[7]), .B (state[3]), .ZN (n_14));
  INV_X1 g8564(.I (n_41), .ZN (n_13));
  INV_X1 g8573(.I (n_27), .ZN (n_48));
  INV_X1 g8575(.I (n_44), .ZN (n_12));
  NAND2_X1 g8581(.A1 (n_9), .A2 (state[1]), .ZN (n_61));
  NOR2_X1 g8574(.A1 (n_9), .A2 (state[2]), .ZN (n_27));
  NAND3_X1 g8556(.A1 (n_9), .A2 (state[2]), .A3 (door_lock), .ZN
      (n_25));
  NOR3_X1 g8559(.A1 (state[0]), .A2 (state[1]), .A3 (state[7]), .ZN
      (n_8));
```

```
  NOR3_X1 g8561(.A1 (state[5]), .A2 (state[7]), .A3 (rst), .ZN (n_7));
  XNOR2_X1 g8563(.A1 (mode[2]), .A2 (mode[1]), .ZN (n_6));
  NAND2_X1 g8566(.A1 (n_9), .A2 (mode[0]), .ZN (n_63));
  NAND2_X1 g8572(.A1 (n_65), .A2 (state[2]), .ZN (n_32));
  NOR2_X1 g8576(.A1 (n_29), .A2 (state[2]), .ZN (n_44));
  NAND2_X1 g8577(.A1 (state[0]), .A2 (n_2), .ZN (n_5));
  NOR2_X1 g8582(.A1 (state[0]), .A2 (n_65), .ZN (n_4));
  NOR2_X1 g8580(.A1 (n_9), .A2 (state[3]), .ZN (n_3));
  NOR2_X1 g8565(.A1 (n_29), .A2 (state[6]), .ZN (n_41));
  NAND2_X1 g8579(.A1 (n_29), .A2 (state[3]), .ZN (n_10));
  NOR2_X1 g8569(.A1 (state[7]), .A2 (state[6]), .ZN (n_24));
  NAND2_X1 g8570(.A1 (state[0]), .A2 (state[7]), .ZN (n_30));
  NOR2_X1 g8568(.A1 (state[4]), .A2 (rst), .ZN (n_22));
  NOR2_X1 g8567(.A1 (count[1]), .A2 (count[0]), .ZN (n_20));
  INV_X1 g8586(.I (state[7]), .ZN (n_2));
  INV_X1 g8588(.I (state[5]), .ZN (n_23));
  INV_X1 g8589(.I (mode[1]), .ZN (n_1));
  INV_X1 g8585(.I (state[2]), .ZN (n_0));
  INV_X1 g8583(.I (state[3]), .ZN (n_65));
  INV_X1 g8584(.I (state[0]), .ZN (n_9));
  INV_X1 g8587(.I (state[1]), .ZN (n_29));
  NAND3_X1 g2(.A1 (n_105), .A2 (n_84), .A3 (n_77), .ZN (n_106));
  OR2_X1 g3(.A1 (n_85), .A2 (count[0]), .Z (n_105));
  NAND2_X1 g8600(.A1 (n_107), .A2 (n_68), .ZN (n_108));
  NOR3_X1 g8601(.A1 (n_58), .A2 (n_49), .A3 (n_74), .ZN (n_107));
  NAND2_X1 g8602(.A1 (n_109), .A2 (n_52), .ZN (n_110));
  AOI21_X1 g8603(.A1 (n_19), .A2 (n_25), .B (n_10), .ZN (n_109));
endmodule
```

Visual Waveforms showing state transitions from mapped Verilog

After synthesis, the circuit generated by the mapped Verilog contains time delays. The figures below compare the original waveform with the synthesized waveform and indicate the delays.

-1. The full scale of the comparison between the un-synthesized and synthesized Verilog

Figure 1. the un-synthesized Verilog model

Figure 2. the synthesized Verilog model

As shown above, the un-synthesized and synthesized models are quite similar. The states transitions and outputs signals work the same as the un-synthesized mode, which indicates the functionality works well after mapped. However, the synthesized model contains some tiny timing delays after zoom in. The figures below show the delays or the state transition and outputs.

-2. The Zoom-in scale of the comparison between the un-synthesized and synthesized Verilog

Figure 3. the un-synthesized Verilog signal of the state transition and output

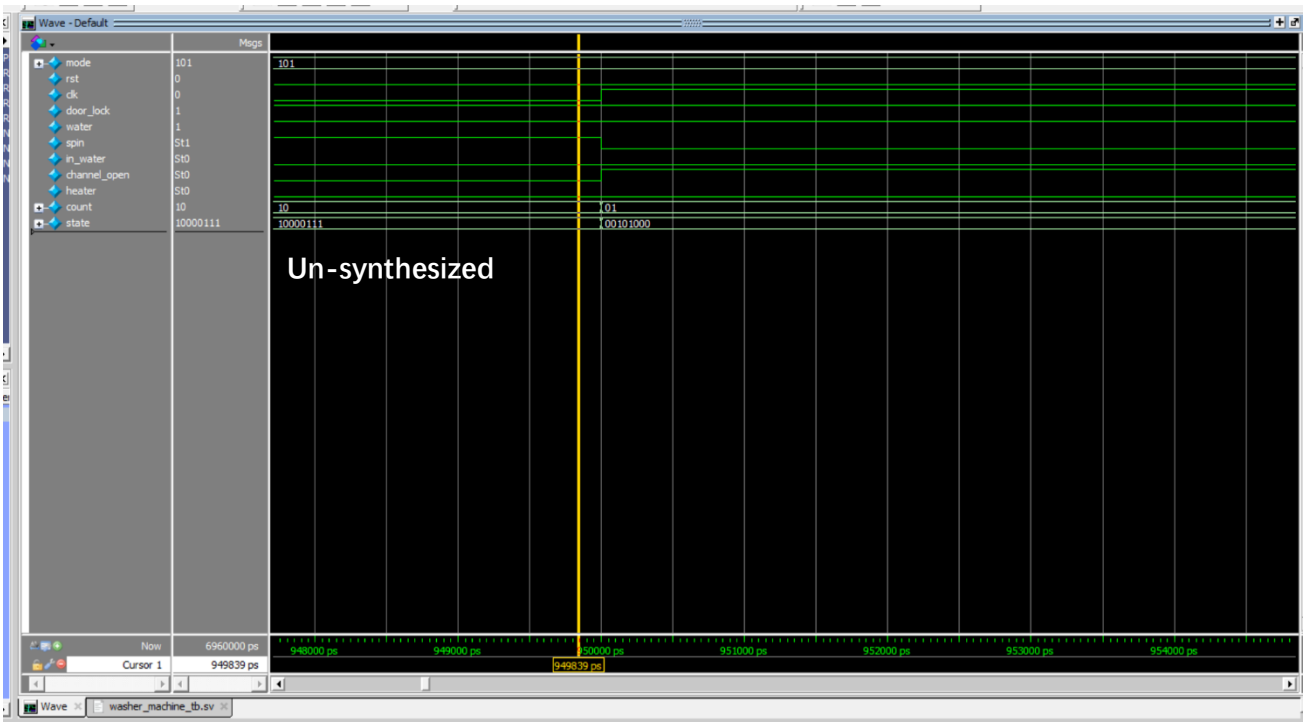
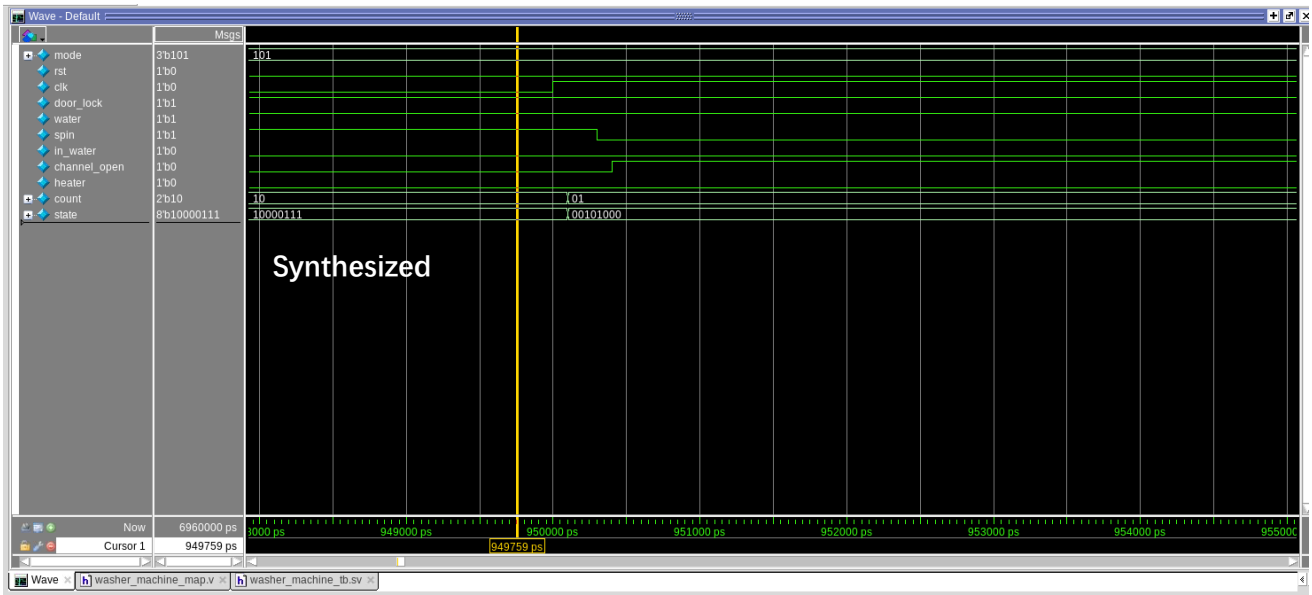


Figure 4. the synthesized Verilog signal of the state transition and output



As shown in **Figure 3**, in the un-synthesized model, the changes of outputs (*clk*, *spin*, *channel_open*) and the state (*0010_1000 wait_for_dry*) and the *count* signal happen exactly at the moment when the rising edge of clk happens.

However, in **Figure 4**, the synthesized model, the outputs (falling edge of *spin* and rising edge of *channel_open*) , the states and count signal are changed slightly behind the rising edge of the *clk*, which indicates a time delay happened.

Figure 5. the un-synthesized Verilog output ‘spin’ signal

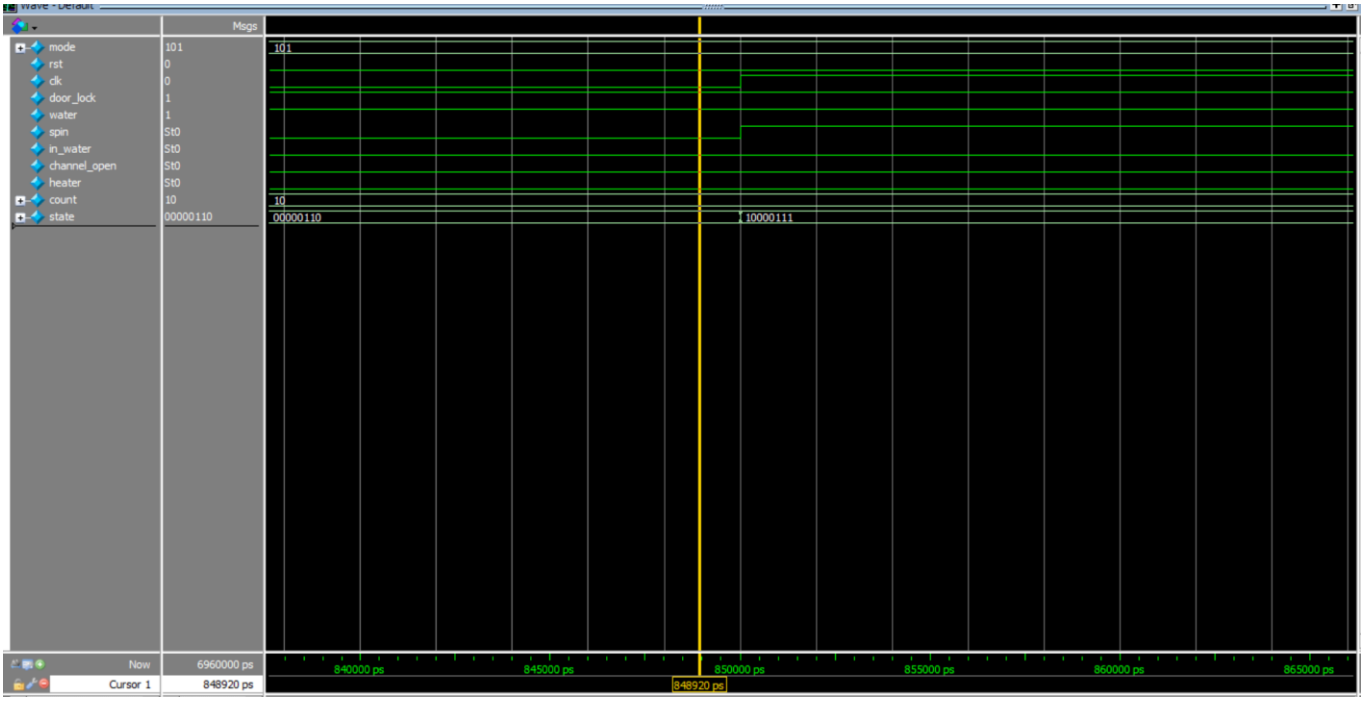
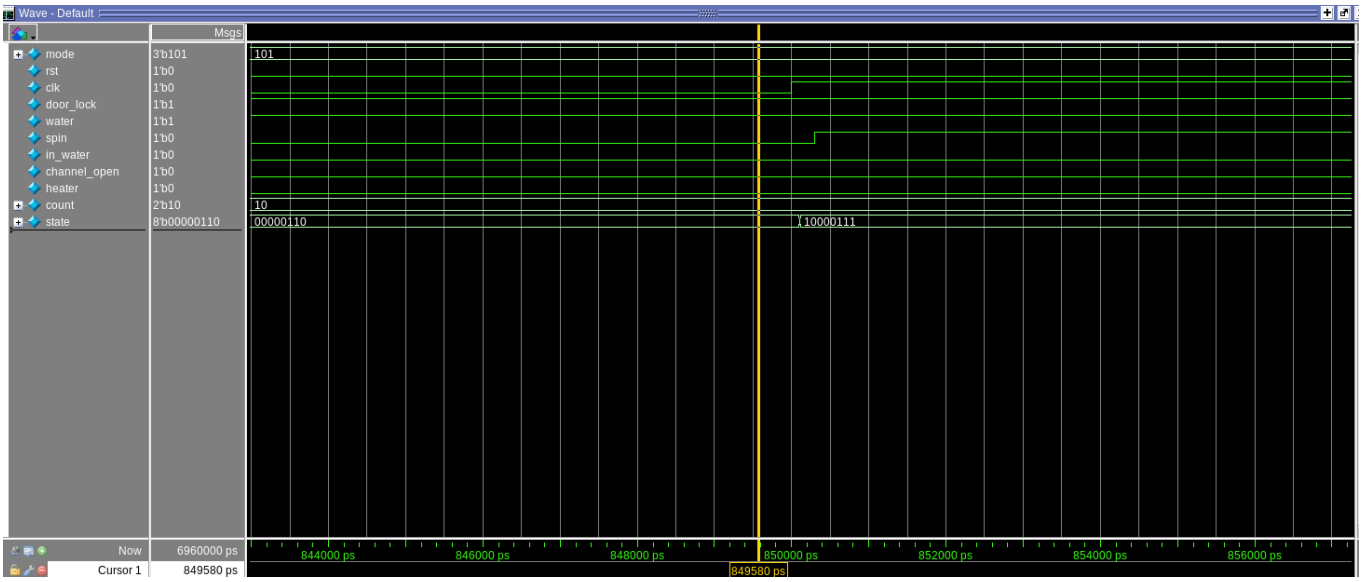


Figure 6. the synthesized Verilog output ‘spin’ signal



It can be seen that there is a timing delay on the output signal ‘spin’ in the synthesized Verilog compared to the un-synthesized model.

Figure 7. the un-synthesized Verilog output ‘in_water’ signal

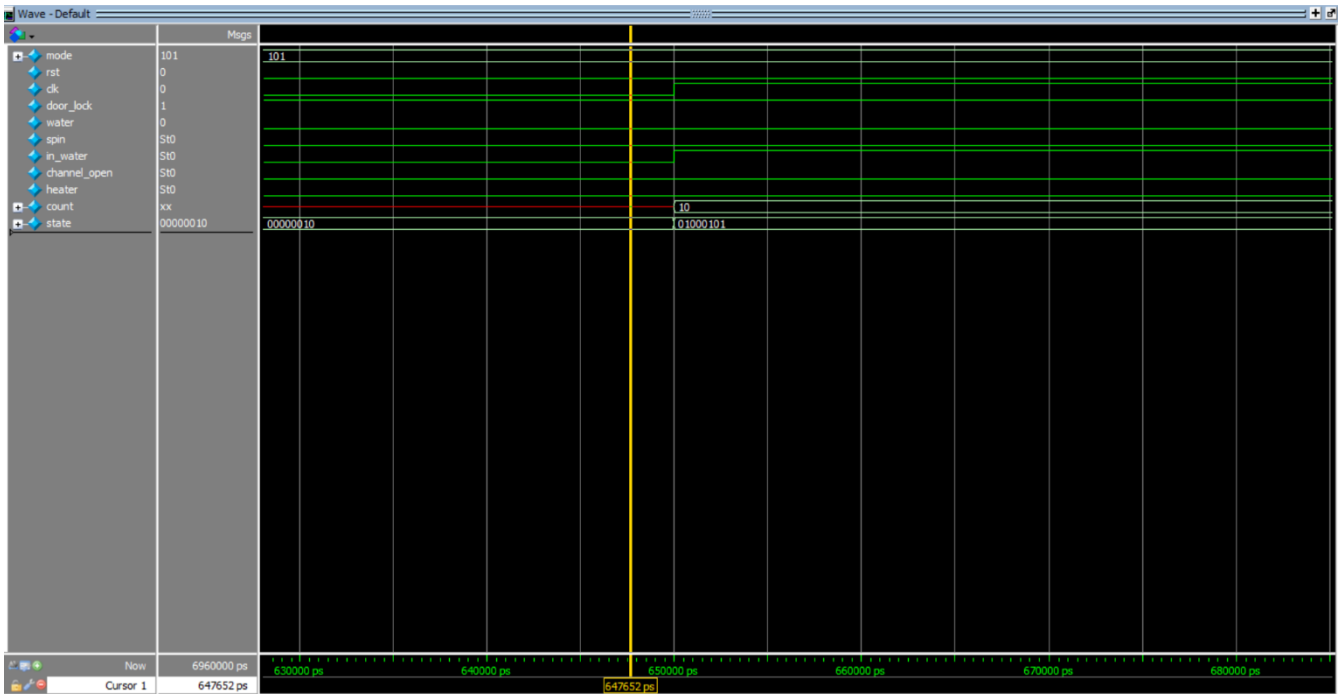
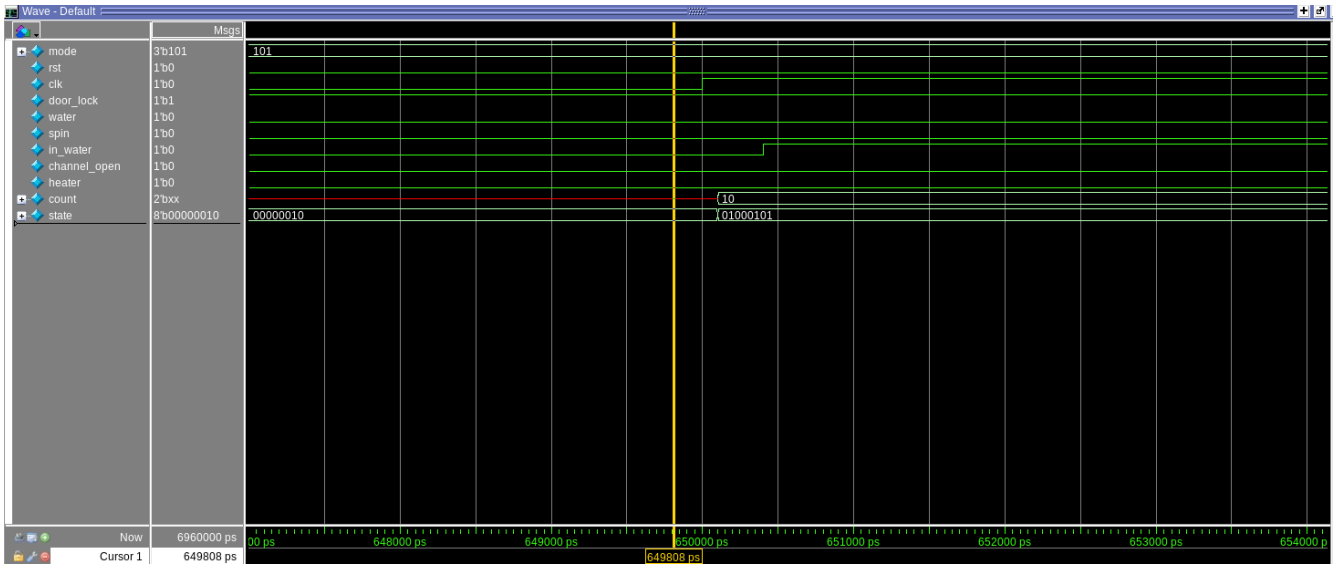


Figure 8. the synthesized Verilog output ‘in_water’ signal



As shown above, there is a timing delay on the output signal ‘in_water’ in the synthesized Verilog compared to the un-synthesized model.

Figure 9. the un-synthesized Verilog output ‘heater’ signal

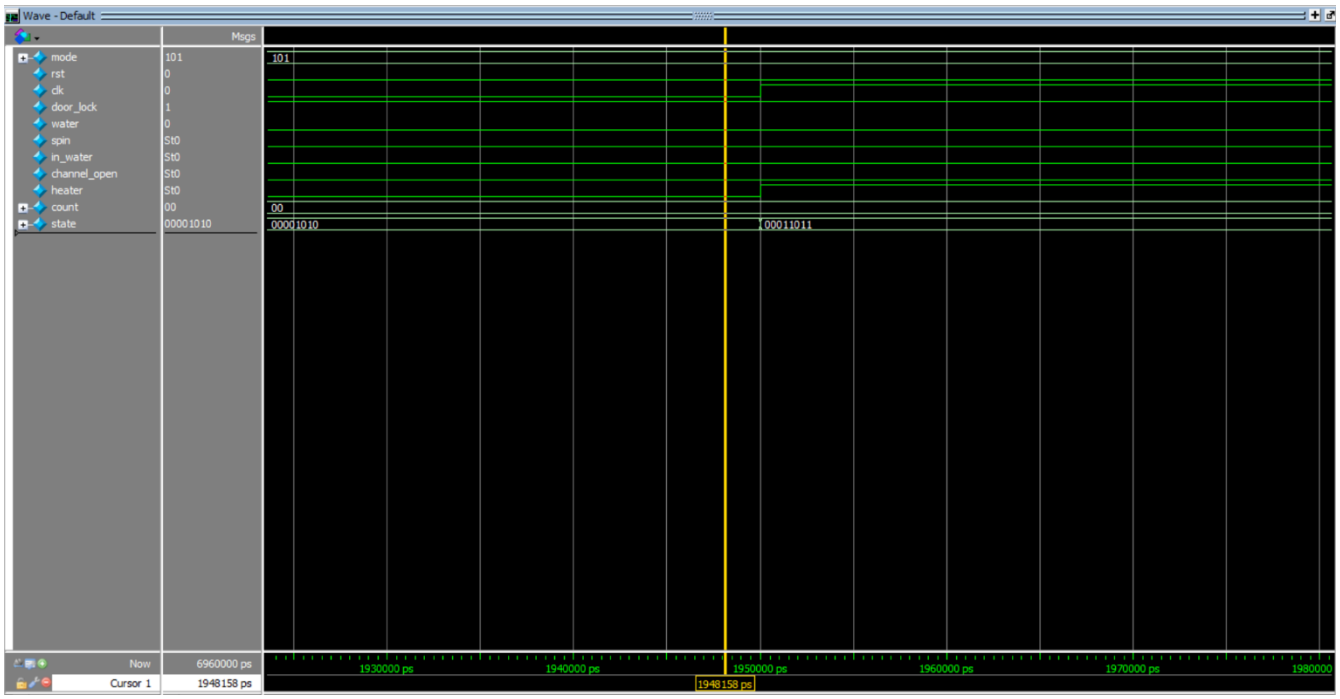


Figure 10. the synthesized Verilog output ‘heater’ signal

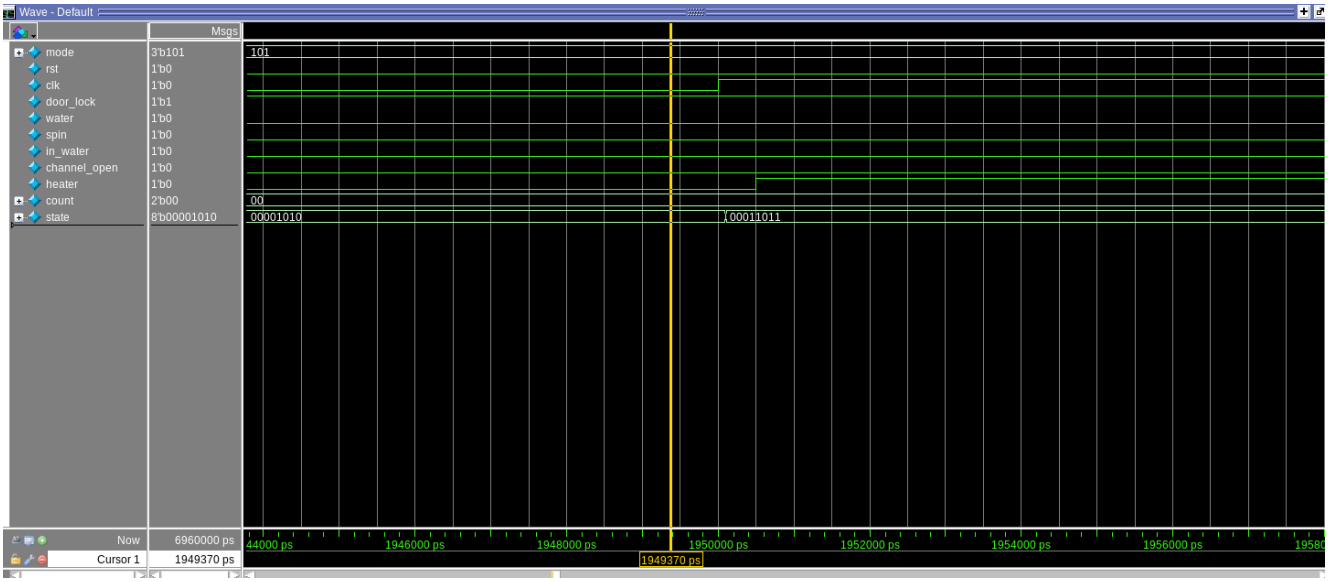


Figure 10 shows there is a timing delay on the output signal ‘heater’ in the synthesized model compared to the un-synthesized one.

Even though all the four output signals and the state transition have the timing delay, the Figure 1 and Figure 2 show that the functionality of this design works well. The timing delay in the synthesized model **may come from the resistance or capacitance in the wires** because the synthesized model considers the physical properties in the real world.

Report from RTL Compiler showing total number of cells in the project

The area report below indicates the total cells of this design contains ***104 cells***, which exceeds the minimum requirements (100 cells). The cells are consisting of the logic gates from the FSM design.

elec402 > Cadence_49581911 > synth > out > washer_machine_area.rpt

```
1   ====================================================================
2     Generated by:           Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
3     Generated on:           Oct 07 2022  08:06:45 pm
4     Module:                 washer_machine
5     Technology library:     NanGate_15nm_OCL revision 1.0
6     Operating conditions:   worst_low (balanced_tree)
7     Wireload mode:          enclosed
8     Area mode:              timing library
9   ====================================================================
10
11    Instance     Cells  Cell Area  Net Area  Total Area  Wireload
12  --------------------------------------------------------------------
13  washer_machine    104         36         0          36    <none> (D)
14
15    (D) = wireload is default in technology library
16
```

Appendix 1. The code of the Mapped Verilog file

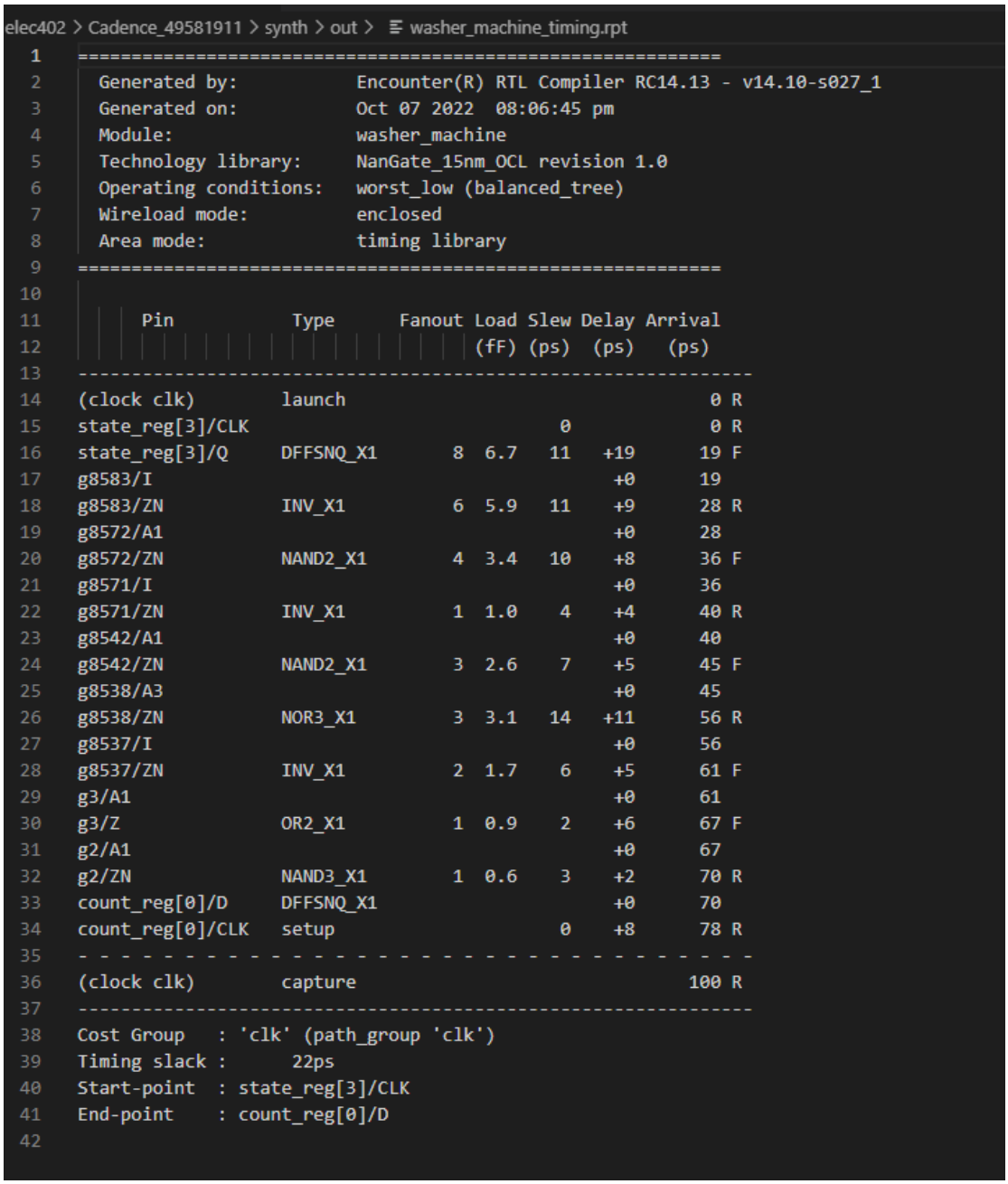
```
// Generated by Cadence Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1

// Verification Directory fv/washer_machine

module washer_machine(mode, rst, clk, door_lock, water, spin, in_water,
        channel_open, heater);
   input [2:0] mode;
   input rst, clk, door_lock, water;
   output spin, in_water, channel_open, heater;
   wire [2:0] mode;
   wire rst, clk, door_lock, water;
   wire spin, in_water, channel_open, heater;
   wire [1:0] count;
   wire [7:0] state;
   wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
   wire n_8, n_9, n_10, n_12, n_13, n_14, n_15, n_16;
   wire n_17, n_18, n_19, n_20, n_21, n_22, n_23, n_24;
   wire n_25, n_26, n_27, n_28, n_29, n_30, n_32, n_33;
   wire n_35, n_36, n_37, n_38, n_39, n_41, n_42, n_44;
   wire n_45, n_47, n_48, n_49, n_50, n_51, n_52, n_53;
   wire n_54, n_56, n_57, n_58, n_60, n_61, n_62, n_63;
   wire n_64, n_65, n_66, n_67, n_68, n_69, n_70, n_71;
   wire n_72, n_73, n_74, n_76, n_77, n_78, n_79, n_80;
   wire n_81, n_82, n_83, n_84, n_85, n_87, n_89, n_91;
   wire n_92, n_93, n_94, n_95, n_105, n_106, n_107, n_108;
   wire n_109, n_110;
   DFFSNQ_X1 \count_reg[0] (.SN (1'b1), .CLK (clk), .D (n_106), .Q
        (count[0]));
   DFFSNQ_X1 \state_reg[2] (.SN (1'b1), .CLK (clk), .D (n_95), .Q
        (state[2]));
   DFFSNQ_X1 \state_reg[6] (.SN (1'b1), .CLK (clk), .D (n_94), .Q
        (state[6]));
   DFFSNQ_X1 \count_reg[1] (.SN (1'b1), .CLK (clk), .D (n_93), .Q
        (count[1]));
   DFFSNQ_X1 \state_reg[3] (.SN (1'b1), .CLK (clk), .D (n_92), .Q
        (state[3]));
   DFFSNQ_X1 \state_reg[0] (.SN (1'b1), .CLK (clk), .D (n_89), .Q
        (state[0]));
   DFFSNQ_X1 \state_reg[1] (.SN (1'b1), .CLK (clk), .D (n_108), .Q
        (state[1]));
   NAND4_X1 g8493(.A1 (n_80), .A2 (n_60), .A3 (n_53), .A4 (n_91), .ZN
        (n_95));
```

```
NAND2_X1 g8495(.A1 (n_84), .A2 (n_82), .ZN (n_94));
NAND2_X1 g8497(.A1 (n_78), .A2 (n_83), .ZN (n_93));
NAND4_X1 g8499(.A1 (n_73), .A2 (n_110), .A3 (n_56), .A4 (n_91), .ZN
        (n_92));
DFFSNQ_X1 \state_reg[5] (.SN (1'b1), .CLK (clk), .D (n_87), .Q
        (state[5]));
OR4_X1 g8491(.A1 (n_67), .A2 (n_81), .A3 (n_79), .A4 (n_57), .Z
        (n_89));
NAND2_X1 g8506(.A1 (n_85), .A2 (n_71), .ZN (n_87));
DFFSNQ_X1 \state_reg[7] (.SN (1'b1), .CLK (clk), .D (n_69), .Q
        (state[7]));
DFFSNQ_X1 \state_reg[4] (.SN (1'b1), .CLK (clk), .D (n_74), .Q
        (state[4]));
NAND2_X1 g8503(.A1 (n_62), .A2 (count[1]), .ZN (n_83));
NOR2_X1 g8504(.A1 (n_70), .A2 (n_81), .ZN (n_82));
NOR3_X1 g8509(.A1 (n_81), .A2 (n_58), .A3 (n_79), .ZN (n_80));
AOI22_X1 g8510(.A1 (n_72), .A2 (n_20), .B1 (n_76), .B2 (n_65), .ZN
        (n_78));
AOI22_X1 g8496(.A1 (count[0]), .A2 (n_42), .B1 (n_3), .B2 (n_76), .ZN
        (n_77));
AOI21_X1 g8505(.A1 (n_4), .A2 (n_76), .B (n_72), .ZN (n_73));
NAND2_X1 g8511(.A1 (n_51), .A2 (water), .ZN (n_71));
NOR3_X1 g8515(.A1 (n_61), .A2 (n_66), .A3 (water), .ZN (n_70));
INV_X1 g8516(.I (n_68), .ZN (n_69));
OAI22_X1 g8498(.A1 (n_66), .A2 (n_28), .B1 (n_64), .B2 (n_63), .ZN
        (n_67));
NOR3_X1 g8522(.A1 (n_65), .A2 (n_64), .A3 (n_63), .ZN (n_74));
NAND4_X1 g8523(.A1 (n_61), .A2 (n_15), .A3 (n_5), .A4 (n_54), .ZN
        (n_62));
OR4_X1 g8525(.A1 (n_48), .A2 (n_66), .A3 (n_1), .A4 (mode[2]), .Z
        (n_60));
INV_X1 g8537(.I (n_72), .ZN (n_85));
NOR2_X1 g8512(.A1 (n_56), .A2 (water), .ZN (n_57));
NAND3_X1 g8517(.A1 (n_79), .A2 (state[1]), .A3 (water), .ZN (n_68));
NAND2_X1 g8518(.A1 (n_8), .A2 (n_54), .ZN (n_84));
AOI21_X1 g8519(.A1 (n_38), .A2 (state[3]), .B (n_45), .ZN (n_81));
NOR3_X1 g8538(.A1 (n_30), .A2 (n_13), .A3 (n_50), .ZN (n_72));
OAI21_X1 g8513(.A1 (n_26), .A2 (n_37), .B (n_52), .ZN (n_53));
INV_X1 g8530(.I (n_64), .ZN (n_76));
INV_X1 g8532(.I (n_56), .ZN (n_51));
NOR3_X1 g8534(.A1 (n_33), .A2 (n_50), .A3 (state[7]), .ZN (n_58));
NOR3_X1 g8536(.A1 (n_32), .A2 (state[0]), .A3 (n_47), .ZN (n_79));
NOR4_X1 g8524(.A1 (n_48), .A2 (state[1]), .A3 (n_47), .A4 (n_21), .ZN
        (n_49));
```

```
NOR2_X1 g8527(.A1 (n_50), .A2 (state[6]), .ZN (n_54));
NAND3_X1 g8528(.A1 (n_36), .A2 (n_41), .A3 (n_7), .ZN (n_91));
NAND2_X1 g8529(.A1 (n_65), .A2 (n_52), .ZN (n_66));
NAND2_X1 g8531(.A1 (n_44), .A2 (n_52), .ZN (n_64));
NAND3_X1 g8533(.A1 (channel_open), .A2 (n_24), .A3 (n_22), .ZN
    (n_56));
OAI21_X1 g8535(.A1 (n_44), .A2 (state[3]), .B (n_52), .ZN (n_45));
NAND4_X1 g8520(.A1 (n_16), .A2 (n_14), .A3 (n_41), .A4 (n_39), .ZN
    (n_42));
NOR2_X1 g8539(.A1 (n_35), .A2 (n_29), .ZN (heater));
NAND2_X1 g8542(.A1 (n_18), .A2 (n_39), .ZN (n_50));
NAND2_X1 g8544(.A1 (n_27), .A2 (n_17), .ZN (n_38));
INV_X1 g8546(.I (n_47), .ZN (n_52));
NOR4_X1 g8548(.A1 (n_10), .A2 (state[0]), .A3 (n_23), .A4 (state[2]),
    .ZN (channel_open));
NOR3_X1 g8555(.A1 (n_12), .A2 (state[0]), .A3 (mode[0]), .ZN (n_37));
INV_X1 g8557(.I (n_35), .ZN (n_36));
NOR2_X1 g8541(.A1 (n_33), .A2 (n_32), .ZN (in_water));
NOR3_X1 g8545(.A1 (n_30), .A2 (n_32), .A3 (n_29), .ZN (spin));
AOI22_X1 g8526(.A1 (n_27), .A2 (n_6), .B1 (n_9), .B2 (door_lock), .ZN
    (n_28));
NOR2_X1 g8540(.A1 (state[1]), .A2 (n_25), .ZN (n_26));
NAND3_X1 g8547(.A1 (n_24), .A2 (n_23), .A3 (n_22), .ZN (n_47));
AOI22_X1 g8549(.A1 (n_20), .A2 (state[3]), .B1 (n_65), .B2 (mode[2]),
    .ZN (n_21));
NAND2_X1 g8551(.A1 (n_27), .A2 (n_20), .ZN (n_19));
NAND3_X1 g8558(.A1 (n_27), .A2 (state[3]), .A3 (state[4]), .ZN
    (n_35));
INV_X1 g8571(.I (n_32), .ZN (n_18));
AND2_X1 g8550(.A1 (n_23), .A2 (n_22), .Z (n_39));
NOR2_X1 g8552(.A1 (n_20), .A2 (state[1]), .ZN (n_17));
NAND2_X1 g8553(.A1 (n_30), .A2 (state[2]), .ZN (n_16));
OAI21_X1 g8554(.A1 (n_29), .A2 (count[0]), .B (state[7]), .ZN (n_15));
NAND3_X1 g8560(.A1 (state[0]), .A2 (n_29), .A3 (state[6]), .ZN
    (n_33));
AOI21_X1 g8562(.A1 (n_0), .A2 (state[7]), .B (state[3]), .ZN (n_14));
INV_X1 g8564(.I (n_41), .ZN (n_13));
INV_X1 g8573(.I (n_27), .ZN (n_48));
INV_X1 g8575(.I (n_44), .ZN (n_12));
NAND2_X1 g8581(.A1 (n_9), .A2 (state[1]), .ZN (n_61));
NOR2_X1 g8574(.A1 (n_9), .A2 (state[2]), .ZN (n_27));
NAND3_X1 g8556(.A1 (n_9), .A2 (state[2]), .A3 (door_lock), .ZN
    (n_25));
NOR3_X1 g8559(.A1 (state[0]), .A2 (state[1]), .A3 (state[7]), .ZN
```

```
        (n_8));
    NOR3_X1 g8561(.A1 (state[5]), .A2 (state[7]), .A3 (rst), .ZN (n_7));
    XNOR2_X1 g8563(.A1 (mode[2]), .A2 (mode[1]), .ZN (n_6));
    NAND2_X1 g8566(.A1 (n_9), .A2 (mode[0]), .ZN (n_63));
    NAND2_X1 g8572(.A1 (n_65), .A2 (state[2]), .ZN (n_32));
    NOR2_X1 g8576(.A1 (n_29), .A2 (state[2]), .ZN (n_44));
    NAND2_X1 g8577(.A1 (state[0]), .A2 (n_2), .ZN (n_5));
    NOR2_X1 g8582(.A1 (state[0]), .A2 (n_65), .ZN (n_4));
    NOR2_X1 g8580(.A1 (n_9), .A2 (state[3]), .ZN (n_3));
    NOR2_X1 g8565(.A1 (n_29), .A2 (state[6]), .ZN (n_41));
    NAND2_X1 g8579(.A1 (n_29), .A2 (state[3]), .ZN (n_10));
    NOR2_X1 g8569(.A1 (state[7]), .A2 (state[6]), .ZN (n_24));
    NAND2_X1 g8570(.A1 (state[0]), .A2 (state[7]), .ZN (n_30));
    NOR2_X1 g8568(.A1 (state[4]), .A2 (rst), .ZN (n_22));
    NOR2_X1 g8567(.A1 (count[1]), .A2 (count[0]), .ZN (n_20));
    INV_X1 g8586(.I (state[7]), .ZN (n_2));
    INV_X1 g8588(.I (state[5]), .ZN (n_23));
    INV_X1 g8589(.I (mode[1]), .ZN (n_1));
    INV_X1 g8585(.I (state[2]), .ZN (n_0));
    INV_X1 g8583(.I (state[3]), .ZN (n_65));
    INV_X1 g8584(.I (state[0]), .ZN (n_9));
    INV_X1 g8587(.I (state[1]), .ZN (n_29));
    NAND3_X1 g2(.A1 (n_105), .A2 (n_84), .A3 (n_77), .ZN (n_106));
    OR2_X1 g3(.A1 (n_85), .A2 (count[0]), .Z (n_105));
    NAND2_X1 g8600(.A1 (n_107), .A2 (n_68), .ZN (n_108));
    NOR3_X1 g8601(.A1 (n_58), .A2 (n_49), .A3 (n_74), .ZN (n_107));
    NAND2_X1 g8602(.A1 (n_109), .A2 (n_52), .ZN (n_110));
    AOI21_X1 g8603(.A1 (n_19), .A2 (n_25), .B (n_10), .ZN (n_109));
endmodule
```

Appendix 2. The timing report



elec402 > Cadence_49581911 > synth > out > washer_machine_timing.rpt

```
1   ============================================================
2     Generated by:           Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
3     Generated on:           Oct 07 2022  08:06:45 pm
4     Module:                 washer_machine
5     Technology library:     NanGate_15nm_OCL revision 1.0
6     Operating conditions:   worst_low (balanced_tree)
7     Wireload mode:          enclosed
8     Area mode:              timing library
9   ============================================================
10
11        Pin           Type      Fanout Load Slew Delay Arrival
12                                        (fF) (ps)  (ps)   (ps)
13  ------------------------------------------------------------
14  (clock clk)         launch                                0 R
15  state_reg[3]/CLK                             0            0 R
16  state_reg[3]/Q      DFFSNQ_X1       8  6.7   11   +19     19 F
17  g8583/I                                          +0      19
18  g8583/ZN            INV_X1          6  5.9   11    +9     28 R
19  g8572/A1                                         +0      28
20  g8572/ZN            NAND2_X1        4  3.4   10    +8     36 F
21  g8571/I                                          +0      36
22  g8571/ZN            INV_X1          1  1.0    4    +4     40 R
23  g8542/A1                                         +0      40
24  g8542/ZN            NAND2_X1        3  2.6    7    +5     45 F
25  g8538/A3                                         +0      45
26  g8538/ZN            NOR3_X1         3  3.1   14   +11     56 R
27  g8537/I                                          +0      56
28  g8537/ZN            INV_X1          2  1.7    6    +5     61 F
29  g3/A1                                            +0      61
30  g3/Z                OR2_X1          1  0.9    2    +6     67 F
31  g2/A1                                            +0      67
32  g2/ZN               NAND3_X1        1  0.6    3    +2     70 R
33  count_reg[0]/D      DFFSNQ_X1                    +0      70
34  count_reg[0]/CLK    setup                        0    +8     78 R
35  - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
36  (clock clk)         capture                             100 R
37  ------------------------------------------------------------
38  Cost Group   : 'clk' (path_group 'clk')
39  Timing slack :      22ps
40  Start-point  : state_reg[3]/CLK
41  End-point    : count_reg[0]/D
42
```

The timing document shows that this design has a positive timing slack (22ps).