Assignment 4

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The NAND3 is designed and make using Cadence. The specifications are shown below: The τ_{HL} is 26.5602ps. The τ_{LH} is 23.0161ps. The average delay is $\frac{26.5602+23.0161}{2}$ = 24.7882ps. The difference between τ_{HL} and τ_{LH} = 26.5602 - 23.0161 = 3.544ps < 5ps

$$\text{Area: } 0.145533\ \mu m^2$$
$$\text{Delay: } 24.7882\ \text{ps}$$
$$\text{Area} \times \text{Delay} = \boxed{3.6074 \mu m^2 \cdot ps}$$

The figure below shows the schematics:

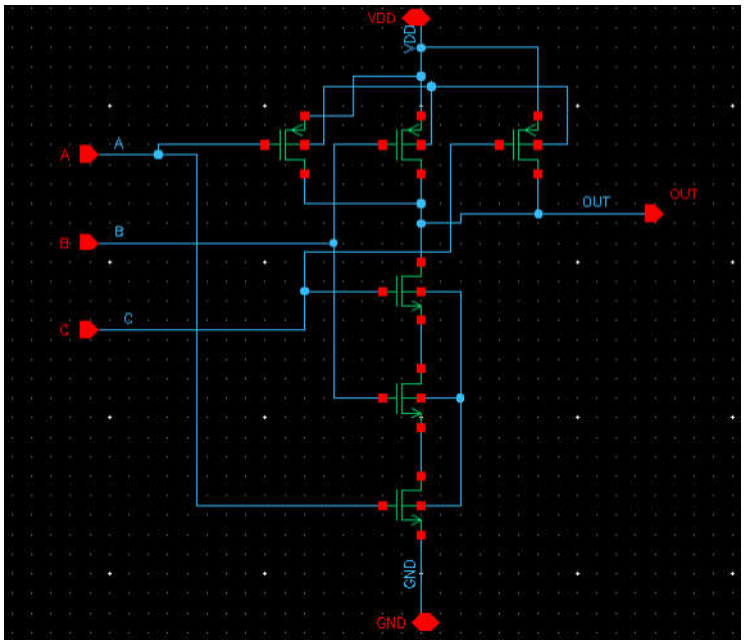

Figure 1: The schematics of the NAND3.

The figures below show the testbench with the ***load capacitor***,the layout with demensions,the netlist including all parasitics,the DRC summary.The last figure shows the simulation waveform, which indicates the τ_{HL} and τ_{LH} and the 10ps clock skew rate.
In Figure 3, the area is calculated by multipling the length with width.

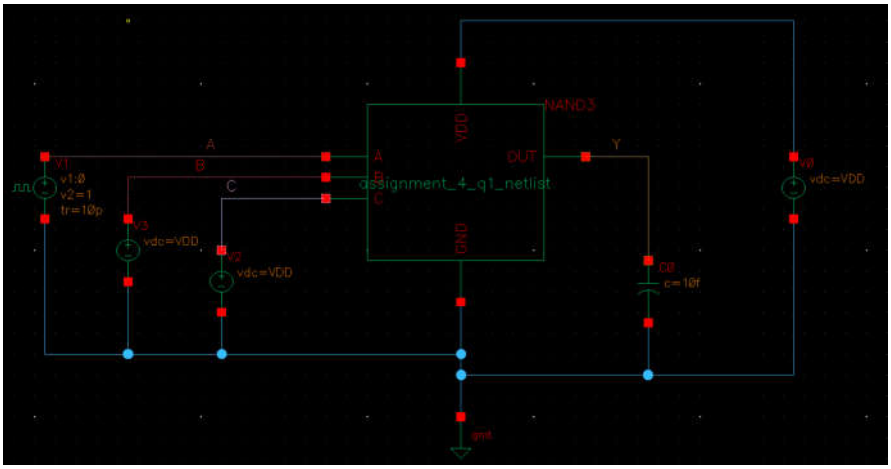

Figure 2: The testbench of the NAND3.

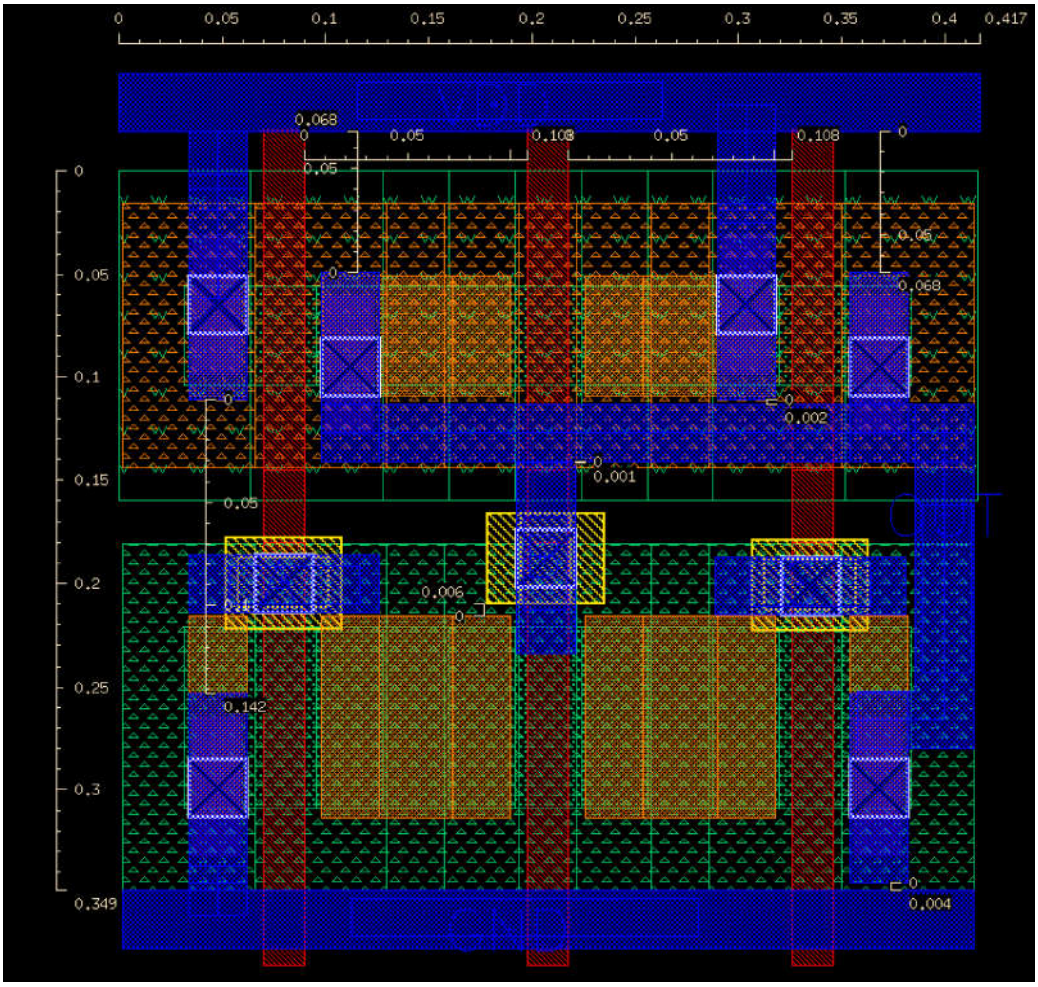

Figure 3: The layout of the NAND3.

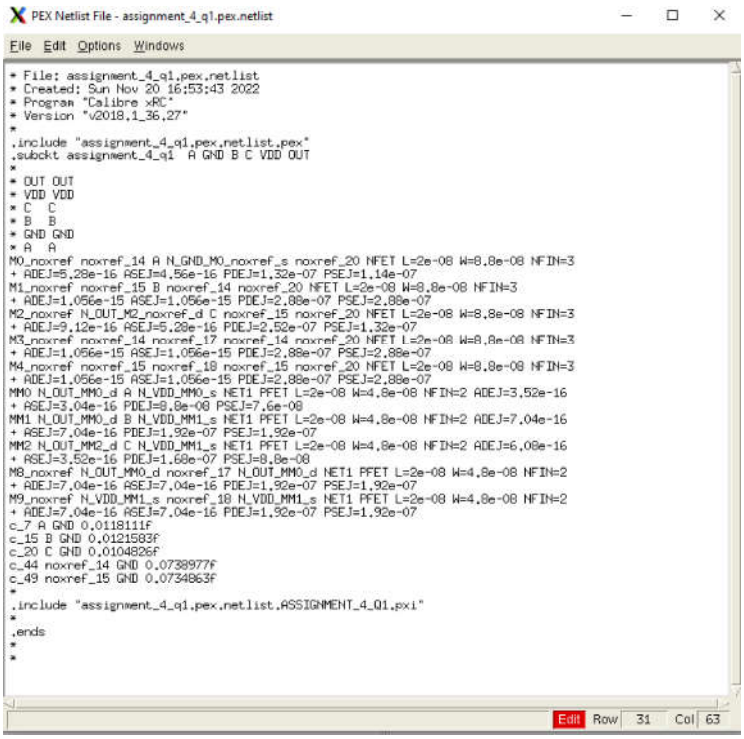

Figure 4: The netlist of the NAND3.

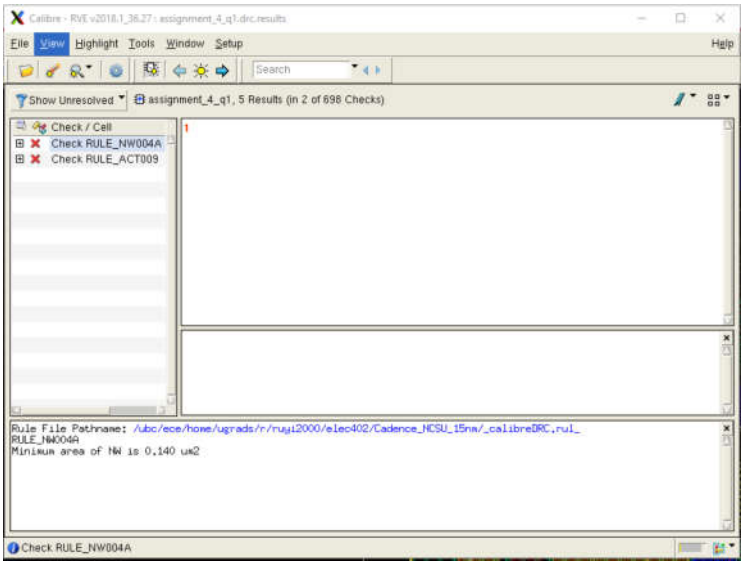

Figure 5: The part 1 of DRC report.

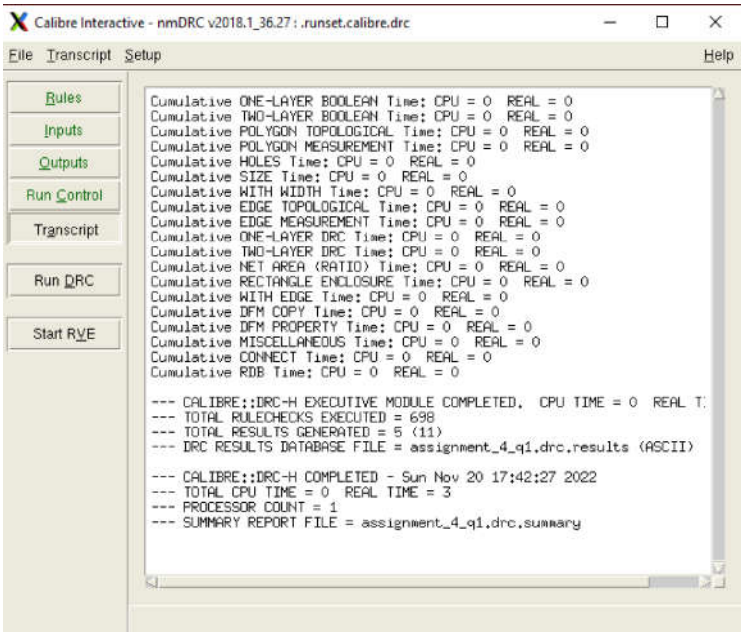

Figure 6: The part 2 of DRC report.

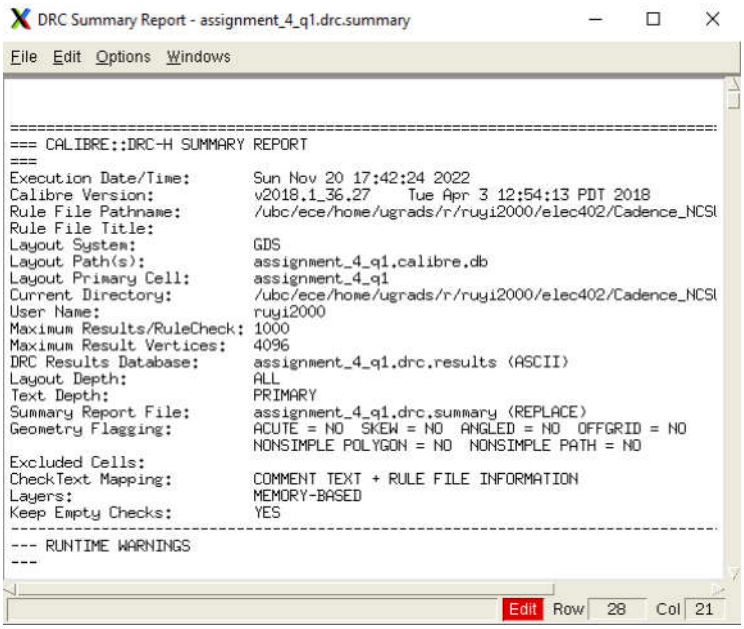

Figure 7: The part 3 of DRC report.

Figure 8: The waveform of the NAND3.