Assignment 4

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1 Question 1

The NAND3 is designed and make using Cadence. The specifications are shown below: The τ_{HL} is 26.5602ps. The τ_{LH} is 23.0161ps. The average delay is $\frac{26.5602+23.0161}{2}$ = 24.7882ps. The difference between τ_{HL} and τ_{LH} = 26.5602 - 23.0161 = 3.544ps < 5ps

$$\text{Area: } 0.145533\ \mu m^2$$
$$\text{Delay: } 24.7882\ \text{ps}$$
$$\text{Area} \times \text{Delay} = \boxed{3.6074 \mu m^2 \cdot ps}$$

The figure below shows the schematics:

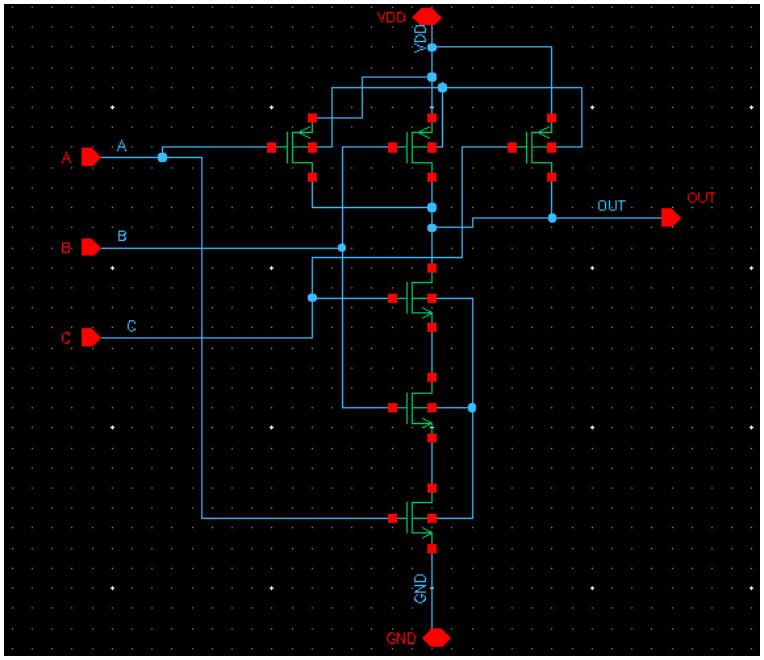

Figure 1: The schematics of the NAND3.

The figures below show the testbench with the ***load capacitor***,the layout with demensions,the netlist including all parasitics,the DRC summary.The last figure shows the simulation waveform, which indicates the τ_{HL} and τ_{LH} and the 10ps clock skew rate.
In Figure 3, the area is calculated by multipling the length with width.

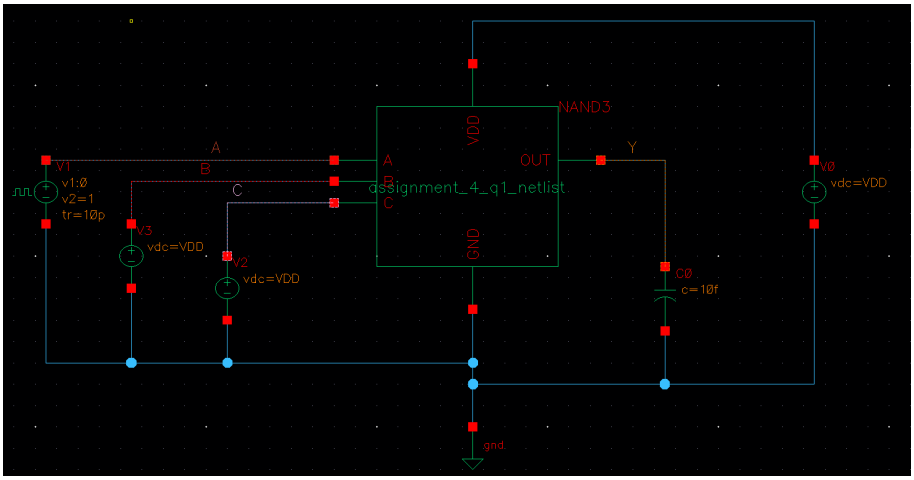

Figure 2: The testbench of the NAND3.

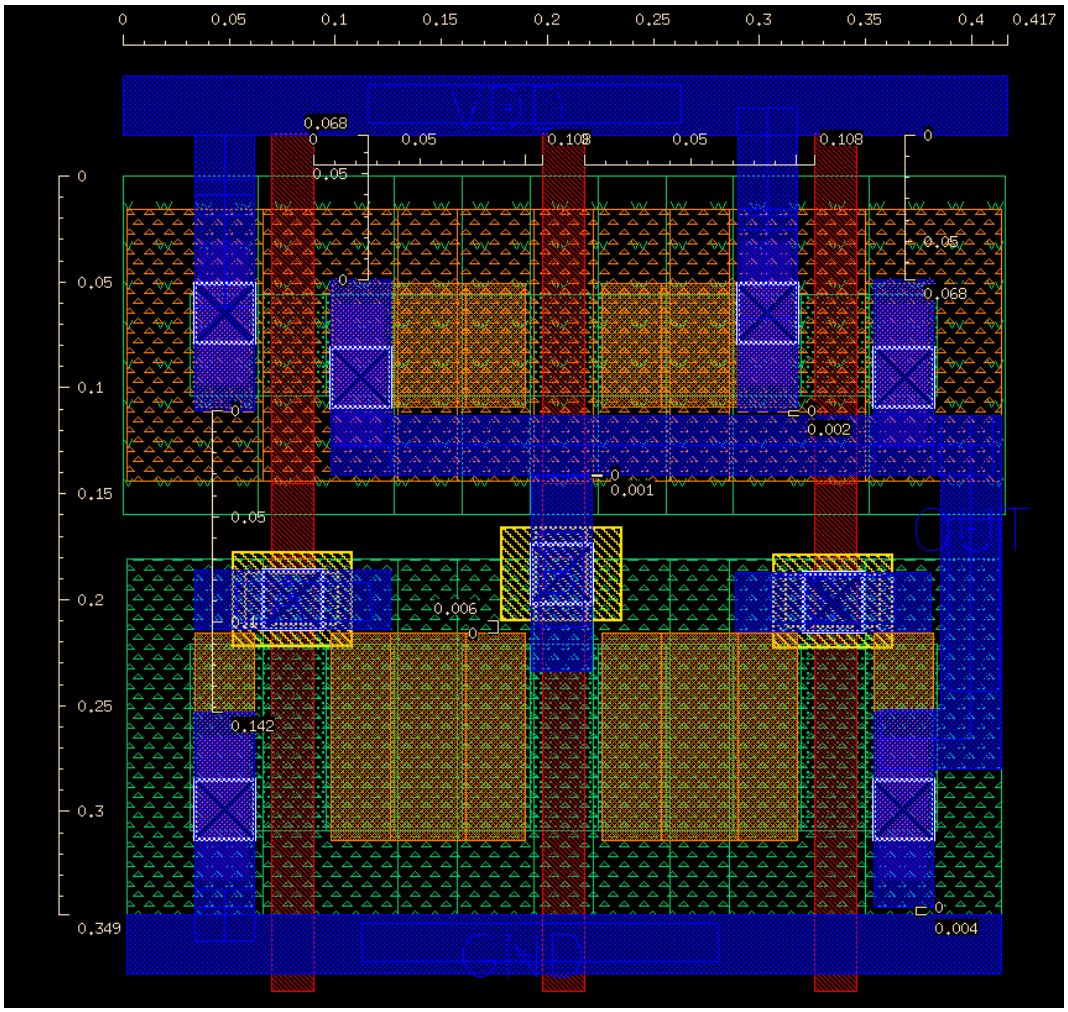

Figure 3: The layout of the NAND3.

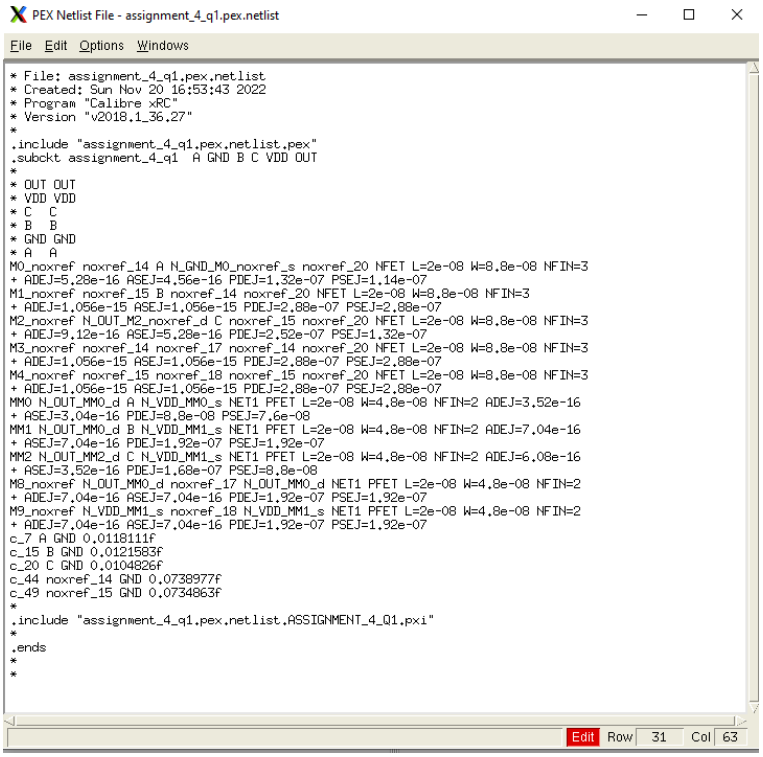

Figure 4: The netlist of the NAND3.

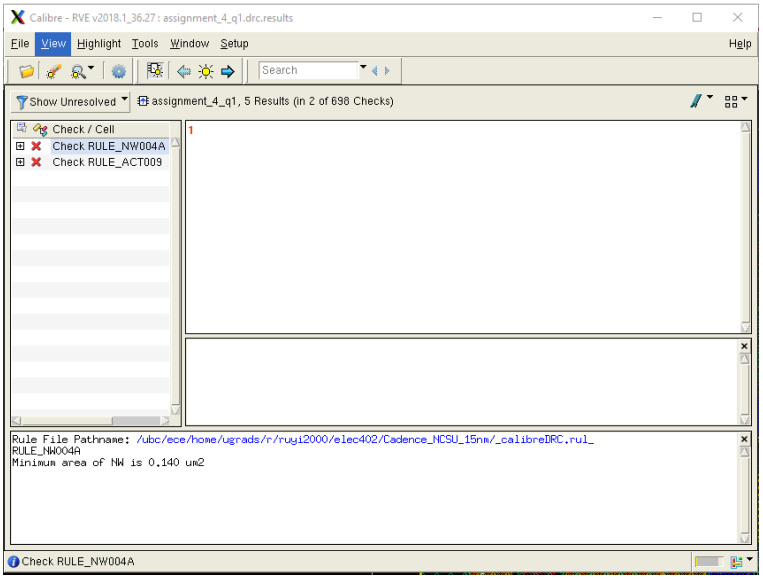

Figure 5: The part 1 of DRC report.

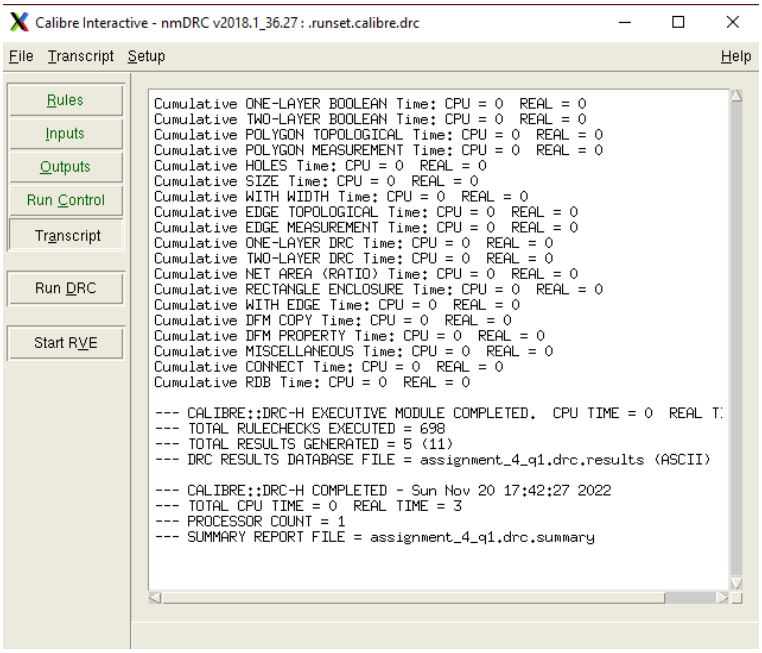

Figure 6: The part 2 of DRC report.

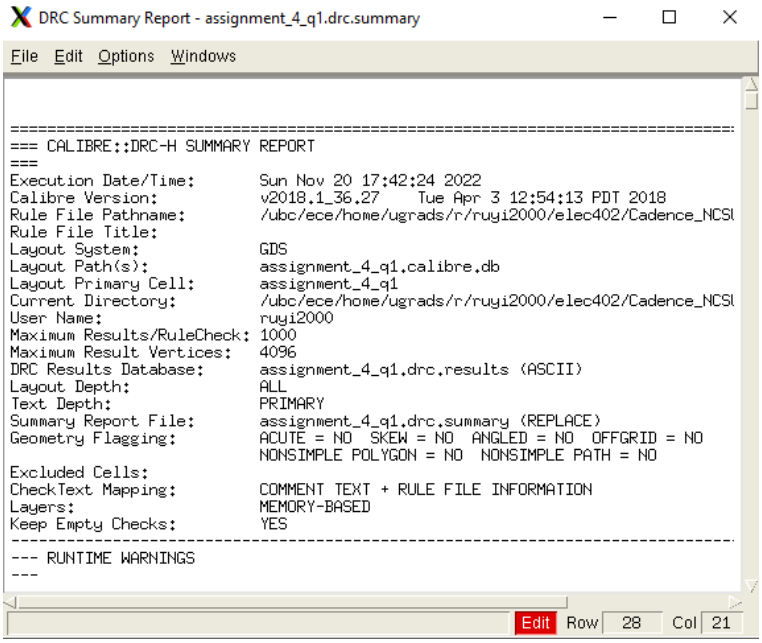

Figure 7: The part 3 of DRC report.

Figure 8: The waveform of the NAND3.

2 Question 2

The circuit is:

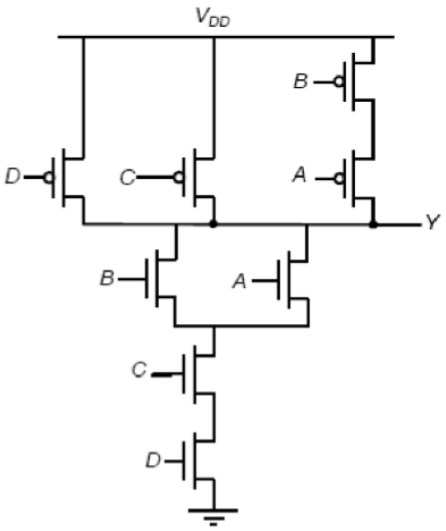

Figure 9: The circuit of question 2.

2.1 (a)

The pull-down logic function is $\overline{F} = \overline{Y} = (A + B) * CD$. The logic function of the circuit can be found by inverting the $\overline{F}$:

$$F = Y = \overline{\overline{Y}} = \overline{(A + B) * CD} = \overline{(A + B)} + \overline{CD} = \boxed{\overline{A} * \overline{B} + \overline{C} + \overline{D}}$$

2.2 (b)

As shown in Figure 1, in the ***Pull − Up*** circuit, either D, C will be ON or both A and B will be ON. When D or C is ON, each branch is has a single resistance of R. Thus, each D and C has a width of $\boxed{2W}$ or $\boxed{8\lambda}$. The other branch is A and B, the worst-case because this branch has two P-MOS in series. The resistance of A and B is $\frac{1}{2}R$. The width of A and B are doubled due to the series connection. Thus, the A and B has a width of $\boxed{4W}$ or $\boxed{16\lambda}$.

For the ***Pull − Down*** circuit, either A or B is ON and the C, D must be ON. The worst-case branch is either B-C-D or A-C-D. Since A and B are in parallel and each connects C,D in series, all A, B, C, D have the resistance of $\frac{1}{3}$R. Thus, the width of A, B, C, D are equal which is $\boxed{3W}$ or $\boxed{12\lambda}$.

2.3 (c)

Pull − Up

For the τ_{LH}, in the worst case, I kept as many nodes to be LOW. Therefore B and C are always HIGH (NMOS on and PMOS off) and A is always LOW (NMOS off and PMOS on). D is HIGH to connect the ground in pull-down circuit. Since the output is pulled up, D is from HIGH to LOW to drain the current from the VDD and disconnect the ground. Therefore, the worse-case input pattern for τ_{LH} is $\boxed{ABCD = 0111 \rightarrow ABCD = 0110}$

Pull − Down

For the τ_{HL}, in the worst case, I kept as many nodes to be charged (HIGH). Therefore, B and C are always HIGH (NMOS on and PMOS off) and A is always LOW (NMOS off and PMOS on) (The same as pull-up). D is LOW (enable in Pull-up circuit) to connect the VDD in pull-up circuit. Since the output is pulled down, D is from LOW to HIGH to disconnect the VDD and drain the current to ground. Therefore, the worse-case input pattern for τ_{LH} is $\boxed{ABCD = 0110 \rightarrow ABCD = 0111}$

Simulations

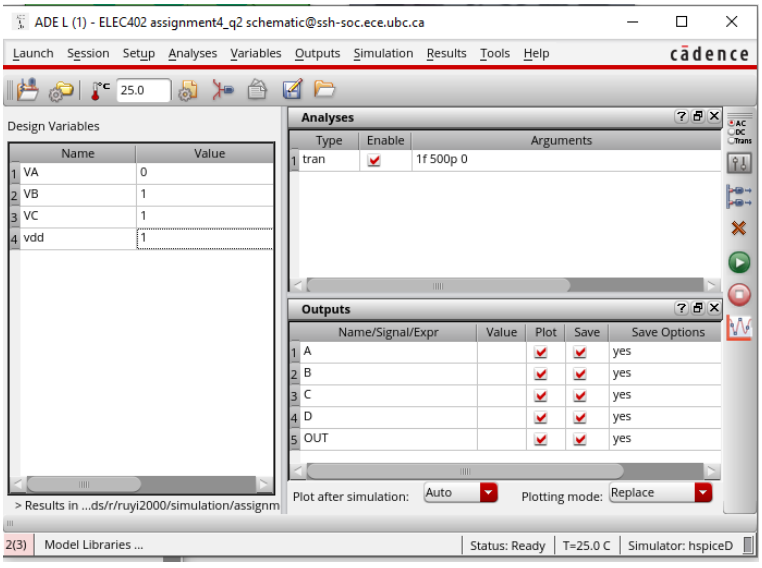

Figure 10: The parameters of the circuit.

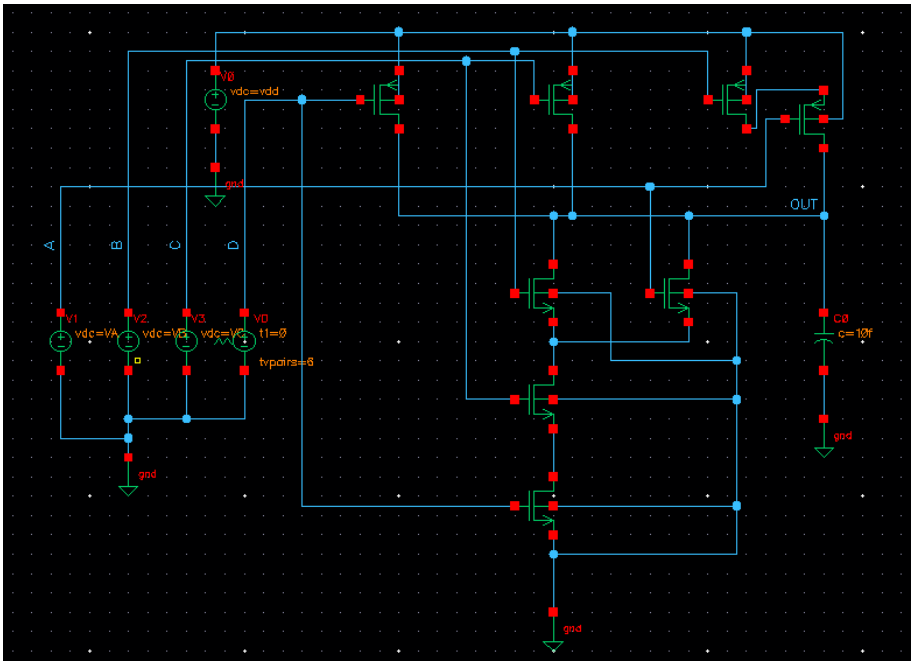

Figure 11: The schematics of the circuit.

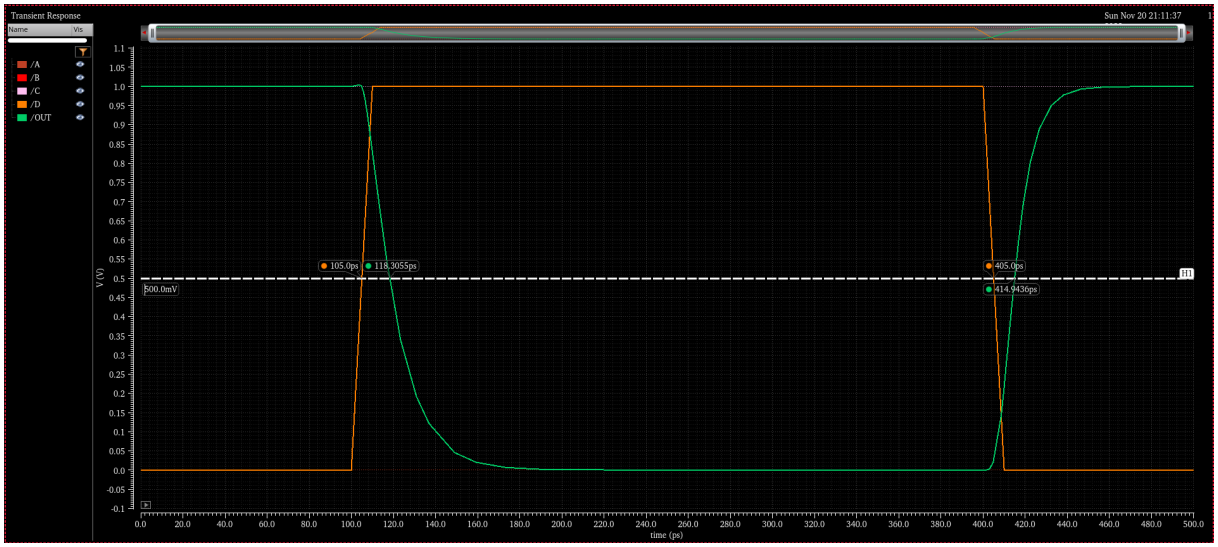

Figure 12: The waveform of the circuit.

Figure 12 shows the output waveform of switching D for pull-up and pull-down. The τ_{HL} = 118.3055 - 105 = 13.3055 ps. The τ_{LH} = 414.9436 - 405 = 9.9436 ps. The τ_{HL} *and* τ_{LH} are the highest value compared to other input patterns. Therefore, the speculated input patterns are the worst.

3 Question 3

3.1 (a)

Know that selB is $\overline{sel}$.
The top TG has a control signal *sel* to select $\bar{A}$. The bottom TG has a control signal $\overline{sel}$ to select $\bar{B}$. When *sel* is 1, branch A is selected. When $\overline{sel}$ is 1, branch B is selected. Thus,

$$C = (\overline{A} * sel) + (\overline{B} * \overline{sel})$$

$$OUT = \bar{C} = \overline{(\overline{A} * sel + \overline{B} * \overline{sel})} = \boxed{(A + \overline{sel}) * (B + sel)}$$

3.2 (b)

The equivalent Circuit:

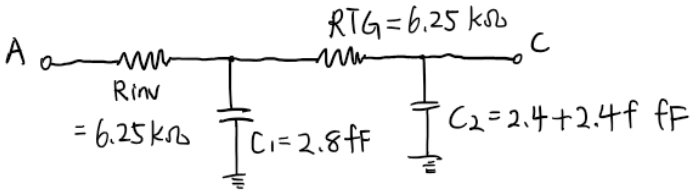

Figure 13: The equivalent circuit of the A-C path.

$$R_{inv} = R_{TG} = R_{eq} * \left(\frac{L}{W}\right) = 12.5k\Omega * \frac{2\lambda}{4\lambda} = \boxed{6.25k\Omega}$$

$$C_1 = C_{inv} + C_{TGin} = [C_{eff} * (4\lambda + 8\lambda)] + 2 * C_{eff} * 4\lambda + C_g * 4\lambda$$

$$C_1 = \frac{1fF}{um} * 12 * 0.1um + \frac{2fF}{um} * 4 * 0.1um + \frac{2fF}{um} * 4 * 0.1um = \boxed{2.8fF}$$

$$C_2 = C_{TGout} + C_{lg} + C_{TG}^{OFF} = [2 * C_{eff} * 4\lambda + C_g * 4\lambda] + f * C_g * (4\lambda + 8\lambda) + (2 * C_{eff} * 4\lambda)$$

$$C_2 = 2 * \frac{1fF}{um} * 4 * 0.1um + \frac{2fF}{um} * 4 * 0.1um + f * \frac{2fF}{um} * 12 * 0.1um + 2 * \frac{1fF}{um} * 4 * 0.1um = \boxed{(2.4 + 2.4f)fF}$$

3.3 (c)

Elmore delay is used to find the delay from A to C:

$$\tau = R_{inv} * C_1 + (R_{inv} + R_{TG}) * C2$$

$$\tau = R_{inv} * (C_{inv} + C_{TGin}^{ON}) + (R_{inv} + R_{TG}) * (C_{TGout}^{ON} + C_{lg} + C_{TG}^{OFF})$$

$$\tau = 6.25k\Omega * 2.8fF + (6.25k\Omega + 6.25k\Omega) * (2.4 + 2.4f)fF = \boxed{(47.5 + 30f)ps}$$

3.4 (d)

The equivalent circuit from A to OUT is:

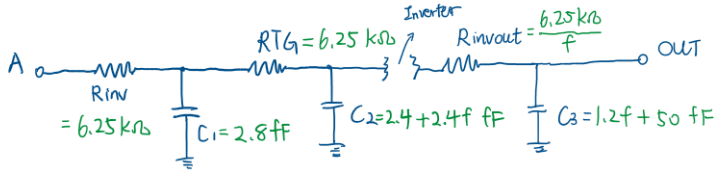

Figure 14: The equivalent circuit of the A-OUT path.

$$R_{invout} = \frac{R_{inv}}{f} = \frac{6.25k\Omega}{f}$$

$$C_3 = f * C_{eff} * (4\lambda + 8\lambda) + C_{load}$$

$$C_3 = f * \frac{1fF}{um} * 12 * 0.1um + 50fF = (1.2 * f + 50)fF$$

The τ_{out} can be calculated:

$$\tau_{out} = R_{invout} * C3 = \frac{6.25k\Omega}{f} * (1.2 * f + 50)fF = \boxed{7.5 + \frac{312.5}{f} ps}$$

Therefore, τ_{total} can be calculated:

$$\tau_{total} = R_{inv} * C1 + (R_{inv} + R_{TG}) * C2 + \tau_{out}$$

$$\tau_{total} = R_{inv} * (C_{inv} + C_{TGin}^{ON}) + (R_{inv} + R_{TG}) * (C_{TGout}^{ON} + C_{lg} + C_{TG}^{OFF}) + R_{invout} * (C_{inv} + C_{load})$$

$$\tau_{total} = 6.25k\Omega * 2.8fF + (12.5k\Omega * (2.4 + 2.4 * f)fF) + 7.5 + \frac{312.5}{f}$$

$$\tau_{total} = (55 + 30f + \frac{312.5}{f})ps$$

3.5 (e)

To minimize the τ_{total}, the term 30f + $\frac{312.5}{f}$ is minimized. The minimum f is calculated using derivative:

$$Derivative\ of\ the\ term = 30 + (\frac{-312.5}{f^2}) = 0$$

$$\boxed{f \Rightarrow 3.2275}$$

As shown in the calculation, the value of f which minimizes the delay is about 3.2275. If the f is an integer (manufactured by Finfet), it is 3.