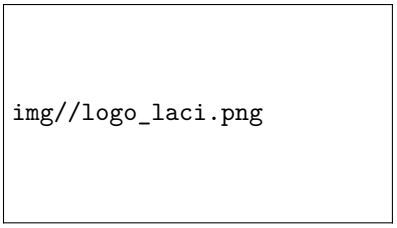

Introduction to Logic Design
EEF205E

Homework 4

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Part 1

1. ABCD TO 7-SEGMENT DISPLAY Decoder Design With Minimum Number of Gates

   Solution:

   (a) Finding the truth table of the 7-segment display:

   The truth table of the 7-segment display is as follows:

7 segment	A	B	C	D	a	b	c	d	e	f	g
	0	0	0	0	1	1	1	1	1	1	0
	0	0	0	1	0	1	1	0	0	0	0
	0	0	1	0	1	1	0	1	1	0	1
	0	0	1	1	1	1	1	1	0	0	1
	0	1	0	0	0	1	1	0	0	1	1
	0	1	0	1	1	0	1	1	0	1	1
	0	1	1	0	1	0	1	1	1	1	1
	0	1	1	1	1	1	1	0	0	0	0
	1	0	0	0	1	1	1	1	1	1	1
	1	0	0	1	1	1	1	1	0	1	1

Table 1: 7-Segment Display Truth Table for BCD Inputs

The remaining 6 rows are not shown in the table since they are not used in the BCD representation. They will be placed as "don't care" in the Karnaugh map.

(b) Constructing the Karnaugh map for each segment:

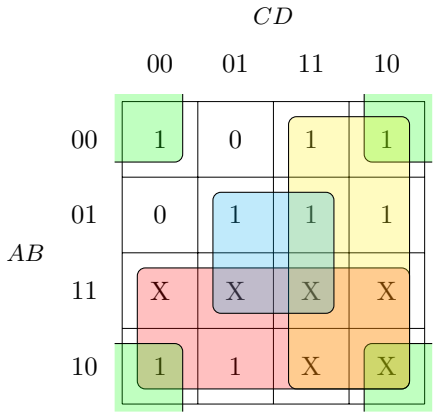

Figure 1: Kmap for a output

The optimized expression for a is: $B'D' + BD + C + A$

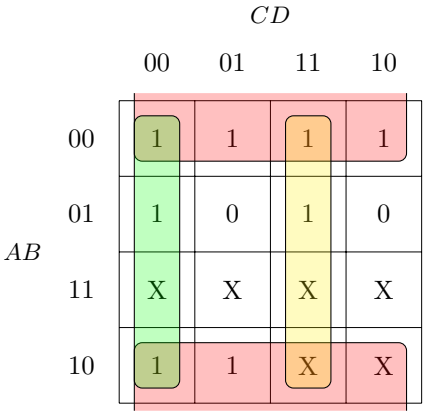

Figure 2: Kmap for b output

The optimized expression for b is: $B' + C'D' + CD$

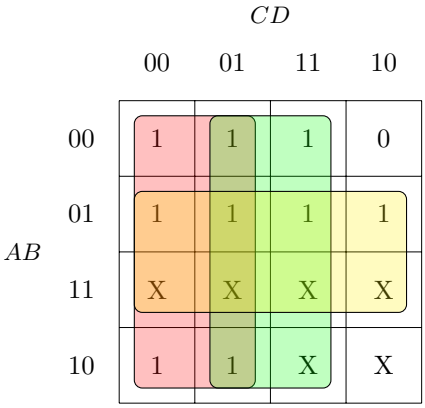

Figure 3: Kmap for c output

The optimized expression for c is: $C' + B + D$

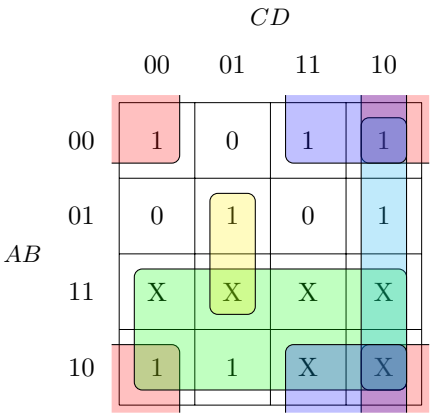

Figure 4: Kmap for d output

The optimized expression for d is: $B'D' + B'C + BC'D + CD' + A$

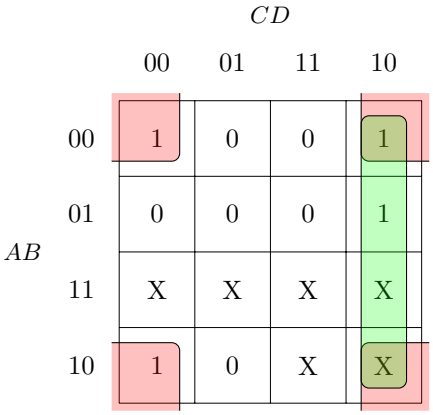

Figure 5: Kmap for e output

The optimized expression for e is: $B'D' + CD'$

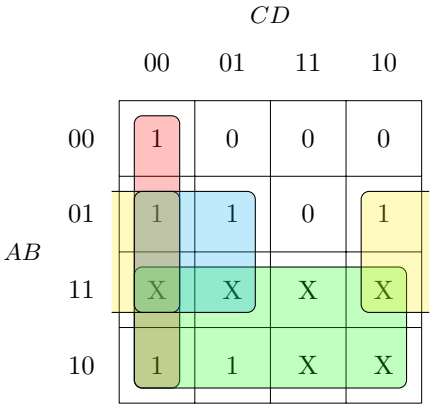

Figure 6: Kmap for f output

The optimized expression for f is: $A + BC' + BD' + C'D'$

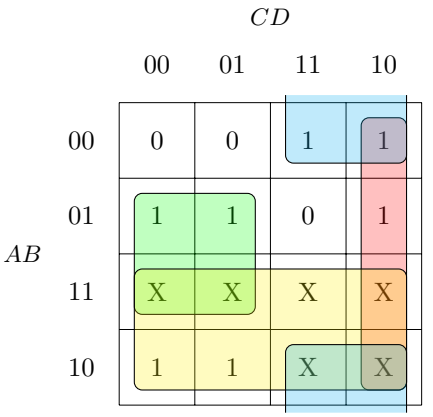

Figure 7: Kmap for g output

The optimized expression for g is: $A + BC' + B'C + CD'$

(c) Design a four-bit combinational circuit 2's complementor. (The output generates the 2's complement of the input binary number.) Show that the circuit can be constructed with exclusive-OR gates. Can you predict what the output functions are for a five-bit 2's complementor?

Solution:

Taking the 2's complement of a binary number is equivalent to inverting all the bits and adding 1 to the result. The circuit can be constructed with exclusive-OR gates as follows:

Input					Output (2's Complement)				
a	b	c	d	Binary	x	y	z	t	Binary
0	0	0	0	0000	0	0	0	0	0000
0	0	0	1	0001	1	1	1	1	1111
0	0	1	0	0010	1	1	1	0	1110
0	0	1	1	0011	1	1	0	1	1101
0	1	0	0	0100	1	1	0	0	1100
0	1	0	1	0101	1	0	1	1	1011
0	1	1	0	0110	1	0	1	0	1010
0	1	1	1	0111	1	0	0	1	1001
1	0	0	0	1000	1	0	0	0	1000
1	0	0	1	1001	0	1	1	1	0111
1	0	1	0	1010	0	1	1	0	0110
1	0	1	1	1011	0	1	0	1	0101
1	1	0	0	1100	0	1	0	0	0100
1	1	0	1	1101	0	0	1	1	0011
1	1	1	0	1110	0	0	1	0	0010
1	1	1	1	1111	0	0	0	1	0001

Table 2: 4-bit 2's Complement Truth Table

Generating KMamps for each output bit:

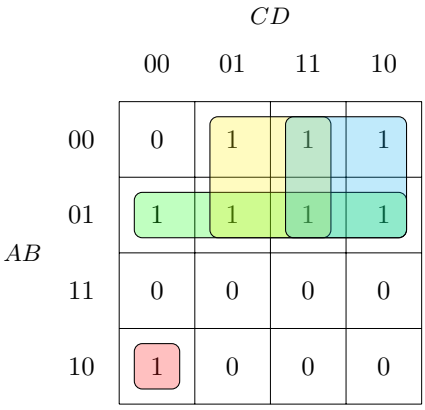

Figure 8: Kmap for x output

The equation for x is: $a'b+a'd+a'c+ab'c'd'$ for converting this to XOR gates, we can use the following equation:

$$x = a'b + a'd + a'c + ab'c'd' \tag{1}$$
$$x = a'\left(b + c + d\right) + ab'c'd' \tag{2}$$
$$x = a'\left(b + d + c\right) + a\left(b + c + d\right)' \tag{3}$$
$$x = a \oplus \left(b + c + d\right) \tag{4}$$

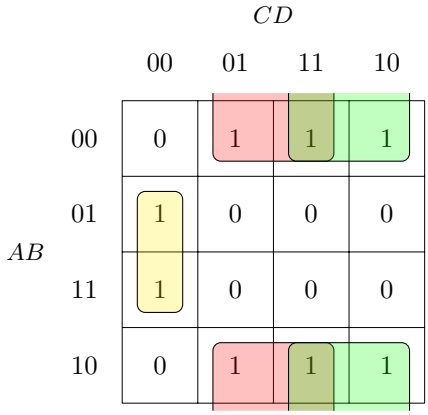

Figure 9: Kmap for y output

The equation for y is $bc'd' + b'd + b'c$ for converting this to XOR gates, we can use the following equation:

$$y = bc'd' + b'd + b'c \tag{5}$$
$$y = b\,(c'd' + d + c) \tag{6}$$
$$y = b \oplus (c + d) \tag{7}$$

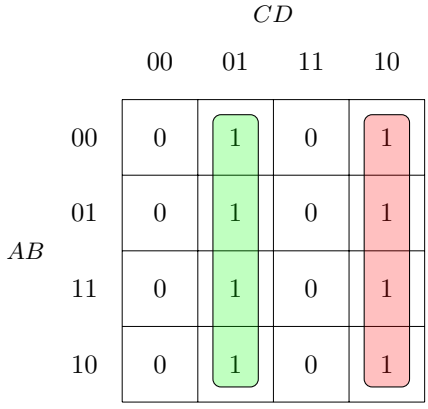

Figure 10: Kmap for z output

The equation for z is $c'd + cd'$ for converting this to XOR gates, we can use the following equation:

$$z = c'd + cd' \tag{8}$$
$$z = c \oplus d \tag{9}$$

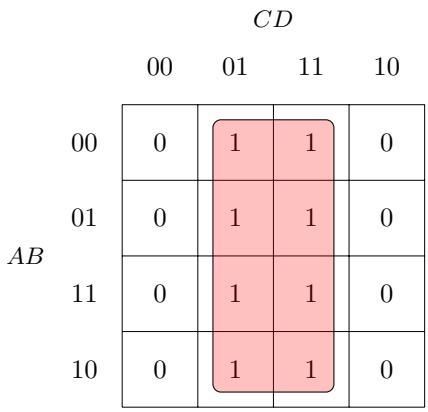

Figure 11: Kmap for t output

The equation for t is d .

The final conversion functions are:

$$x = a \oplus (b + c + d) \tag{10}$$
$$y = b \oplus (c + d) \tag{11}$$
$$z = c \oplus d \tag{12}$$
$$t = d \tag{13}$$

We can expect that for a 5 bit 2's complementor the inputs are A_4, A_3, A_2, A_1, A_0 and the outputs are X_4, X_3, X_2, X_1, X_0. The equations for the outputs can be derived by following the same steps as above. The final equations will be:

$$X_4 = A_4 \oplus (A_3 + A_2 + A_1 + A_0) \tag{14}$$
$$X_3 = A_3 \oplus (A_2 + A_1 + A_0) \tag{15}$$
$$X_2 = A_2 \oplus (A_1 + A_0) \tag{16}$$
$$X_1 = A_1 \oplus A_0 \tag{17}$$
$$X_0 = A_0 \tag{18}$$