Introduction to Logic Design
EEF205E

Homework 5

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Question 1

Recalling the JK flip-flop equations we can derive $A(t+1)$ and $B(t+1)$ as follows:

$$Q(t+1) = J \cdot \overline{Q} + \overline{K} \cdot Q \tag{1}$$

For the A flip-flop: $J_A = x$ and $K_A = b$

$$A(t+1) = x \cdot \overline{A} + \overline{b} \cdot A \tag{2}$$

For the B flip-flop: $J_B = x$ and $K_B = \overline{a}$

$$B(t+1) = x \cdot \overline{B} + a \cdot B \tag{3}$$

Given that there are 2 flip-flops there are $2^2 = 4$ states and we can write the state transition table as follows:

Table 1: State Transition Table

Present State			Next State	
A	B	x	A(t+1)	B(t+1)
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	1

We can draw the state diagram as follows:

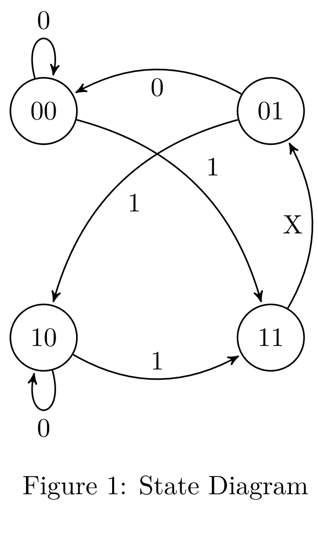

Figure 1: State Diagram

Question 2

The logic diagram for the state machine can be drawn as follows:

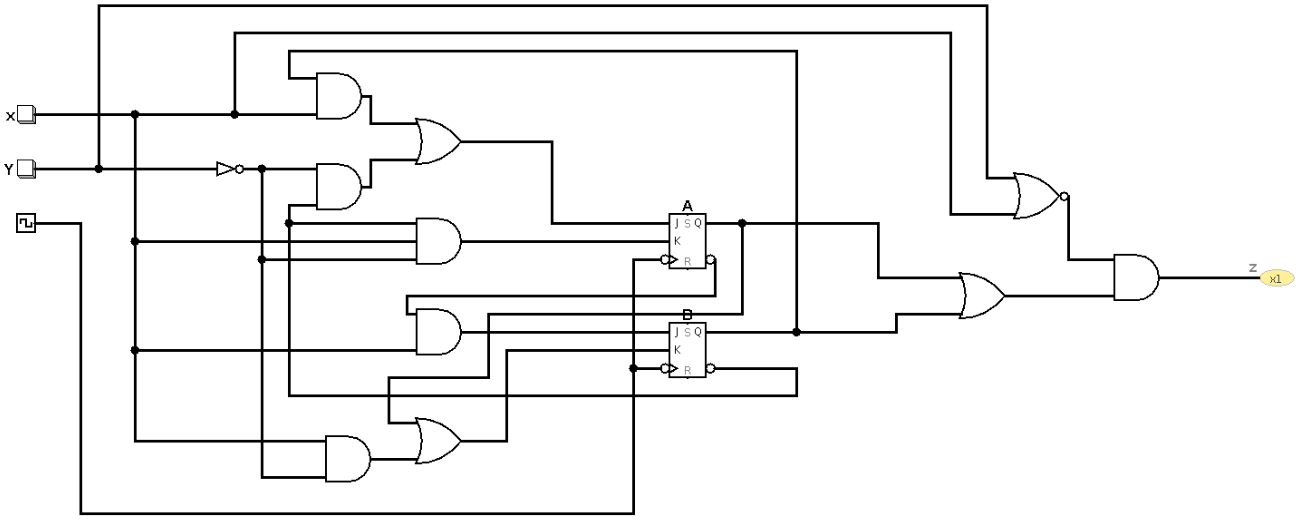

Figure 2: Logic Diagram for the State Machine

The state table can be written as follows:

Figure 3: State Table

Present State				Next State		
A	**B**	**x**	**y**	**A***	**B***	**z**
0	0	0	0	1	0	0
0	0	0	1	0	0	0
0	0	1	0	1	1	0
0	0	1	1	0	1	0
0	1	0	0	0	1	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	1	0
1	0	0	0	1	0	1
1	0	0	1	1	0	0
1	0	1	0	0	0	0
1	0	1	1	1	0	0
1	1	0	0	1	0	1
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

Recalling the JK flip-flop equations we can derive $A(t+1)$ and $B(t+1)$ as follows:

$$Q(t+1) = J \cdot \overline{Q} + \overline{K} \cdot Q \tag{4}$$

For the A flip-flop:

$$A^* = (b \cdot x + b' \cdot y') \cdot A' + (b + x' + y) \cdot A \tag{5}$$

$$B^* = (a' \cdot x) \cdot B' + [a' \cdot (x' + y)] \cdot B \tag{6}$$

1 Question 3

Part A

The state table for the requested circuit can be written as follows:

Table 2: State Table

Present State			Next State	
A	B	x	A(t+1)	B(t+1)
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

To design the circuit with D Flip Flops We need its excitation table:

Table 3: D Flip-Flop Excitation Table

Present State	Next State	D Input
0	0	0
0	1	1
1	0	0
1	1	1

It can be seen that the equation for the D flip-flop is $D = Q(t+1)$ so we can take the next state values from the state table and write the D values as follows:

Table 4: State Table

Present State			Next State		D Inputs	
A	B	x	A(t+1)	B(t+1)	D_A	D_B
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	1	1	1	1
1	0	0	1	0	1	0
1	0	1	0	0	0	0
1	1	0	1	1	1	1
1	1	1	1	0	1	0

We can find equations for D_A and D_B with the help of kmaps:

AB \ x	0	1
00	0	0
01	0	1
11	1	1
10	1	0

Figure 4: K-Map for D_A

The simplified equation for D_A is:

$$D_A = (\overline{x_{in}} \cdot A) + (x_{in} \cdot B) \tag{7}$$

We can draw the K-Map for D_B as follows:

AB \ x	0	1
00	0	1
01	1	1
11	1	0
10	0	0

Figure 5: K-Map for D_B

The simplified equation for D_B is:

$$D_B = (\overline{x_{in}} \cdot B) + (x_{in} \cdot \overline{A}) \tag{8}$$

All of the equations can be implemented in a circuit as follows:

$$D_A = (\overline{x_{in}} \cdot A) + (x_{in} \cdot B) \tag{9}$$

$$D_B = (\overline{x_{in}} \cdot B) + (x_{in} \cdot \overline{A}) \tag{10}$$

Part B

The state table for the requested circuit can be written as follows:

Table 5: State Table

Present State			Next State	
A	B	x	A(t+1)	B(t+1)
0	0	0	0	0
0	0	1	1	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	0	1

Again using the principle of D flip-flops we can add the D inputs to the state table as follows:

Table 6: State Table

Present State			Next State		D Inputs	
A	B	x	A(t+1)	B(t+1)	D_A	D_B
0	0	0	0	0	0	0
0	0	1	1	1	1	1
0	1	0	0	1	0	1
0	1	1	1	0	1	0
1	0	0	1	0	1	0
1	0	1	0	0	0	0
1	1	0	1	1	1	1
1	1	1	0	1	0	1

We can find equations for D_A and D_B with the help of kmaps:

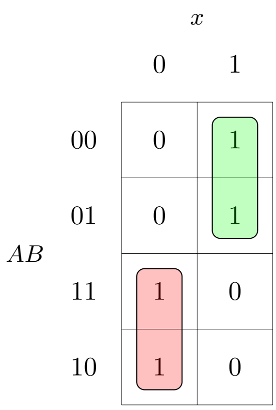

Figure 6: K-Map for D_A

The simplified equation for D_A is:

$$D_A = (\overline{x_{in}} \cdot A) + (x_{in} \cdot \overline{A}) \tag{11}$$

This shows an XOR gate is needed for the implementation of D_A.

$$D_A = x_{in} \oplus A \tag{12}$$

We can draw the K-Map for D_B as follows:

AB \ x	0	1
00	0	1
01	1	0
11	1	1
10	0	0

Figure 7: K-Map for D_B

The simplified equation for D_B is:

$$D_B = (\overline{x_{in}} \cdot B) + (x_{in} \cdot \overline{B} \cdot \overline{A}) + (x_{in} \cdot A \cdot B) \tag{13}$$

Also it can be simplified with XNOR gates as follows:

$$D_B = (\overline{x_{in}} \cdot B) + (x_{in} \cdot (A \odot B)) \tag{14}$$

So the circuit can be implemented as follows:

$$D_A = x_{in} \oplus A \tag{15}$$

$$D_B = (\overline{x_{in}} \cdot B) + (x_{in} \cdot (A \odot B)) \tag{16}$$

Question 4

For a serial 2s complementer, the circuit can be implemented as follows:
S_0 : We have not seen a 1 yet copy the input to the output

S_1 : We have seen a 1, invert the output.

This is for LSB sent first approach.

The finite state machine can be implemented as follows:

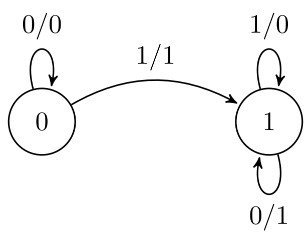

Figure 8: State Diagram

The state table can be written as follows:

Table 7: State Table

Present State		Next State	
Q	x	Q(t+1)	y
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	0

We are using D latch for this implementation. The D input can be written as follows:

It can be seen from the table that the D input it:

$$D = Q + x \tag{17}$$

And it can be seen that the y is the xor of the Q and x:

$$y = Q \oplus x \tag{18}$$

The circuit can be implemented as follows:

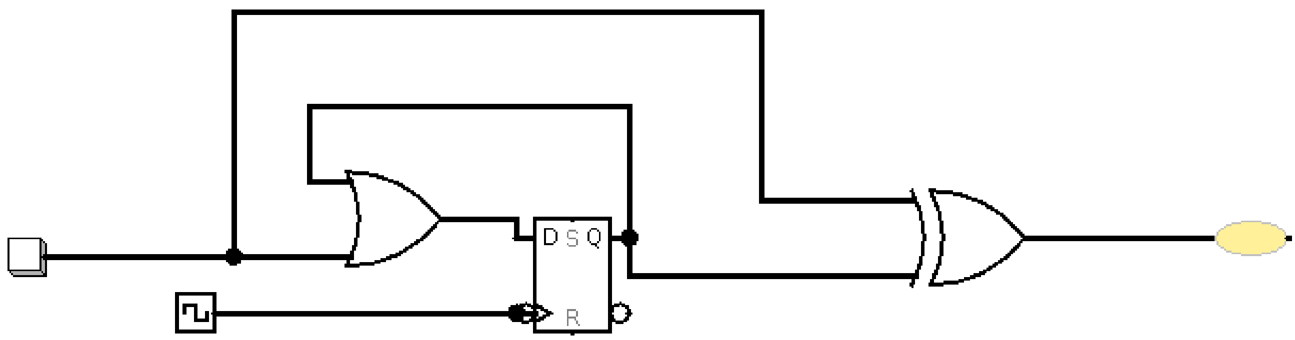

Figure 9: Logic Diagram for the State Machine

Question 5

The requested state transition table is given in Table 8.

Table 8: State Transition Table for Sequential Circuit

Current State		Inputs		Next State	
A	B	E	F	A*	B*
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	0
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	0	0

The state machine diagram can be drawn as follows:

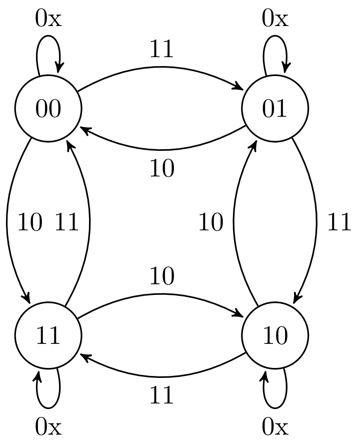

Figure 10: State Diagram

The E signal allows signal to change if its 0 F signal does not matter and the state does not change.

F = 1 counts up the state and F = 0 counts down the state.

The JK flip-flop equations can be written as follows:

$$Q(t+1) = J \cdot \overline{Q} + \overline{K} \cdot Q \tag{19}$$

And the excitation table for the JK flip-flop can be written as follows:

Table 9: JK Flip-Flop Excitation Table

Present State	Next State	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

We can add 4 columns for J_A, J_B, K_A, K_B

Table 10: State Transition Table for Sequential Circuit

Current State		Inputs		Next State		FF Inputs			
A	B	E	F	A*	B*	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	0	1	0	0	0	X	0	X
0	0	1	0	1	1	1	X	1	X
0	0	1	1	0	1	0	X	1	X
0	1	0	0	0	1	0	X	X	0
0	1	0	1	0	1	0	X	X	0
0	1	1	0	0	0	0	X	X	1
0	1	1	1	1	0	1	X	X	1
1	0	0	0	1	0	X	0	0	X
1	0	0	1	1	0	X	0	0	X
1	0	1	0	0	1	X	1	1	X
1	0	1	1	1	1	X	0	1	X
1	1	0	0	1	1	X	0	X	0
1	1	0	1	1	1	X	0	X	0
1	1	1	0	1	0	X	0	X	1
1	1	1	1	0	0	X	1	X	1

For finding the equations we can use kmaps:

AB \ EF	00	01	11	10
00	0	0	0	1
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

Figure 11: K-map for J_A

AB \ EF	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	1	0
10	0	0	0	1

Figure 12: K-map for K_A

AB \ EF	00	01	11	10
00	0	0	1	1
01	X	X	X	X
11	X	X	X	X
10	0	0	1	1

Figure 13: K-map for J__B

AB \ EF	00	01	11	10
00	X	X	X	X
01	0	0	1	1
11	0	0	1	1
10	X	X	X	X

Figure 14: K-map for K__B

The final equations for the flip flops can be obtained from kmaps as follows:

$$J_A = A'B \cdot (BF + B'F') \tag{20}$$

$$K_A = AE \cdot (BF + B'F') \tag{21}$$

$$J_B = E \tag{22}$$

$$K_B = E \tag{23}$$