Unified Instruction Format for Custom Microprocessor

1. Unified 32-bit Instruction Format

```
All instructions follow a consistent structure for simplified decoding:

[31:28] cond     - 4-bit condition code
[27:23] opcode   - 5-bit opcode
[22:19] Rn       - 4-bit source register 1
[18:15] Rm       - 4-bit source register 2 or base register
[14:11] Rd       - 4-bit destination register
[10:0]  imm      - 11-bit immediate / shift / offset field

Shift-related fields (when applicable):
  [10:9]  shift_type - 2 bits (00=LSL, 01=LSR, 10=ASR, 11=ROR)
  [8:4]   shift_amt  - 5-bit shift amount
  [3:0]   unused     - reserved (set to 0)
```

2. Data Processing (Register-to-Register)

```
- Uses Rn, Rm, Rd directly
- Uses shift_type and shift_amt from imm[10:4]

Opcodes (5-bit):
ADD  00000 | SUB  00001 | MUL  00010 | DIV  00011
MOD  00100 | AND  00101 | ORR  00110 | XOR  00111
BIC  01000 | MVN  01001 | CMP  01010 | TST  01011
```

3. Immediate Instructions

```
- Rn and Rd are used normally
- Immediate value in imm[10:0]

Opcodes (5-bit):
MVI   01100 | ADDI  01101 | SUBI  01110
ANDI  01111 | ORI   10000 | XORI  10001
```

4. Load/Store Instructions

```
- Rn: base address register
- Rd: source (STR) or destination (LDR)
- imm[10:0]: unsigned offset

Opcodes (5-bit):
LDR 10010 | STR 10011
```

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5. Branch Instructions

- Branch target offset in imm[10:0] (signed)
- Rn, Rm, Rd ignored

Opcodes (5-bit):

B   10100 | BEQ 10101 | BNE 10110

BLT 10111 | BGT 11000