Non-synchronous Boost Converter Calculations

Component Parameters (From SMPS Datasheet)

Switching FET On Resistance

$R_{DS\_ON} := 500\ \text{m}\Omega$

Feedback Voltage

$V_{FB} := 1.23\ \text{V}$

Switching Frequency

$f_{SW} := 1.6\ \text{MHz}$

Diode forward voltage

$V_{DIODE} := 0.5\ \text{V}$

Design Parameters

Input Voltage

$V_{IN} := 5\ \text{V}$

Output Current

$I_{OUT} := 200\ \text{mA}$

Estimated Average Switching Current

$I_{SW\_AVG} := 0.5\ \text{A}$

Top Feedback Resistor

$R_{FB\_T} := 115\ \text{k}\Omega$

Bottom Feedback Resistor

$R_{FB\_B} := 13.3\ \text{k}\Omega$

Inductor Value

$L := 10\ \mu\text{H}$

Inductor Self-Resonant Frequency

$SRF := 41\ \text{MHz}$

Calculated Parameters

FET Drain-Source Voltage Drop

$$V_{SW} := R_{DS\_ON} \cdot I_{SW\_AVG} = 0.25\ \text{V}$$

Output Voltage

$$V_{OUT} := V_{FB} \cdot \frac{R_{FB\_T} + R_{FB\_B}}{R_{FB\_B}} = 11.8653\ \text{V}$$

Duty Cycle

$$DC := \frac{V_{OUT} + V_{DIODE} - V_{IN}}{V_{OUT} + V_{DIODE} - V_{SW}} = 60.7935\ \%$$

Average Inductor Current

$$I_{IND\_AVG} := \frac{I_{OUT}}{1 - DC} = 0.5101\ \text{A}$$

Inductor Ripple Current

$$I_{RIPPLE} := DC \cdot \frac{V_{IN} - V_{SW}}{f_{SW} \cdot L} = 0.1805\ \text{A}$$

Inductor Switching Current

$$I_{SW} := I_{IND\_AVG} + \frac{I_{RIPPLE}}{2} = 0.6004\ \text{A}$$

Parasitic Capacitance of Inductor

$$C_{PARASITIC} := \frac{1}{\left(2 \cdot \pi \cdot SRF\right)^2 \cdot L} = 1.5069\ \text{pF}$$

Output Filter Design

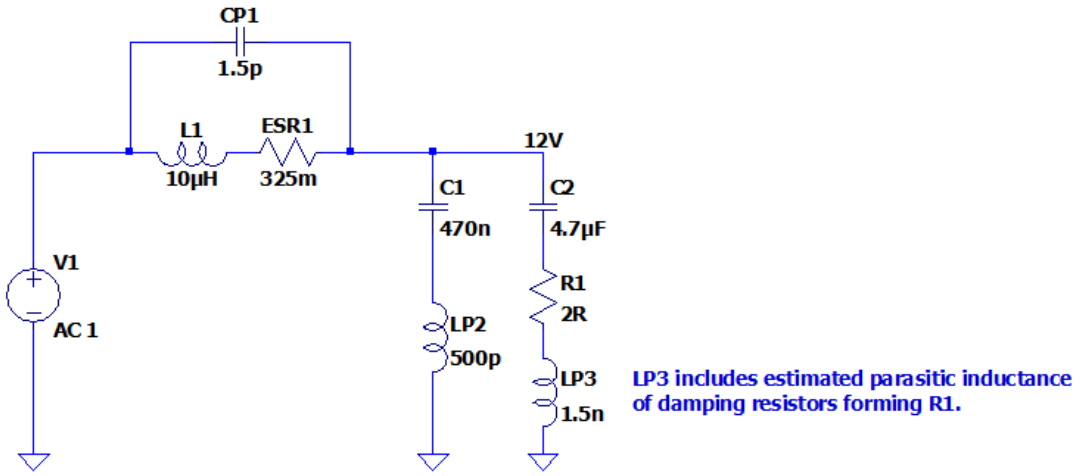
The design criteria for the output filter is to attenuate frequencies between the switching frequency and knee frequency of the converter. A worst case 10ns rise time of the FET is assumed. This should be confirmed upon prototyping as it is not stated in the datasheet.

Rise/fall time of FET

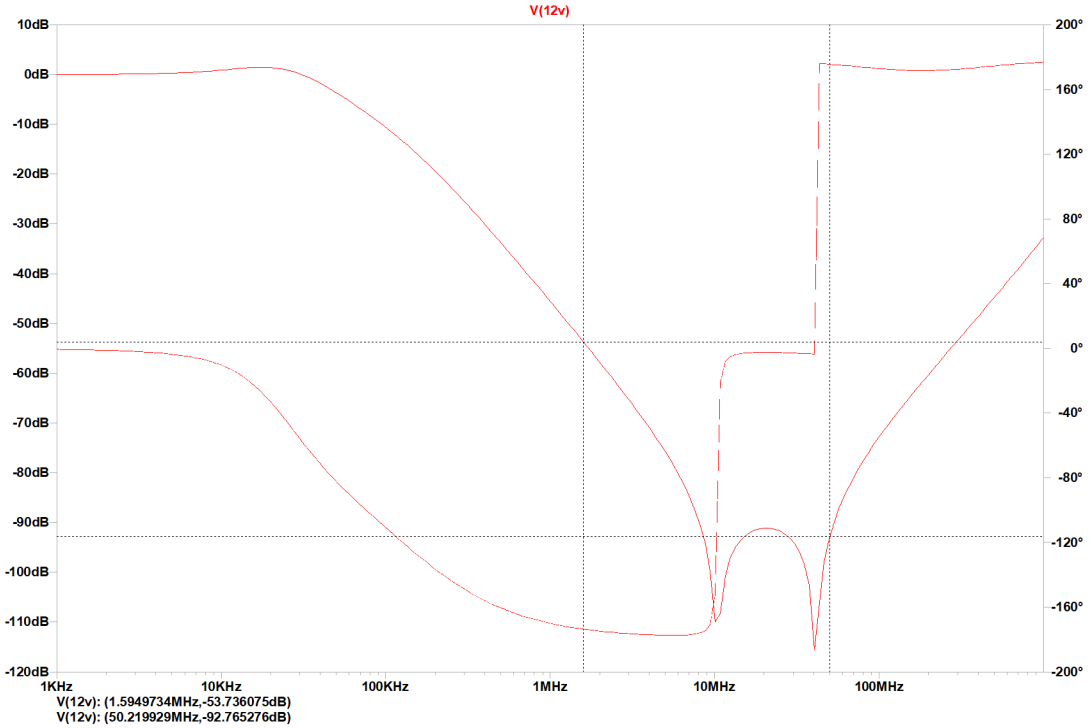
$t_r := 10\ \text{ns}$

Knee frequency of SMPS

$f_{knee} := \frac{0.5}{t_r} = 50\ \text{MHz}$



.ac oct 10 1K 1G



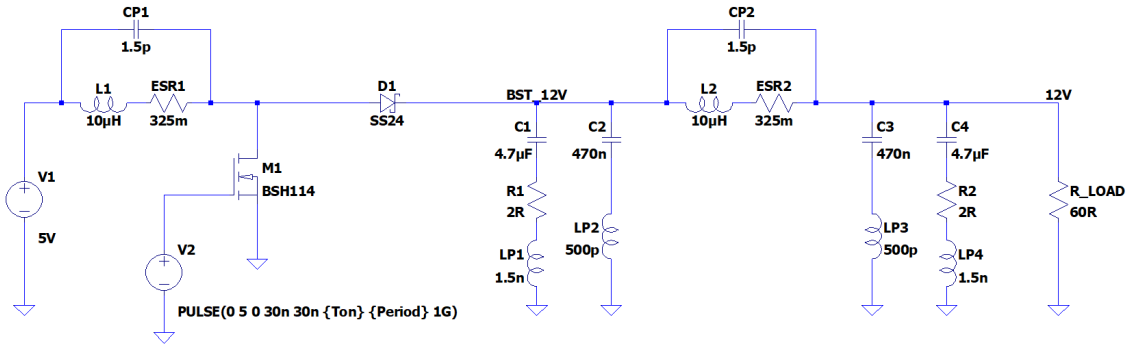
As shown in the graph, the attenuation at 1.6MHz is ~54dB with good attenuation up to the knee frequency of 50MHz. The selected output filter should be suitable for the SMPS.

Transient Analysis

A transient analysis was performed to check the circuit performs as expected. The fixed duty cycle calculated in the SMPS calcs. This simulation does not include the control loop of the SMPS. It is assumed to be stable as the loop compensation recommendations in the datasheet have been followed.

Parameters found by simulation:
Avg Inductor Current (L1): 570mA
Peak Inductor Current (L1): 650mA
Output Ripple Voltage: 250µA
Avg Power of ESR2: 2.3mW

The inductor current was found to be slightly higher during the simulation, this is mostly due to the inclusion of ESR in the simulated inductor. Otherwise, the calculated duty cycle matched the simulation results, a 60.79% duty cycle resulted in an output voltage (BST_12V) of 11.86V. As shown in the graph, the output filter is effective at attenuating the switching noise.

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.tran 2m
.param Fsw=1.6Meg
.param DC=0.6079

.param Period=1/Fsw
.param Ton=Period*DC
```

NOTES:
1. BSH114 has similar on-resistance to the internal FET in the LM27313 IC.
2. Rise time of V2 has been tuned to achieve a 10ns rise time of M1.