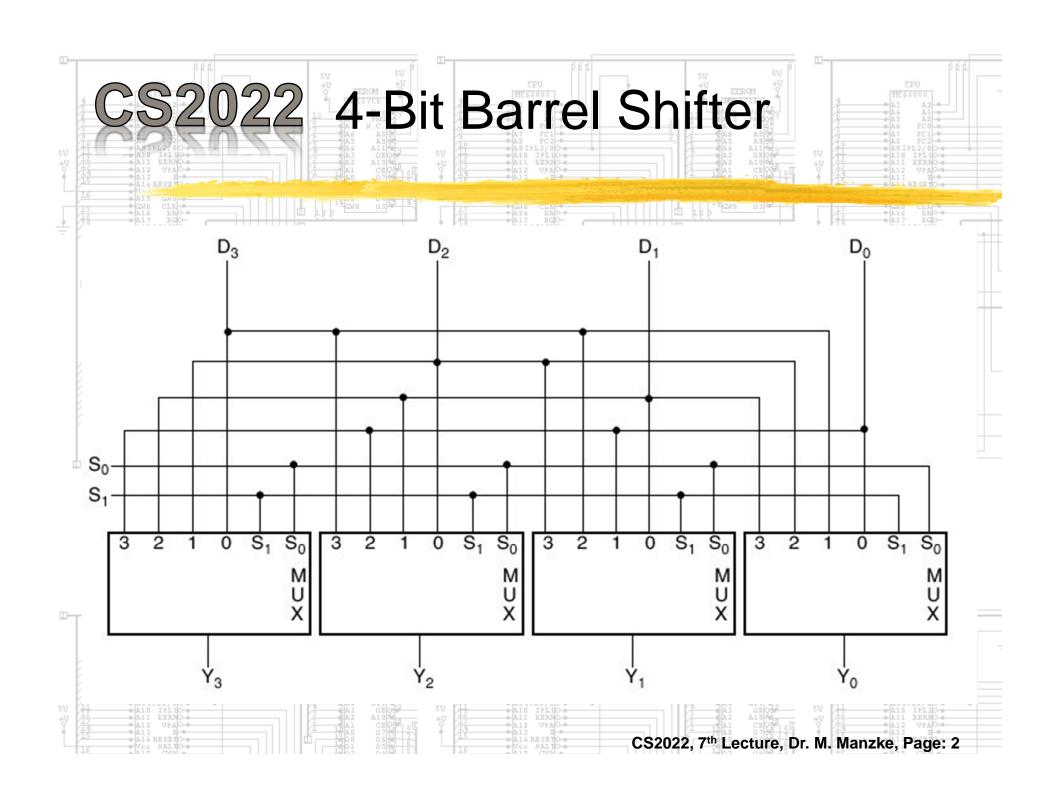
Shift Operations By controlling IR and IL with multiplexers it is straightforward to adapt this circuit to perform arithmetic shifts, constructive and destructive shifts, Rotates and rotate-thencarry operation CS2022, 7th Lecture, Dr. M. Manzke, Page: 1



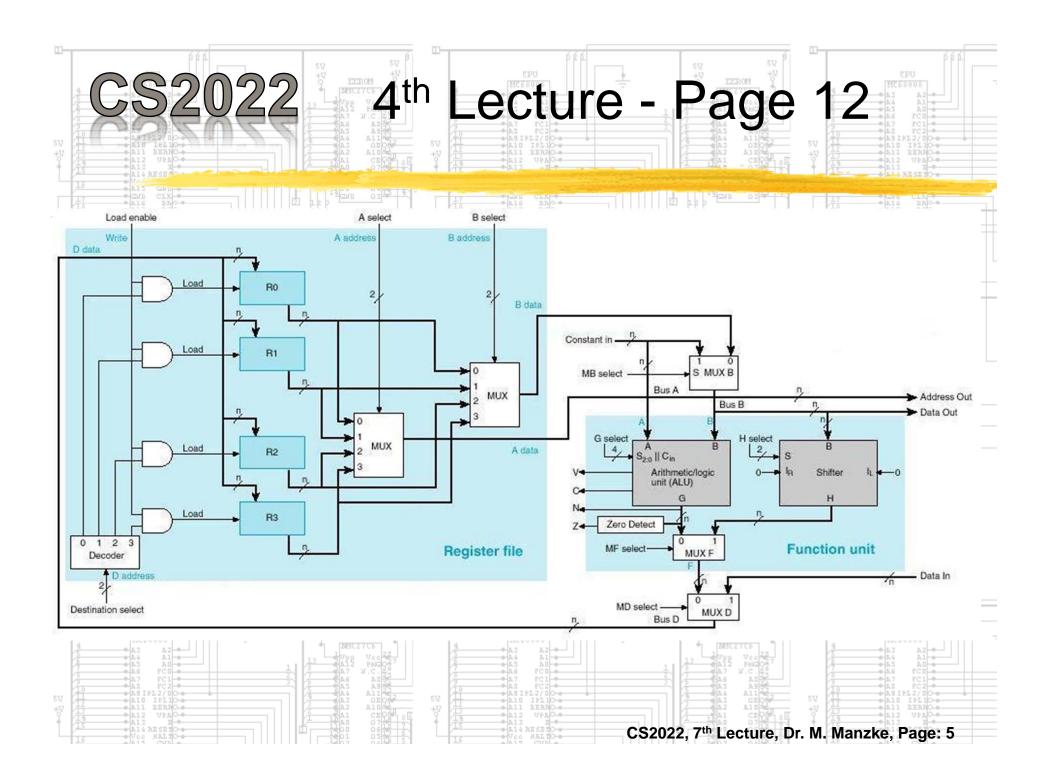
C\$2022 Multiple Shifts

If multiple shifts are required we wire them into multiplexers that have an input for every bit on the bus to obtain a Barrel shifter (Previous slide).

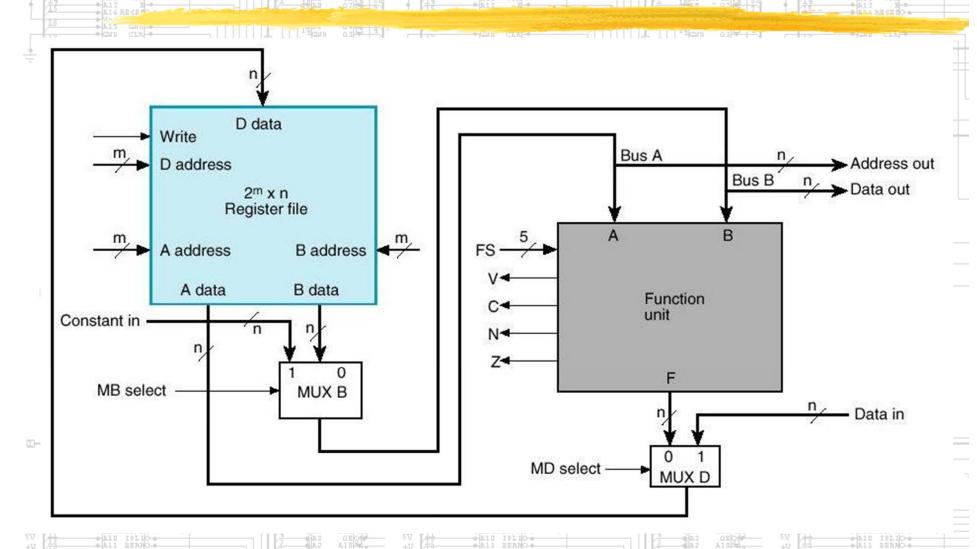
S ₁ S ₂	$Y_3 Y_2 Y_1 Y_0$	Micro-ops	
0 0	$D_3 D_2 D_1 D_0$	No Rotate	
O 1 countries 50	D_2 D_1 D_0 D_3	Rotate One	
1 0 1 20 1 20 1 2	$D_1 D_0 D_3 D_2$	Rotate Two	
1 1	D_0 D_3 D_2 D_1	Rotate Three	

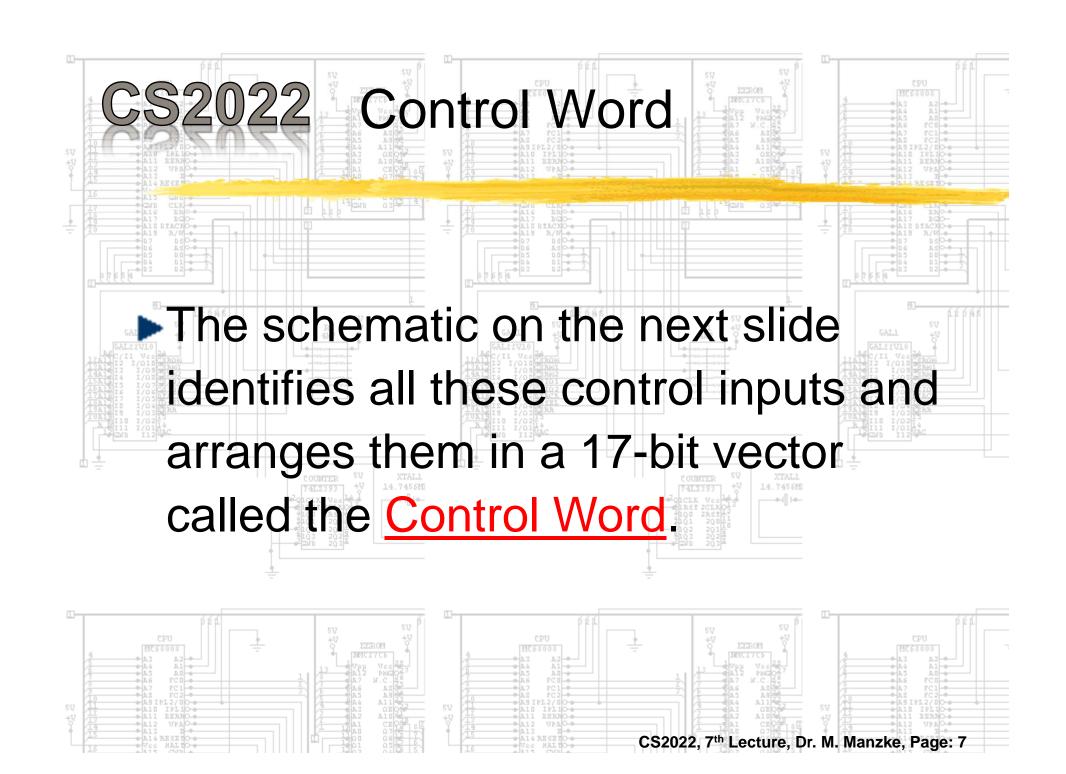
CS2022 Controlling a Datapath The Control Word

- The figure on the next slide is an updated version of our introductory datapath (4th Lecture, Page 12) where the register file has been expanded to a more realistic eight n-bit registers.
- Consequently the destination decoder and A and B bus MUX require three-bit select input.
- ► The Function Unit still requires five bits to select ALU/Shift micro-ops.
- ▶ Three more bits are required to control:
 - Writing to the registers (RW)
 - ► MUX B (MB)
 - ► MUX D (MD)

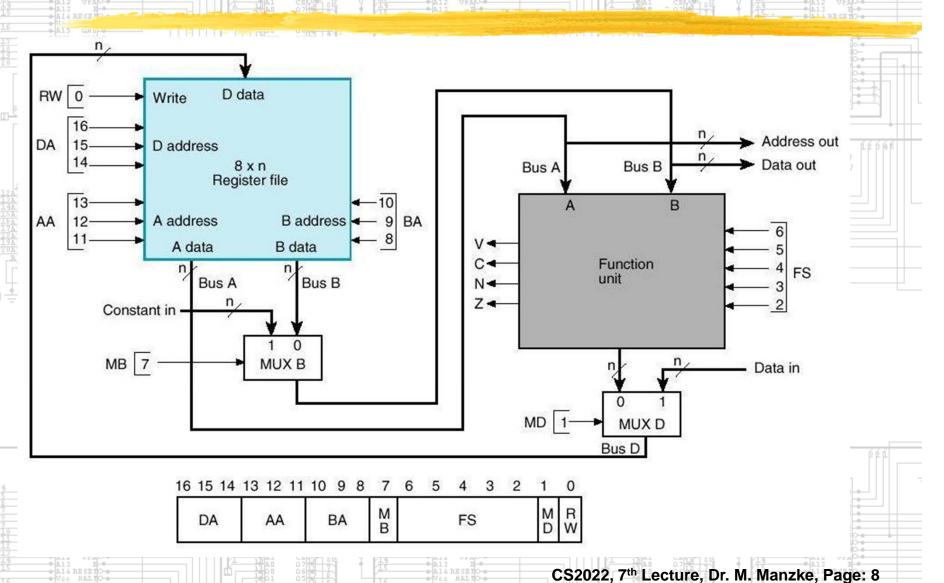


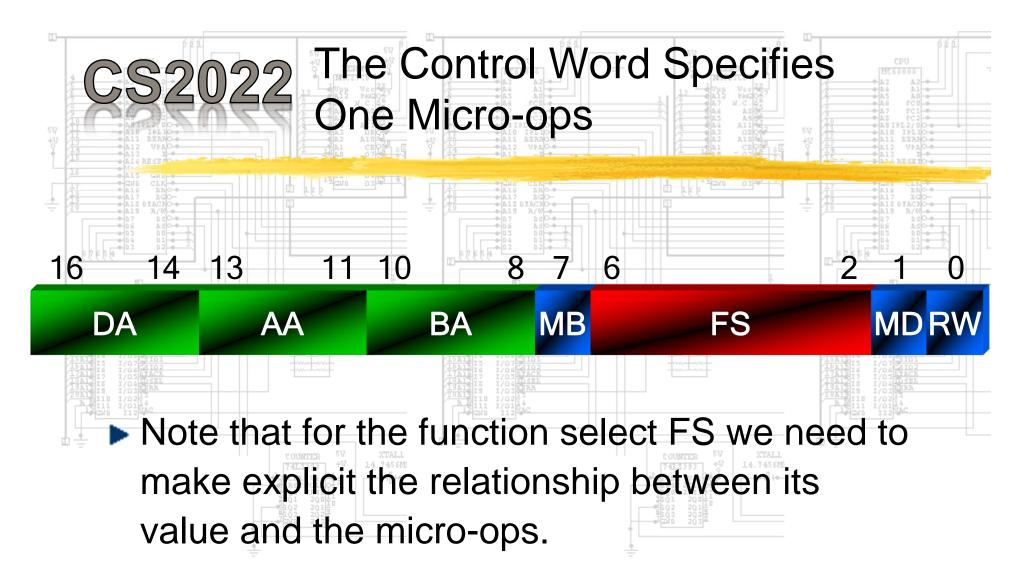
C\$2022 Updated Datapath





CS2022 Datapath and the Control Word





S2022 Select, H Select and MF Select determine the FS code

- All EGO-	FS	MF	G + 13 20	A17 EGO-	Output	18 +A17 EGO- - A18 BIACNO+
07 0500 005 0500 005 000		Select	Select	Select	Output	05 00 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
87654		Select				87654 03 02 03
E	00000	0	0000	XX	G = A	TRANSFER
5V (6 6	00001	0 81 59	0001	XX	G = A + 1 RL 50	INCREMENT
	00010	0	0010	XX	G = A + B	ADD SALESVIO
T 11311 1/01 C 1862 T 11311 1/02 C 1862 T 11311 1/02 C 102	00011	0	0011	XX	G = A + B + 1	ADD WITH C
T 11517 1/05 MACK	00100	0	0100	XX	G = A + B	A plus 1's C.B
Den Tille	00101	0	0101	XX	G = A + B + 1	SUBTRACT
1	00110	0 517	0110	XX	G = A - 1	DECREMENT
	00111	0 393 +V 14	0111	XX	G = A 2 (CX Vec 4) 14.1	TRANSFER
	01000	0	1000	XX	$G = A \wedge B$	AND
	01010	0	1010	XX	$G = A \vee B$	OR
	01100	0	1100	XX	$G = \underline{A} \oplus B$	XOR
66	<u>01110</u>	0	1110	XX	G = A	NOT
CPU (MCESOOS)	10000	577 +77 Q EEROM	XXXX	OO CPU	G = B 50 EEEROM	TRANSFER
\$ 0 A3 A2 0 A5 A6 A1 0 A5 A6	10100	NMUEYUB 12 SAI2 PAGE	XXXX	0 1 A A A A A A A A A A A A A A A A A A	G = sr B	SHIFT RIGTH
#	11000	2 1 2 A A A A A A A A A A A A A A A A A	XXXX	10° PC1	G = sl B	SHIFT LEFT

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