CS2022 Computer Architecture

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Project 1 -Datapath Design -Part A

8 February 2018

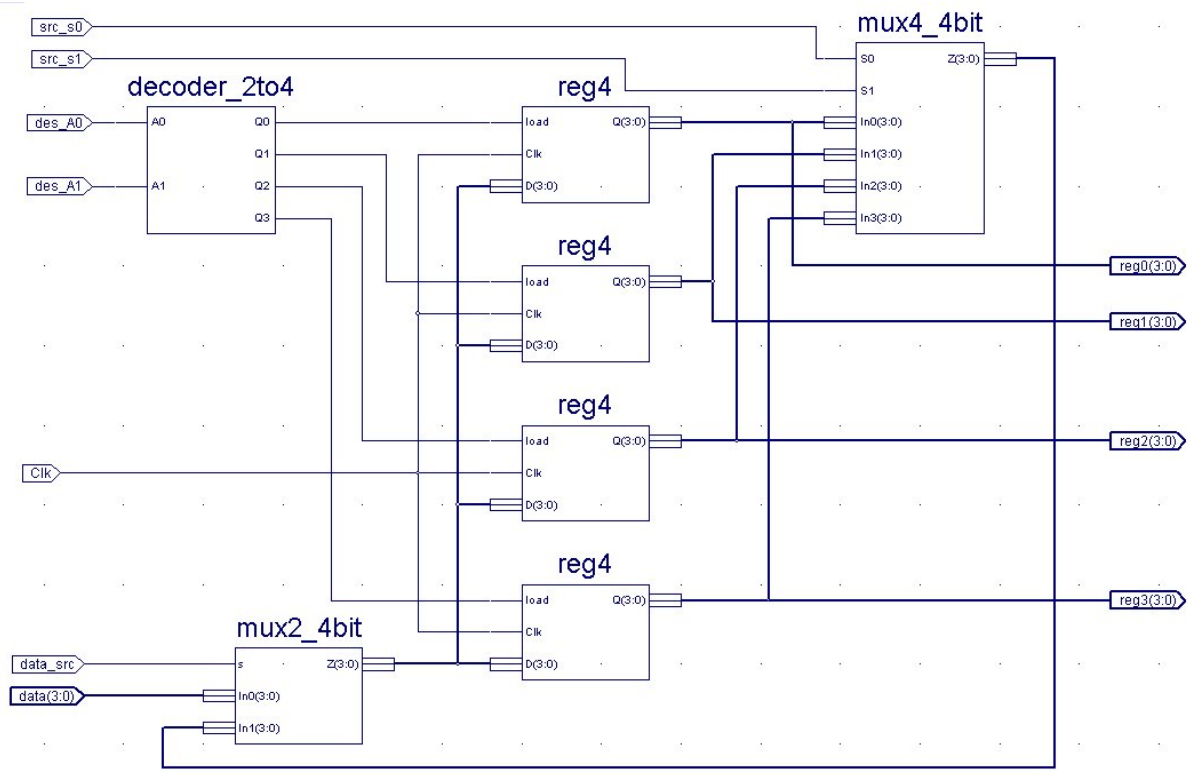
Description:

The circuit overleaf implements a 4-bit version of the Register file section of the datapath shown in Mano and Kime figure 7-9 (or 4th lecture, page 12), by using components designed in VHDL and connected at the top-level through a schematic.

1. Design the VHDL components (Register, Decoder, and two Multiplexer 16 bit) and interconnect them to build a register file. The schematic shows only four registers. Your solution should implement eight registers.
2. You should provide test benches and simulations that prove the correctness of the following operations:
    a. Correctly load an arbitrary HEX value into each of the eight registers, i.e. that it can execute the transfers R_i <-X_i i=0,7
    b. Correctly transfer the contents of any register to any other register, i.e. that it can execute the transfers R_i <- R_j, I,j=O,7

DUE: Friday, 16th February 2018

Please submit a copy of your VHDL-code and test-benches including all simulation results to Blackboard.


src_s0
src_s1
mux4_4bit
S0
S1
Z(3:0)
decoder_2to4
reg4
des_A0
des_A1
A0
A1
Q0
Q1
Q2
Q3
load
Clk
D(3:0)
Q(3:0)
In0(3:0)
In1(3:0)
In2(3:0)
In3(3:0)
reg0(3:0)
reg1(3:0)
reg2(3:0)
reg3(3:0)
Clk
mux2_4bit
data_src
data(3:0)
s