DLD lab report 6
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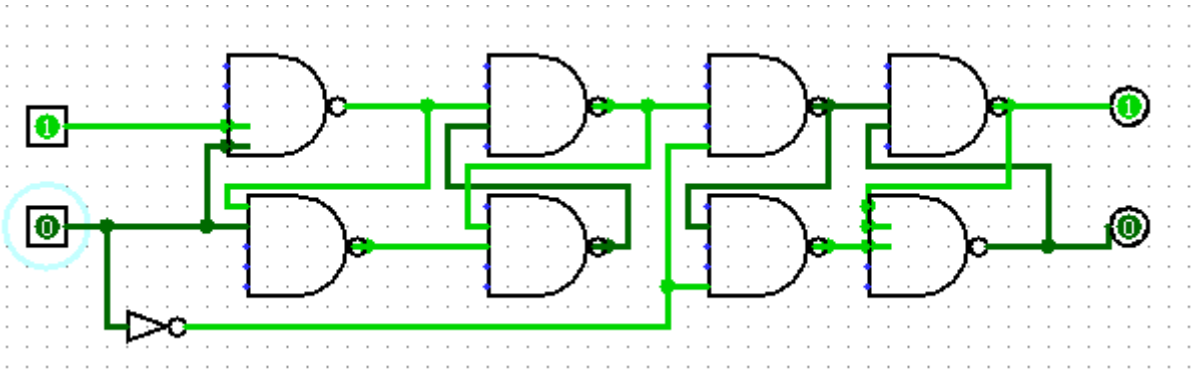
Negative edge triggered D flip-flop:



This flip-flop works as follow. Only when the clock switch from a logic state 1 to a logic state 0 can the state of the outputs change. From that, if data is 1, then Q will stay 1 or change to 1. And if data is 0 then Q will become 0 or stay 0.

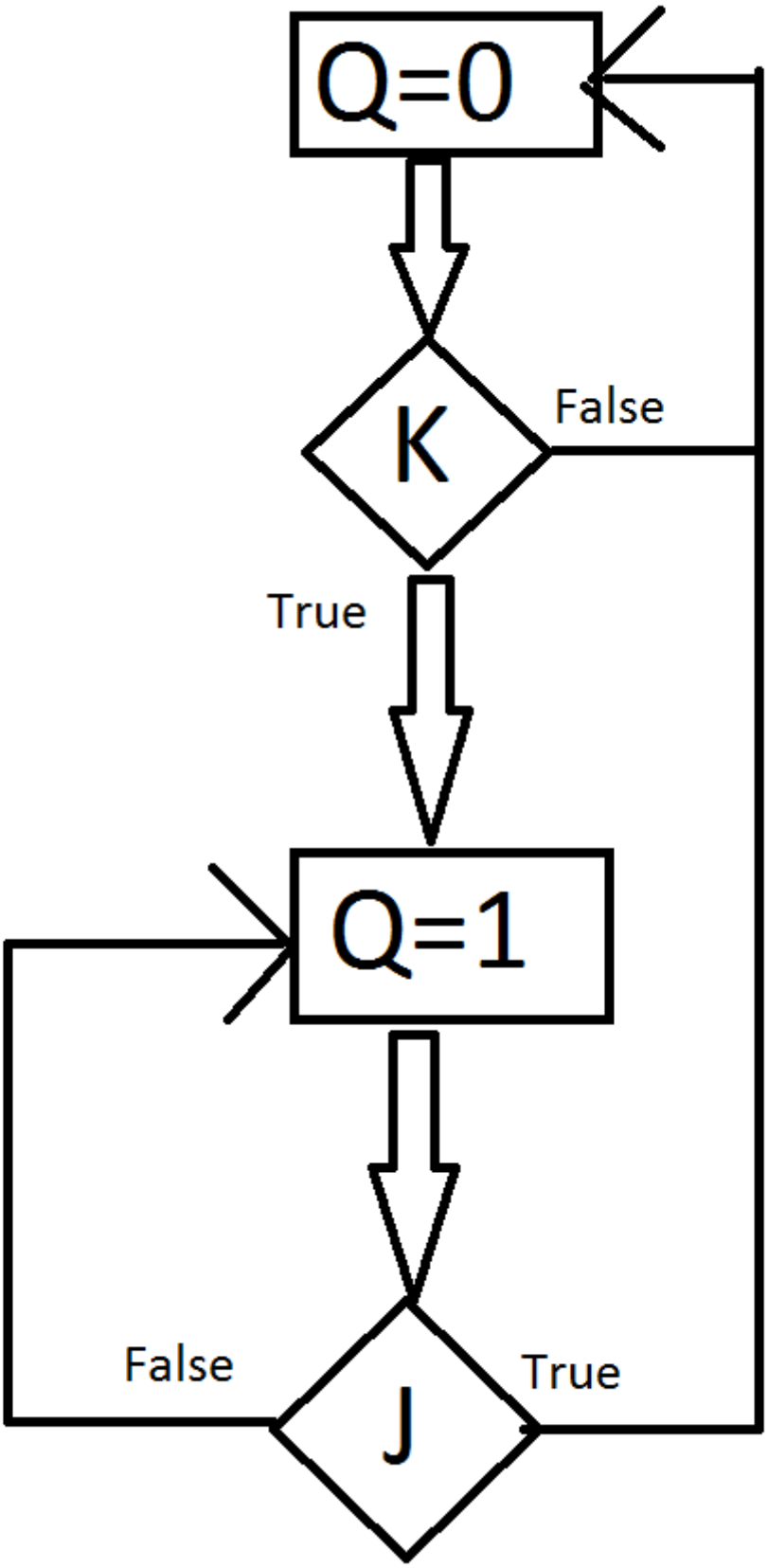
J-K flip-flop PS/NS table:

J	K	Q(next)	Q'(next)
0	0	Q	Q'
0	1	0	1
1	0	1	0
1	1	Q'	Q

A J-K flip-flop can be rising edge or falling edge, but when both inputs are 1, they act as a toggle flip-flop.

J-K flip-flop ASM:

We just read from the PS/NS table and we can draw an ASM with it. Diamonds represents evaluation and rectangle the state of our output.


Q=0
K
False
True
Q=1
False
J
True