DECODERS

A binary code of n bits is capable of representing up to 2^n distinct elements of coded information.

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.

If the n-bit coded information has unused combinations, the decoder may have fewer than 2^n outputs.

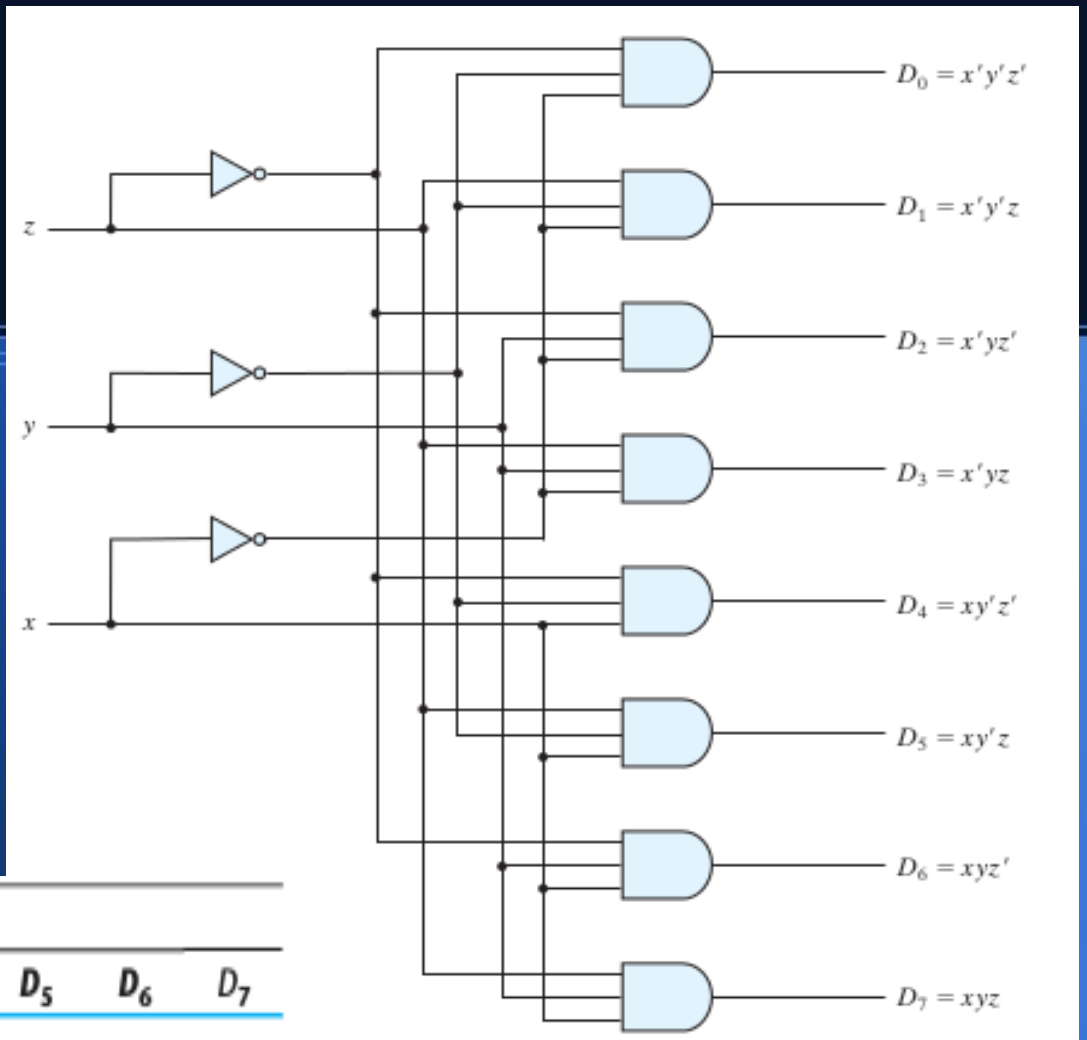
In digital circuits, one-hot refers to a group of bits among which the legal combinations of values are only those with a single high '1' bit and all the others low '0'.

A similar implementation in which all bits are '1' except one '0' is sometimes called one-cold.

A simple decoder circuit is a binary to one-hot or one-cold converter

Three-to-eight-line decoder

The decoder is a commonly used type of integrated circuit.
This decoder generates all of the minterms of the three input variables.



Inputs			Outputs							
x	y	z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Exactly one of the output lines will be 1 for each combination of the values of the input variables.

For a boolean function of n variables {x1, ... xn}, a product term in which each of the n variables appears once (in either its complemented or uncomplemented form) is called a minterm.

Thus, a minterm is a logical expression of n variables that employs only the complement operator and the conjunction operator.

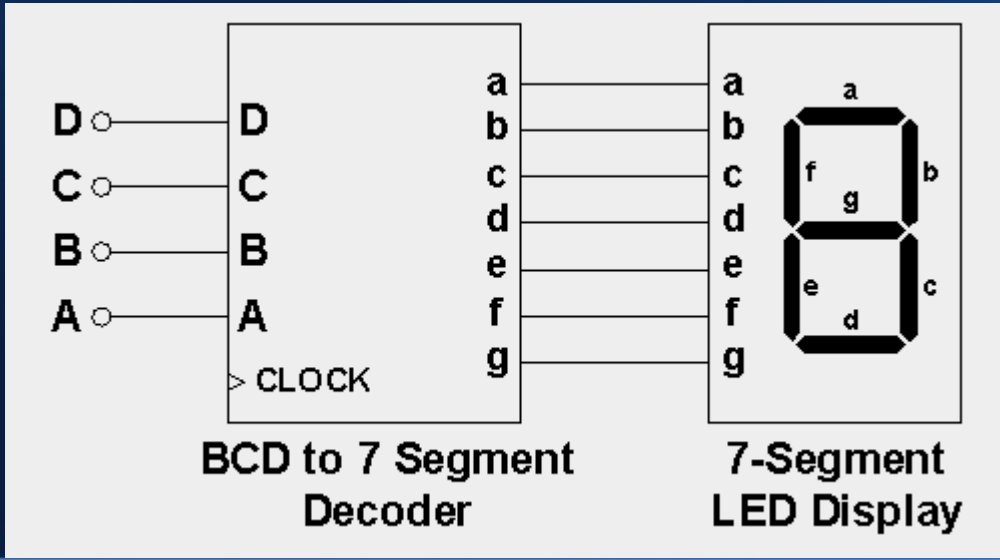
For example, abc, ab'c and abc' are 3 examples of the 8 minterms for a boolean function of the three variables a, b, and c.

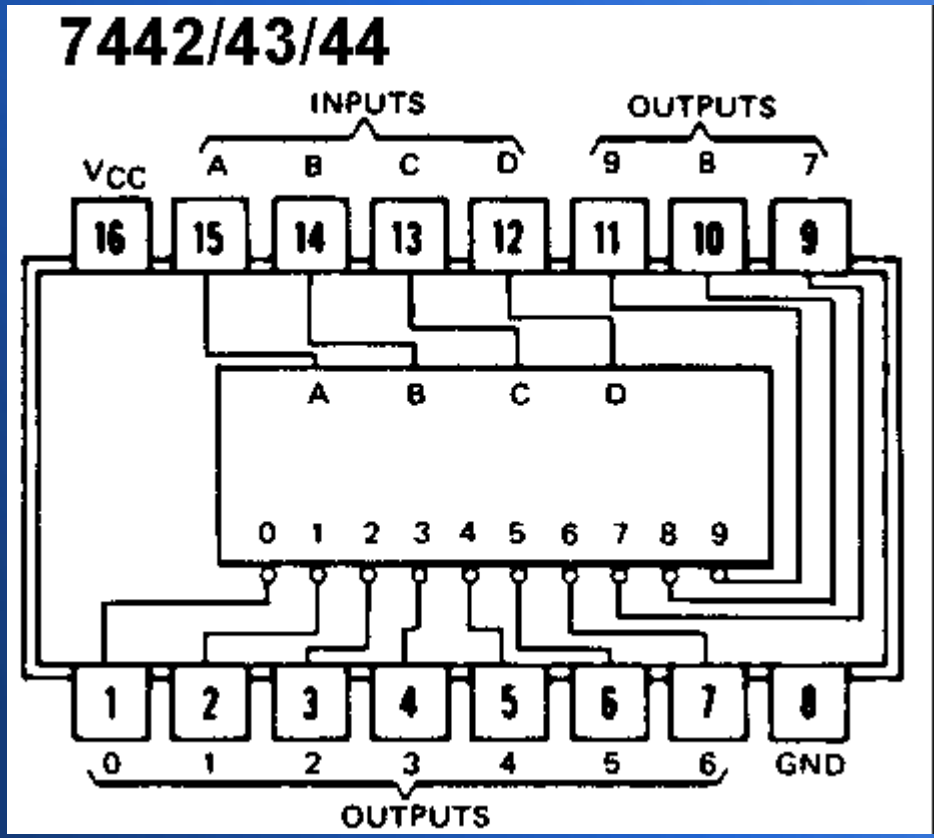
The customary reading of the last of these is a AND b AND NOT-c.

There are 2^n minterms of n variables, since a variable in the minterm expression can be in either its direct or its complemented form—two choices per n variables.

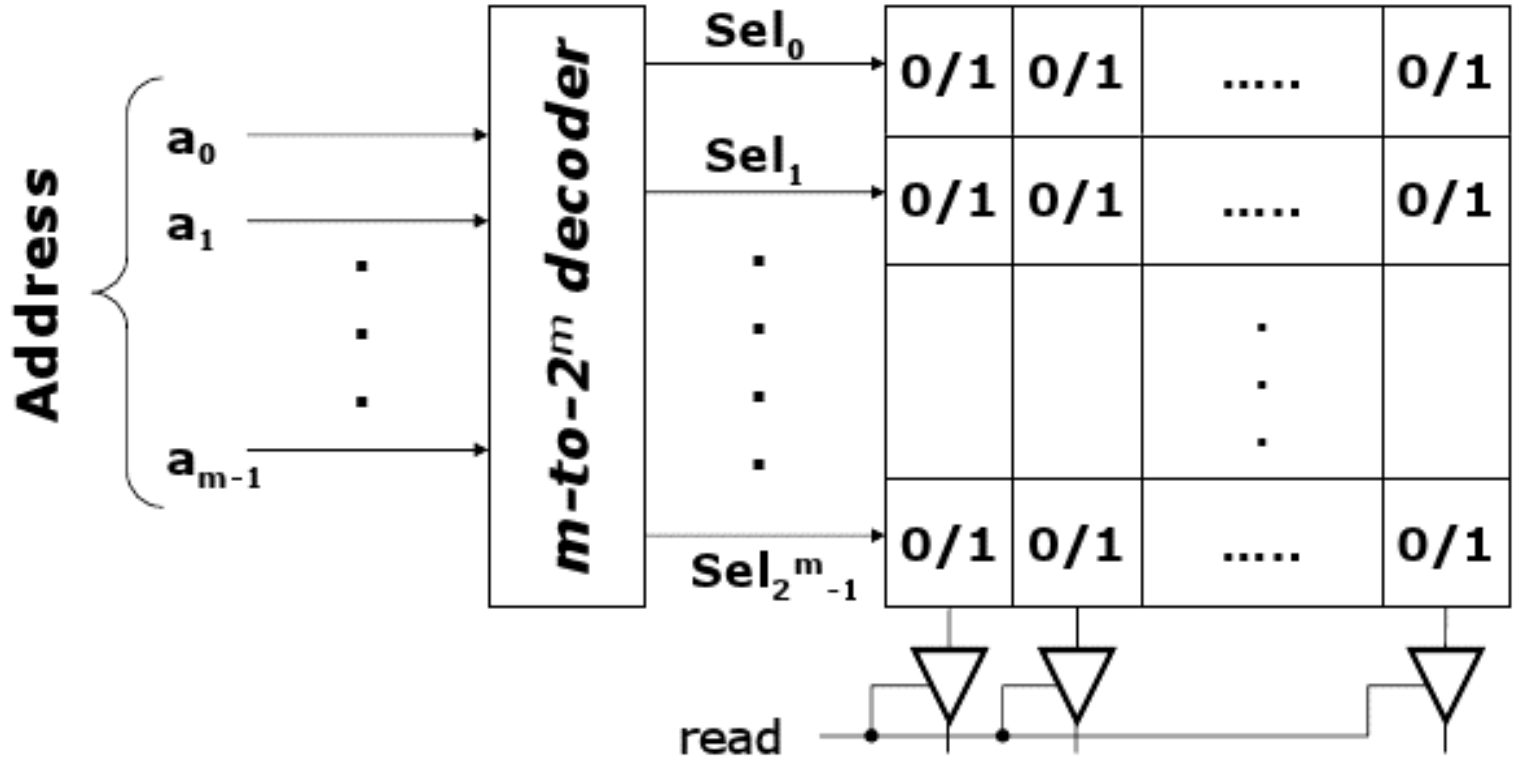
The term decoder is sometimes also used in conjunction with other code converters, such as a BCD-to-seven-segment decoder

Binary Inputs				Decoder Outputs							7-Segment Display Outputs
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9





- A common decoder application is the decoding of address lines for memory chips

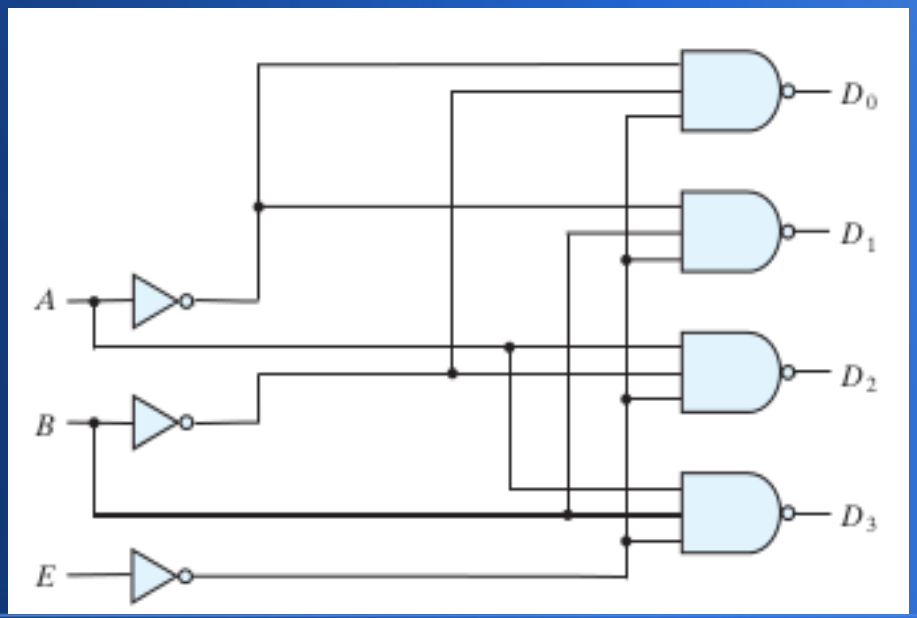


Two-to-four-line decoder with enable input

Some decoders are constructed with NAND gates. Since a NAND gate produces the AND operation with an inverted output, it becomes more economical to generate the decoder minterms in their complemented form.

Furthermore, decoders include one or more enable inputs to control the circuit operation.

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0



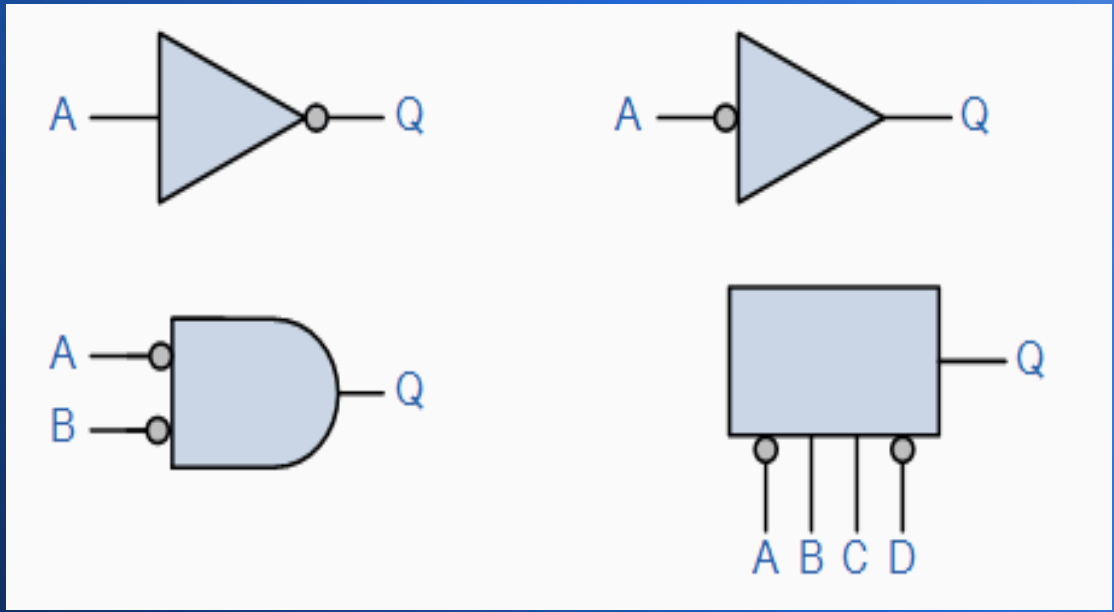
The decoder above can function as a one-to-four-line demultiplexer when E is taken as a data input line and A and B are taken as the selection inputs.

The single input variable E has a path to all four outputs, but the input information is directed to only one of the output lines, as specified by the binary combination of the two selection lines A and B.

This feature can be verified from the truth table of the circuit. For example, if the selection lines A B = 1 0, output D2 will be the same as the input value E, while all other outputs are maintained at 1.

Because decoder and demultiplexer operations are obtained from the same circuit, a decoder with an enable input is referred to as a decoder–demultiplexer.

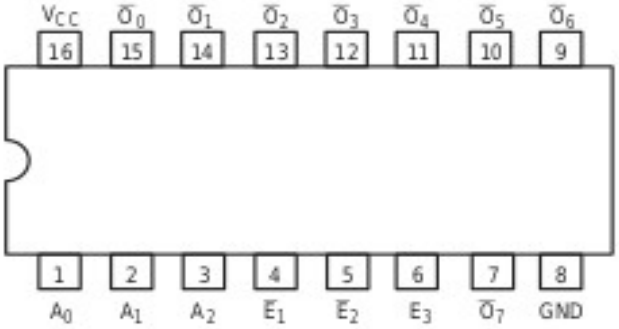
The "bobble" (o) present at the end of the NOT gate symbol above denotes a signal inversion (complimentation) of the output signal. But this bubble can also be present at the gates input to indicate an active-LOW input.



This inversion of the input signal is not restricted to the NOT gate only but can be used on any digital circuit or gate as shown with the operation of inversion being exactly the same whether on the input or output terminal. The easiest way is to think of the bobble as simply an inverter.

SN74LS138

CONNECTION DIAGRAM DIP (TOP VIEW)

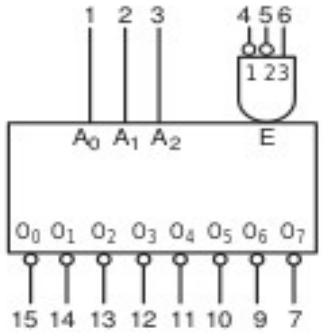


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a) HIGH	LOW
$A_0 - A_2$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_1, \overline{E}_2$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_3	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_7$	Active LOW Outputs	10 U.L.	5 U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.

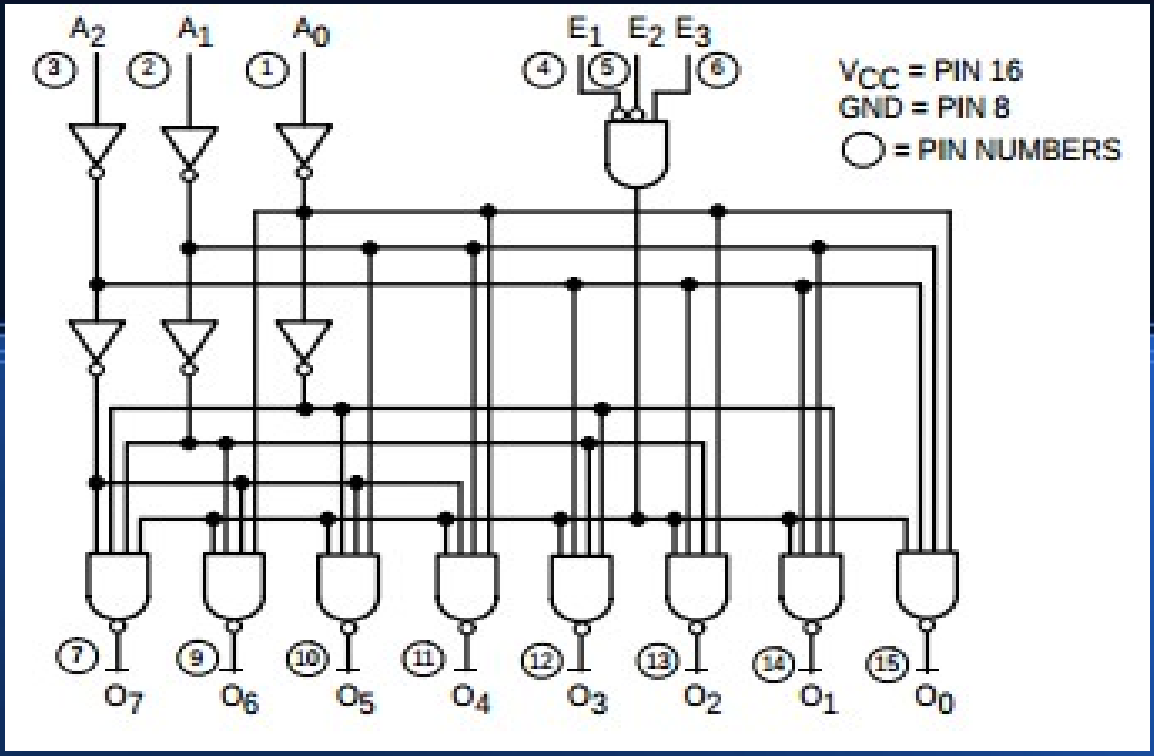
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

The prefix SN indicates that the chip was made by Texas Instruments

Low-power Schottky TTL (LS) – used the higher resistance values of low-power TTL and the Schottky diodes to provide a good combination of speed (9.5ns) and reduced power consumption (2 mW).



TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E_1}$	$\overline{E_2}$	$\overline{E_3}$	A_0	A_1	A_2	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$	$\overline{O_4}$	$\overline{O_5}$	$\overline{O_6}$	$\overline{O_7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Multiplexing

In telecommunications and computer networks, multiplexing (sometimes contracted to muxing) is a method by which multiple analog message signals or digital data streams are combined into one signal over a shared medium.

The aim is to share an expensive resource. For example, in telecommunications, several telephone calls may be carried using one wire.

The multiplexed signal is transmitted over a communication channel, which may be a physical transmission medium (e.g. a cable).

A reverse process, known as demultiplexing, can extract the original channels on the receiver side.

Decoder–Demultiplexer

A decoder with enable input can function as a demultiplexer—a circuit that receives information from a single line and directs it to one of 2^n possible output lines.

The selection of a specific output is controlled by the bit combination of n selection lines.

The 74139 contains two demultiplexers; pins 1-7 on the left control the 1st demux, while pins 9-15 control the 2nd demux

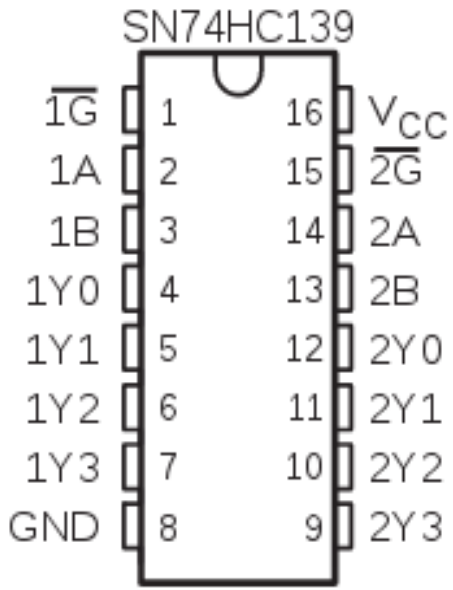


Figure 1. SN74HC139 pin-out.

SN74HC139 Demux Truth Table

INPUTS			OUTPUTS			
	SELECT					
I ($\overline{1G}$)	S1 (1B)	S0 (1A)	Y0 (1Y0)	Y1 (1Y1)	Y2 (1Y2)	Y3 (1Y3)
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	X	X	1	1	1	1

1 = Vcc 0 = Ground X = don't care () = IC pin name

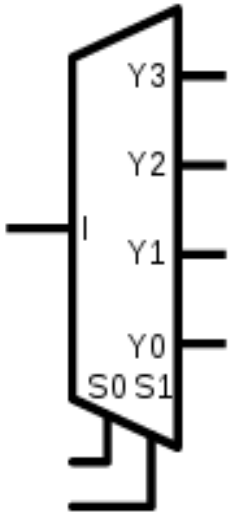
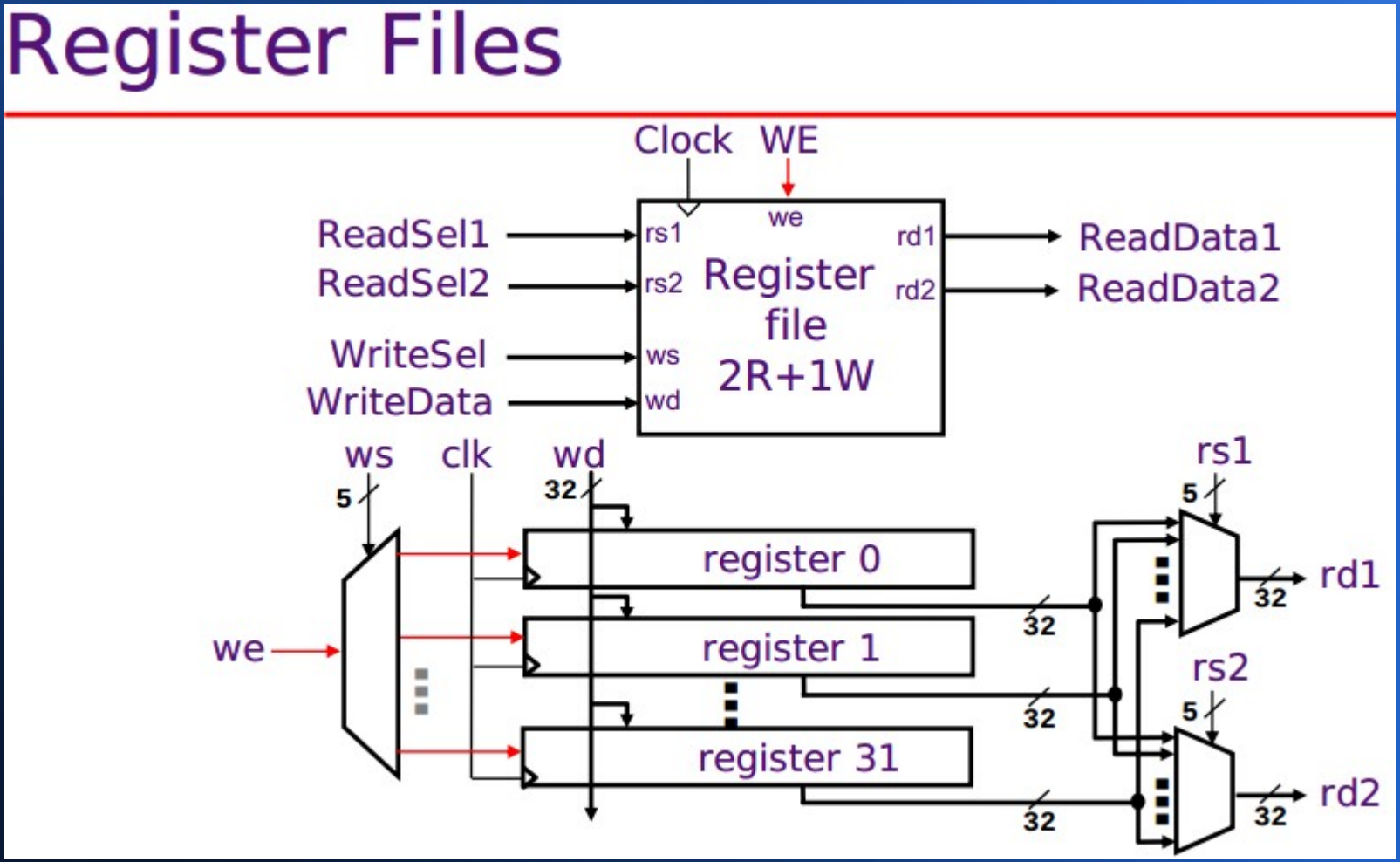


Figure 2. Demux function table.

The schematic symbol for a demultiplexer is an isosceles trapezoid with the longer parallel side containing the output pins and the short parallel side containing the input pin

This register file makes it possible to simultaneously read from two registers and write into one register.



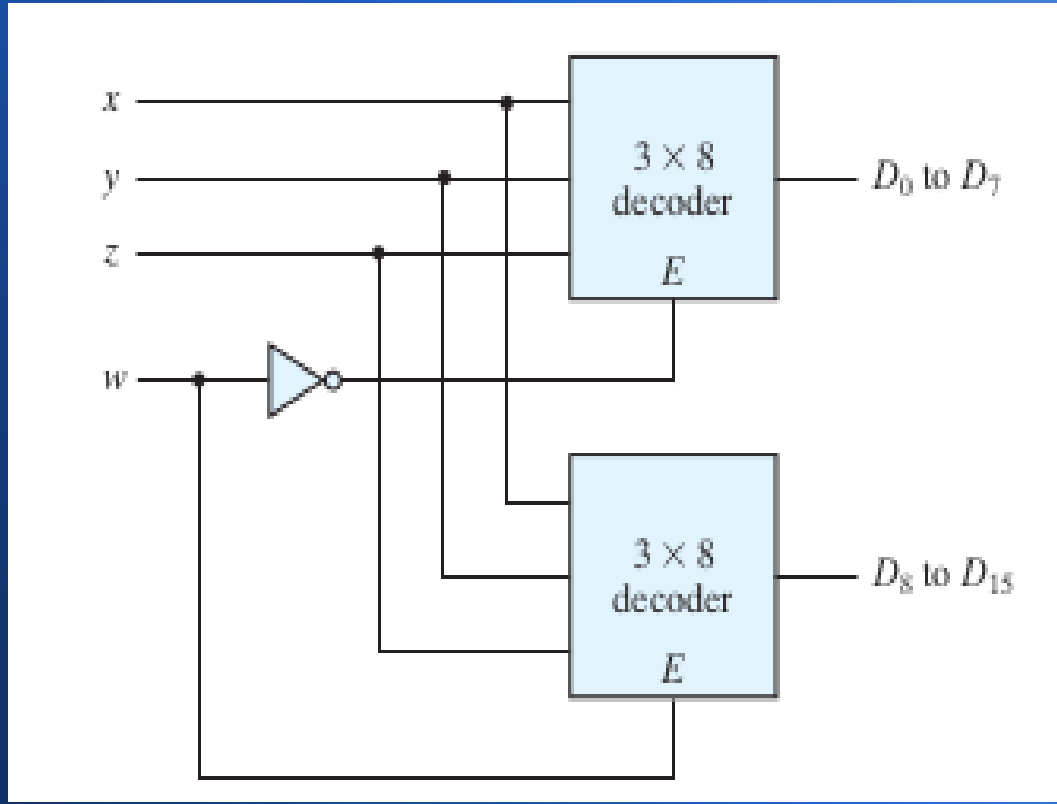
4 * 16 decoder constructed with two 3 * 8 decoders

Decoders with enable inputs can be connected together to form a larger Decoder circuit.

This shows two 3-to-8-line decoders with enable inputs connected to form a 4-to-16-line decoder.

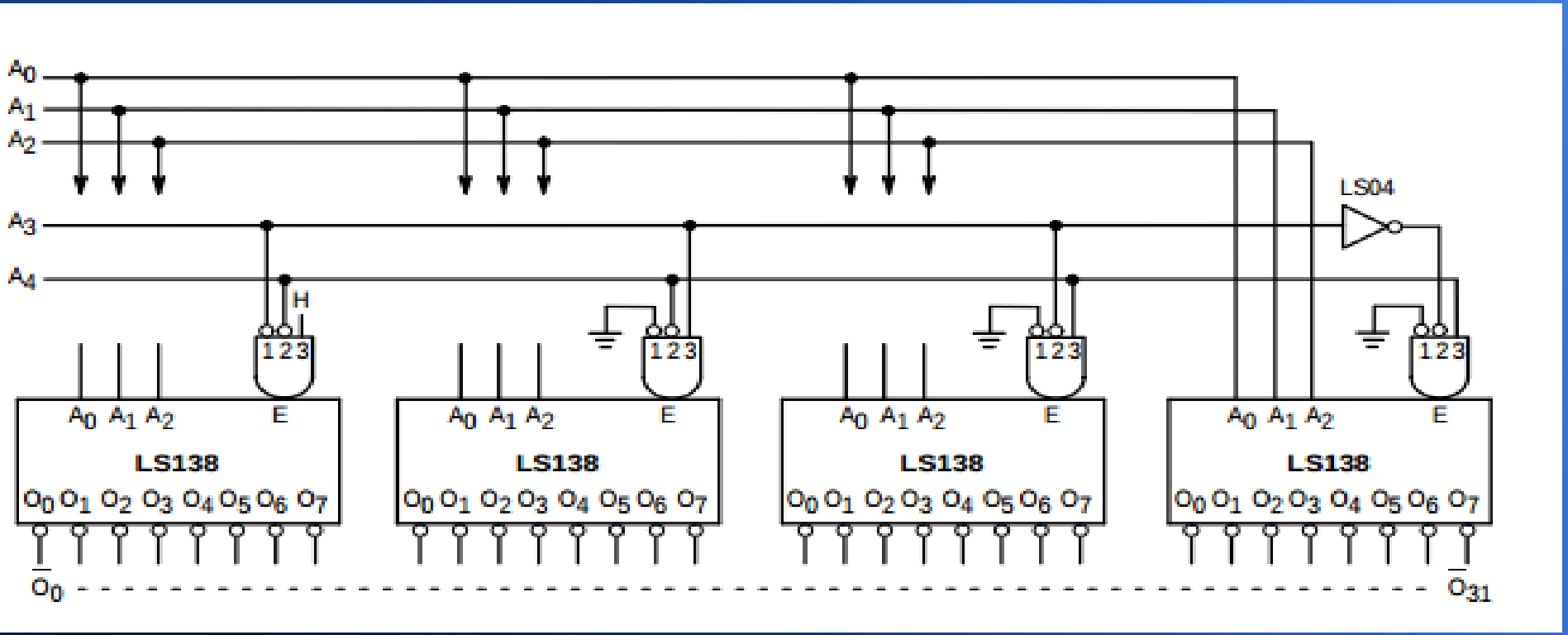
When w = 0, the top decoder is enabled and the other is disabled.

The bottom decoder outputs are all 0's, and the top eight outputs generate minterms 0000 to 0111.



When w = 1, the enable conditions are reversed: The bottom decoder outputs generate minterms 1000 to 1111, while the outputs of the top decoder are all 0's.

In general, enable inputs are a convenient feature for interconnecting two or more standard components for the purpose of combining them into a similar function with more inputs and outputs.



A decoder provides the 2^n minterms of n input variables.

Each asserted output of the decoder is associated with a unique pattern of input bits.

Since any Boolean function can be expressed in sum-of-minterms form, a decoder that generates the minterms of the function, together with an external OR gate that forms their logical sum, provides a hardware implementation of the function.

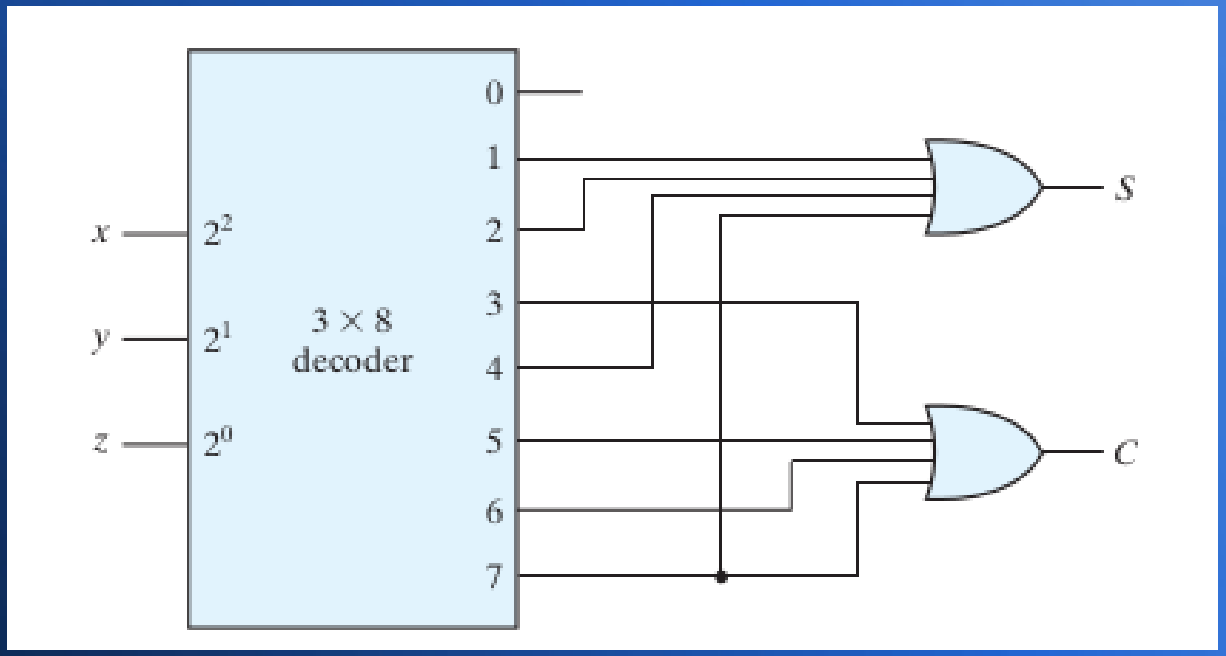
In this way, any combinational circuit with n inputs and m outputs can be implemented with an n-to-2^n-line decoder and m OR gates.

Implementation of a full adder with a decoder

$$S(x, y, z) = \Sigma(1, 2, 4, 7)$$

$$C(x, y, z) = \Sigma(3, 5, 6, 7)$$

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



A function with a long list of minterms requires an OR gate with a large number of inputs. A function having a list of k minterms can be expressed in its complemented Form F' with 2^n - k minterms. If the number of minterms in the function is greater than 2^n/2, then F' can be expressed with fewer minterms (use NOR gate).

If NAND gates are used for the decoder, as in then the external gates must be NAND gates instead of OR gates.

This is because a two-level NAND gate circuit implements a sum-of-minterms function and is equivalent to a two-level AND–OR circuit.

By means of a DeMorgan Transformation, we've taken our original circuit comprising two ANDs and an OR (with 18 transistors) and transformed it into a new version comprising three NANDs (with 14). This equates to around a 20% reduction in transistors.