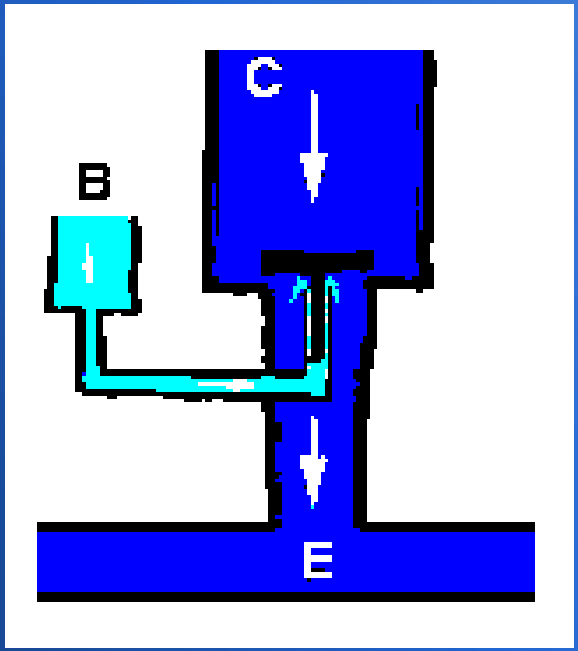
BIPOLAR JUNCTION TRANSISTORS (BJTS)

William Bradford Shockley Jr. (February 13, 1910 – August 12, 1989) was an American physicist and inventor.

Along with John Bardeen and Walter Houser Brattain, Shockley co-invented the Transistor in 1948, for which all three were awarded the 1956 Nobel Prize in Physics

How transistors work, fluid analogy

Provide a reservoir of water for "C" (the "power supply voltage") but it can't move because there's a big black plunger thing in the way which is blocking the outlet to "E". The reservoir of water is called the "supply voltage". If we increase the amount of water sufficiently, it will burst our transistor just the same as if we increase the voltage to a real transistor. We don't want to do this, so we keep that "supply voltage" at a safe level.



If we pour water current into "B" this current flows along the "Base" pipe and pushes that black plunger thing upwards, allowing quite a lot of water to flow from "C" to "E". Some of the water from "B" also joins it and flows away.
If we pour even more water into "B", the black plunger thing moves up further and a great torrent of water current flows from "C" to "E"

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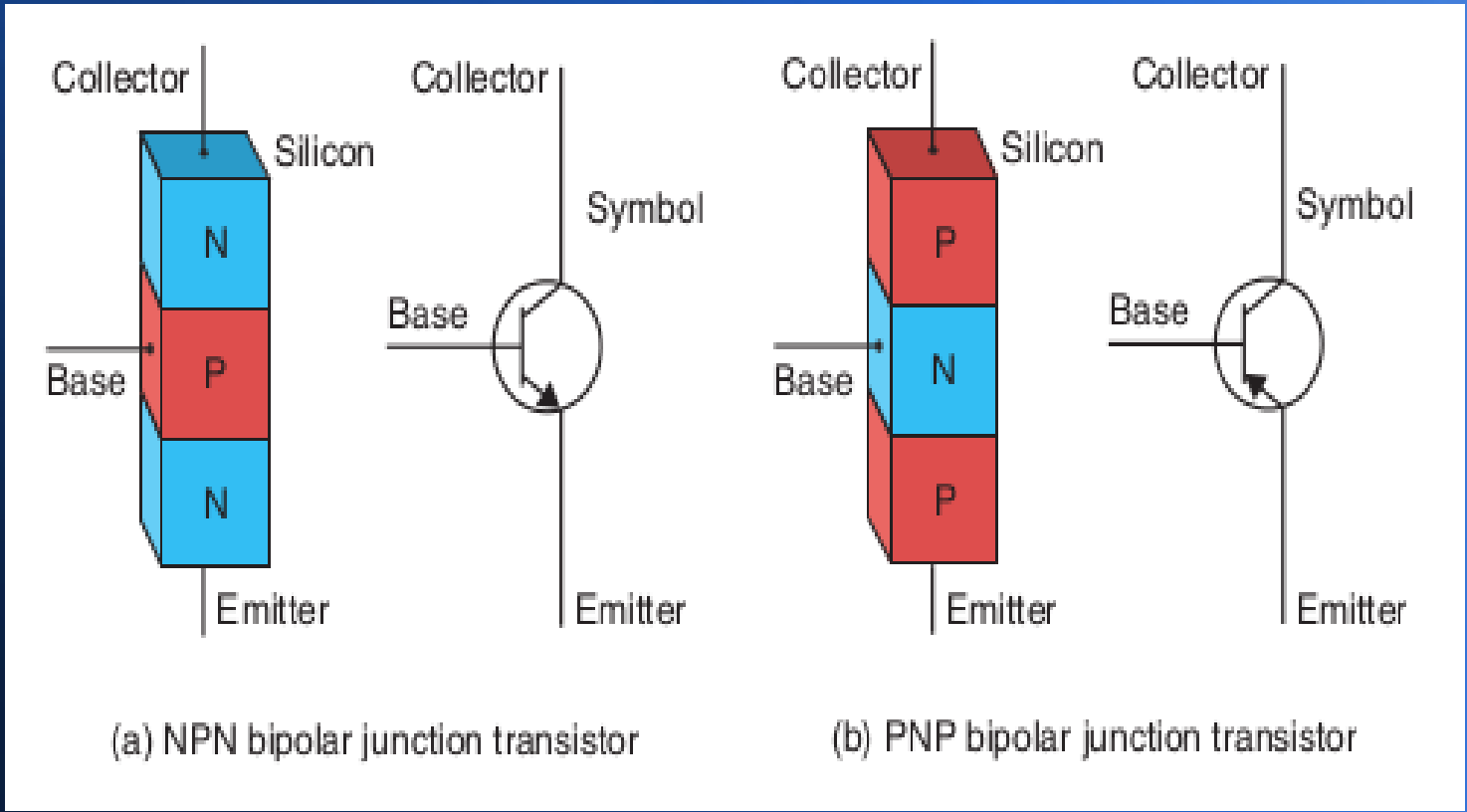
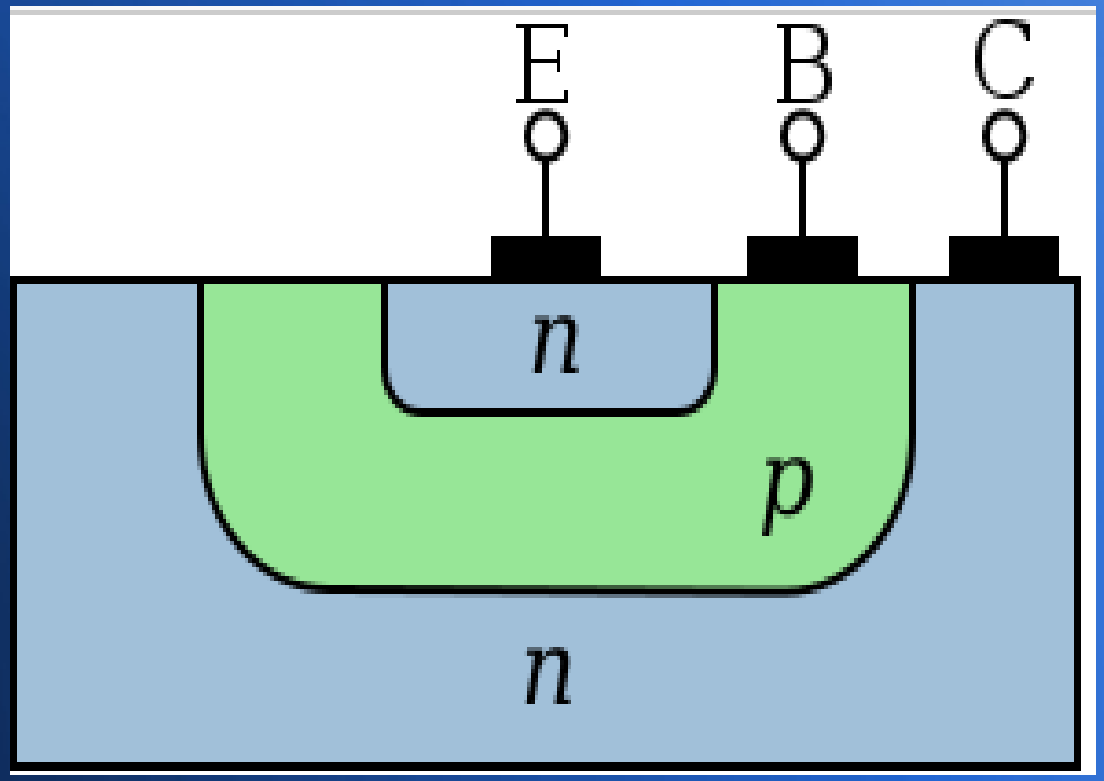
With an electrical current applied to the center layer (called the base), electrons will move from the N-type side to the P-type side. The initial small trickle acts as a switch that allows much larger current to flow.



Simplified cross section of a planar NPN bipolar junction transistor

Transistors can be created by forming a sandwich out of three regions of doped silicon



In 1948, Shockley invented a new device called a Bipolar Junction Transistor

In the analogue world, a transistor can be used as a voltage amplifier, a current amplifier, or a switch; in the digital world, a transistor is primarily considered to be a switch

BIPOLAR JUNCTION TRANSISTORS (BJTS)

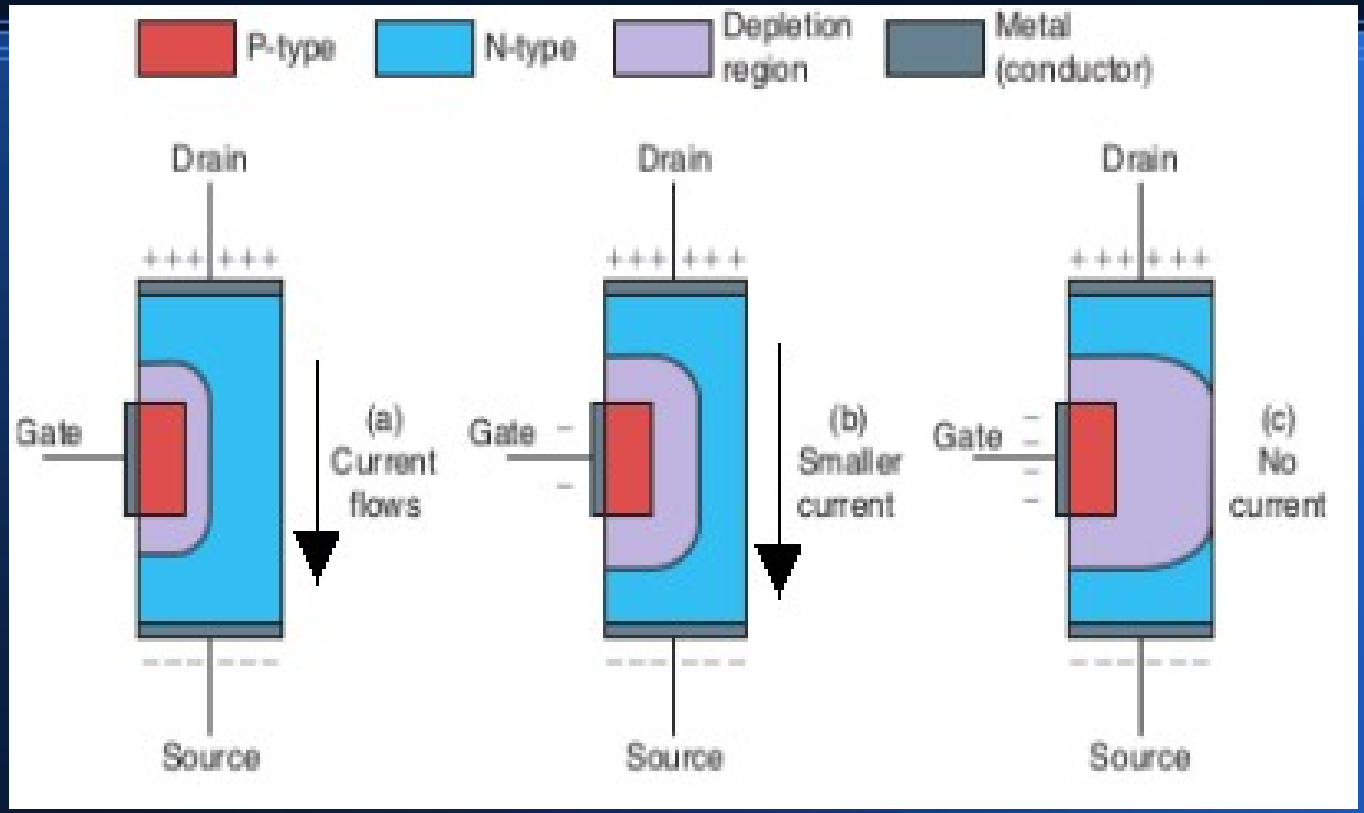
While the n-type has a surplus of electrons, the p-type has holes where electrons should be. Normally, the holes in the base act like a barrier, preventing any significant current flow flowing from the emitter to the collector and the transistor is in its "off" state.

Suppose we attach a small positive voltage to the base, make the emitter negatively charged, and make the collector positively charged. Electrons are pulled from the emitter into the base—and then from the base into the collector. And the transistor switches to its "on" state

BIPOLAR JUNCTION TRANSISTORS (BJTS)

The small current that we turn on at the base makes a big current flow between the emitter and the collector. By turning a small input current into a large output current, the transistor acts like an amplifier. But it also acts like a switch at the same time

Junction Field-Effect Transistors



In field-effect transistors (FETs), depletion mode and enhancement mode are two major transistor types, corresponding to whether the transistor is in an ON state or an OFF state at zero gate–source voltage.

Junction Field-Effect Transistors

Formed by the junction of P-type and N-type silicon

The drain and source as form “data” terminals and the gate acting as the “control” terminal.

When no signal is being applied to the gate terminal, the default depletion region still leaves a channel of N-type silicon between the source and the drain, thereby allowing electrons to flow.

Junction Field-Effect Transistors

Applying a small negative potential to the gate terminal, (reverse bias) like pinching a garden hosepipe to reduce the flow of water, reduces the size of the conducting channel between the source and the drain terminals.

In turn, this increases the resistance of the channel and reduces the flow of current between the source and the drain terminals.

If we keep on increasing the negative potential on the gate terminal, at some stage the depletion zone will completely block the channel.

Junction Field-Effect Transistors

JFETs have good linearity and low noise, and they are used almost entirely for processing analog signals.

Typical applications include low-level audio amplification and Radio Frequency (RF) circuits such as RF mixers.

JFETs also have a very high input impedance, which makes them suitable for applications like test equipment because they have minimal disturbance on the signals being measured.

Enhancement mode - to turn ON the channel, you need to bias the gate higher than the Vt, the threshold voltage.

Depletion mode - the device is normally ON, you need to provide a bias to turn off, or "Pinch OFF" the channel.

All modern digital ICs use enhancement mode NMOS and PMOS in CMOS.

If you try to use depletion mode, the gate voltage must go beyond the power supply rails to shut the devices off.

Depletion mode devices are useful in analog circuits.

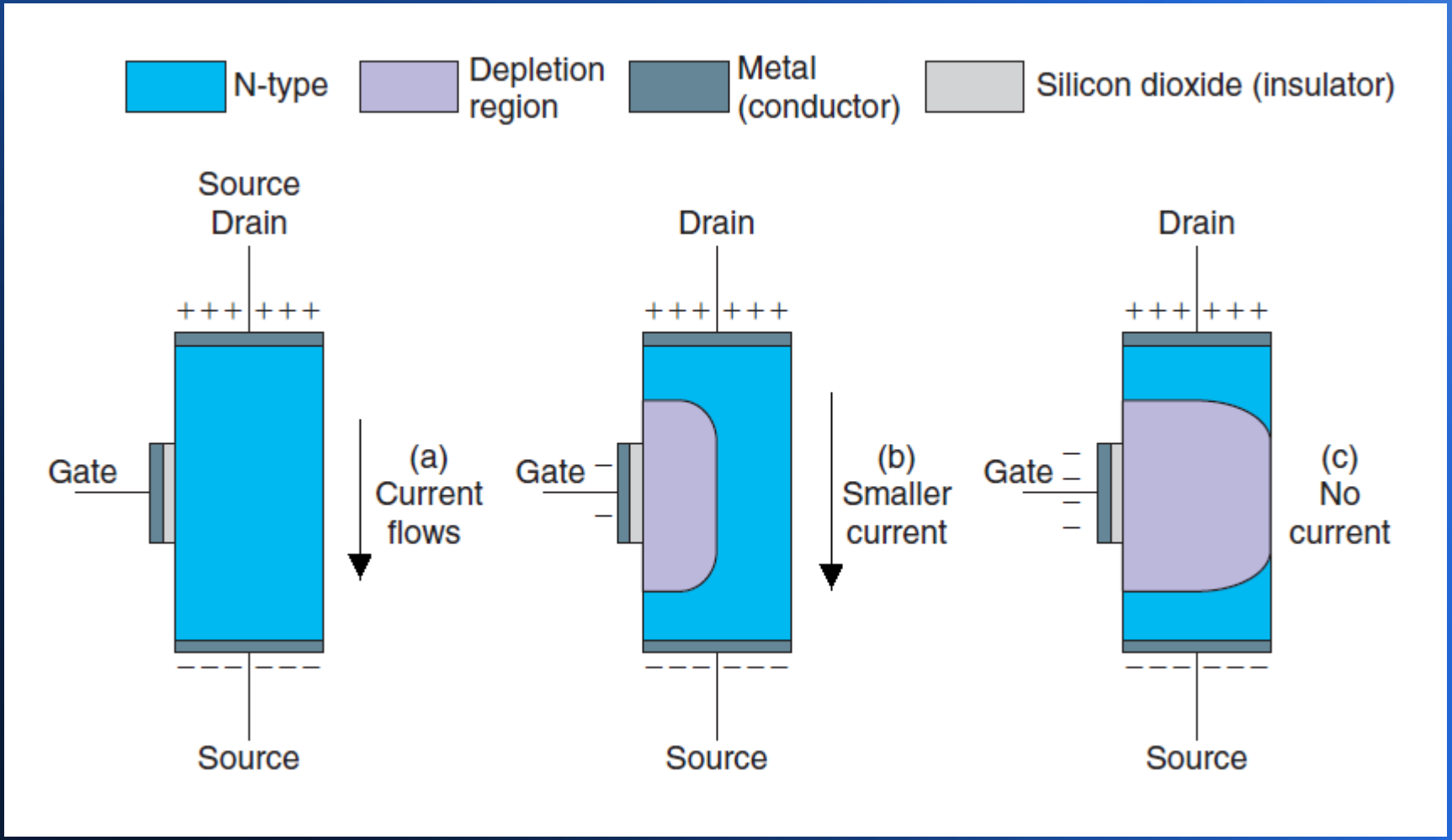
The JFET was predicted by Julius Lilienfeld in 1925 and by the mid-1930s its theory of operation was sufficiently well known to justify a patent.

However, it was not possible for many years to make doped crystals with enough precision to show the effect.

In 1947, researchers John Bardeen, Walter Houser Brattain, and William Shockley were trying to make a JFET when they discovered the point-contact transistor.

The first practical JFETs were made many years later, in spite of their conception long before the junction transistor.

Depletion-mode n-channel MOSFET



Depletion-mode n-channel MOSFET

In the case of these devices, the drain and source form the data terminals and the gate acts as the control terminal. Unlike bipolar devices, the control terminal is connected to a conducting plate, which is insulated from the silicon by a layer of non conducting oxide or a layer of polycrystalline silicon (poly silicon)

Depletion-mode n-channel MOSFET is a unipolar transistor because only one kind ("polarity") of electric charge is involved in making it work.

Depletion-mode n-channel MOSFET

When no signal is being applied to the gate, the channel of N-type silicon between the source and the drain allows current to flow. This means that these devices are ON by default and we have to apply a signal to the gate terminal in order to turn them OFF.

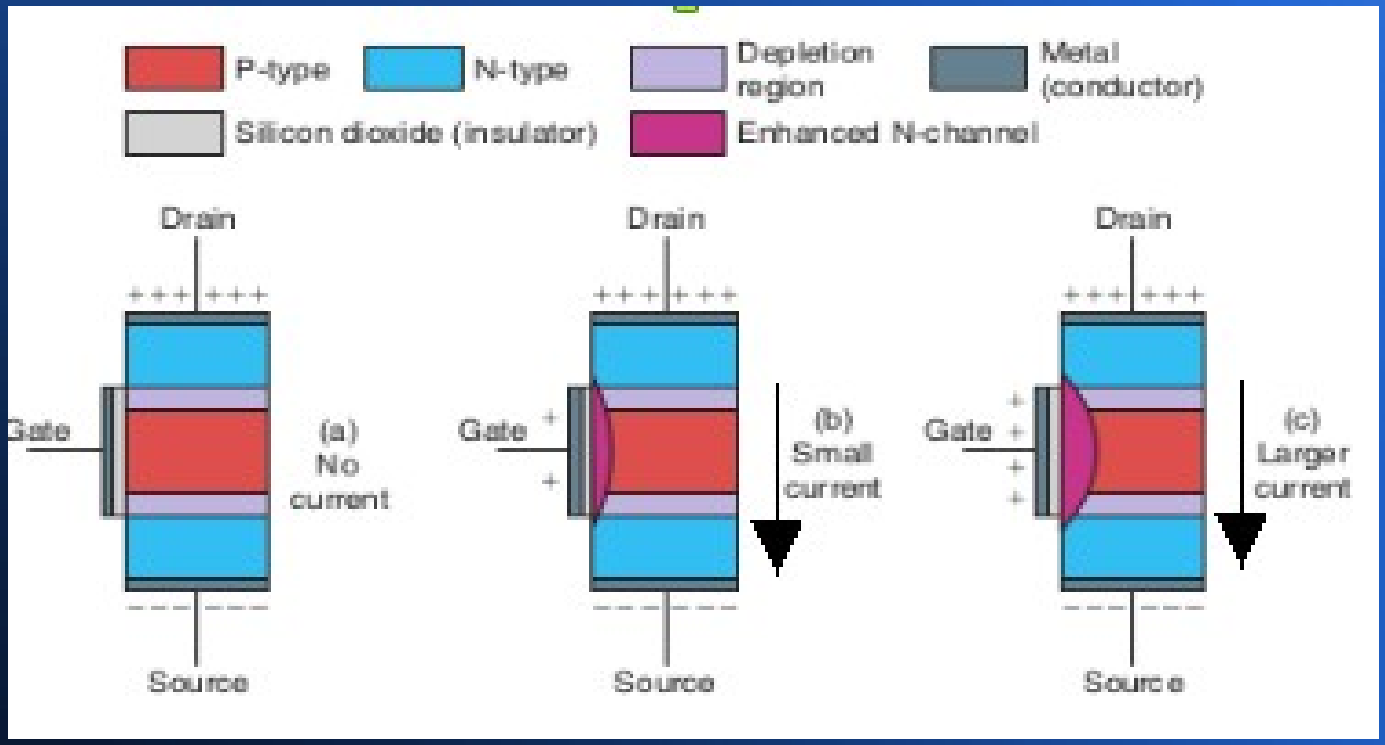
Due to their low noise figure in the RF region, and better gain, these devices are often preferred to bipolars in RF front-ends such as in TV sets.

Depletion-mode n-channel MOSFET

The control terminal is connected to a conducting plate, which is insulated from the silicon by a layer of non conducting oxide. In the original devices the conducting plate was metal—hence, the term “metal-oxide”—but this is now something of a misnomer because modern versions tend to use a layer of polycrystalline silicon (poly silicon).

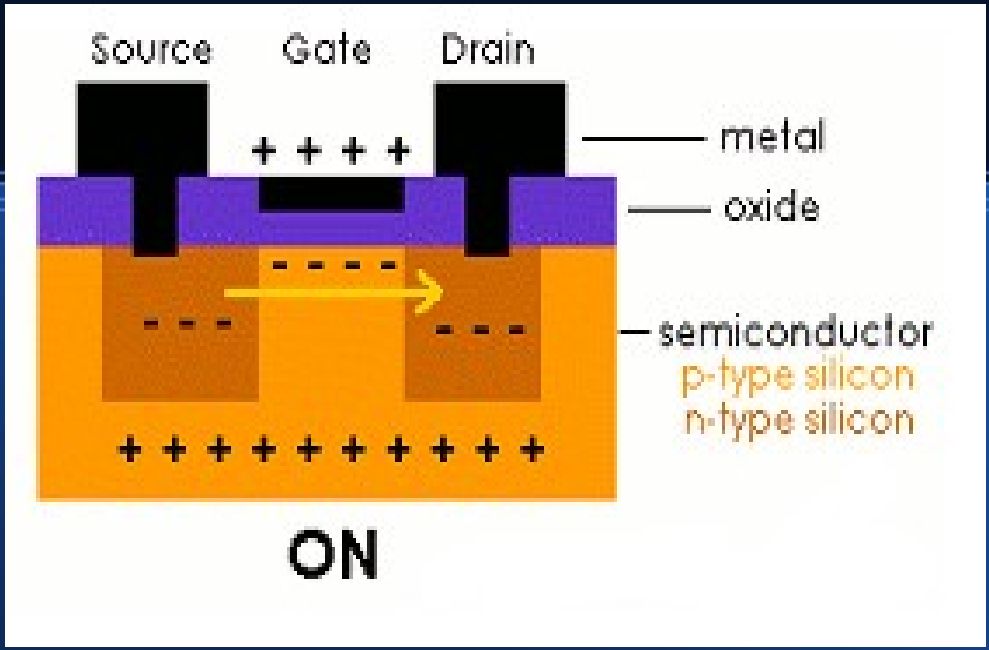
When a signal is applied to the gate terminal, the plate, insulated by the oxide, creates an electromagnetic field, which turns the transistor ON or OFF—hence, the term “field-effect.”

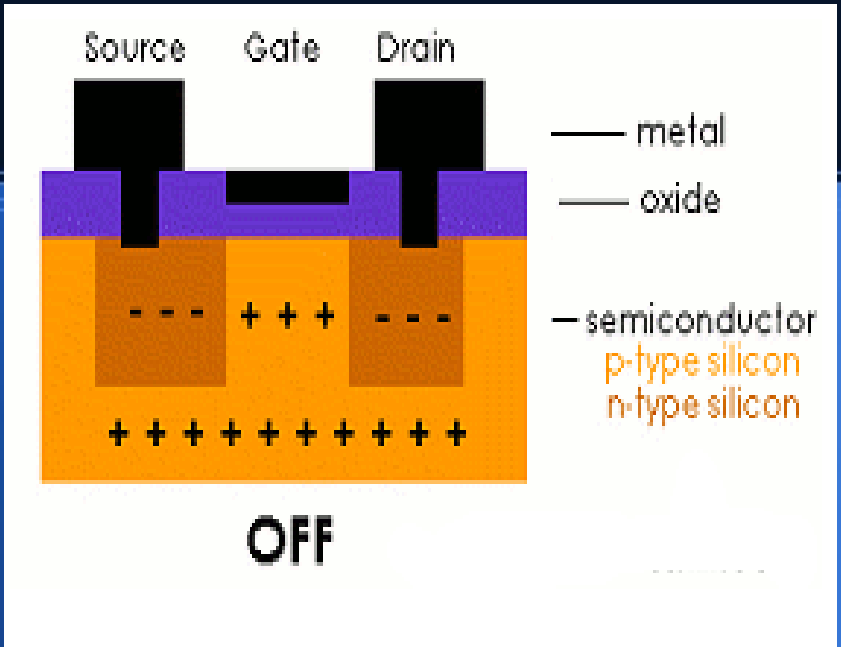
ENHANCEMENT-MODE MOSFETS



nMOS is made with a p-type substrate (active high)

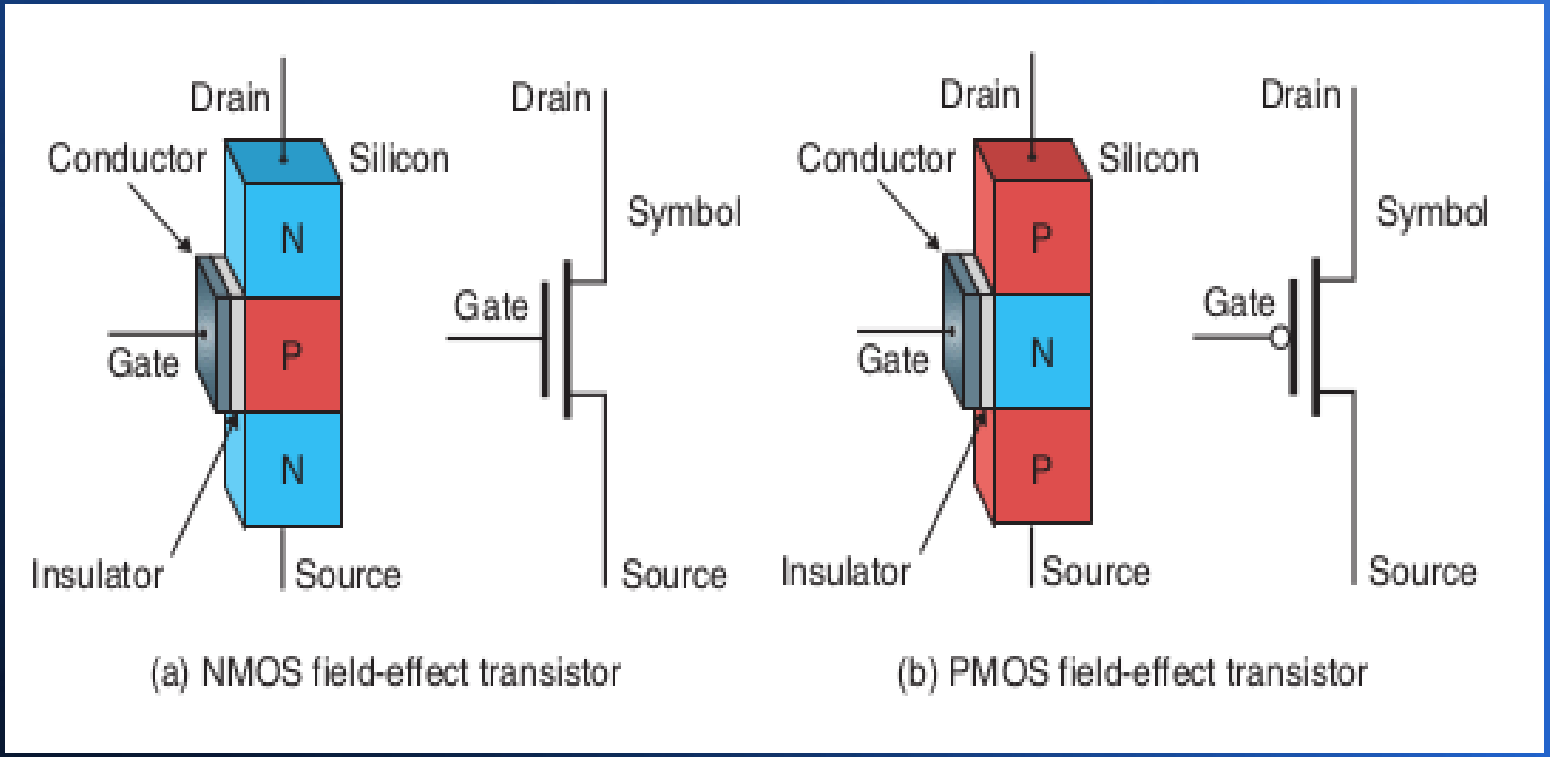
ENHANCEMENT-MODE MOSFETS





The gate has a voltage applied to it that makes it positive with respect to the source. This causes holes in the P type layer close to the silicon dioxide layer beneath the gate to be repelled down into the P type substrate, and at the same time this positive potential on the gate attracts free electrons from the surrounding substrate material. These free electrons form a thin layer of charge carriers beneath the gate electrode (they can't reach the gate because of the insulating silicon dioxide layer) bridging the gap between the heavily doped source and drain areas. This layer is sometimes called an "inversion layer" because applying the gate voltage has caused the P type material immediately under the gate to firstly become "intrinsic" (with hardly any charge carriers) and then an N type layer within the P type substrate.

ENHANCEMENT-MODE MOSFETS



ENHANCEMENT-MODE MOSFETS

Enhancement-mode MOSFETs are formed from two p-n-junctions, which act like two back-to-back diodes

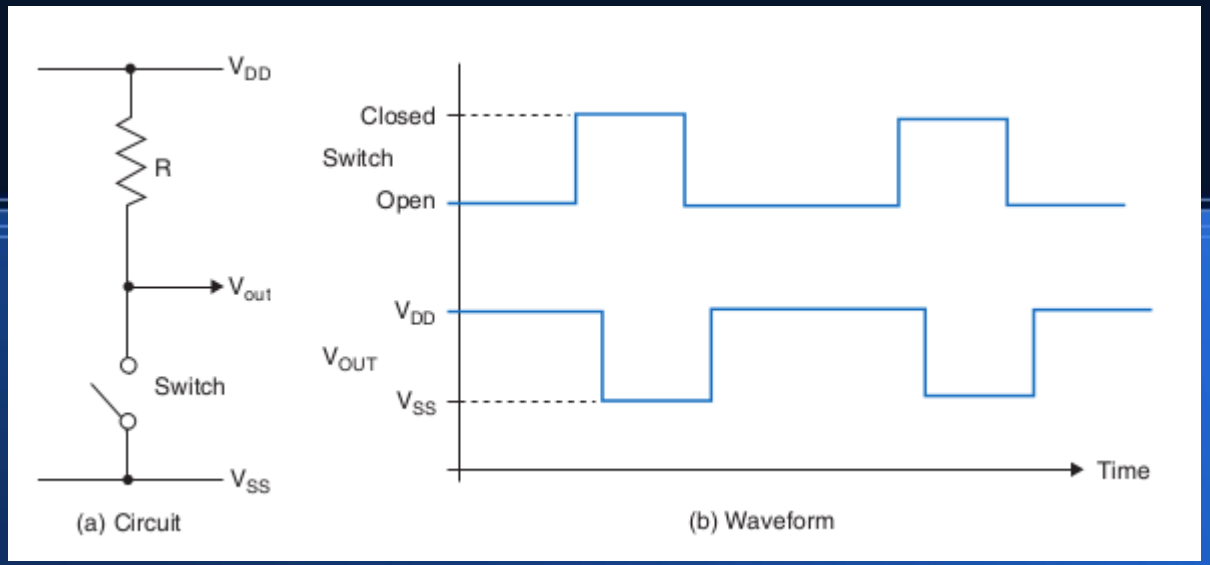
By default, this device is OFF and we have to apply an electrical potential to its gate terminal to turn it ON

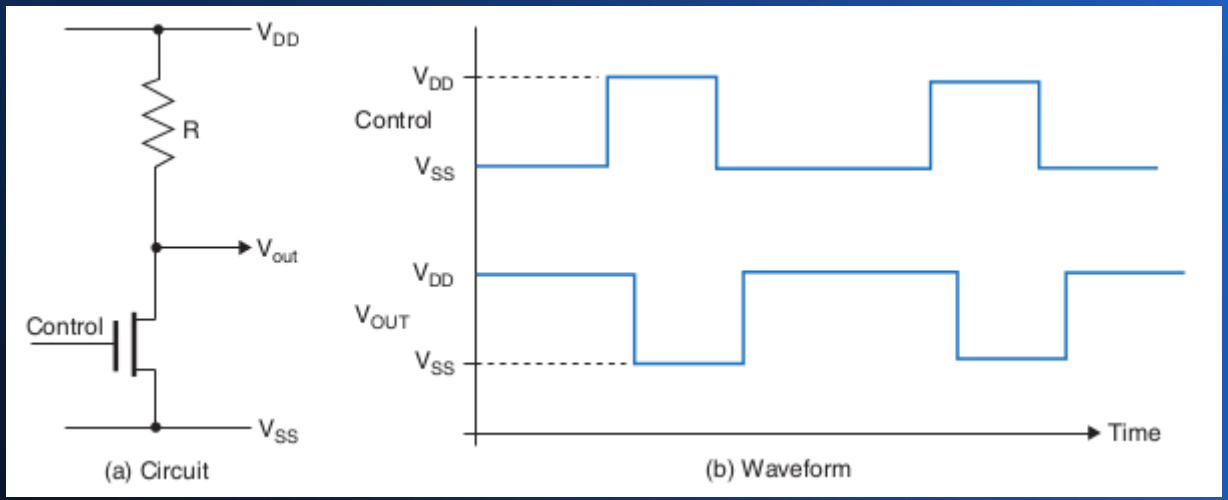
Enhancement-mode MOSFETs are the most widely used member of the FET family

ENHANCEMENT-MODE MOSFETS

The term "enhancement mode" refers to the increase of conductivity with increase in oxide field that adds carriers to the channel, also referred to as the inversion layer.

The channel can contain electrons (called an nMOSFET or nMOS), or holes (called a pMOSFET or pMOS), opposite in type to the substrate, so nMOS is made with a p-type substrate, and pMOS with an n-type substrate.


V_{DD}
R
V_{out}
Switch
V_{SS}
(a) Circuit
Closed
Switch
Open
V_{DD}
V_{OUT}
V_{SS}
Time
(b) Waveform


V_{DD}
R
V_{out}
Control
V_{SS}
(a) Circuit
V_{DD}
Control
V_{SS}
V_{DD}
V_{OUT}
V_{SS}
Time
(b) Waveform

Using Transistors to Build Logic Gates

MOSFETs are the most widely used transistors in the world, finding application in both analogue and digital circuits, especially in today’s digital integrated circuits, the largest of which may literally contain billions.

CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor. The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption.

Significant power is only drawn when the transistors in the CMOS device are switching between on and off states.

Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic.

CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

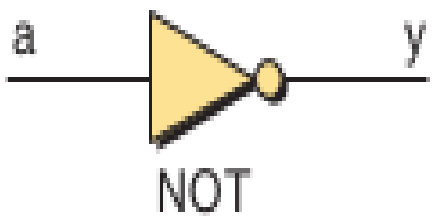
The transition level between high and low logic states is usually half the supply voltage, which means CMOS has superior noise immunity to TTL.

Unlike TTL and its critical +5 volt power supply requirement, CMOS can operate over a wide supply voltage
range, typically +3 to +15 volts.

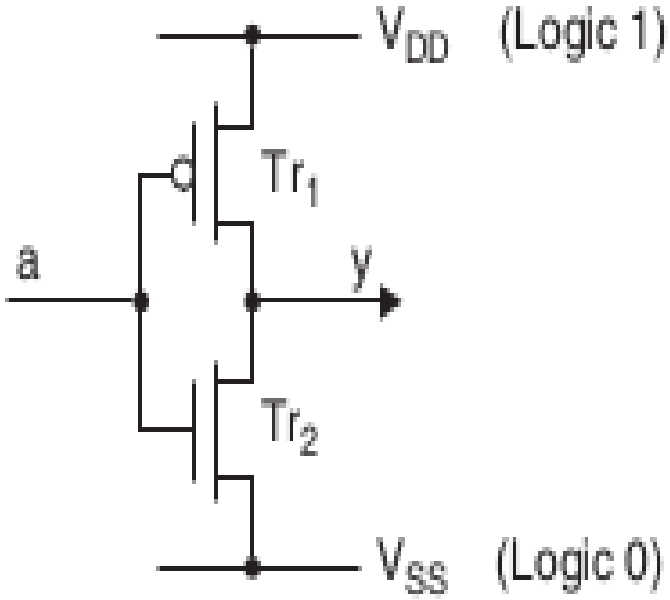
To help differentiate between TTL and CMOS supply voltages, the supply voltage for CMOS is referred to as Vdd and the ground connection is sometimes referred to as Vss.

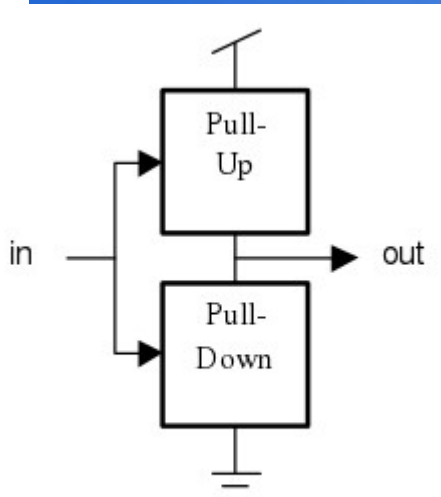
CMOS has a major drawback, however, and that is its susceptibility to damage due to static electricity. CMOS devices are constructed by placing several thin layers atop a silicon substrate, and these layers can be punctured by a static electricity discharge.

CMOS implementation of a NOT gate



a	y
0	1
1	0

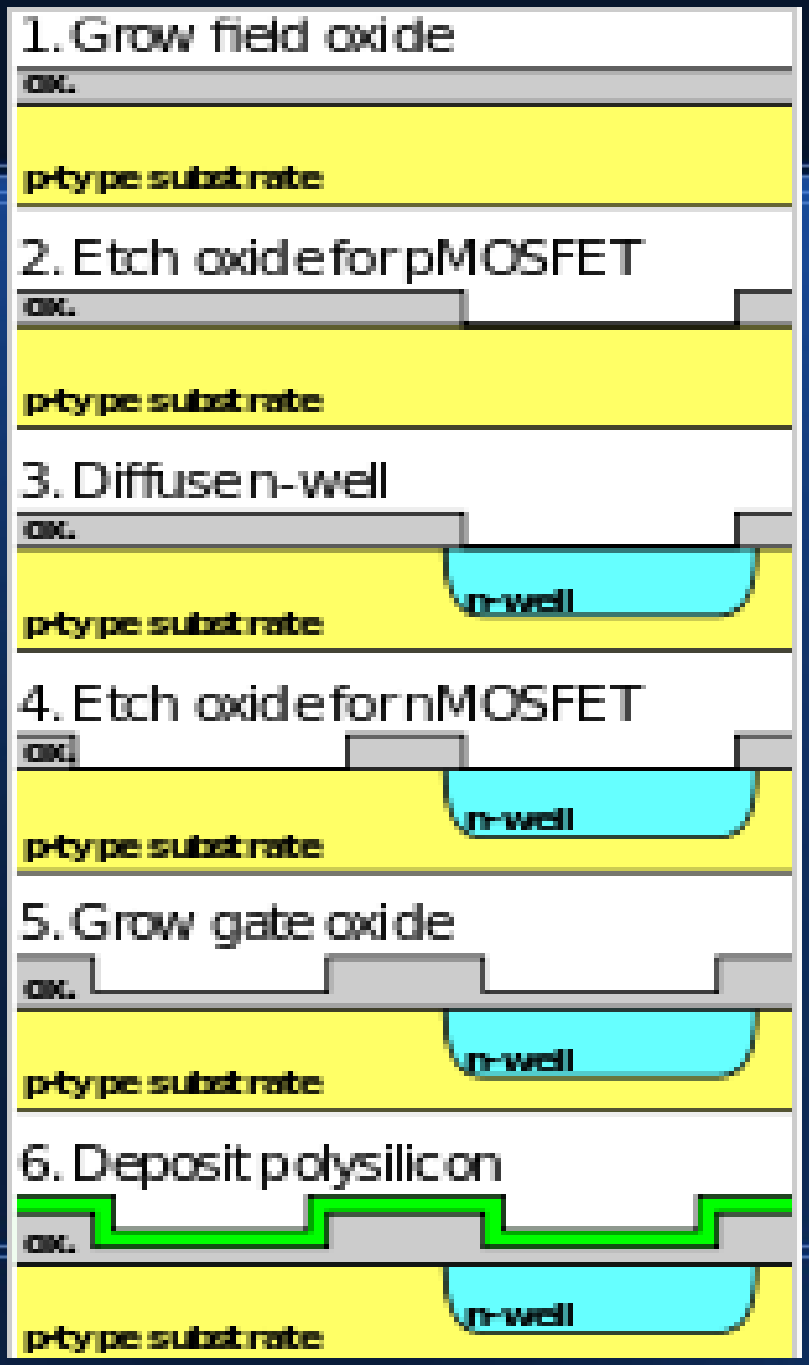


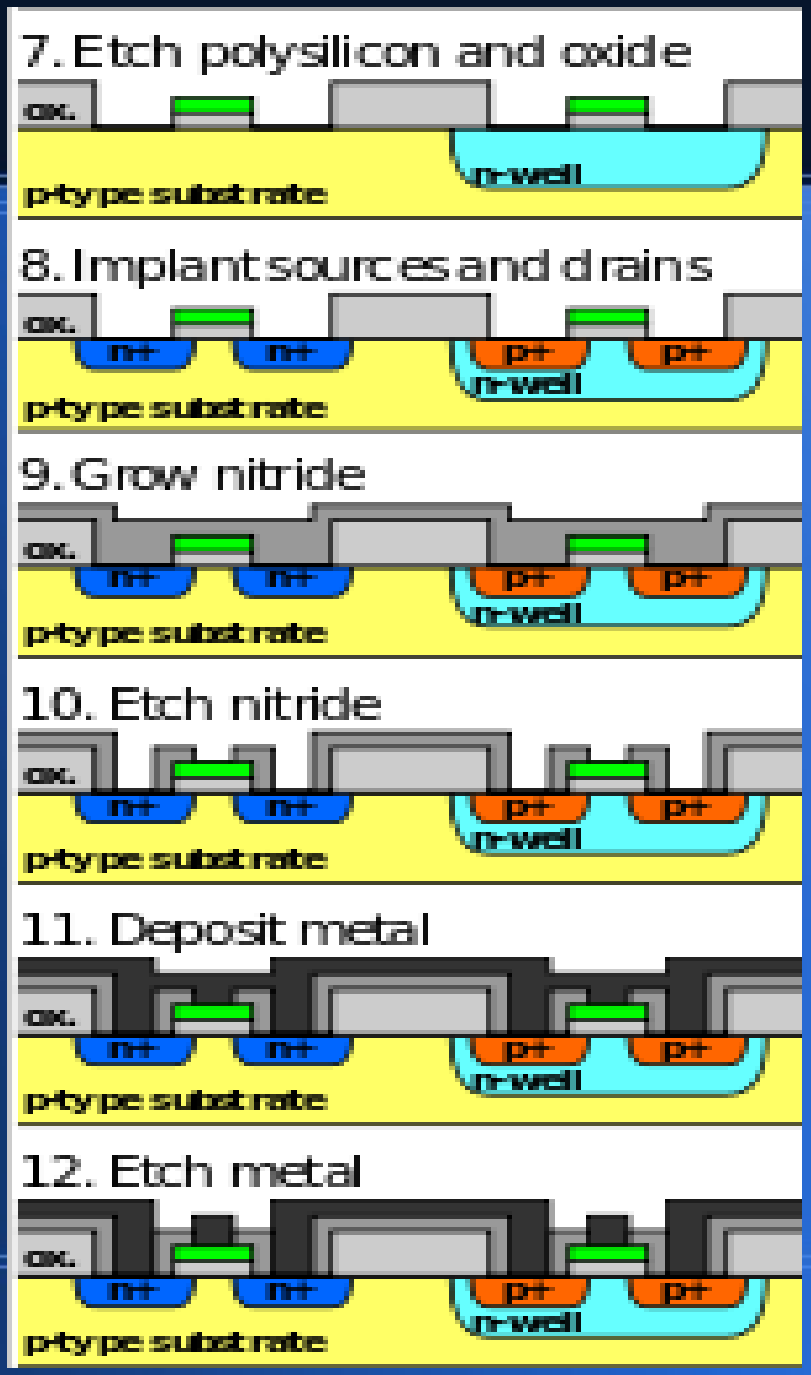


Generic CMOS gate

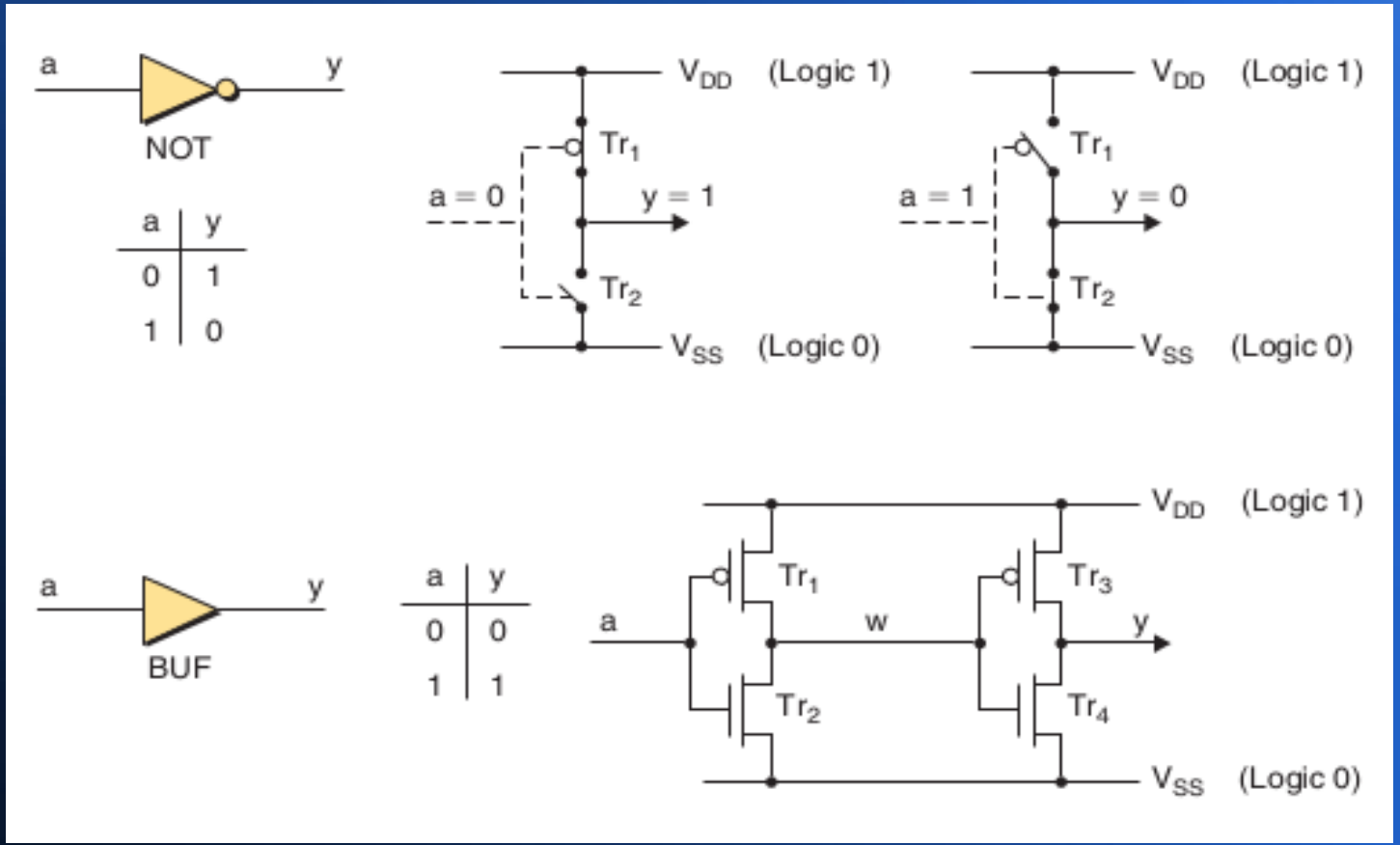
The small circle, or bobble, on the control input of transistor Tr1, indicates a PMOS transistor. The bobble is used to indicate that this transistor has an active-low control, which means that a logic 0 applied to the control input turns the transistor ON and a logic 1 turns it OFF

Simplified process of fabrication of a CMOS inverter on p-type substrate





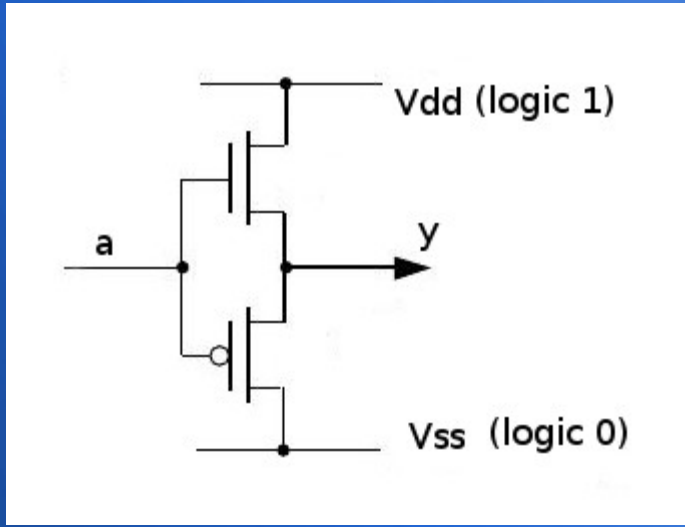
CMOS implementation of a BUF gate



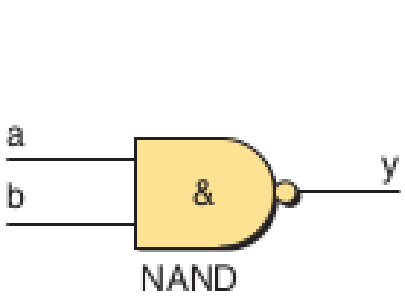
Nothing will happen. Neither transistor will be able to turn on.

The N-channel enhancement-mode transistor (active high) requires its gate to be at a higher voltage than the source (or drain), which can't happen if it's connected to Vcc.

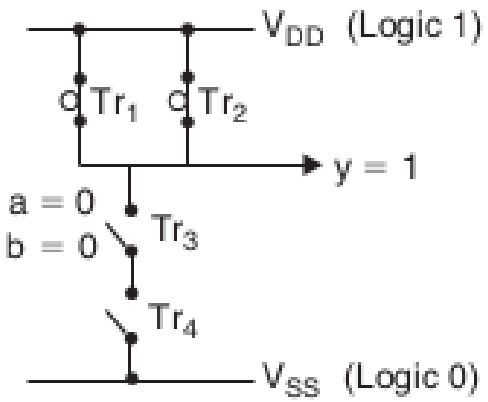
Similarly, the P-channel transistor requires a negative voltage on its gate, which can't happen if it's connected to ground.

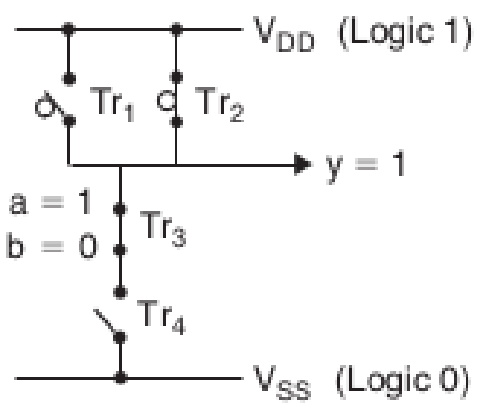


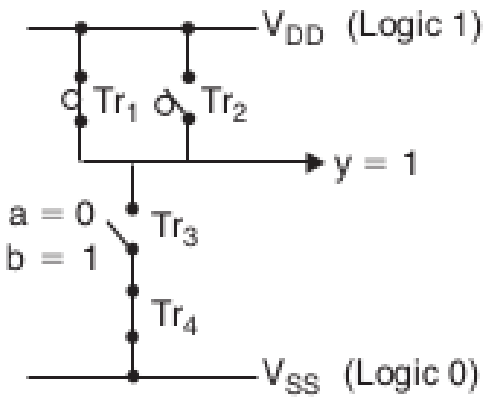
NAND gate's operation represented using switches

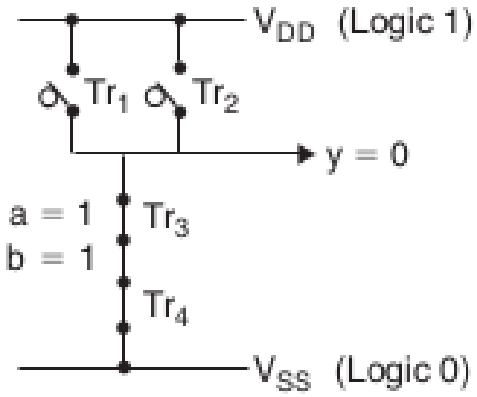


a	b	y
0	0	1
0	1	1
1	0	1
1	1	0



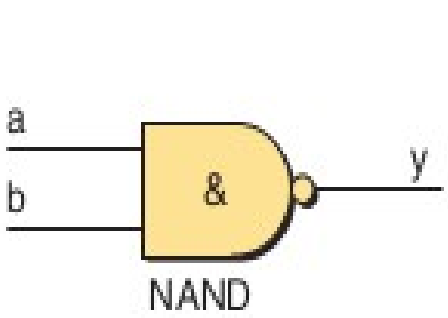




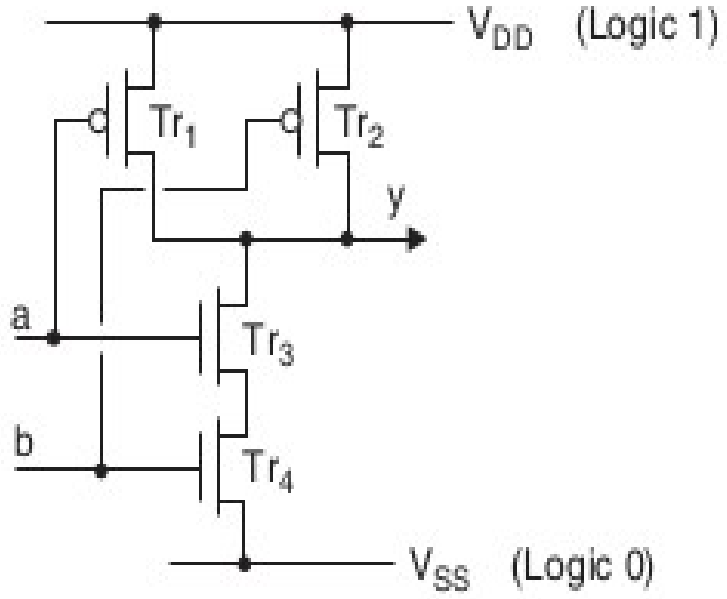


Because the NAND function has functional completeness all logic systems can be converted into NAND gates. This is also true of NOR gates.

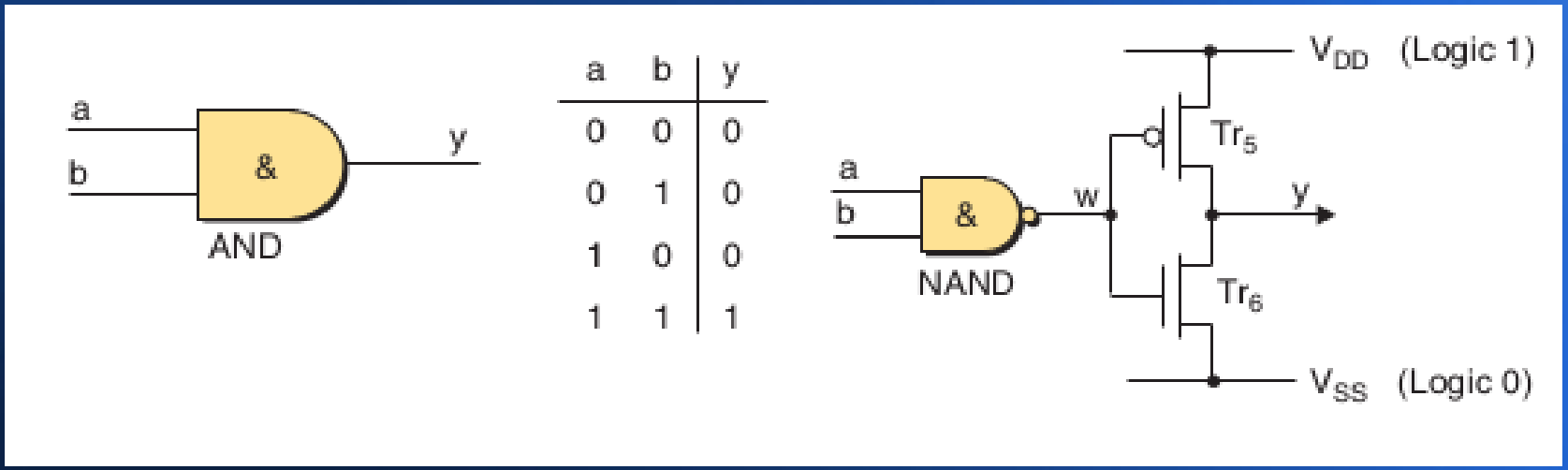
CMOS implementation of a 2-input NAND gate



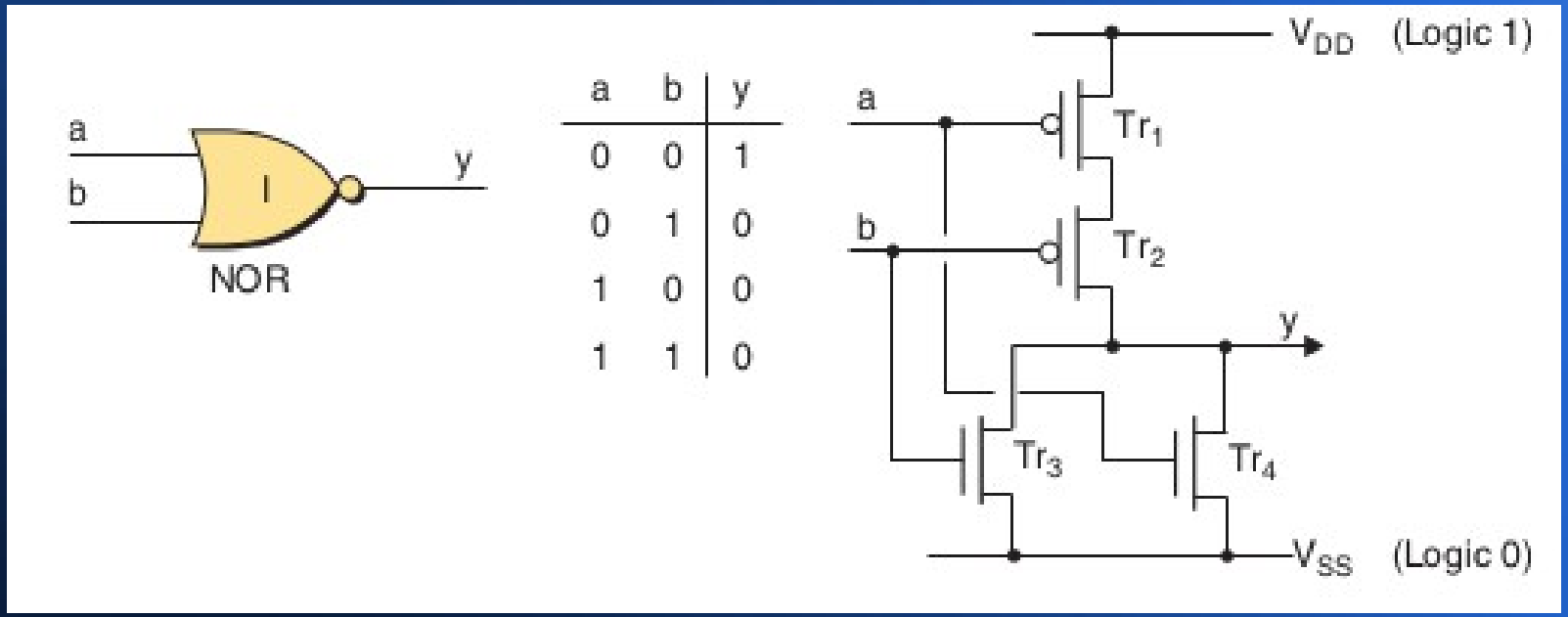
a	b	y
0	0	1
0	1	1
1	0	1
1	1	0



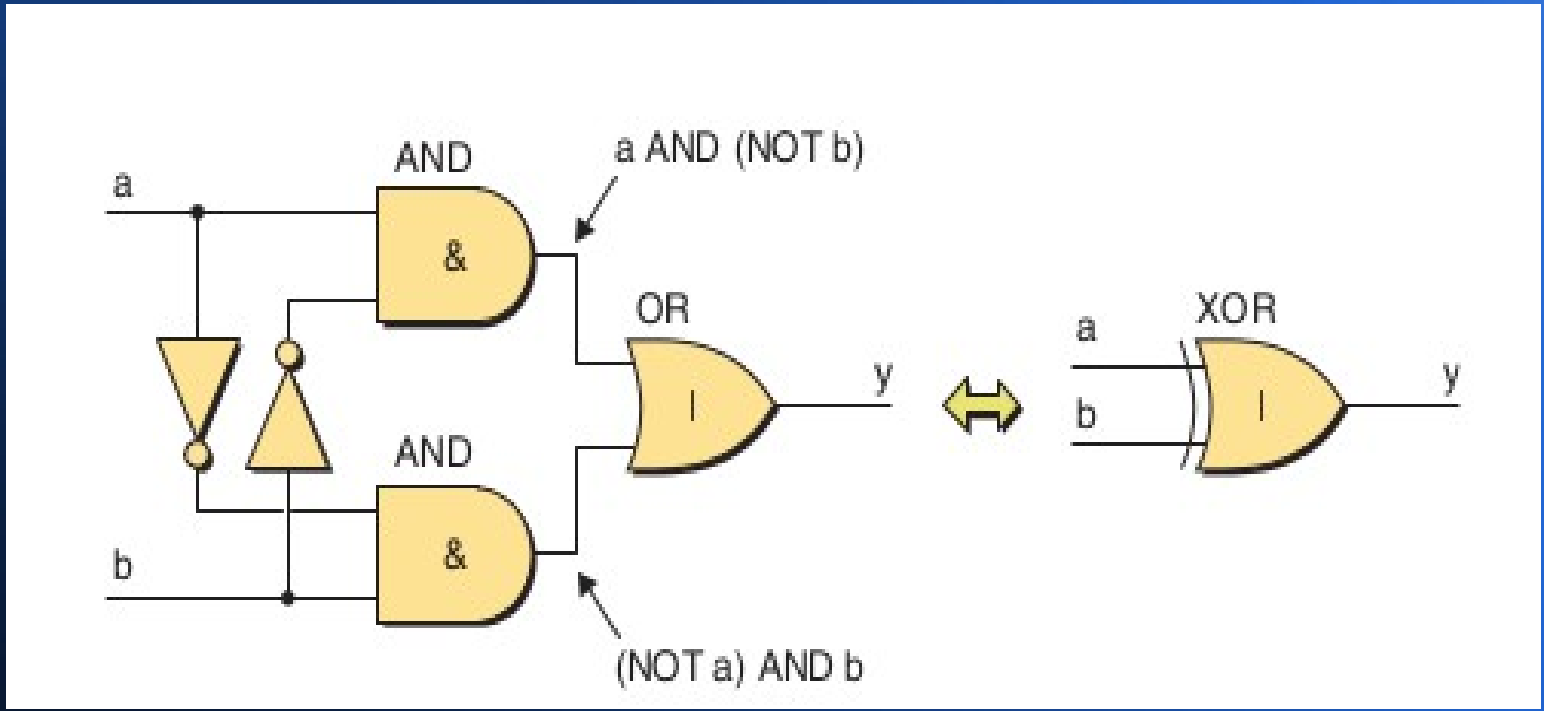
CMOS implementation of a 2-input AND gate



CMOS implementation of a 2-input NOR gate



Implementing a 2-input XOR from NOT, AND, and OR gates



22 transistors - two each for the two NOT gates, six each for the two AND gates, and six more for the OR gate