Rule-Based Defect Identification Module

Functional Design & Operation Report

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1. Purpose of the Rule-Based Module

The rule-based defect identification module serves as the **first decision layer** in the Edge-WaferNet V2+ inspection pipeline. Its primary purpose is to **deterministically identify physical violations in wafer images** using geometry, topology, and signal-consistency rules derived from semiconductor manufacturing principles.

Unlike data-driven models, this module operates without learning or statistical inference. It provides **explainable, low-latency, and power-efficient defect detection**, making it suitable for real-time deployment on edge hardware in semiconductor fabrication environments.

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2. Design Philosophy

The rule engine is designed around the following principles:

1. **Physics Awareness**
   All decisions are based on known physical and geometric properties of semiconductor layouts.
2. **Determinism and Explainability**
   Every defect decision can be traced to a specific violated rule.
3. **Fail-Safe Operation**
   The module is intentionally conservative, preferring to flag uncertainty rather than incorrectly classifying a defect.
4. **Compute Efficiency**
   Operations rely on classical image processing and integer arithmetic, avoiding heavy compute or memory usage.

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3. Input and Output Specification

Input

- Grayscale wafer or die image
- Resolution: 28×28 (post-preprocessing)
- Pixel values normalized to reflect material density or electrical continuity

Output

One of three deterministic states:

- **CLEAN** – No physical violation detected
- **DEFECT** – Clear rule violation detected
- **AMBIGUOUS** – Potential irregularity requiring further verification

This output does **not** assign defect class labels.

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4. Preprocessing Stage

Before rule evaluation, each image undergoes minimal preprocessing to stabilize signal interpretation:

- **Median Filtering (3×3)**
  Removes isolated sensor noise without altering edge geometry.
- **Resolution Normalization**
  Ensures consistent spatial scale for geometric analysis.

This preprocessing is intentionally lightweight to preserve physical structures.

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5. Rule Set Description (A–E)

The rule engine applies a **sequential rule evaluation pipeline**, where each rule targets a specific category of physical defects commonly observed in semiconductor manufacturing.

Rule A: Connectivity Violations (Bridges & Opens)

Objective:
Detect unintended electrical connections (bridges) or broken conductive paths (opens).

Method:

- Perform edge detection to isolate conductive paths
- Compute connected components on the edge map
- Analyze component count and distribution

Rationale:
Well-formed layouts exhibit predictable connectivity. Excessive or fragmented components indicate structural failure.

Decision Logic:

- Abnormally high number of connected components → **DEFECT**

Rule B: Crack and Fracture Detection

Objective:
Identify long, thin discontinuities caused by mechanical stress or thermal mismatch.

Method:

- Skeletonize detected edges to reduce structures to 1-pixel width
- Measure cumulative skeleton length

Rationale:
Cracks manifest as extended linear paths that differ significantly from designed geometries.

Decision Logic:

- Skeleton length exceeding empirical threshold → **DEFECT**

Rule C: CMP Scratch Detection

Objective:
Detect surface scratches introduced during Chemical Mechanical Planarization.

Method:

- Compute horizontal and vertical image gradients
- Analyze dominant gradient orientation across the image

Rationale:
CMP scratches produce strong directional gradients inconsistent with normal layout patterns.

Decision Logic:

- Dominant unidirectional gradient → **AMBIGUOUS**

(This rule intentionally escalates rather than directly flags defects due to visual similarity with some valid structures.)

Rule D: Line Edge Roughness (LER) Detection

Objective:
Identify irregular edge waviness caused by lithography or etching instabilities.

Method:

- Measure positional variance of detected edges
- Compute statistical dispersion of edge coordinates

Rationale:
Manufactured edges should be smooth and consistent at the given scale.

Decision Logic:

- Edge variance exceeding tolerance → **DEFECT**

Rule E: Via and Contact Deformation Detection

Objective:
Detect malformed vias, including elongation, collapse, or misalignment.

Method:

- Extract contours from edge map
- Compute bounding box aspect ratio for each via candidate

Rationale:
Vias are designed to be approximately symmetric. Deviation from expected aspect ratio indicates manufacturing failure.

Decision Logic:

- Aspect ratio outside acceptable range → **DEFECT**

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6. Decision Flow and Conflict Resolution

Rules are evaluated sequentially. The decision logic follows a **short-circuit strategy**:

1. If any rule returns **DEFECT**, evaluation stops.
2. If no rule flags a defect but uncertainty exists, output **AMBIGUOUS**.
3. Only if all rules pass cleanly is **CLEAN** returned.

This ensures:

- Fast rejection of clear defects
- Safe escalation of uncertain cases
- Zero false “clean” decisions due to rule conflicts

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7. Role in the Hybrid Inspection Pipeline

The rule-based module acts as the **primary defect identification gate**:

- **CLEAN outputs** bypass further processing
- **DEFECT outputs** are forwarded for classification and logging
- **AMBIGUOUS outputs** are escalated to CNN-based pattern analysis and optional autoencoder verification

This significantly reduces:

- CNN inference load
- False positives
- Unnecessary compute on edge hardware

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8. Advantages Over Pure ML Approaches

Aspect	**Rule-Based Module**
Explainability	Fully interpretable
Latency	Sub-millisecond on edge CPUs
Power	Minimal
Robustness	Immune to data drift
Safety	Conservative, fail-safe

The rule engine provides **guarantees that learned models cannot**, particularly in safety-critical manufacturing contexts.

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9. Limitations and Scope

- Rules do not assign semantic defect labels

- Performance depends on image scale consistency
- Novel defect types may appear as ambiguous

These limitations are intentionally addressed by downstream ML modules.

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10. Conclusion

The rule-based defect identification module forms the **foundation of the Edge-WaferNet V2+ system**, providing deterministic, explainable, and efficient detection of physical violations in semiconductor wafer images. By encoding domain knowledge directly into the inspection pipeline, it ensures safety, reduces computational load, and enhances overall system reliability when combined with learning-based verification stages.
