1. Assume that a particular device transfers data at an average of 32 kB/s on a continuous basis. Determine what fraction of the processor time is consumed by this I/O device using interrupt-driven I/O in each of the following cases.

   (a) First assume that the device interrupts for every byte and that interrupt processing takes 20 µs. This includes the overhead of setting up the interrupt service procedure (ISP) and returning from the ISP, as well as the 4 µs it takes to transfer one byte from the controller of the device.

   (b) Next assume that the controller of the device has two 16-byte buffers and it interrupts the processor whenever one of the buffers is full.

   (c) Assume, in addition to the buffers, that the processor is equipped with a block transfer I/O instruction which speeds up the transfer of a byte to 2 µs.

2. A 2 GHz processor provides an instruction for loading a string of bytes from memory to an internal cache. The fetching and decoding of the instruction takes 10 clock cycles. Thereafter, it takes 5 clock cycles to transfer each byte.

   (a) Determine the length (in seconds) of the instruction cycle for the case of a string of 64 bytes.

   (b) What is the worst-case delay for acknowledging an interrupt if the instruction is non-interruptable?

(c) Repeat the previous item assuming that the instruction can be interrupted at the beginning of each byte transfer.