

1. Assume that a particular device transfers data at an average of 32 kB/s on a continuous basis. Determine what fraction of the processor time is consumed by this I/O device using interrupt-driven I/O in each of the following cases.

- (a) First assume that the device interrupts for every byte and that interrupt processing takes 20 μ s. This includes the overhead of setting up the interrupt service procedure (ISP) and returning from the ISP, as well as the 4 μ s it takes to transfer one byte from the controller of the device.

$$32\,000\text{ B/s} = 32\text{ kB/s} = \text{Average data transfer}$$

$$2 \times 10^{-5}\text{ s} = 20\text{ }\mu\text{s} = \text{Interrupt time}$$

$$32000 \times (2 \times 10^{-5}) = 0.64$$

$$0.64 = 64\% = 64/100 = 16/25$$

- (b) Next assume that the controller of the device has two 16-byte buffers and it interrupts the processor whenever one of the buffers is full.

$$32\,000\text{ B/s} = 32\text{ kB/s} = \text{Average transfer}$$

$$4 \times 10^{-6}\text{ s} = 4\text{ }\mu\text{s} = \text{transfer time for 1 byte}$$

$$1.6 \times 10^{-5}\text{ s} = 16\text{ }\mu\text{s} = \text{ISP time}$$

$$16\text{ B} = \text{Buffer size}$$

$$2 = \# \text{ of buffers}$$

$$(\text{Average buffer transfer}) = (\text{Average transfer}) \div (\# \text{ of buffers})$$

$$16000 = 32000 \div 2$$

$$(\text{interrupts per buffer}) = (\text{Average buffer transfer}) \div (\text{Buffer size})$$

$$1000 = 16000 \div 16$$

$$(\# \text{ of interrupts}) = (\# \text{ of interrupts for a buffer}) \times (\# \text{ of buffers})$$

$$2000 = 1000 \times 2$$

$$(\text{time to load a buffer}) = (\text{transfer time for 1 byte}) \times (\text{Buffer size})$$

$$64 = 4 \times 16$$

$$(\text{interrupt time}) = (\text{time to load a buffer}) + (\text{ISP time})$$

$$8 \times 10^{-5} = 80 = 64 + 16$$

$$(\text{percentage for interrupt}) = (\# \text{ of interrupts}) \times (\text{interrupt time})$$

$$0.16 = 2000 \times (8 \times 10^{-5})$$

$$0.16 = 16\% = \frac{16}{100} = \frac{4}{25}$$

- (c) Assume, in addition to the buffers, that the processor is equipped with a block transfer I/O instruction which speeds up the transfer of a byte to $2\text{ }\mu\text{s}$.

$$32\,000\text{ B/s} = 32\text{ kB/s} = \text{Average transfer}$$

$$2 \times 10^{-6}\text{ s} = 2\text{ }\mu\text{s} = \text{transfer time for 1 byte}$$

$$1.6 \times 10^{-5}\text{ s} = 16\text{ }\mu\text{s} = \text{ISP time}$$

$$16\text{ B} = \text{Buffer size}$$

$$2 = \# \text{ of buffers}$$

$$(\text{Average buffer transfer}) = (\text{Average transfer}) \div (\# \text{ of buffers})$$

$$16000 = 32000 \div 2$$

$$(\text{interrupts per buffer}) = (\text{Average buffer transfer}) \div (\text{Buffer size})$$

$$1000 = 16000 \div 16$$

$$(\# \text{ of interrupts}) = (\# \text{ of interrupts for a buffer}) \times (\# \text{ of buffers})$$

$$2000 = 1000 \times 2$$

$$(\text{time to load a buffer}) = (\text{transfer time for 1 byte}) \times (\text{Buffer size})$$

$$32 = 2 \times 16$$

$$(\text{interrupt time}) = (\text{time to load a buffer}) + (\text{ISP time})$$

$$4.8 \times 10^{-5} = 48 = 32 + 16$$

$$(\text{percentage for interrupt}) = (\# \text{ of interrupts}) \times (\text{interrupt time})$$

$$0.096 = 2000 \times (4.8 \times 10^{-5})$$

$$0.096 = 9.6\% = \frac{9.6}{100} = \frac{12}{125}$$

2. A 2 GHz processor provides an instruction for loading a string of bytes from memory to an internal cache. The fetching and decoding of the instruction takes 10 clock cycles. Thereafter, it takes 5 clock cycles to transfer each byte.
- (a) Determine the length (in seconds) of the instruction cycle for the case of a string of 64 bytes.

$$\begin{aligned} \text{cycles/s} &= \text{Hz} \\ 2 \times 10^9 \text{ Hz} &= 2\,000\,000\,000 \text{ Hz} = 2 \text{ GHz} \\ 10 \text{ Hz} &= \text{fetching and decoding instruction} \\ 5 \text{ Hz} &= \text{byte transfer} \\ 64 \text{ B} &= \text{string} \\ \\ (\# \text{ of cycles for string}) &= (\text{byte transfer}) \times (\text{bytes}) \\ 320 &= 64 \times 5 \\ \\ (\text{total cycles}) &= (\text{fetching and decoding}) + (\# \text{ of cycles for string}) \\ 330 &= 10 + 320 \\ \\ (\text{length (in seconds)}) &= (\text{total cycles}) \div (2 \text{ GHz}) \\ 1.65 \times 10^{-7} \text{ s} &= 0.000000165 = 330 \div (2 \times 10^9) \end{aligned}$$

- (b) What is the worst-case delay for acknowledging an interrupt if the instruction is non-interruptable?

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- (c) Repeat the previous item assuming that the instruction can be interrupted at the beginning of each byte transfer.

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