

1. Assume that a particular device transfers data at an average of 32 kB/s on a continuous basis. Determine what fraction of the processor time is consumed by this I/O device using interrupt-driven I/O in each of the following cases.

- (a) First assume that the device interrupts for every byte and that interrupt processing takes 20  $\mu$ s. This includes the overhead of setting up the interrupt service procedure (ISP) and returning from the ISP, as well as the 4  $\mu$ s it takes to transfer one byte from the controller of the device.

$$32\,000\text{ B/s} = 32\text{ kB/s} = \text{Average data transfer}$$

$$2 \times 10^{-5}\text{ s} = 20\text{ }\mu\text{s} = \text{Interrupt time}$$

$$32000 \times (2 \times 10^{-5}) = 0.64$$

$$0.64 = 64\% = 64/100 = 16/25$$

- (b) Next assume that the controller of the device has two 16-byte buffers and it interrupts the processor whenever one of the buffers is full.

Assumption: It can transfer all bytes from the buffer in the same amount of time as transferring one at a time from the previous question.

$$32\,000\text{ B/s} = 32\text{ kB/s} = \text{Average data transfer}$$

$$2 \times 10^{-5}\text{ s} = 20\text{ }\mu\text{s} = \text{Interrupt time}$$

$$16\text{ B} = \text{Buffer size}$$

$$2 = \# \text{ of buffers}$$

$$32000 \div 16 = 2000$$

$$2000 \times 2 = 4000$$

$$4000 \times (2 \times 10^{-5}) = 0.08$$

$$0.08 = 8\% = 8/100 = 4/50 = 2/25$$

- (c) Assume, in addition to the buffers, that the processor is equipped with a block transfer I/O instruction which speeds up the transfer of a byte to  $2\text{ }\mu\text{s}$ .

$$\begin{aligned}2\text{ }\mu\text{s} &= \text{Transfer time} \\16\text{ }\mu\text{s} &= \text{ISP setup time} \\32\,000\text{ B/s} &= 32\text{ kB/s} = \text{Average data transfer} \\1.8 \times 10^{-5}\text{ s} &= 18\text{ }\mu\text{s} = 16\text{ }\mu\text{s} + 2\text{ }\mu\text{s} = \text{Interrupt time} \\16\text{ B} &= \text{Buffer size} \\2 &= \# \text{ of buffers} \\[10pt]32000 \div 16 &= 2000 \\2000 \times 2 &= 4000 \\4000 \times (1.8 \times 10^{-5}) &= 0.072 \\[10pt]0.072 &= 7.2\% = 7.2/100 = 9/125\end{aligned}$$

2. A 2 GHz processor provides an instruction for loading a string of bytes from memory to an internal cache. The fetching and decoding of the instruction takes 10 clock cycles. Thereafter, it takes 5 clock cycles to transfer each byte.

- (a) Determine the length (in seconds) of the instruction cycle for the case of a string of 64 bytes.

□

- (b) What is the worst-case delay for acknowledging an interrupt if the instruction is non-interruptable?

□

- (c) Repeat the previous item assuming that the instruction can be interrupted at the beginning of each byte transfer.

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