1. Assume that a particular device transfers data at an average of 32 kB/s on a continuous basis. Determine what fraction of the processor time is consumed by this I/O device using interrupt-driven I/O in each of the following cases.

   (a) First assume that the device interrupts for every byte and that interrupt processing takes 20 µs. This includes the overhead of setting up the interrupt service procedure (ISP) and returning from the ISP, as well as the 4 µs it takes to transfer one byte from the controller of the device.

   $32\,000\,\mathrm{B/s} = 32\,\mathrm{kB/s} =$ Average data transfer
   $2 \times 10^{-5}\,\mathrm{s} = 20\,\mu\mathrm{s} =$ Interrupt time

   $32000 \times (2 \times 10^{-5}) = 0.64$
   $0.64 = 64\,\% = {}^{64}/_{100} = {}^{16}/_{25}$

(b) Next assume that the controller of the device has two 16-byte buffers and it interrupts the processor whenever one of the buffers is full.

$32\,000\,\mathrm{B/s} = 32\,\mathrm{kB/s}$ = Average transfer
$4 \times 10^{-6}\,\mathrm{s} = 4\,\mu\mathrm{s}$ = transfer time for 1 byte
$1.6 \times 10^{-5}\,\mathrm{s} = 16\,\mu\mathrm{s}$ = ISP time
$16\,\mathrm{B}$ = Buffer size
2 = # of buffers

(Average buffer transfer) = (Average transfer) ÷ (# of buffers)
$16000 = 32000 \div 2$

(interrupts per buffer) = (Average buffer transfer) ÷ (Buffer size)
$1000 = 16000 \div 16$

(# of interrupts) = (# of interrupts for a buffer) × (# of buffers)
$2000 = 1000 \times 2$

(time to load a buffer) = (transfer time for 1 byte) × (Buffer size)
$64 = 4 \times 16$

(interrupt time) = (time to load a buffer) + (ISP time)
$8 \times 10^{-5} = 80 = 64 + 16$

(percentage for interrupt) = (# of interrupts) × (interrupt time)
$0.16 = 2000 \times (8 \times 10^{-5})$

$0.16 = 16\,\% = {}^{16}/_{100} = {}^{4}/_{25}$

(c) Assume, in addition to the buffers, that the processor is equipped with a block transfer I/O instruction which speeds up the transfer of a byte to 2 µs.

$32\,000\,\mathrm{B/s} = 32\,\mathrm{kB/s}$ = Average transfer
$2 \times 10^{-6}\,\mathrm{s} = 2\,\mu\mathrm{s}$ = transfer time for 1 byte
$1.6 \times 10^{-5}\,\mathrm{s} = 16\,\mu\mathrm{s}$ = ISP time
$16\,\mathrm{B}$ = Buffer size
2 = # of buffers

(Average buffer transfer) = (Average transfer) ÷ (# of buffers)
$16000 = 32000 \div 2$

(interrupts per buffer) = (Average buffer transfer) ÷ (Buffer size)
$1000 = 16000 \div 16$

(# of interrupts) = (# of interrupts for a buffer) × (# of buffers)
$2000 = 1000 \times 2$

(time to load a buffer) = (transfer time for 1 byte) × (Buffer size)
$32 = 2 \times 16$

(interrupt time) = (time to load a buffer) + (ISP time)
$4.8 \times 10^{-5} = 48 = 32 + 16$

(percentage for interrupt) = (# of interrupts) × (interrupt time)
$0.096 = 2000 \times (4.8 \times 10^{-5})$

$0.096 = 9.6\,\% = {}^{9.6}/_{100} = {}^{12}/_{125}$

2. A 2 GHz processor provides an instruction for loading a string of bytes from memory to an internal cache. The fetching and decoding of the instruction takes 10 clock cycles. Thereafter, it takes 5 clock cycles to transfer each byte.

   (a) Determine the length (in seconds) of the instruction cycle for the case of a string of 64 bytes.

   $cycles/\text{s} = \text{Hz}$
   $2 \times 10^9\,\text{Hz} = 2\,000\,000\,000\,\text{Hz} = 2\,\text{GHz}$
   $10\,\text{Hz}$ = fetching and decoding instruction
   $5\,\text{Hz}$ = byte transfer
   $64\,\text{B}$ = string

   (# of cycles for string) = (byte transfer) $\times$ (bytes)
   $320 = 64 \times 5$

   (total cycles) = (fetching and decoding) + (# of cycles for string)
   $330 = 10 + 320$

   (length (in seconds)) = (total cycles) $\div$ (2 GHz)
   $1.65 \times 10^{-7}\,\text{s} = 0.0000001.65 = 330 \div (2 \times 10^9)$

   (b) What is the worst-case delay for acknowledging an interrupt if the instruction is non-interruptable?

   The worst case delay before acknowledging and interrupt, if the the instruction is non-interrupable, is the length of the instruction. So, it is $1.65 \times 10^{-7}\,\text{s}$ assuming that it is $64\,\text{B}$.

(c) Repeat the previous item assuming that the instruction can be interrupted at the beginning of each byte transfer.

The worst case delay case delay for servicing an interrupt if it can happen at the beginning of each byte transfer is immediately after the fetch and decode procedure.

$2 \times 10^9\,\text{Hz} = 2\,000\,000\,000\,\text{Hz} = 2\,\text{GHz}$
$10\,\text{Hz}$ = fetching and decoding instruction

length (in seconds)) = (fetching and decoding) $\div$ (2 GHz)
$5 \times 10^{-9}\,\text{s} = 0.000000005 = 10 \div (2 \times 10^9)$