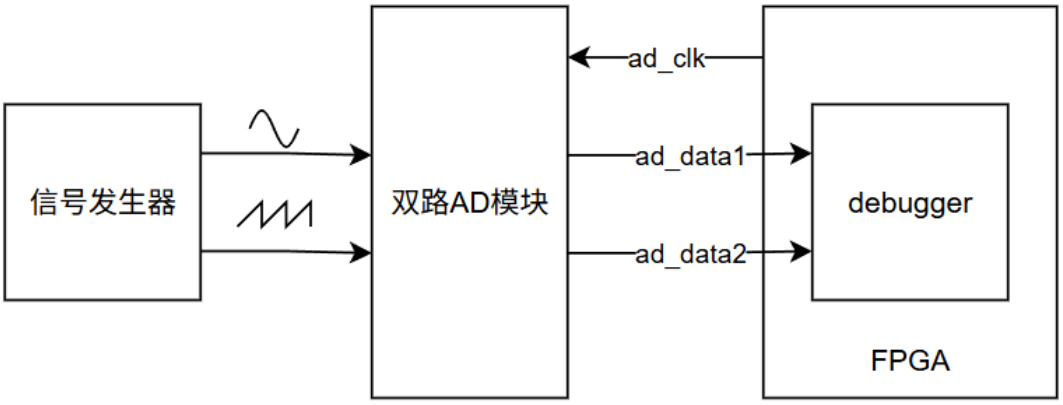
RyanFPGA双路高速AD采集模块 debug实验例程说明

1 实验简介

实验使用信号发生器向我们的双路高速AD采集模块发送各类波形的模拟信号，AD采集模块将其进行模数转换，在FPGA端使用pango debugger工具观察接收的数字波形是否符合信号发生器输出的波形特征。

本实验练习使用硬件为：鹏野嘉途双路AD模块与小眼睛科技盘古50k开发板，AD信号来源为信号发生器；



2 程序设计

使用例程观察实验现象可以直接跳到第3节

实验代码

RyanFPGA双路高速AD采集模块使用的adc芯片为3pa1030，硬件管脚配置为了top bottom模式，模拟信号为单端输入，输入时钟和输出数据的时序图如下，即只需给该adc提供允许范围内的时钟就能得到采样的数字信号。

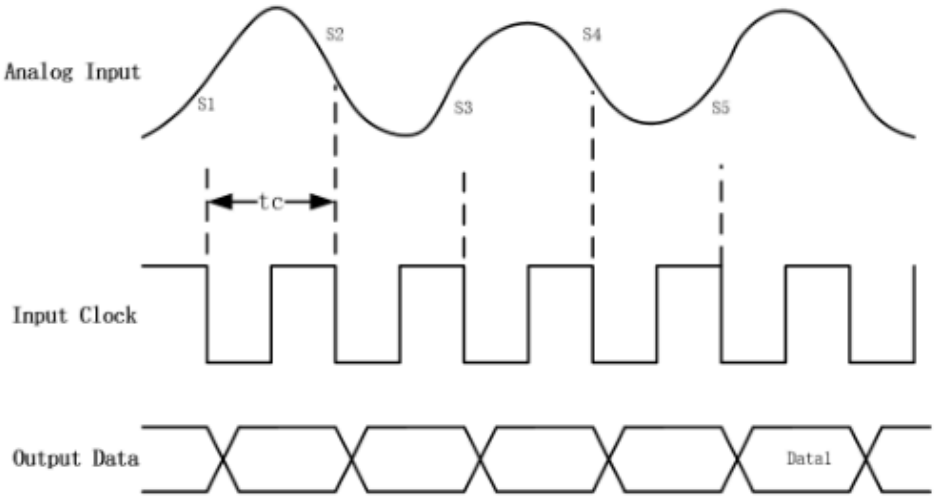


Figure 22. Timing Diagram

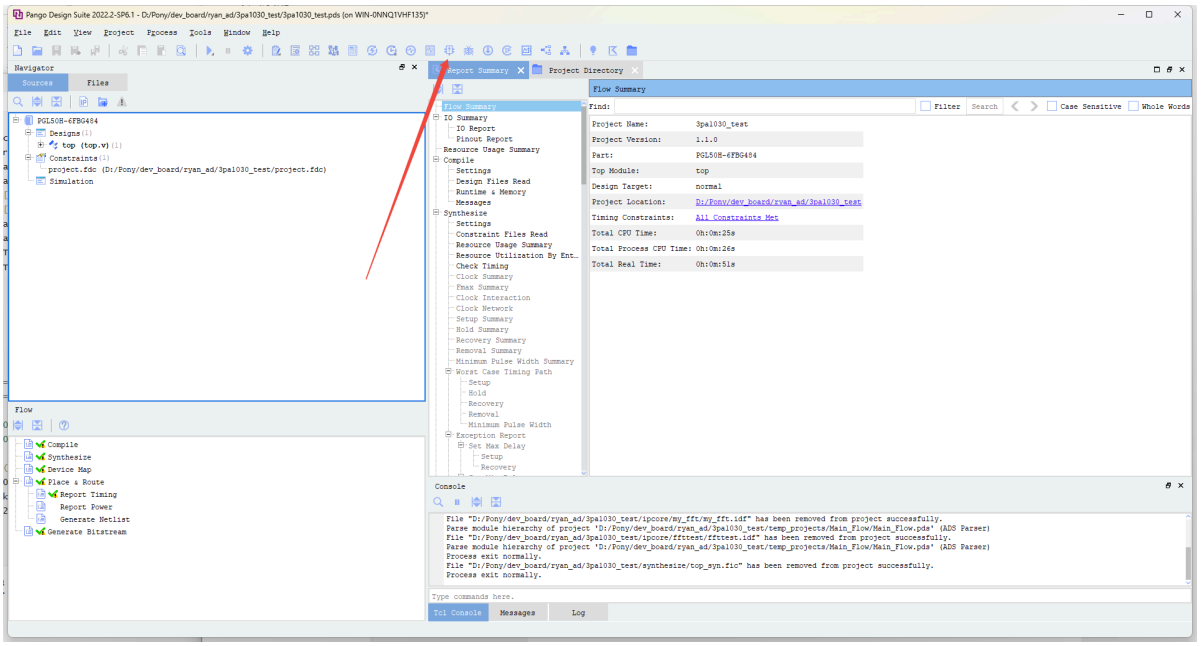
我们的程序中调用pll将fpga输入时钟改变为需要的采样率，再输出给adc，同时对端口信号添加debug语句`/* synthesis PAP_MARK_DEBUG="true" */`

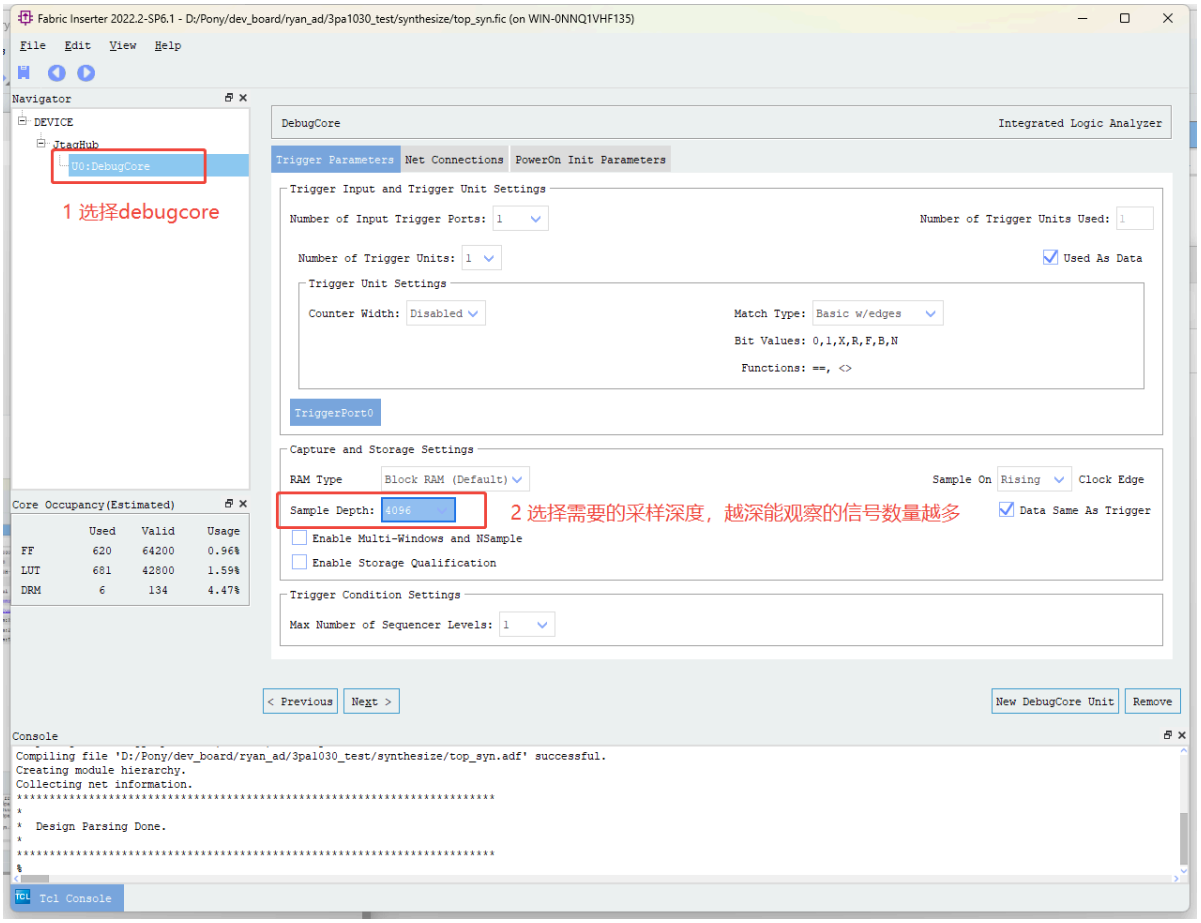
ad1oe、ad2oe为adc的使能信号，低电平有效，这里直接赋0；

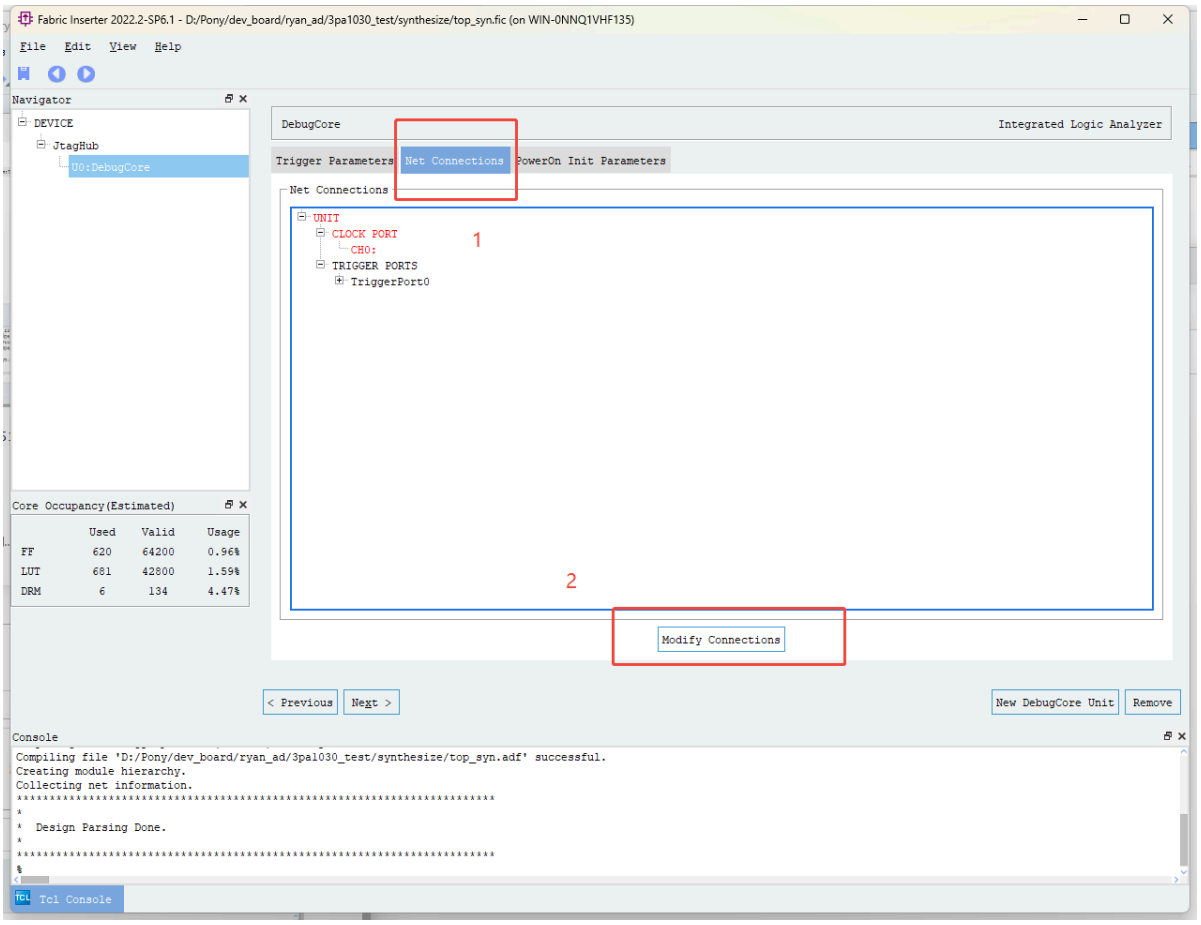
```
module top(
   input  wire clk_50M ,
   input  wire rst_n ,
   output wire ad_clk1 /* synthesis PAP_MARK_DEBUG="true" */,
   output wire ad_clk2 /* synthesis PAP_MARK_DEBUG="true" */,
   input  wire [9:0]ad_data1 /* synthesis PAP_MARK_DEBUG="true" */,
   input  wire [9:0]ad_data2 /* synthesis PAP_MARK_DEBUG="true" */,
   output wire ad1oe /* synthesis PAP_MARK_DEBUG="true" */,
   output wire ad2oe /* synthesis PAP_MARK_DEBUG="true" */,
   input wire OTR1   /* synthesis PAP_MARK_DEBUG="true" */,
   input wire OTR2   /* synthesis PAP_MARK_DEBUG="true" */

   );

wire lock ;
reg  [7:0]cnt ;
wire clk_20M;

assign ad_clk1 = clk_20M ;
assign ad_clk2 = clk_20M ;

assign ad1oe = 0;
assign ad2oe = 0;

ad_clock u_pll (
  .clkin1(clk_50M),        // input
  .pll_lock(lock),    // output
  .clkout0(clk_20M)       // output
);

endmodule
```

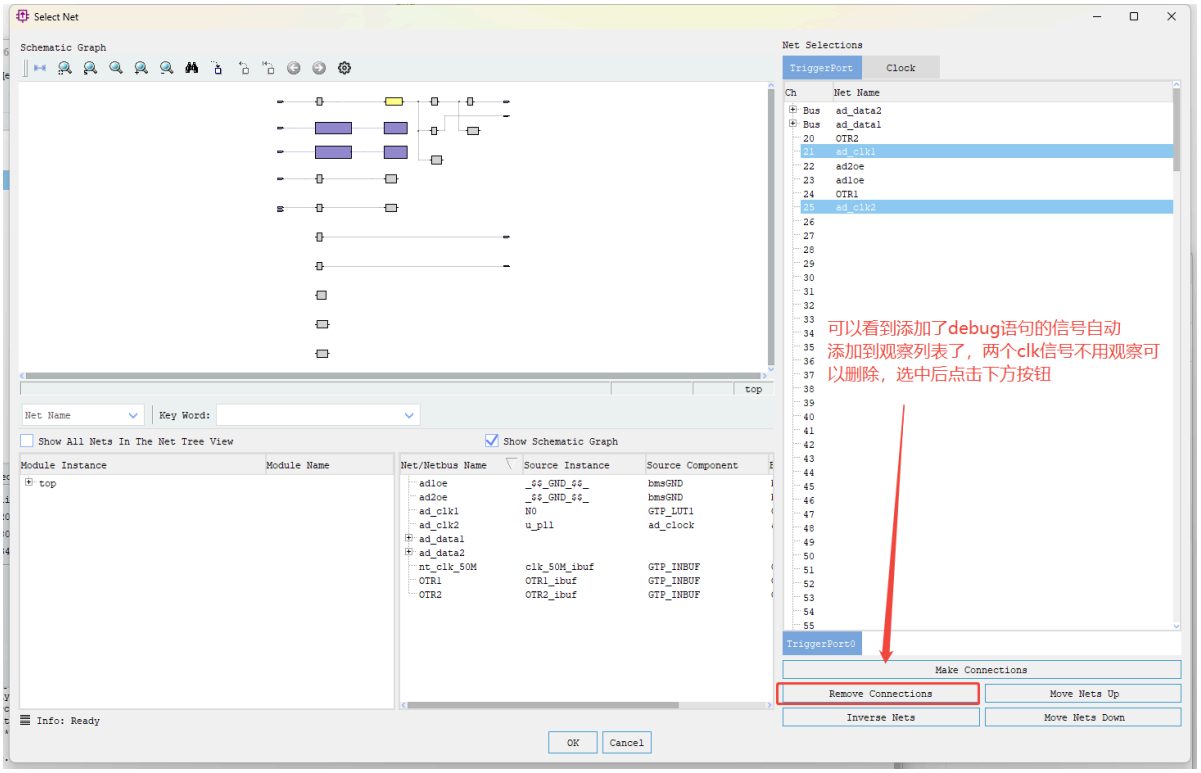
debug核设置

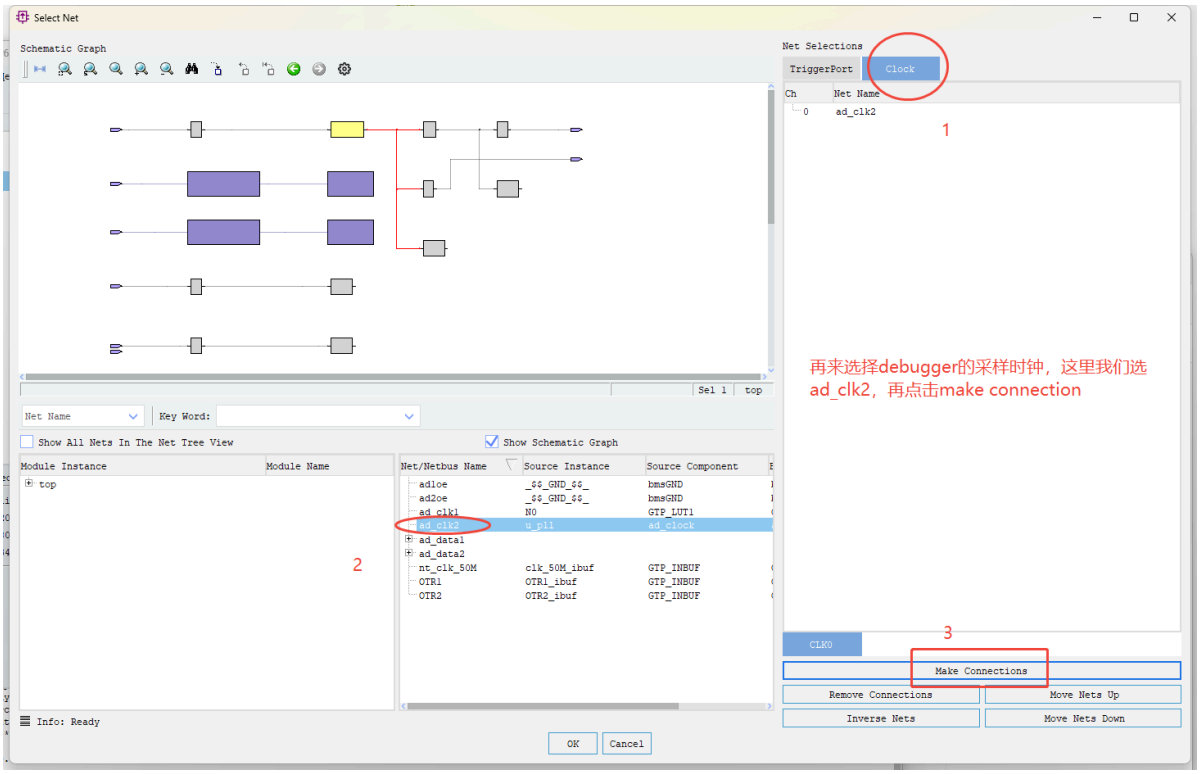
点击inserter工具




Fabric Inserter 2022.2-SP6.1 - D:/Pony/dev_board/ryan_ad/3pa1030_test/synthesize/top_syn.fic (on WIN-0NNQ1VHF135)
File Edit View Help
Navigator
DEVICE
JtagHub
U0:DebugCore
1 选择debugcore
DebugCore
Integrated Logic Analyzer
Trigger Parameters
Net Connections
PowerOn Init Parameters
Trigger Input and Trigger Unit Settings
Number of Input Trigger Ports: 1
Number of Trigger Units Used: 1
Number of Trigger Units: 1
Used As Data
Trigger Unit Settings
Counter Width: Disabled
Match Type: Basic w/edges
Bit Values: 0,1,X,R,F,B,N
Functions: ==, <>
TriggerPort0
Capture and Storage Settings
RAM Type: Block RAM (Default)
Sample On: Rising Clock Edge
Sample Depth: 4096
2 选择需要的采样深度，越深能观察的信号数量越多
Data Same As Trigger
Enable Multi-Windows and NSample
Enable Storage Qualification
Trigger Condition Settings
Max Number of Sequencer Levels: 1
Core Occupancy(Estimated)
Used Valid Usage
FF 620 64200 0.96%
LUT 681 42800 1.59%
DRM 6 134 4.47%
< Previous
Next >
New DebugCore Unit
Remove
Console
Compiling file 'D:/Pony/dev_board/ryan_ad/3pa1030_test/synthesize/top_syn.adf' successful.
Creating module hierarchy.
Collecting net information.
Design Parsing Done.
Tcl Console

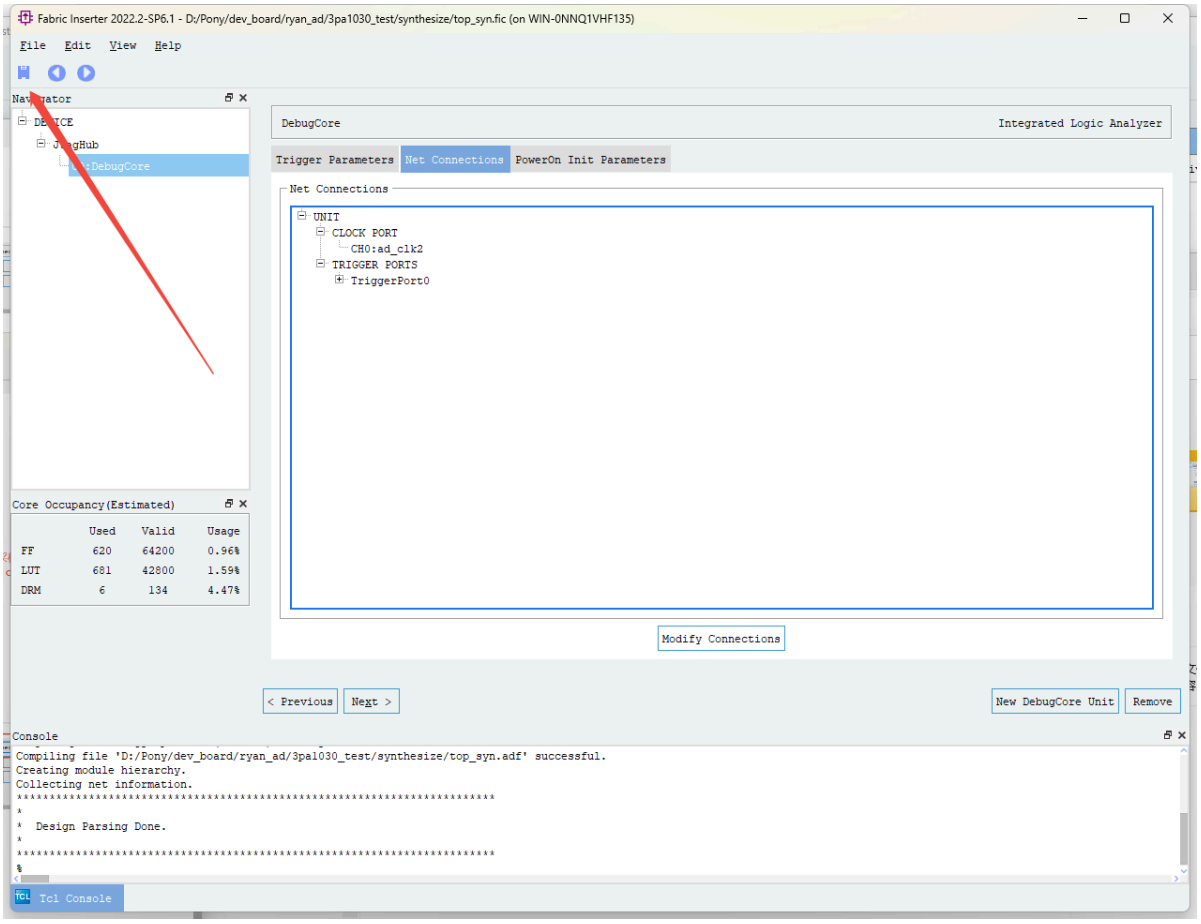

Fabric Inserter 2022.2-SP6.1 - D:/Pony/dev_board/ryan_ad/3pa1030_test/synthesize/top_syn.fic (on WIN-0NNQ1VHF135)
File Edit View Help
Navigator
DEVICE
JtagHub
U0:DebugCore
DebugCore
Integrated Logic Analyzer
Trigger Parameters
Net Connections
PowerOn Init Parameters
Net Connections
UNIT
CLOCK PORT
CH0:
TRIGGER PORTS
TriggerPort0
1
2
Modify Connections
Core Occupancy(Estimated)
Used Valid Usage
FF 620 64200 0.96%
LUT 681 42800 1.59%
DRM 6 134 4.47%
< Previous
Next >
New DebugCore Unit
Remove
Console
Compiling file 'D:/Pony/dev_board/ryan_ad/3pa1030_test/synthesize/top_syn.adf' successful.
Creating module hierarchy.
Collecting net information.
Design Parsing Done.
Tcl Console


Select Net
Schematic Graph
Net Selections
TriggerPort
Clock
Ch
Net Name
Bus ad_data2
Bus ad_data1
20 OTR2
21 ad_clk1
22 ad2oe
23 ad1oe
24 OTR1
25 ad_clk2
可以看到添加了debug语句的信号自动添加到观察列表了，两个clk信号不用观察可以删除，选中后点击下方按钮
Net Name
Key Word:
Show All Nets In The Net Tree View
Show Schematic Graph
Module Instance
Module Name
top
Net/Netbus Name
Source Instance
Source Component
ad1oe _$$_GND_$$_ bmsGND
ad2oe _$$_GND_$$_ bmsGND
ad_clk1 N0 GTP_LUT1
ad_clk2 u_pll ad_clock
ad_data1
ad_data2
nt_clk_50M clk_50M_ibuf GTP_INBUF
OTR1 OTR1_ibuf GTP_INBUF
OTR2 OTR2_ibuf GTP_INBUF
TriggerPort0
Make Connections
Remove Connections
Move Nets Up
Inverse Nets
Move Nets Down
Info: Ready
OK
Cancel



信号选择完毕后点击OK

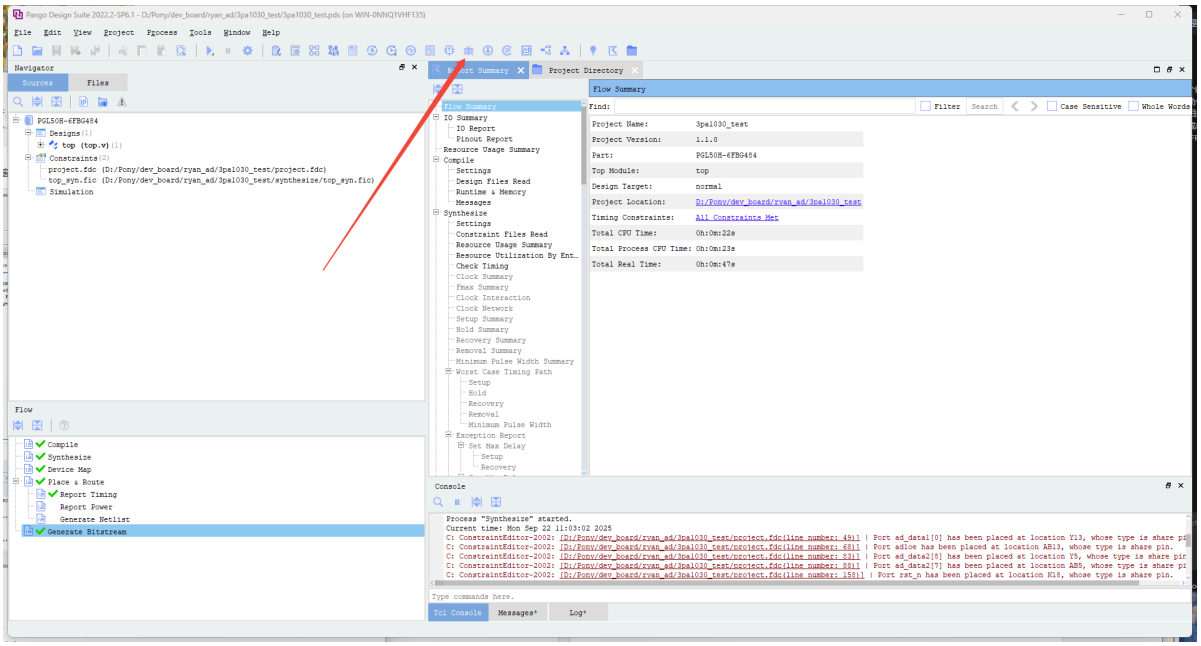
点击保存或ctrl+s保存，然后关闭该窗口



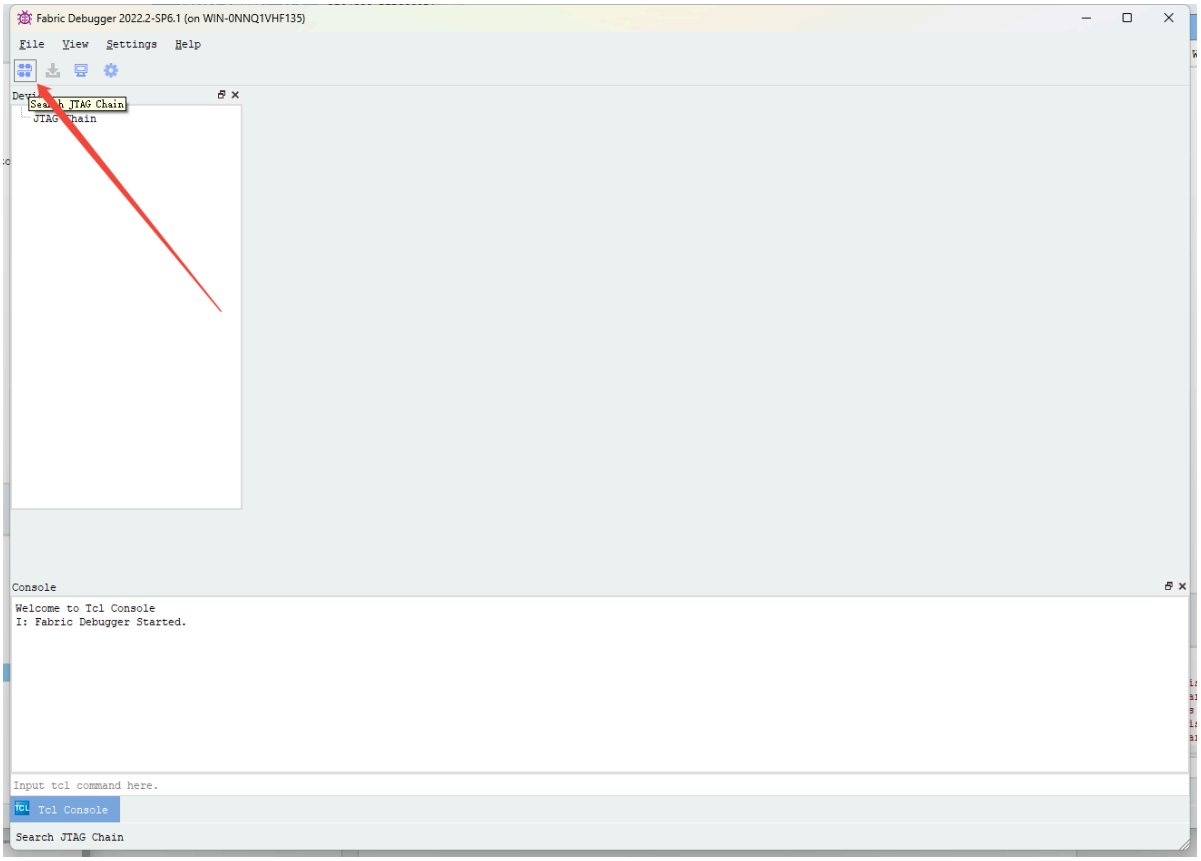
在主界面重新生成bitstream

3 实验现象

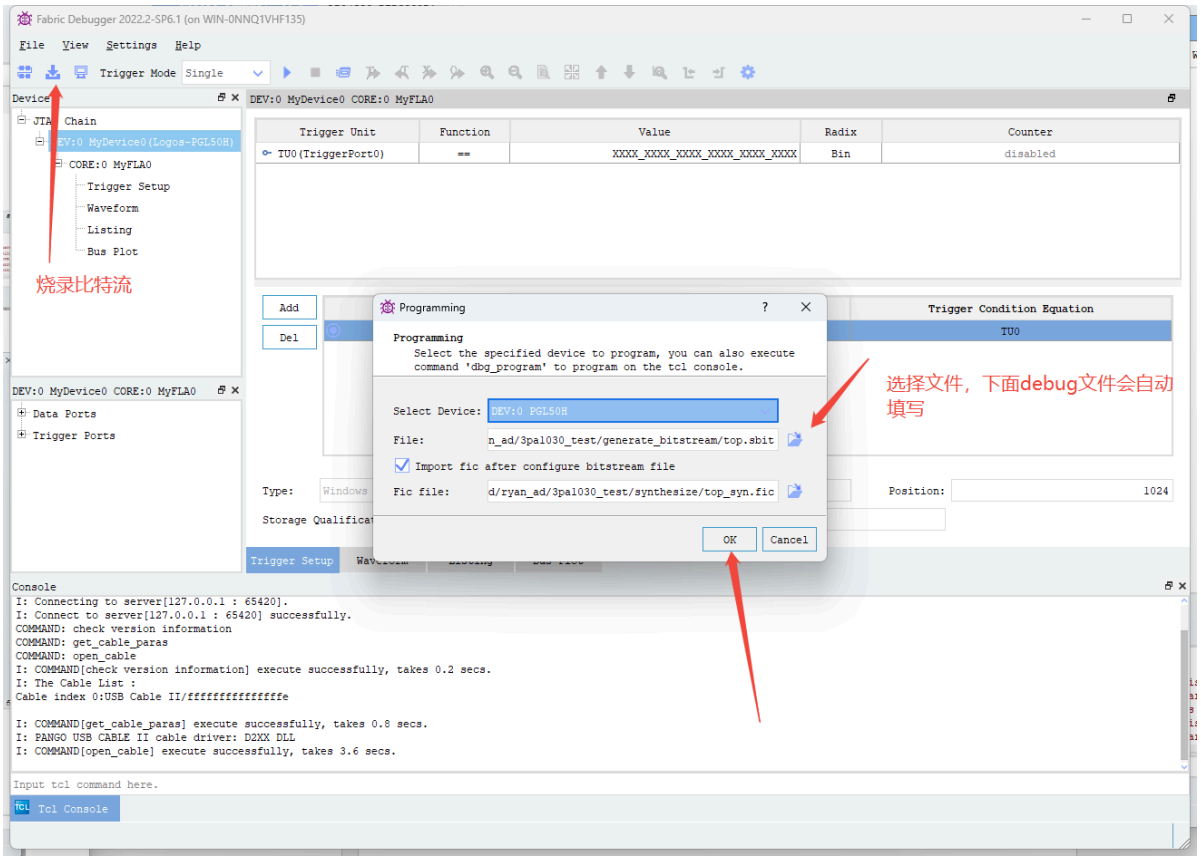
接好模块和jtag后对板子上电，点击debugger工具



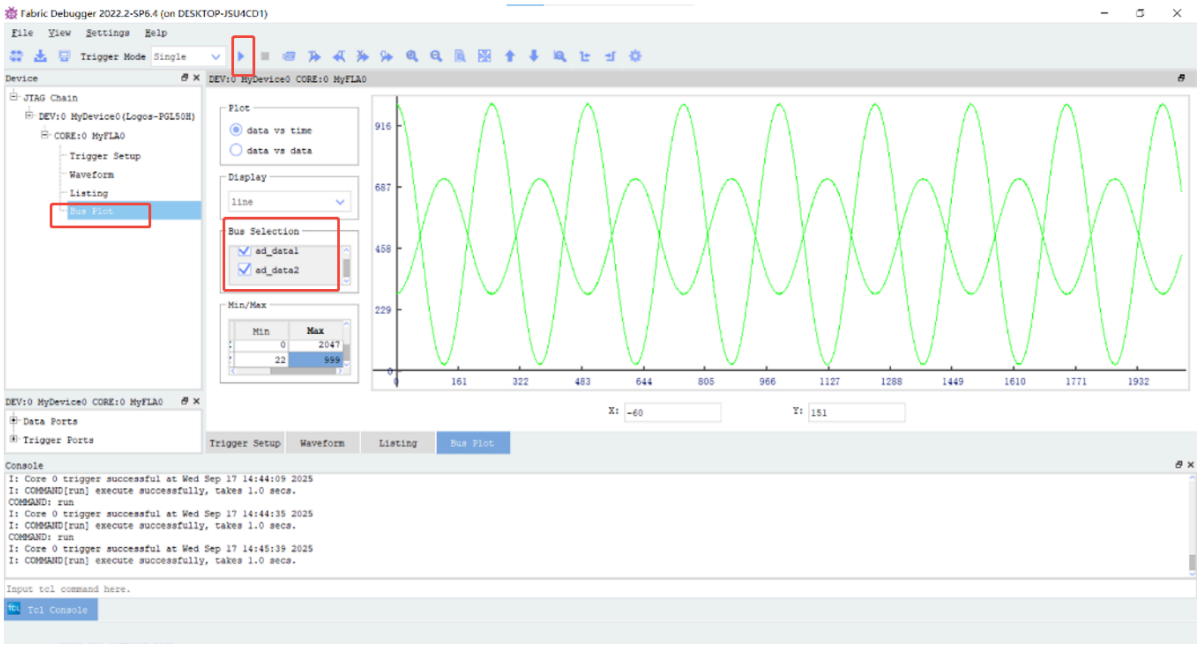
点击扫描芯片

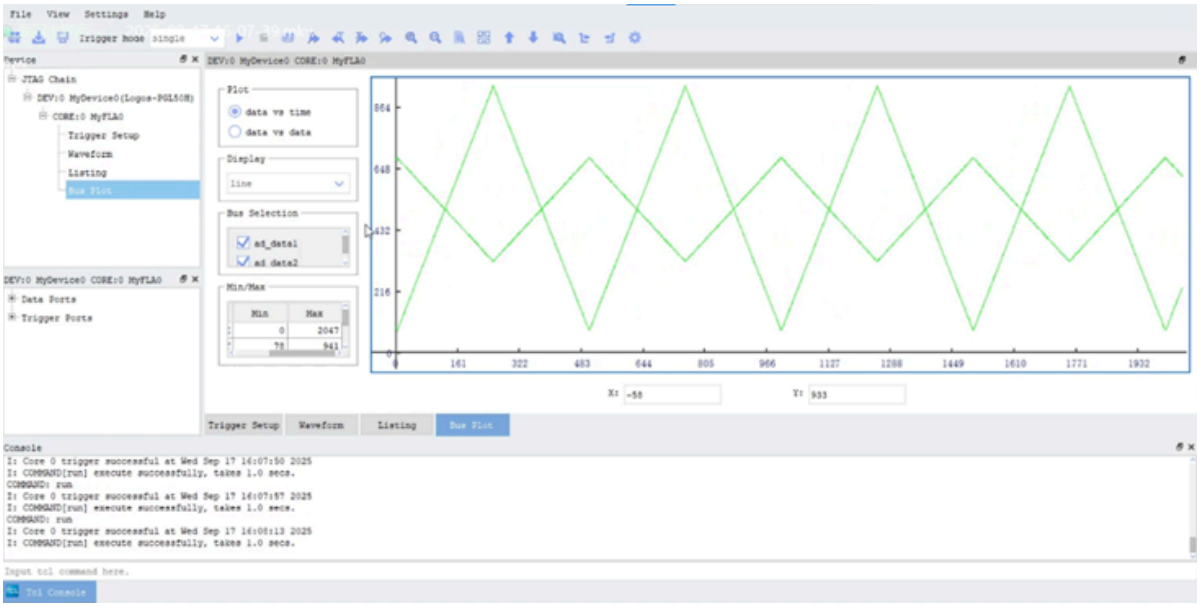


扫描到jtag有连接芯片后，点击烧录



在bus plot即可观察到模拟波形





可以在信号发生器更换不同波形、频率、振幅进行观察，注意振幅不要超过-5V ~ +5V

同样在fpga端也可以通过修改pll的输出频率来改变AD模块的采样频率