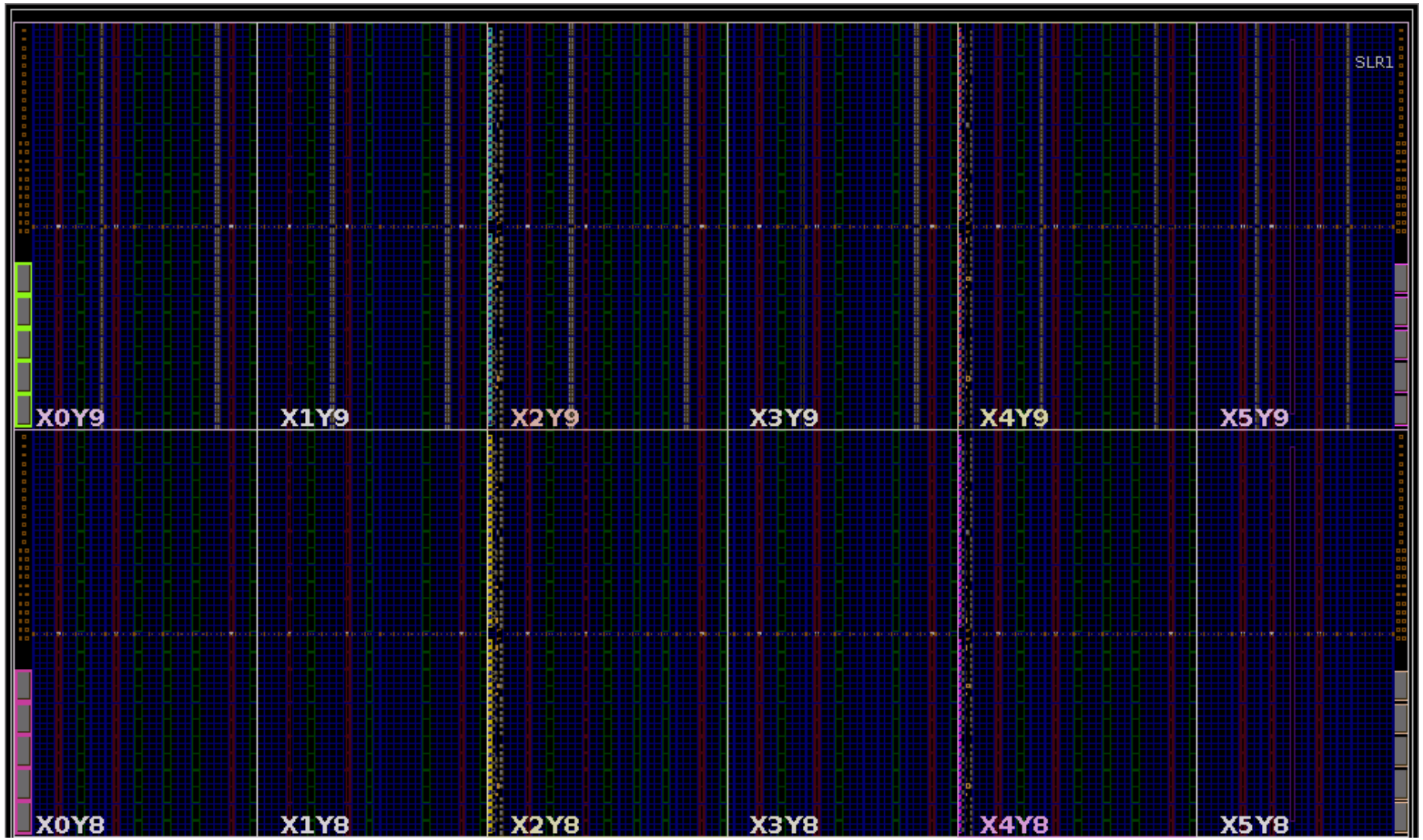
J. de Fine Licht and T. Hoefler

Productive parallel programming on FPGA using High-level Synthesis

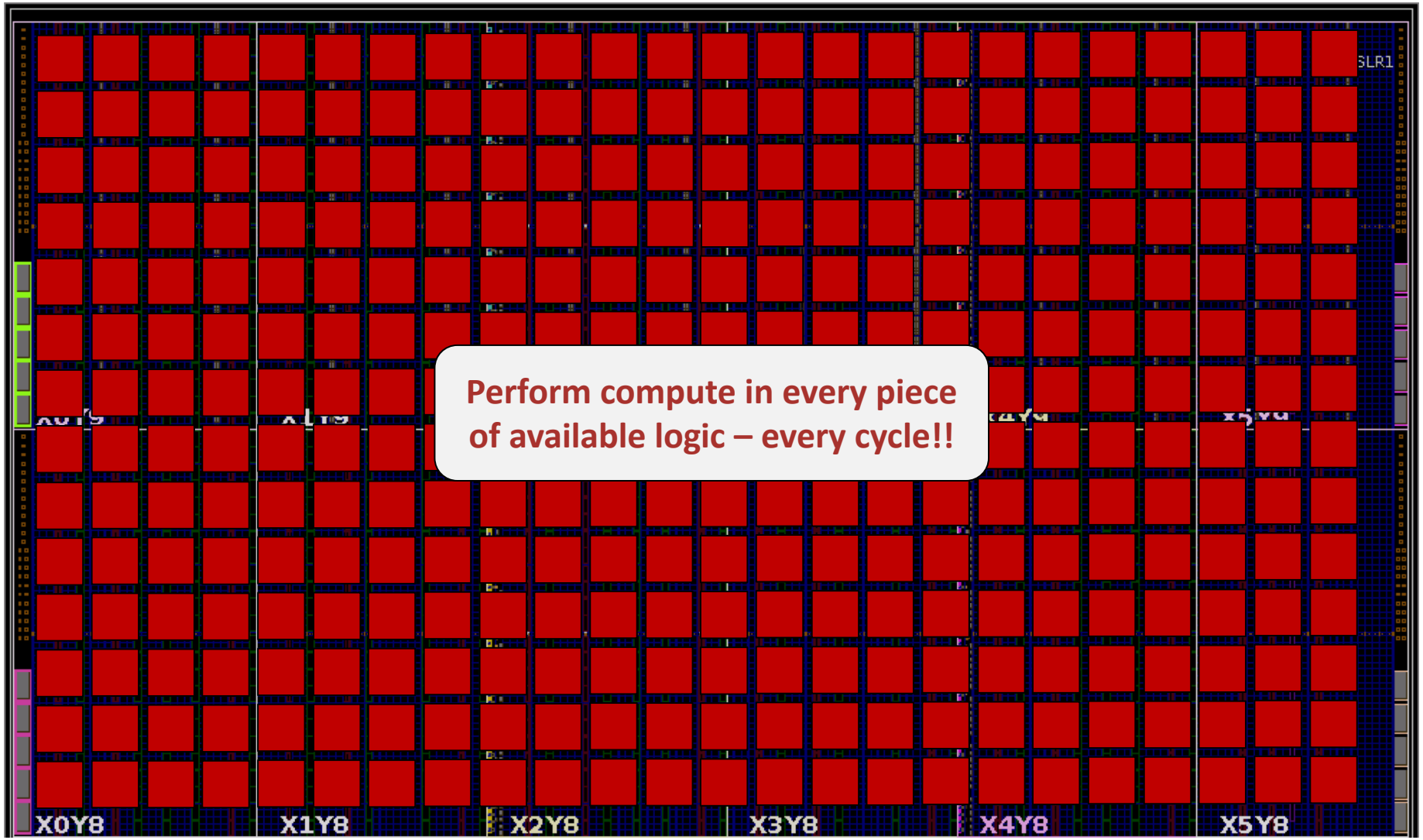
Code examples found at:

https://github.com/spcl/hls_tutorial_examples

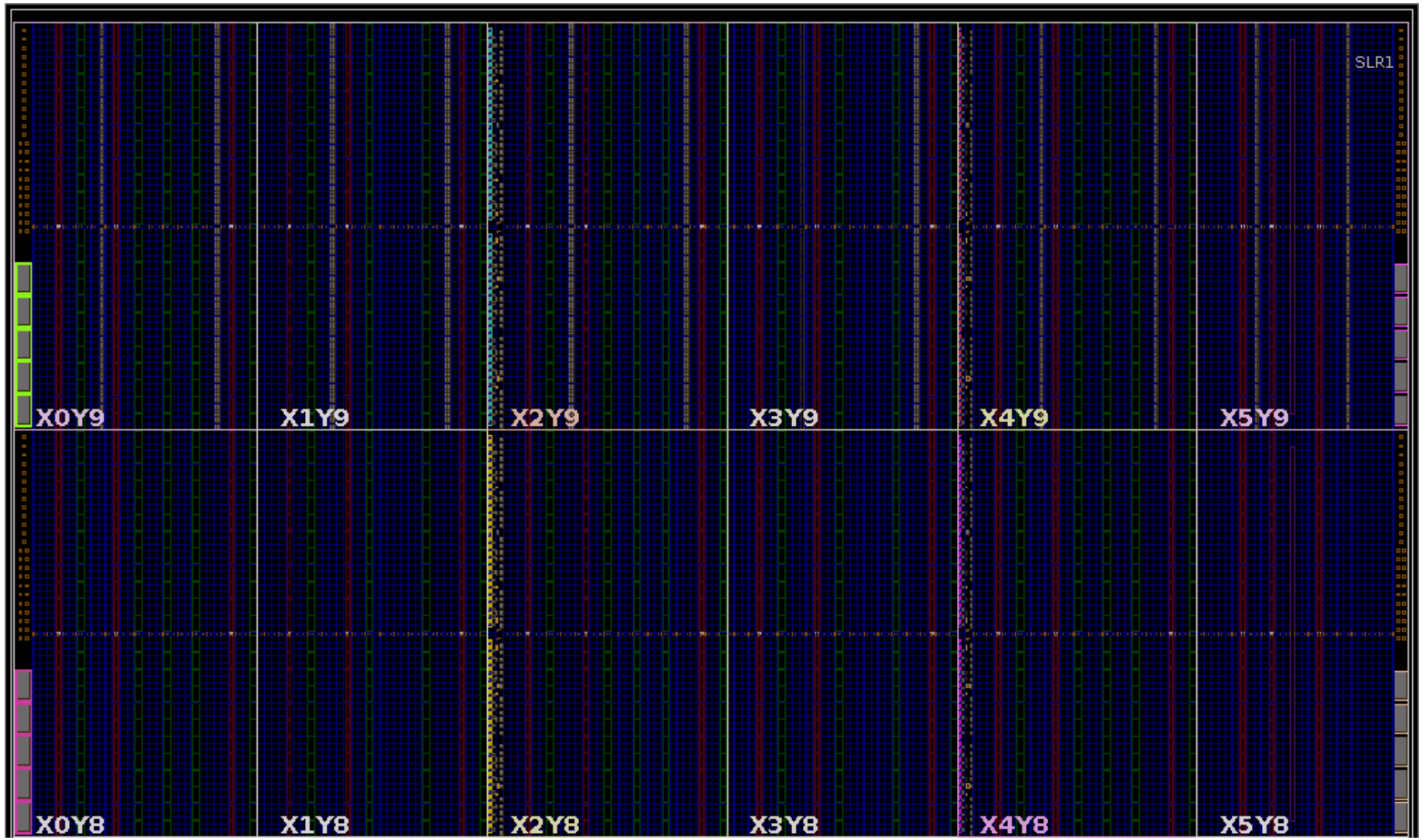
Our goal


SLR1
X0Y9
X1Y9
X2Y9
X3Y9
X4Y9
X5Y9
X0Y8
X1Y8
X2Y8
X3Y8
X4Y8
X5Y8

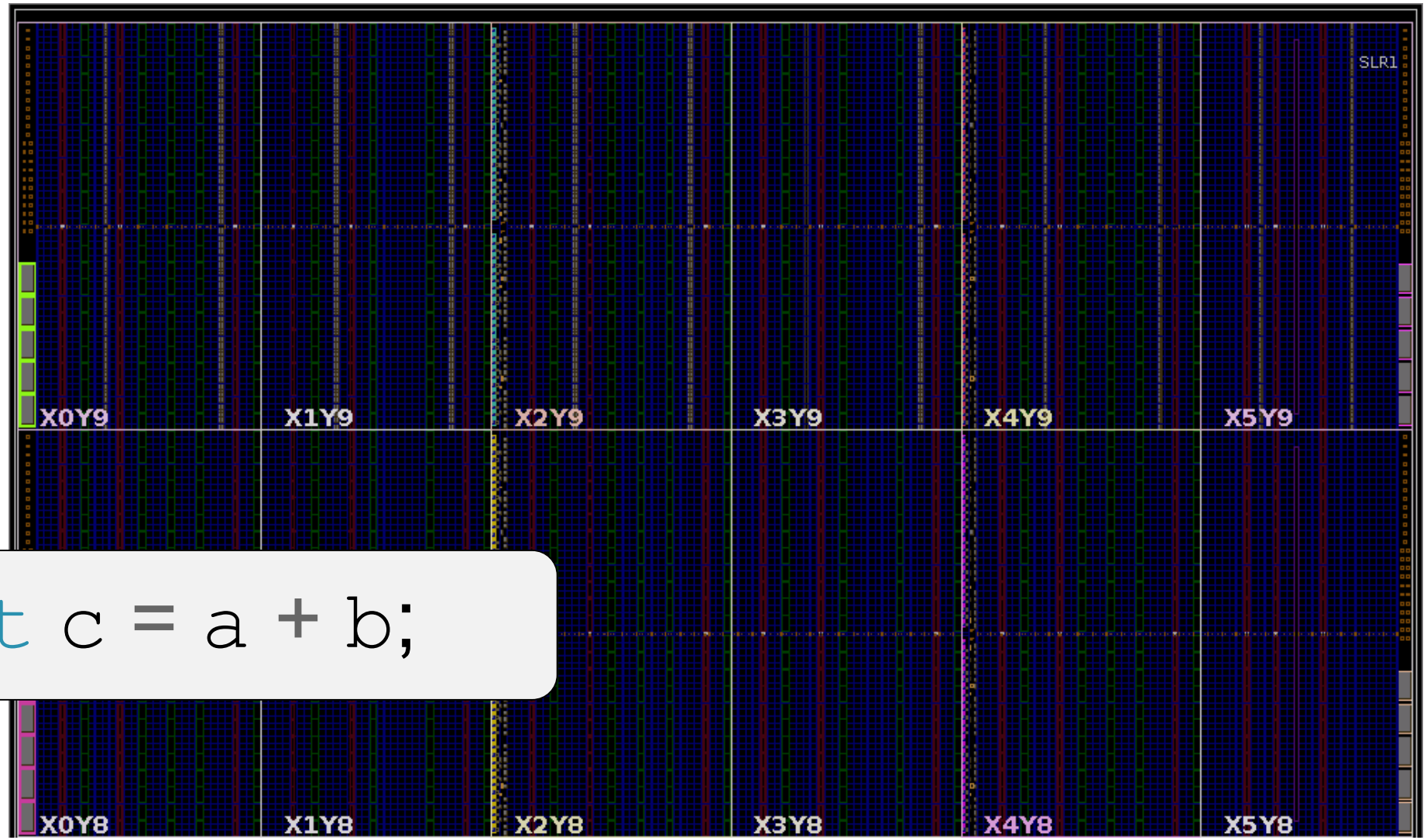
Our goal


SLR1
Perform compute in every piece of available logic – every cycle!!
X0Y8
X1Y8
X2Y8
X3Y8
X4Y8
X5Y8

A single operation

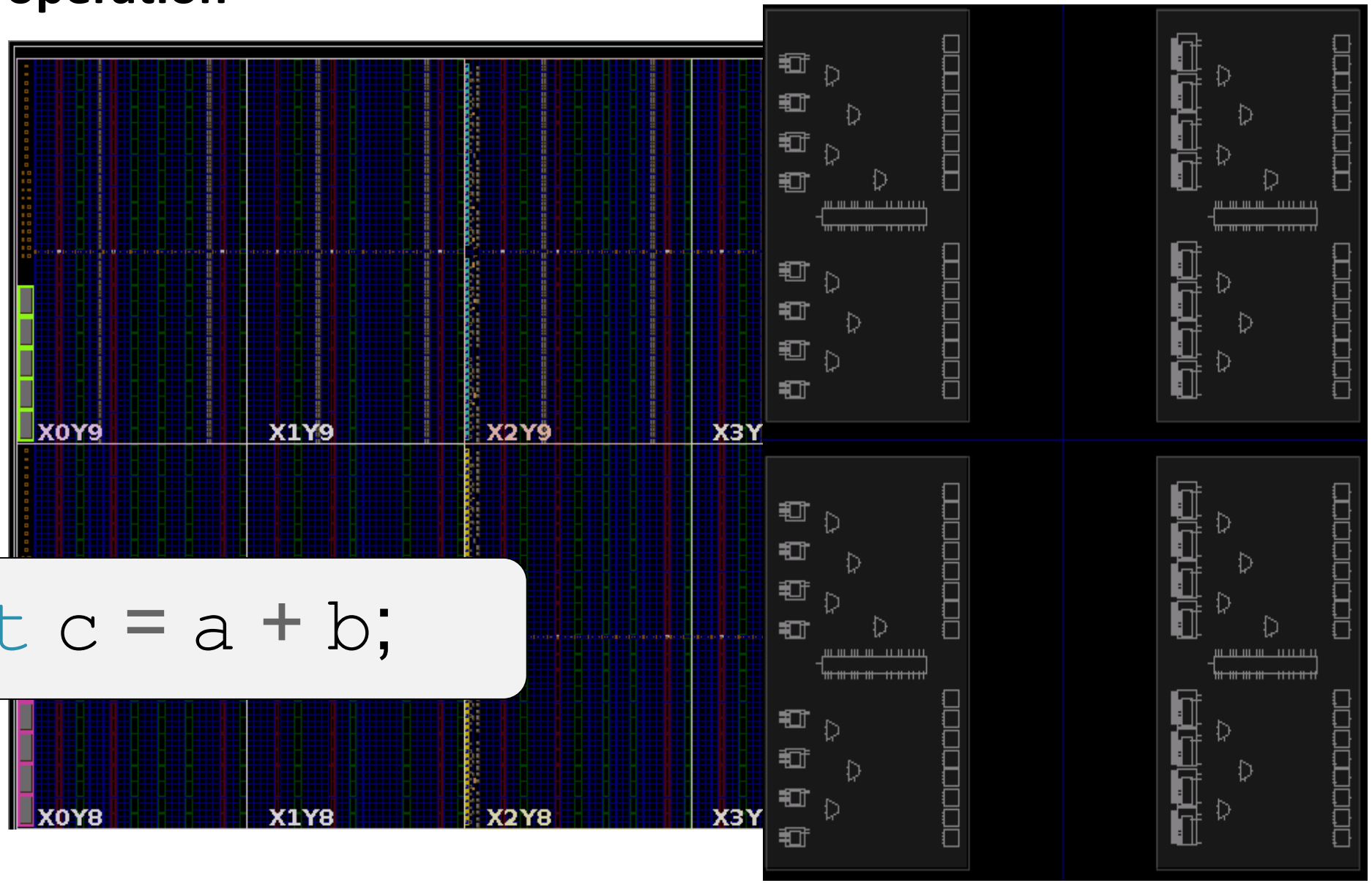


A single operation




```
int c = a + b;
```

A single operation

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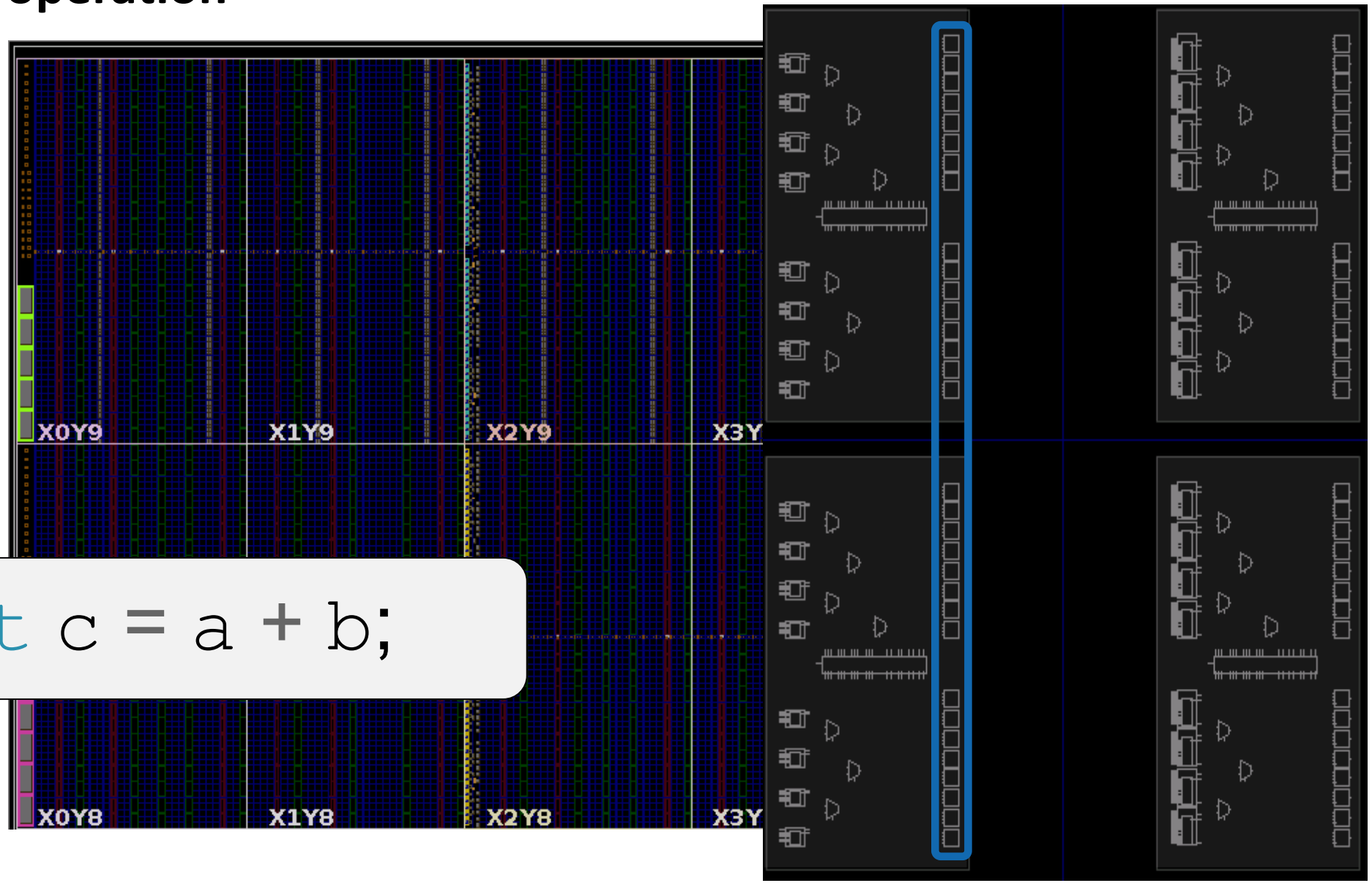


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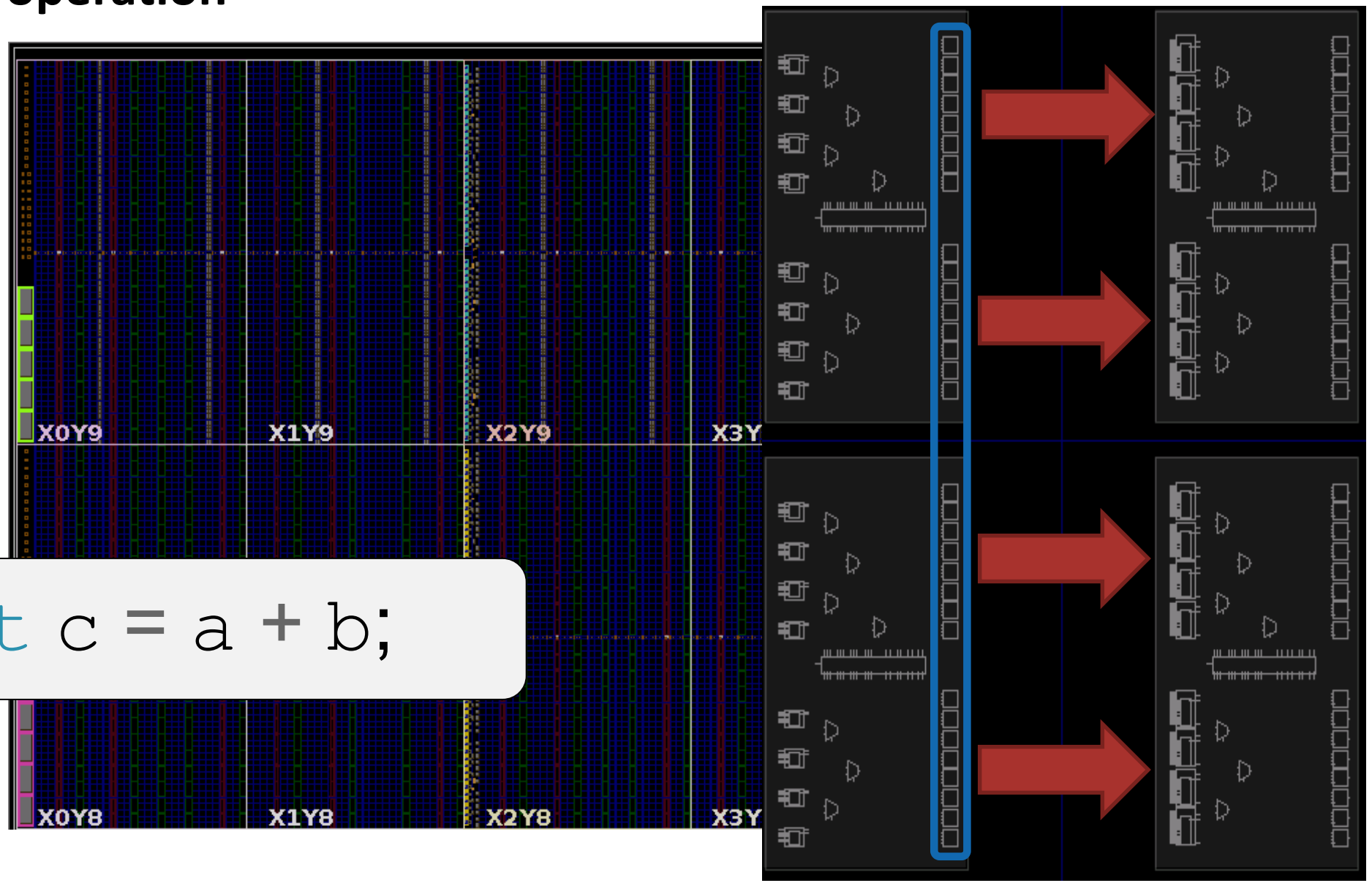


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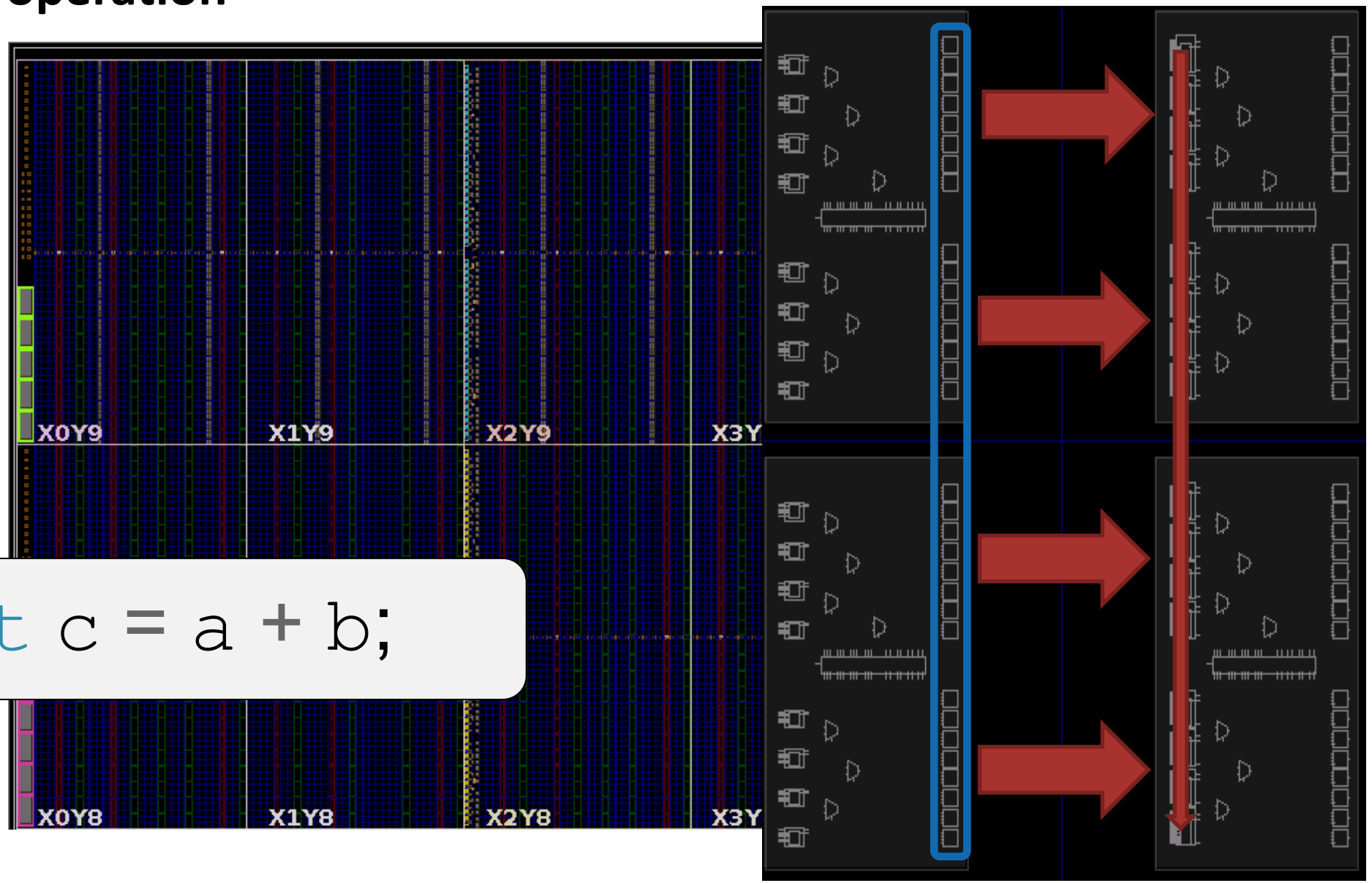


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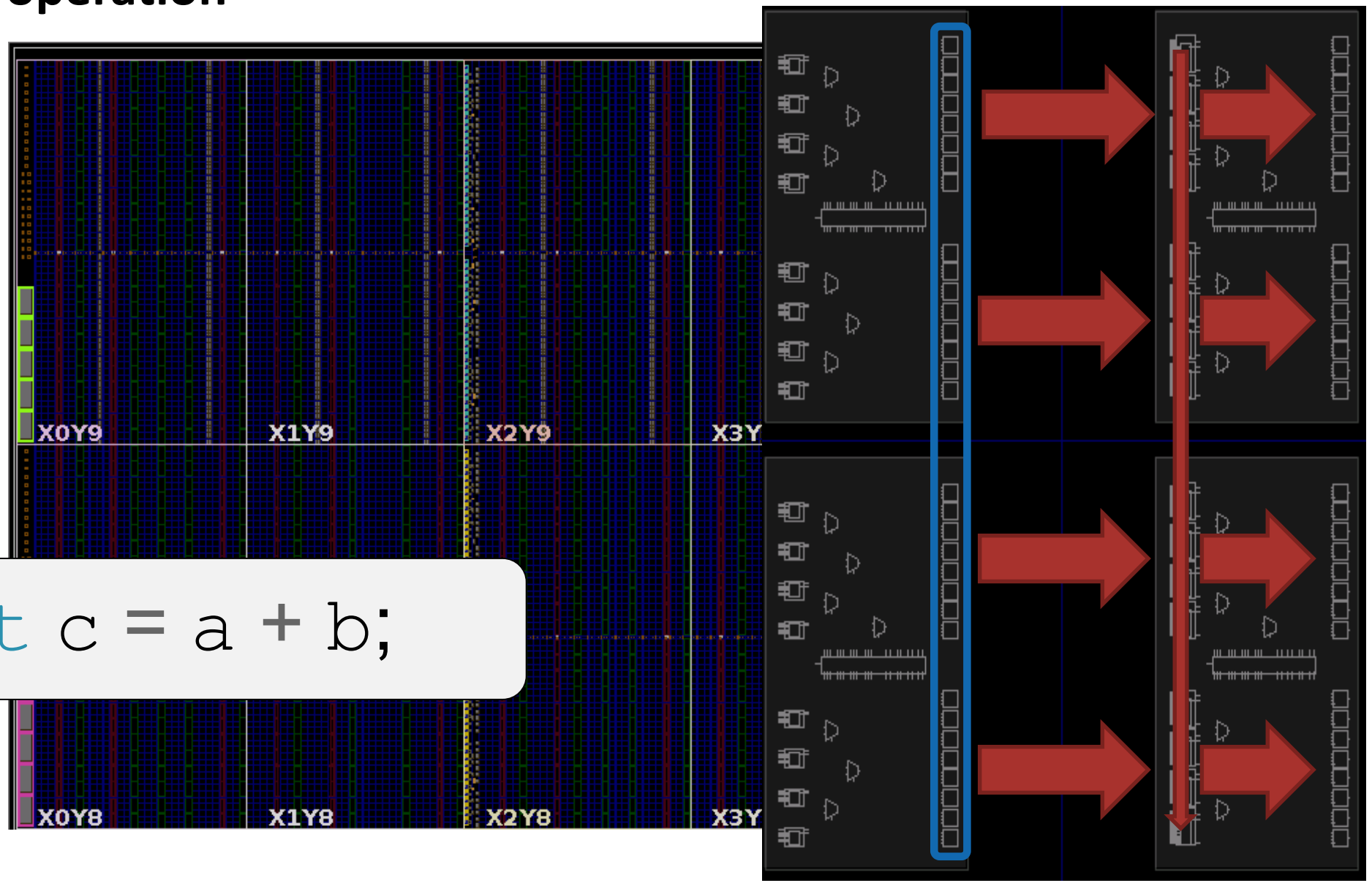


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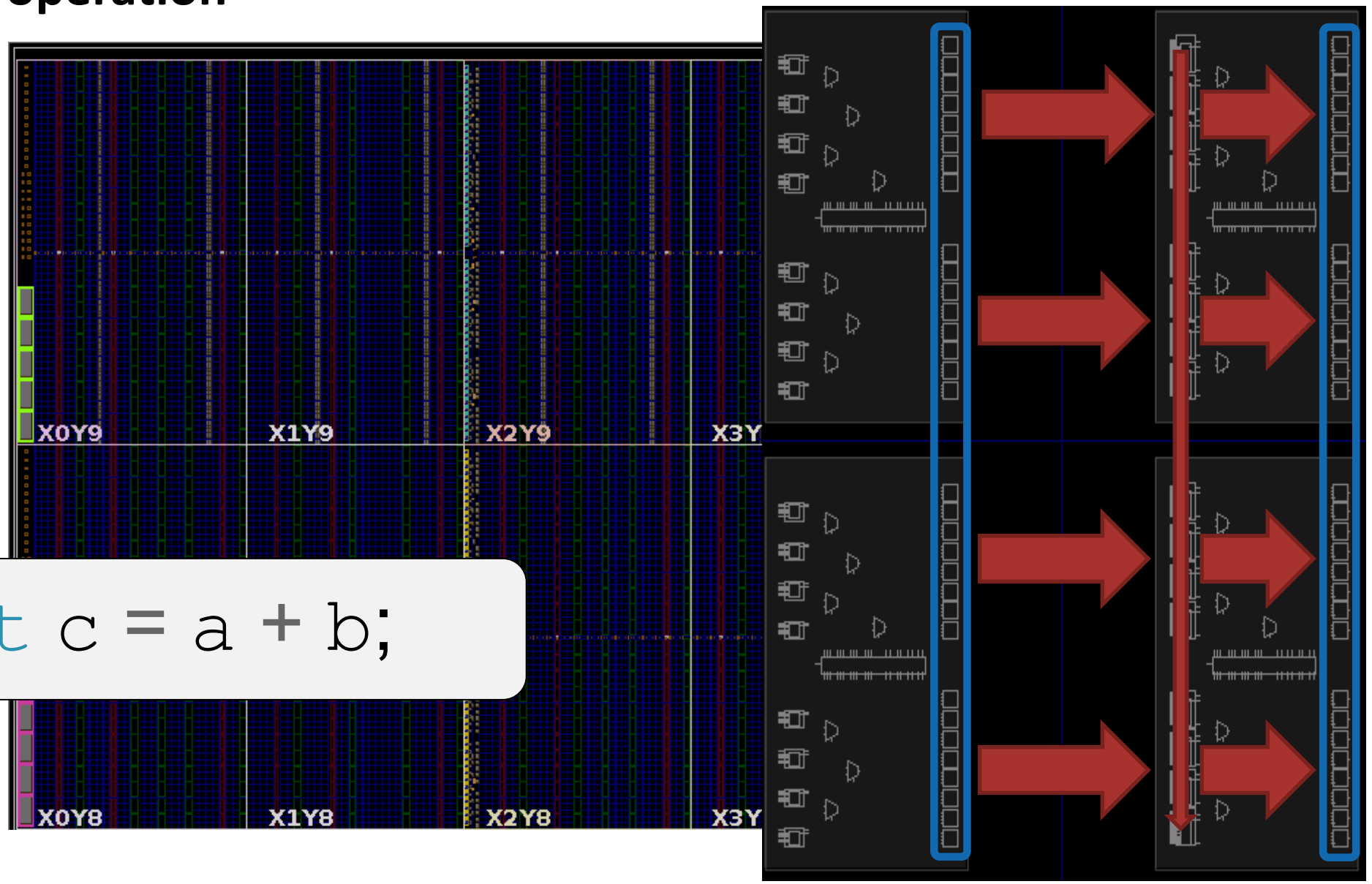
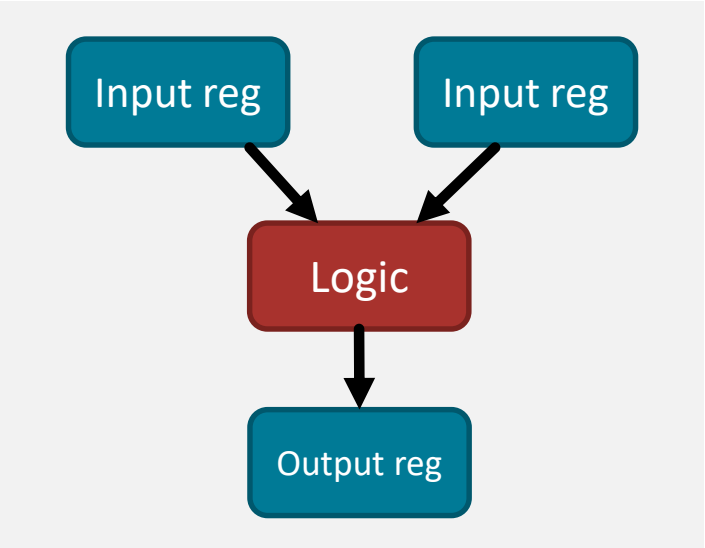



```
int c = a + b;
```

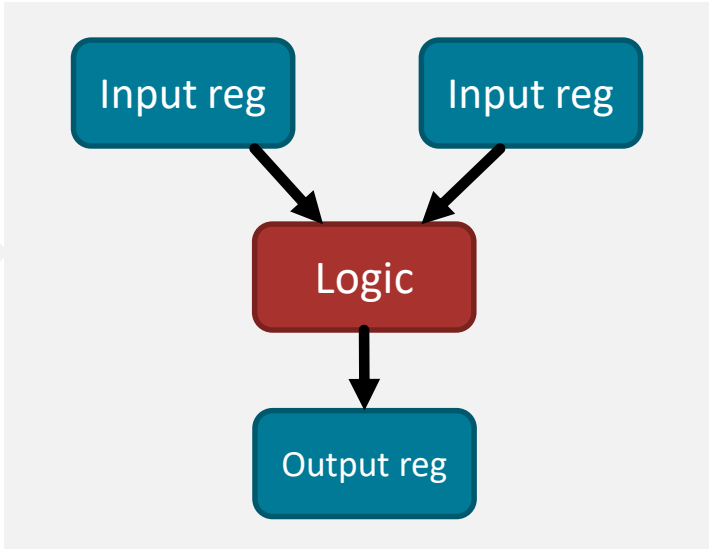
Register transfer level




```
int c = a + b;
```

Register transfer level

```
always @(posedge clk)
  if (start) begin
      out <= in + 1;
  end
```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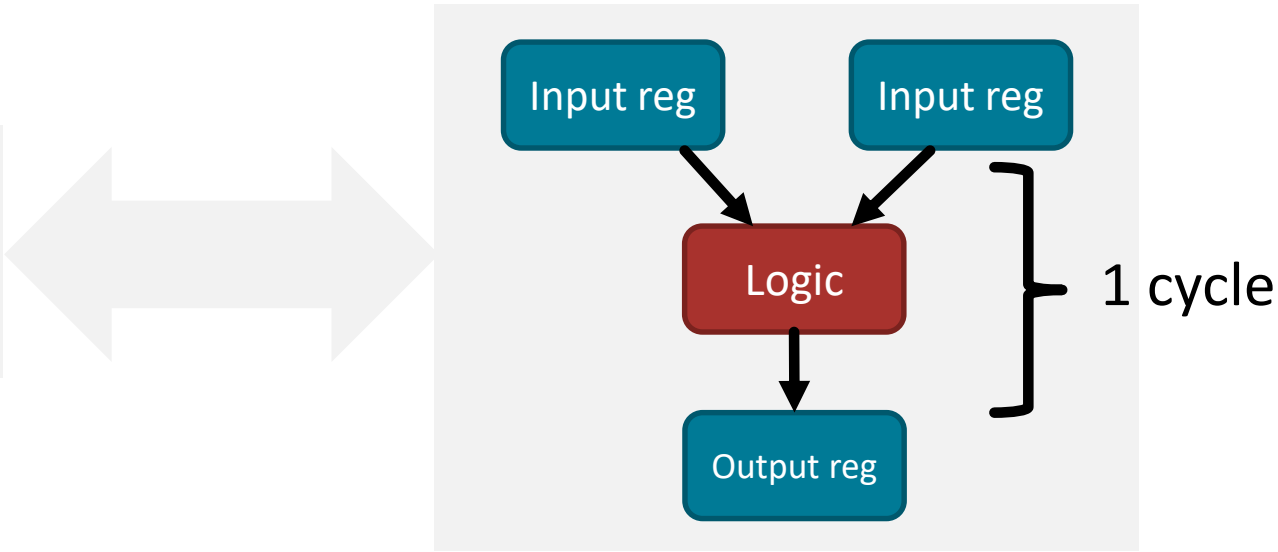


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int c = a + b;
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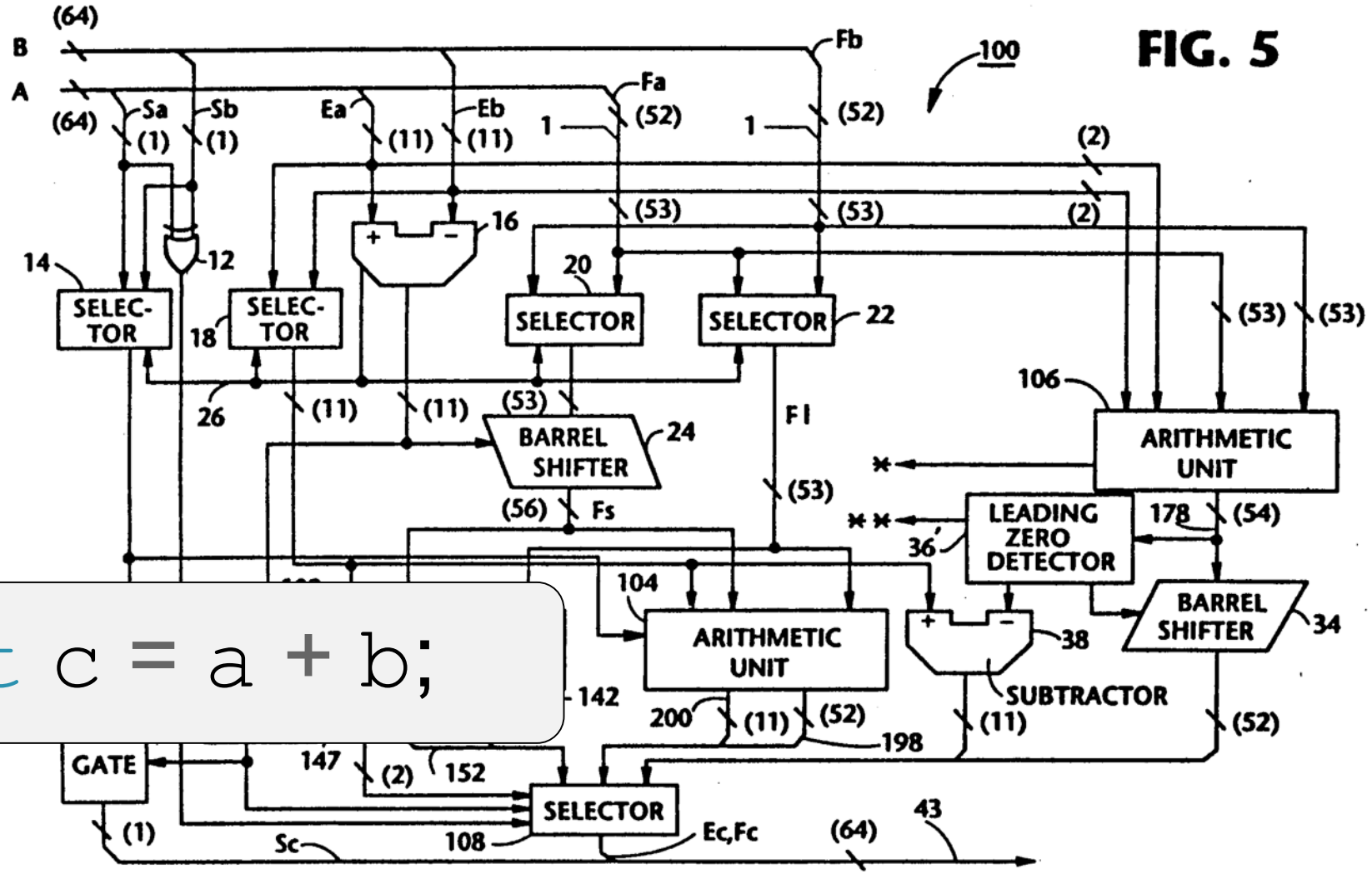
Single floating point operation

```
float c = a + b;
```

Single floating point operation

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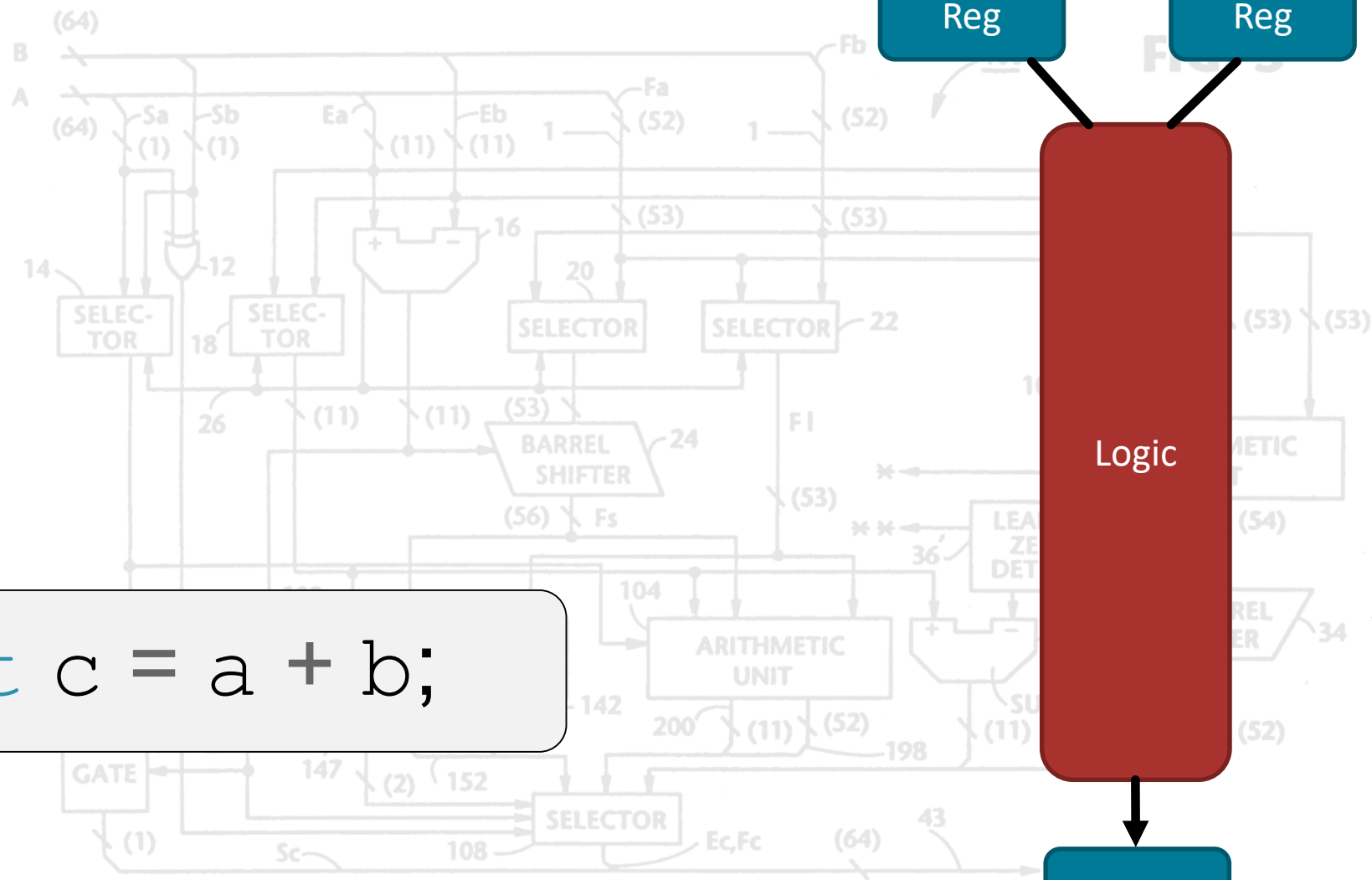
Nakayama, T. *Hardware arrangement for floating-point addition and subtraction*, 1993, US Patent 5,197,023.

Single floating point operation

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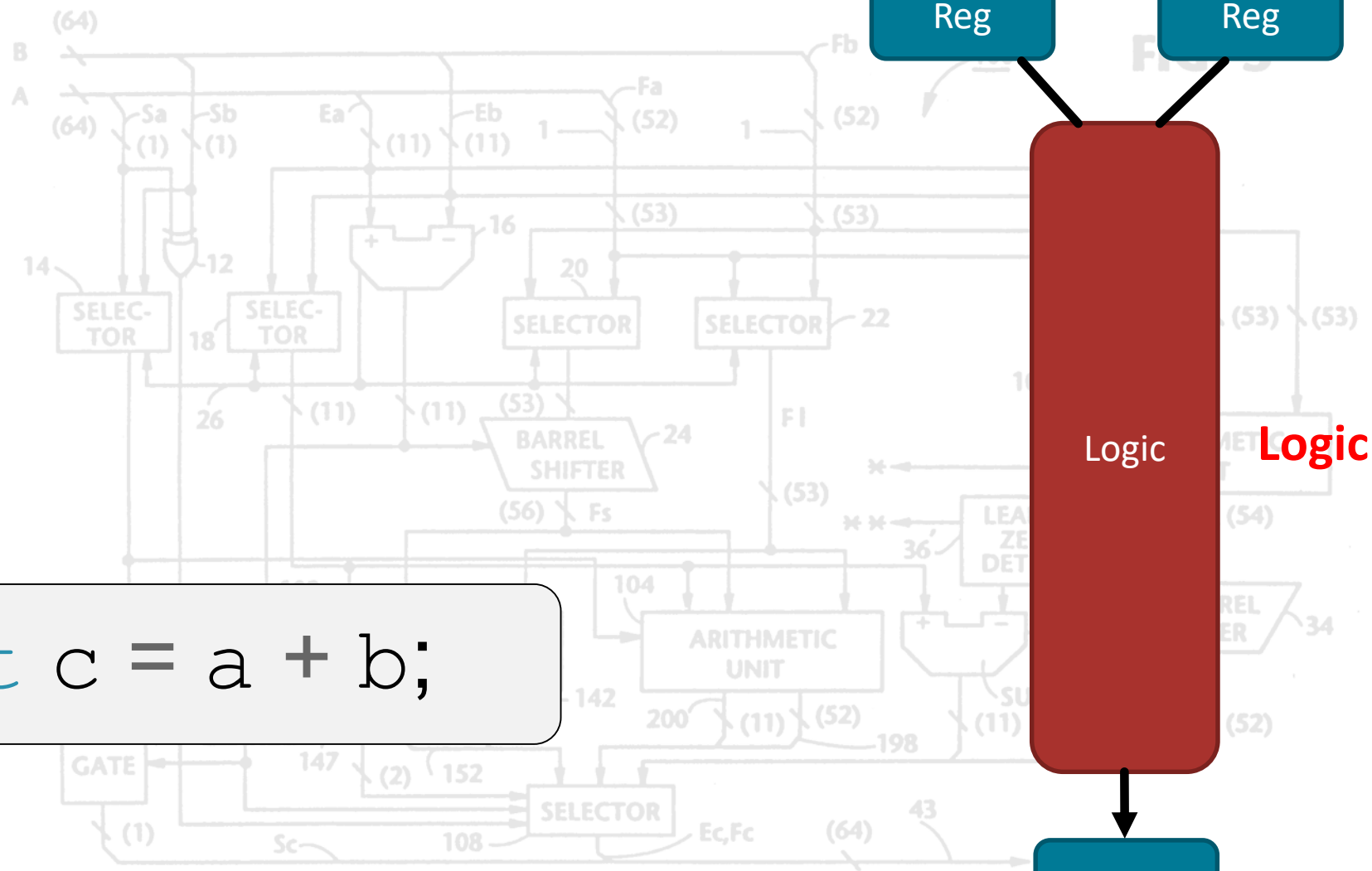


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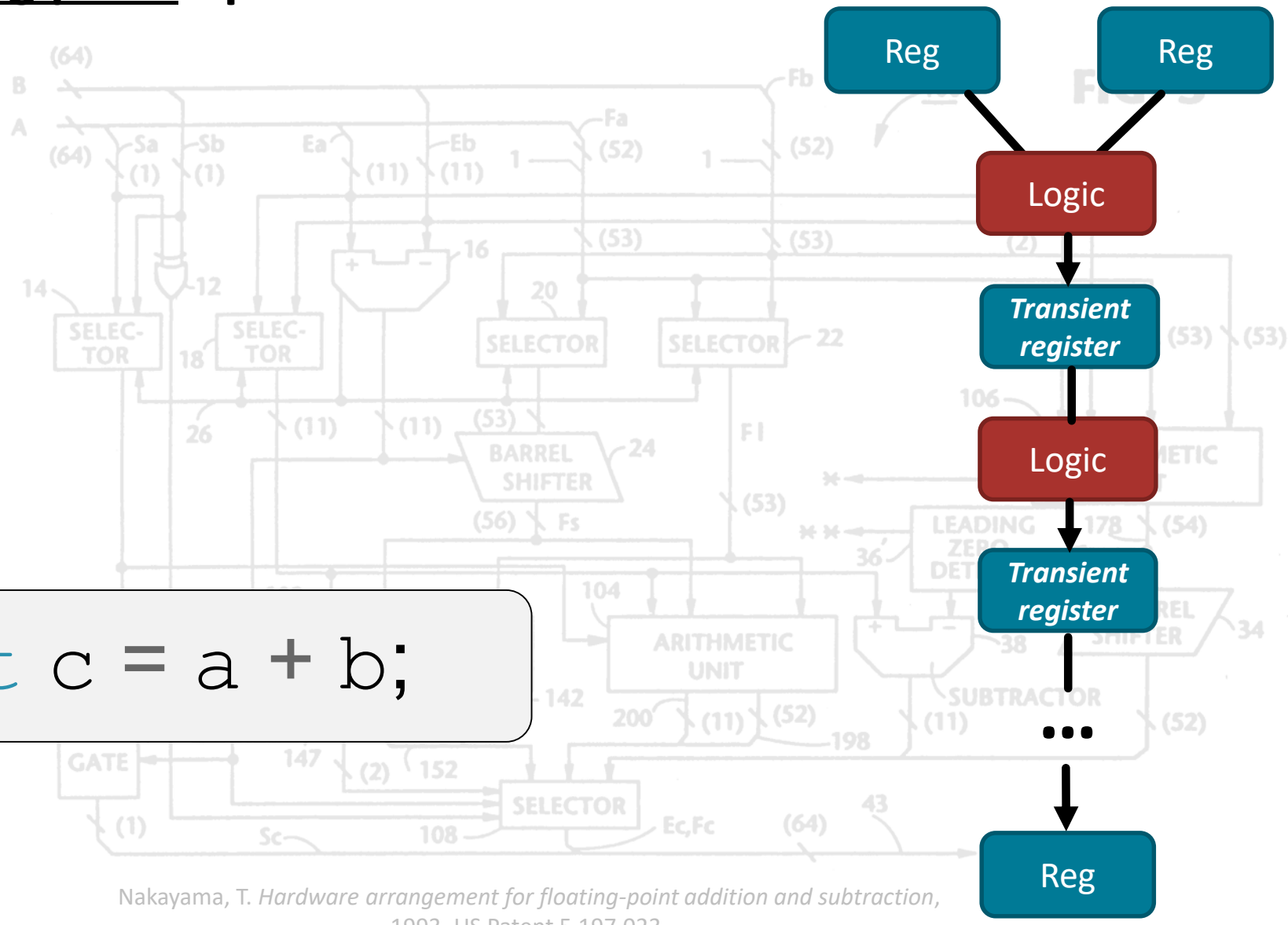


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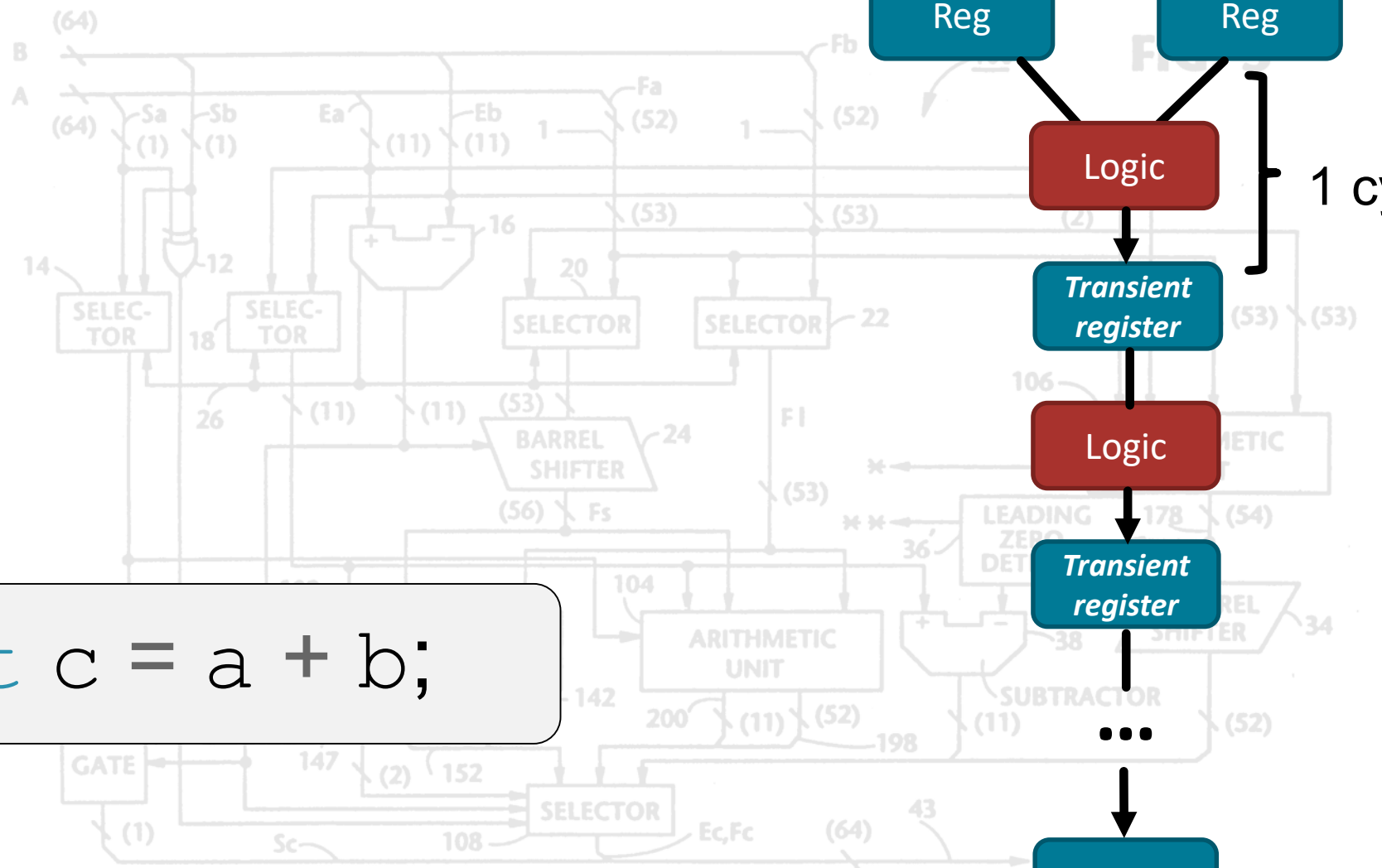


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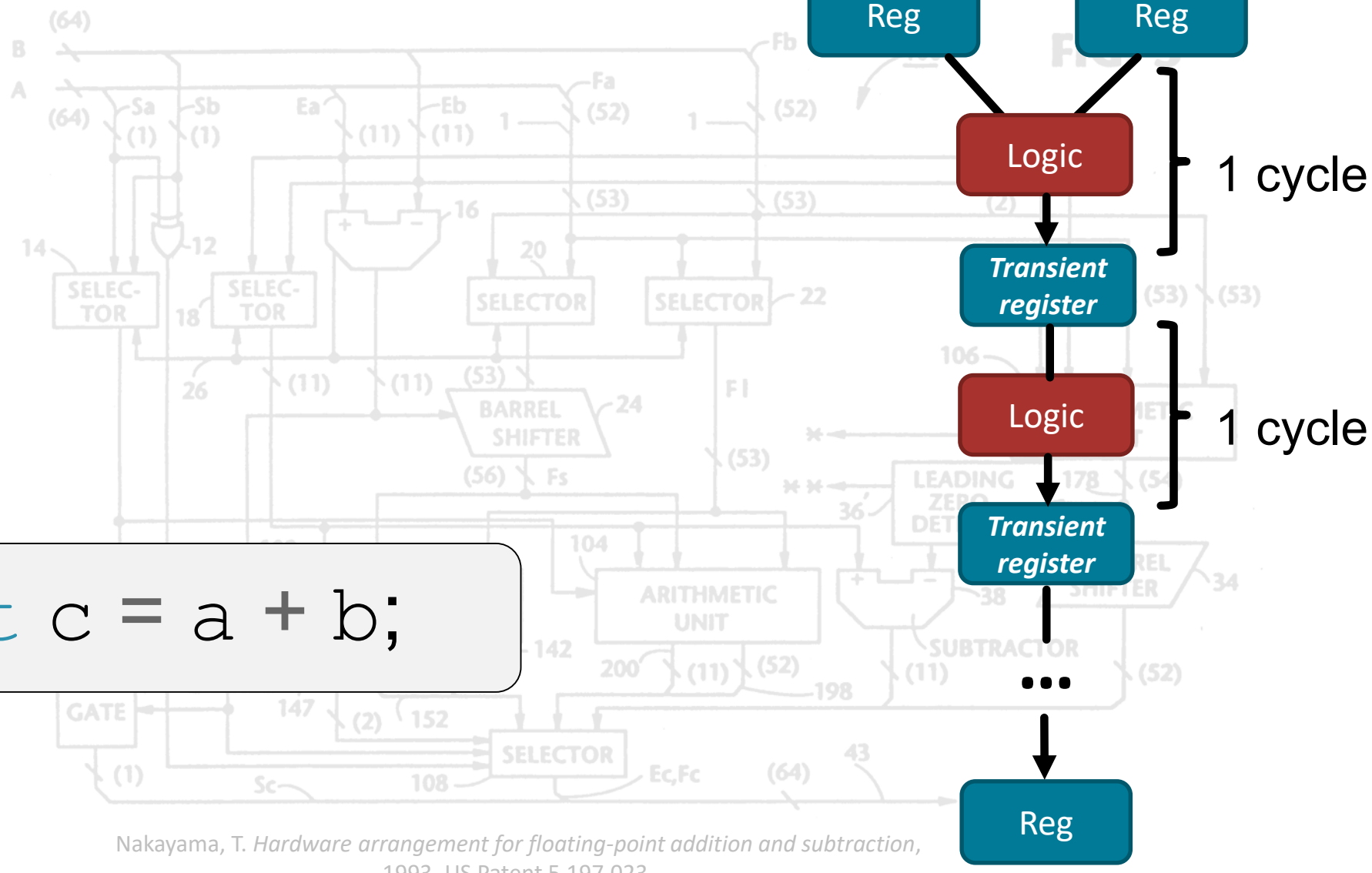


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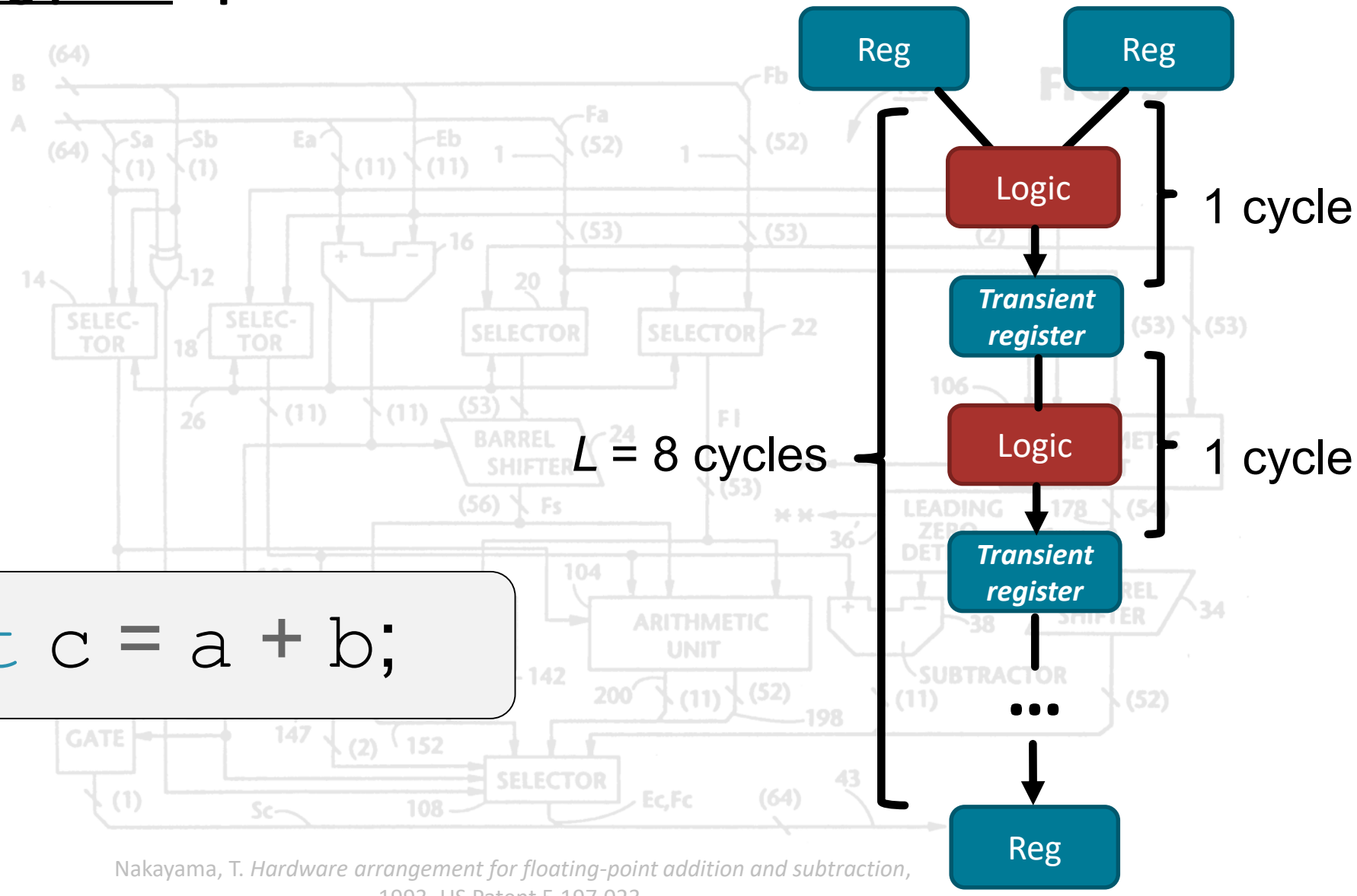


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Our point of view

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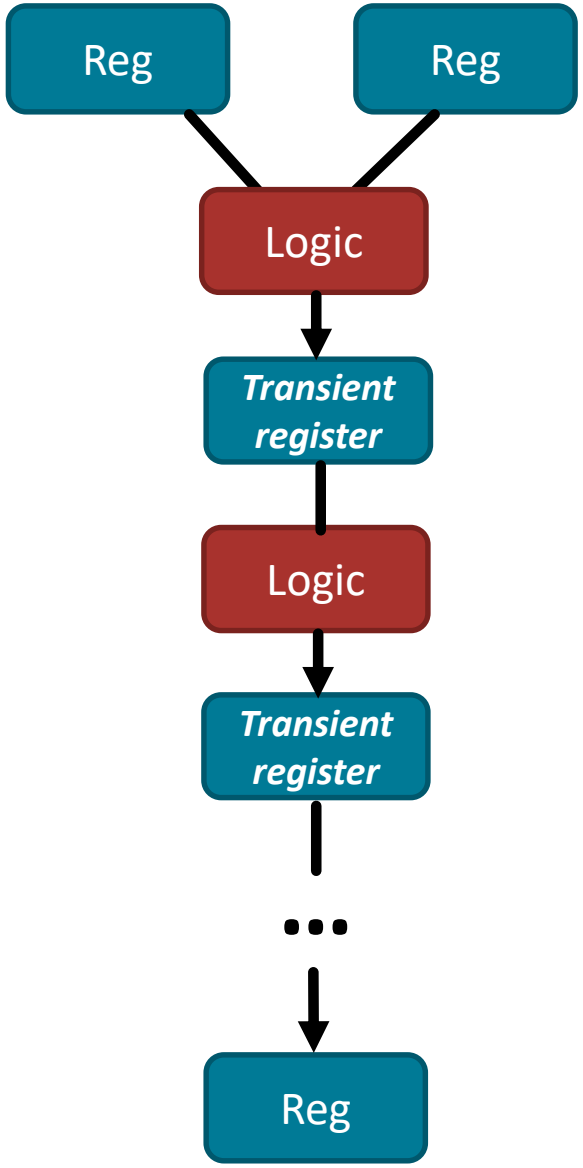

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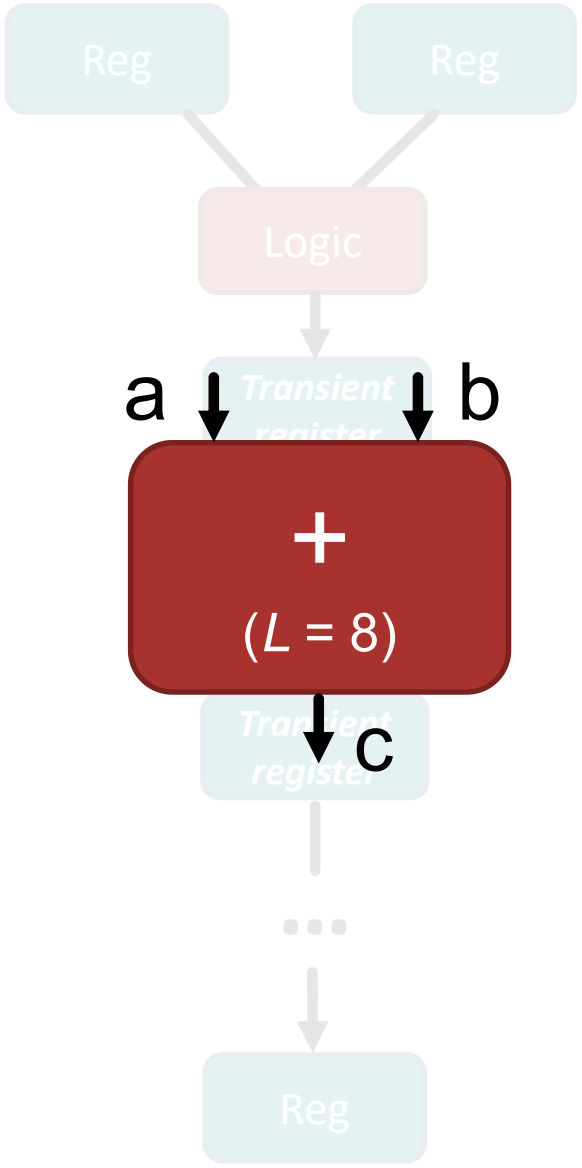
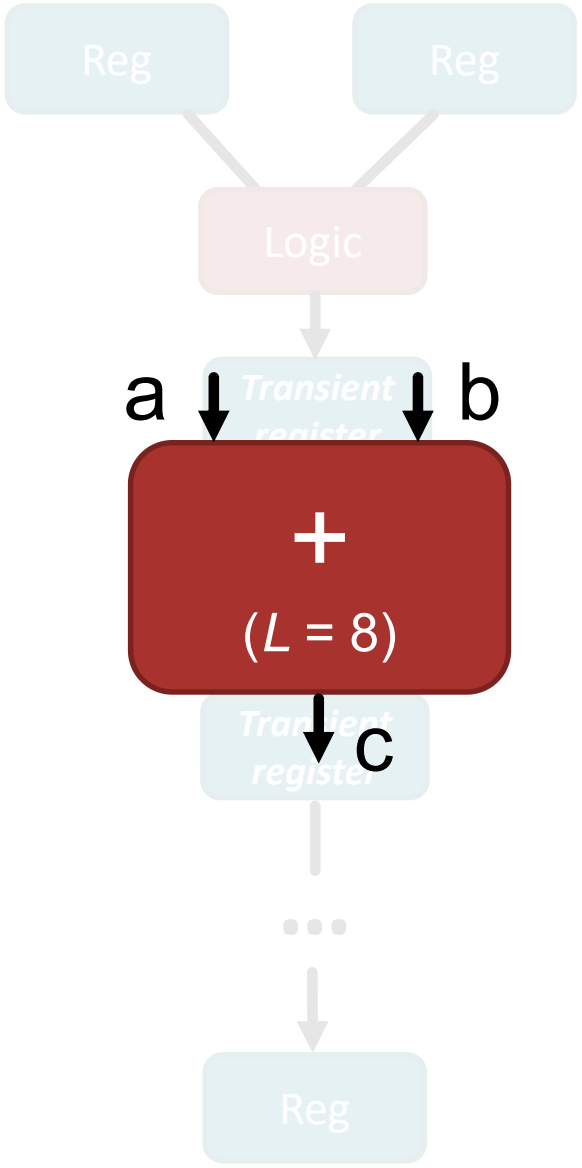


Our point of view

In HLS, we treat **pipelines**.

```
float c = a + b;
```



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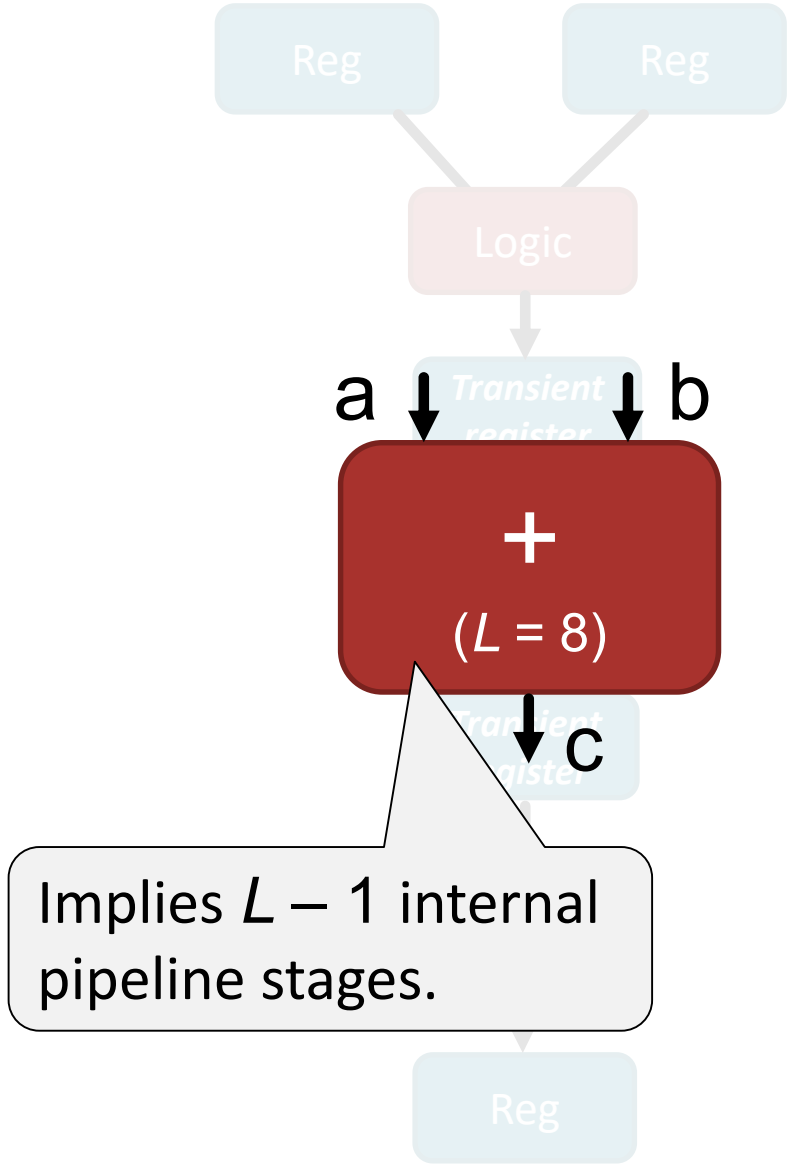
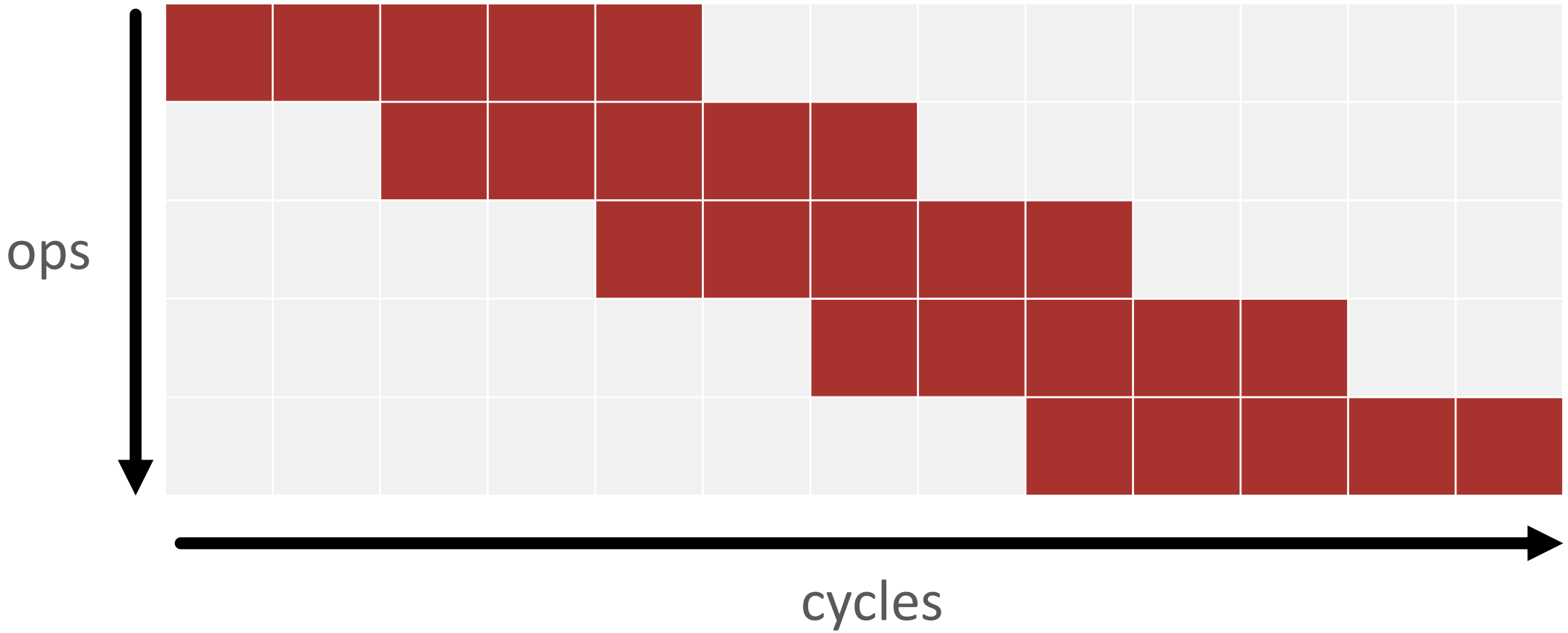


Pipelines



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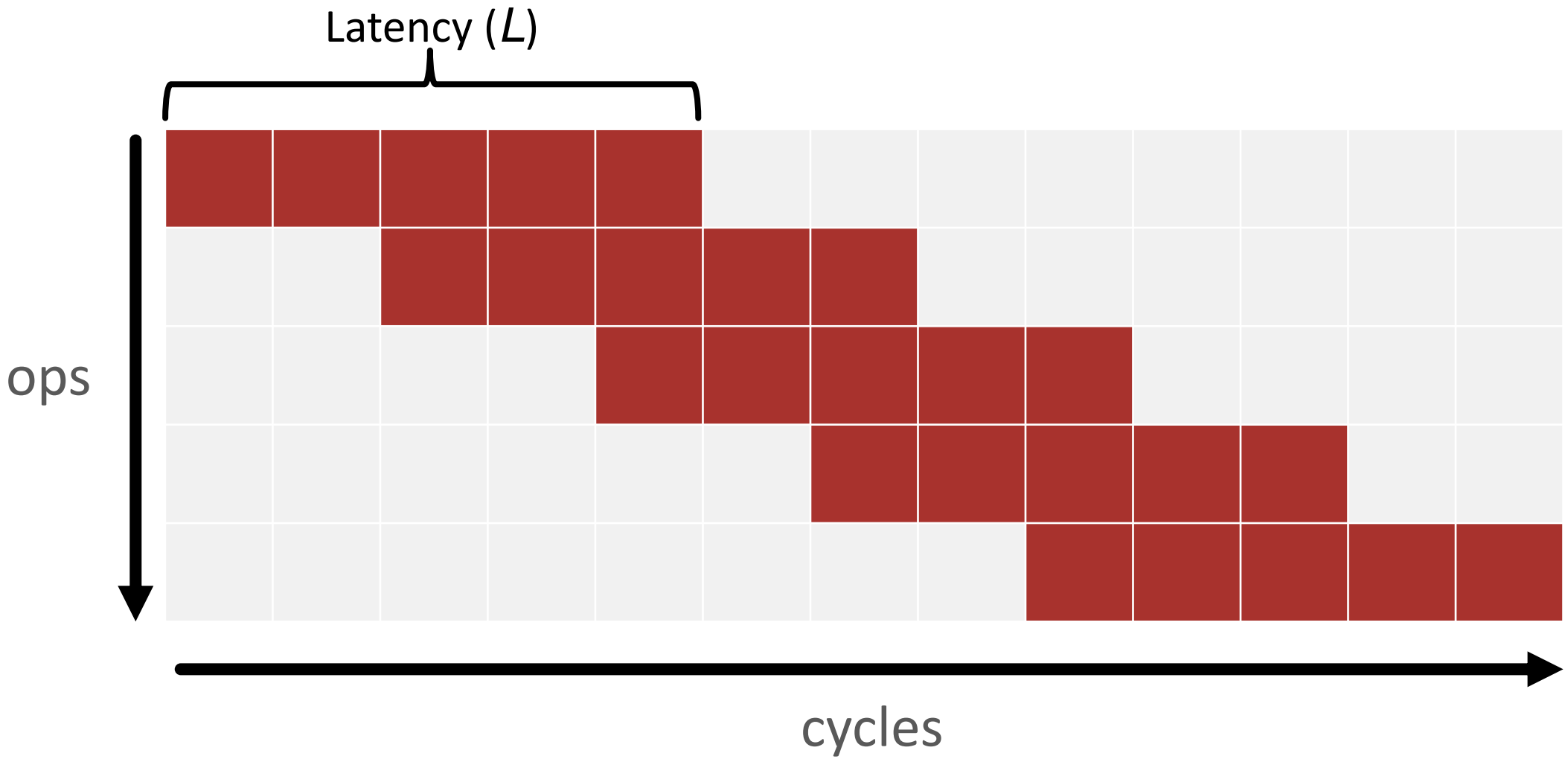

Multiple floating point operations

```
float c = (a + b) * (a - b);
```

Multiple floating point operations

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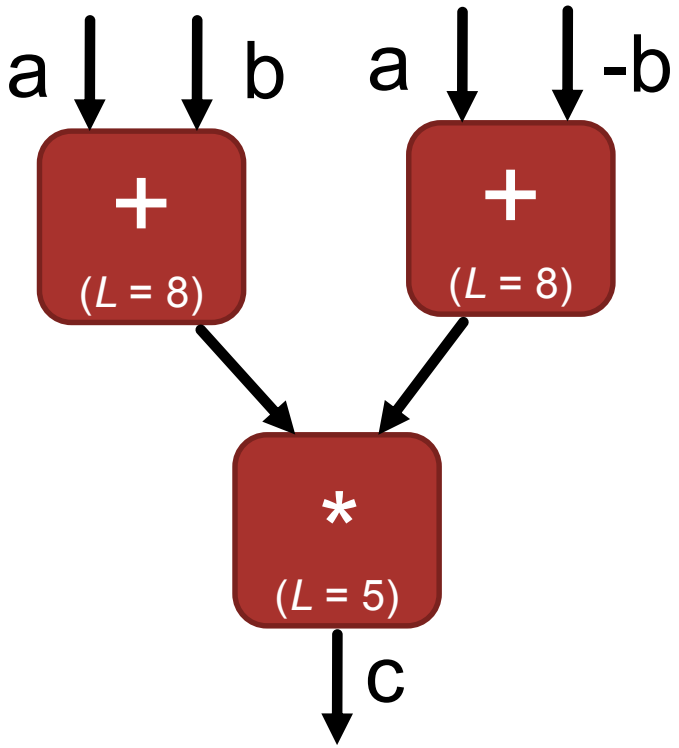
≥ Two ways to implement this

Multiple floating point operations

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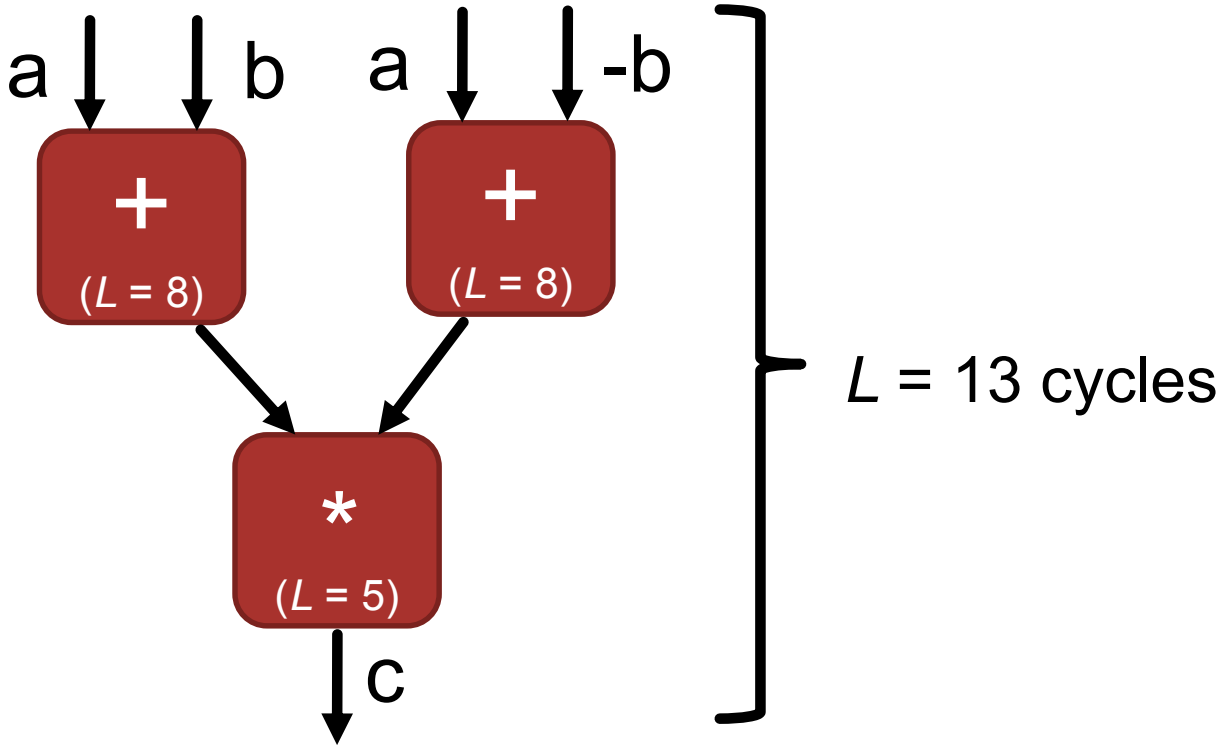


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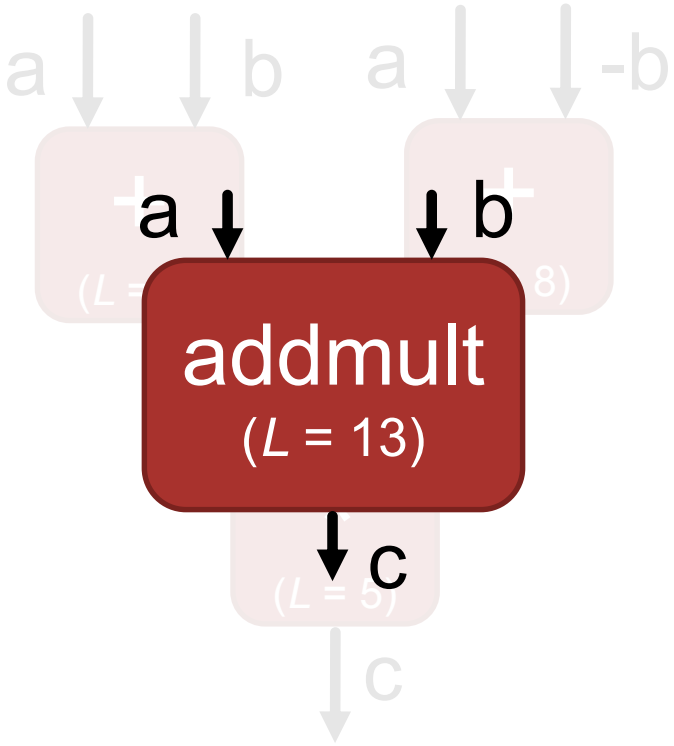


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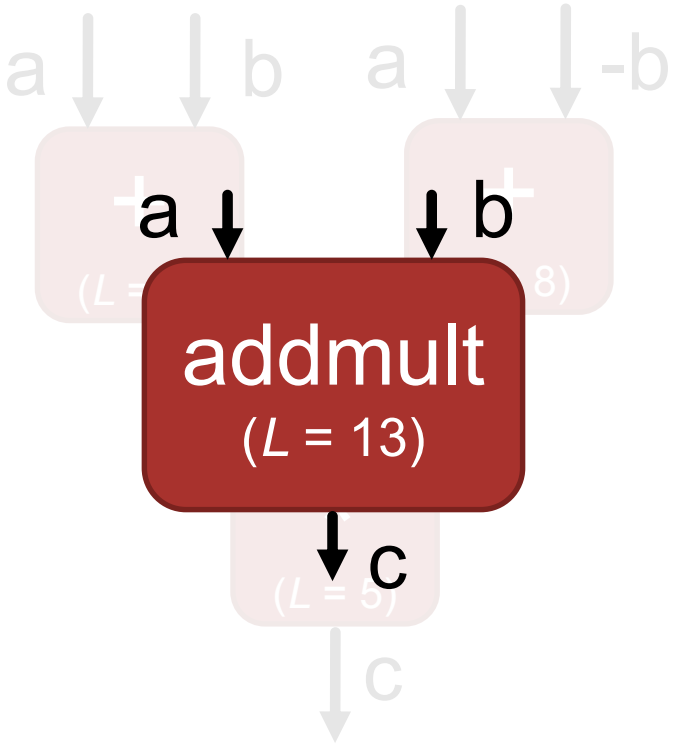

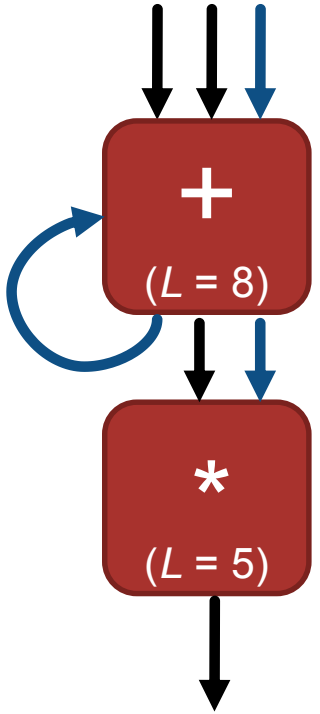


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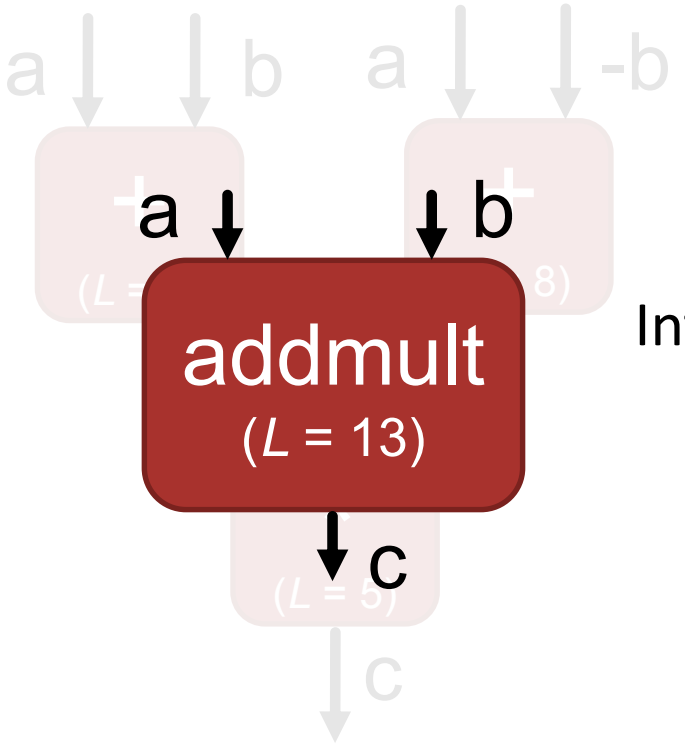
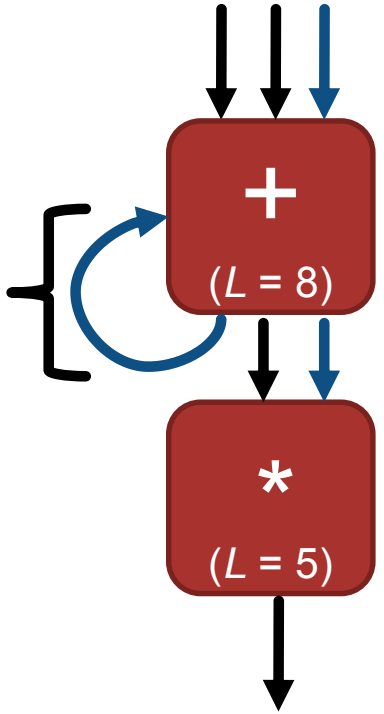


Interleave: +1 cycle

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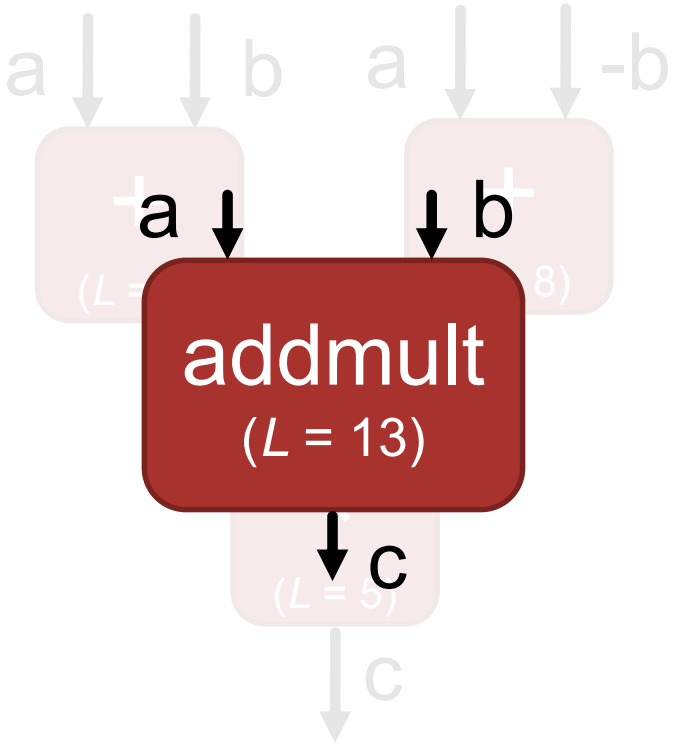

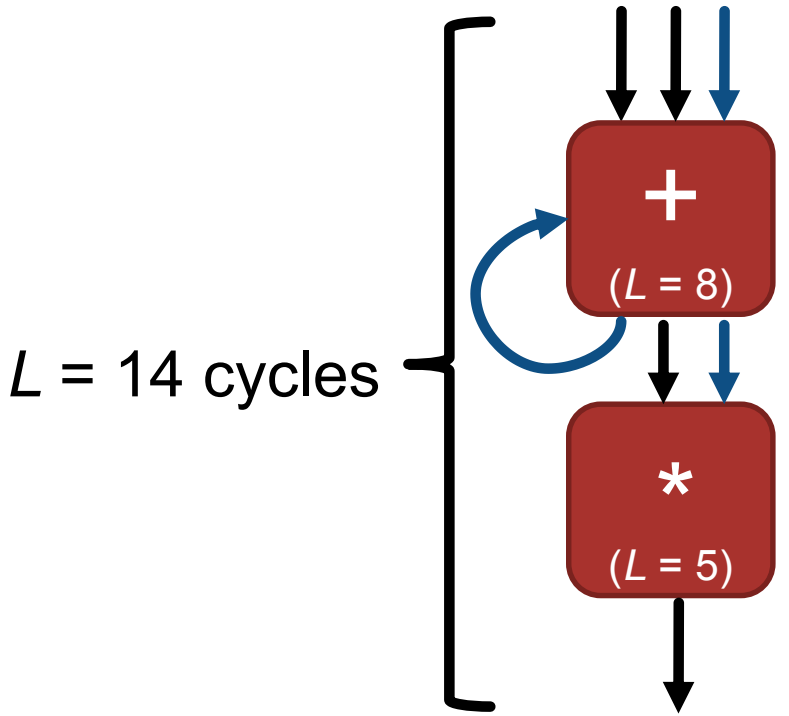


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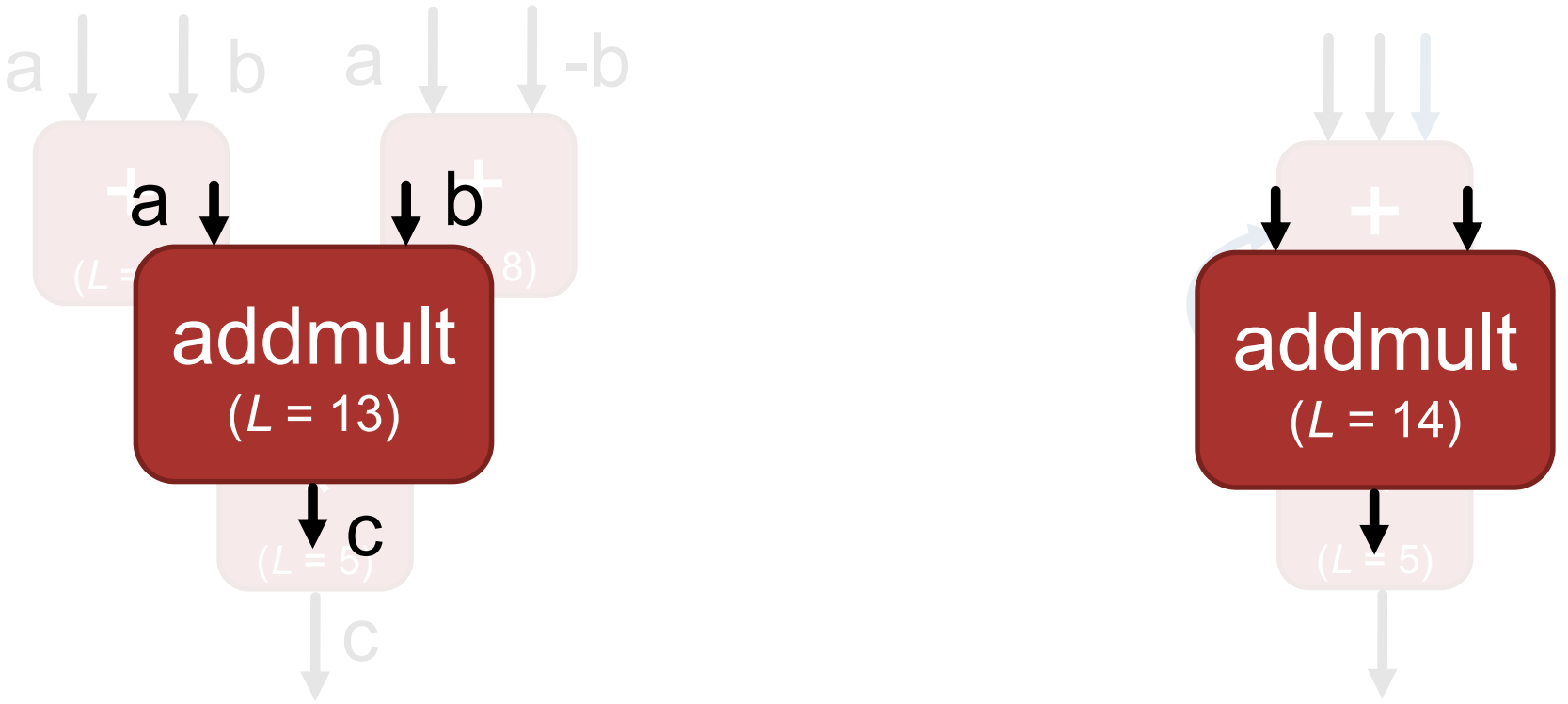


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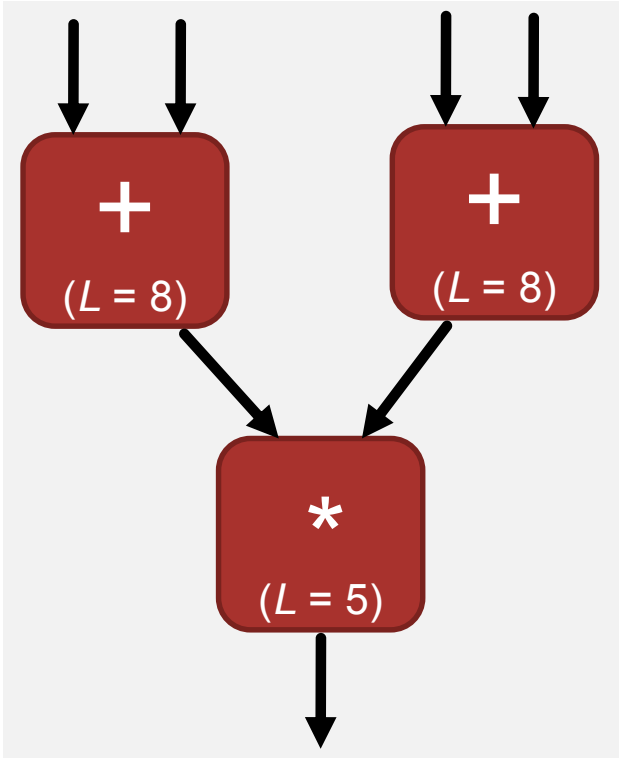
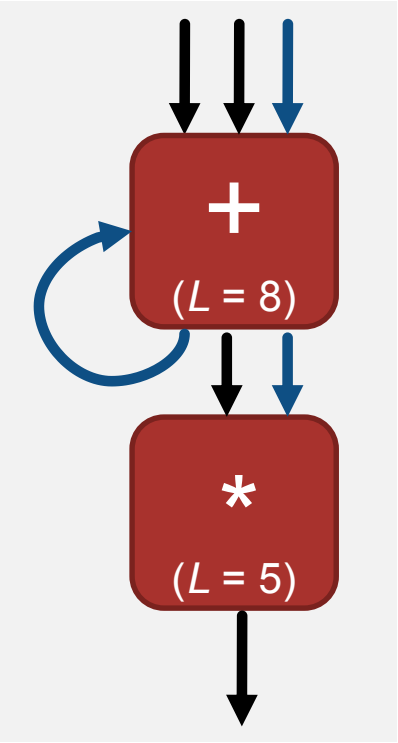
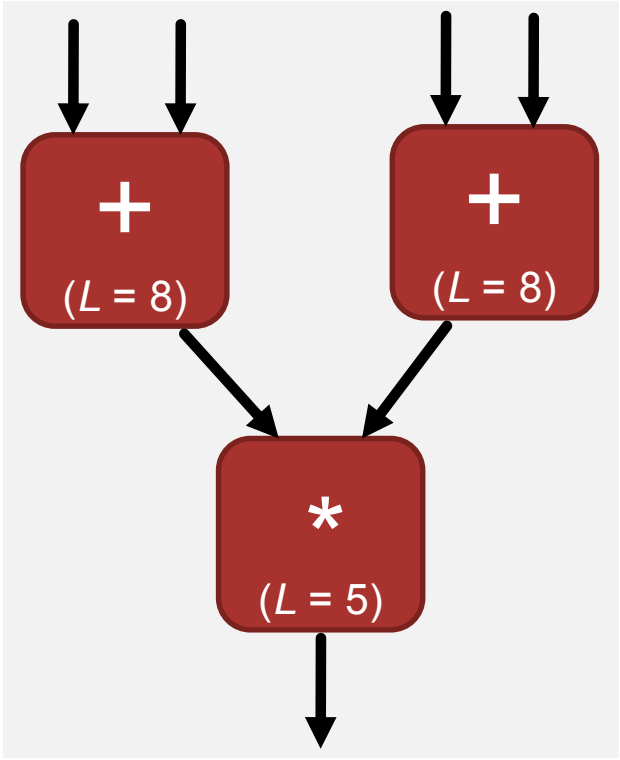
Initiation interval

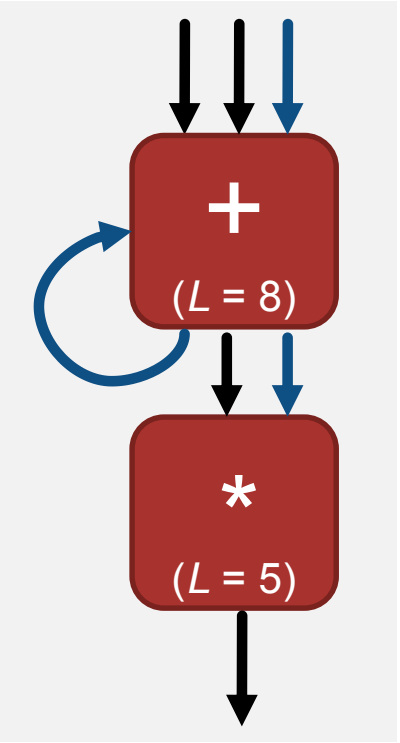




Initiation interval

In addition to **latency** (*L*), we introduce the property **initiation interval** ("II", here *I*).

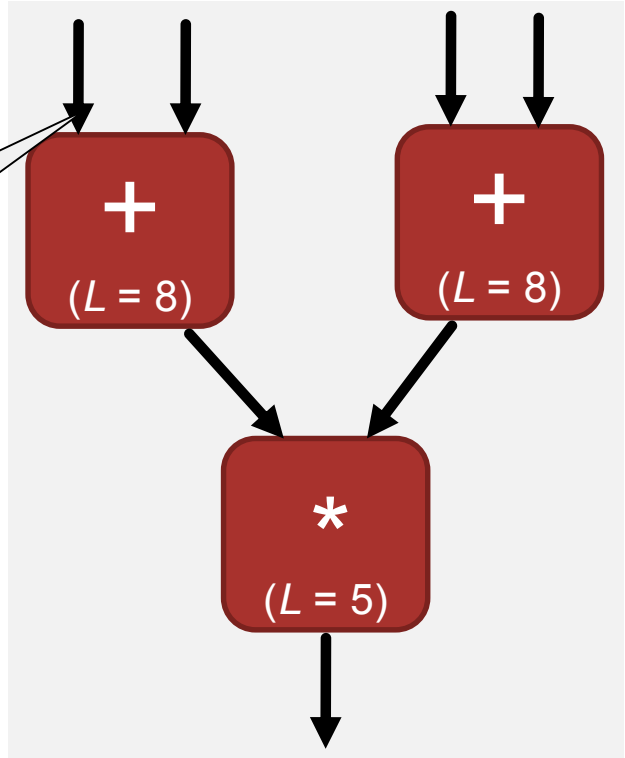


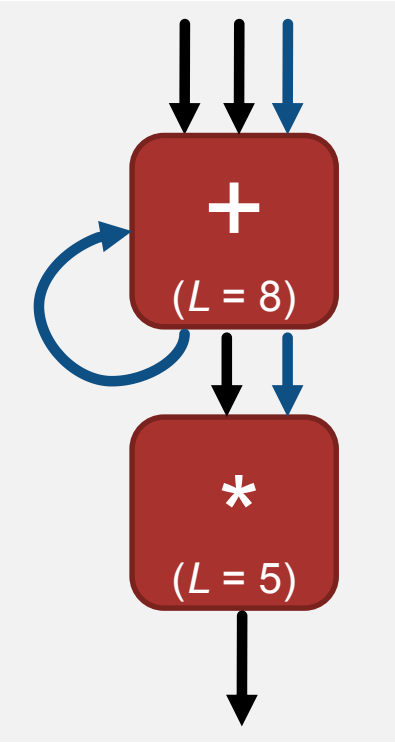


Initiation interval

In addition to **latency** (*L*), we introduce the property **initiation interval** ("II", here *I*).

Can accept all four inputs in parallel





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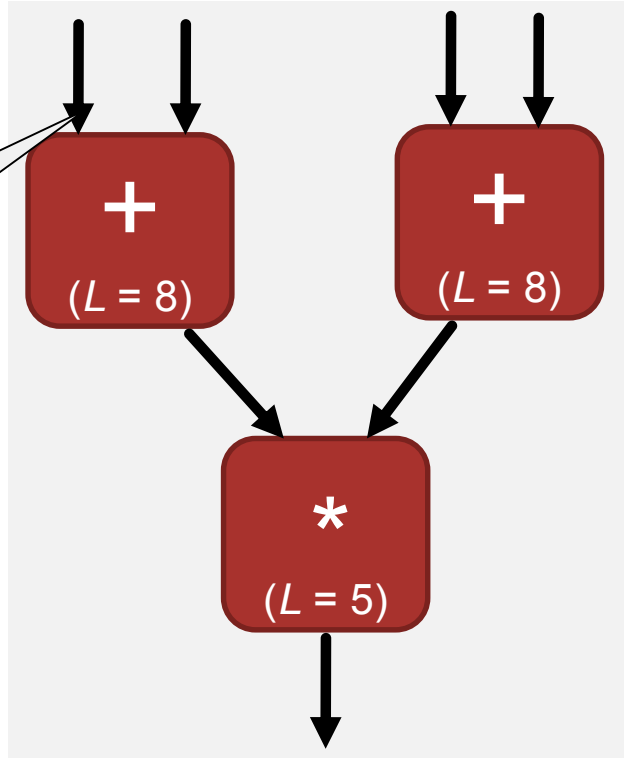

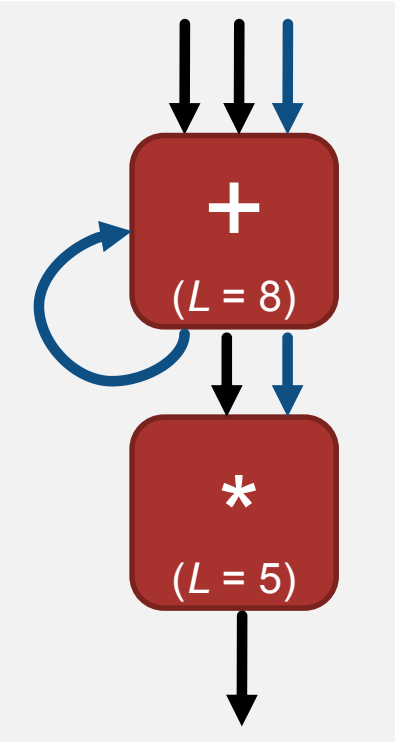

L = 13 cycles
I = 1 cycle
2 adds, 1 mult

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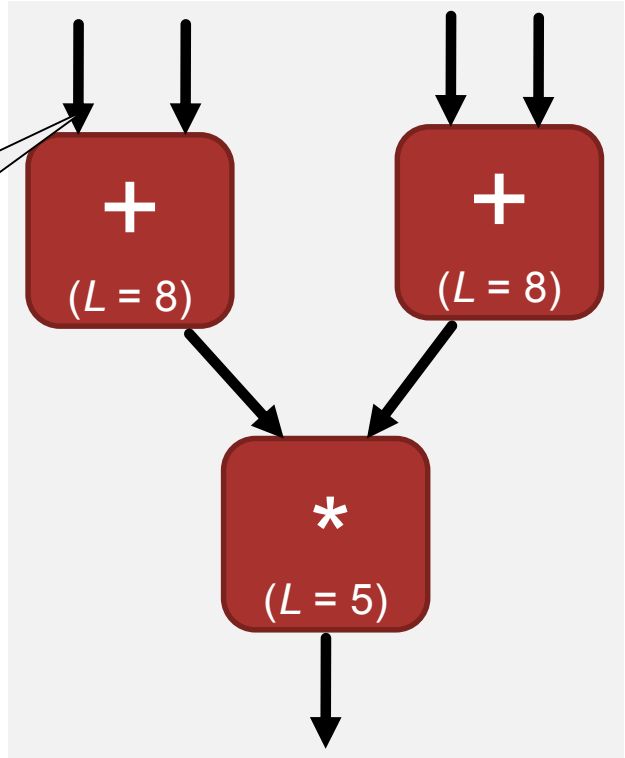
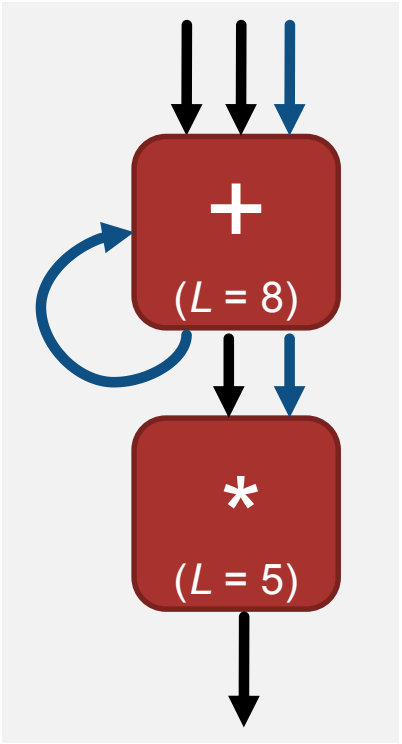
Can accept all four inputs in parallel



L = 13 cycles
I = 1 cycle
2 adds, 1 mult



L = 14 cycles
I = 2 cycles
1 add, 1 mult

Initiation interval

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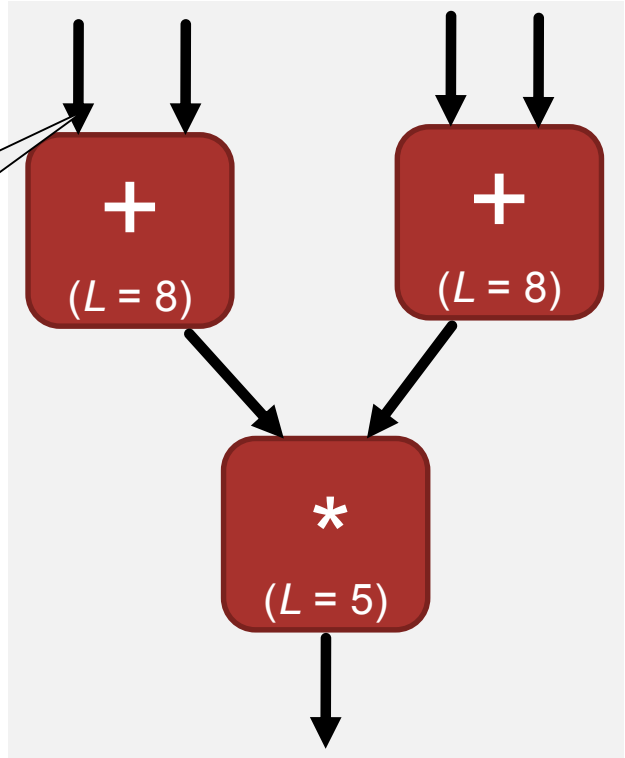
Can accept all four inputs in parallel



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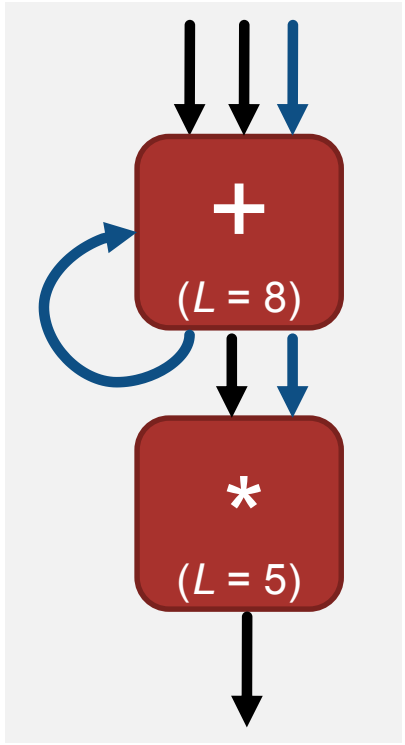

L = 14 cycles
I = 2 cycles
1 add, 1 mult
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Initiation interval

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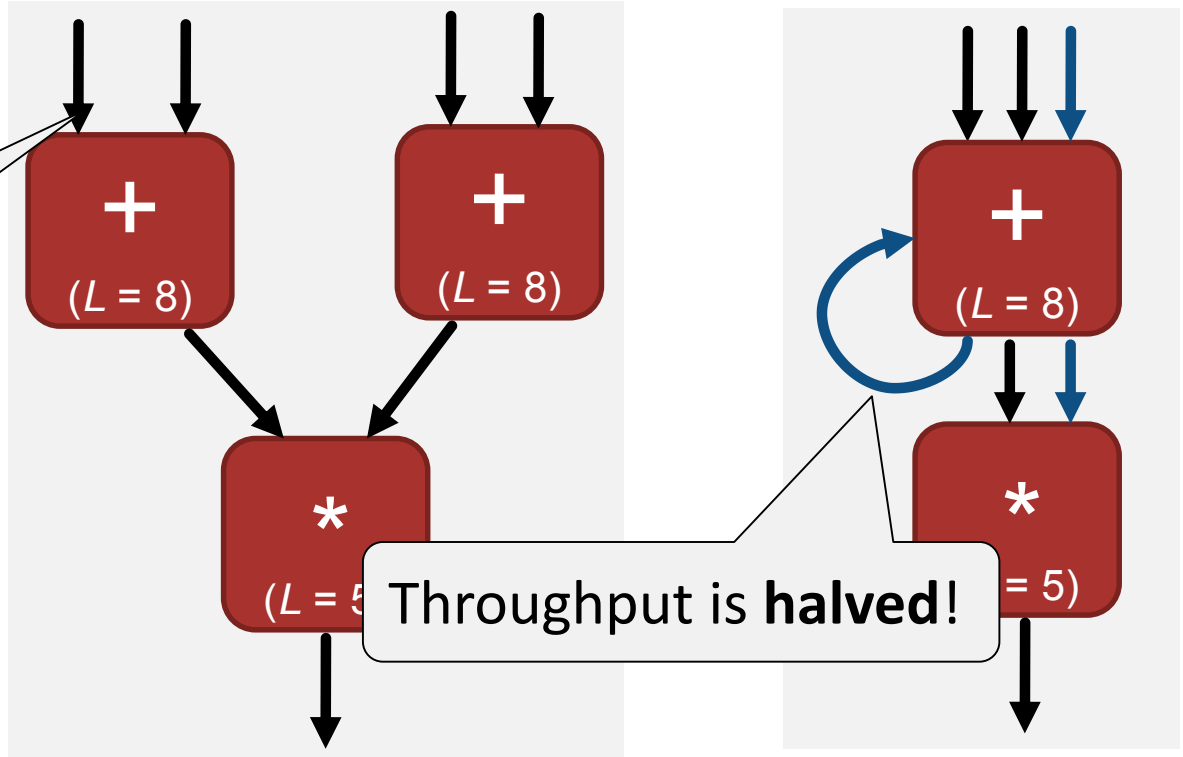

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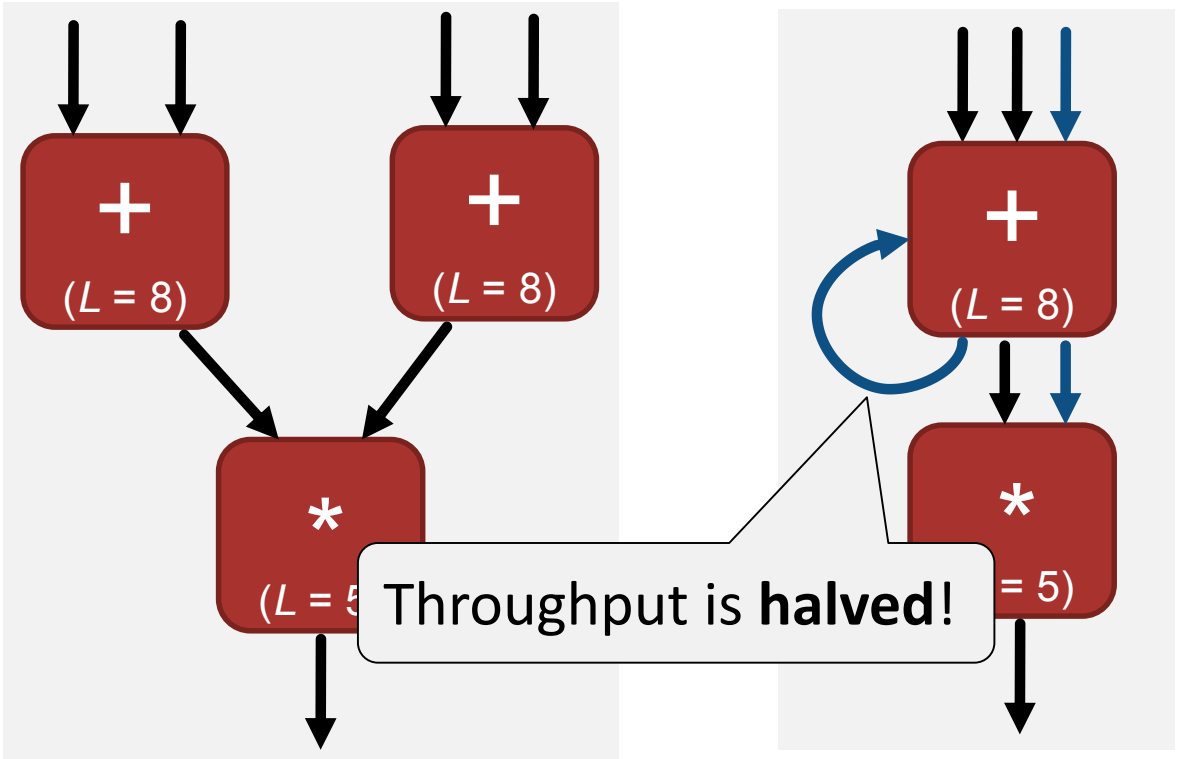

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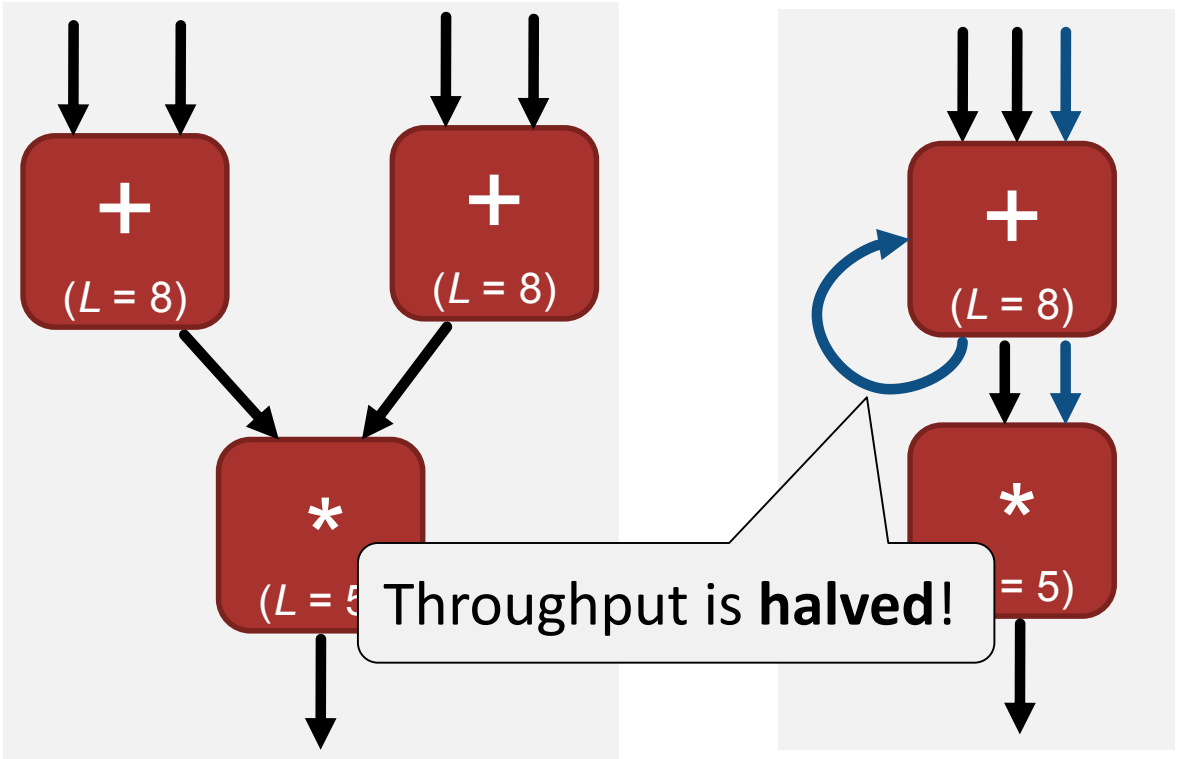
1. *No. of cycles before we can accept new inputs (sometimes called "gap")*



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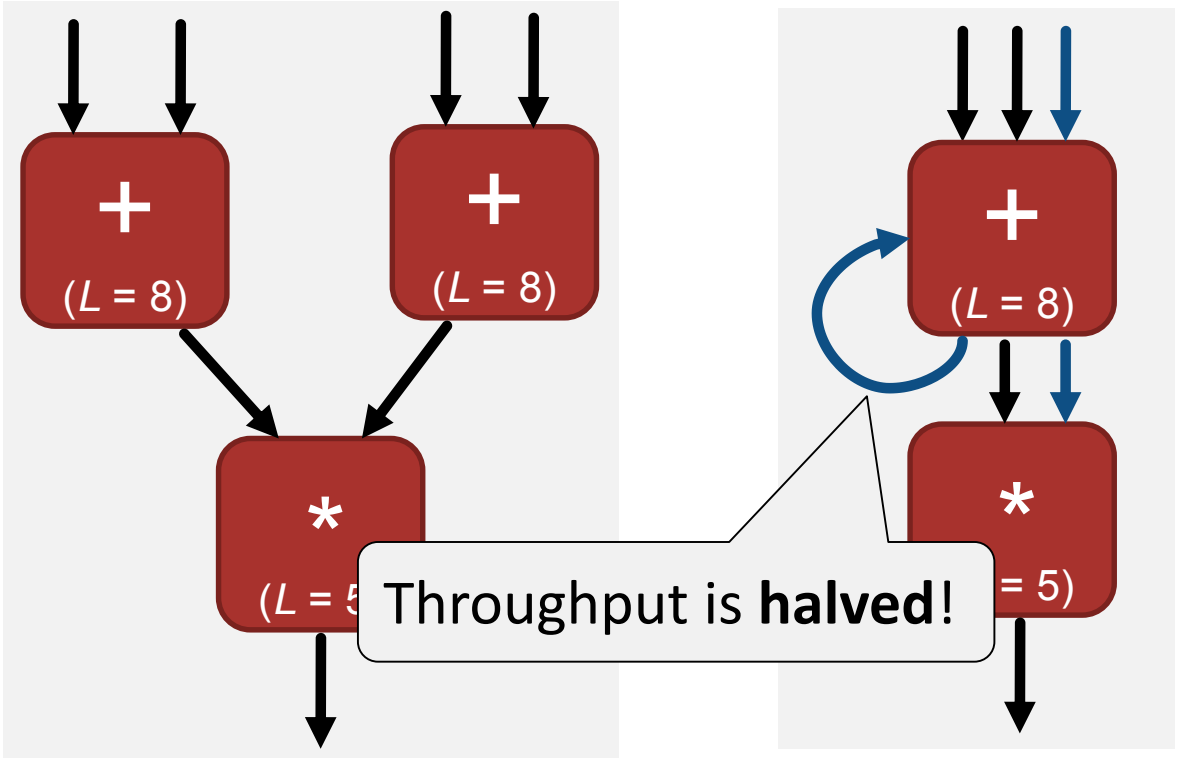
2. *Inverse throughput of the pipeline*



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Interpretations:

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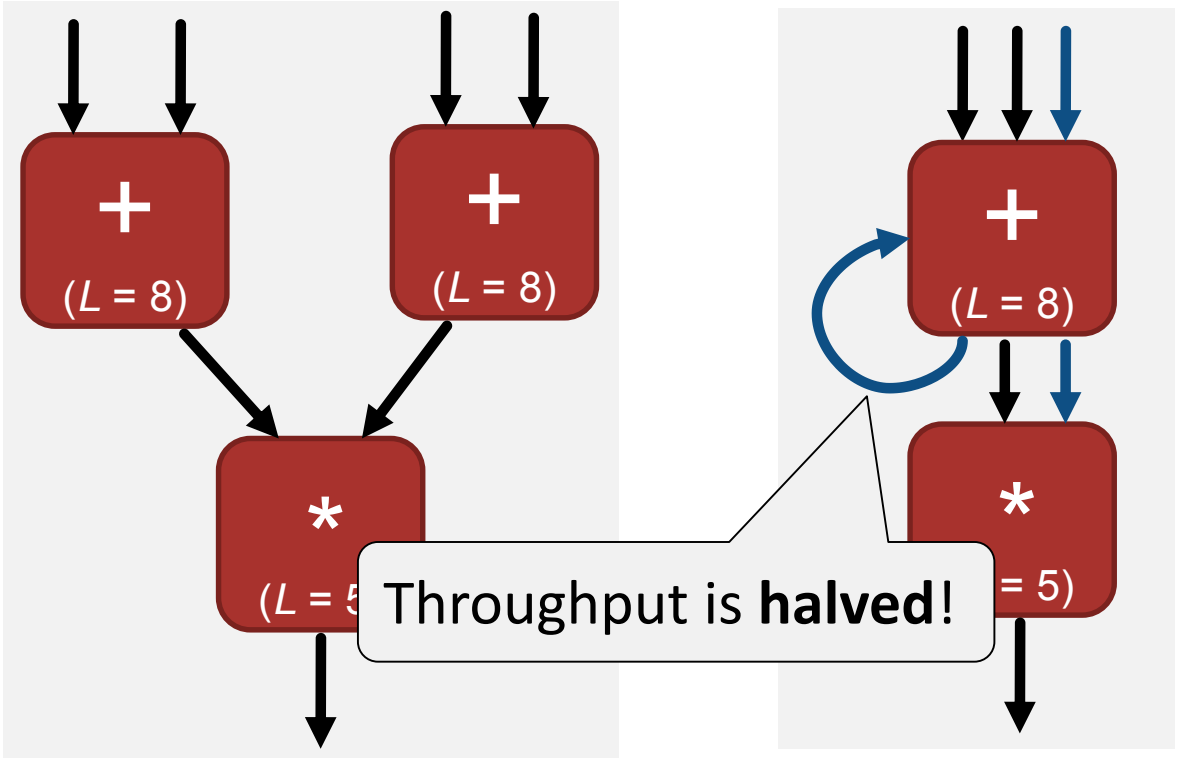
2. *Inverse throughput of the pipeline*
3. *Factor slowdown of your application ☺*



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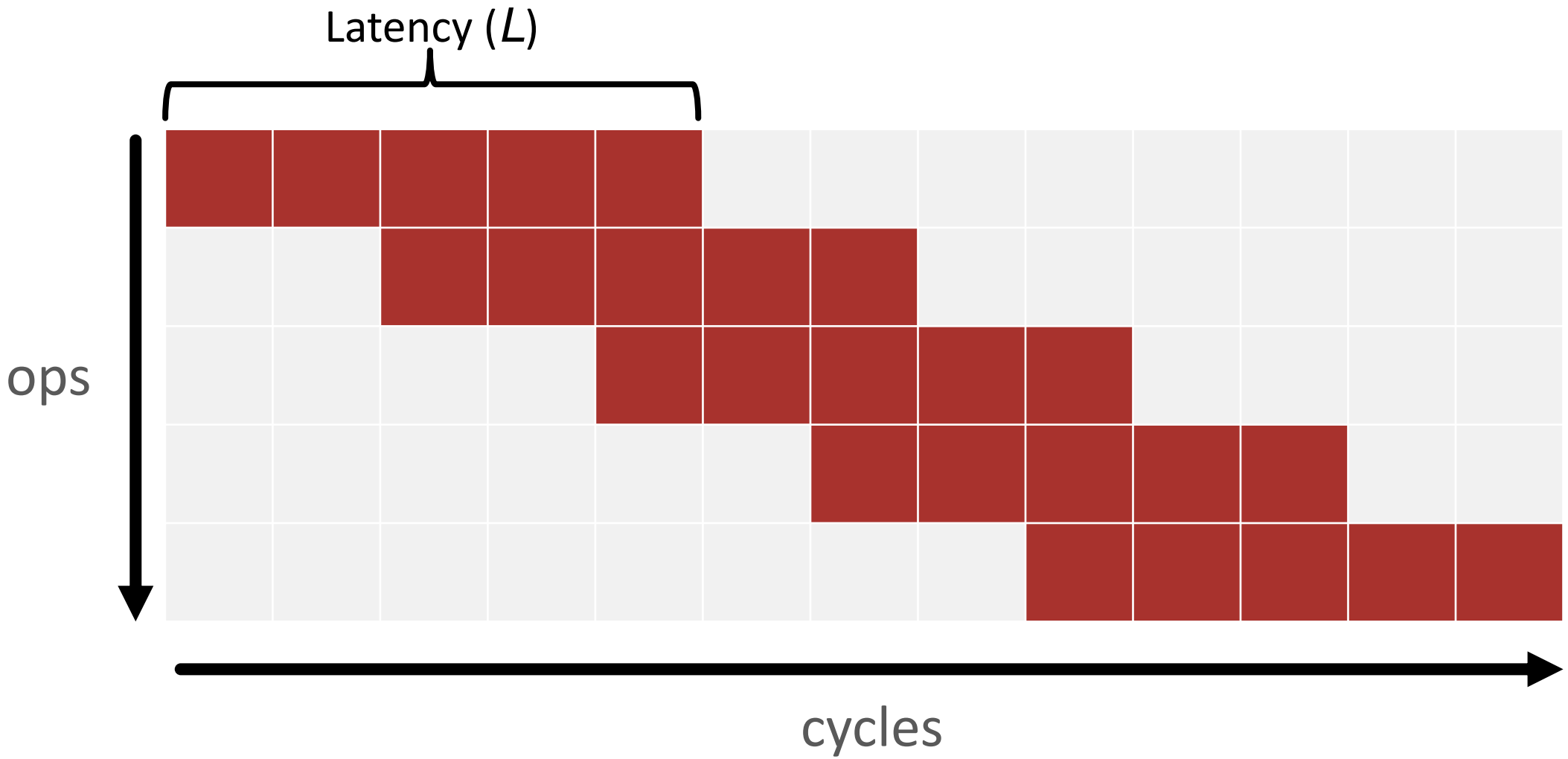
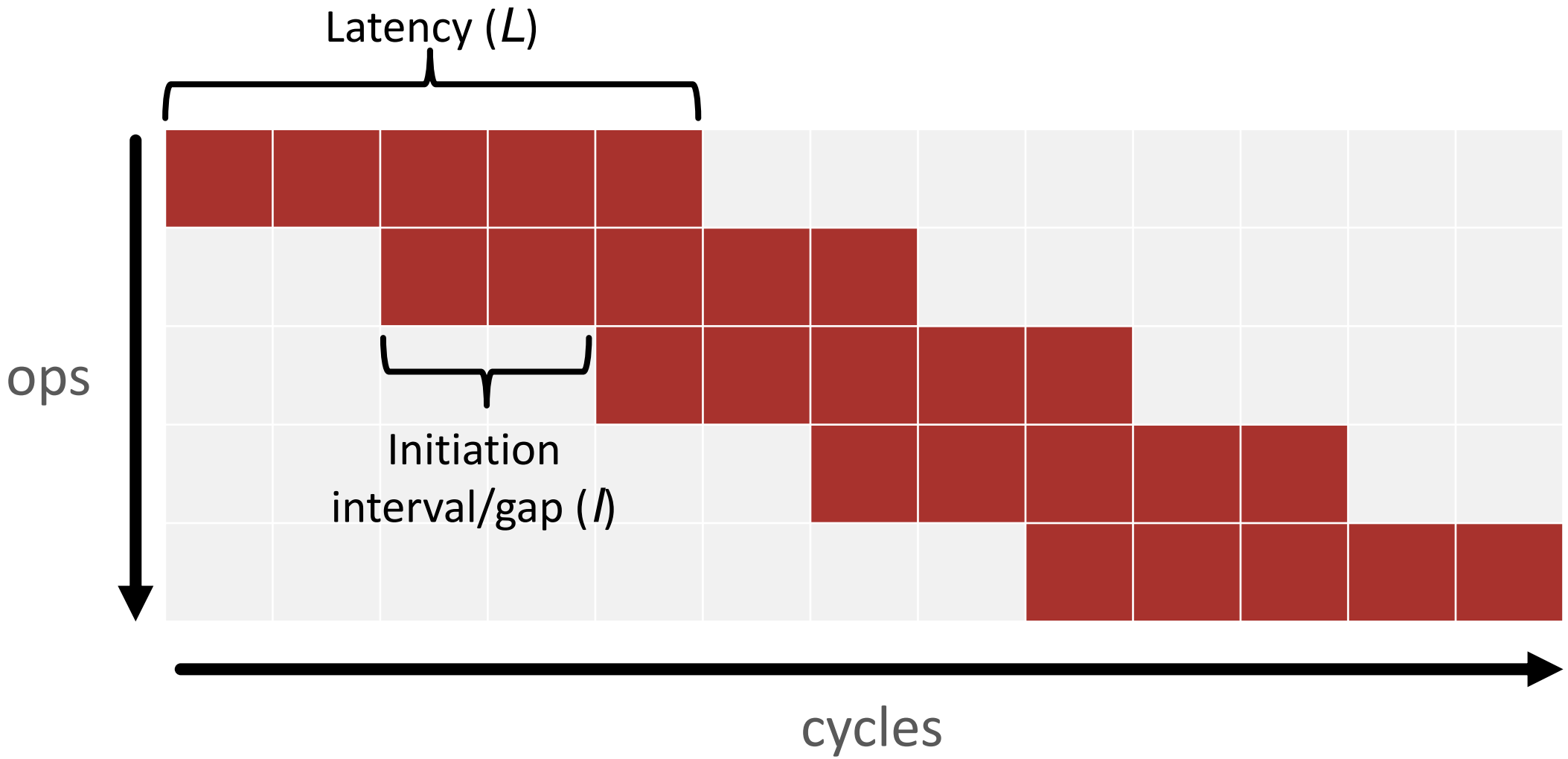
Pipelines vol. II

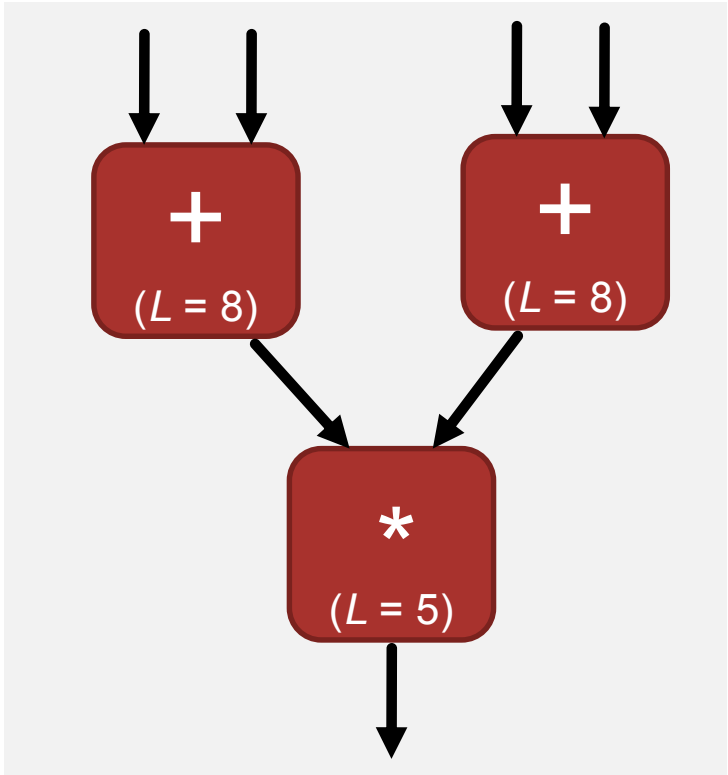


Pipelines vol. II



Adding loops

```
for (int i = 0; i < N; ++i) {
  #pragma HLS PIPELINE II=1
  c[i] = (a[i] + b[i]) *
         (a[i] - b[i]);
}
```



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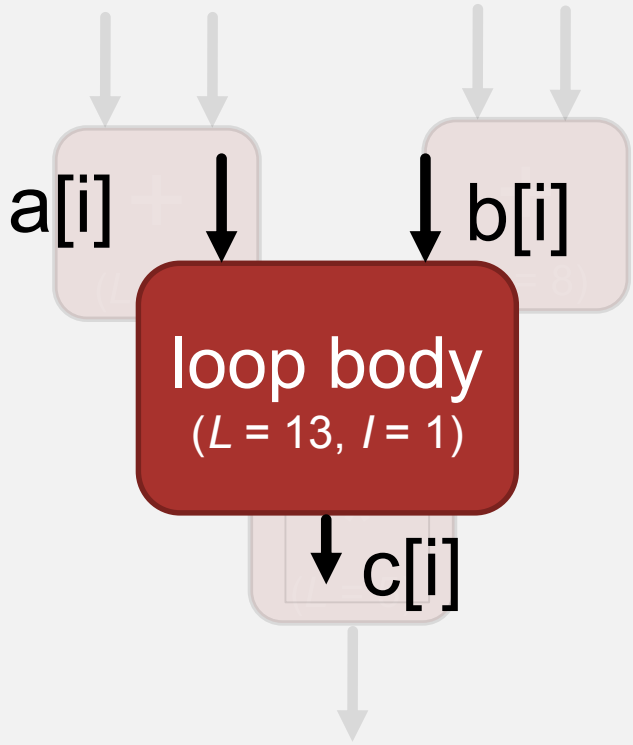

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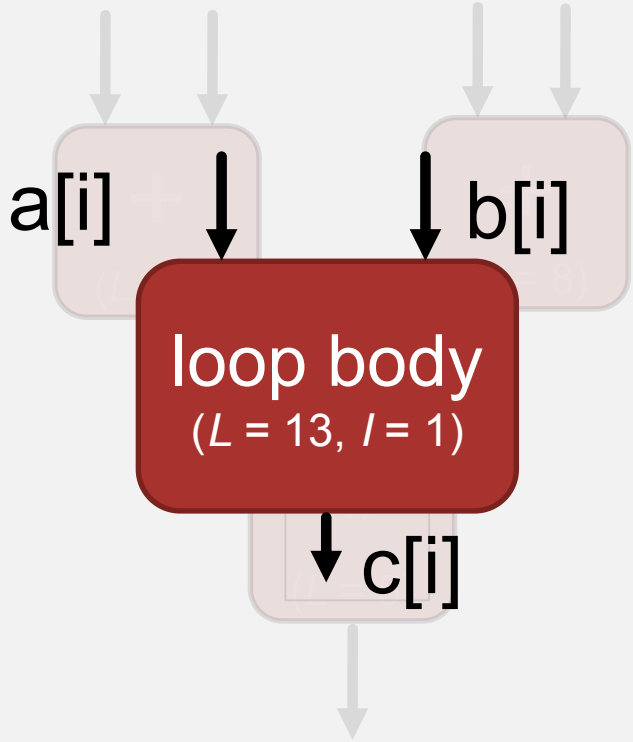
1 iteration	13 + 1 = 14 cycles
10 iterations	13 + 10 = 23 cycles
N iterations	13 + *N* cycles



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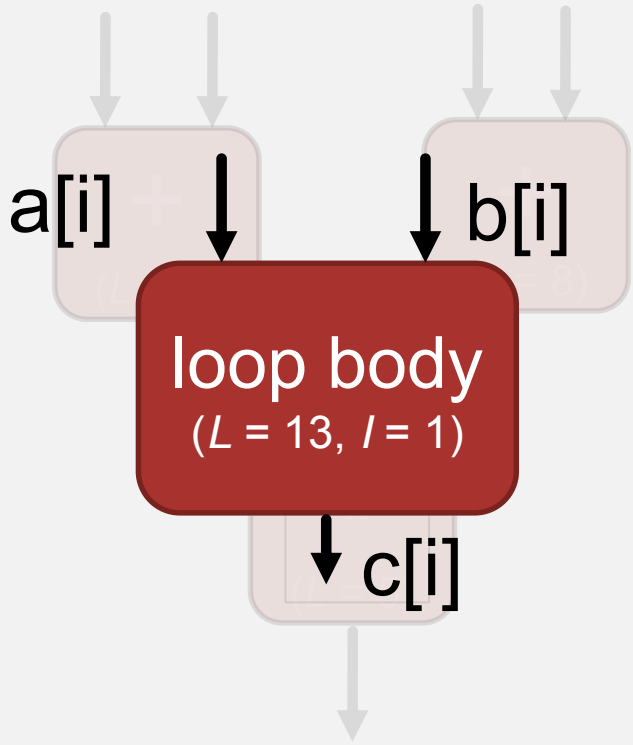

Loop iterations affect the runtime **additively**, regardless of body content

Adding loops

```
for (int i = 0; i < N; ++i) {
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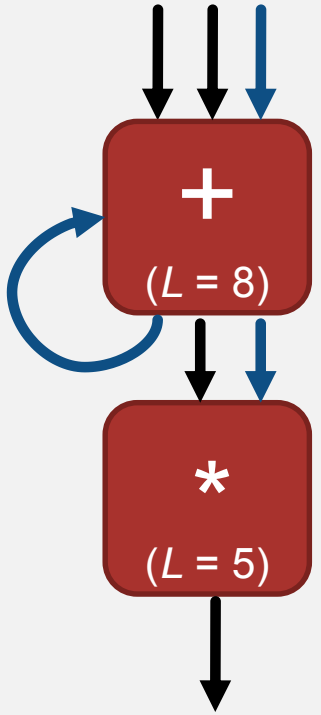

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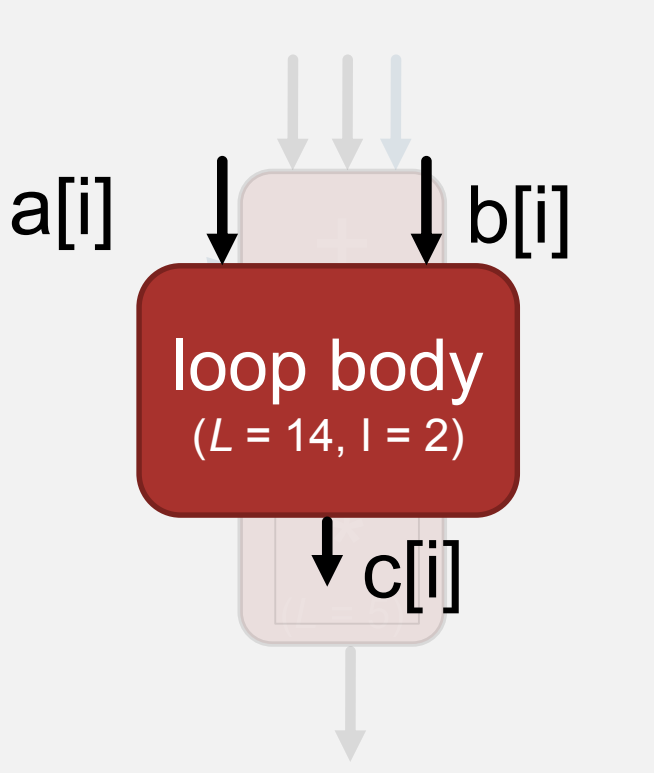

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```
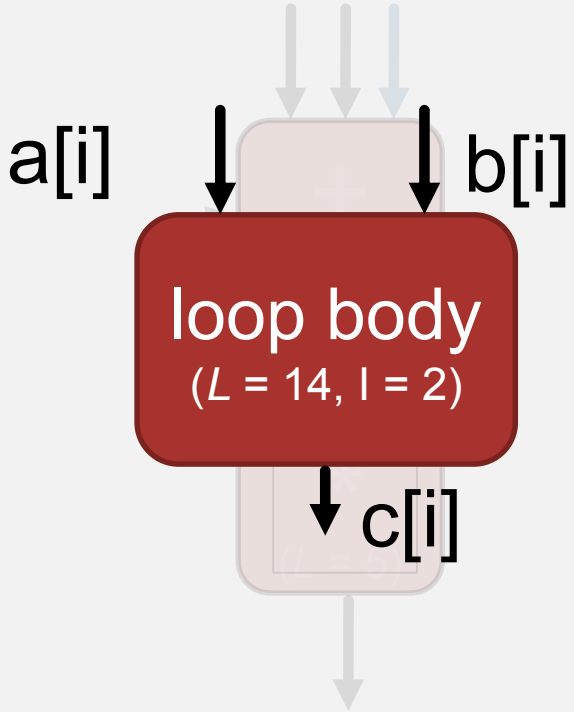

1 iteration	14 + 2 = 16 cycles
10 iterations	14 + 20 = 34 cycles
N iterations	14 + 2*N* cycles



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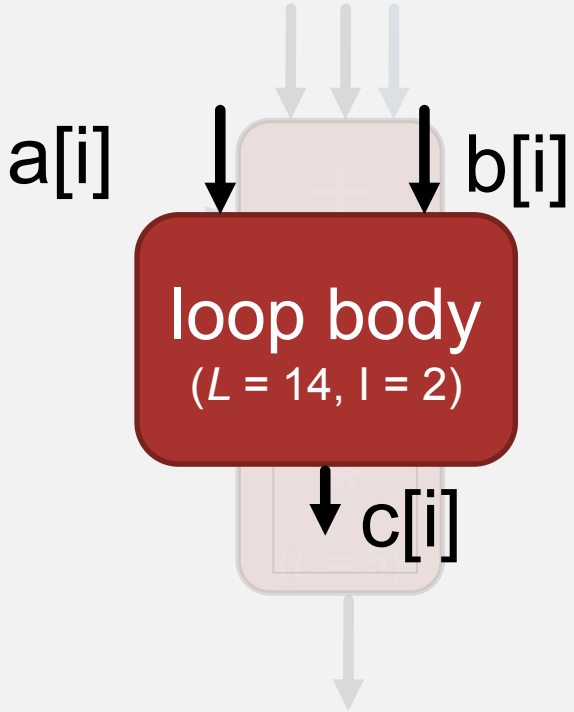

Initiation interval paid at *every iteration*

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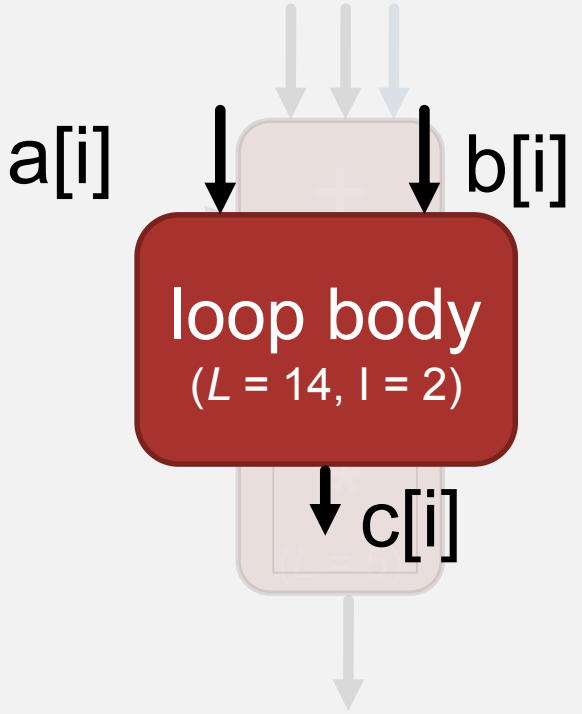
Generally:

$$L_{\text{tot}} = L + I \cdot N$$



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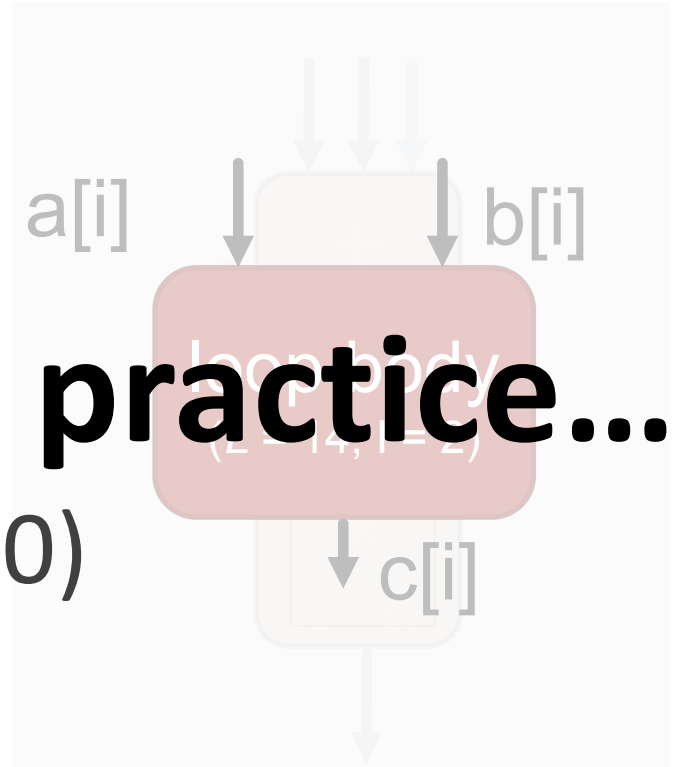

Generally:

$$L_{\text{tot}} = L + I \cdot N$$

Initiation interval paid at *every iteration*

Let's see this in practice…

(example 0)

Pipeline stalls in practice

Why do we worry so much? Just set $l = 1$…

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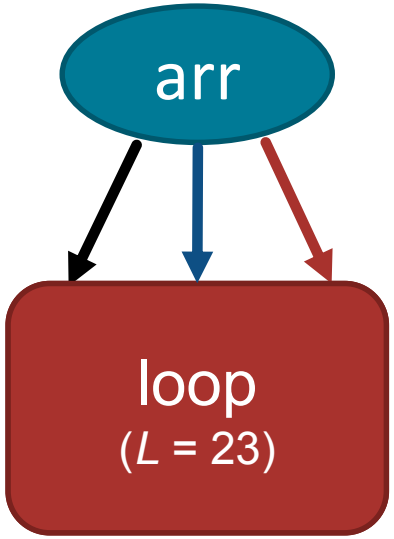

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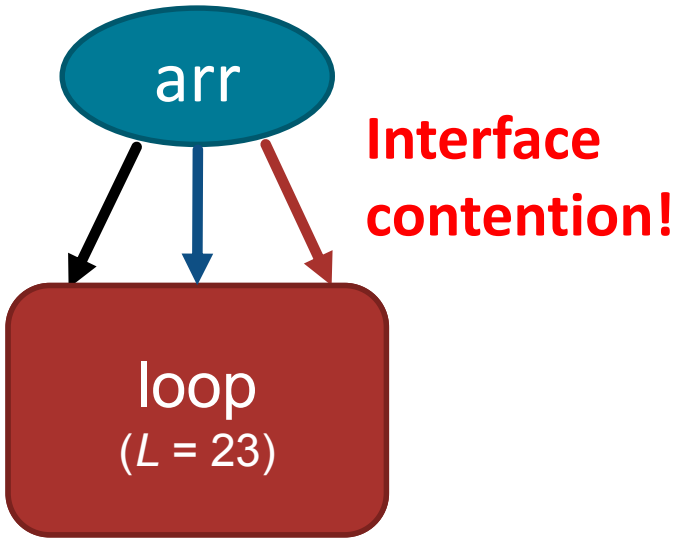

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```
for (int i = 1; i < N - 1; ++i) {
  #pragma HLS PIPELINE ~~II=1~~ II=3
  res[i] = 0.3333 *
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}
```

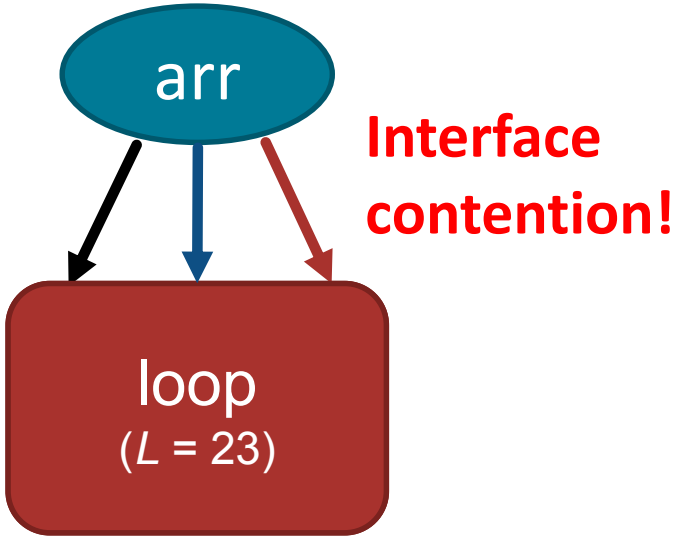

Fast memory everywhere

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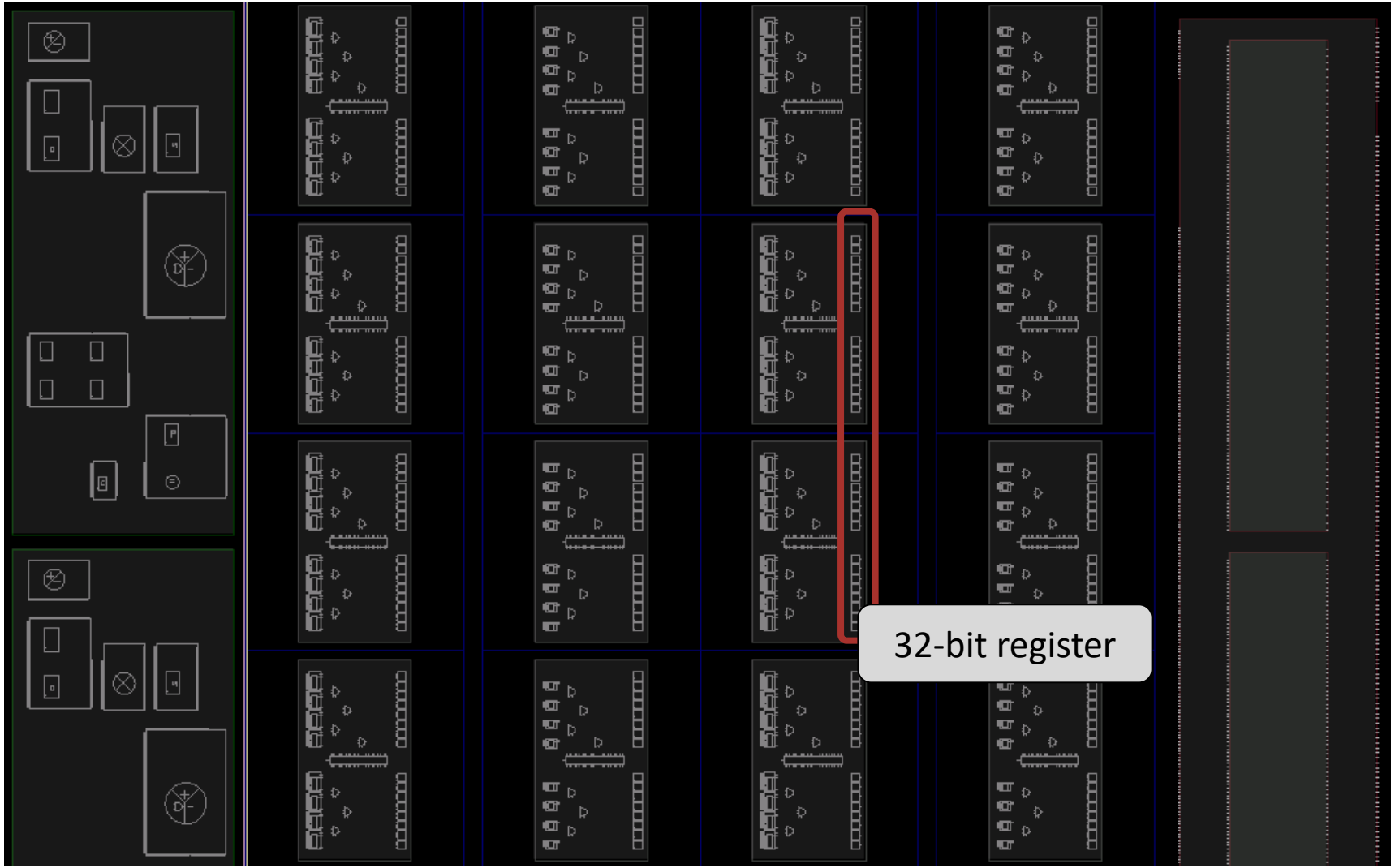

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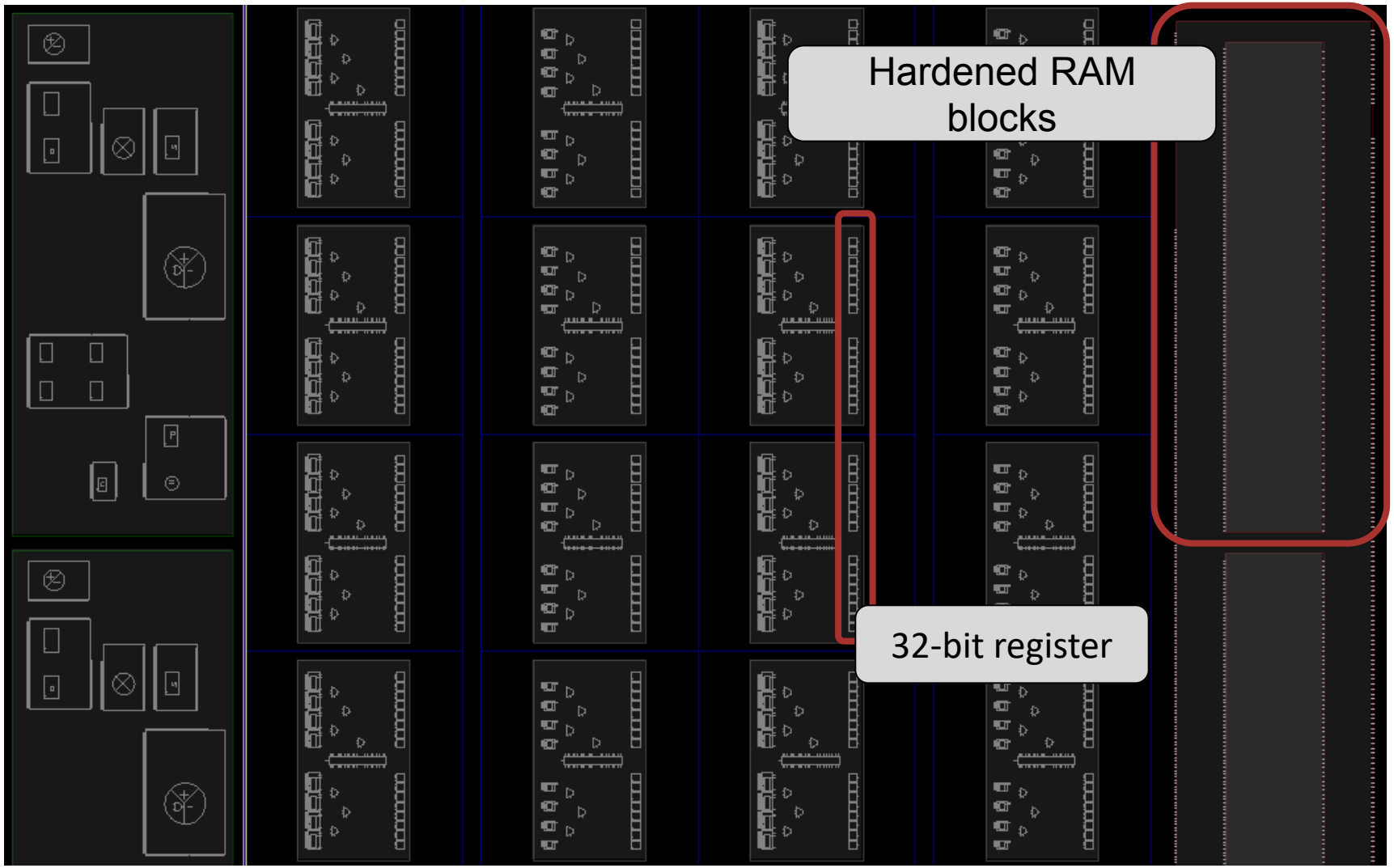

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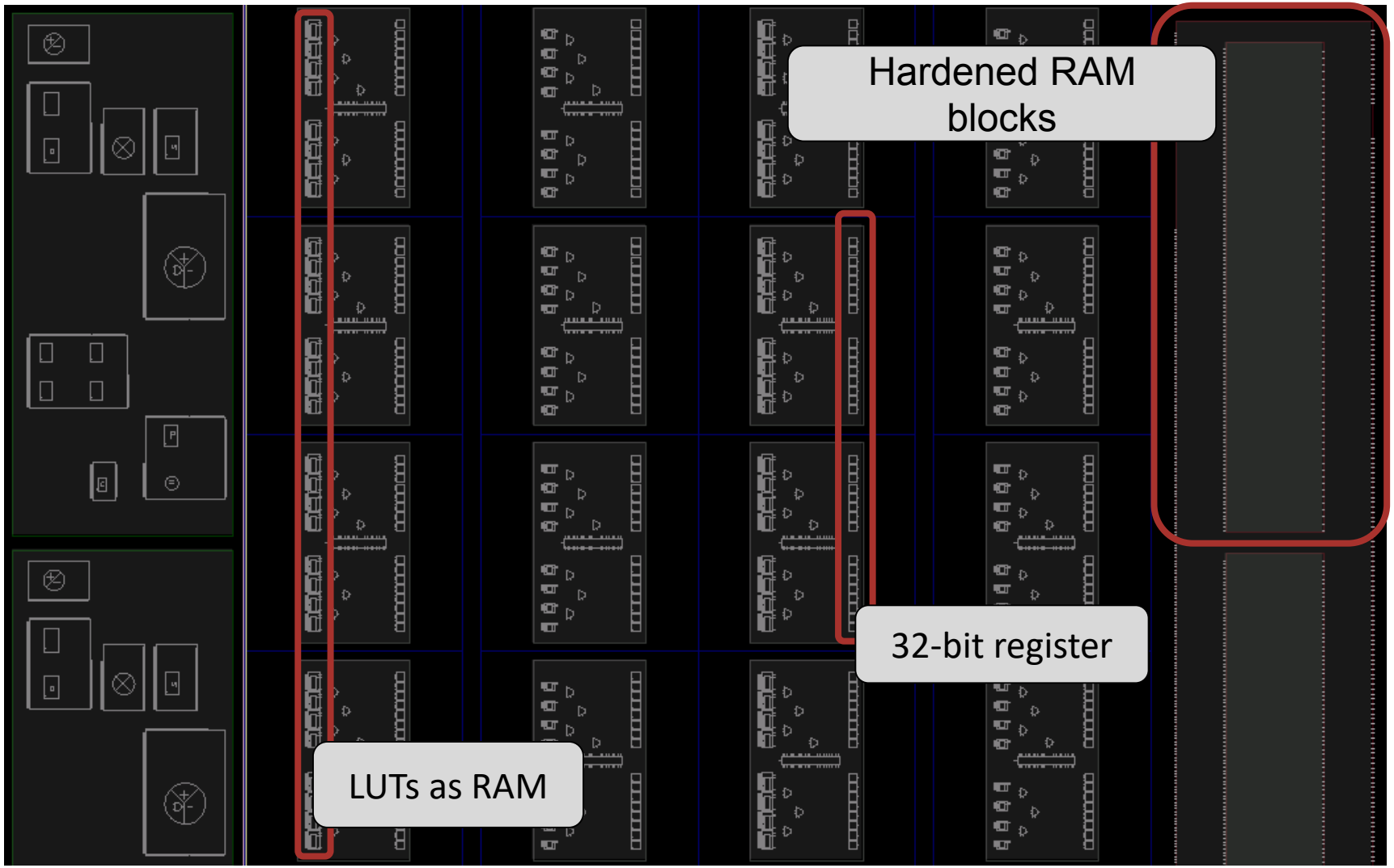

Inserting registers

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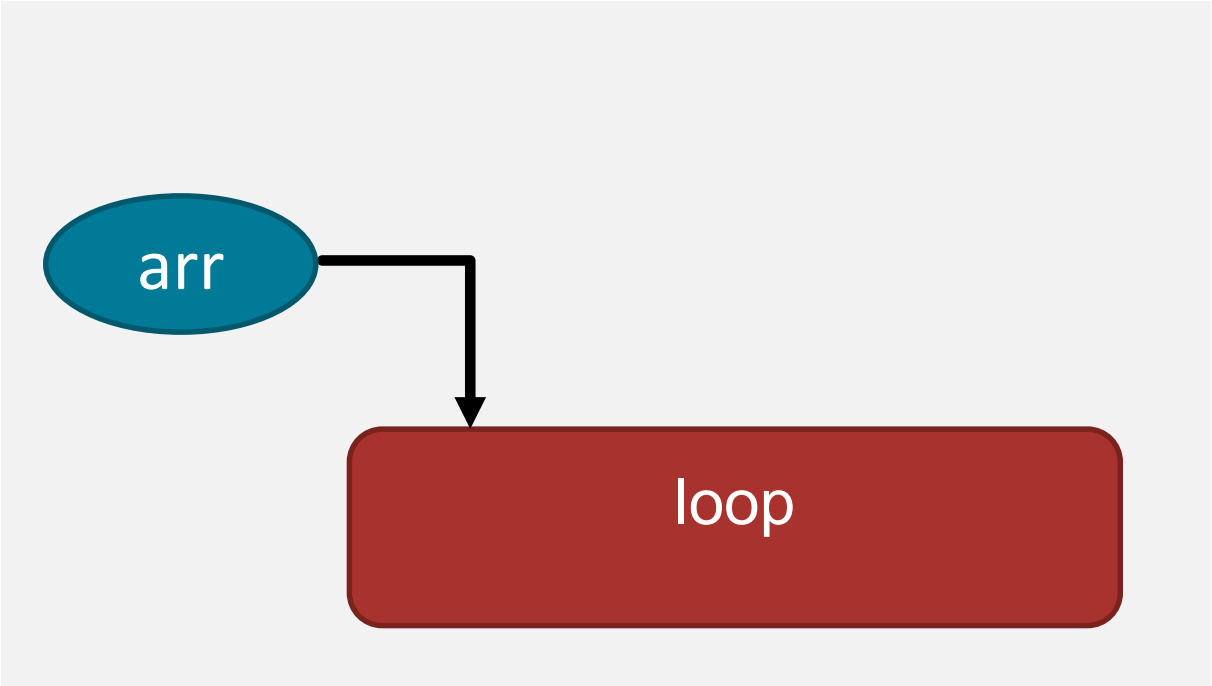

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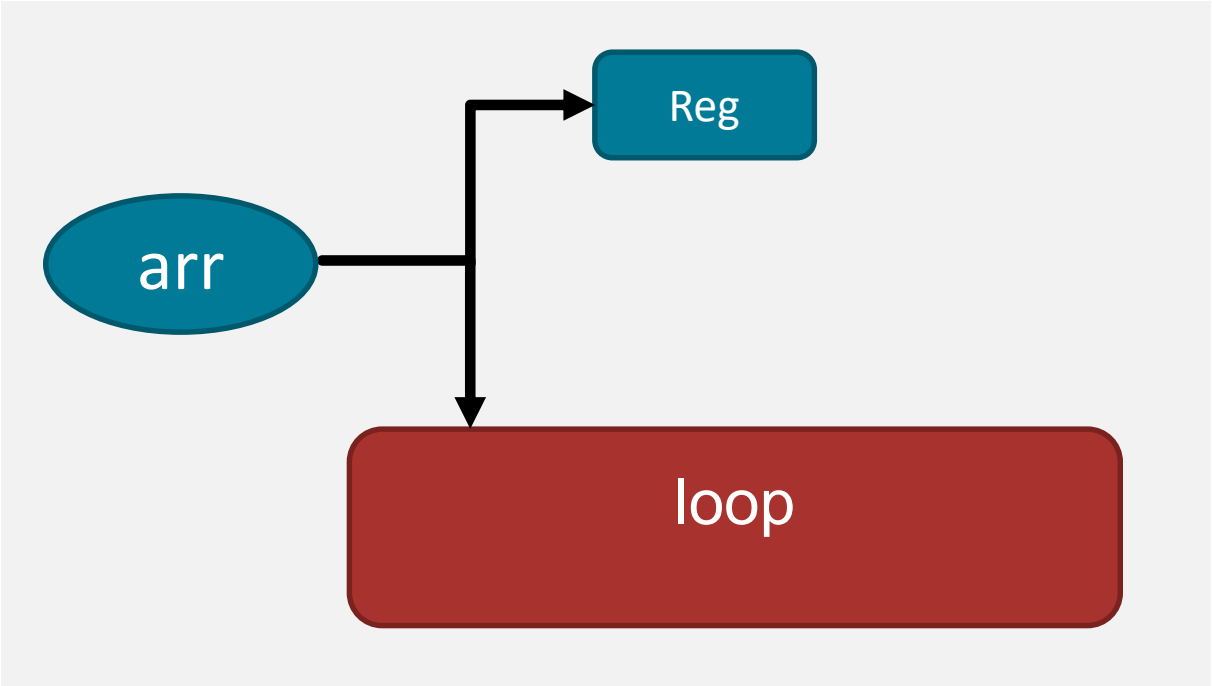

Stage 1

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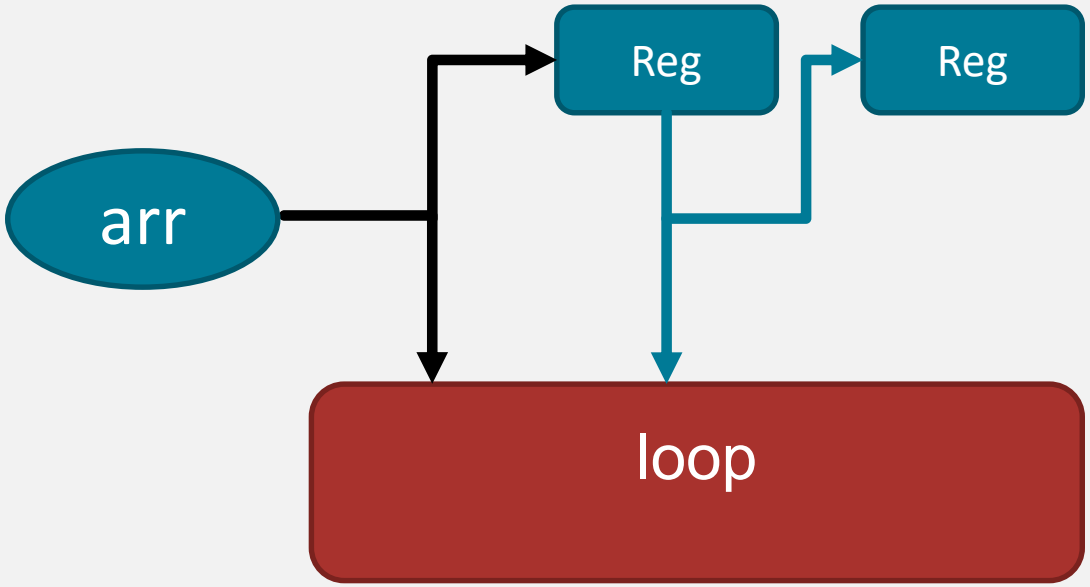
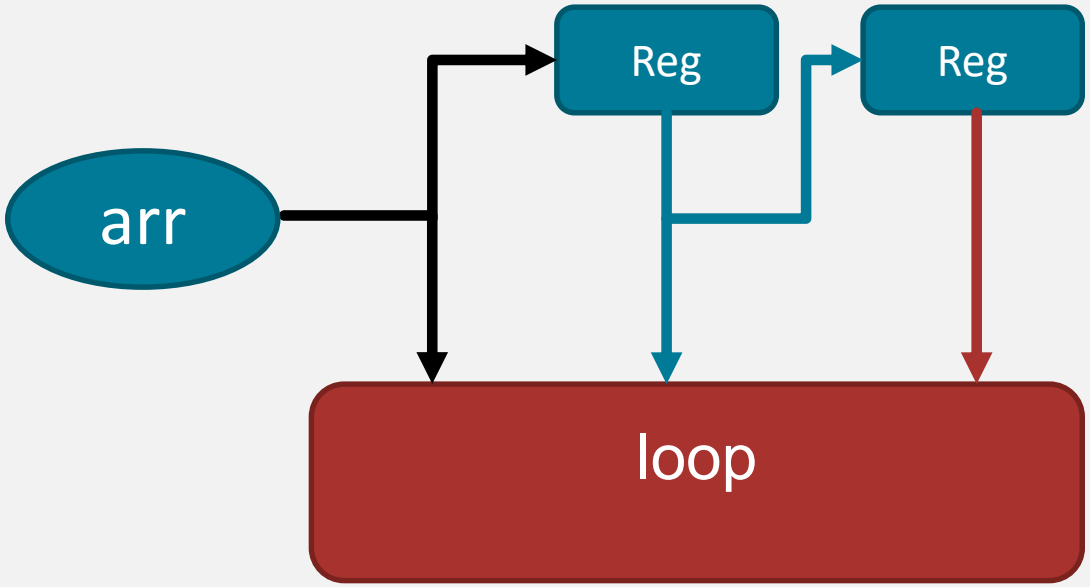


Stage 1

Stage 2

Inserting registers

```
for (int i = 1; i < N - 1; ++i) {
  res[i] = 0.3333 *
    (arr[i-1] + arr[i] + arr[i+1]);
}
```



Stage 1

Stage 2

Stage 3

Inserting registers

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for (int i = 1; i < N - 1; ++i) {
  res[i] = 0.3333 *
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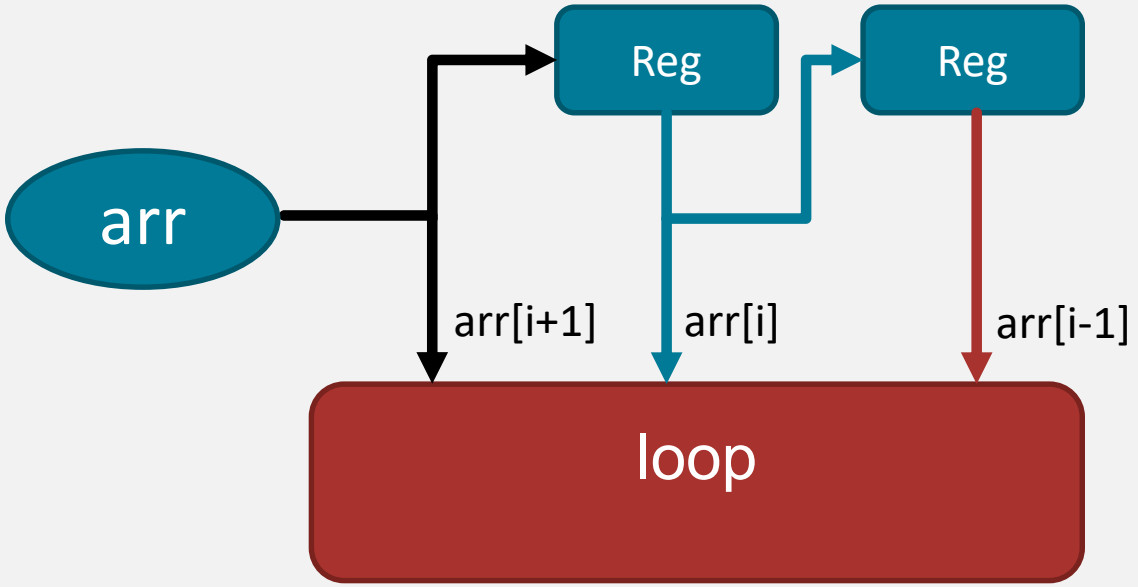
}
```



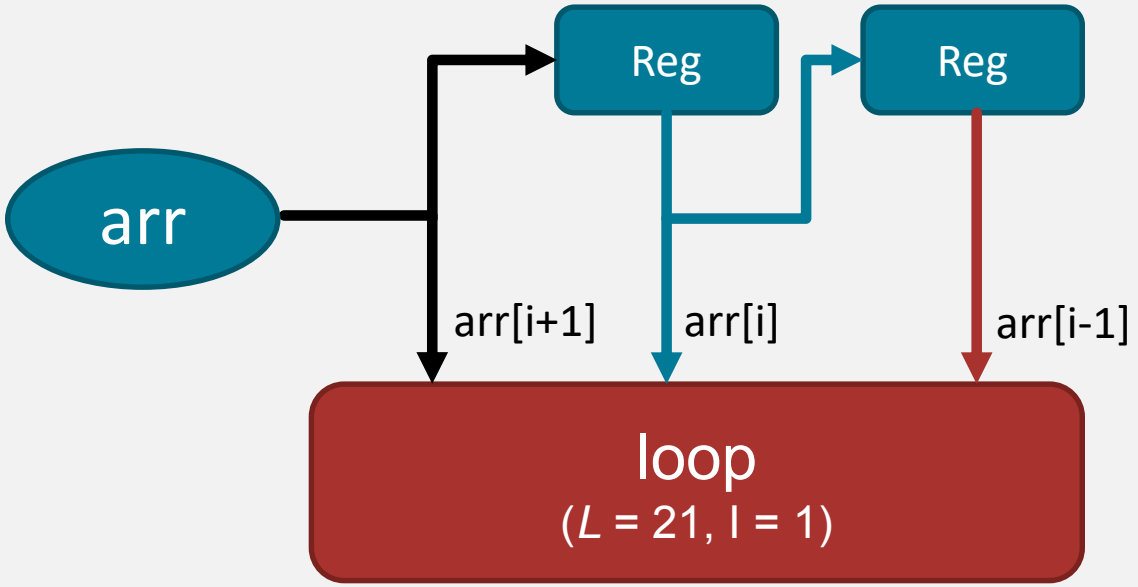
Stage 1

Stage 2

Stage 3

Inserting registers

```
for (int i = 1; i < N - 1; ++i) {
  res[i] = 0.3333 *
    (arr[i-1] + arr[i] + arr[i+1]);
}
```



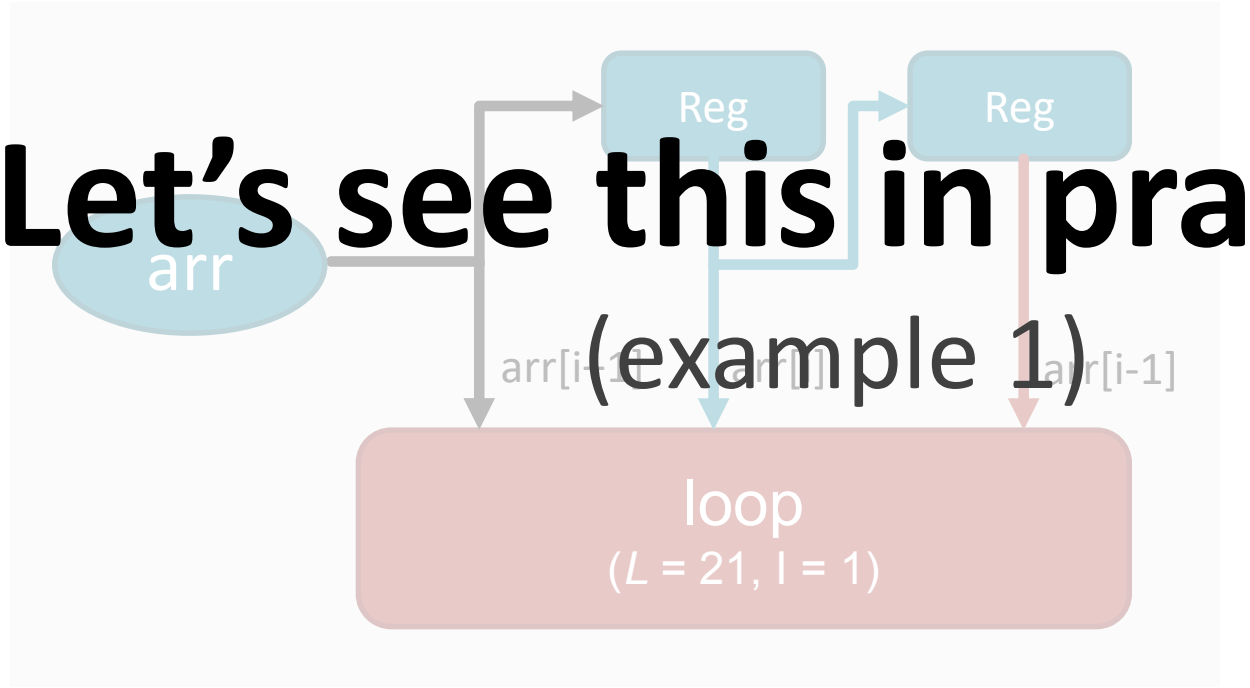
Stage 1

Stage 2

Stage 3

Inserting registers

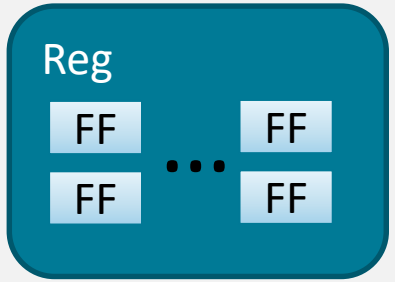
```
for (int i = 1; i < N - 1; ++i) {
  res[i] = 0.3333 *
    (arr[i-1] + arr[i] + arr[i+1]);
}
```



Let's see this in practice…

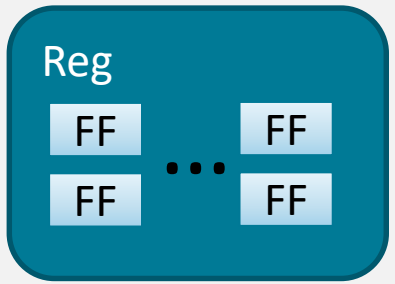
(example 1)

≥ Two classes of storage

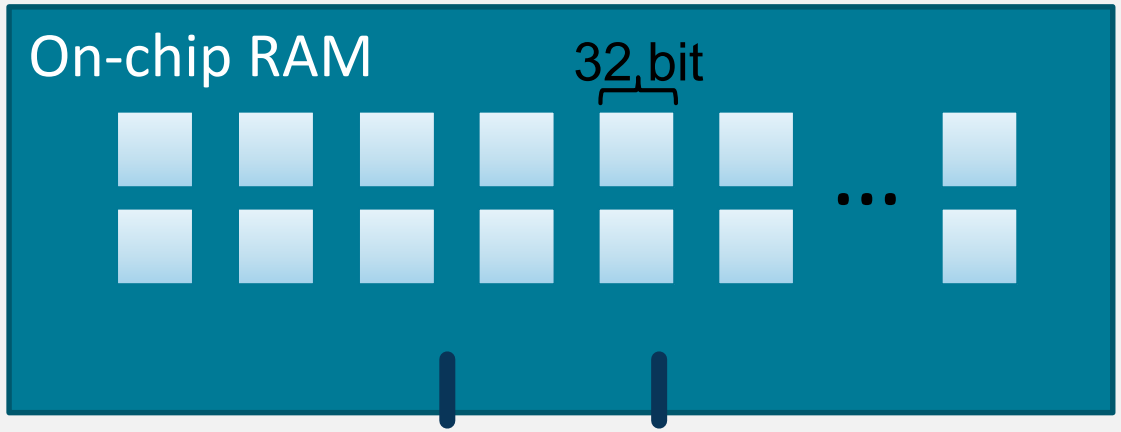


$4\ \text{Byte} = 32\ \text{bit} \cdot 1$

≥ Two classes of storage



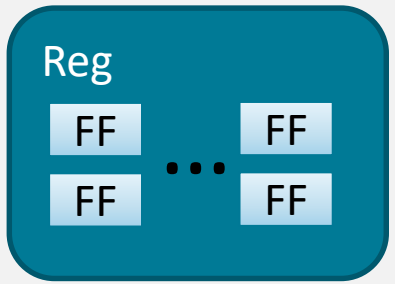
4 Byte = 32 bit · 1



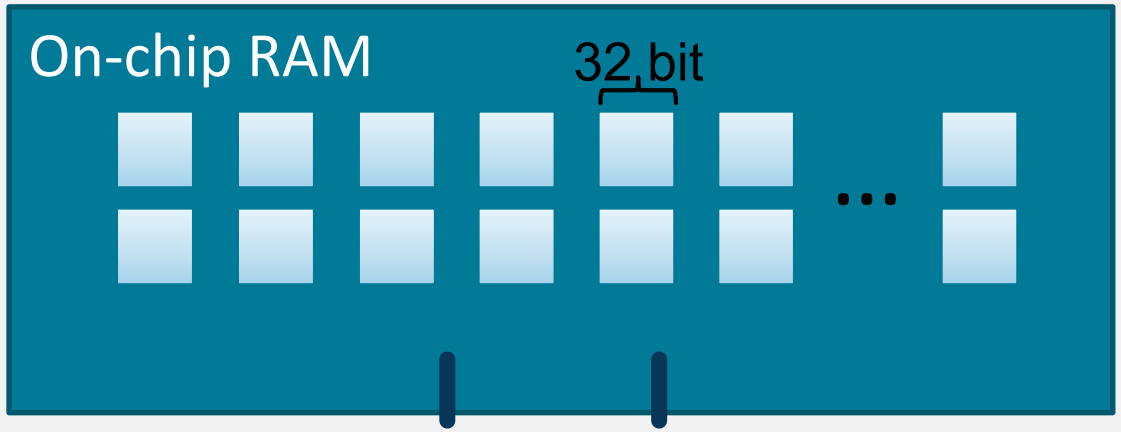
4096 Byte = 32 bit · 1024

(example configuration of Xilinx BRAM)

≥ Two classes of storage



4 Byte = 32 bit · 1

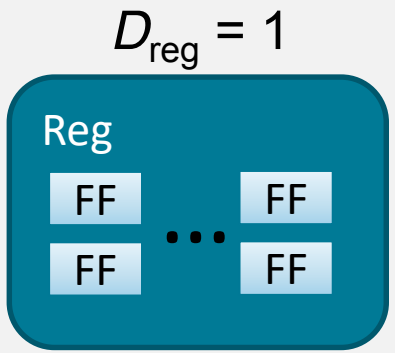


4096 Byte = 32 bit · 1024

(example configuration of Xilinx BRAM)

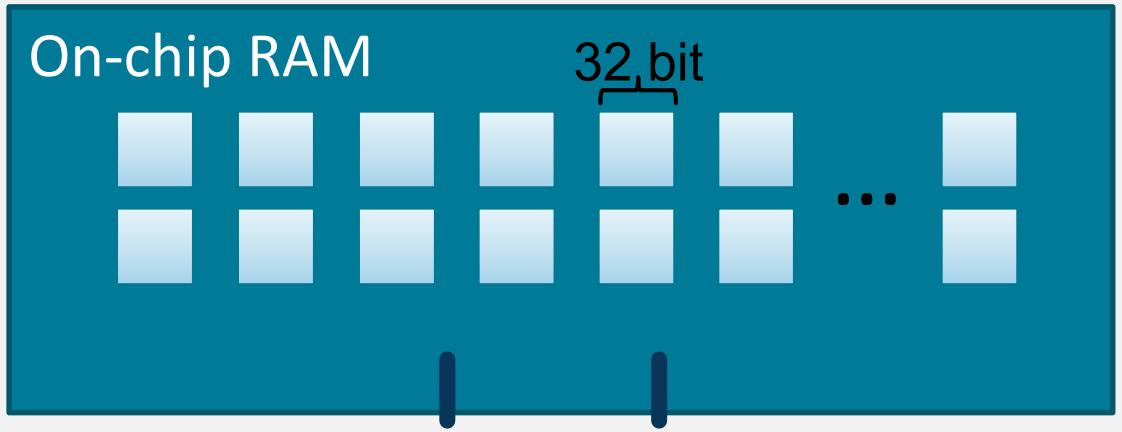
Useful to think of memory in terms of **depth** (*D*) and **width** (*W*)

≥ Two classes of storage



W_{reg} = 32 bit

4 Byte = 32 bit · 1

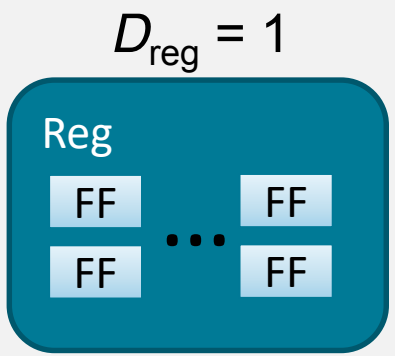


4096 Byte = 32 bit · 1024

(example configuration of Xilinx BRAM)

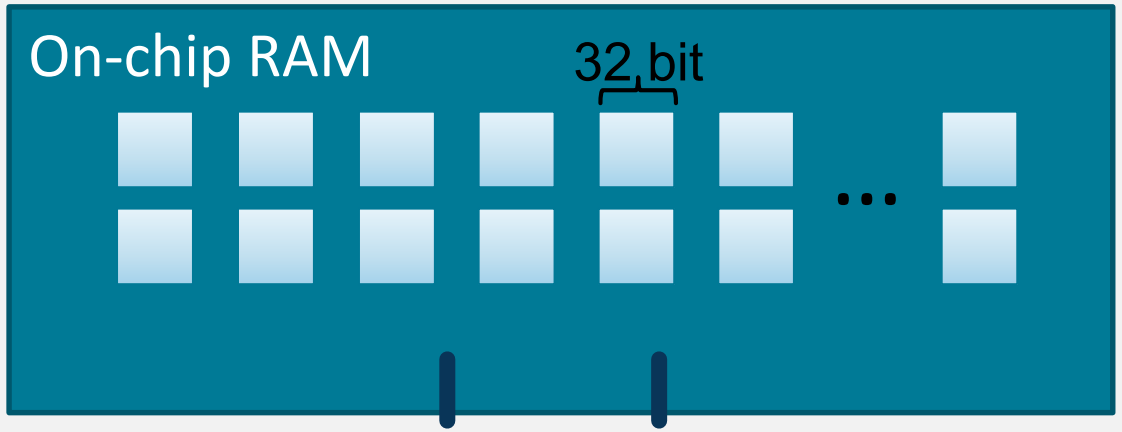
Useful to think of memory in terms of **depth** (*D*) and **width** (*W*)

≥ Two classes of storage



W_{reg} = 32 bit

4 Byte = 32 bit · 1



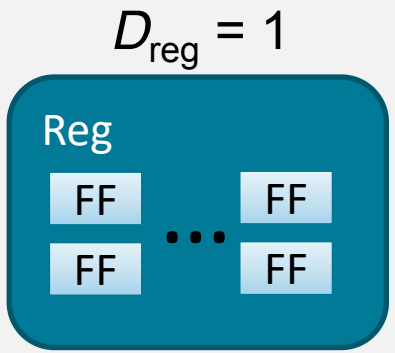
W_{RAM} = 32 bit

4096 Byte = 32 bit · 1024

(example configuration of Xilinx BRAM)

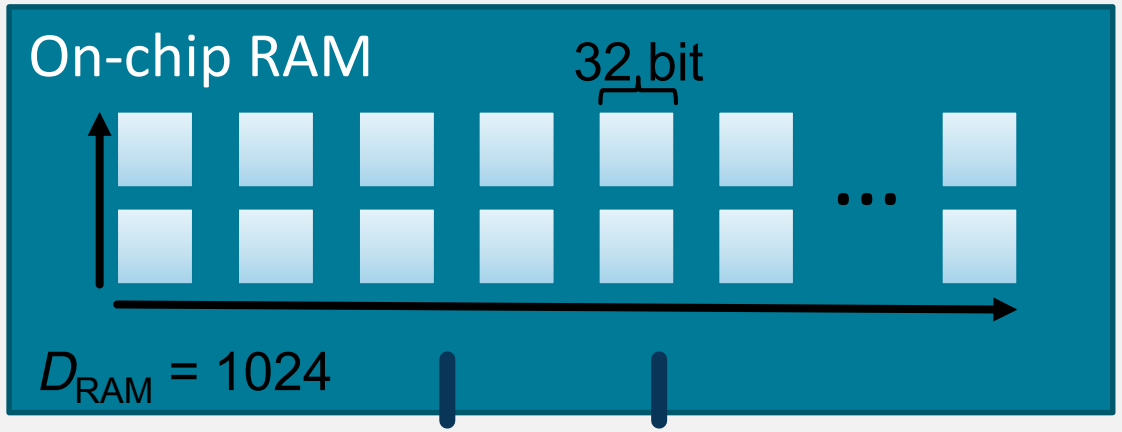
Useful to think of memory in terms of **depth** (*D*) and **width** (*W*)

≥ Two classes of storage



W_{reg} = 32 bit

4 Byte = 32 bit · 1



W_{RAM} = 32 bit

4096 Byte = 32 bit · 1024

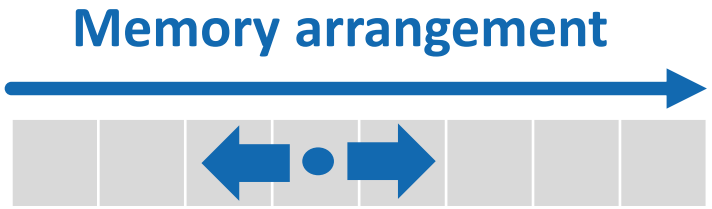
(example configuration of Xilinx BRAM)

Useful to think of memory in terms of **depth** (*D*) and **width** (*W*)

Buffer depth

1D stencil program:

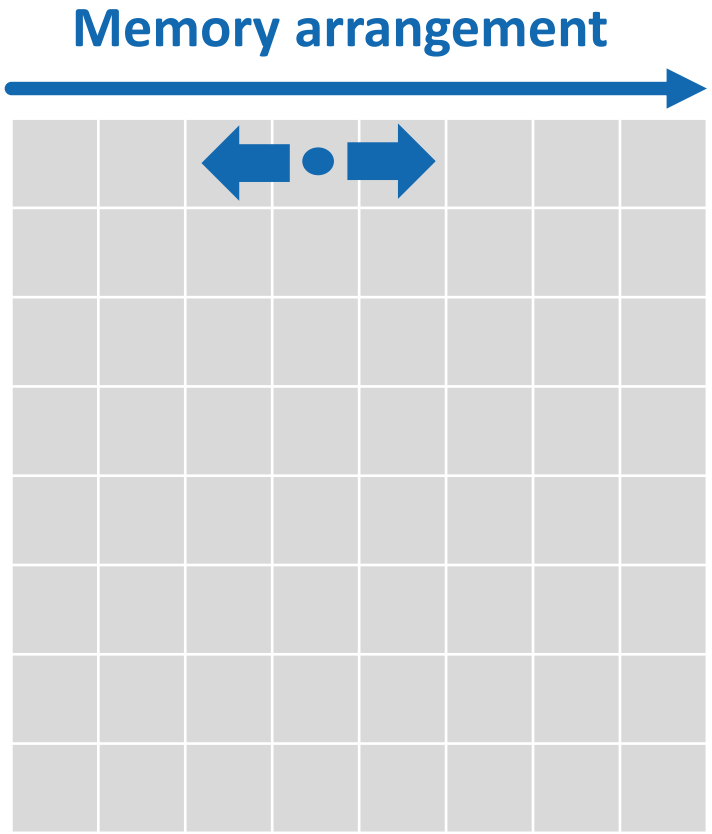
$W = 2,\ D = 1$



Buffer depth

1D stencil program:

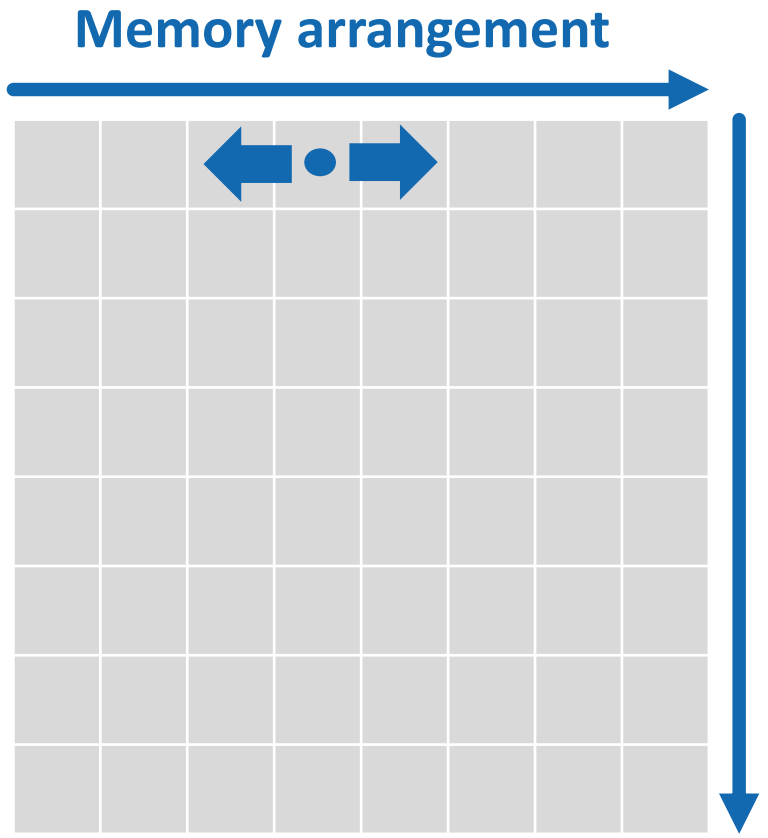
$W = 2,\ D = 1$



Buffer depth

1D stencil program:

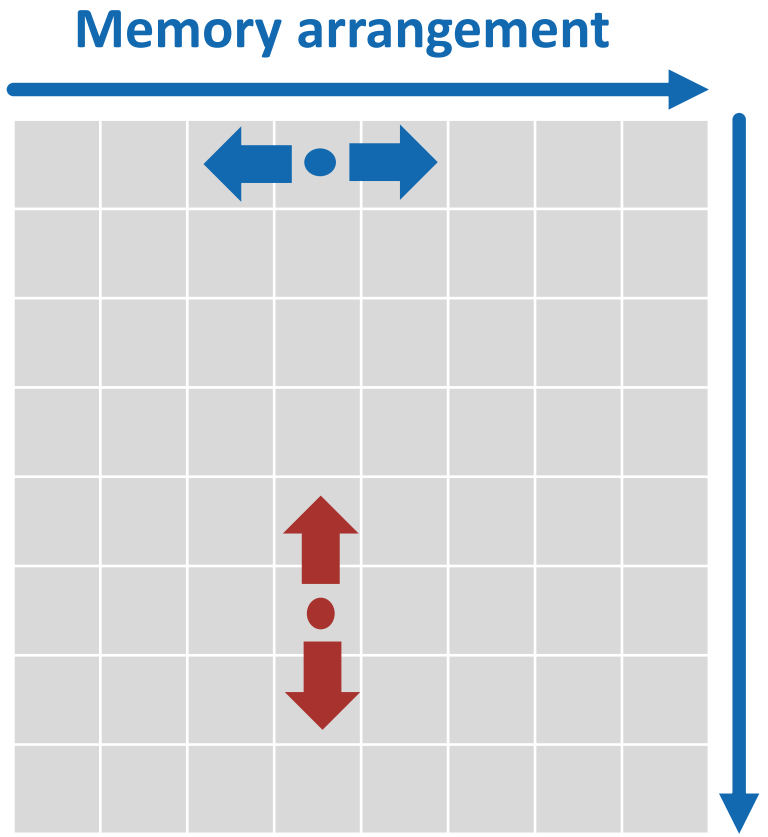
$W = 2,\ D = 1$



Buffer depth

1D stencil program:

$W = 2,\ D = 1$



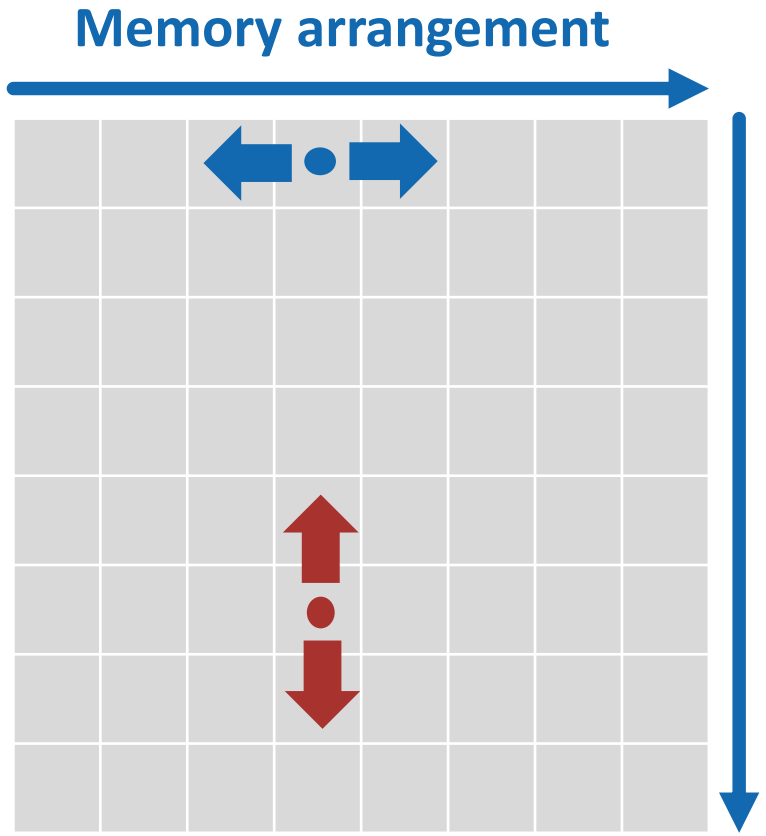
Buffer depth

1D stencil program:

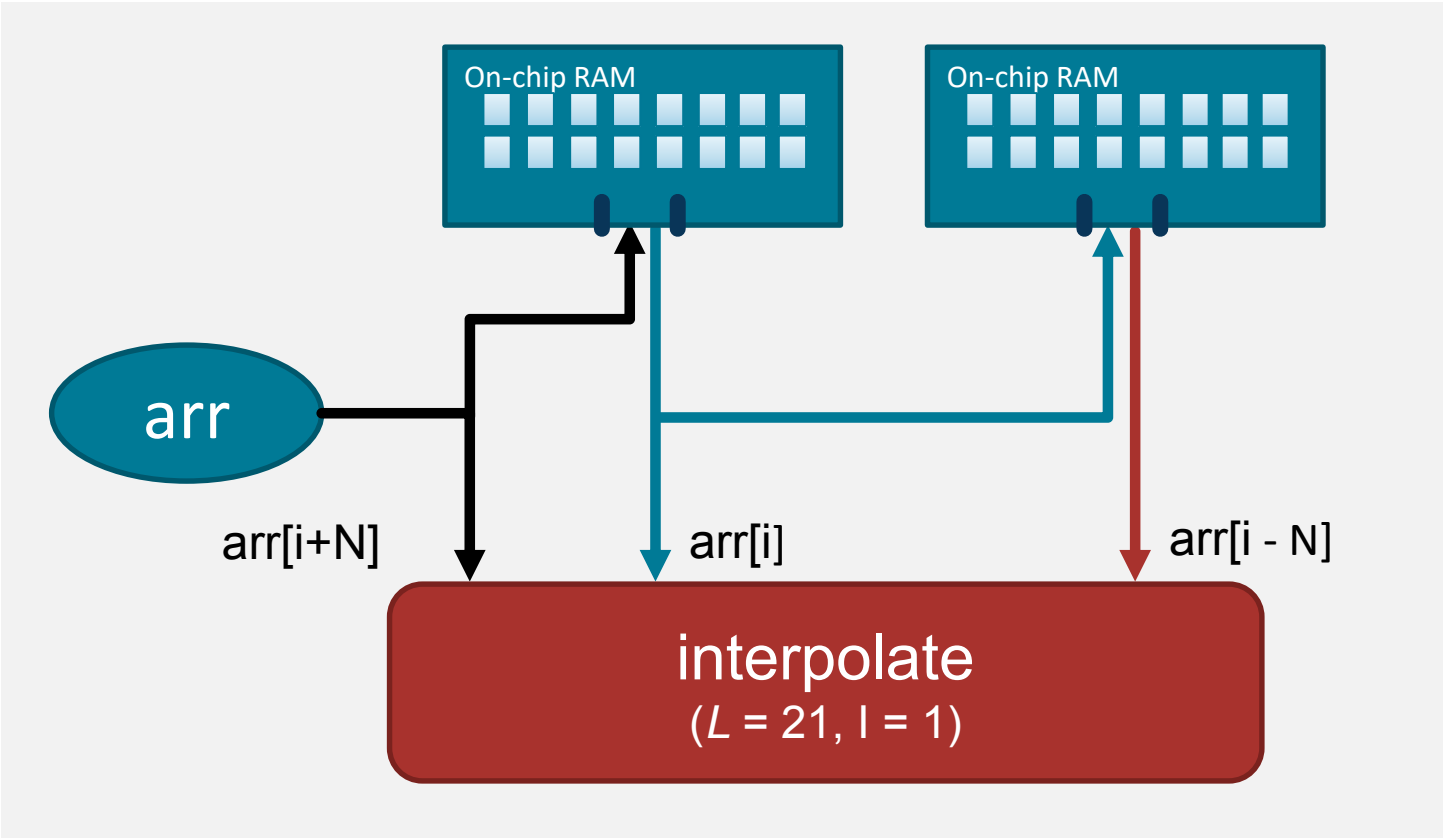
$W = 2,\ D = 1$

2D row-major:

$W = 2,\ D = N$



Modified example

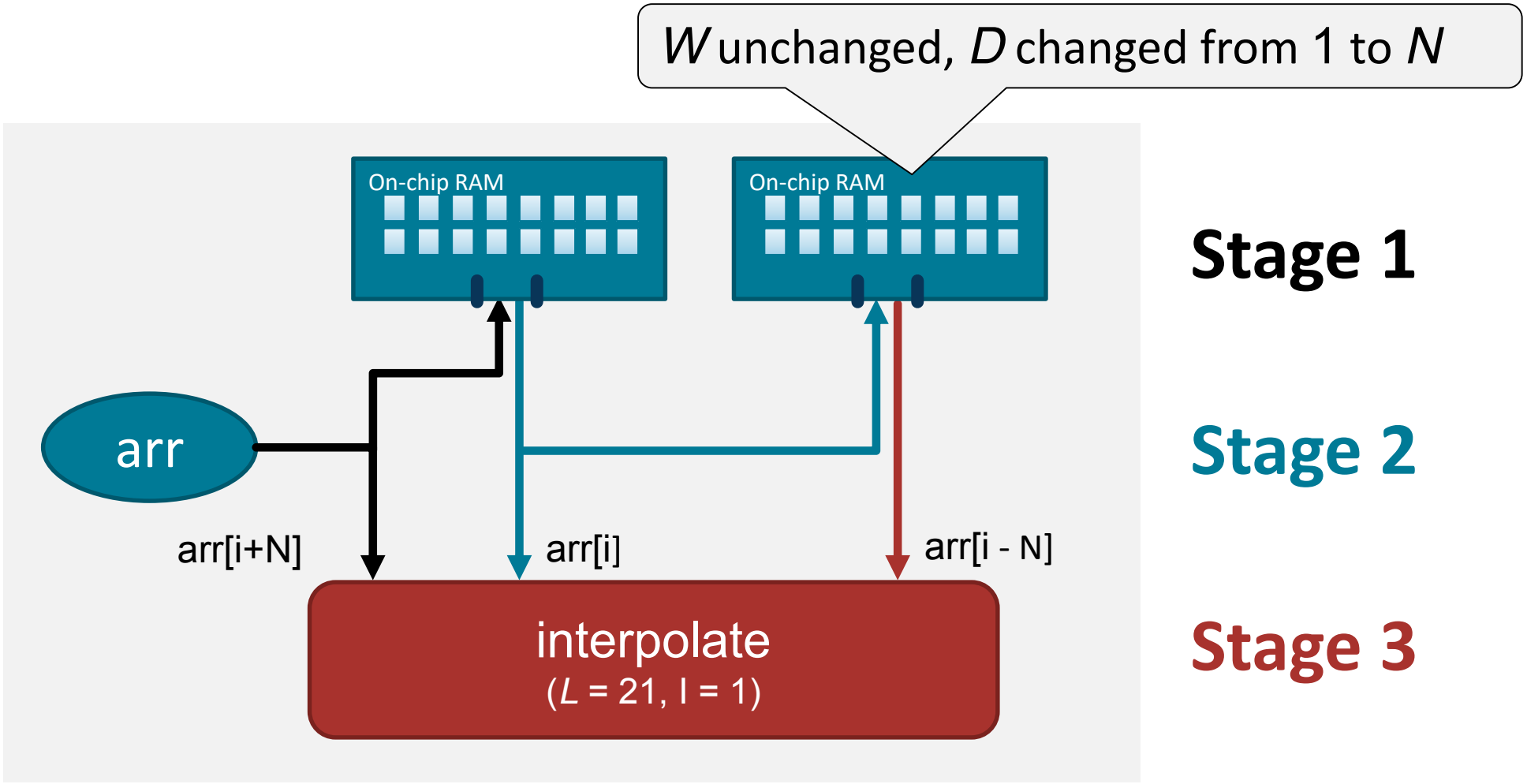


Stage 1

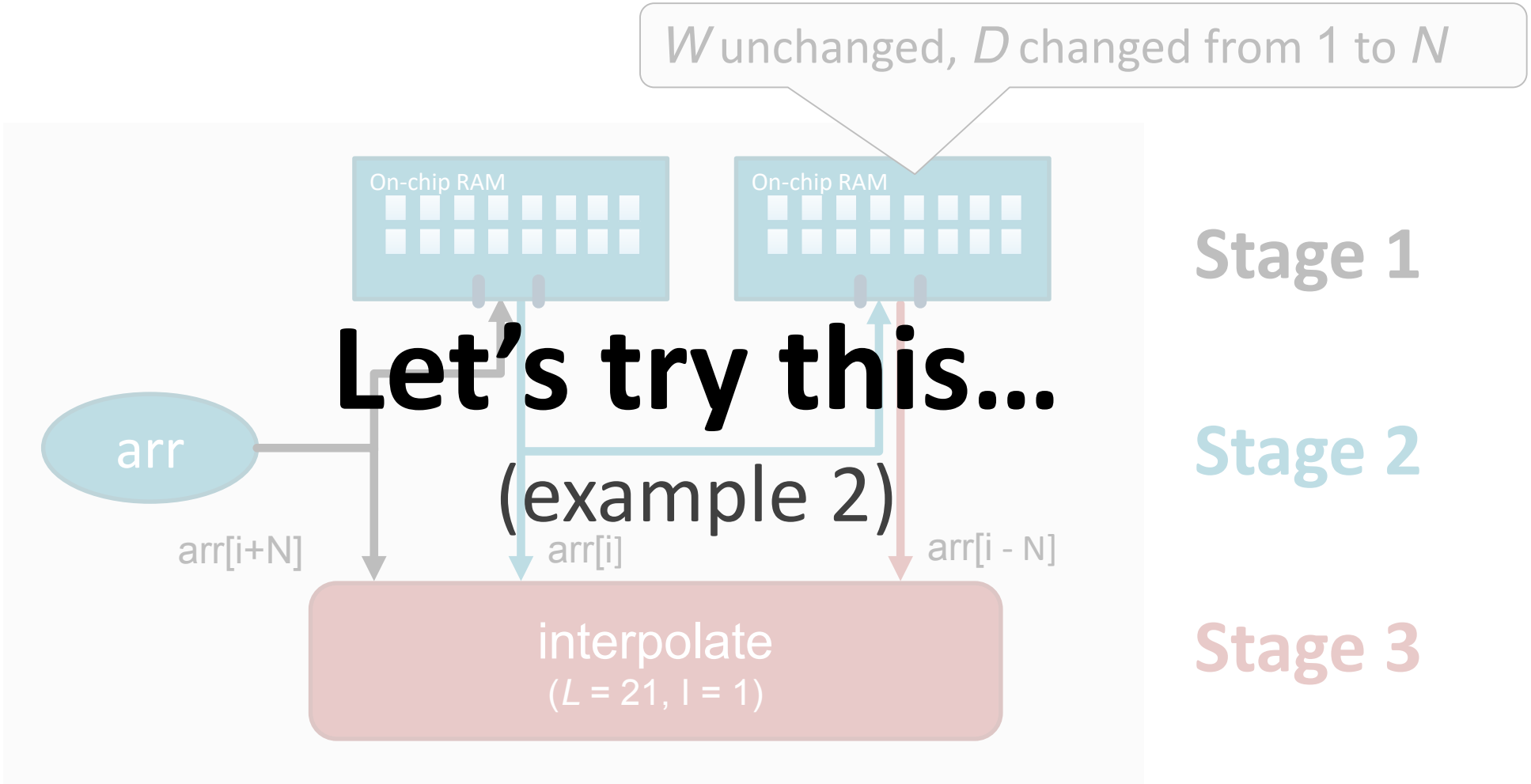
Stage 2

Stage 3

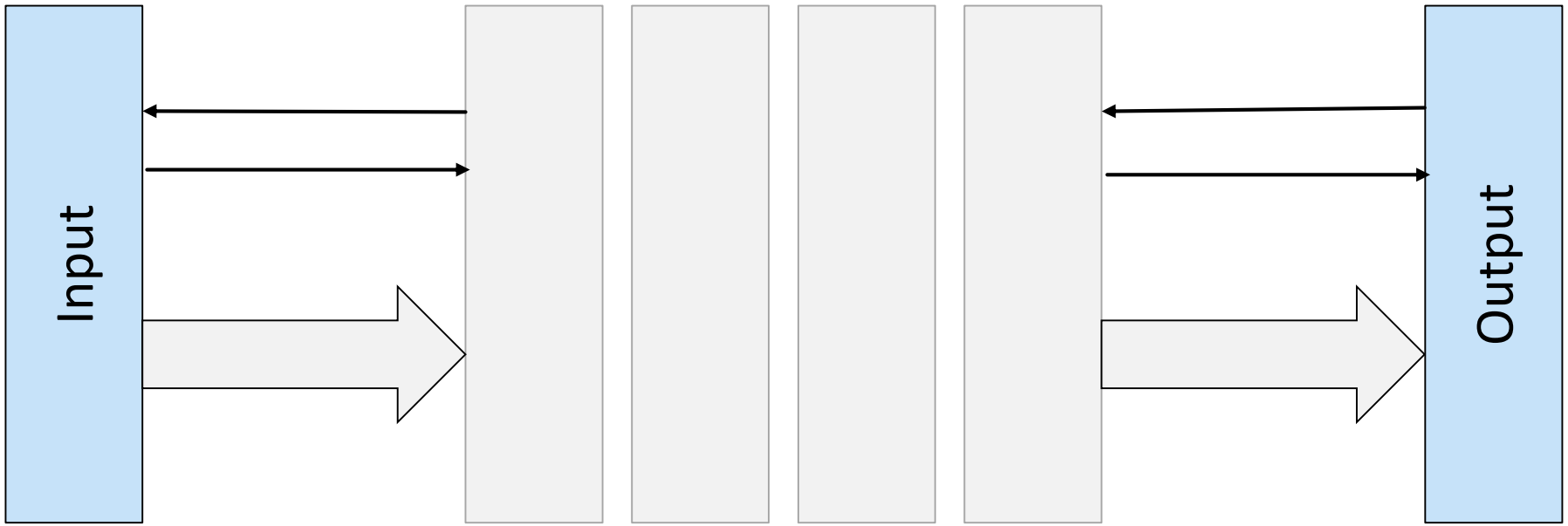
Modified example



Modified example

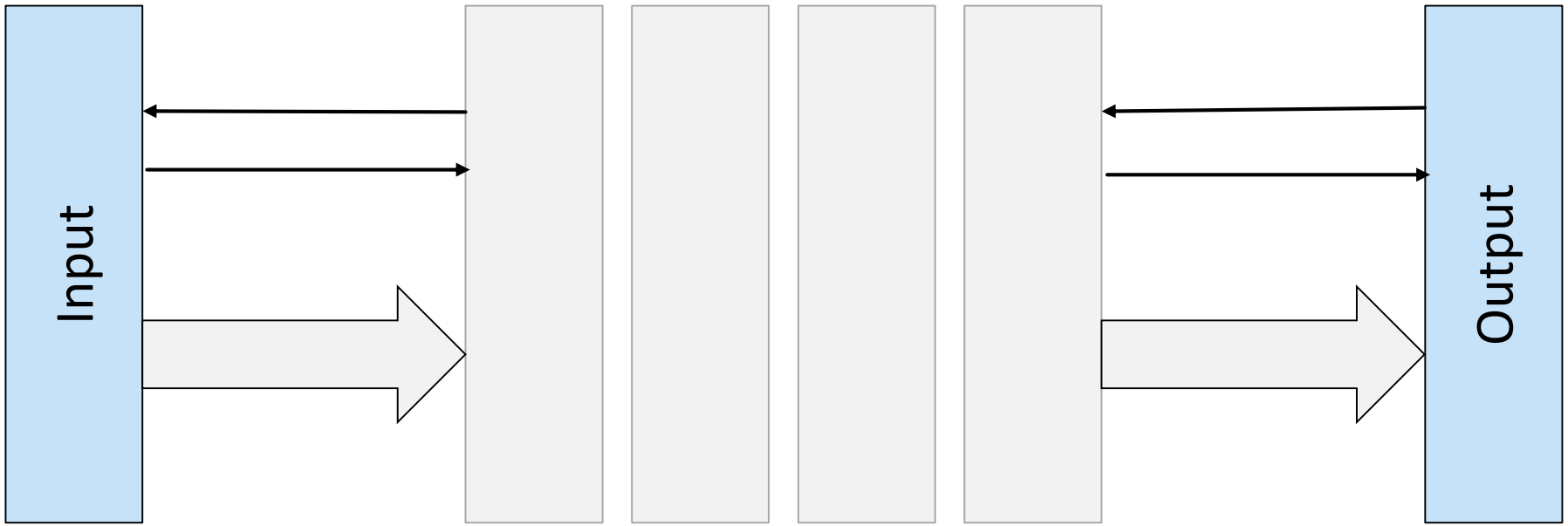


Streams



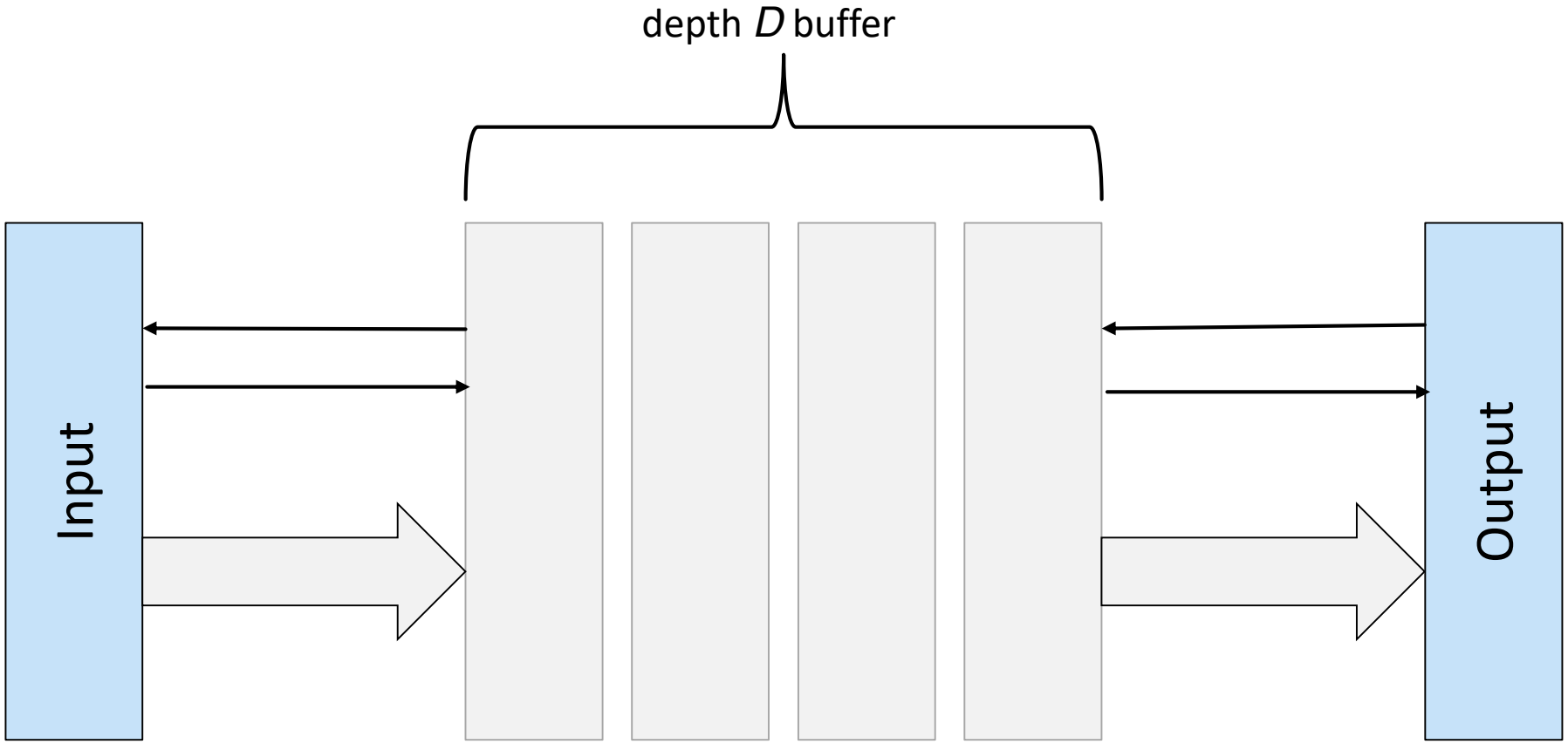
Streams

(FIFOs, queues...)



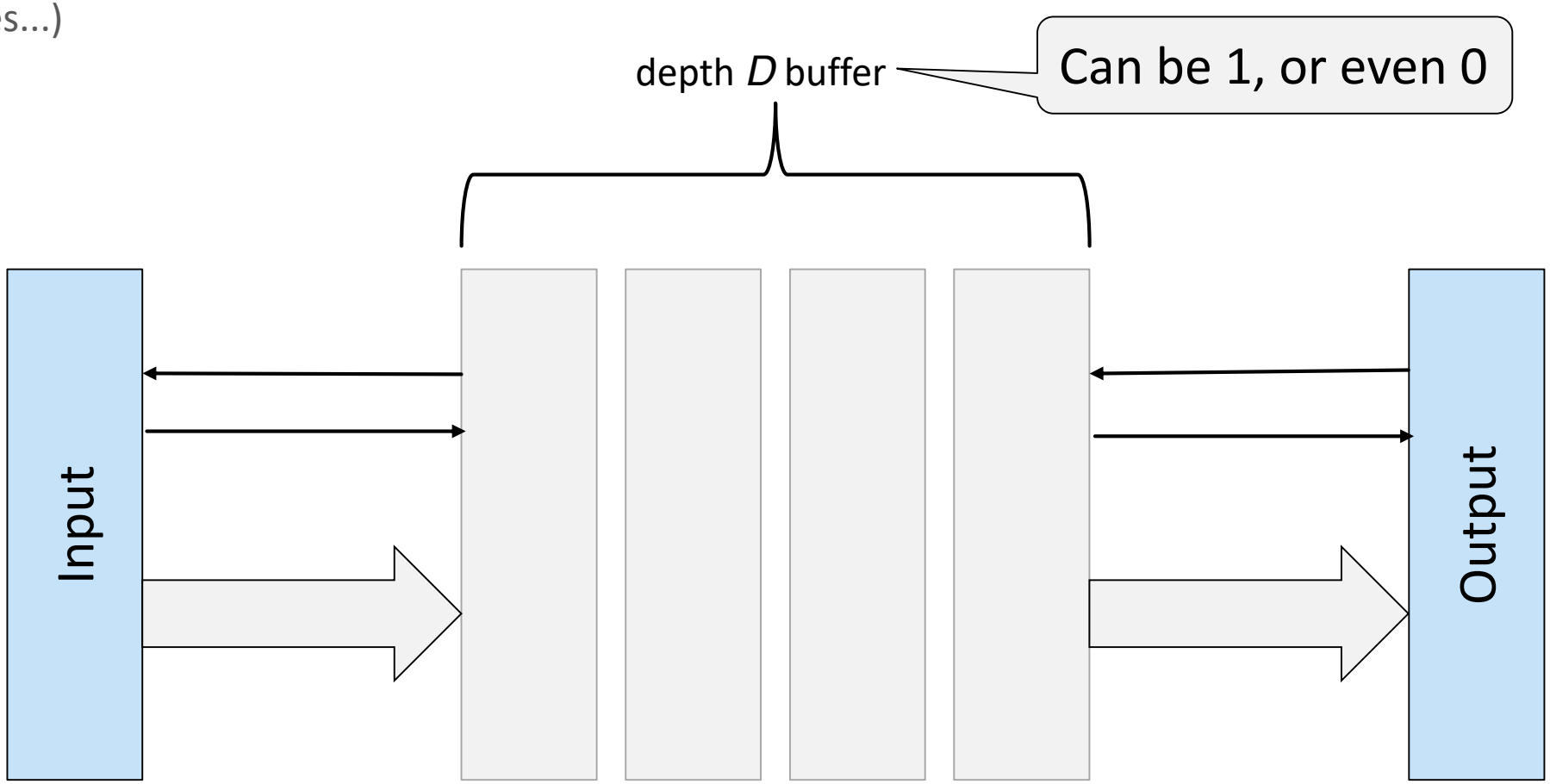
Streams

(FIFOs, queues...)



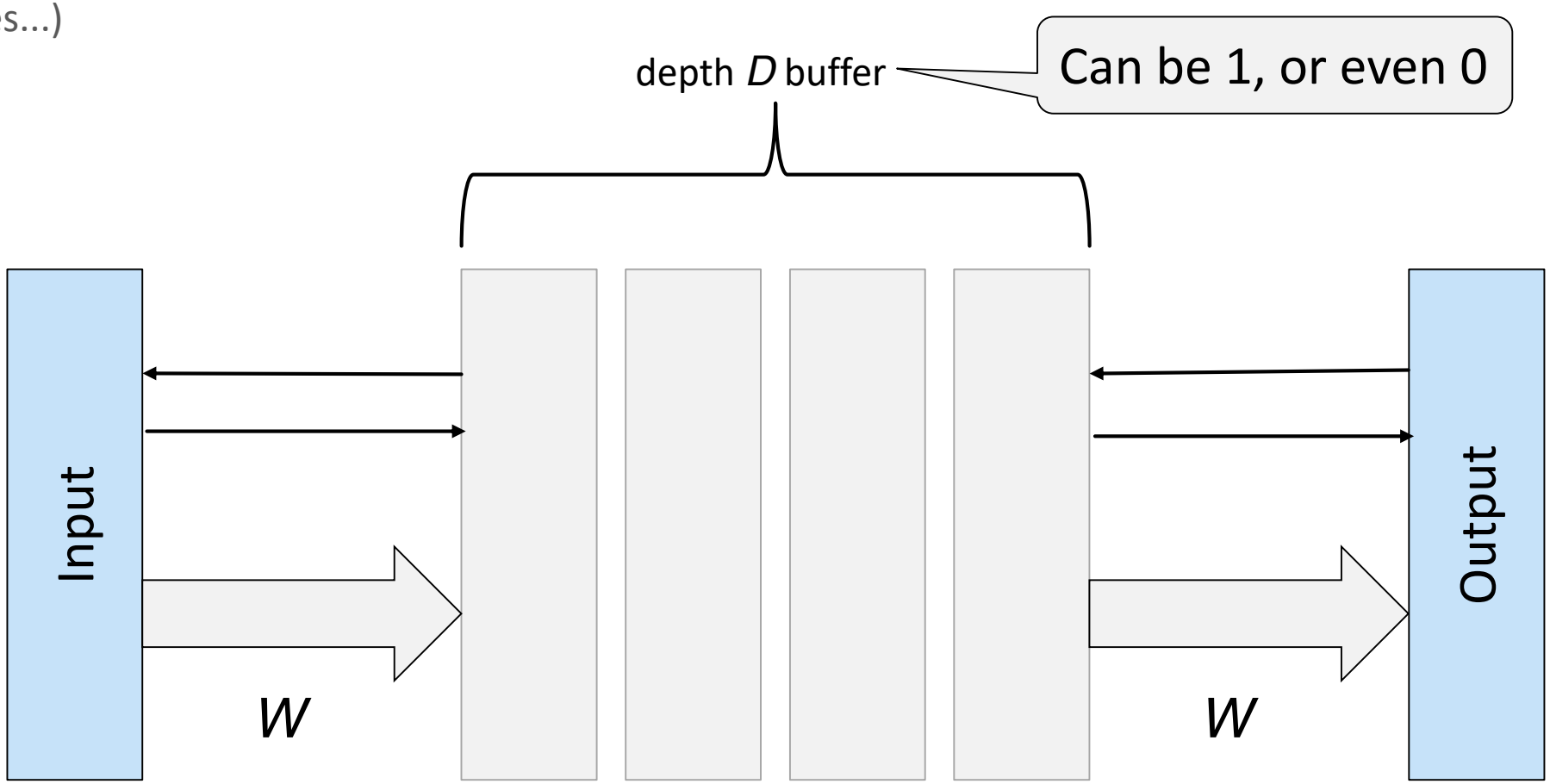
Streams

(FIFOs, queues...)



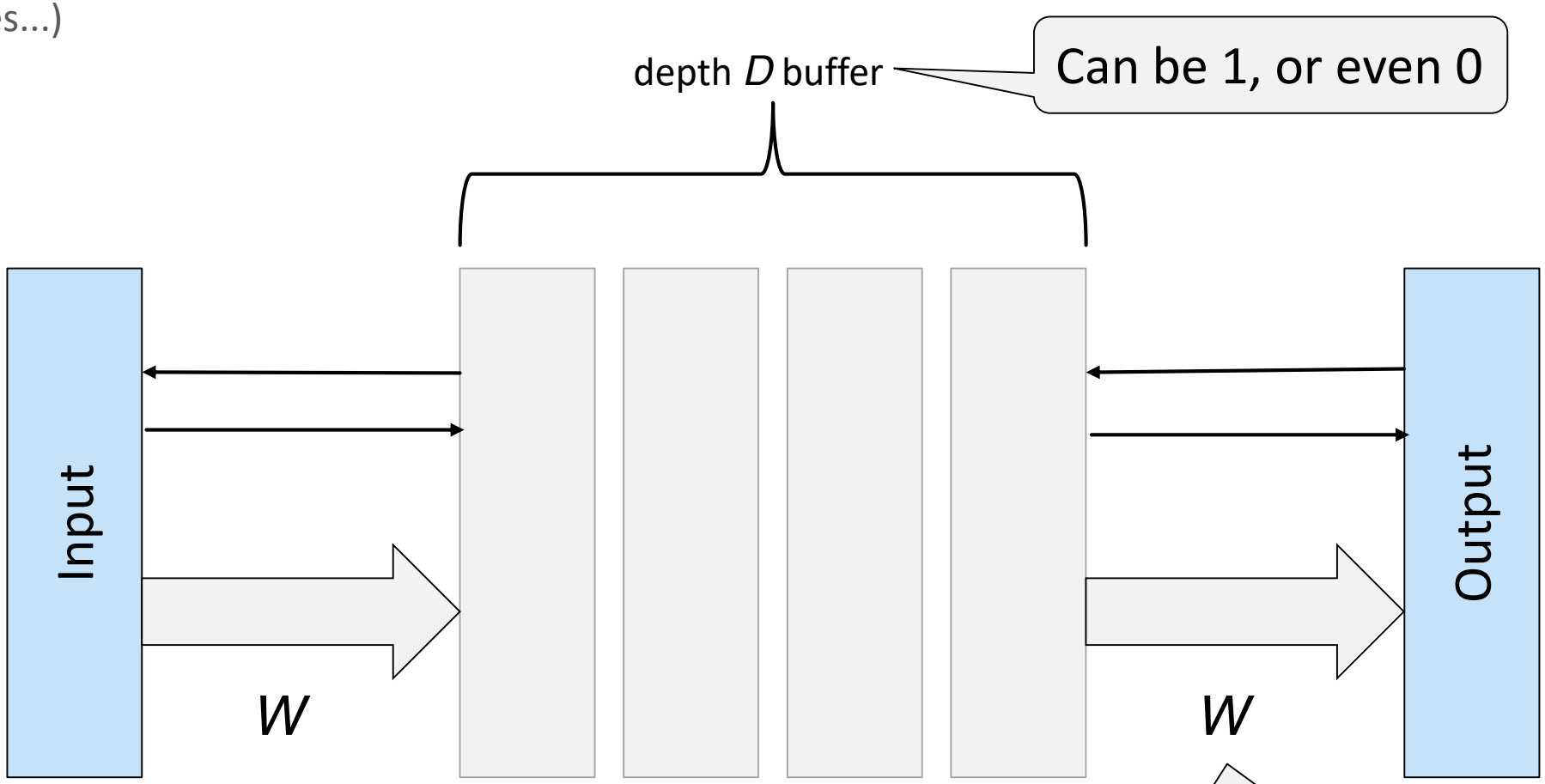
Streams

(FIFOs, queues...)



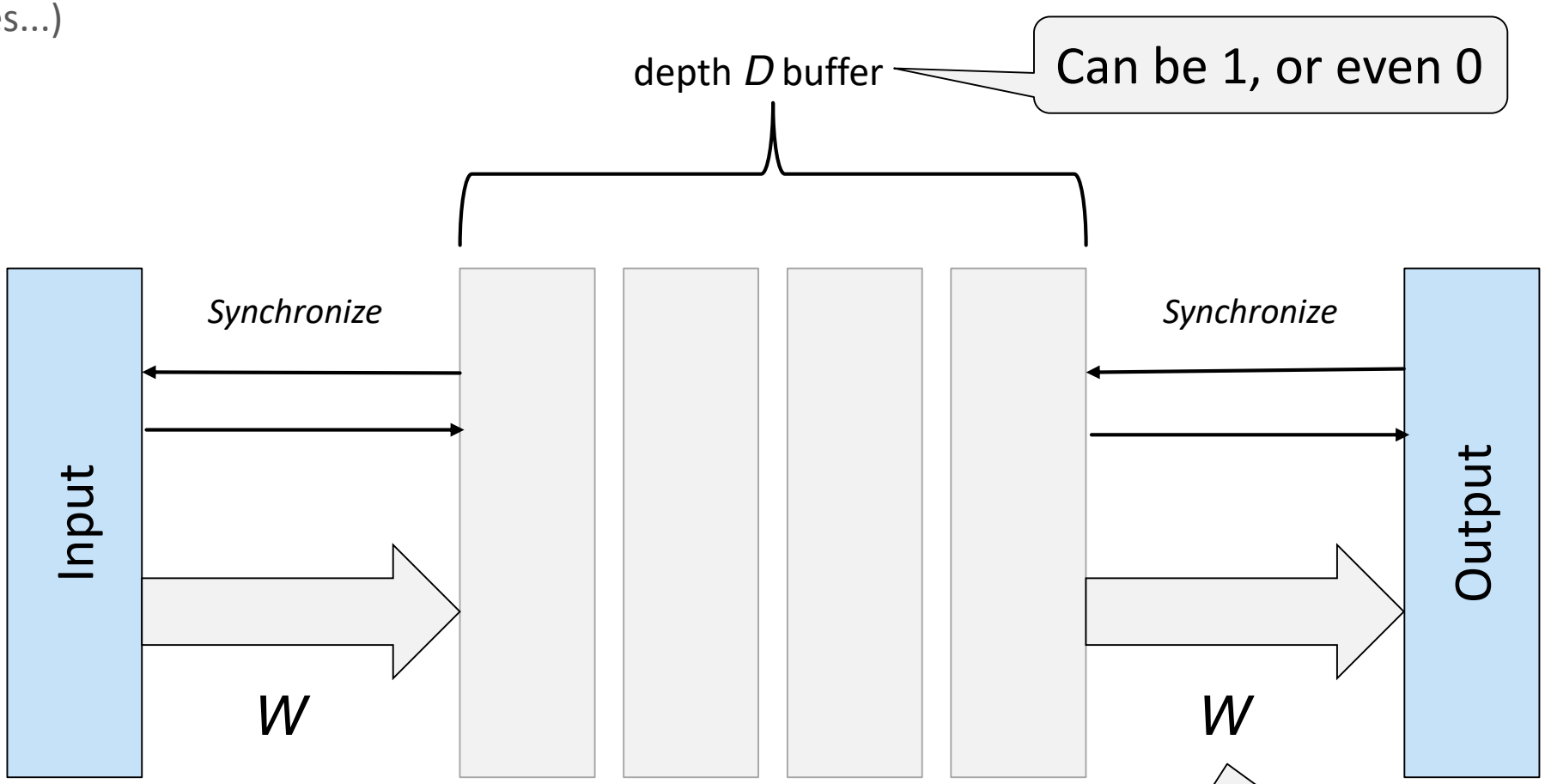
Streams

(FIFOs, queues...)

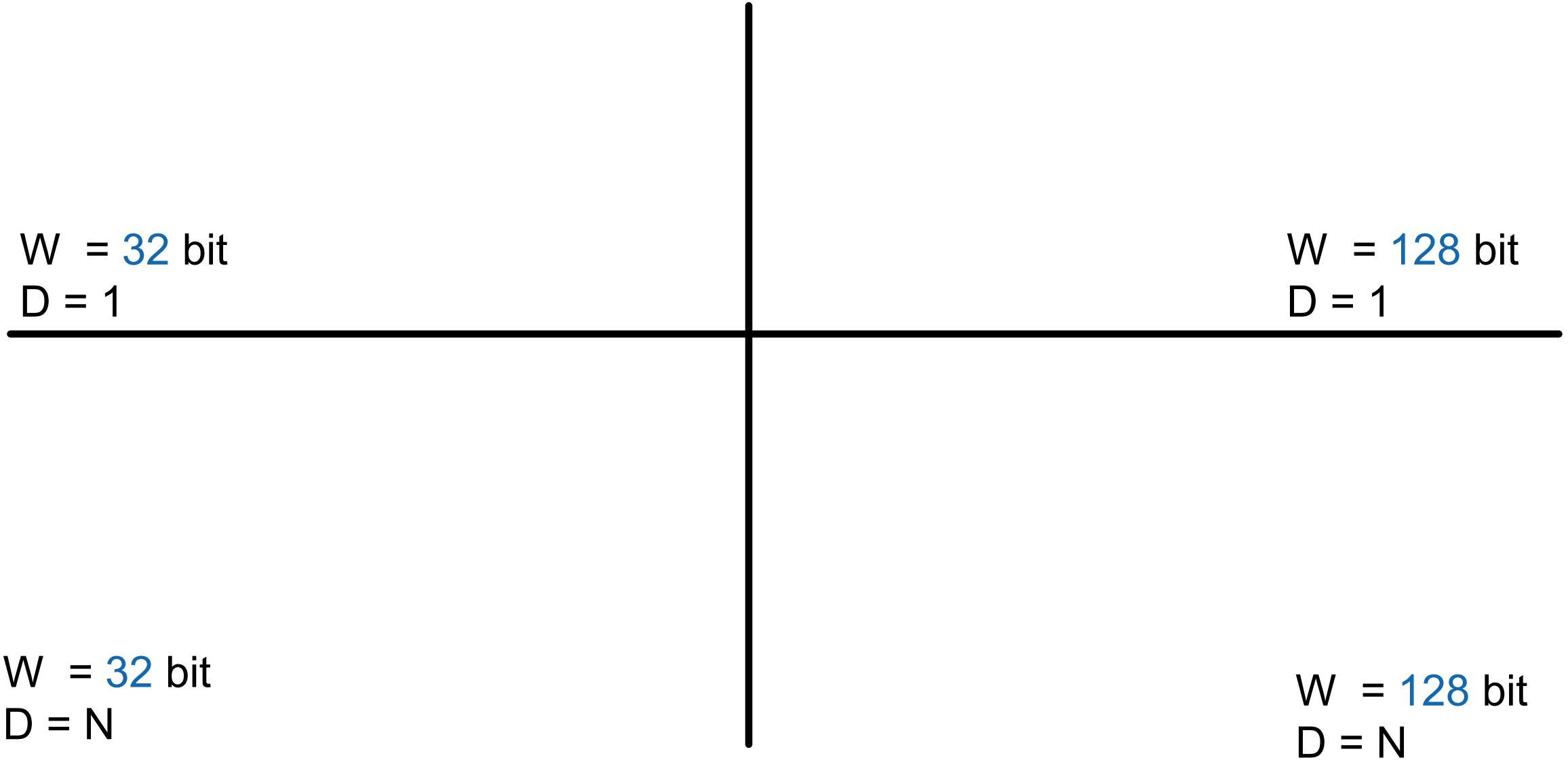


Streams

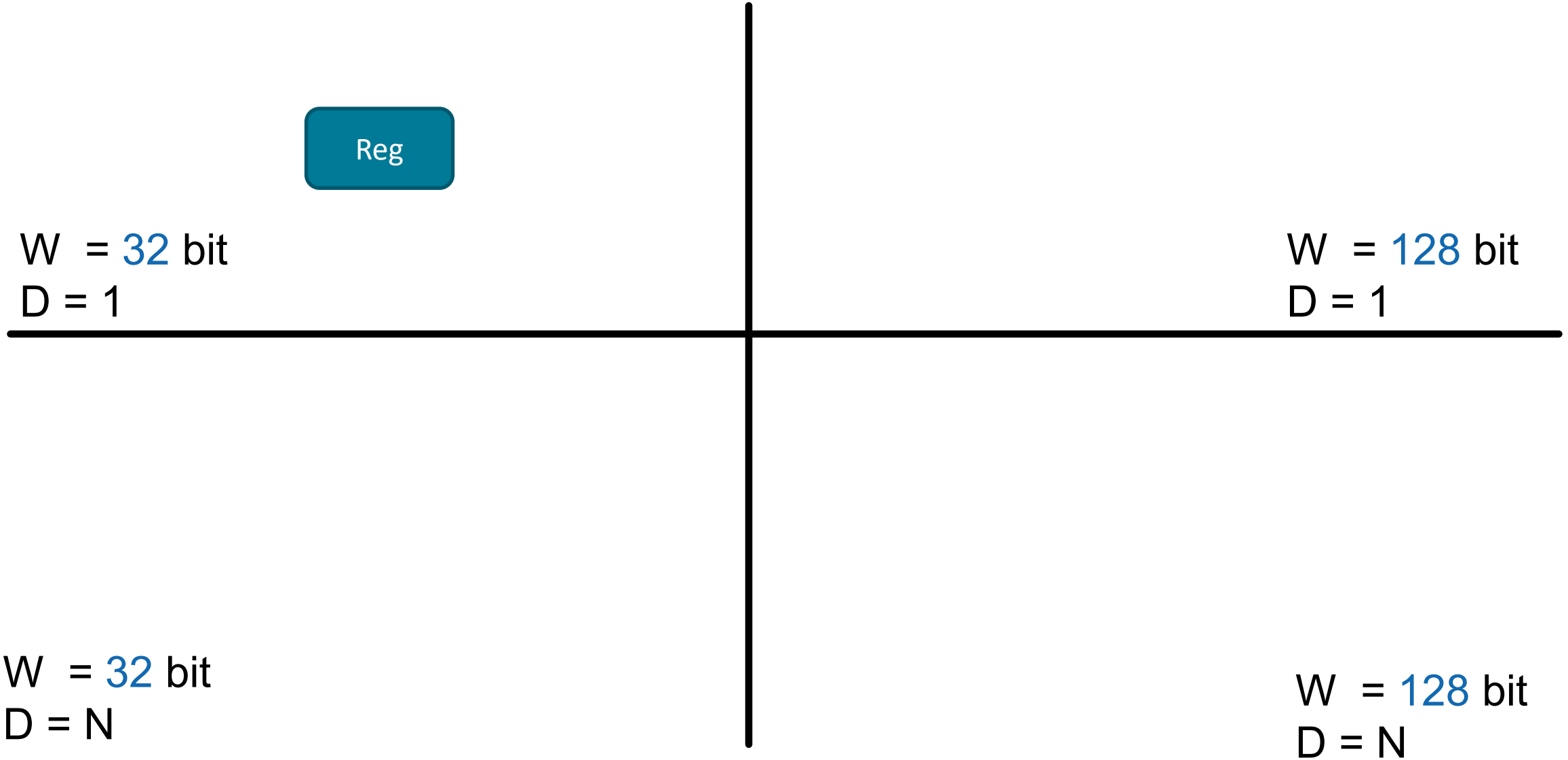
(FIFOs, queues...)



Thinking in width and depth



Thinking in width and depth



Thinking in width and depth

```
float reg;
```

W = 32 bit
D = 1

W = 128 bit
D = 1

W = 32 bit
D = N

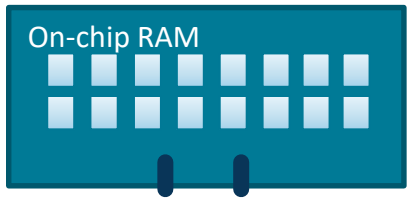
W = 128 bit
D = N

Thinking in width and depth

```
float reg;
```

W = 32 bit
D = 1

W = 128 bit
D = 1



W = 32 bit
D = N

W = 128 bit
D = N

Thinking in width and depth

```
float reg;
```

W = 32 bit
D = 1

W = 128 bit
D = 1

On-chip RAM

```
float buffer[N];
Stream<float> fifo(N);
```

W = 32 bit
D = N

W = 128 bit
D = N

Thinking in width and depth

```
float reg;
```

W = 32 bit
D = 1

W = 128 bit
D = 1

```
float buffer[N];
Stream<float> fifo(N);
```

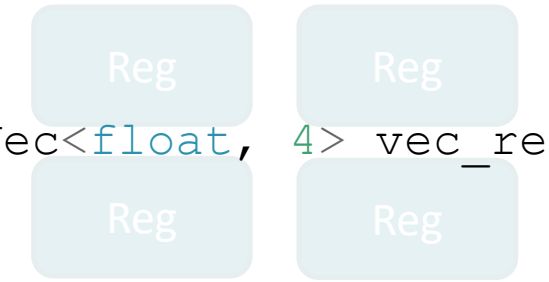
W = 32 bit
D = N

W = 128 bit
D = N

Thinking in width and depth

```
float reg;
```

W = 32 bit
D = 1




```
Vec<float, 4> vec_reg;
```

W = 128 bit
D = 1

```
float buffer[N];
Stream<float> fifo(N);
```

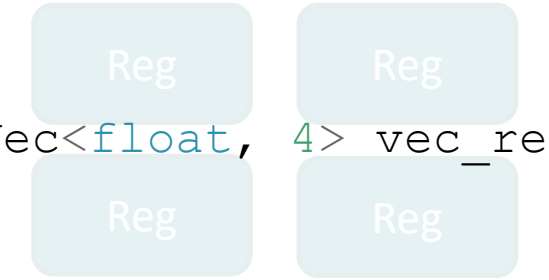
W = 32 bit
D = N

W = 128 bit
D = N

Thinking in width and depth

```
float reg;
```

W = 32 bit
D = 1

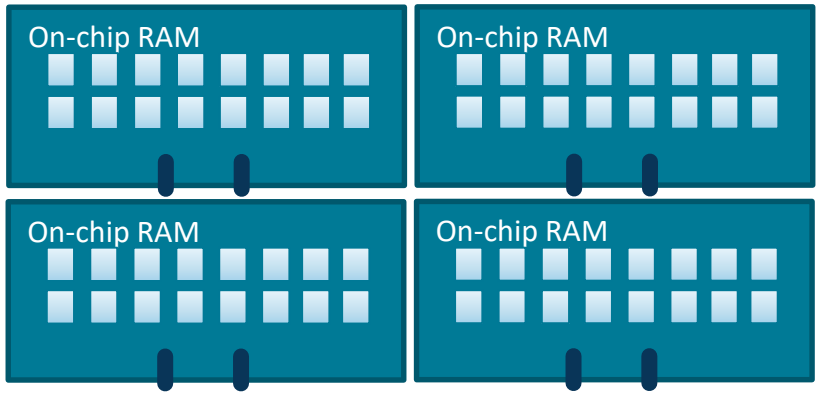



```
Vec<float, 4> vec_reg;
```

W = 128 bit
D = 1

```
float buffer[N];
Stream<float> fifo(N);
```

W = 32 bit
D = N

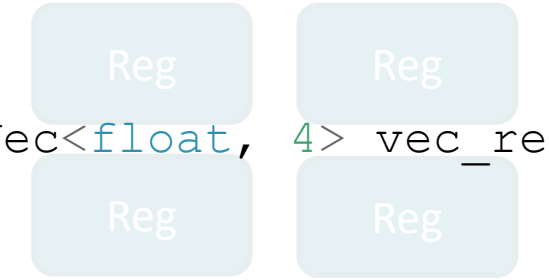


W = 128 bit
D = N

Thinking in width and depth

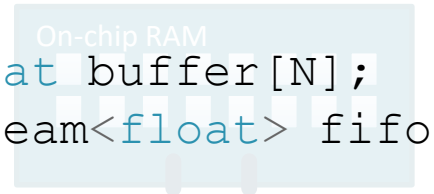
```
float reg;
```

W = 32 bit
D = 1



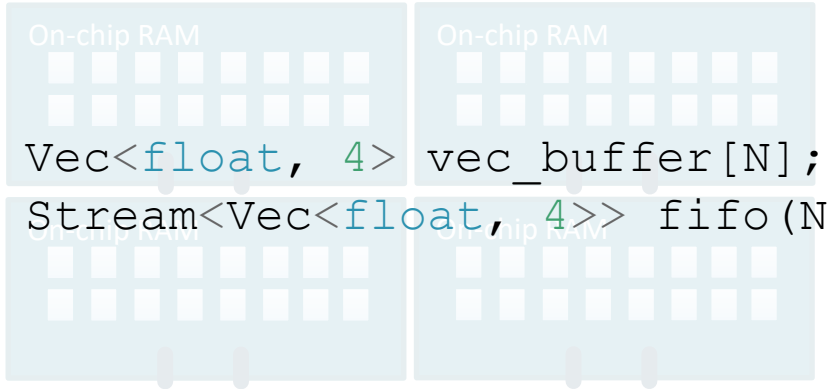

```
Vec<float, 4> vec_reg;
```

W = 128 bit
D = 1




```
float buffer[N];
Stream<float> fifo(N);
```

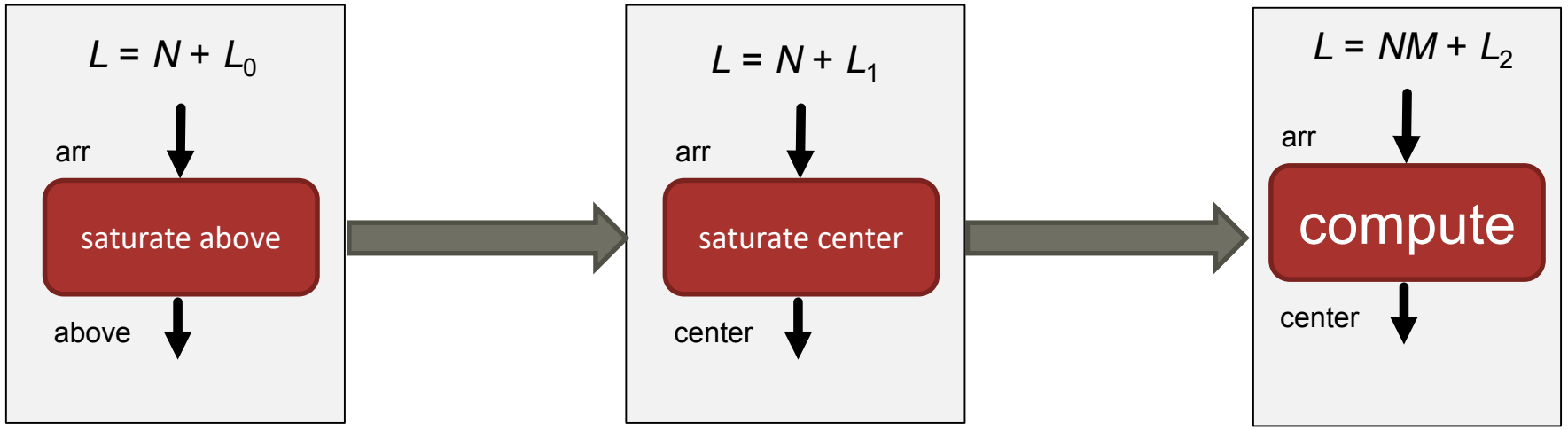
W = 32 bit
D = N




```
Vec<float, 4> vec_buffer[N];
Stream<Vec<float, 4>> fifo(N);
```

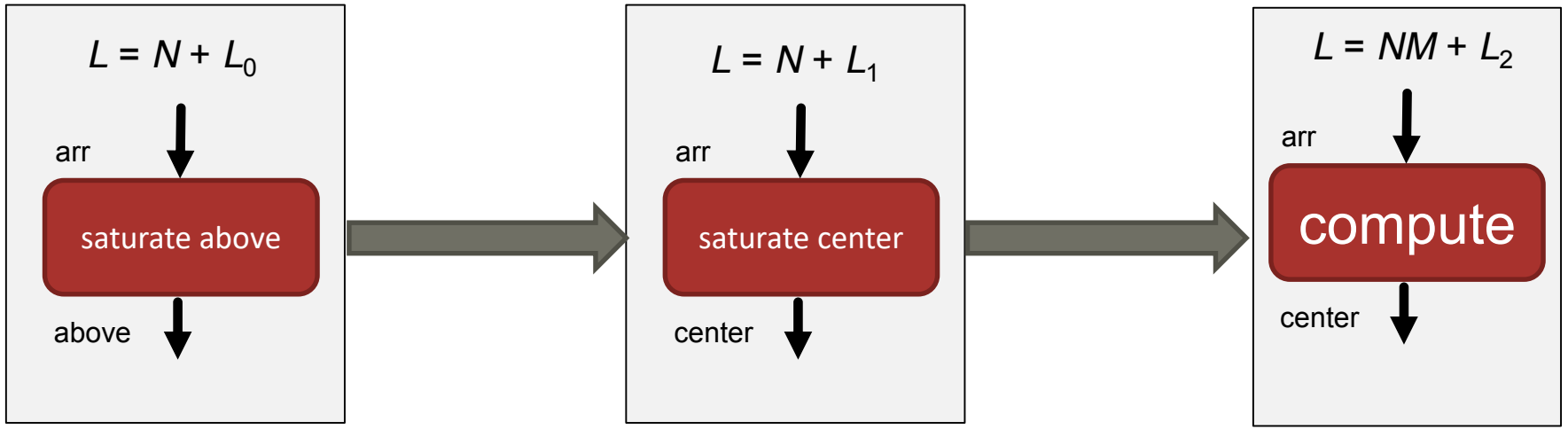
W = 128 bit
D = N

Finite state machine



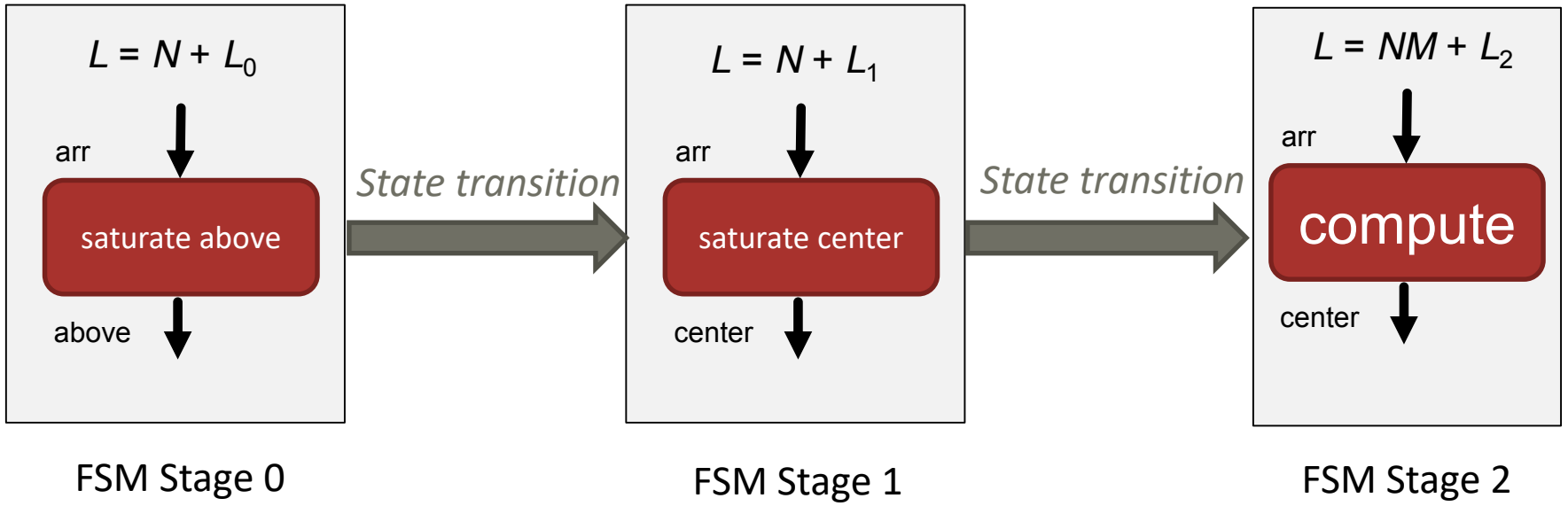
FSM Stage 0 FSM Stage 1 FSM Stage 2

Finite state machine

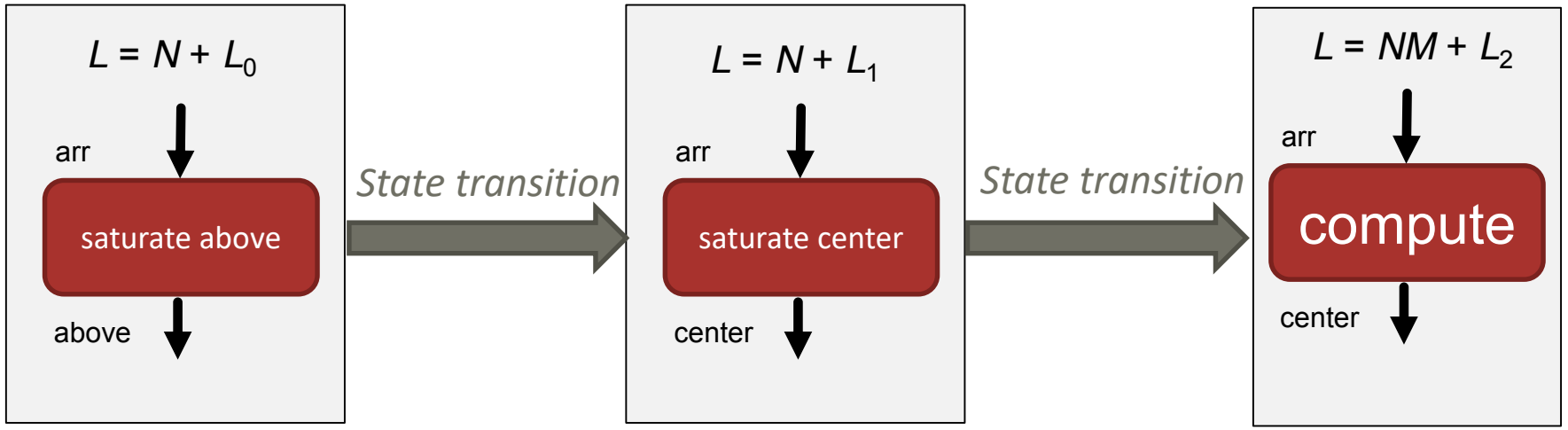


FSM Stage 0 FSM Stage 1 FSM Stage 2

Finite state machine

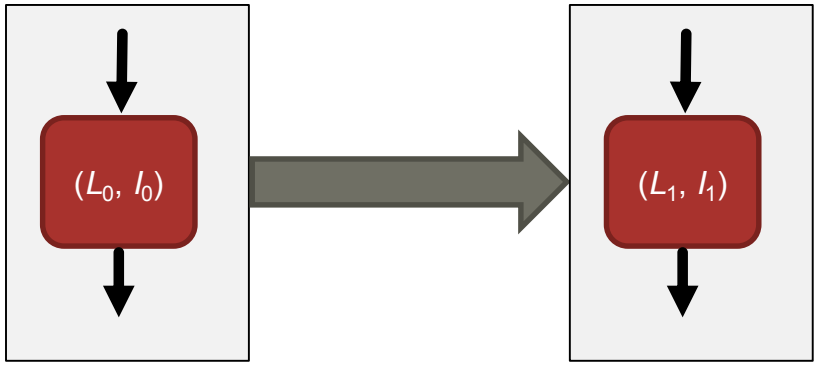


Finite state machine

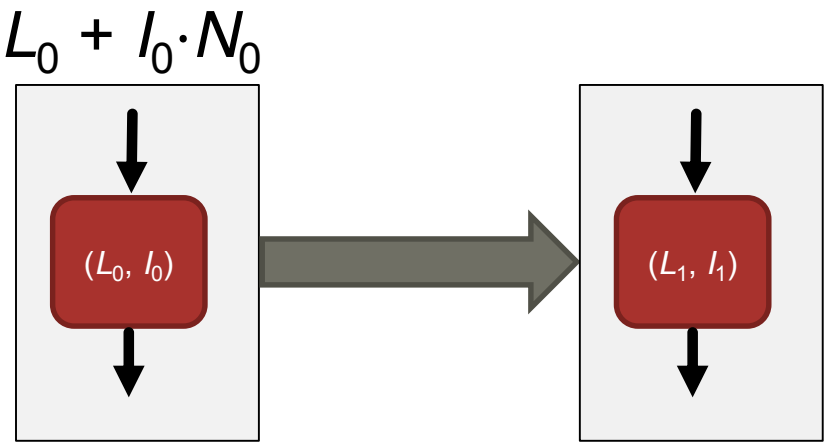


Sequential execution of
(pipeline-)**parallel** stages

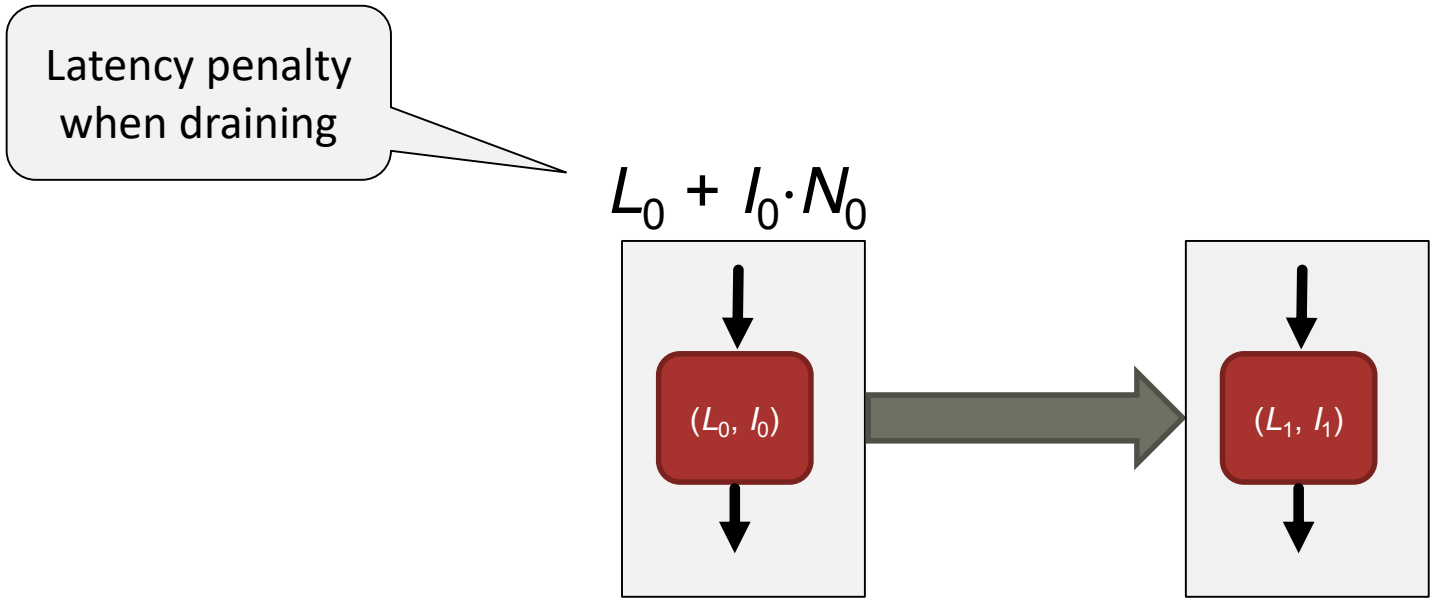
Draining and saturation phases



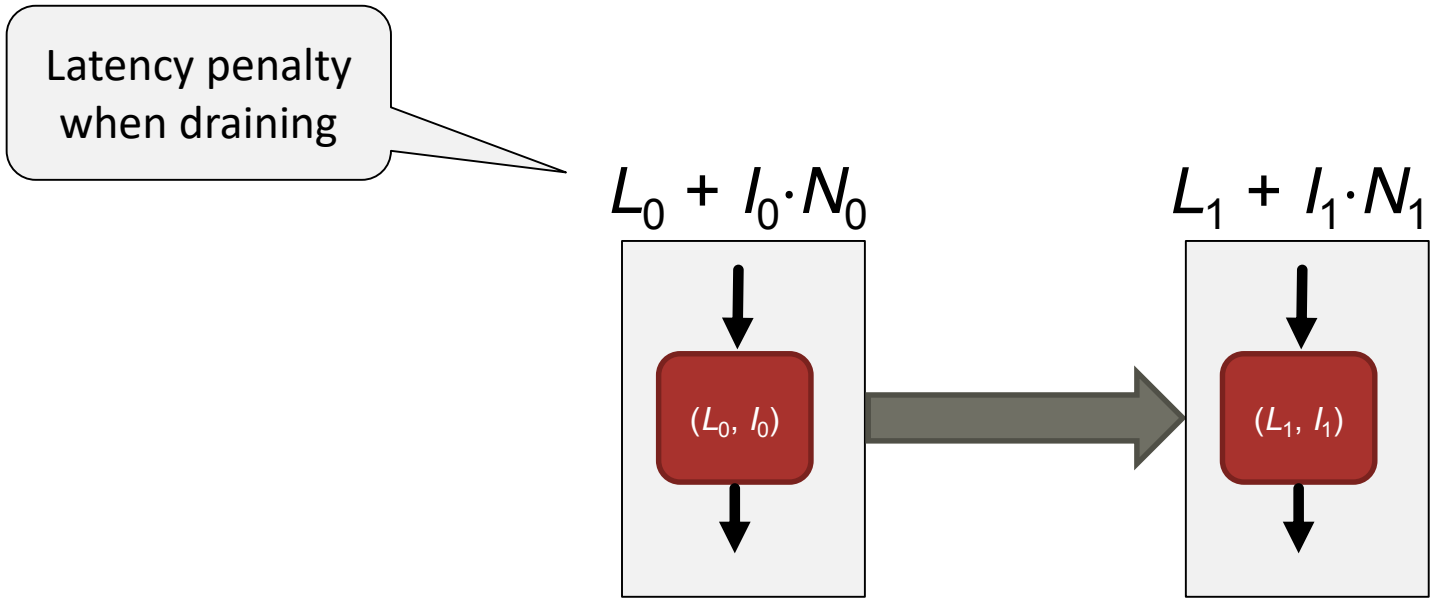
Draining and saturation phases



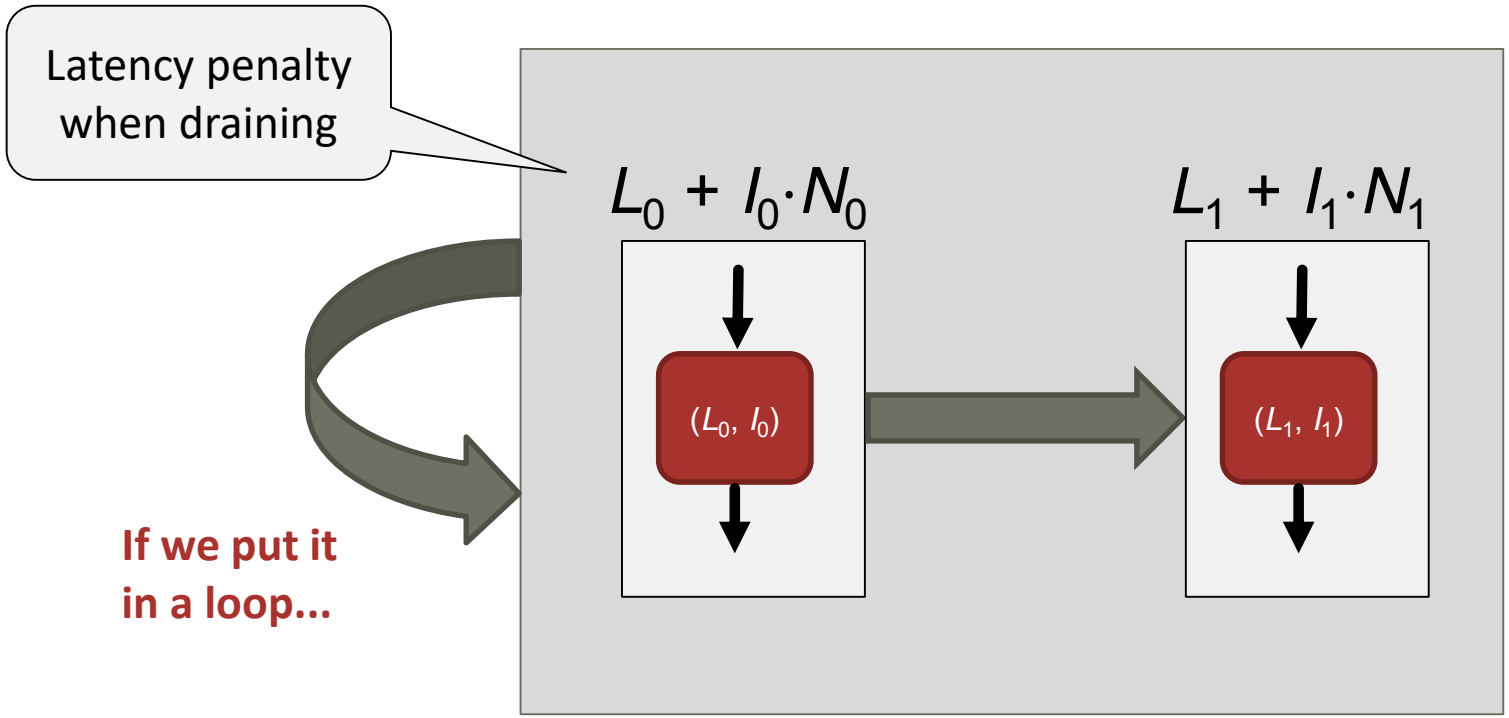
Draining and saturation phases



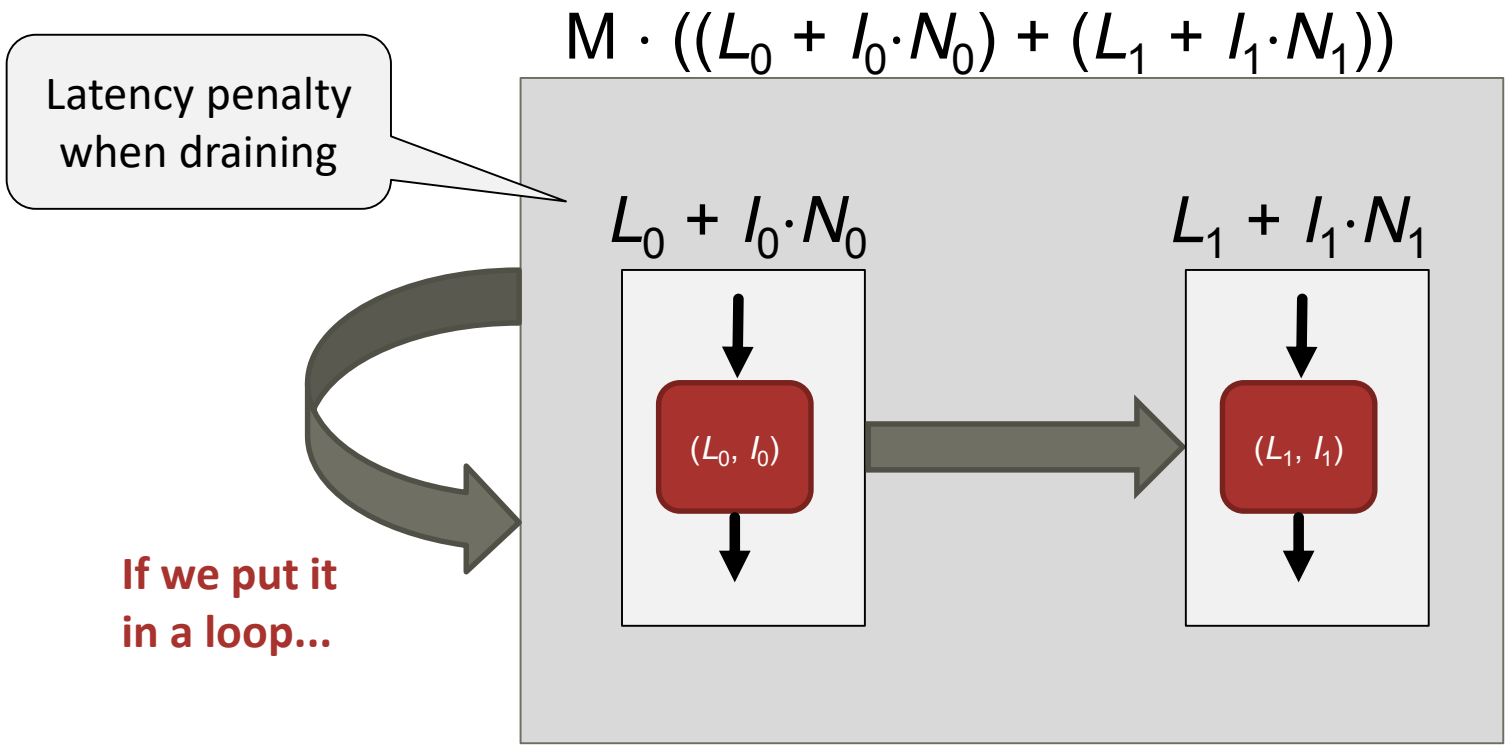
Draining and saturation phases



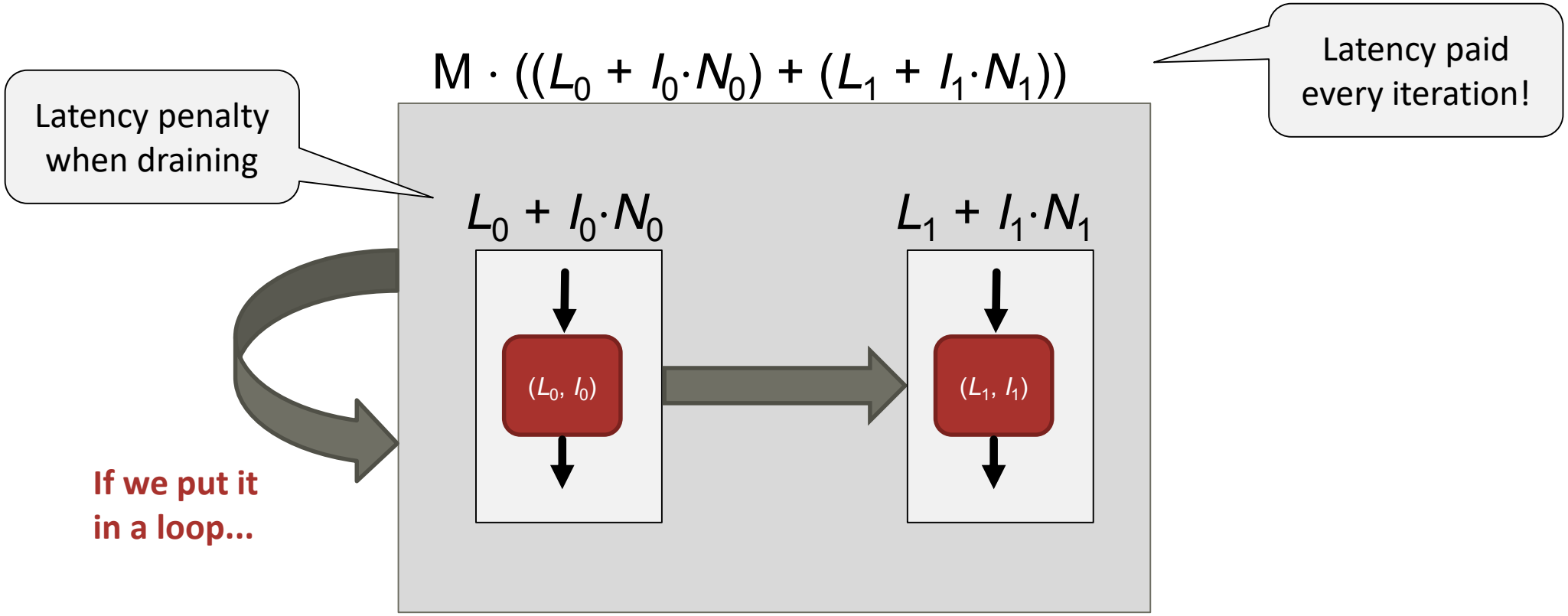
Draining and saturation phases



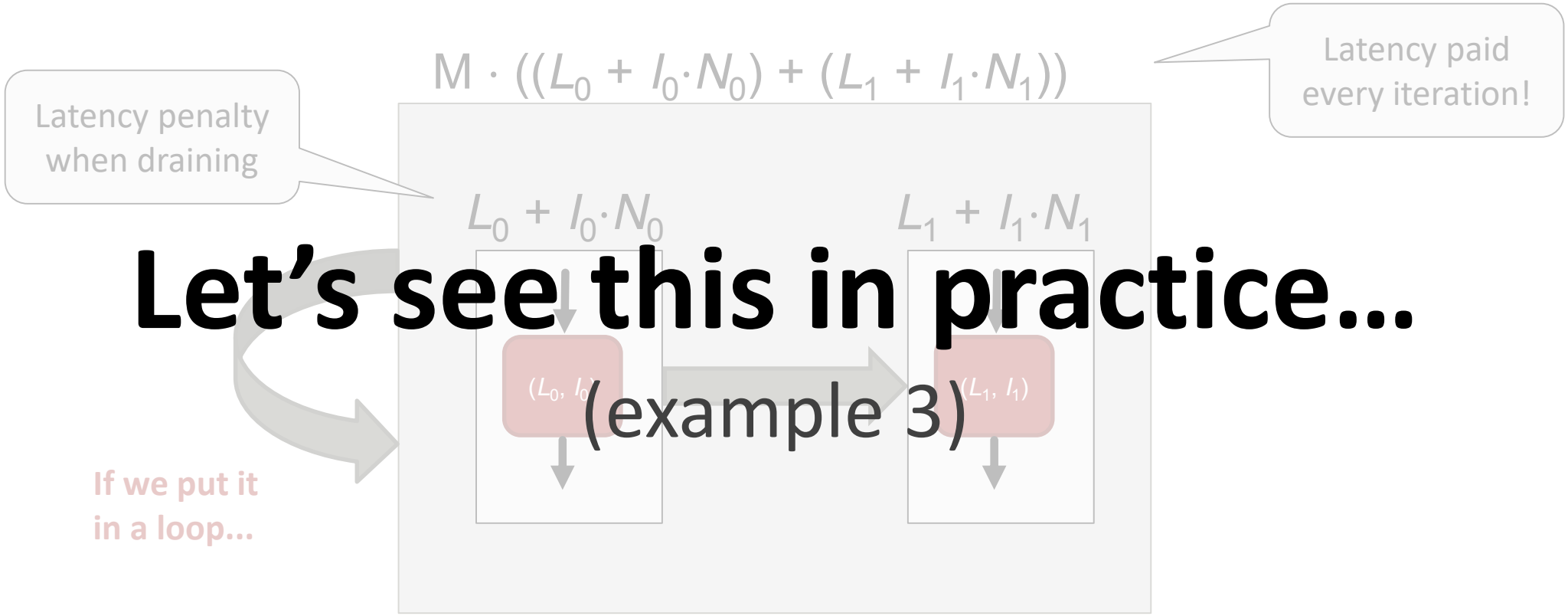
Draining and saturation phases



Draining and saturation phases



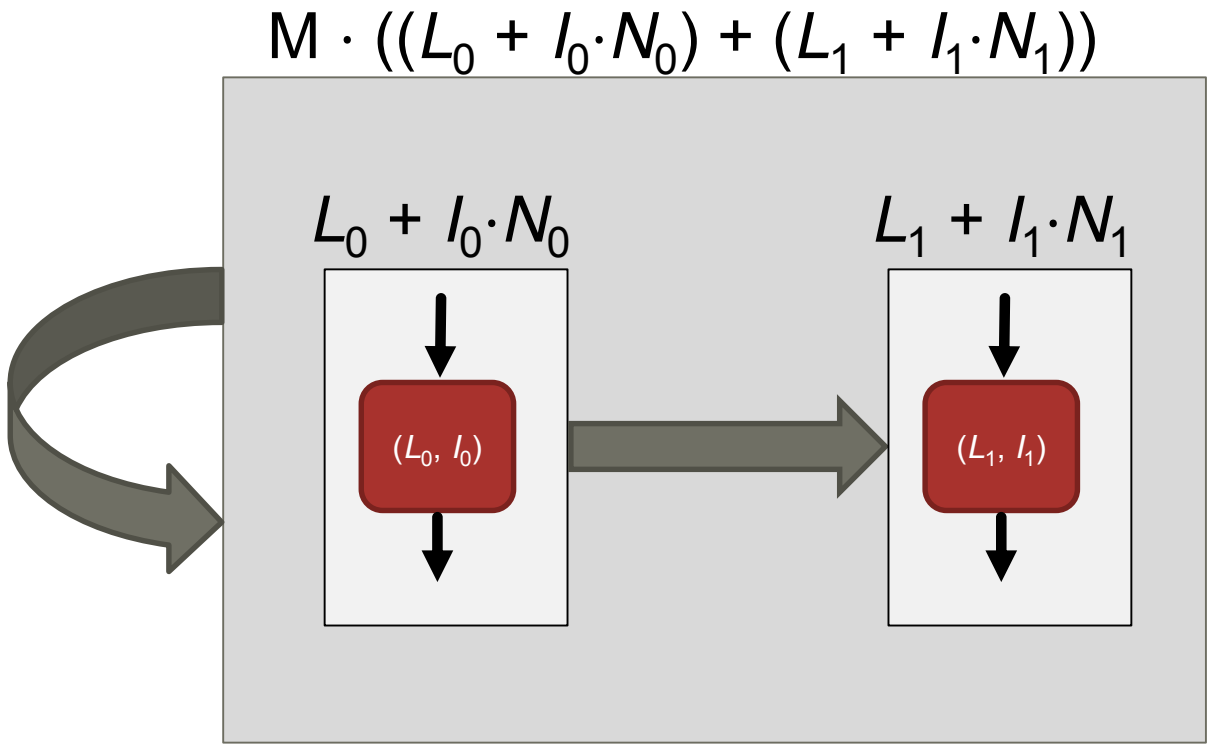
Draining and saturation phases



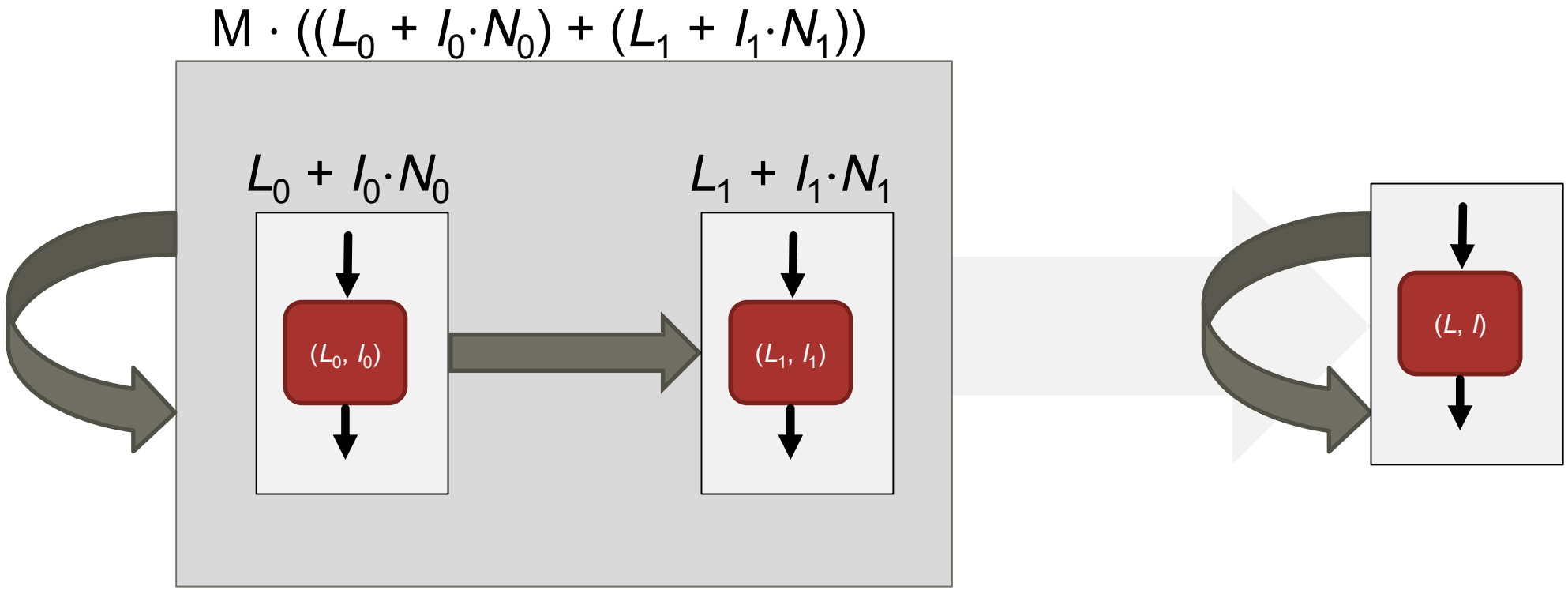
Let's see this in practice…

(example 3)

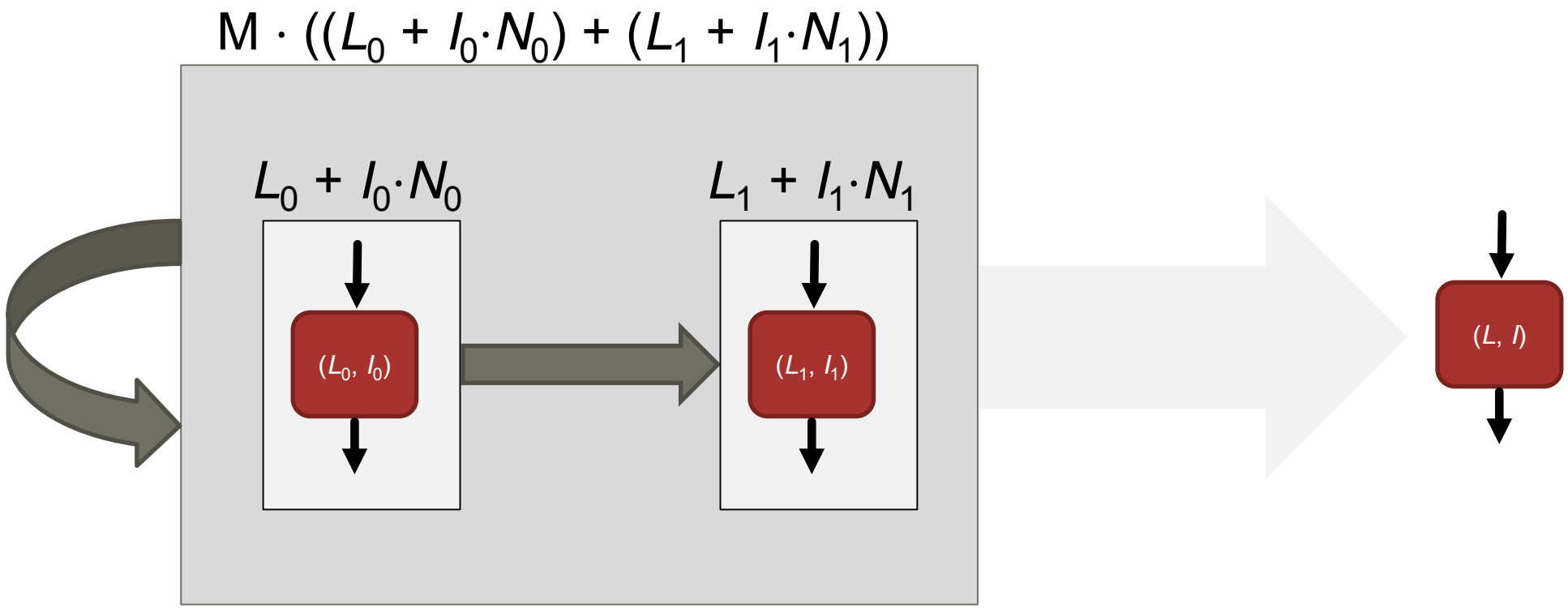
Flattening



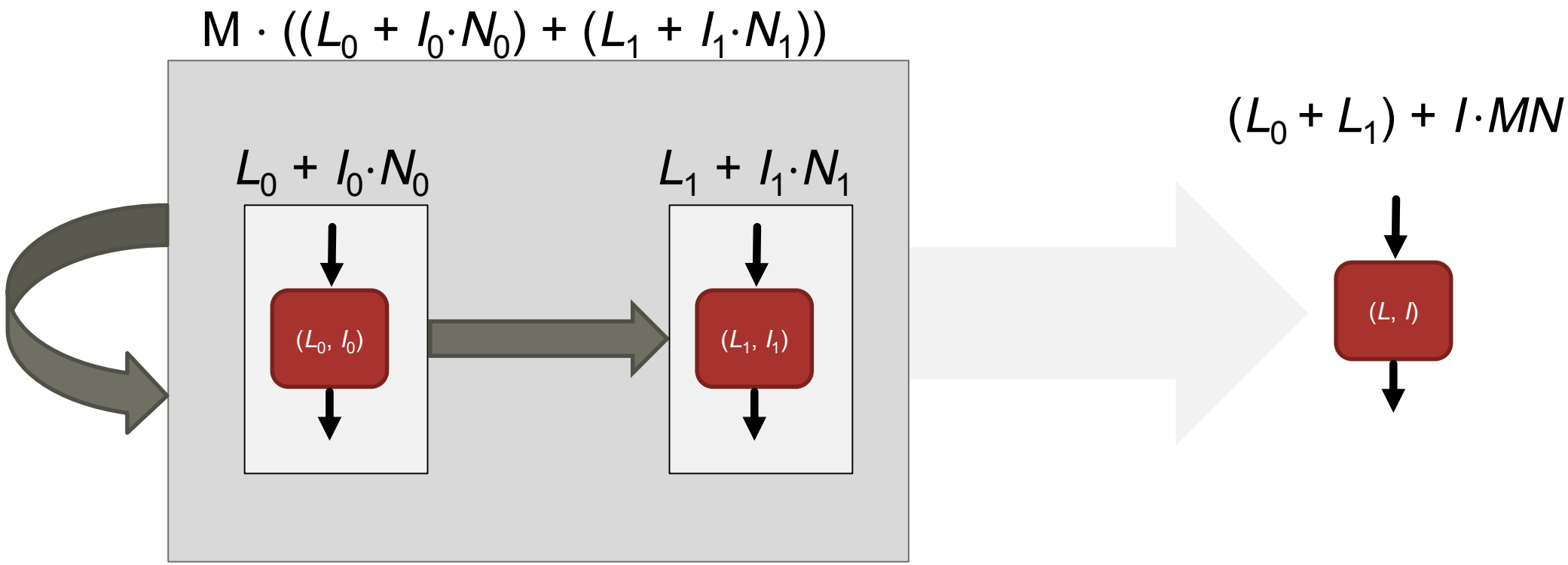
Flattening



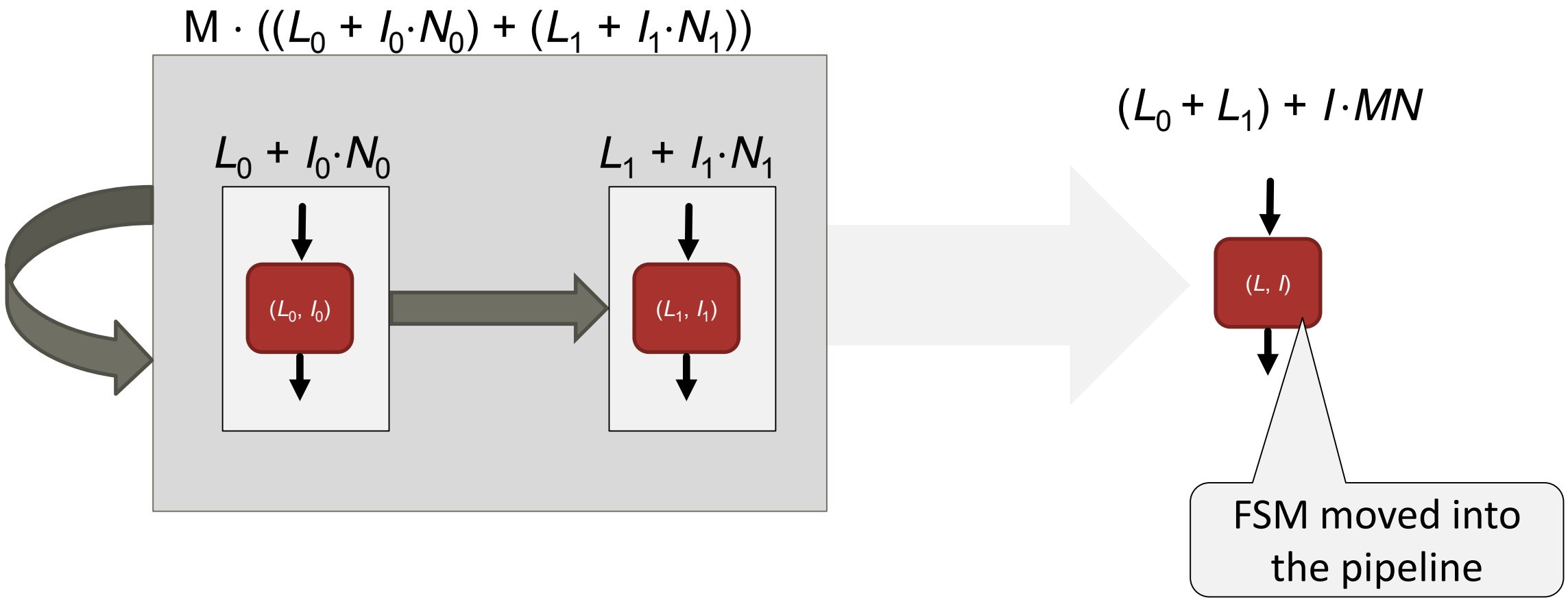
Flattening



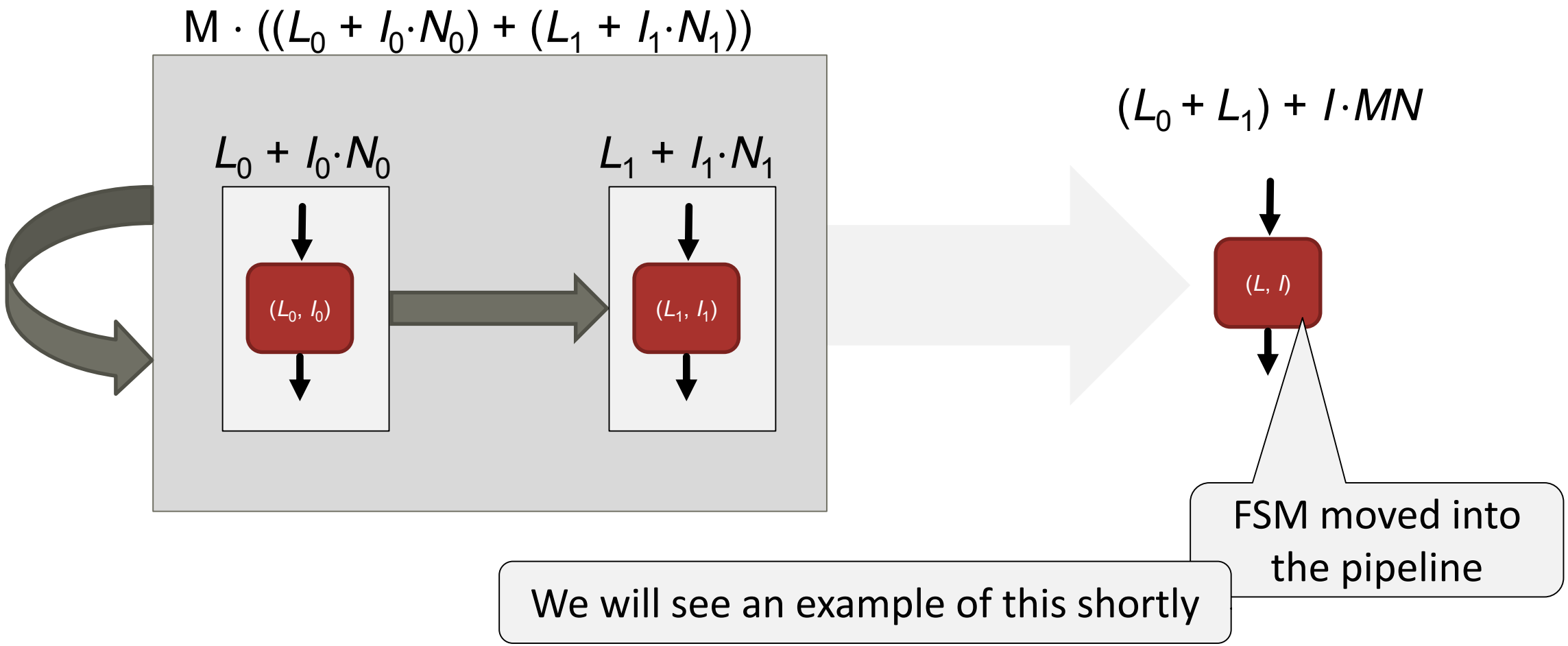
Flattening



Flattening

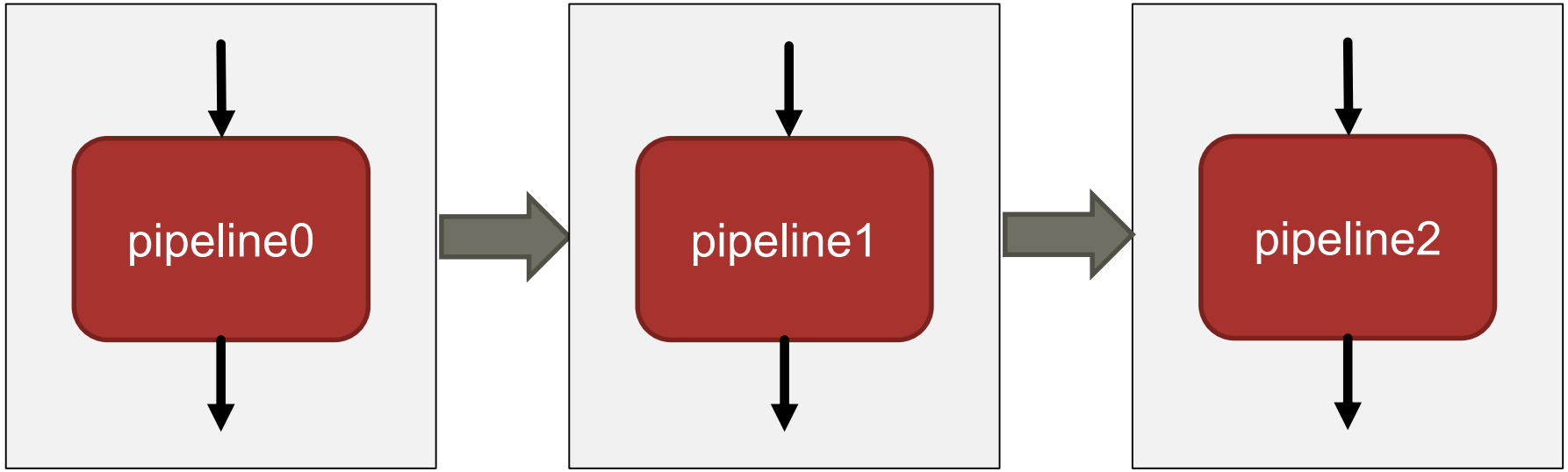

M · ((L0 + l0·N0) + (L1 + l1·N1))
L0 + l0·N0
L1 + l1·N1
(L0, l0)
(L1, l1)
(L0 + L1) + l·MN
(L, l)
FSM moved into the pipeline

Flattening


M · ((L0 + I0·N0) + (L1 + I1·N1))
L0 + I0·N0
L1 + I1·N1
(L0, I0)
(L1, I1)
(L0 + L1) + I·MN
(L, I)
FSM moved into the pipeline
We will see an example of this shortly

(Pipeline) parallel pipelines

$$(L_0 + l_0 \cdot N_0) + (L_1 + l_1 \cdot N_1) + (L_2 + l_2 \cdot N_2)$$



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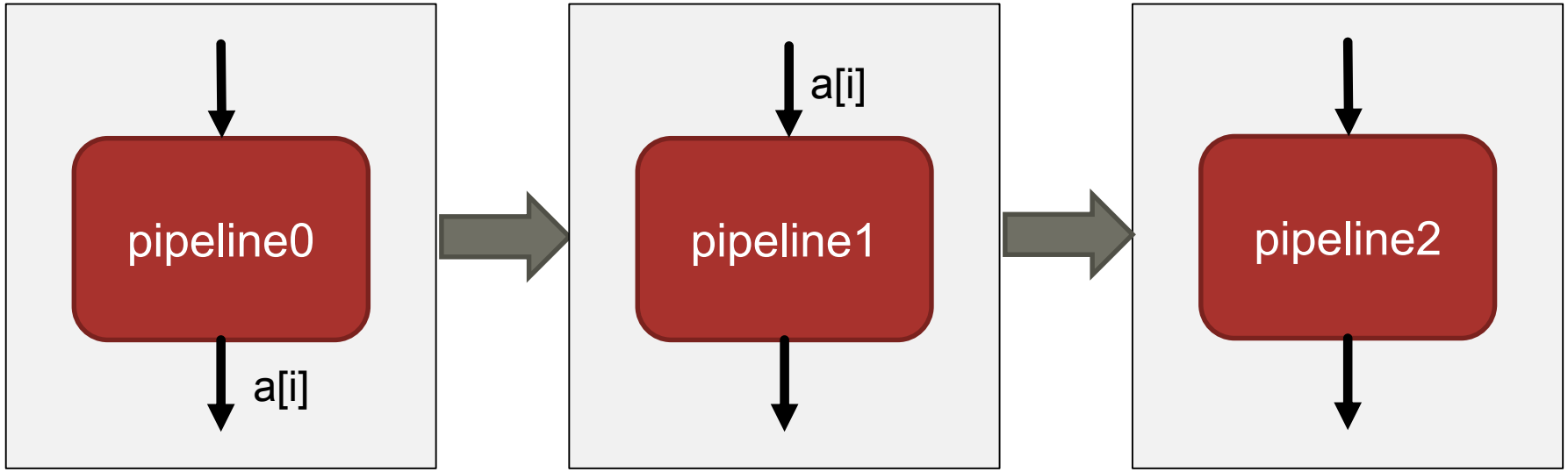

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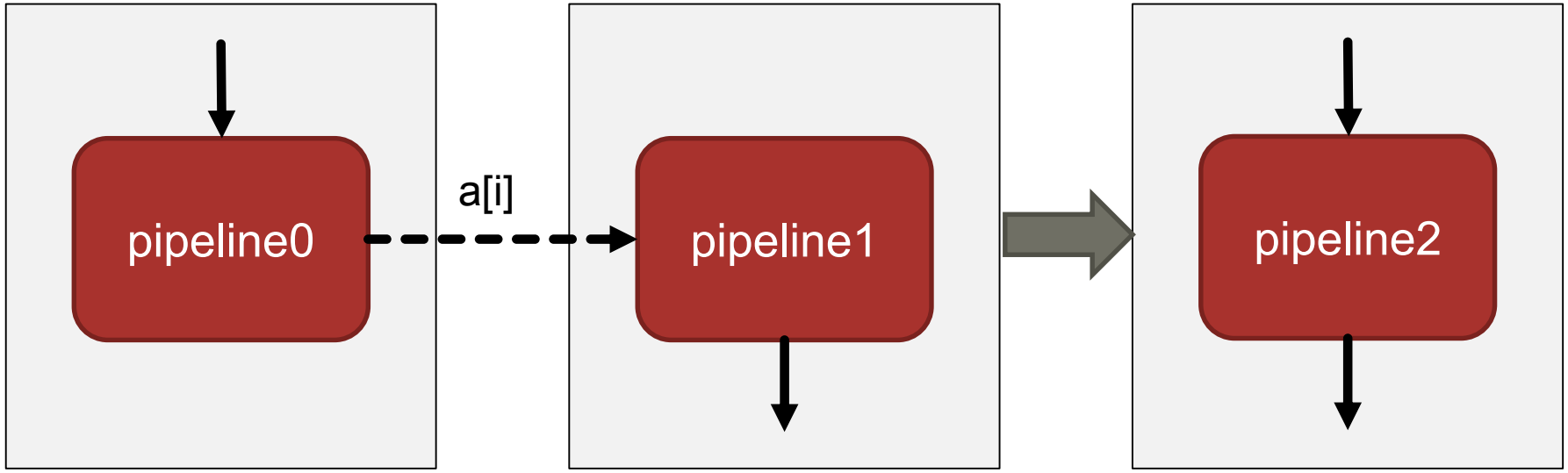
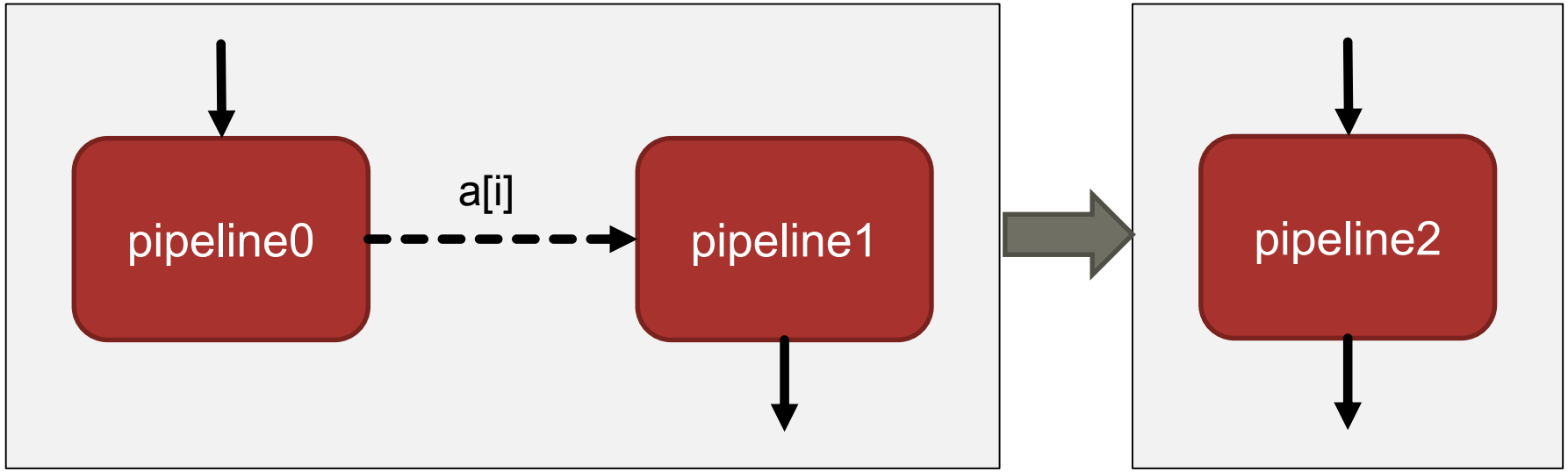


(Pipeline) parallel pipelines

$$((L_0 + L_1) + I \cdot N) + (L_2 + I_2 \cdot N_2)$$



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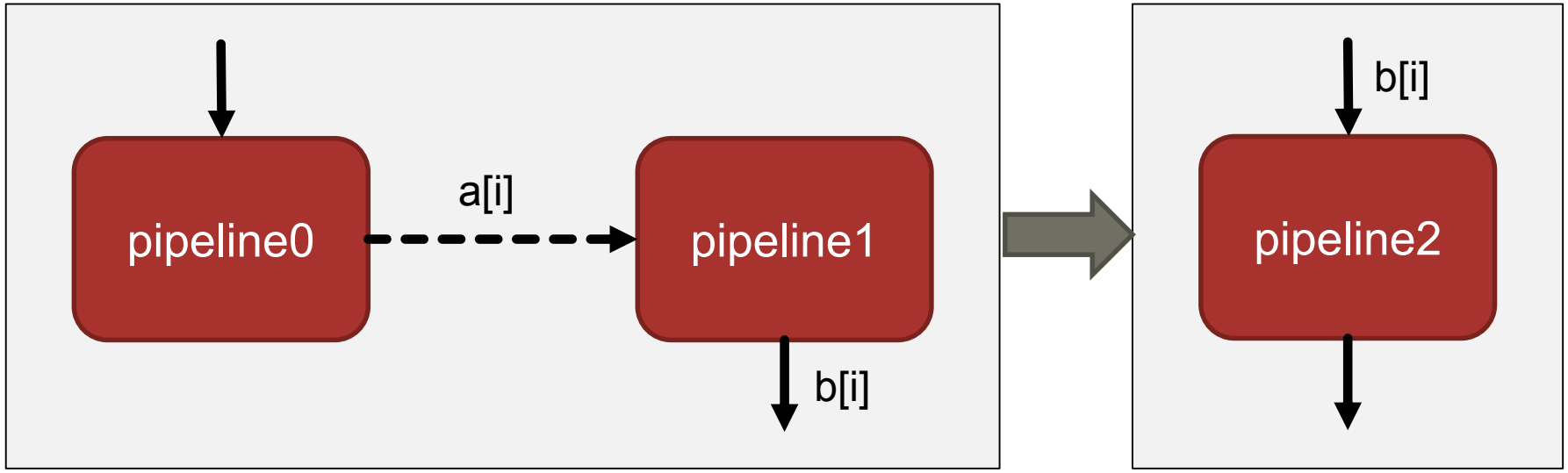

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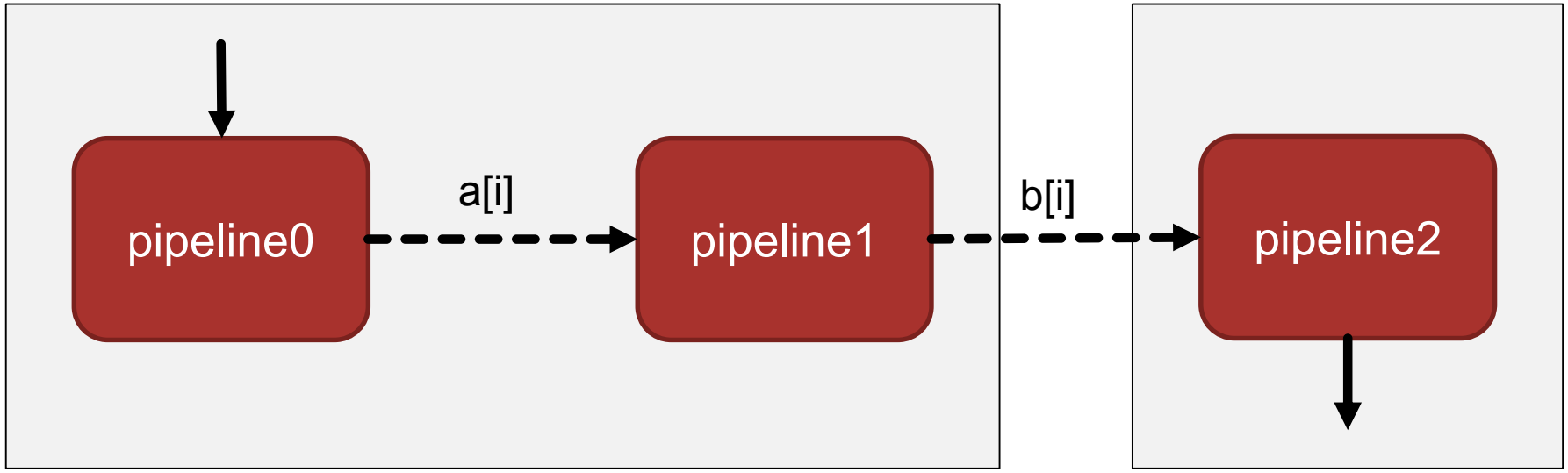
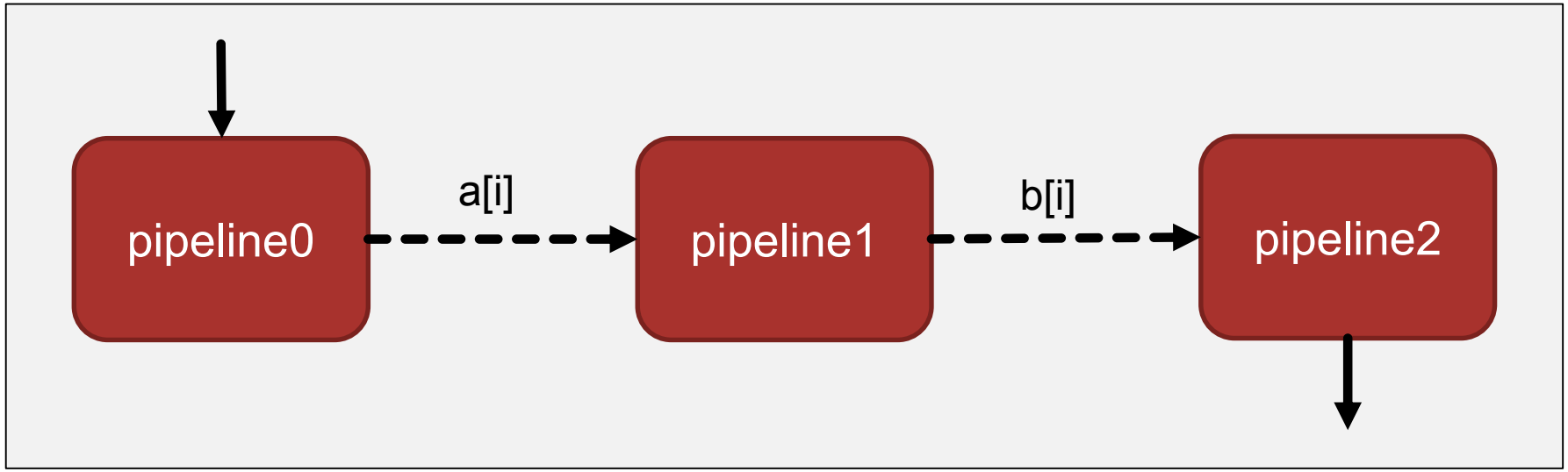


(Pipeline) parallel pipelines

$$(L_0 + L_1 + L_2) + I \cdot N$$



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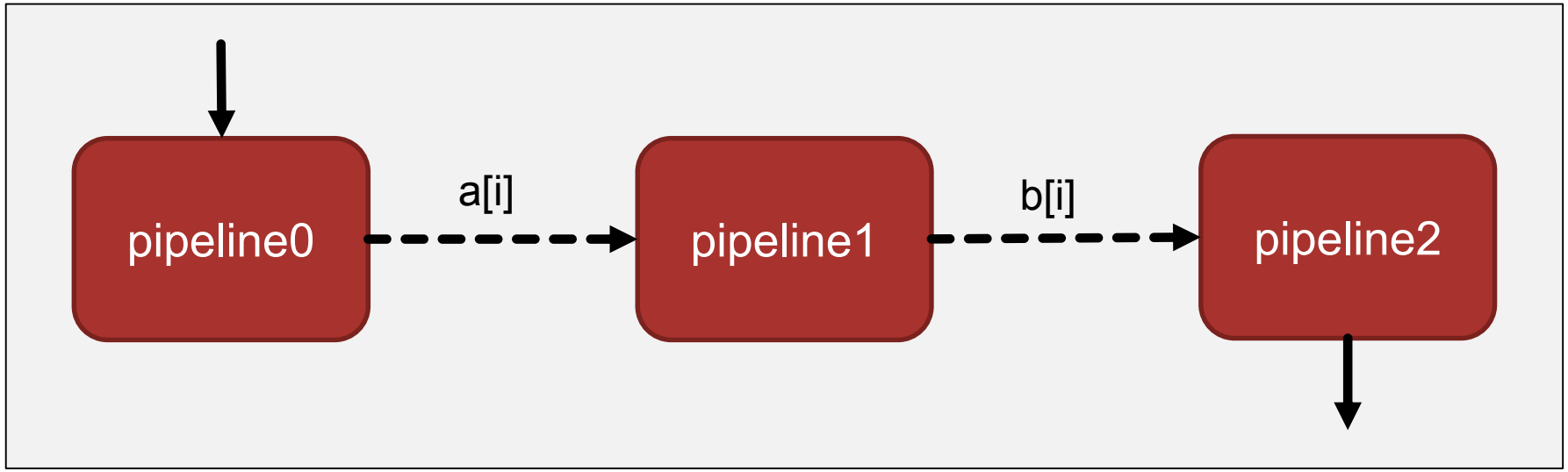
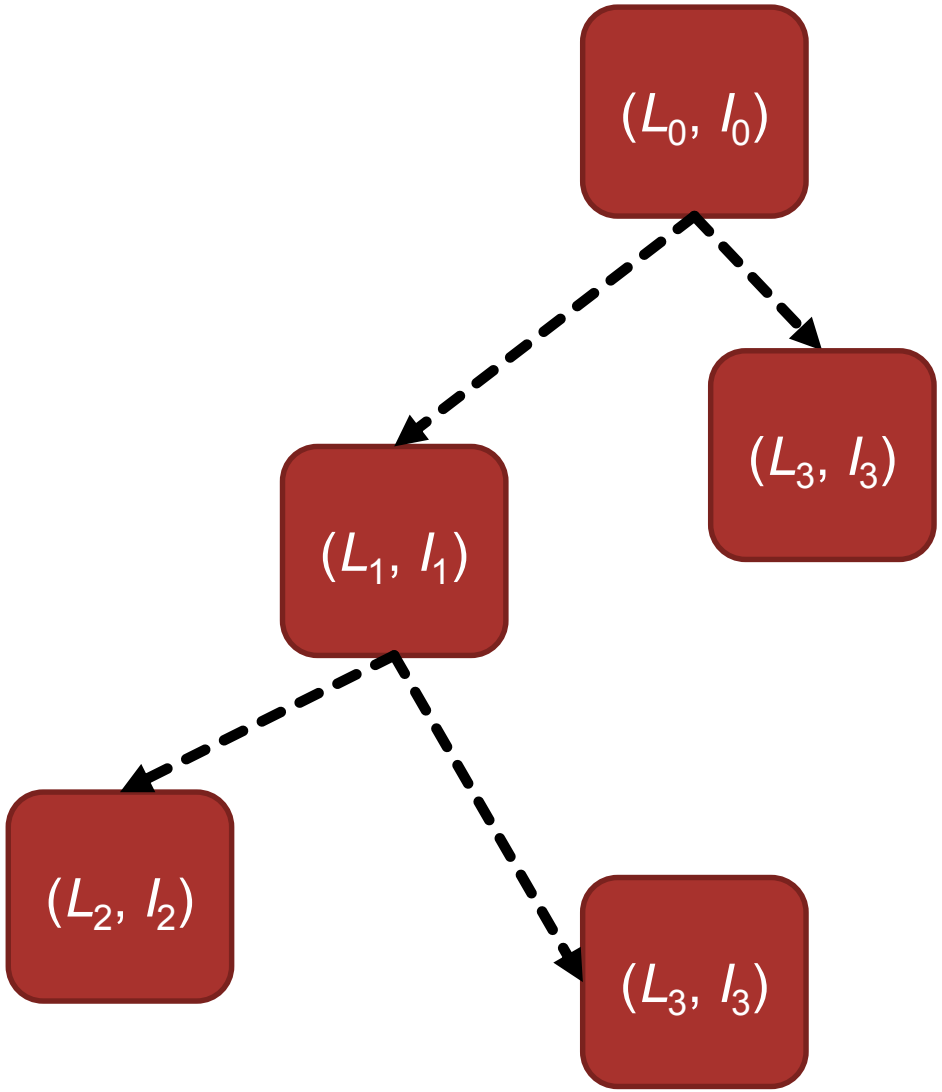
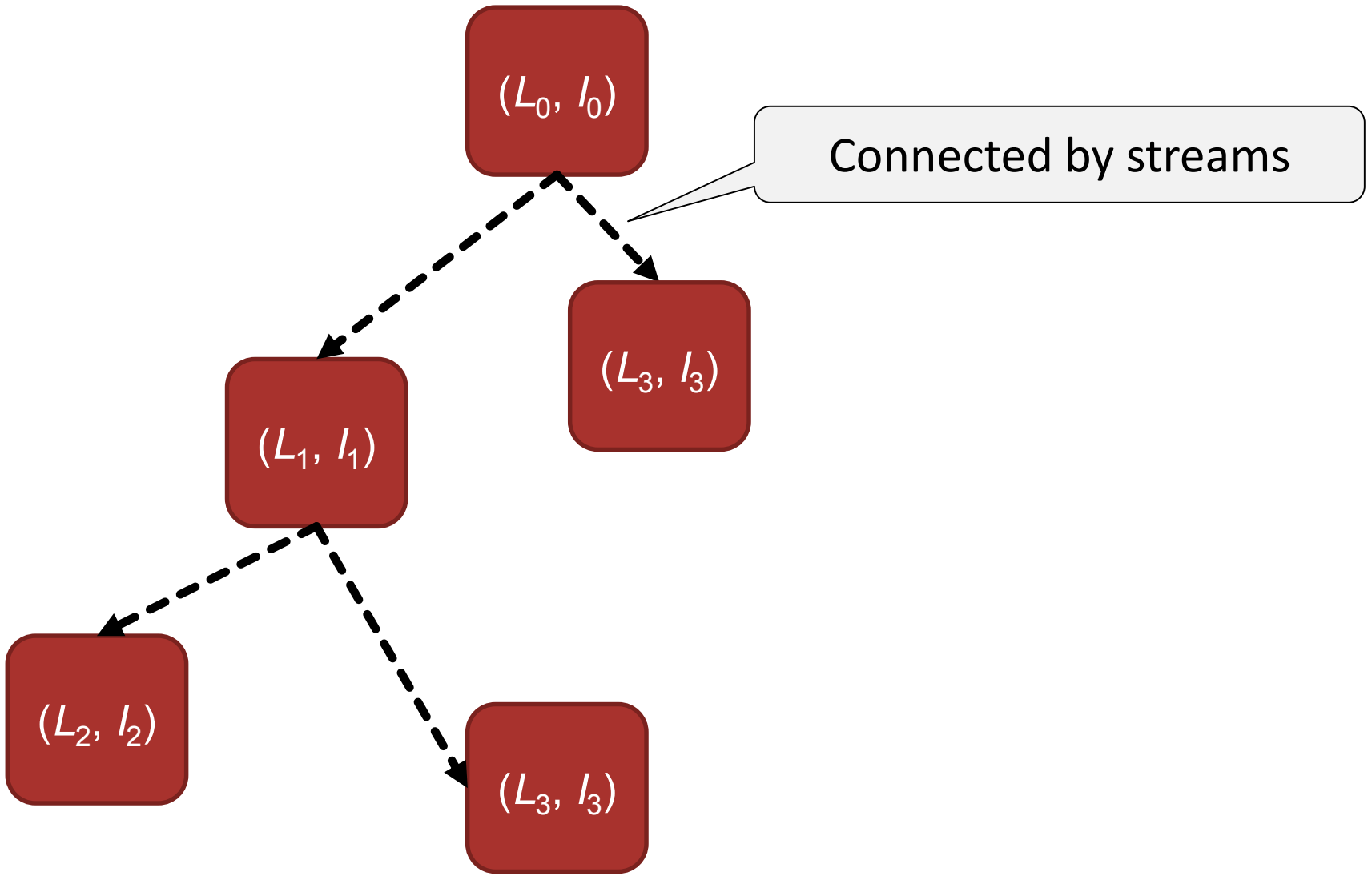


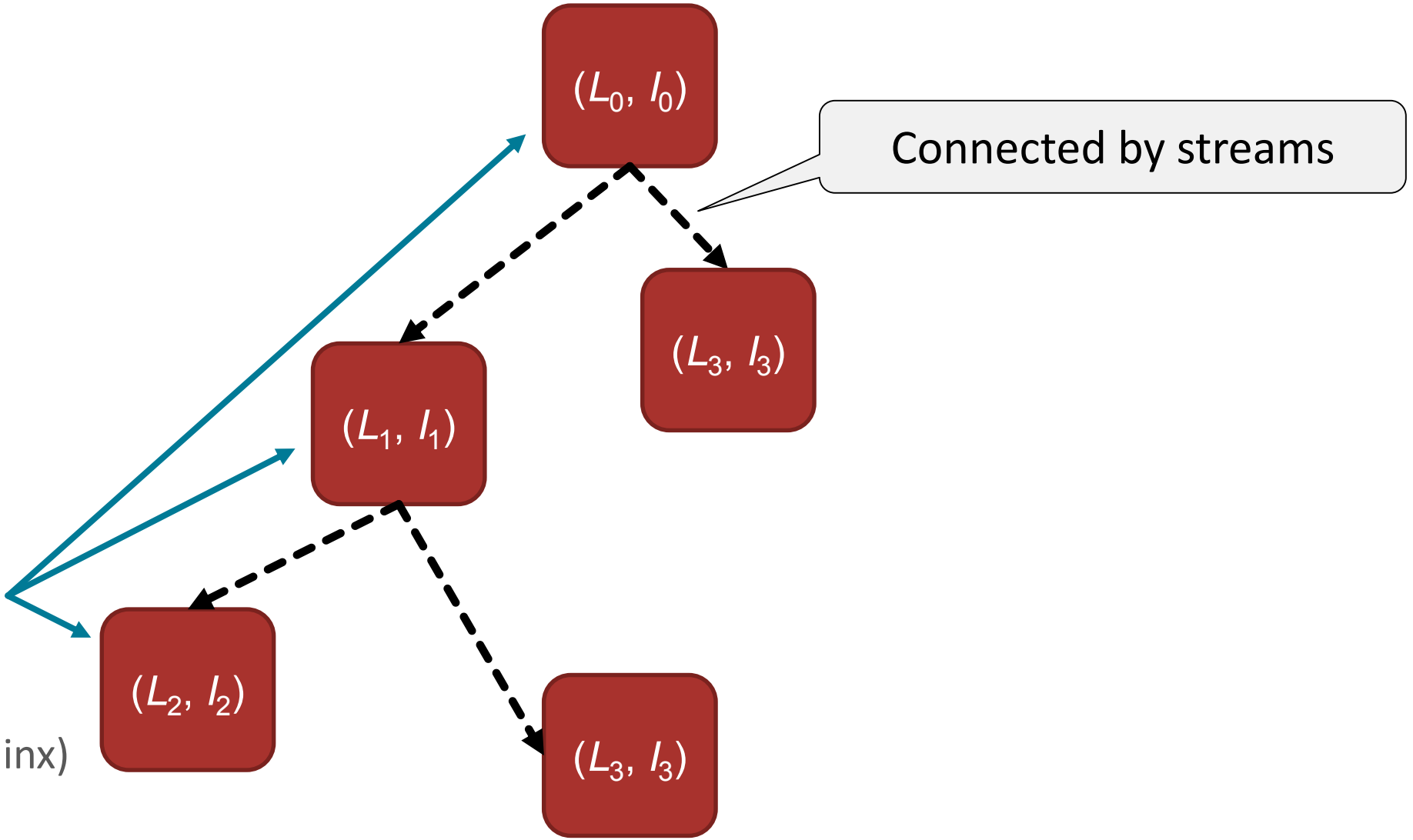
Processing elements



Processing elements



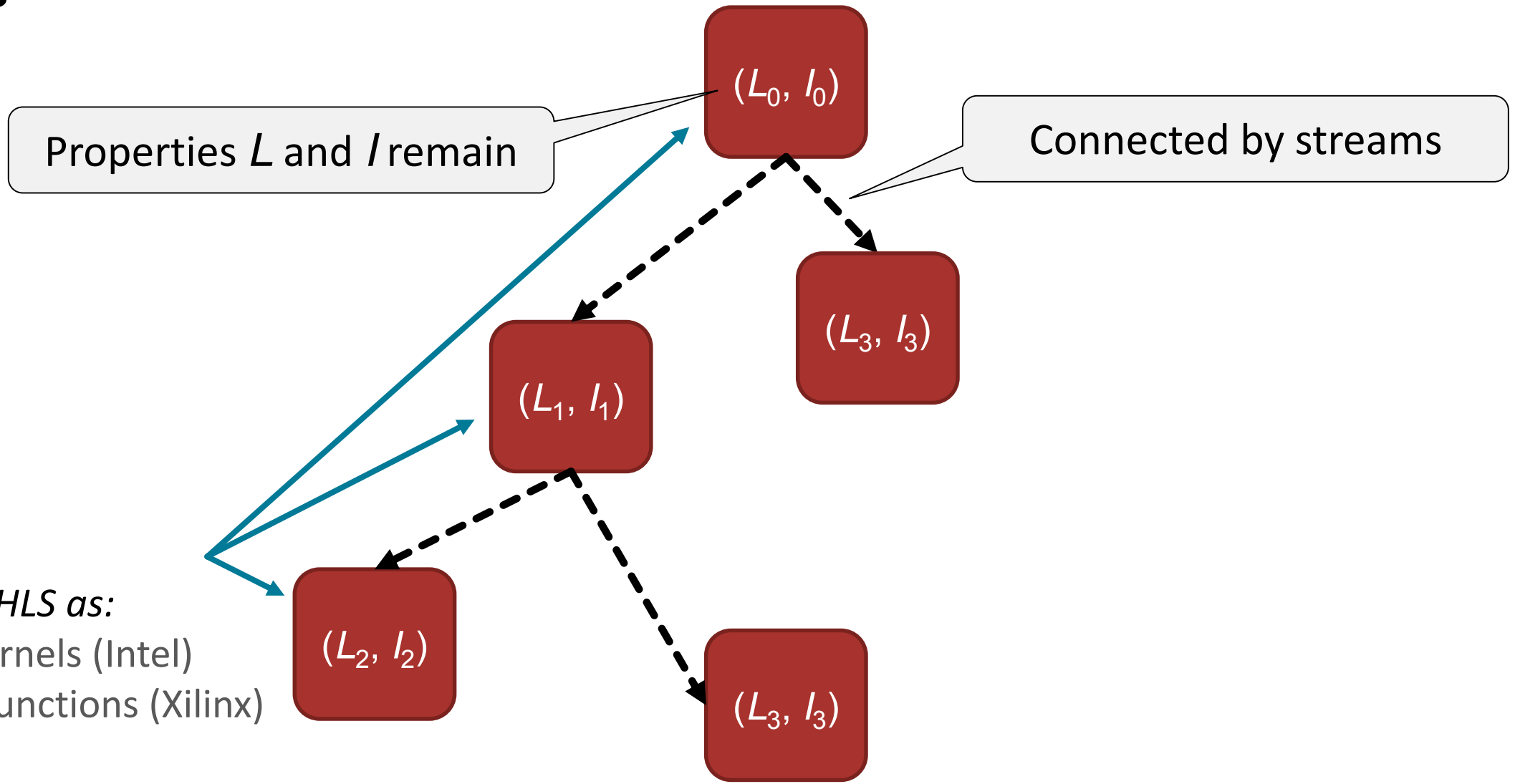
Processing elements



Expressed in HLS as:

- OpenCL kernels (Intel)
- Top-level functions (Xilinx)

Processing elements



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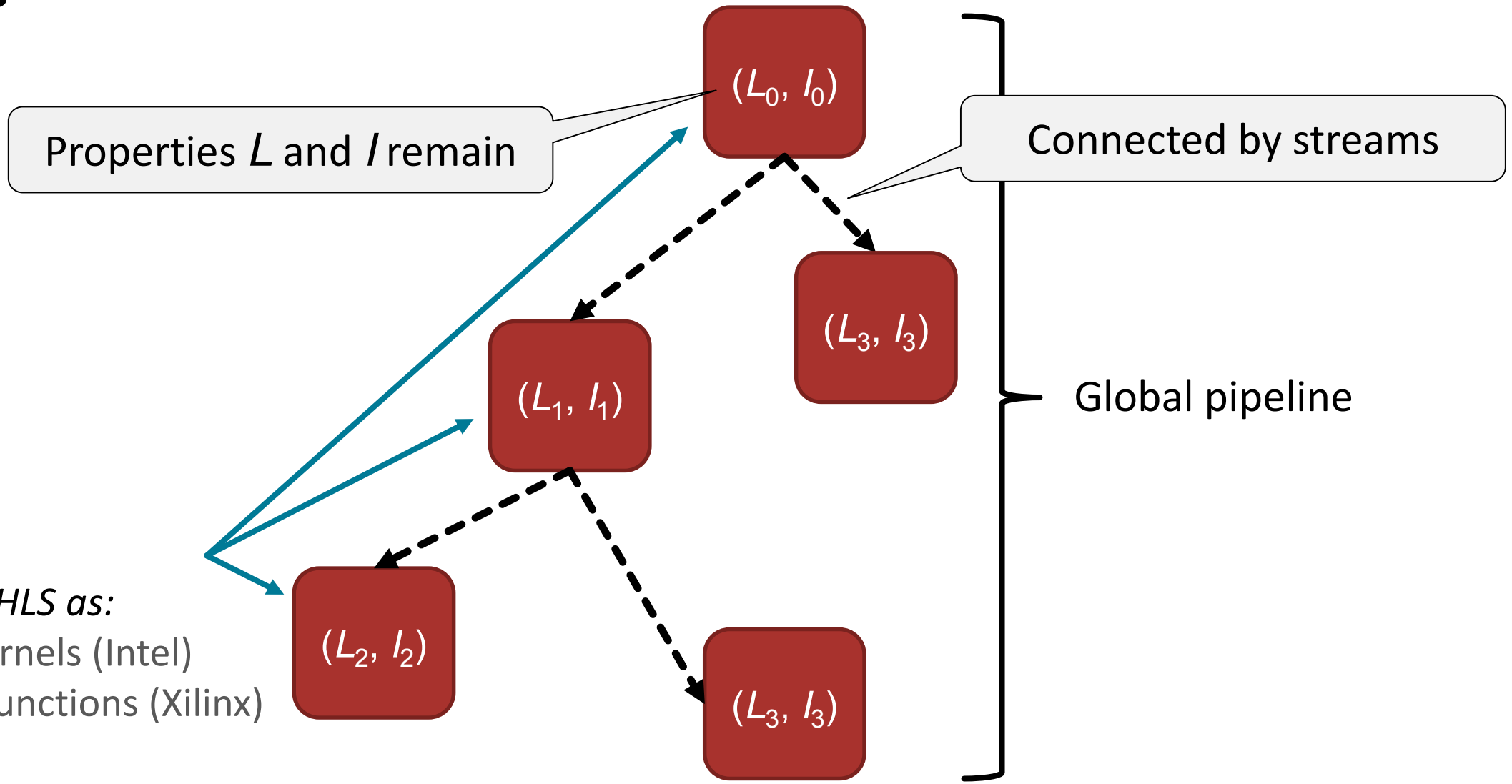

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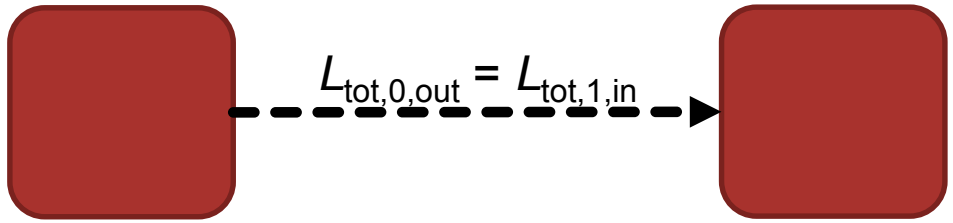
Properties of the global pipeline



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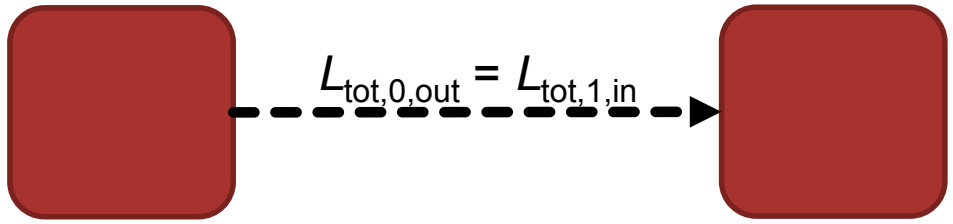
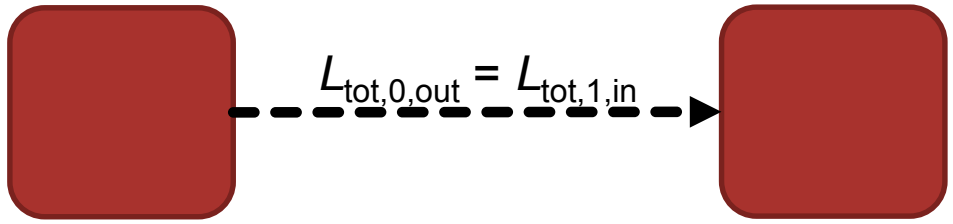


What goes in must come out:

Every stream write needs a corresponding read

Properties of the global pipeline



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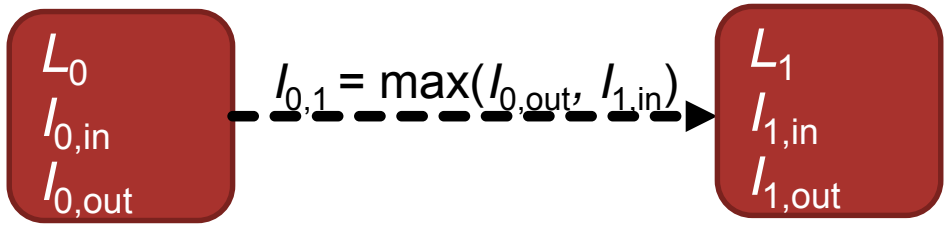

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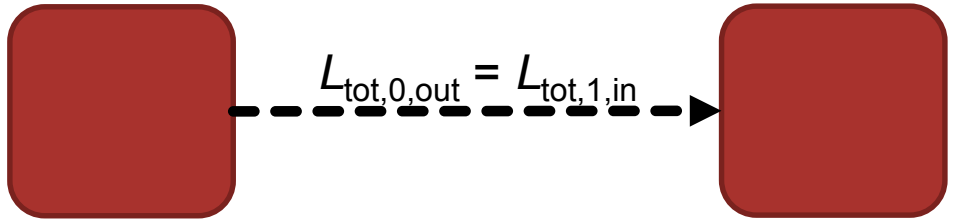

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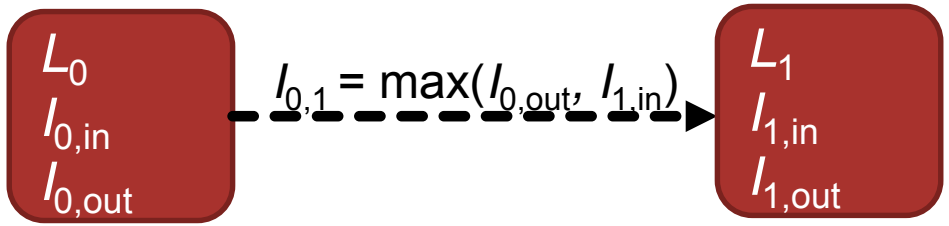
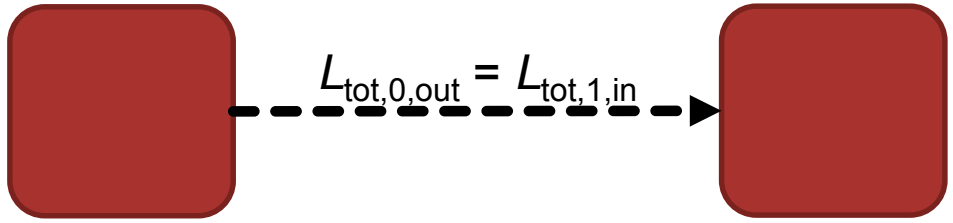


Slow dominates:
Can only stream with the highest initiation interval (producer/consumer) at each interface

Properties of the global pipeline



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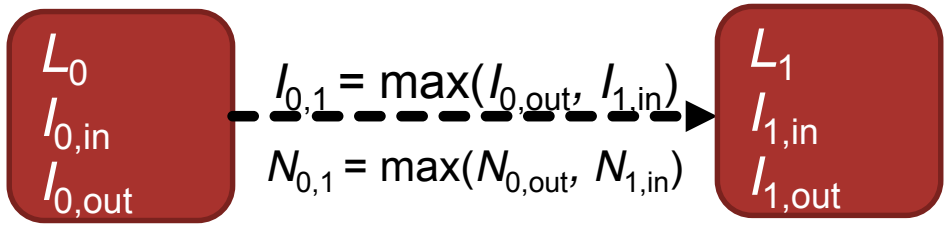

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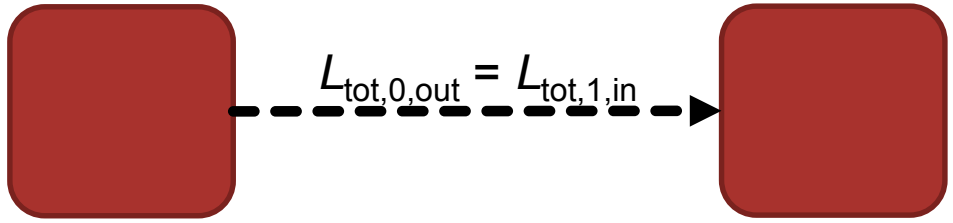

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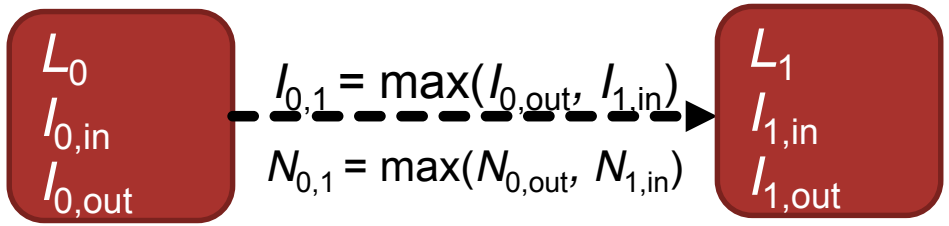

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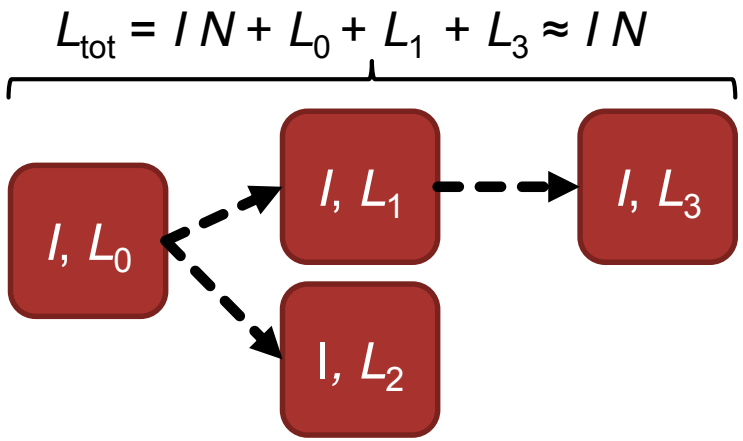

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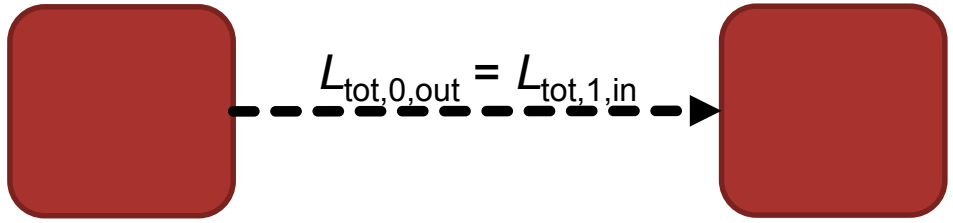

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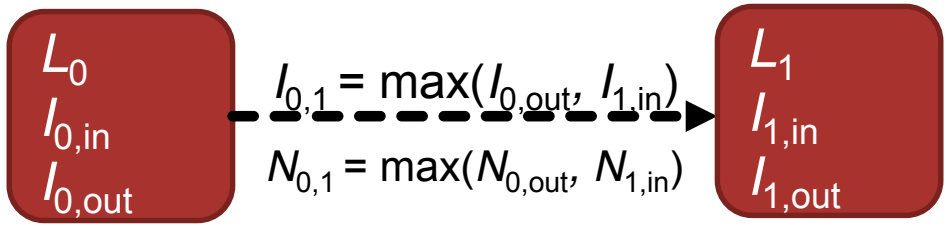

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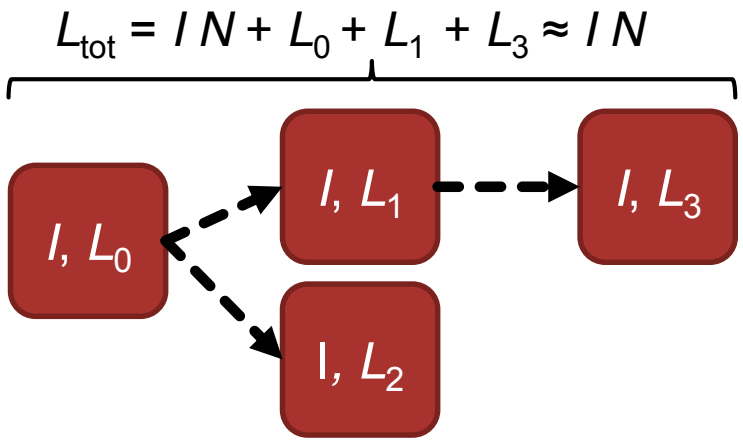


Depth is "free":
In a perfect pipeline for large N, the influence of pipeline latency is negligible w.r.t. the total runtime

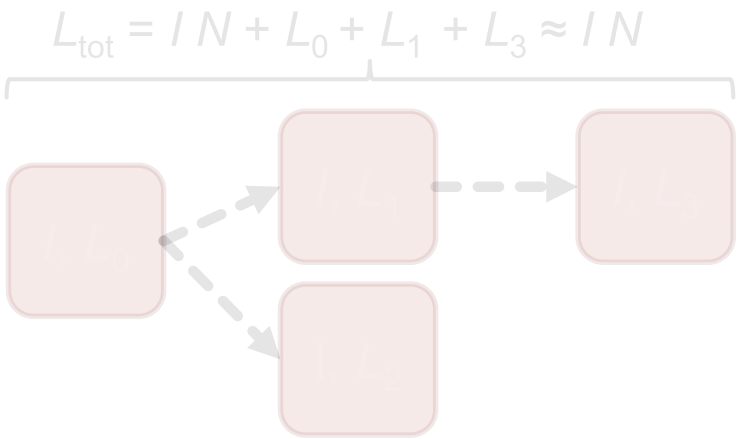
Properties of the global pipeline

What goes in must come out:
Every stream write needs a corresponding read

Sync dimensions:
Can only stream with the highest initiation interval (producer/consumer) at each interface

Let's see this in practice…

(example 4)



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Unrolling

Much stronger meaning on FPGA than for an instruction-based architecture.

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for (int w = 0; w < 4; ++w) {
  #pragma HLS PIPELINE II=1
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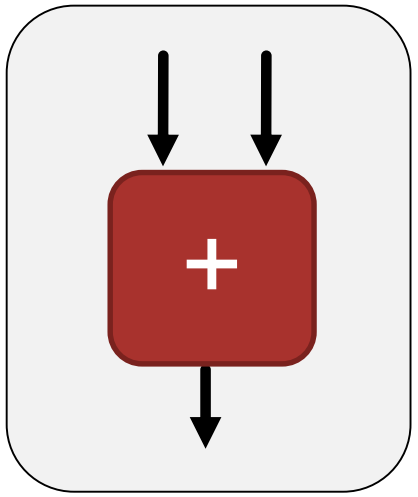

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  #pragma HLS PIPELINE II=1
  res[w] = a[w] + b[w];
}
```
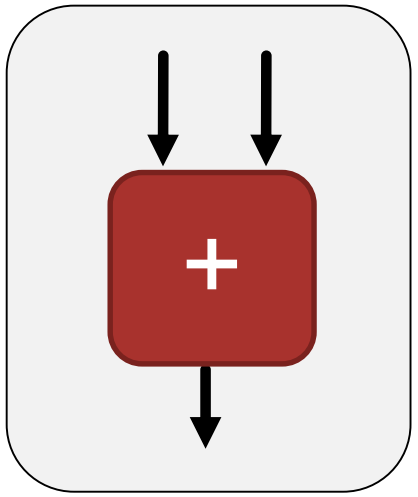

```
#pragma HLS PIPELINE II=1
for (int w = 0; w < 4; ++w) {
  #pragma HLS UNROLL
  res[w] = a[w] + b[w];
}
```



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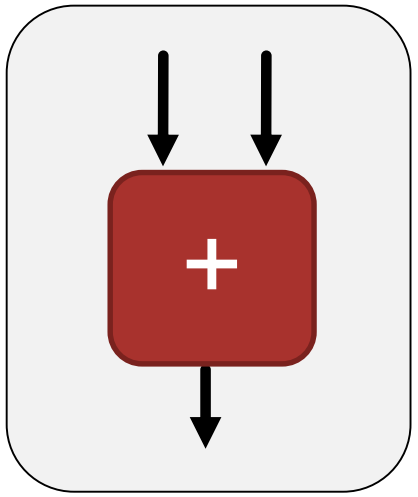
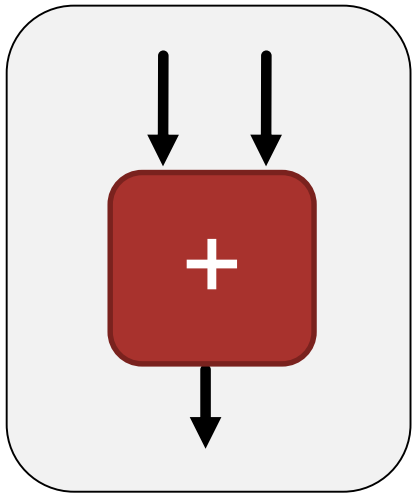



```
#pragma HLS PIPELINE II=1
res[0] = a[0] + b[0];
res[1] = a[1] + b[1];
res[2] = a[2] + b[2];
res[3] = a[3] + b[3];
```

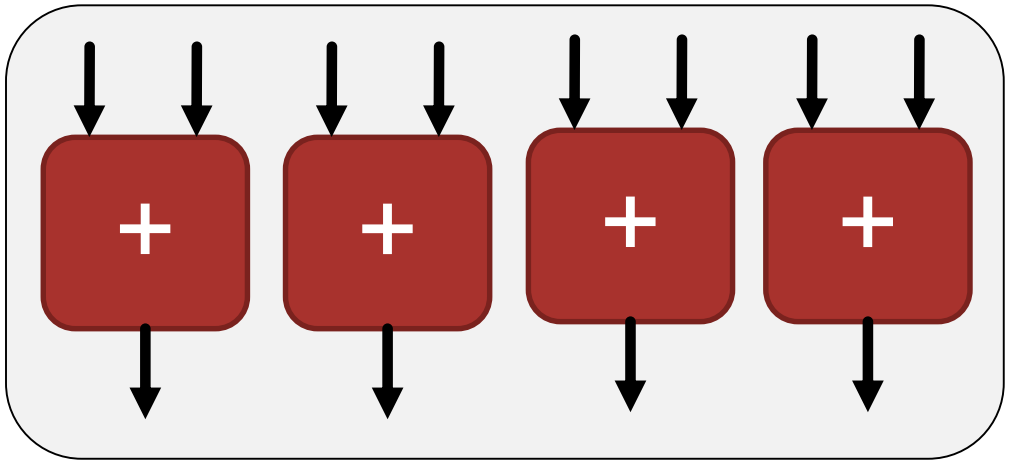
Unrolling

Much stronger meaning on FPGA than for an instruction-based architecture.

```
for (int w = 0; w < 4; ++w) {
  #pragma HLS PIPELINE II=1
  res[w] = a[w] + b[w];
}
```




```
#pragma HLS PIPELINE II=1
res[0] = a[0] + b[0];
res[1] = a[1] + b[1];
res[2] = a[2] + b[2];
res[3] = a[3] + b[3];
```



Unrolling

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```
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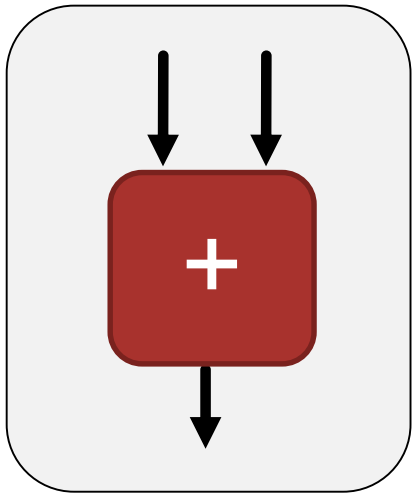
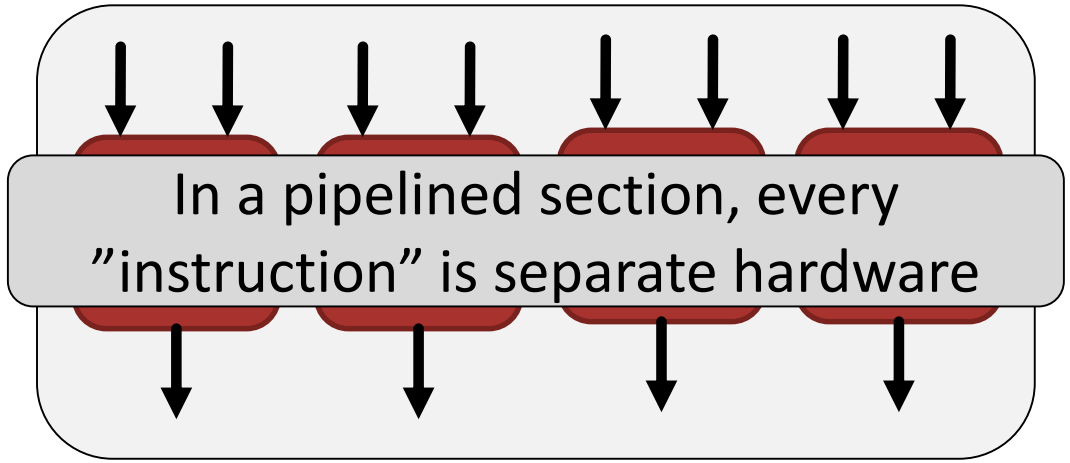



```
#pragma HLS PIPELINE II=1
res[0] = a[0] + b[0];
res[1] = a[1] + b[1];
res[2] = a[2] + b[2];
res[3] = a[3] + b[3];
```

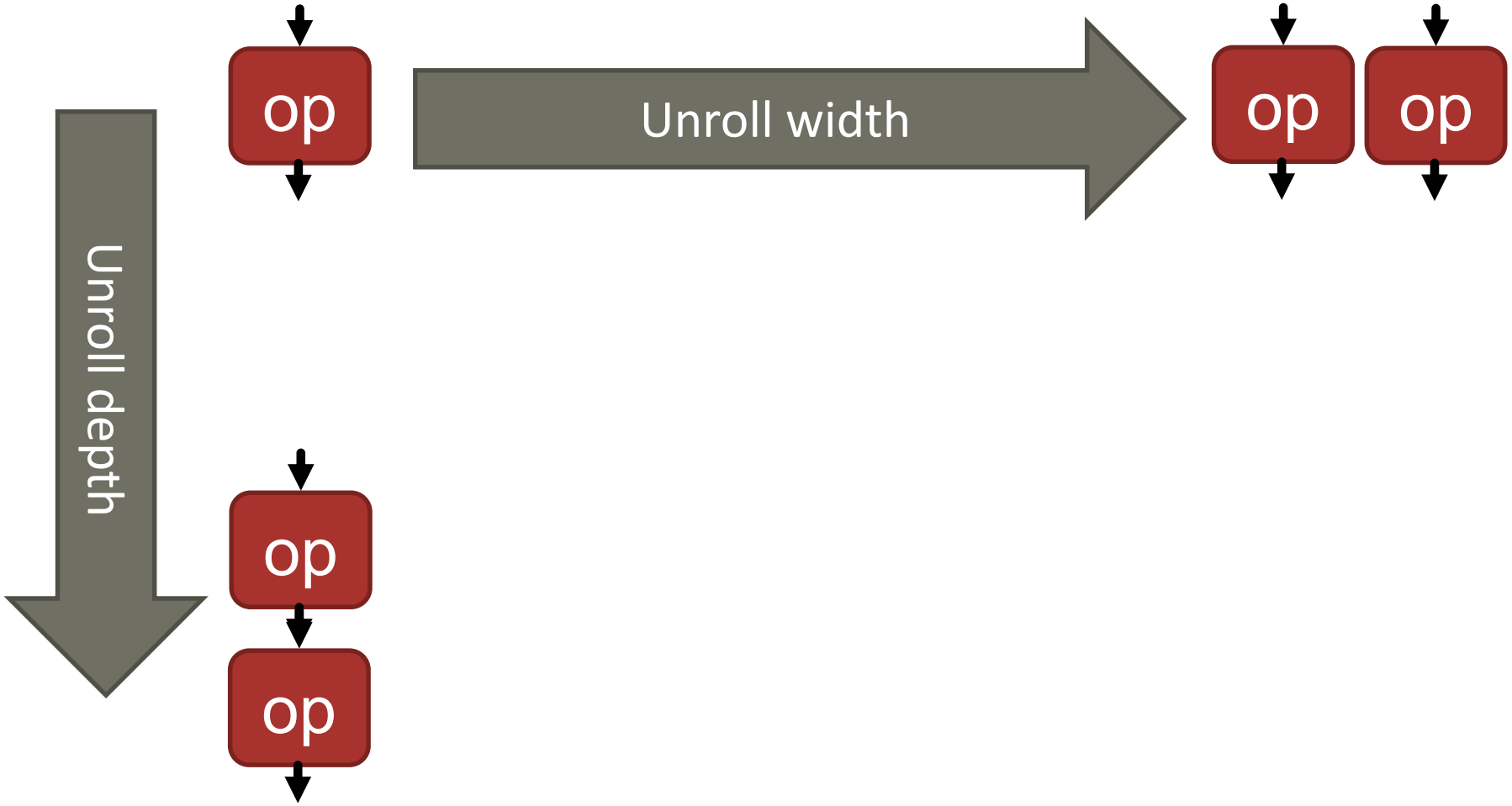


Unrolling is scaling

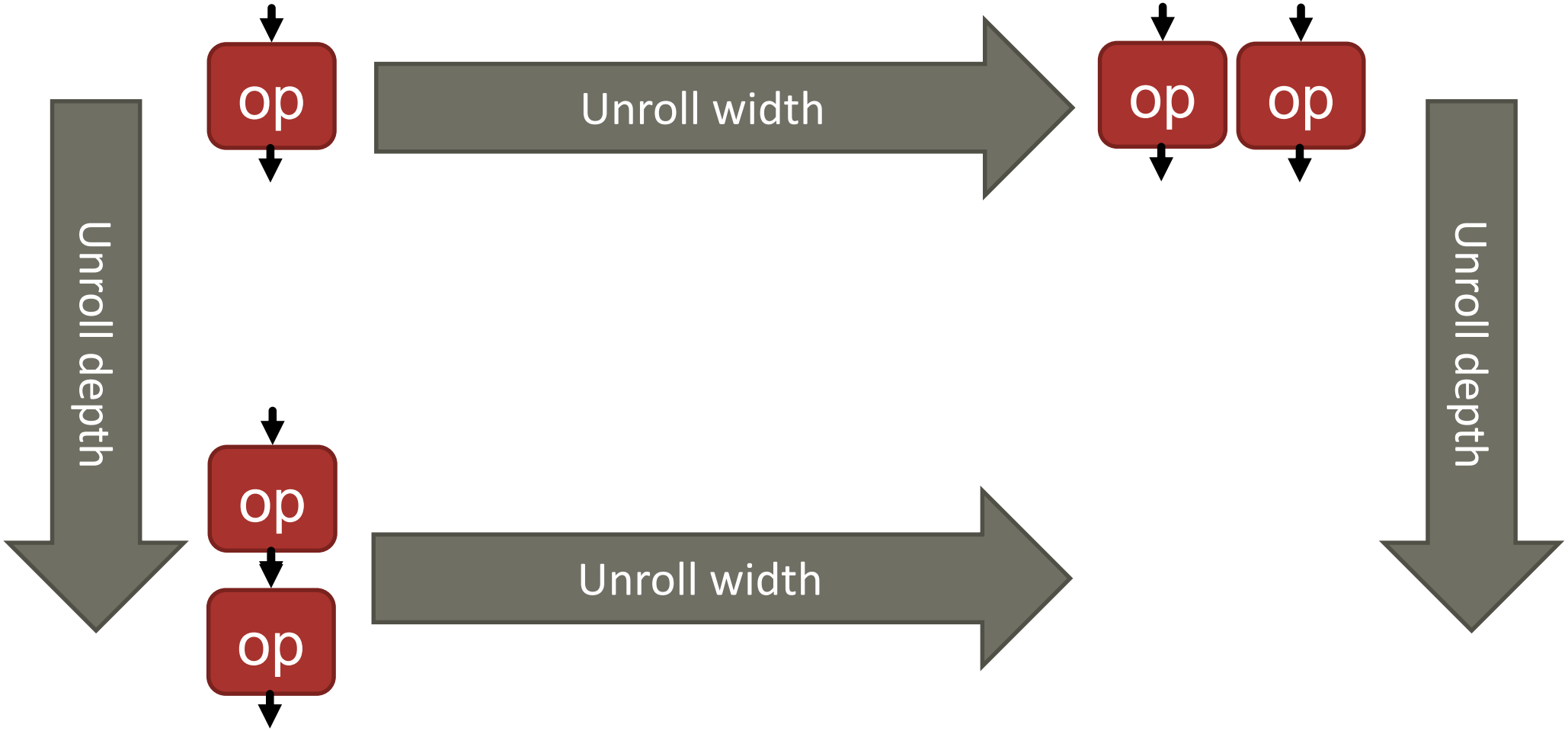
Unrolling is scaling

Unrolling is scaling

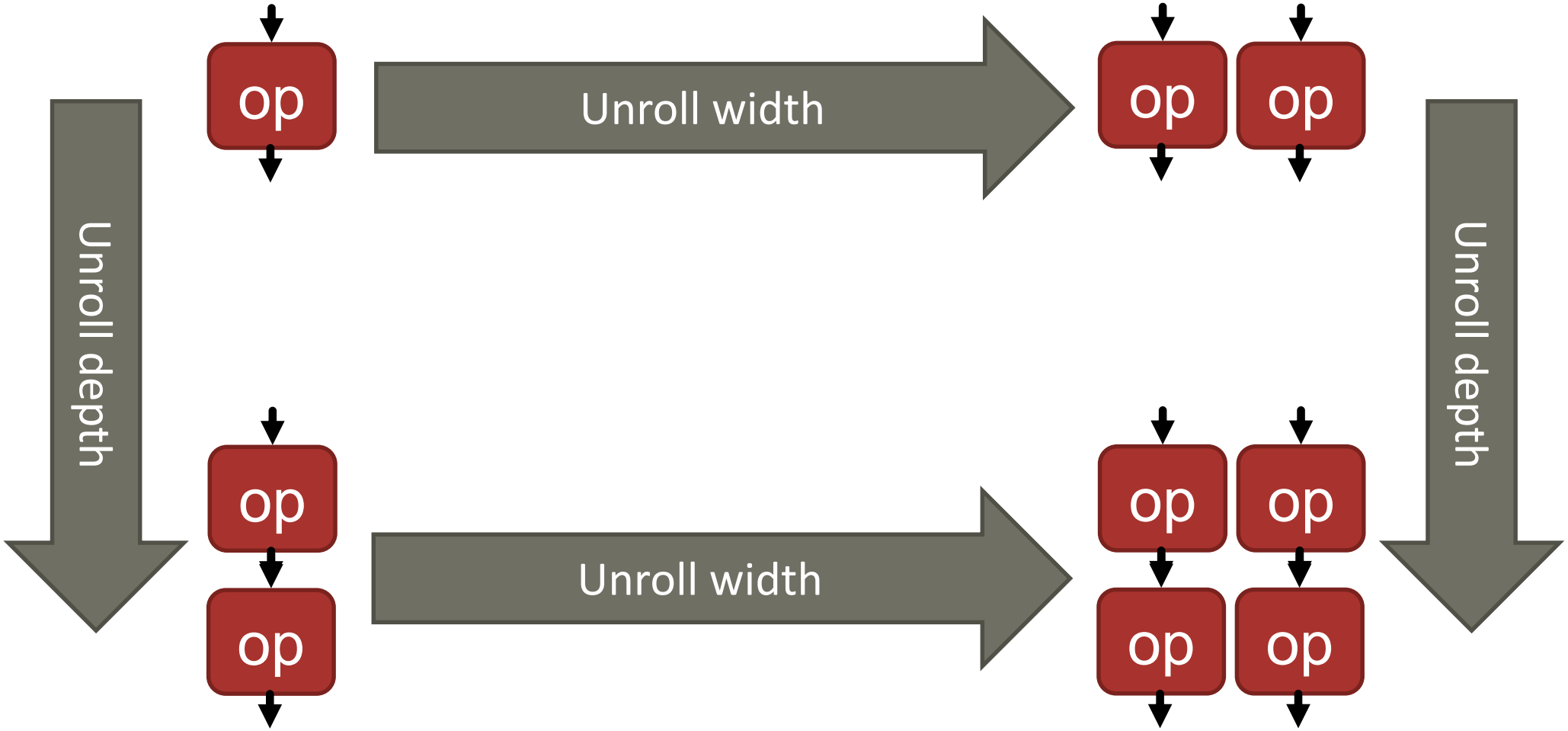
Unrolling is scaling



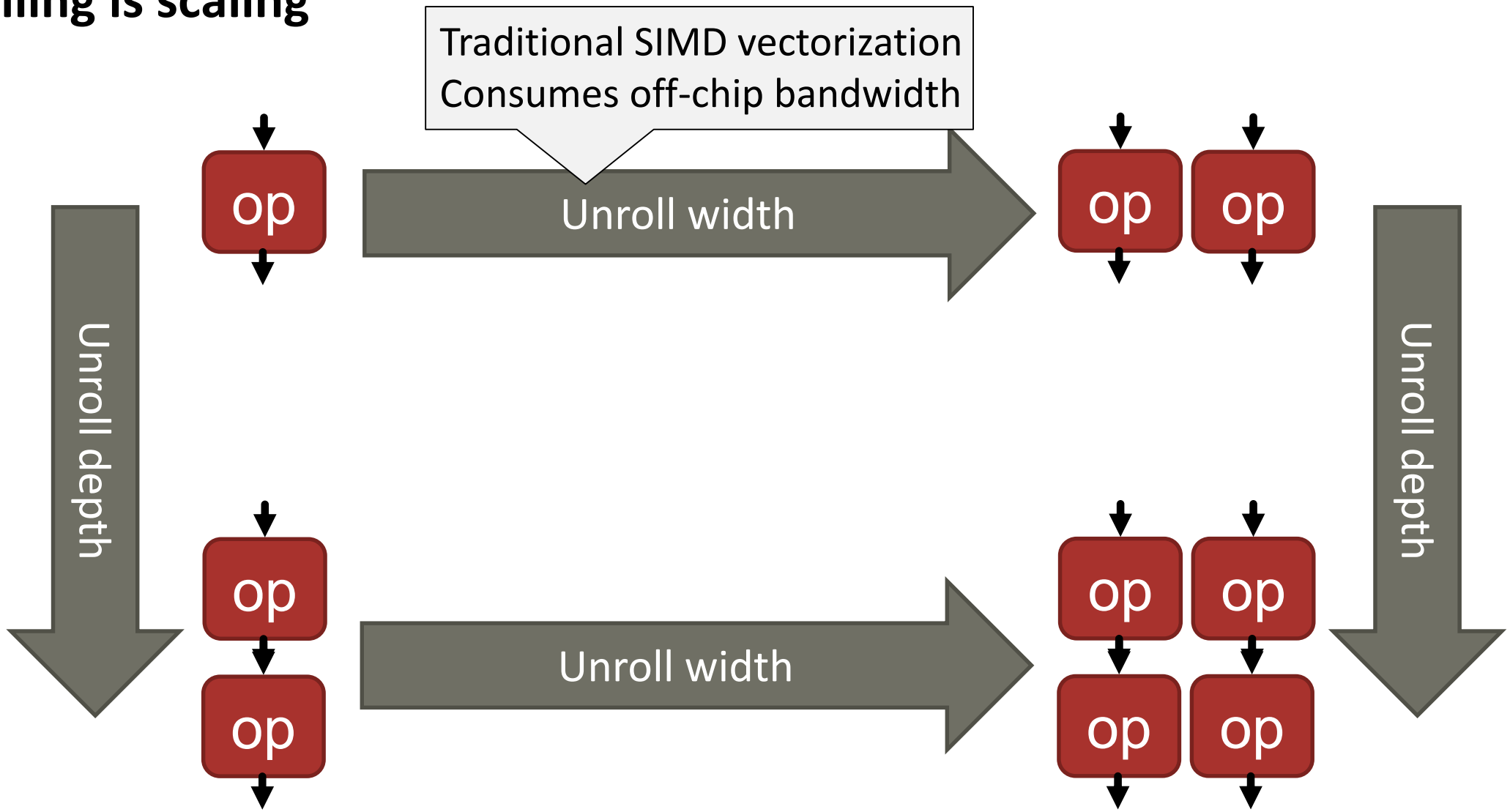
Unrolling is scaling



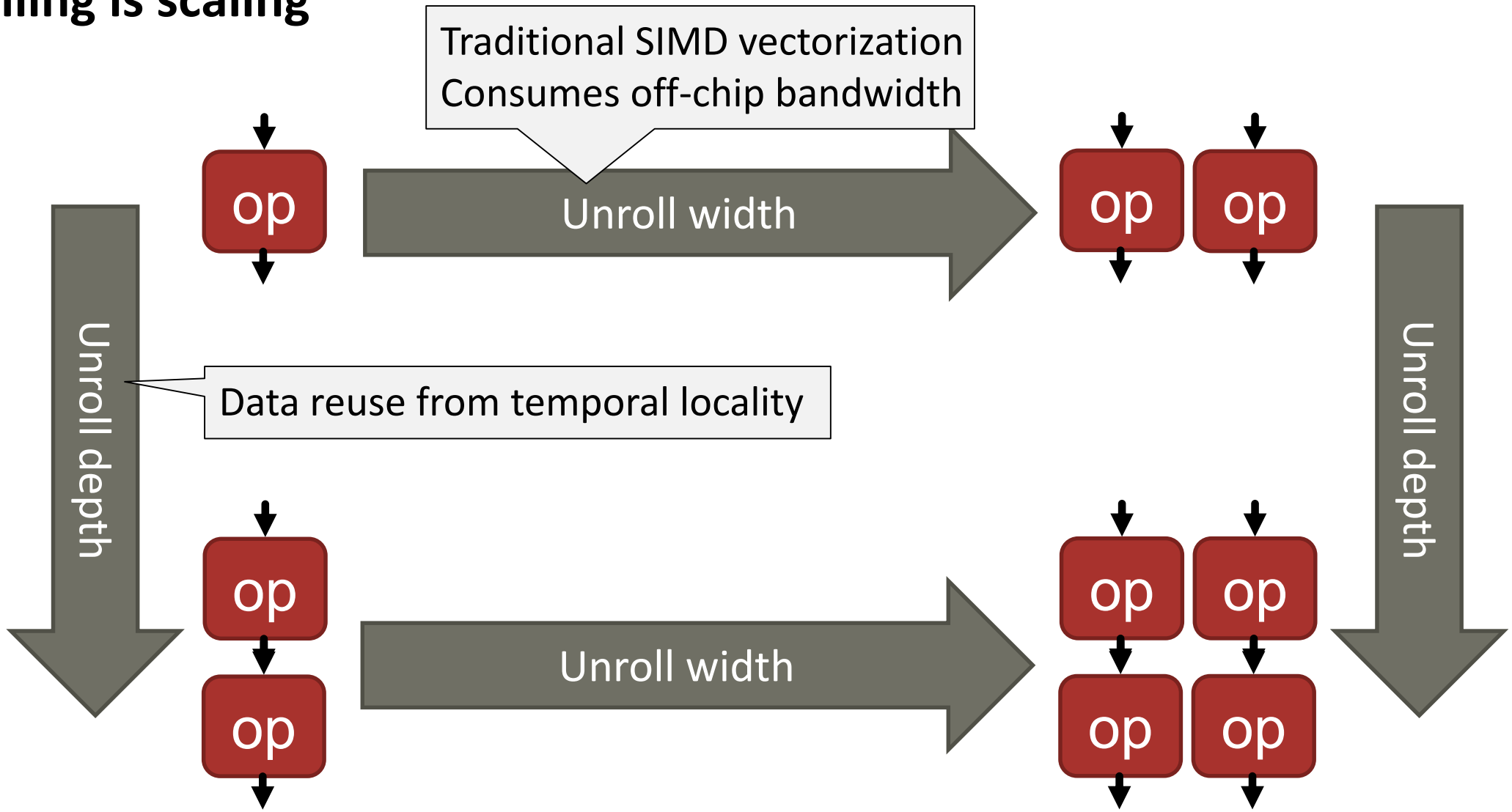
Unrolling is scaling



Unrolling is scaling

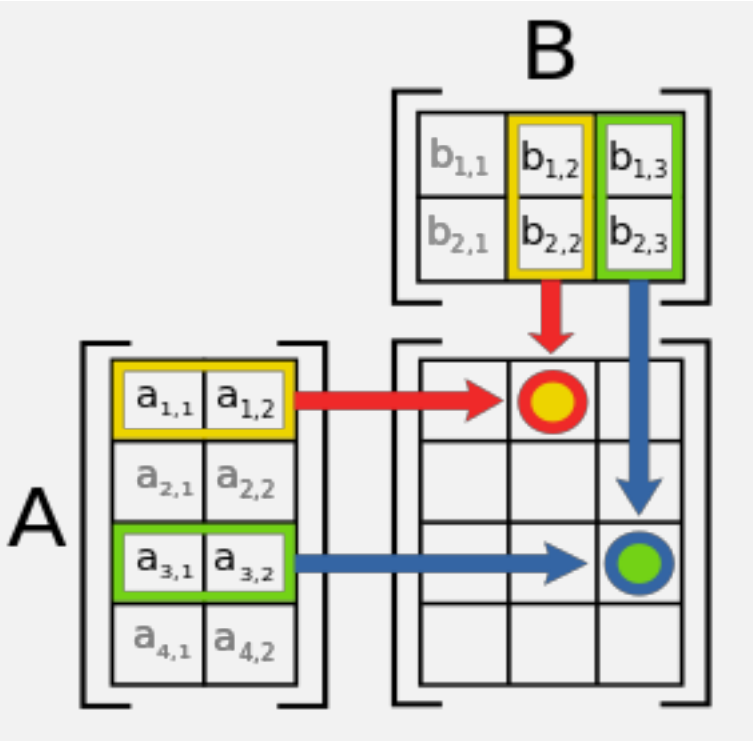


Unrolling is scaling



Matrix-matrix multiplication

```
for (int n = 0; n < N; ++n)
  for (int p = 0; p < P; ++p)
    for (int m = 0; m < M; ++m)
      C[n, p] += A[n, m] * B[m, p];
```



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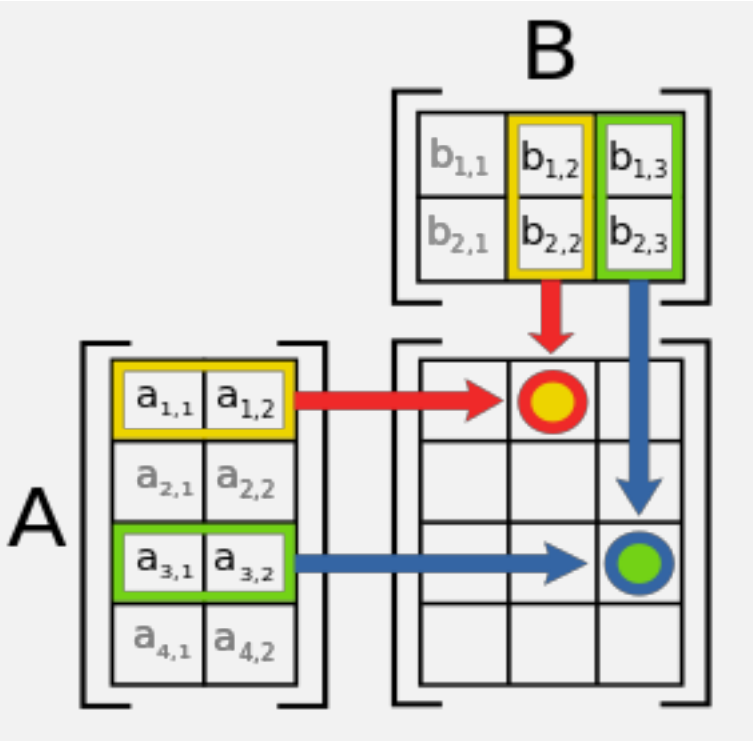

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      C[n, p] += A[n, m] * B[m, p];
```
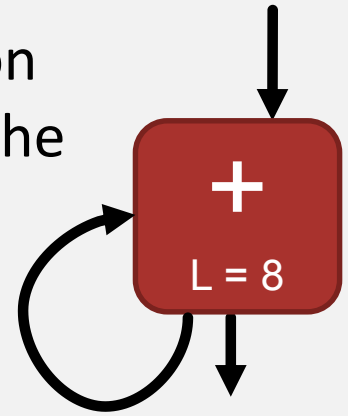
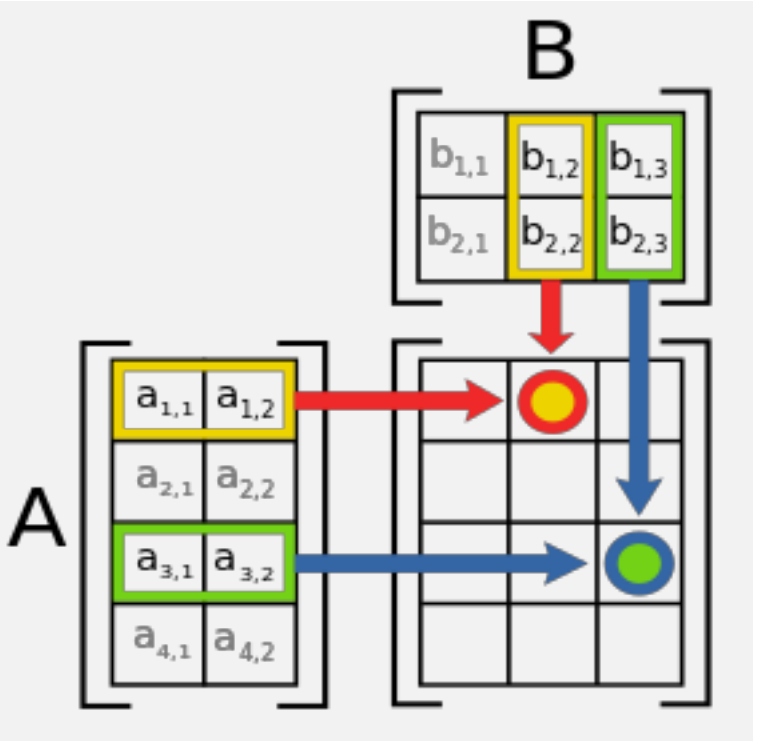

Every iteration depends on the previous:





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```
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  for (int p = 0; p < P; ++p)
    for (int m = 0; m < M; ++m)
      C[n, p] += A[n, m] * B[m, p];
```
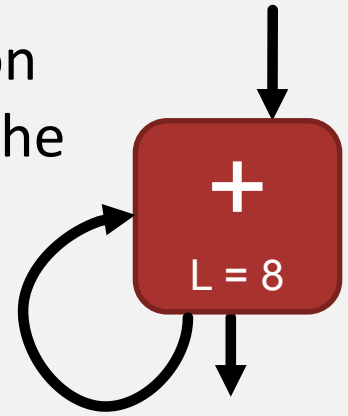
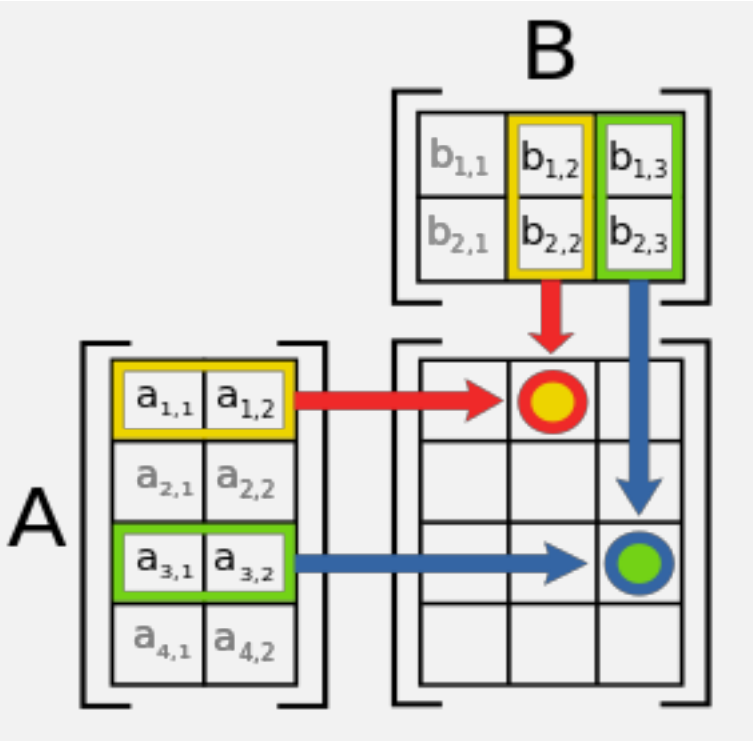

Every iteration depends on the previous:

$I = 8$





Matrix-matrix multiplication

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for (int n = 0; n < N; ++n)
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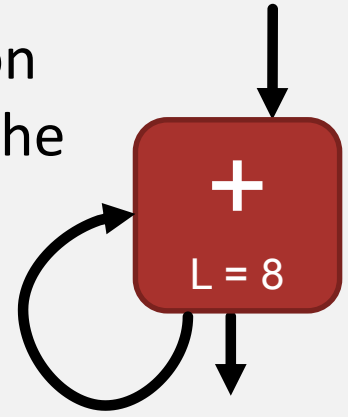
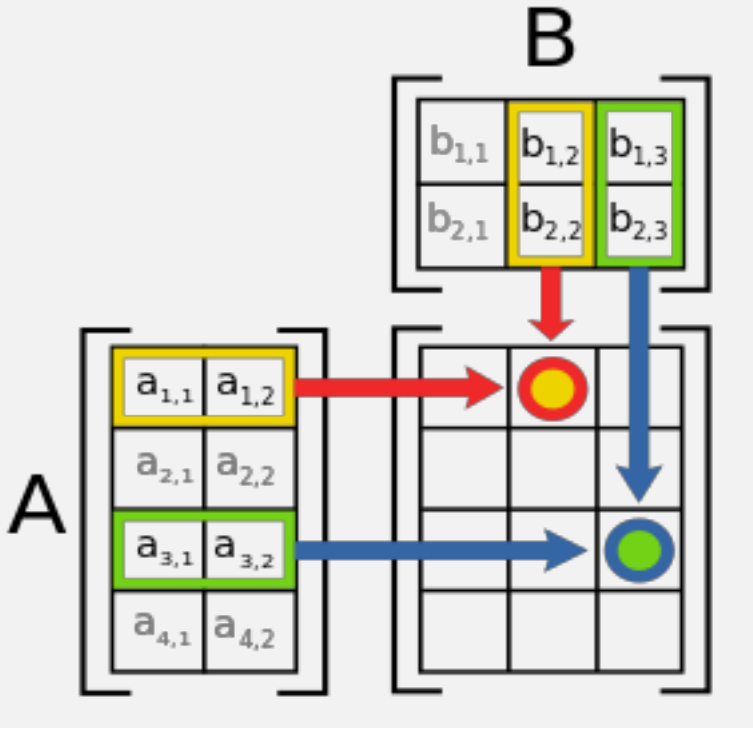
    for (int m = 0; m < M; ++m)
      C[n, p] += A[n, m] * B[m, p];
```

Our intuition of temporal locality does not work here!

Every iteration depends on the previous:



$I = 8$



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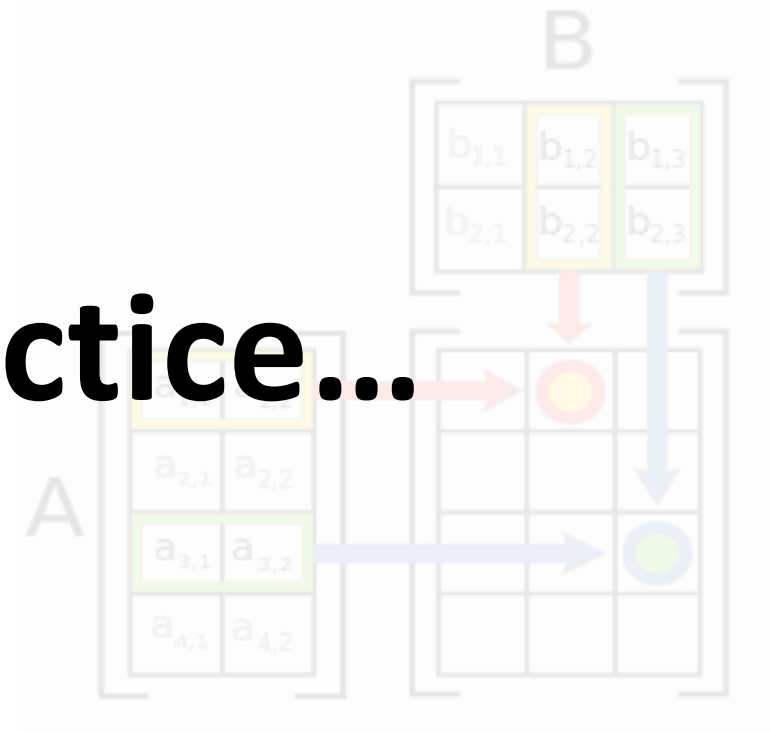


Let's see this in practice…

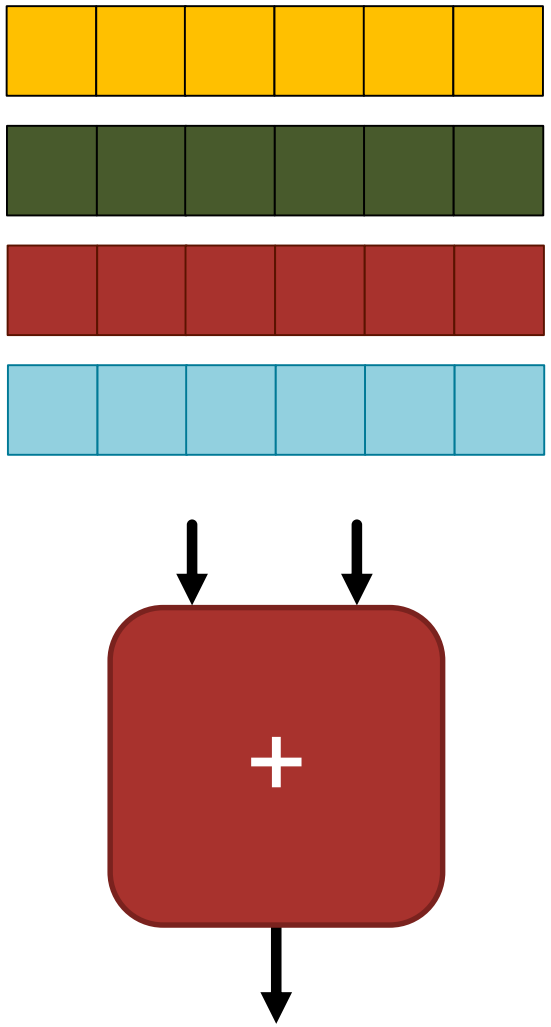
(example 5)

Our intuition of temporal locality does not work here!

Every iteration depends on the previous:

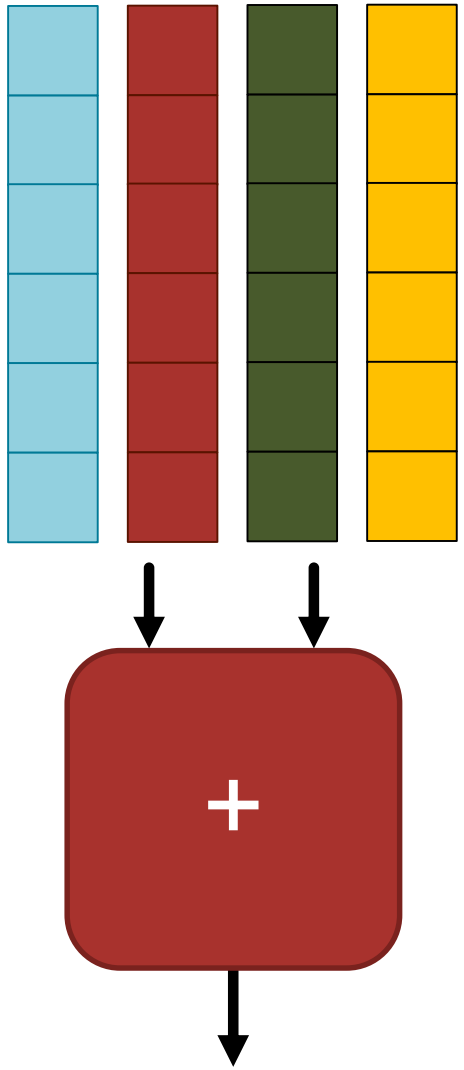
l = 8

Solving loop-carried data dependencies



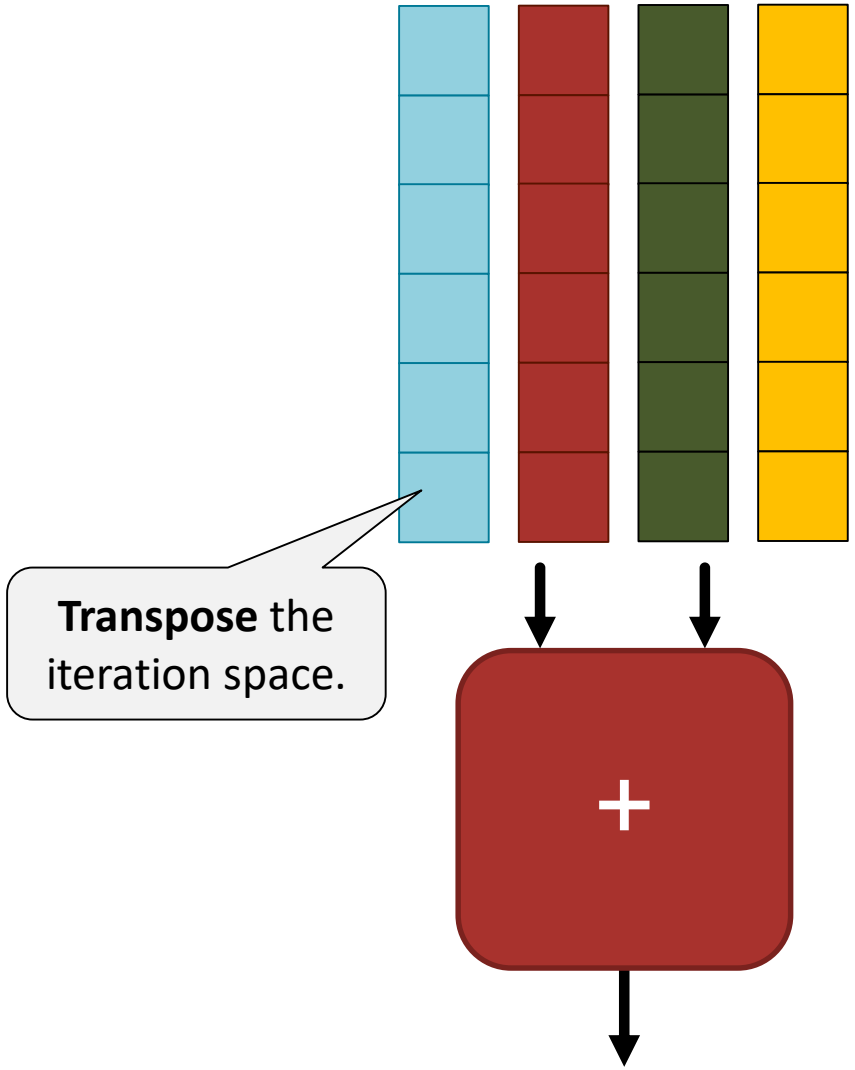

```
for (int i = 0; i < N; ++i) {
  float acc = 0;
  for (int j = 0; j < M; ++j) {
    acc += in.Pop();
  }
  out.Push(acc);
}
```

Solving loop-carried data dependencies



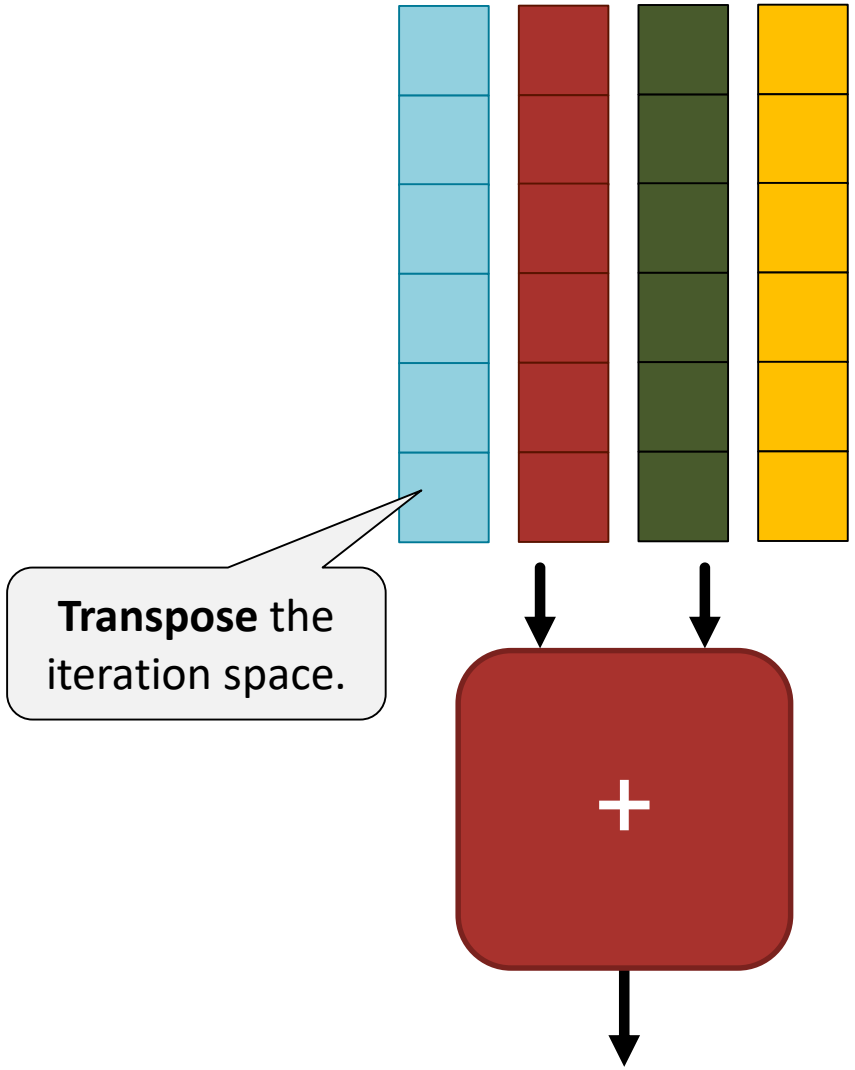

```
for (int i = 0; i < N; ++i) {
  float acc = 0;
  for (int j = 0; j < M; ++j) {
    acc += in.Pop();
  }
  out.Push(acc);
}
```

Solving loop-carried data dependencies




```
for (int i = 0; i < N; ++i) {
  float acc = 0;
  for (int j = 0; j < M; ++j) {
    acc += in.Pop();
  }
  out.Push(acc);
}
```

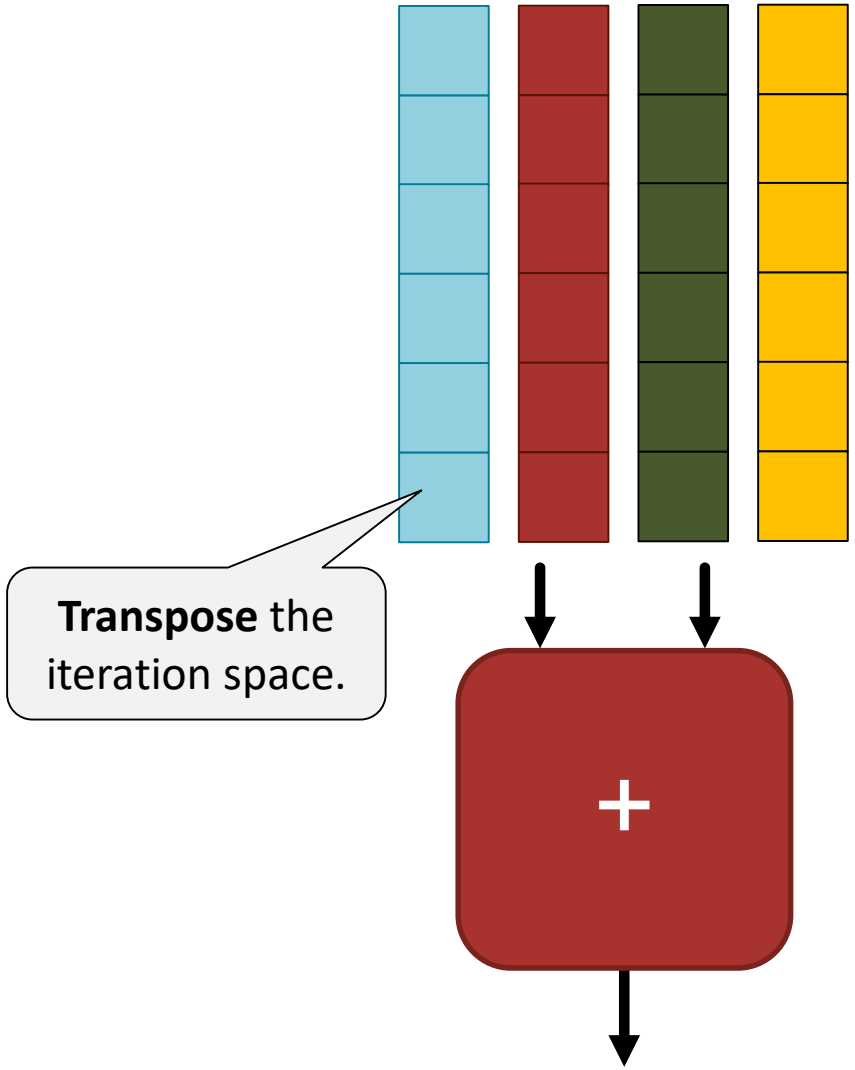
Solving loop-carried data dependencies




```
for (int i = 0; i < N; ++i) {
  float acc = 0;
  for (int j = 0; j < M; ++j) {
    acc += in.Pop();
  }
  out.Push(acc);
}
```

```
float acc[N];
for (int j = 0; j < M; ++j) {
  for (int i = 0; i < N; ++i) {
    acc[i] += in.Pop();
  }
}
for (int i = 0; i < N; ++i) {
  out.Push(acc[i]);
}
```

Solving loop-carried data dependencies

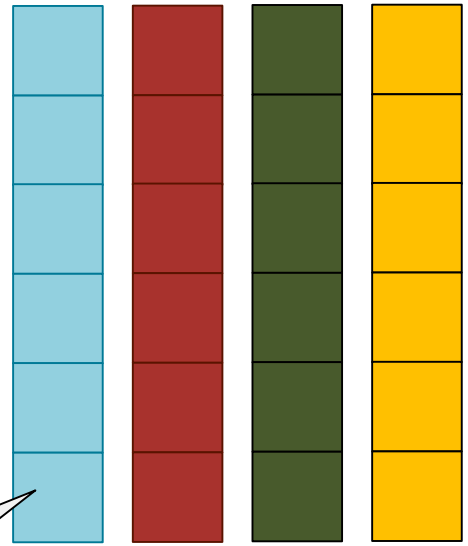



```
for (int i = 0; i < N; ++i) {
  float acc = 0;
  for (int j = 0; j < M; ++j) {
    acc += in.Pop();
  }
  out.Push(acc);
```

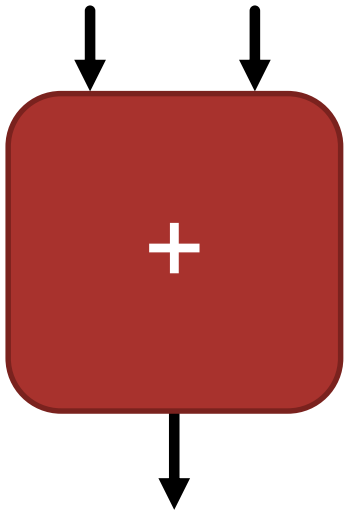
Comes at the cost of buffer space.

```
float acc[N];
for (int j = 0; j < M; ++j) {
  for (int i = 0; i < N; ++i) {
    acc[i] += in.Pop();
  }
}
for (int i = 0; i < N; ++i) {
  out.Push(acc[i]);
}
```

Solving loop-carried data dependencies



Transpose the iteration space.




```
for (int i = 0; i < N; ++i) {
  float acc = 0;
  for (int j = 0; j < M; ++j) {
    acc += in.Pop();
  }
  out.Push(acc);
```

Comes at the cost of buffer space.

```
float acc[N];
for (int j = 0; j < M; ++j) {
  for (int i = 0; i < N; ++i) {
    acc[i] += in.Pop();
  }
}
for (int i = 0; i < N; ++i) {
  out.Push(acc[i]);
}
```

Only needs to be larger than the latency

Locality in the program

```
for (int n = 0; n < N; ++n) {
  float acc[P];

  for (int k = 0; k < K; ++k) {
    const auto a = A[n*K + k];

    for (int m = 0; m < M; ++m) {
      #pragma HLS PIPELINE II=1
      const float prev = (k == 0) ? 0 : acc[m];
      acc[m] = prev + a * B[k*M + m];
    }
  }
  // ...
}
```

Locality in the program

```
for (int n = 0; n < N; ++n) {
  float acc[P];

  for (int k = 0; k < K; ++k) {
    const auto a = A[n*K + k];

    for (int m = 0; m < M; ++m) {
      #pragma HLS PIPELINE II=1
      const float prev = (k == 0) ? 0 : acc[m];
      acc[m] = prev + a * B[k*M + m];
    }
  }
  // ...
}
```

Spatial locality: Vectorizable.

Locality in the program

```
for (int n = 0; n < N; ++n) {
  float acc[P];

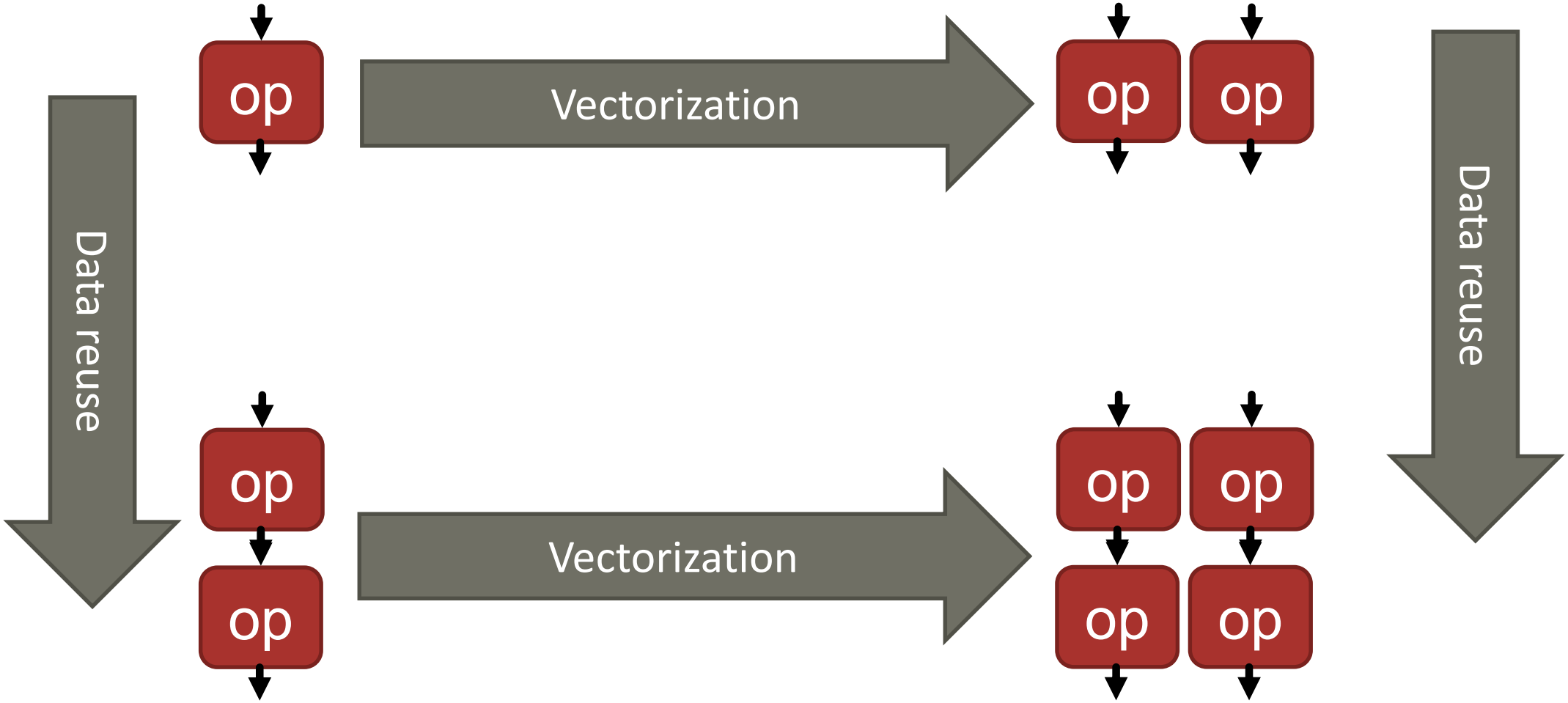
  for (int k = 0; k < K; ++k) {
    const auto a = A[n*K + k];

    for (int m = 0; m < M; ++m) {
      #pragma HLS PIPELINE II=1
      const float prev = (k == 0) ? 0 : acc[m];
      acc[m] = prev + a * B[k*M + m];
    }
  }
  // ...
}
```

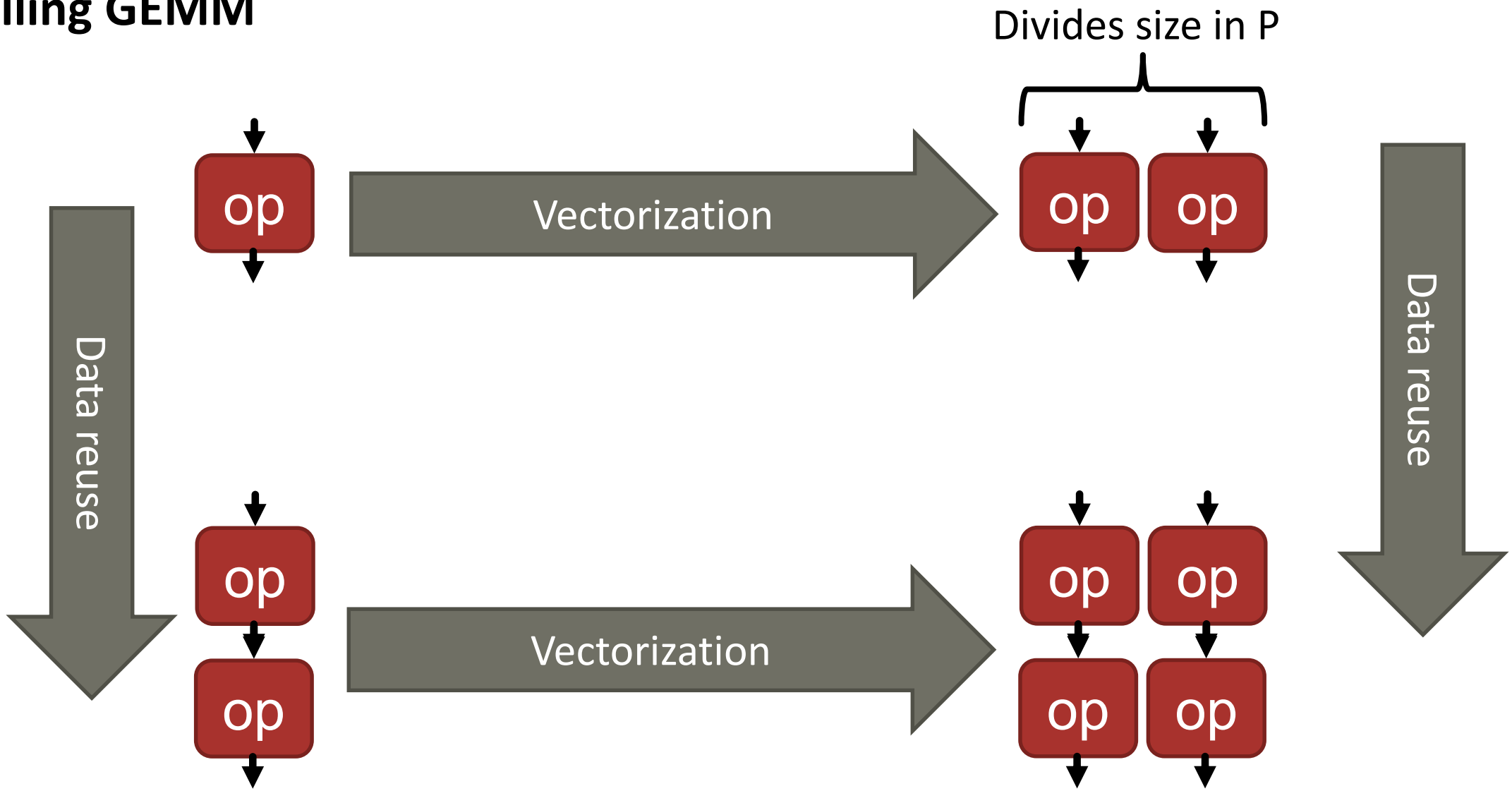
Temporal locality: Reused P times. Load more of these and tile N!

Spatial locality: Vectorizable.

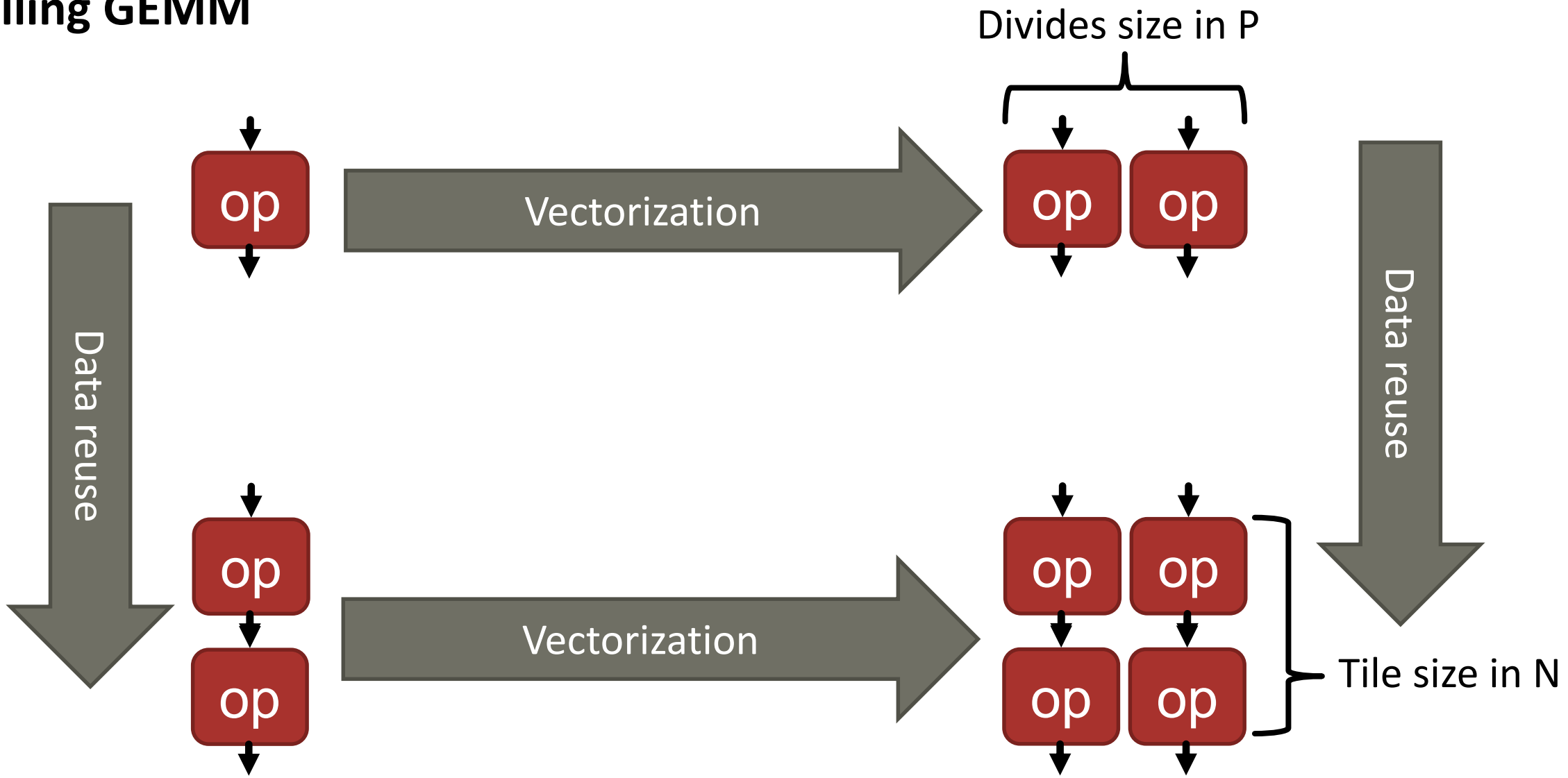
Unrolling GEMM



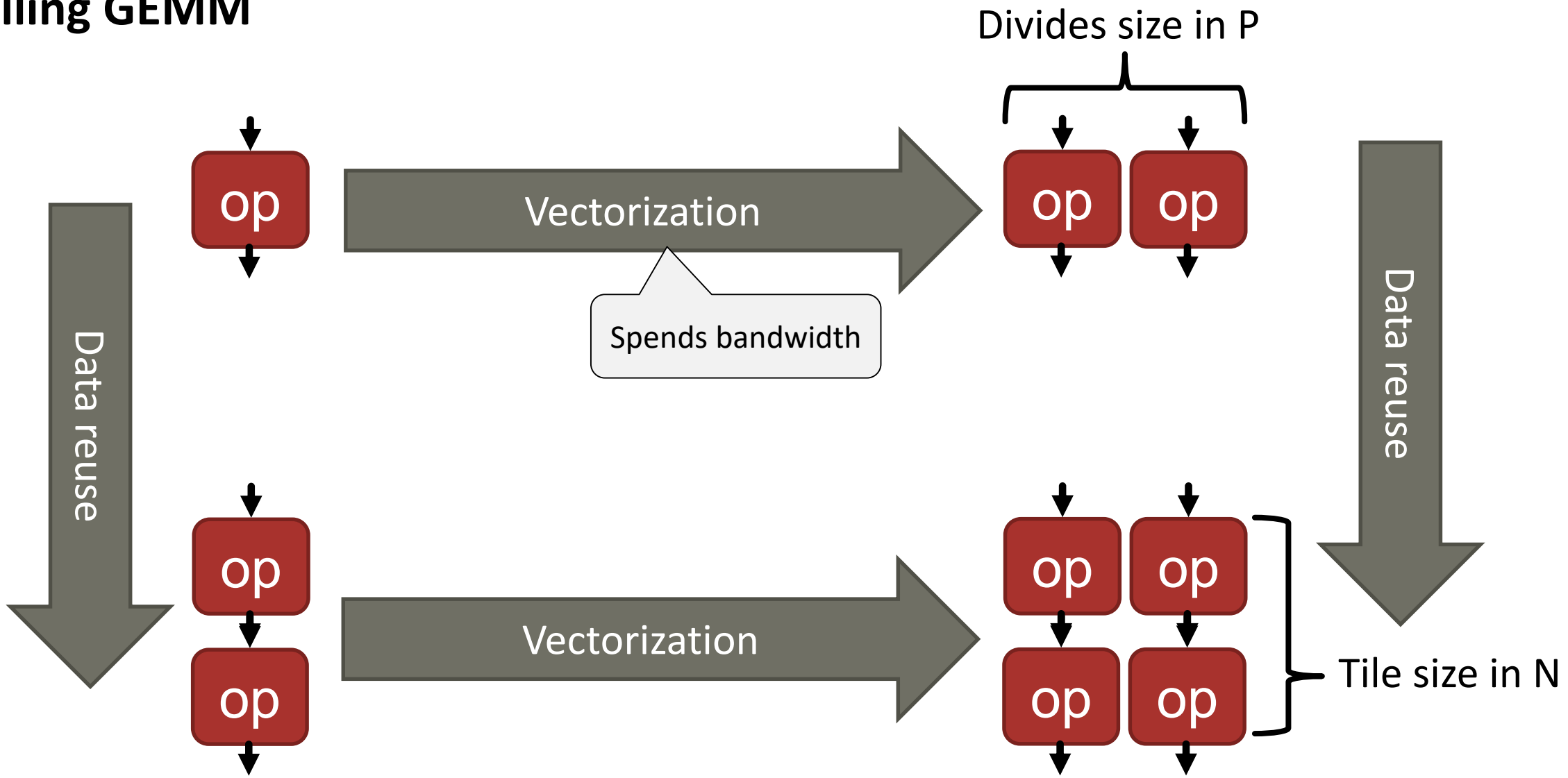
Unrolling GEMM



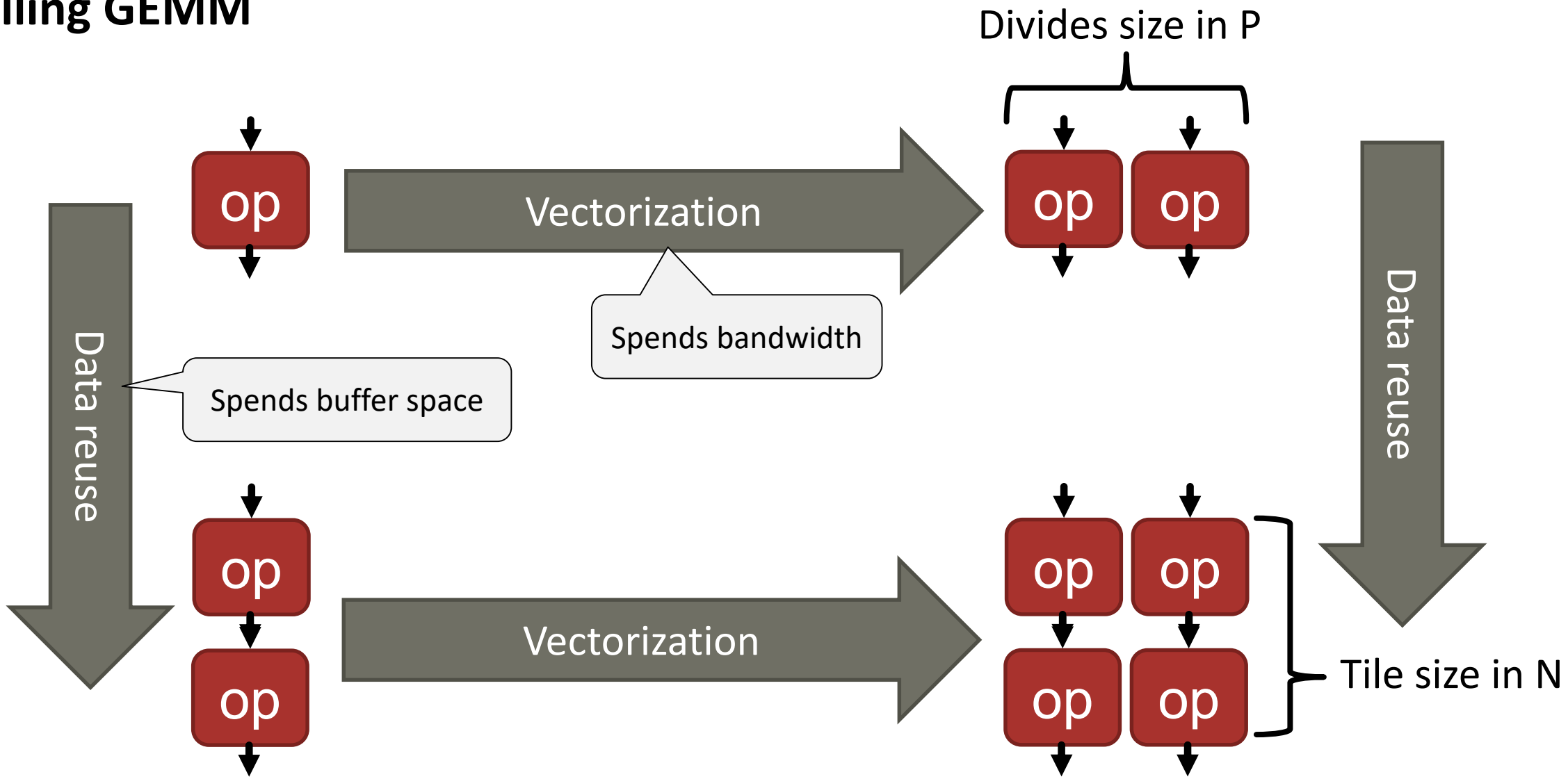
Unrolling GEMM



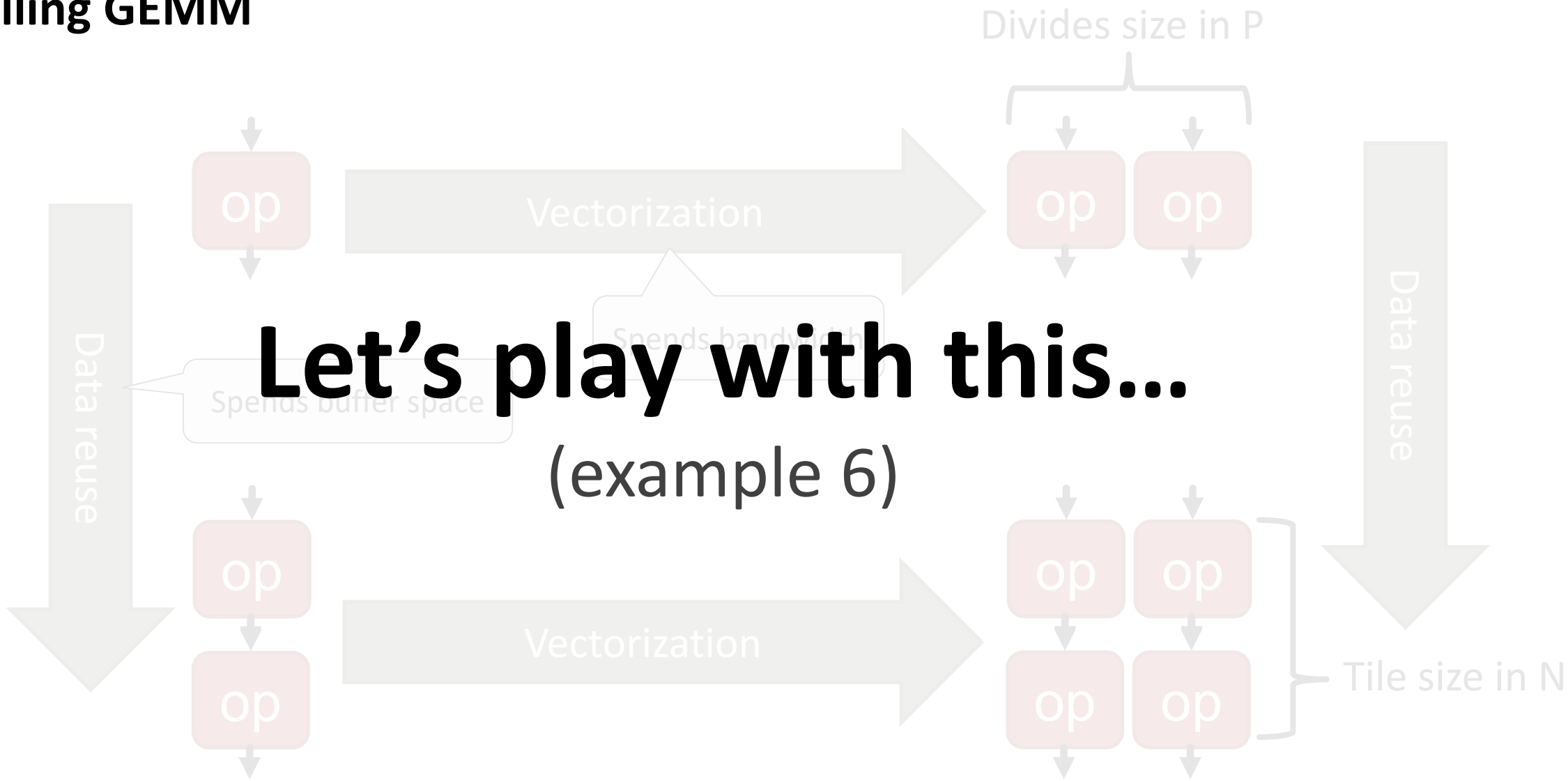
Unrolling GEMM



Unrolling GEMM



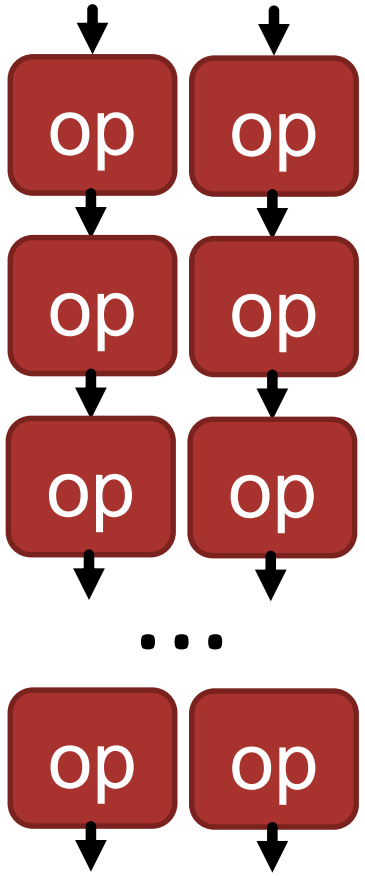
Unrolling GEMM



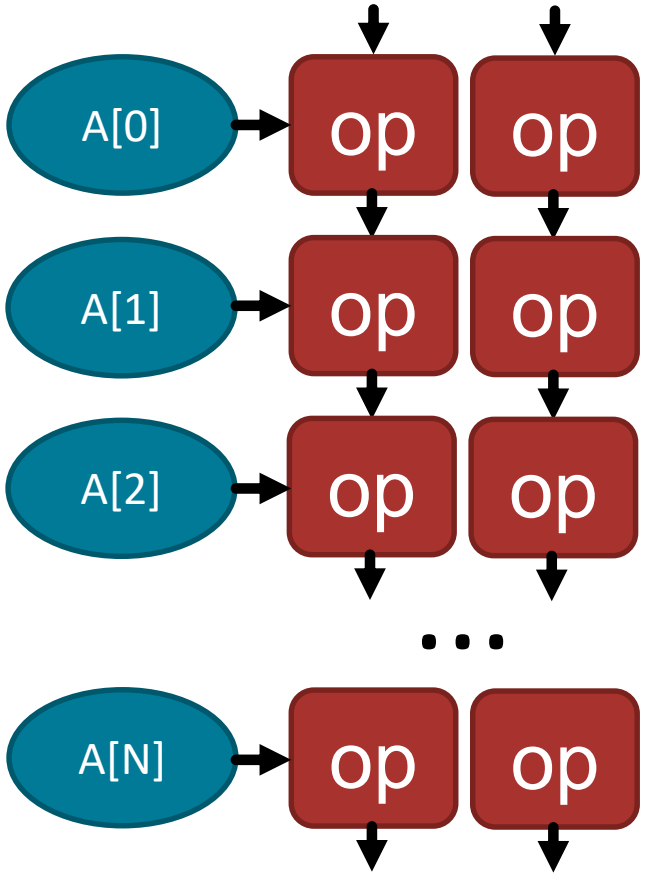
Let’s play with this…

(example 6)

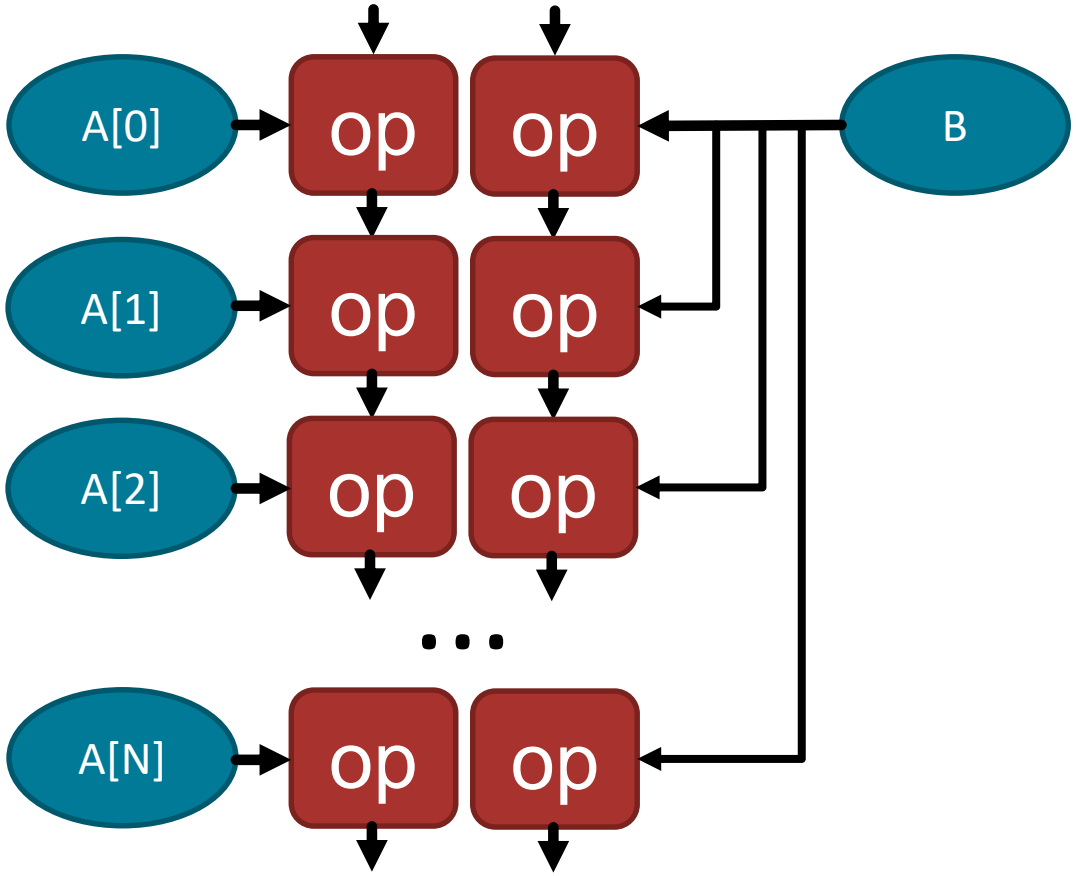
Fanout issue



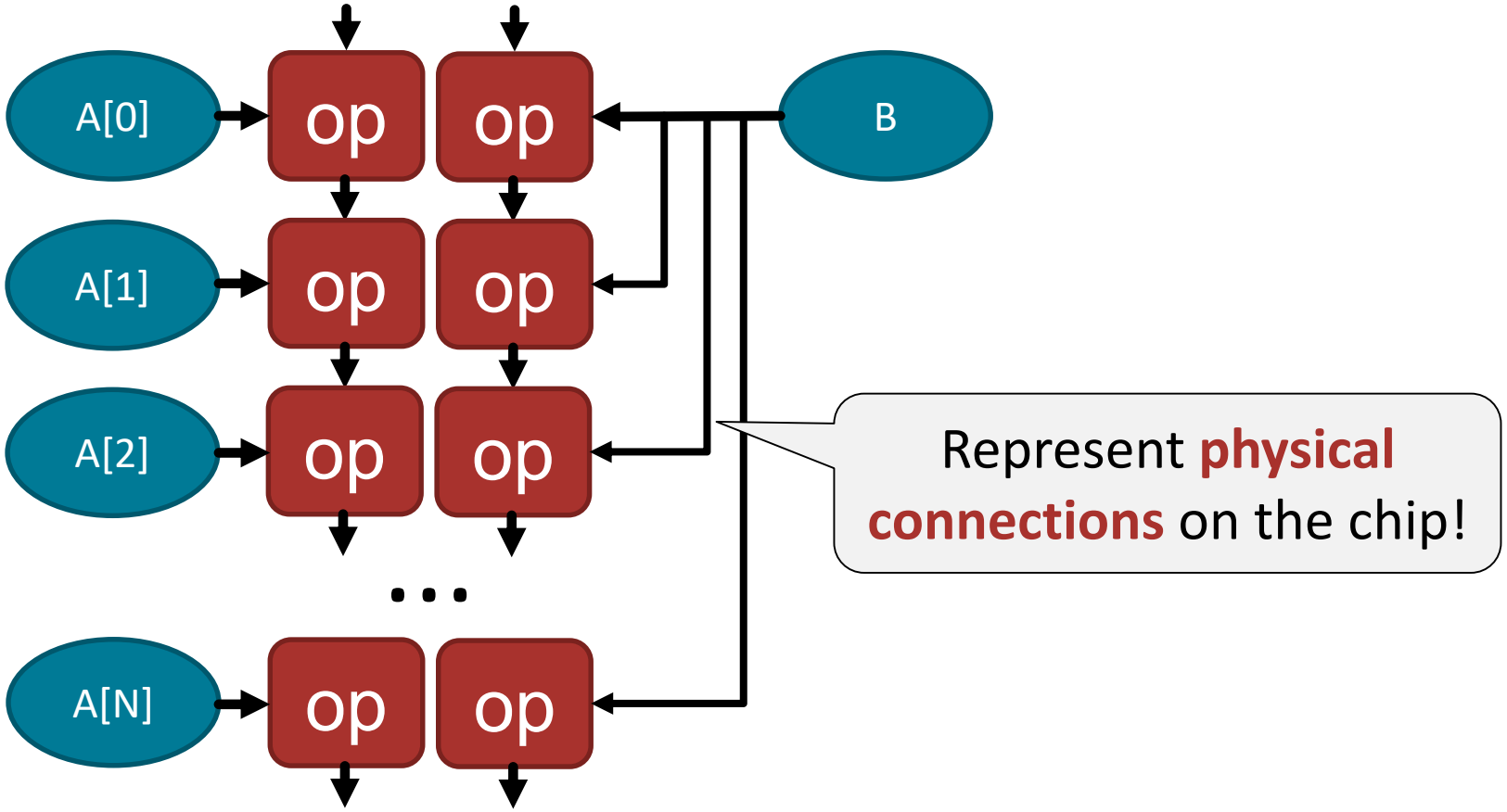
Fanout issue



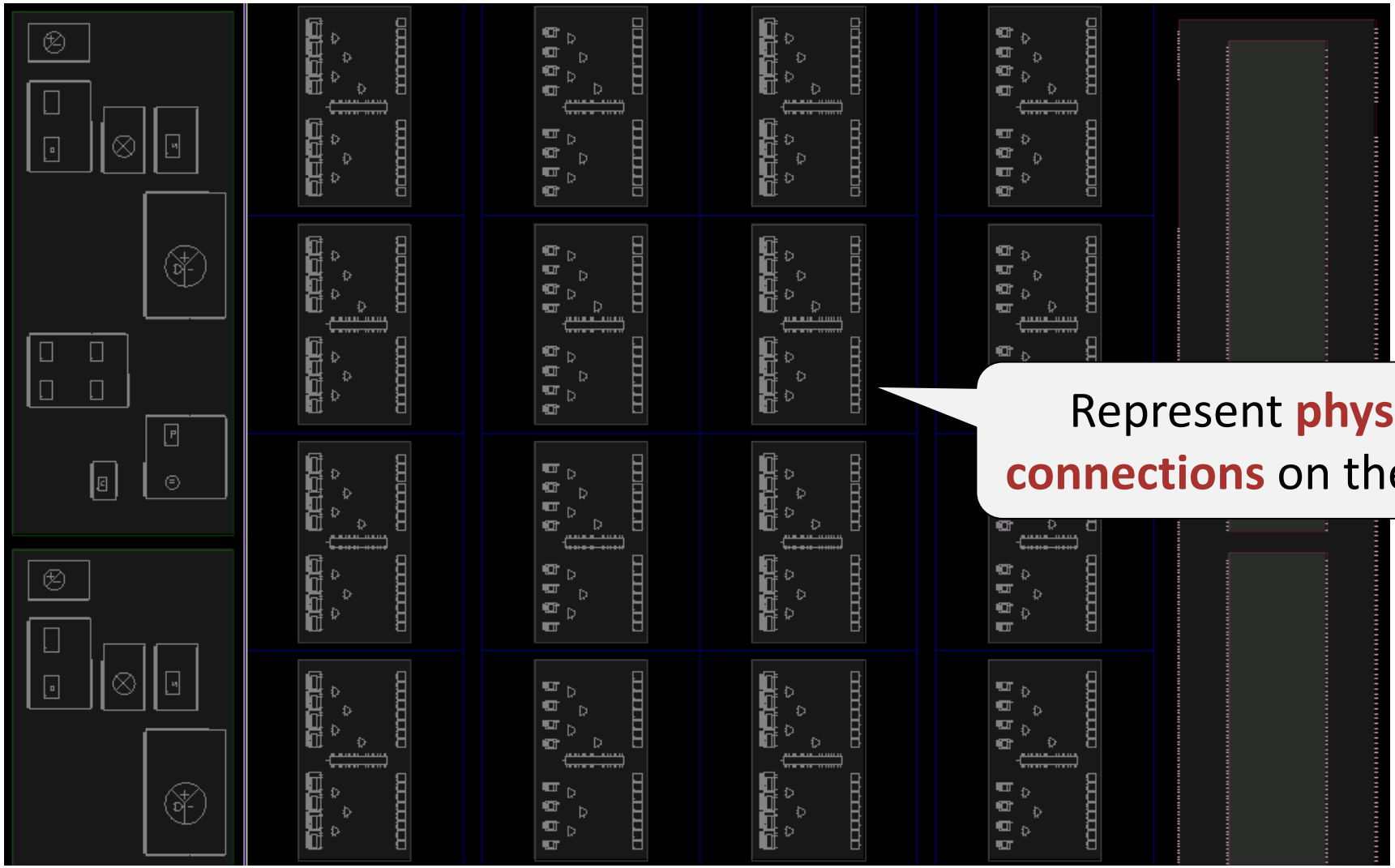
Fanout issue



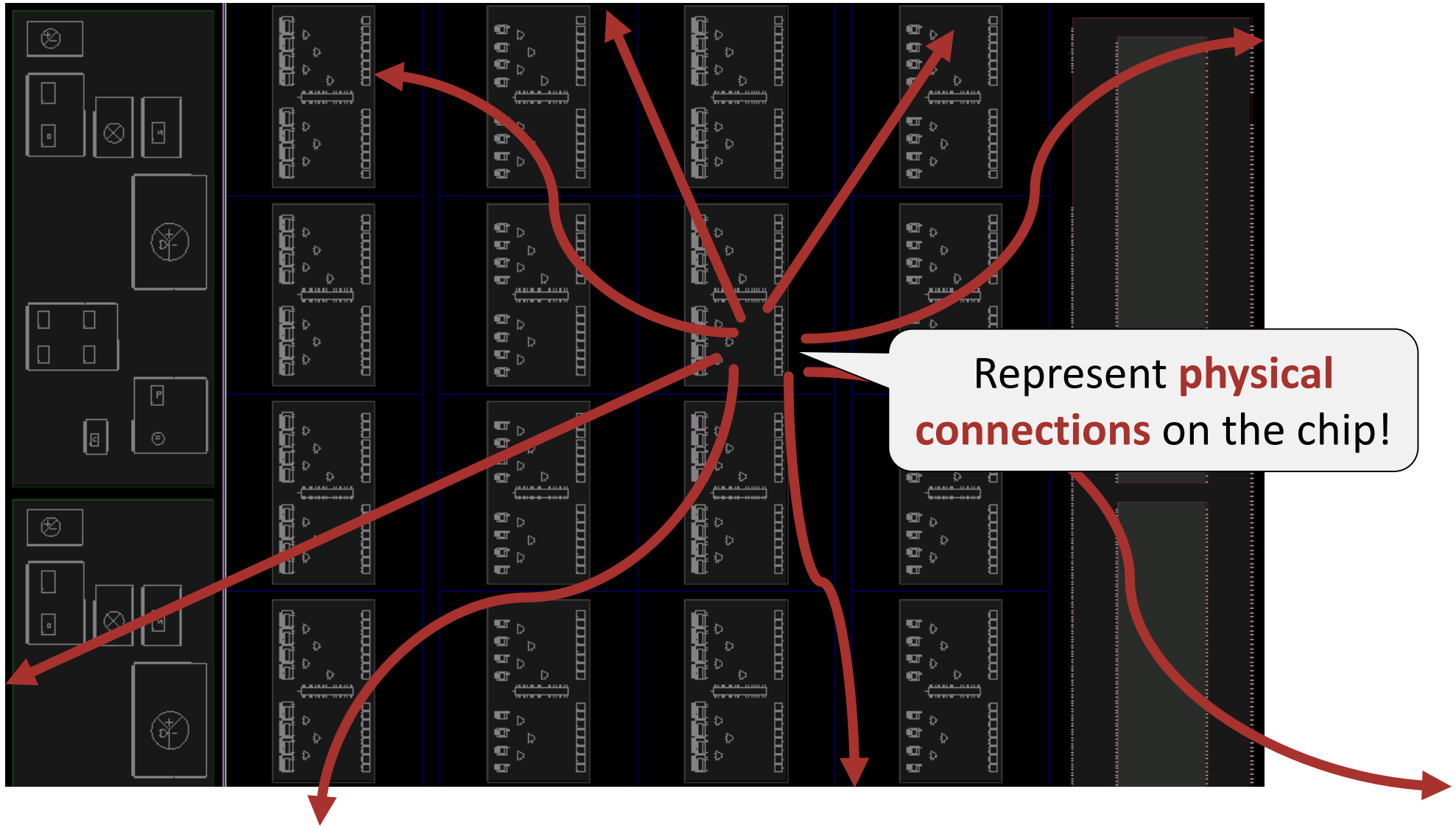
Fanout issue



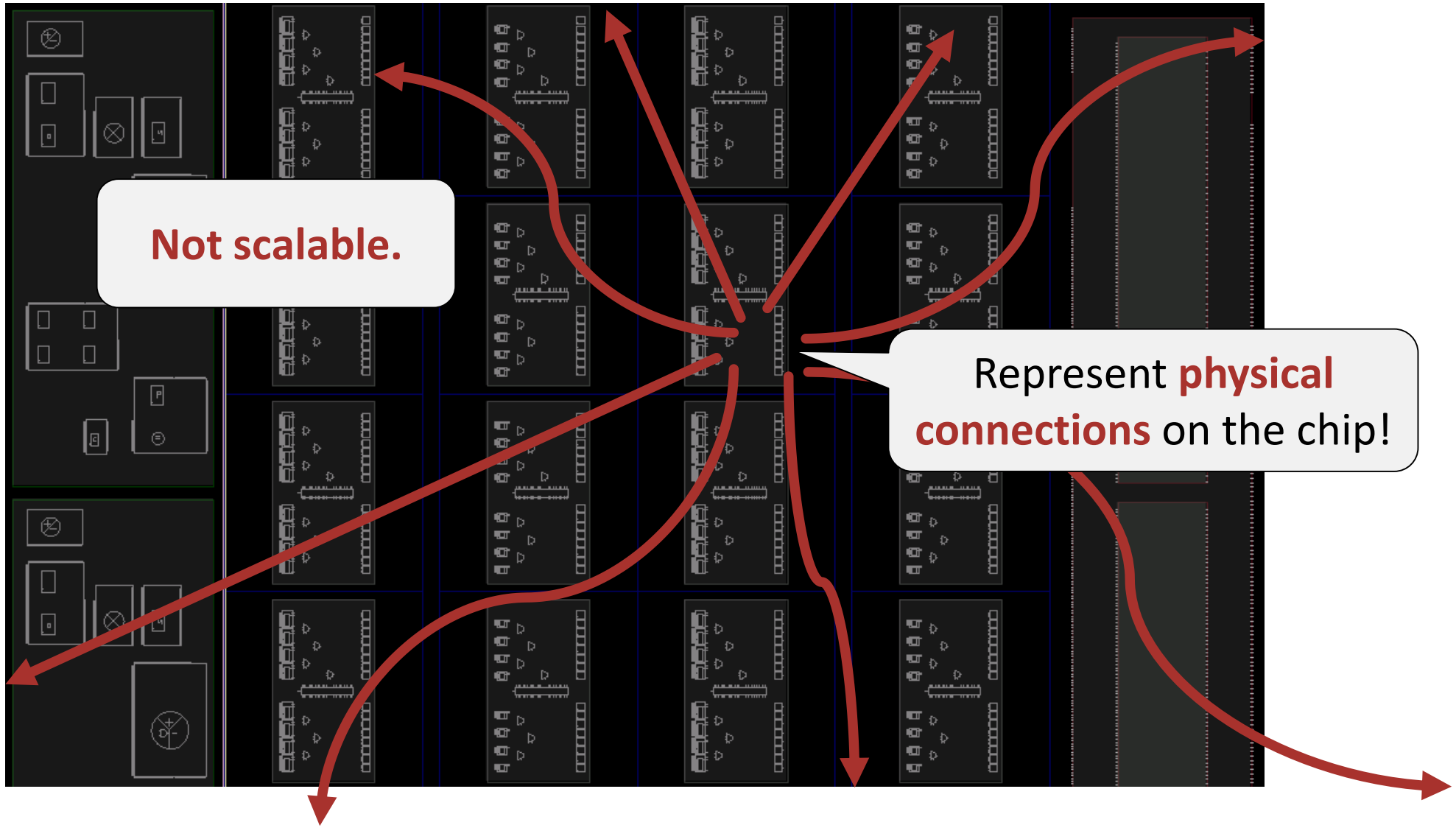
Fanout issue



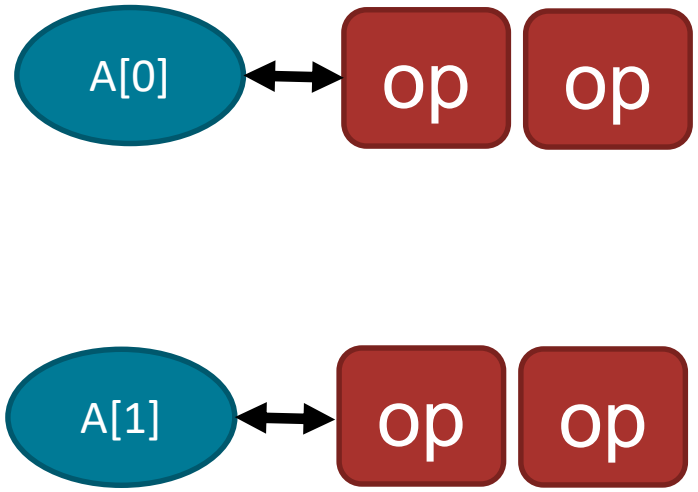
Fanout issue



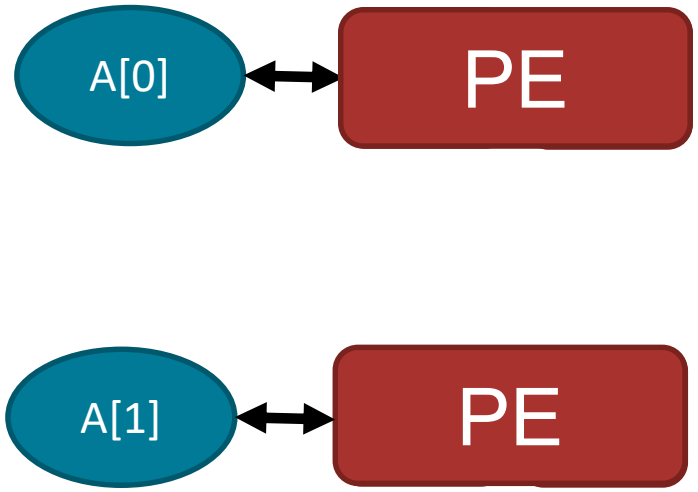
Fanout issue



Breaking into processing elements



Breaking into processing elements



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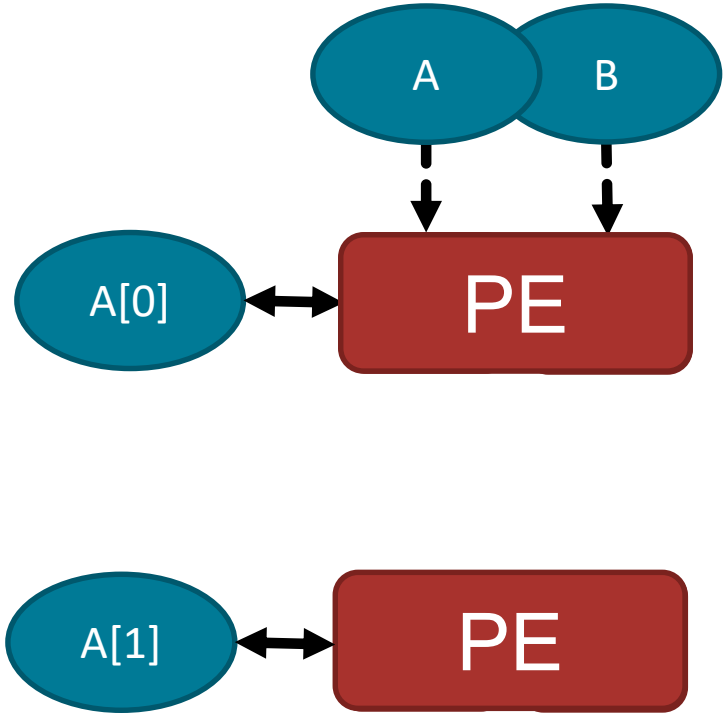

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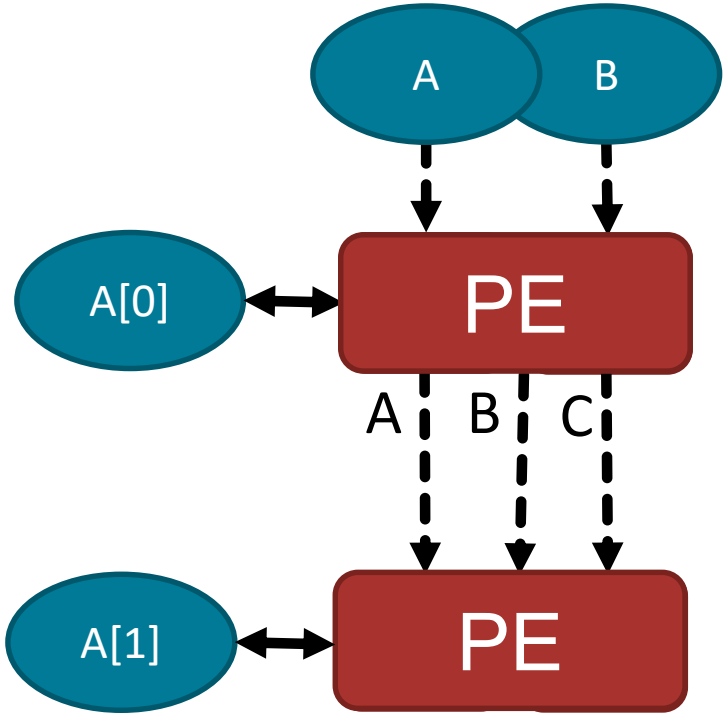

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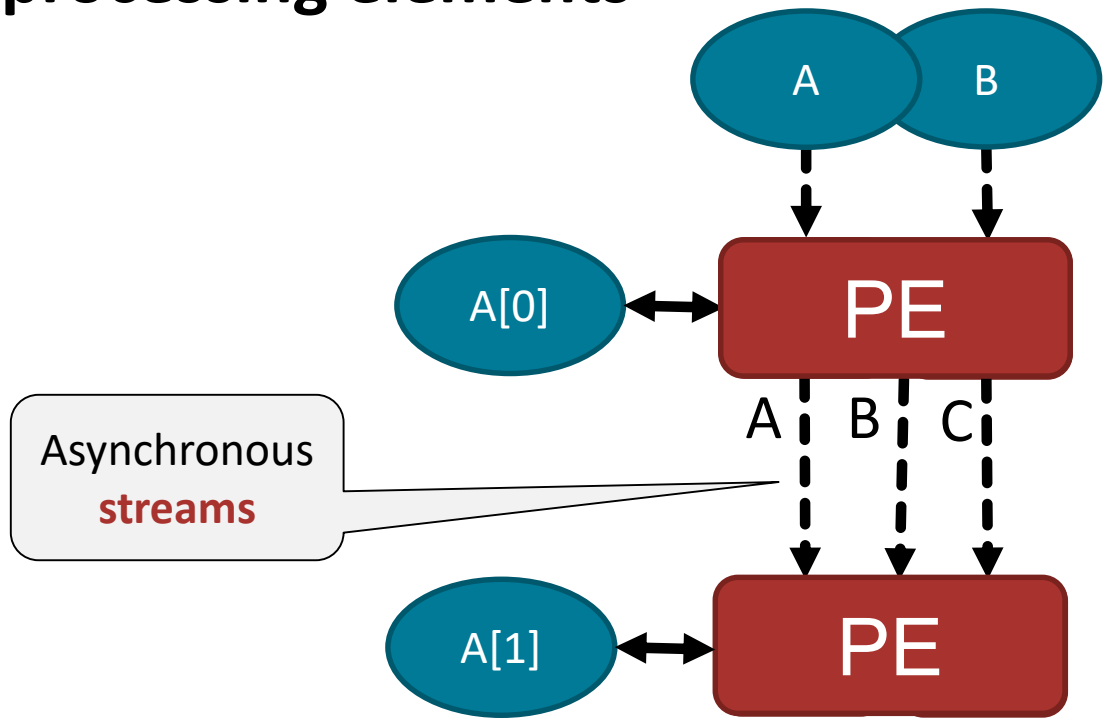

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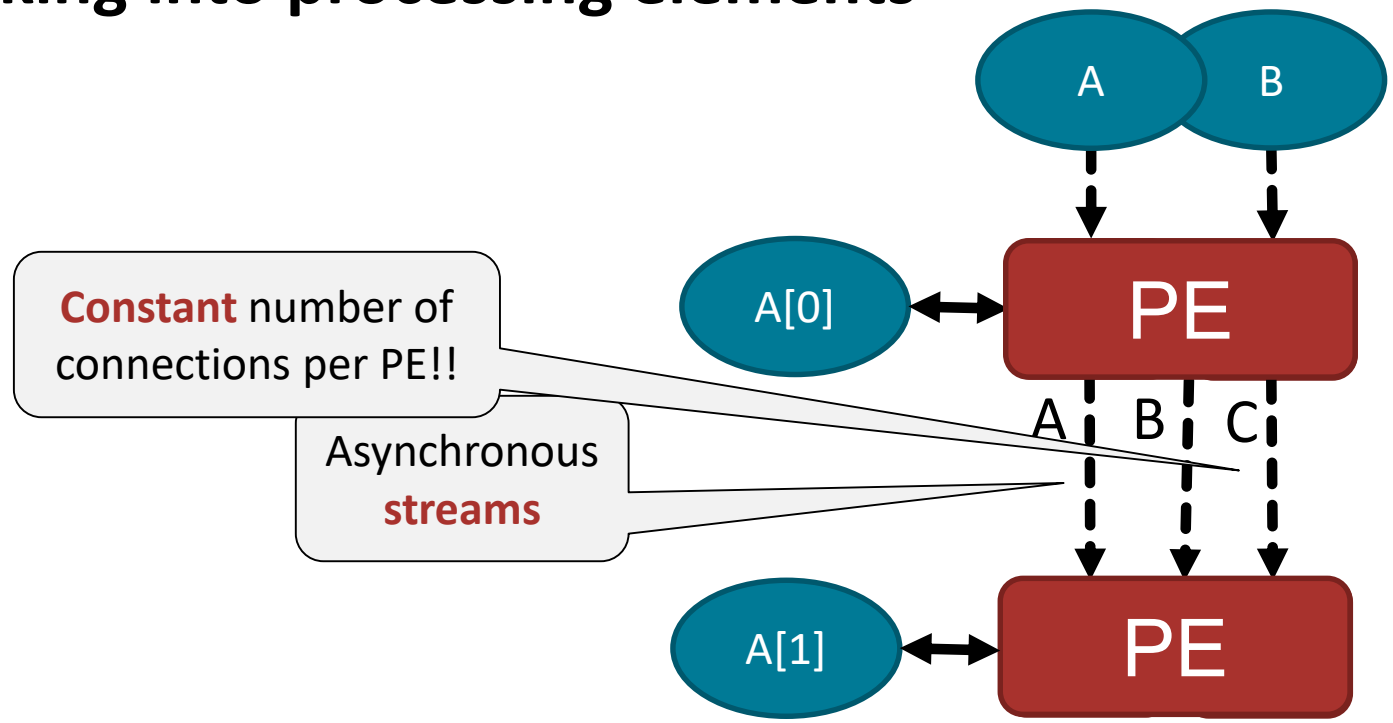
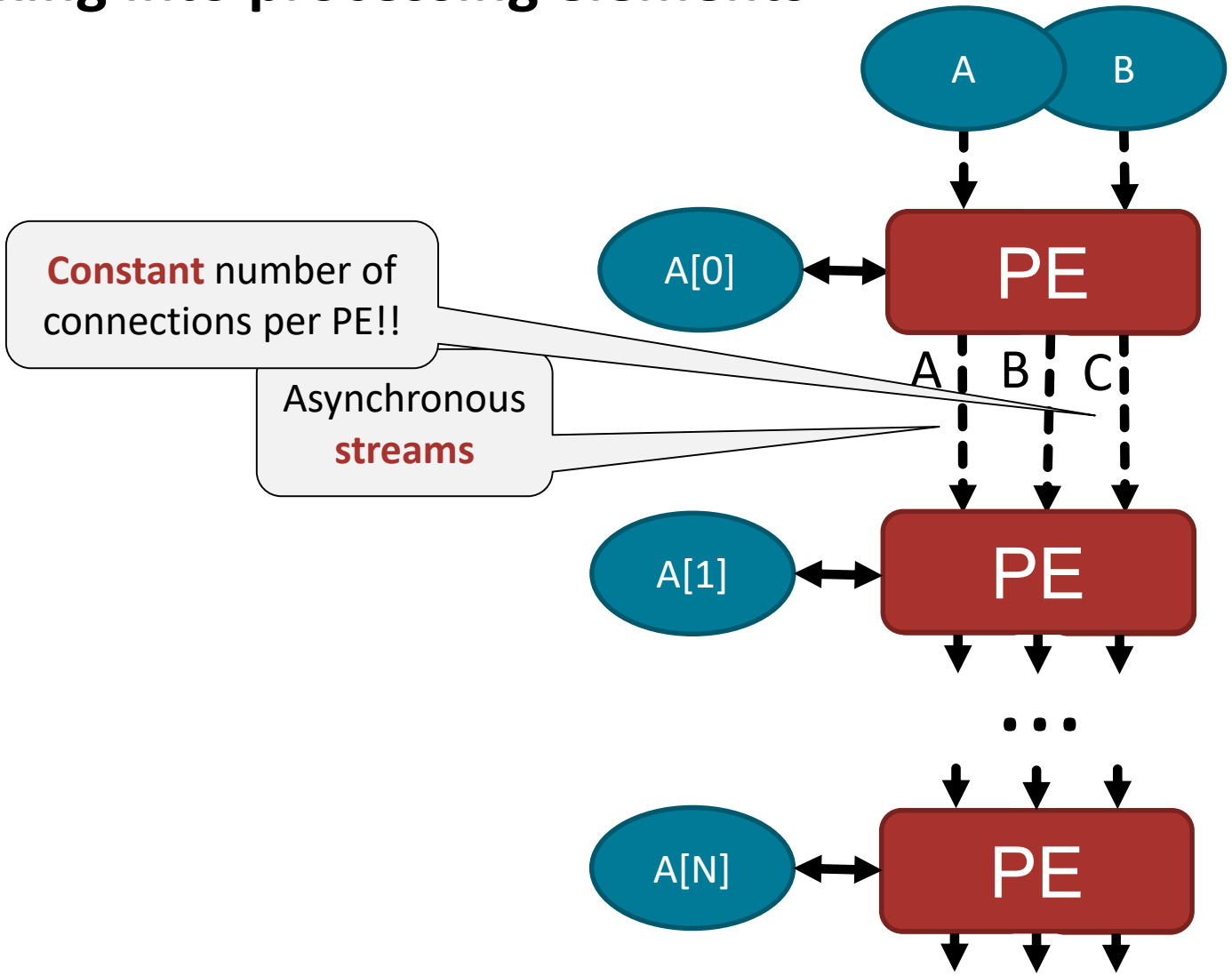


Breaking into processing elements



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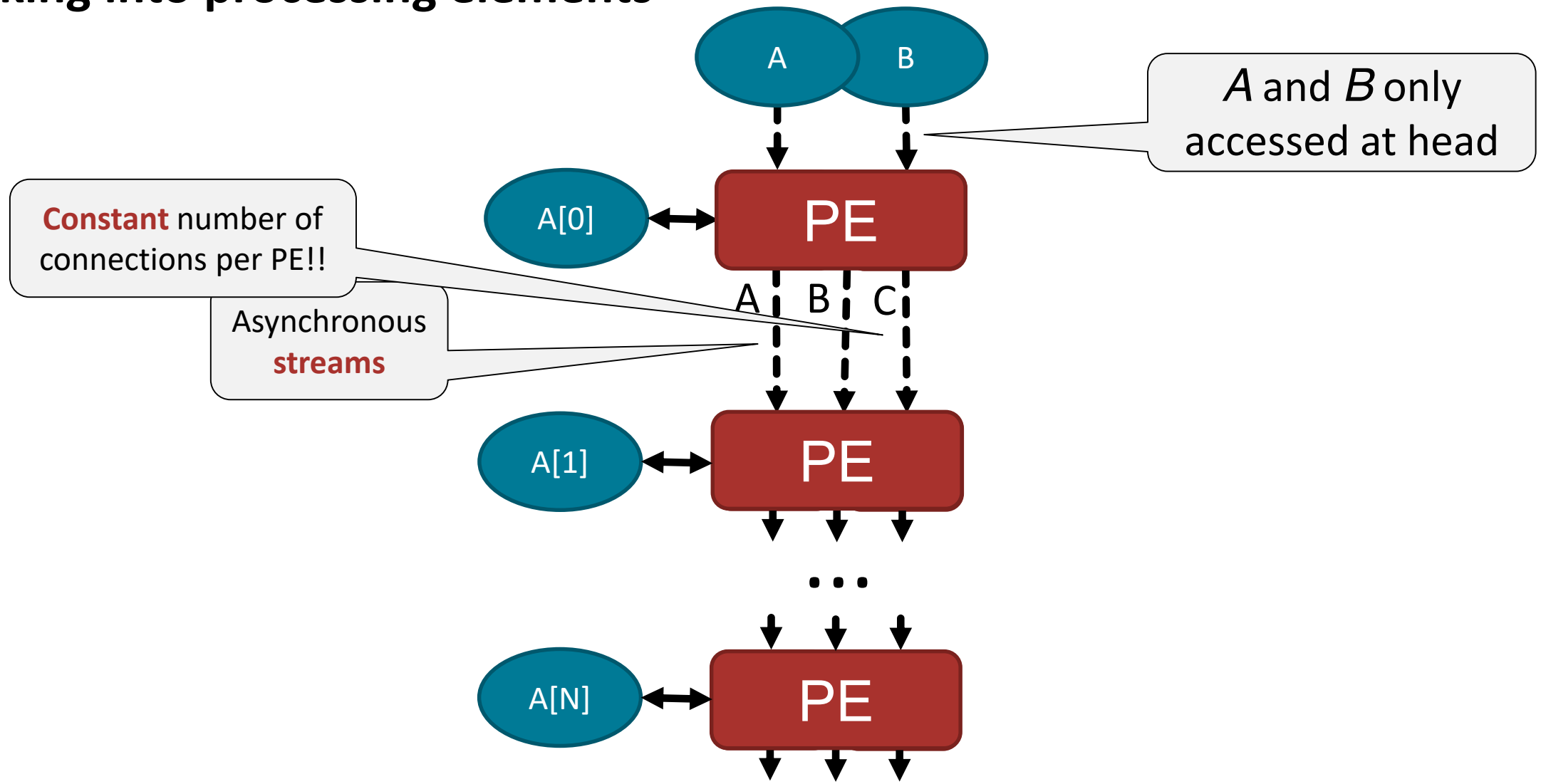

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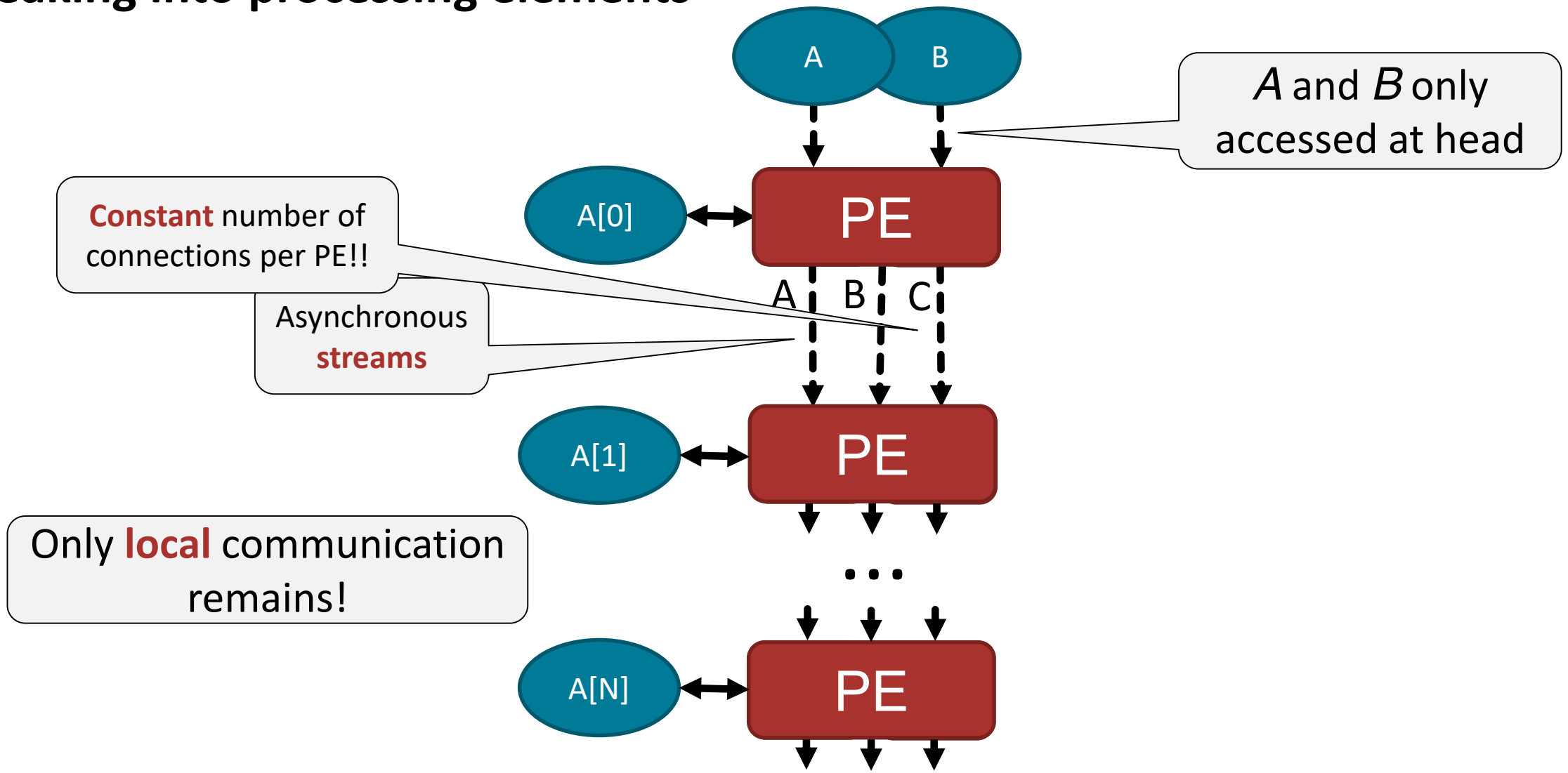
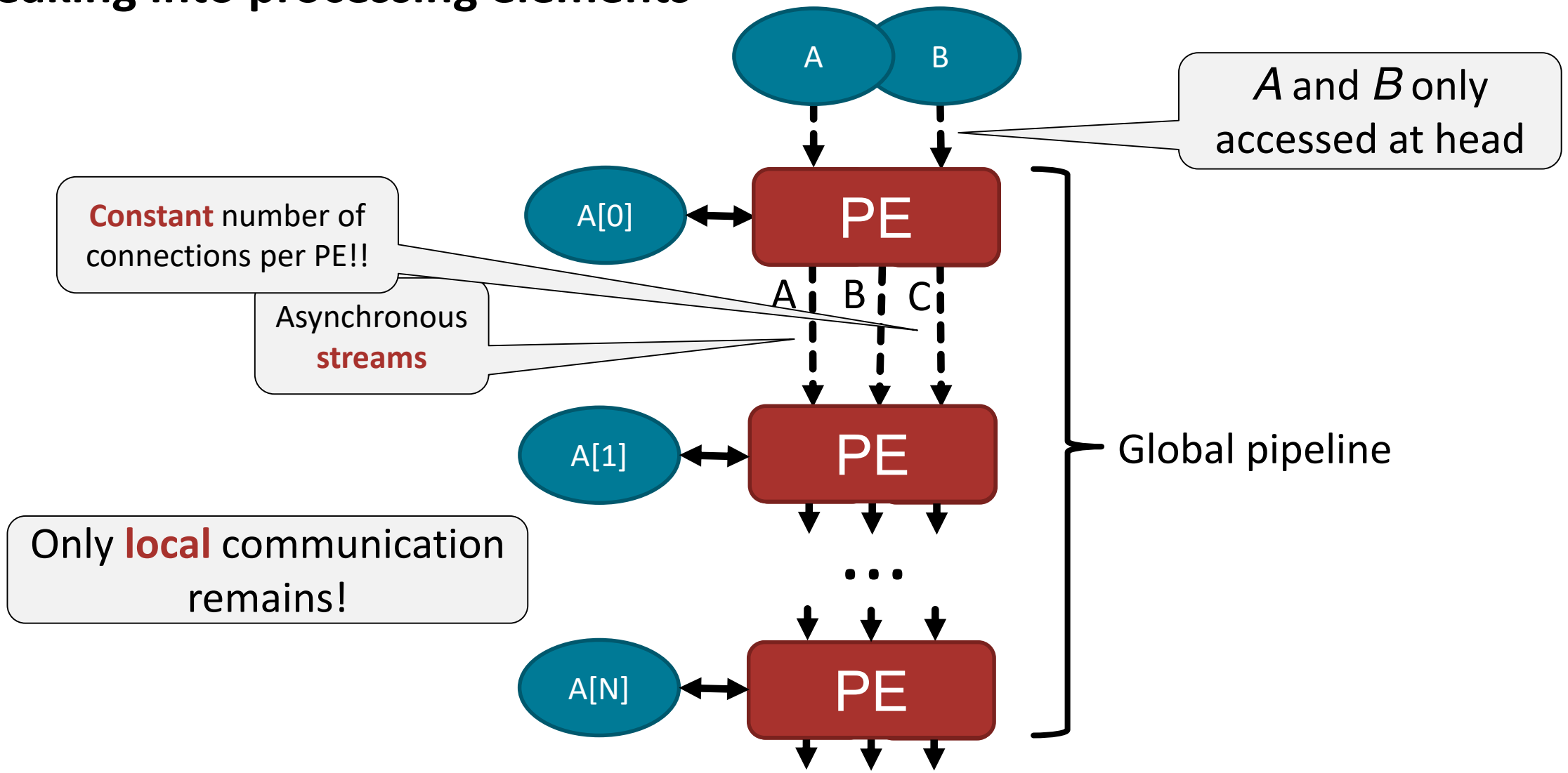
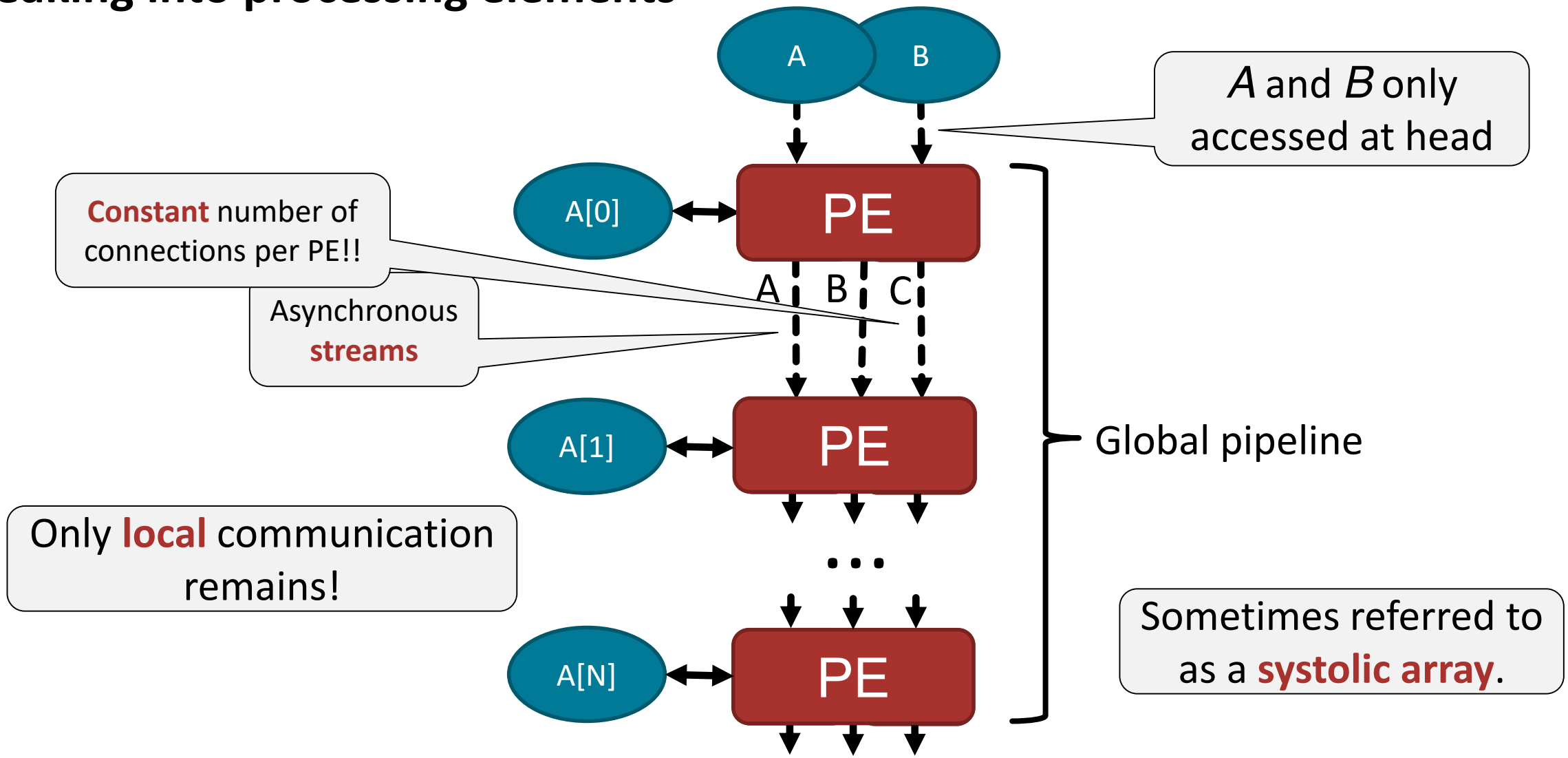


Breaking into processing elements



Breaking into processing elements



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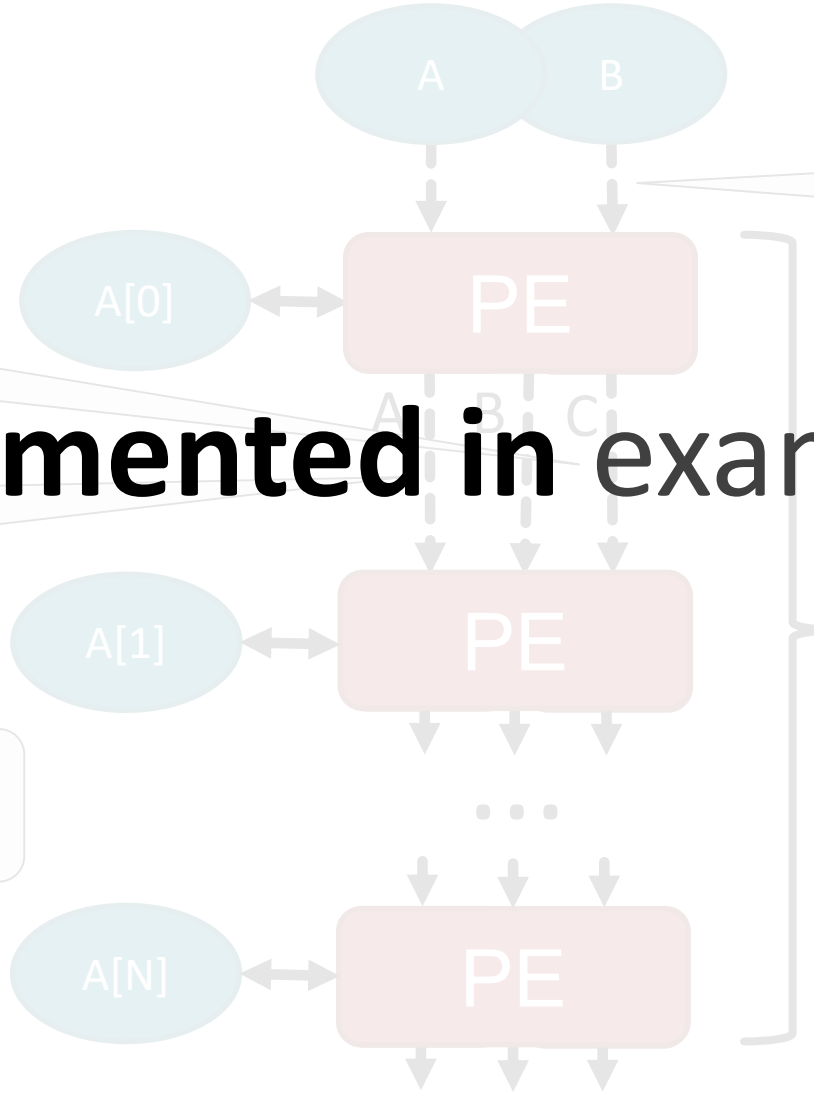


A and *B* only accessed at head

Constant number of connections per PE!!

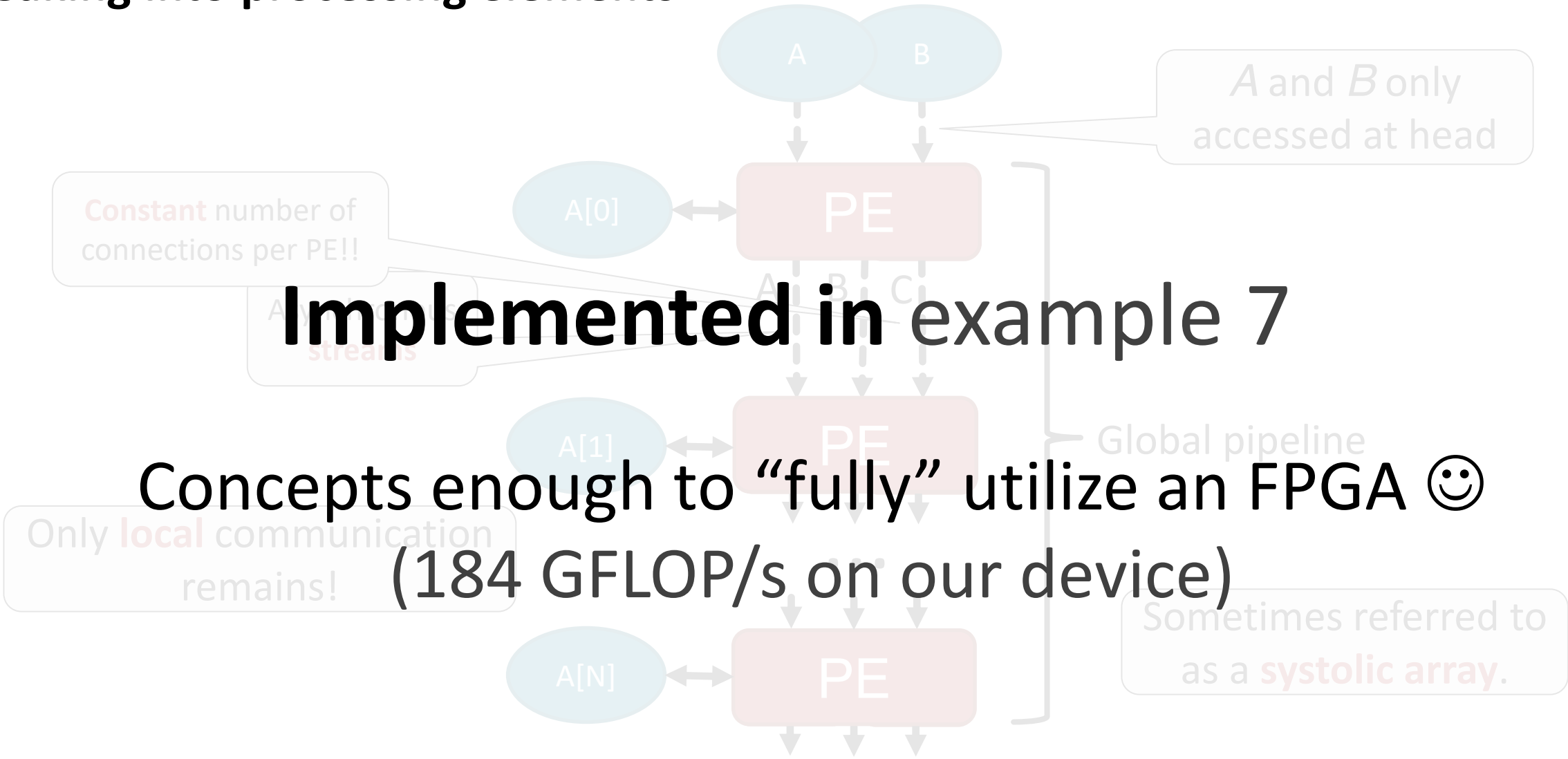
Only **local** communication remains!

Global pipeline

Sometimes referred to as a **systolic array**.

Implemented in example 7

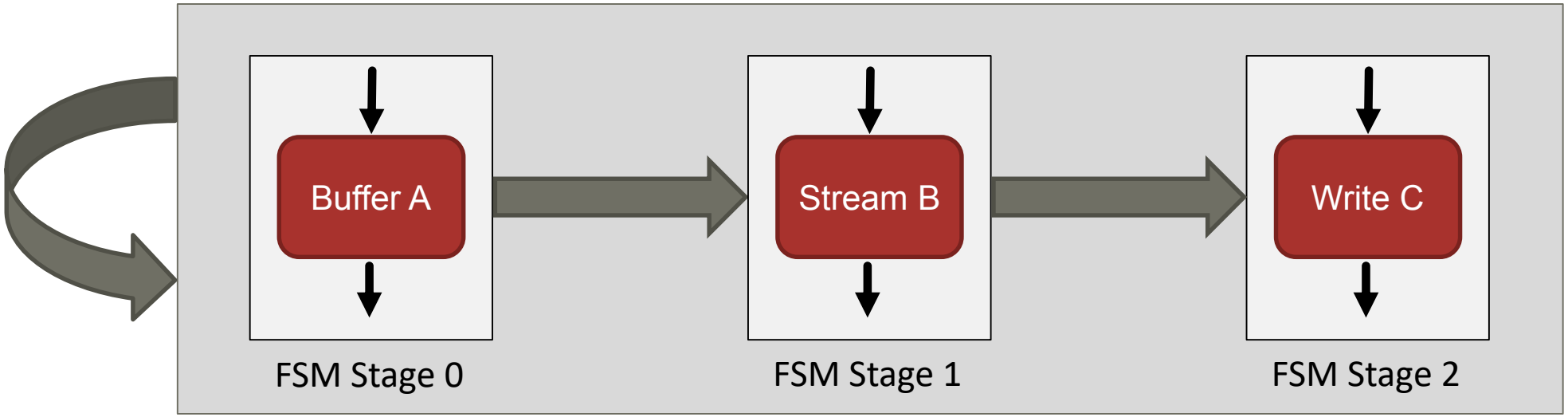
Breaking into processing elements



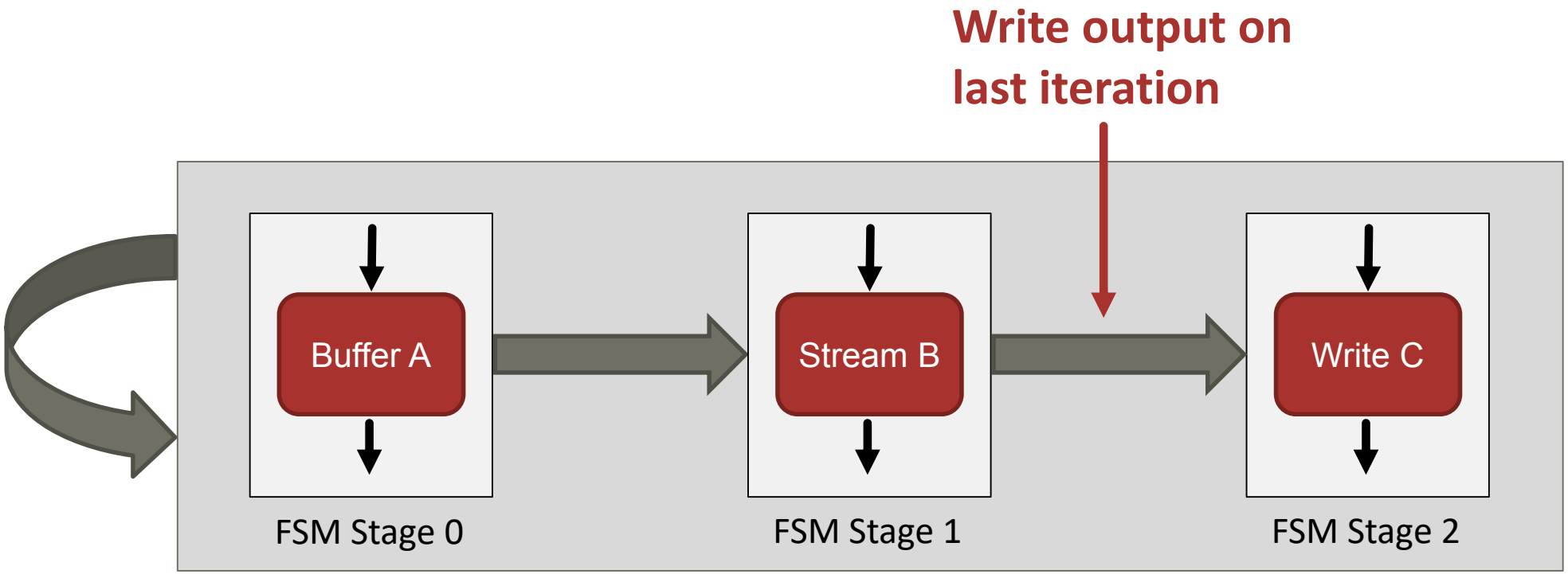
Implemented in example 7

Concepts enough to “fully” utilize an FPGA ☺
(184 GFLOP/s on our device)

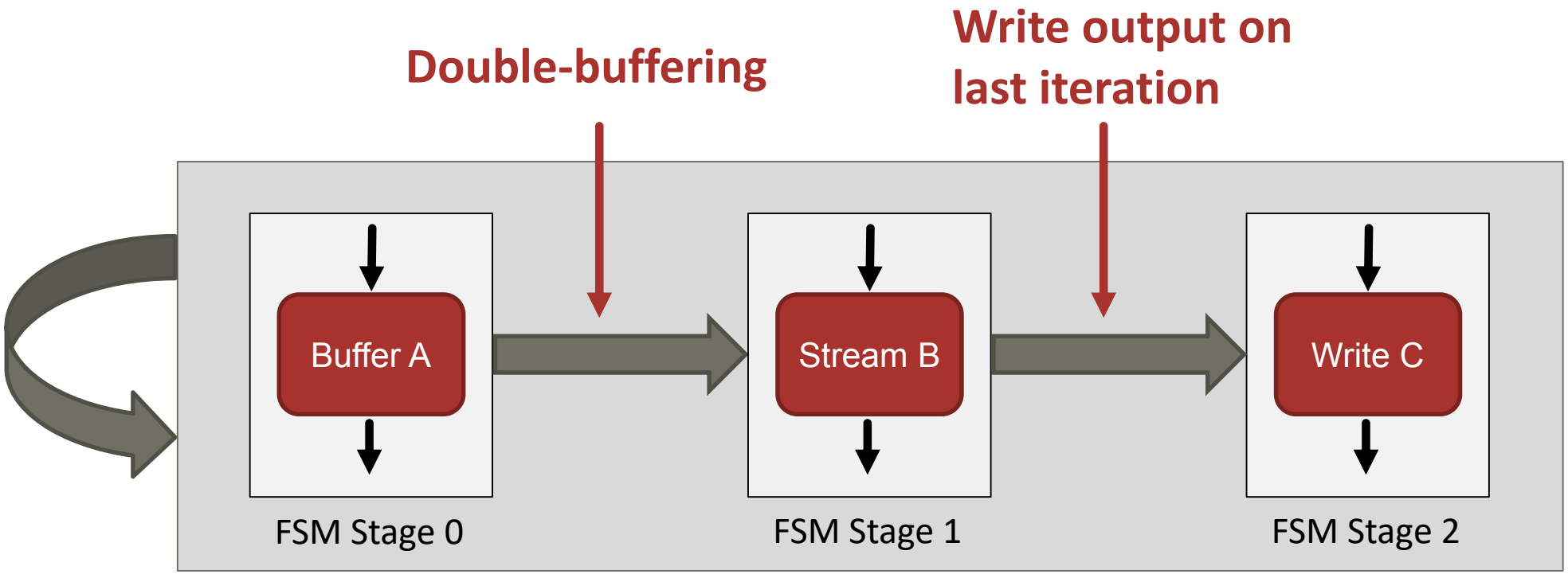
Remaining optimization potential



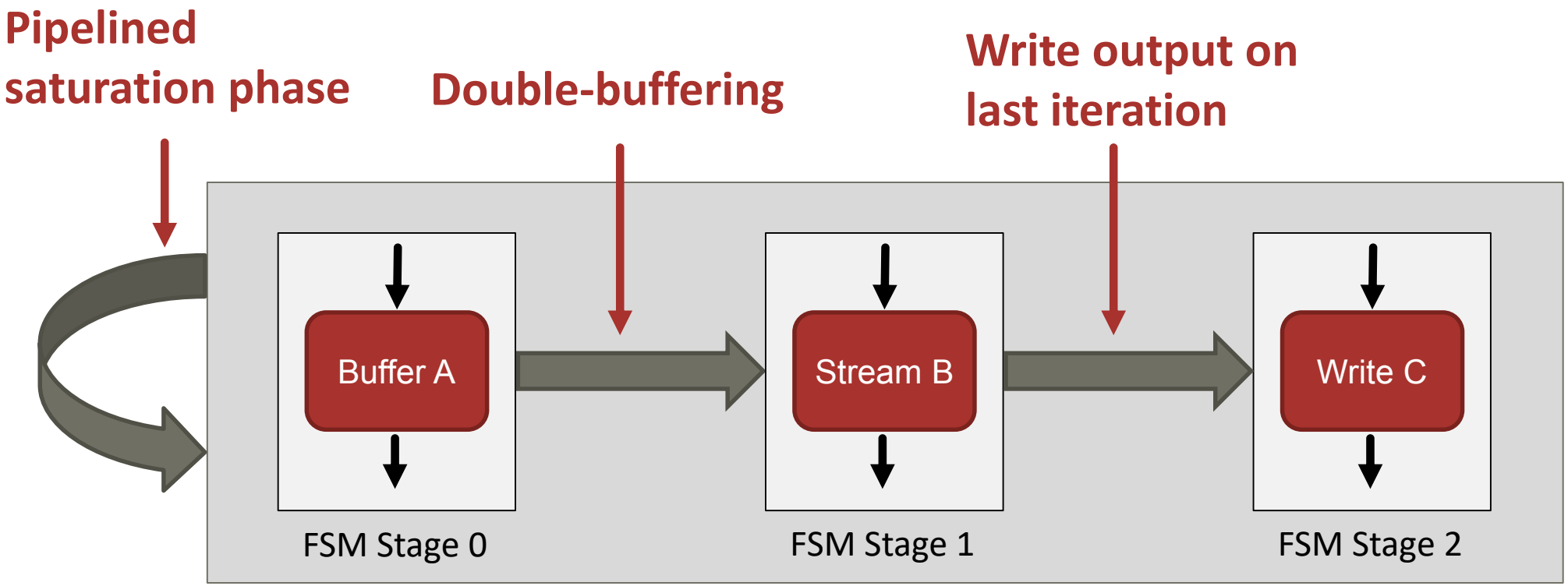
Remaining optimization potential



Remaining optimization potential



Remaining optimization potential



Summary

Challenge: Pipeline throughput (initiation interval) is limited by hardware interfaces.

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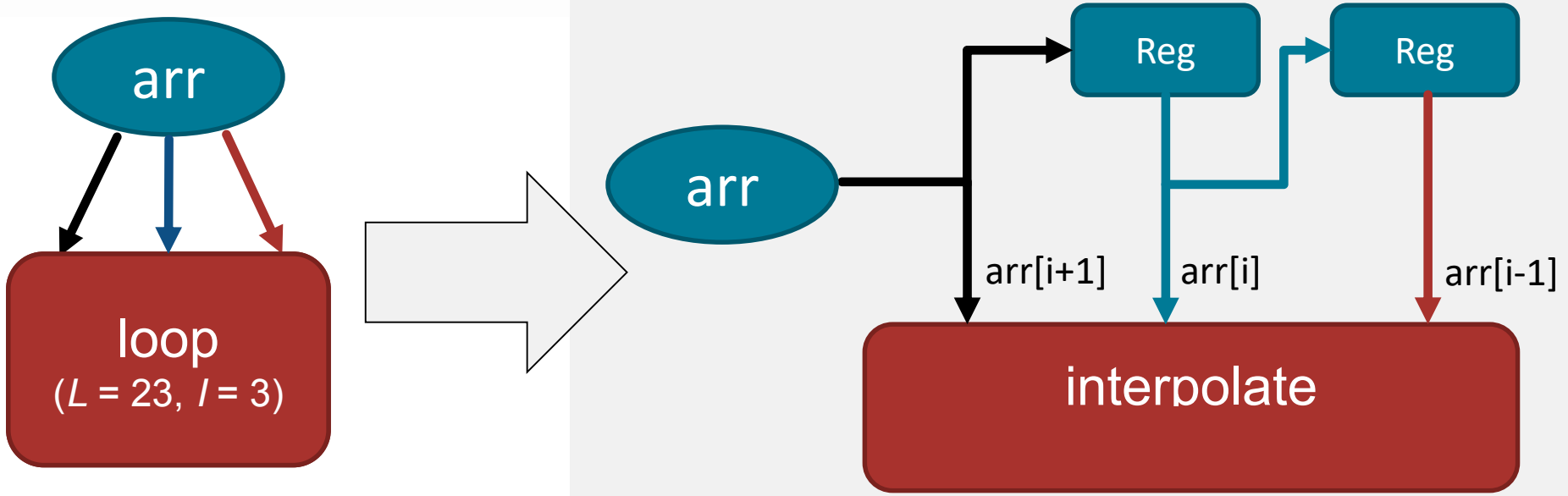

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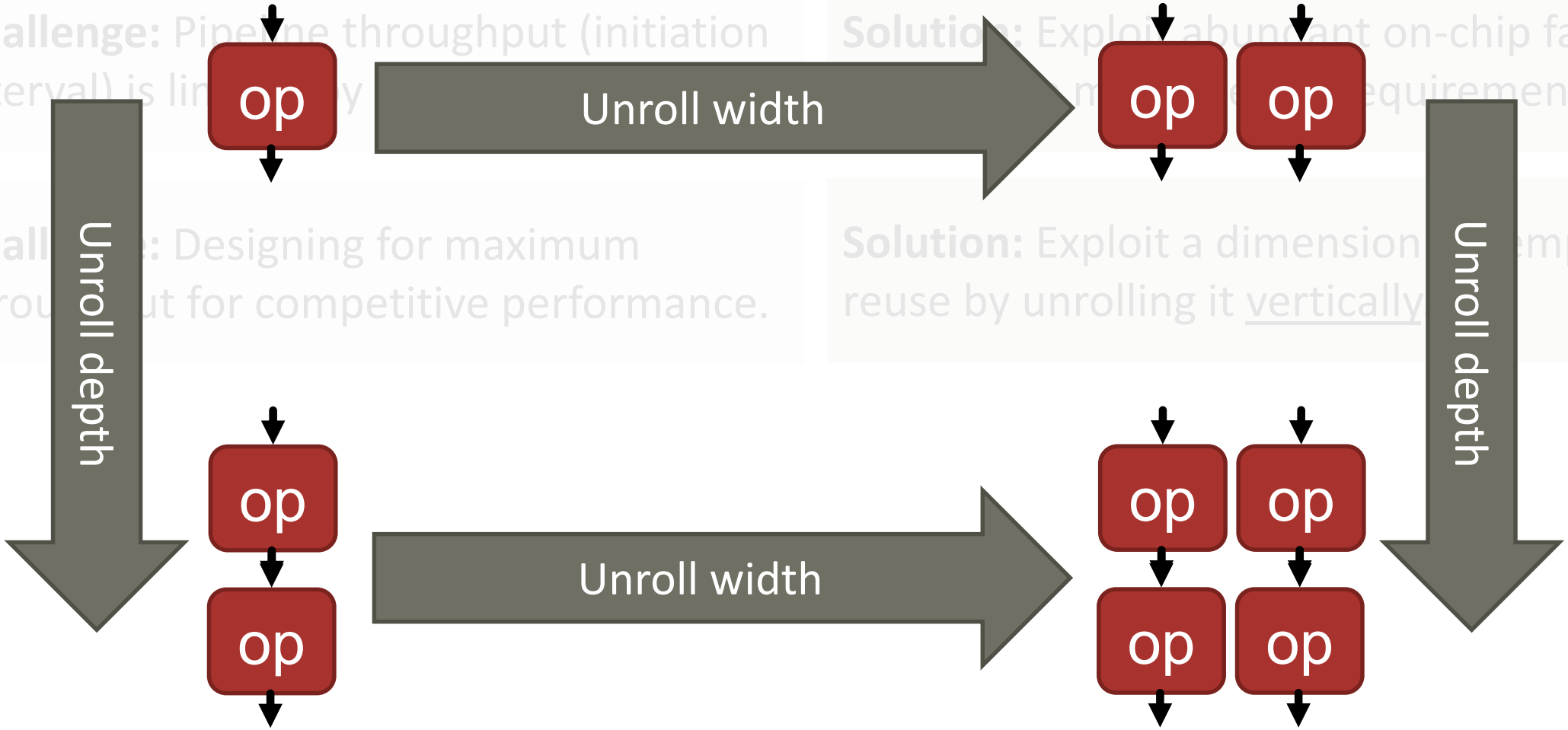
Solution: Exploit a dimension of temporal reuse by unrolling it vertically.

Summary


op
Unroll width
op
op
Unroll depth
op
op
Unroll width
op
op
op
op
Unroll depth

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Challenge: Loop-carried dependencies cause pipeline stalls that kill performance.

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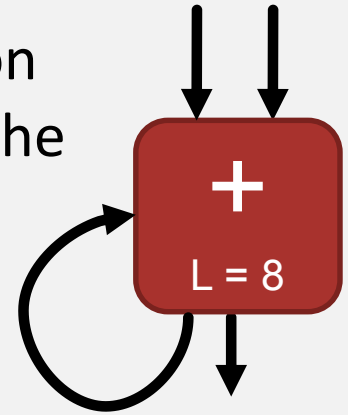
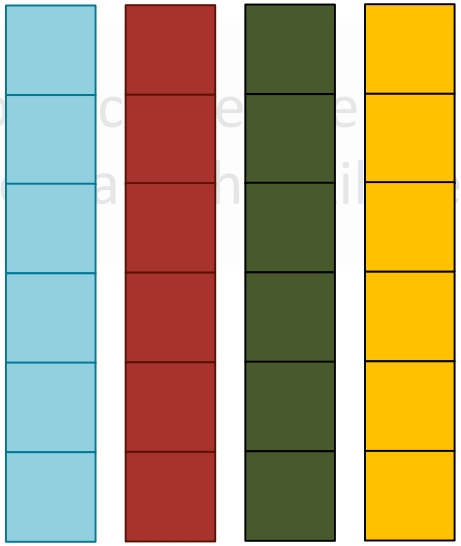
Challenge: Loop-carried dependencies cause pipeline stalls that kill performance.	**Solution:** Transpose iteration space to delay inter-iteration dependencies.

Summary

Every iteration depends on the previous:

$I = 8$





```
for (int i = 0; i < N; ++i) {
  float acc = 0;
  for (int j = 0; j < M; ++j) {
    acc += stream.Pop();
  }
}
```

```
float acc[M];
for (int i = 0; i < N; ++i) {
  for (int j = 0; j < M; ++j) {
    acc[M] += stream.Pop();
  }
}
```

Summary

Challenge: Pipeline throughput (initiation interval) is limited by hardware interfaces.	**Solution:** Exploit abundant on-chip fast memory to minimize I/O requirements.
Challenge: Designing for maximum throughput for competitive performance.	**Solution:** Exploit a dimension of temporal reuse by unrolling it vertically.
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Solution: Exploit abundant on-chip fast memory to minimize I/O requirements.

Challenge: Designing for maximum throughput for competitive performance.

Solution: Exploit a dimension of temporal reuse by unrolling it vertically.

Challenge: Loop-carried dependencies cause pipeline stalls that kill performance.

Solution: Transpose iteration space to delay inter-iteration dependencies.

Challenge: Large fan-out causes placement and routing to fail.

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Challenge: Pipeline throughput (initiation interval) is limited by hardware interfaces.	**Solution:** Exploit abundant on-chip fast memory to minimize I/O requirements.
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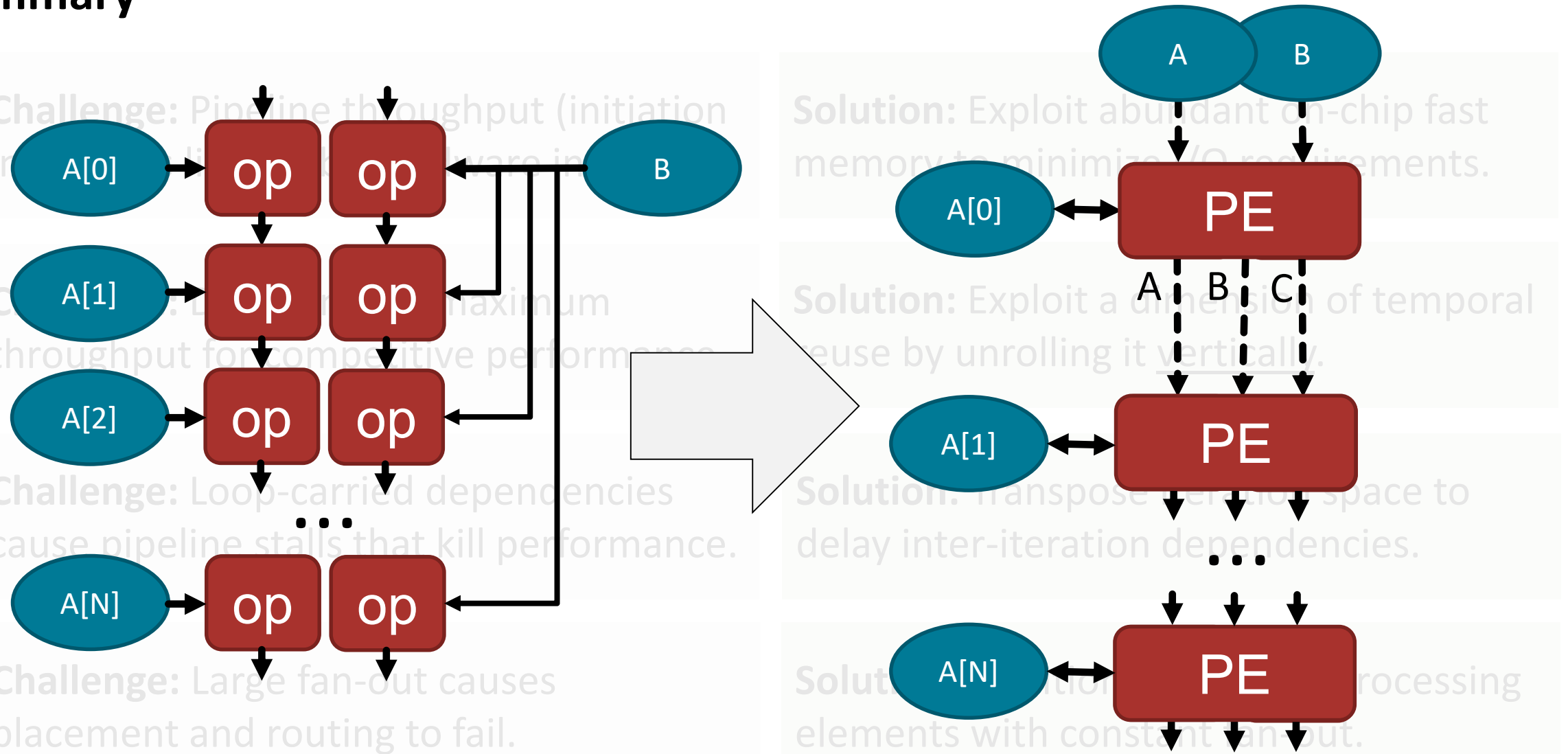

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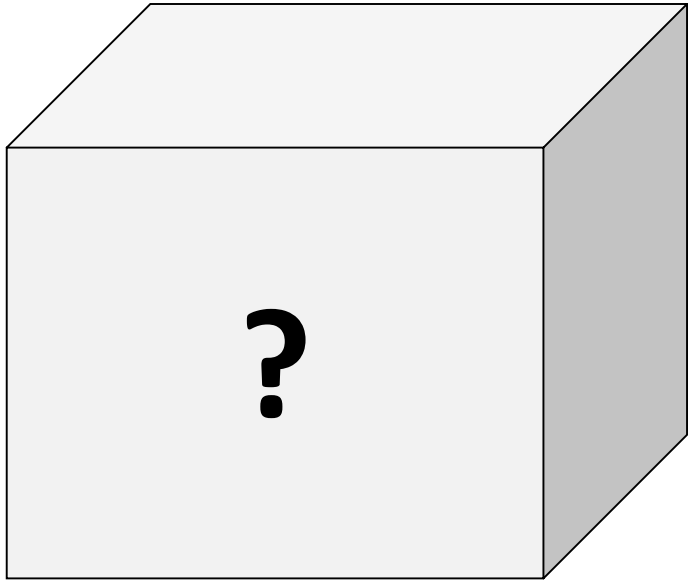
Thank you for your attention ☺

Approaching a new problem



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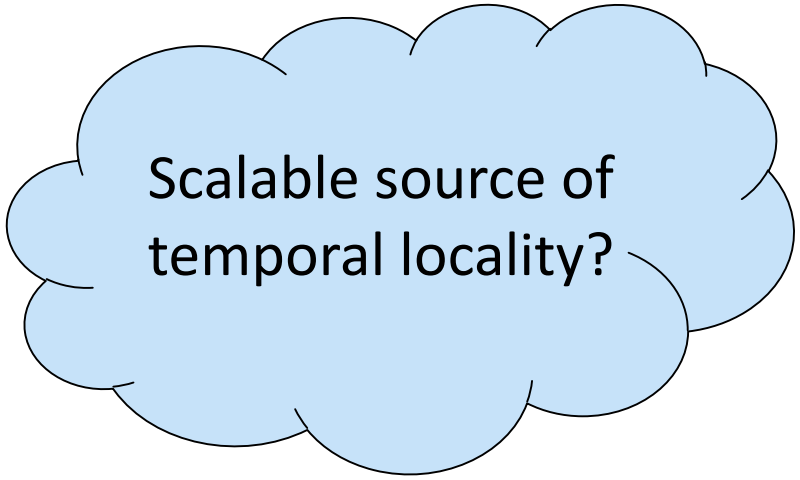

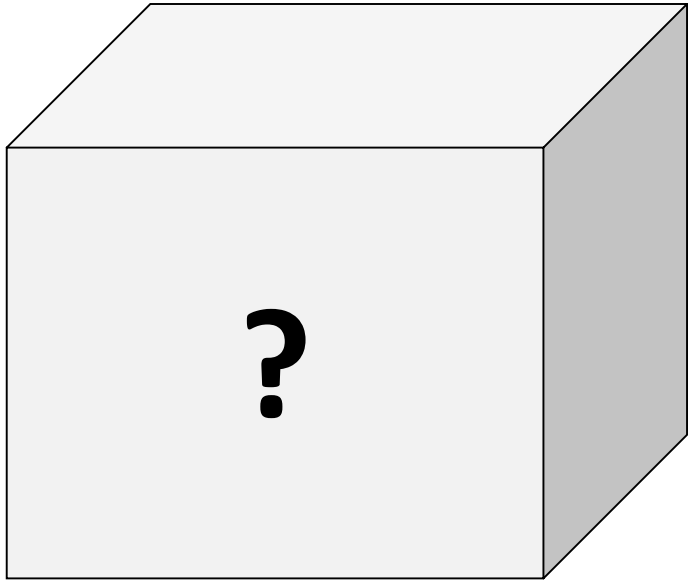

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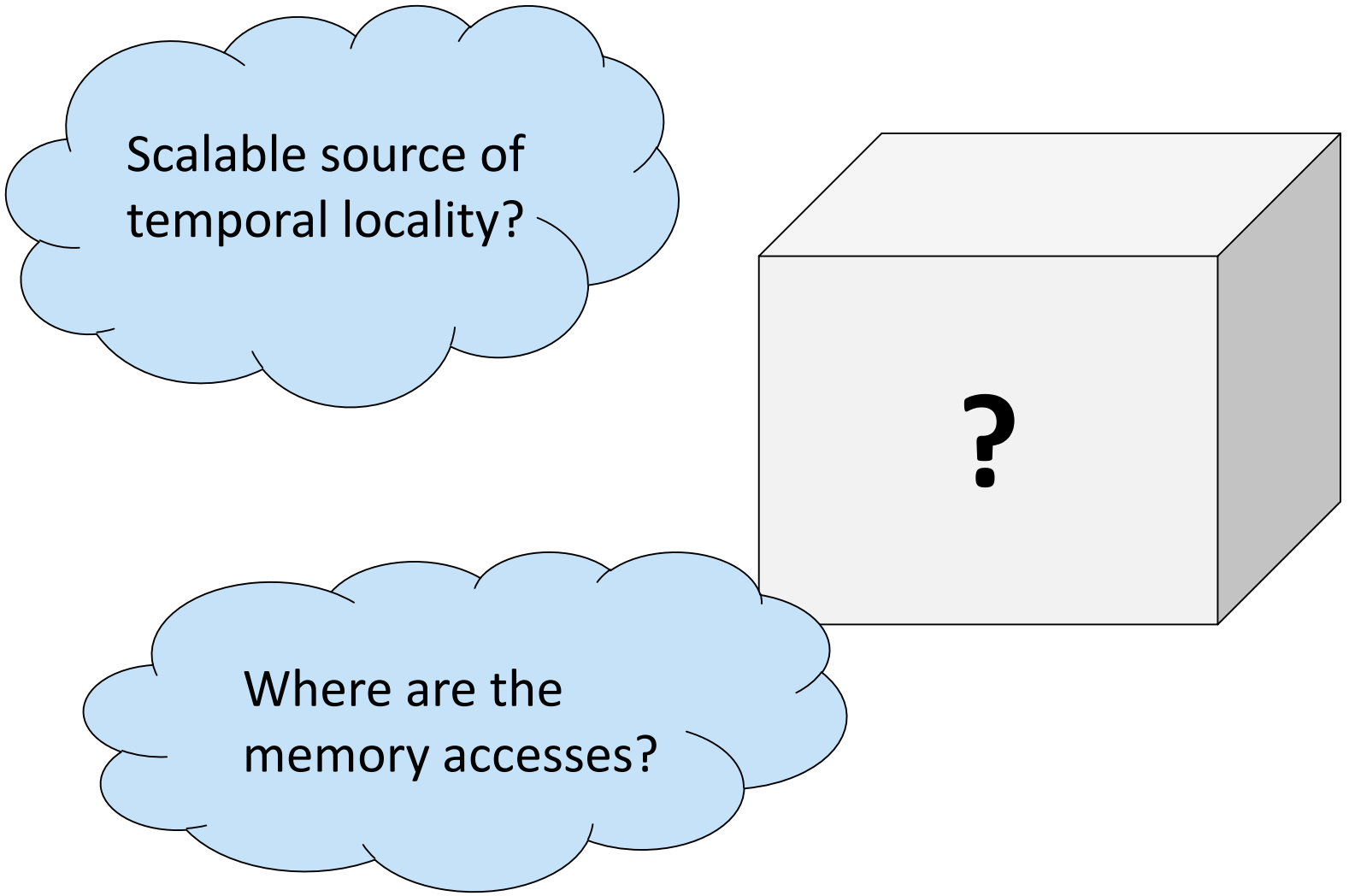

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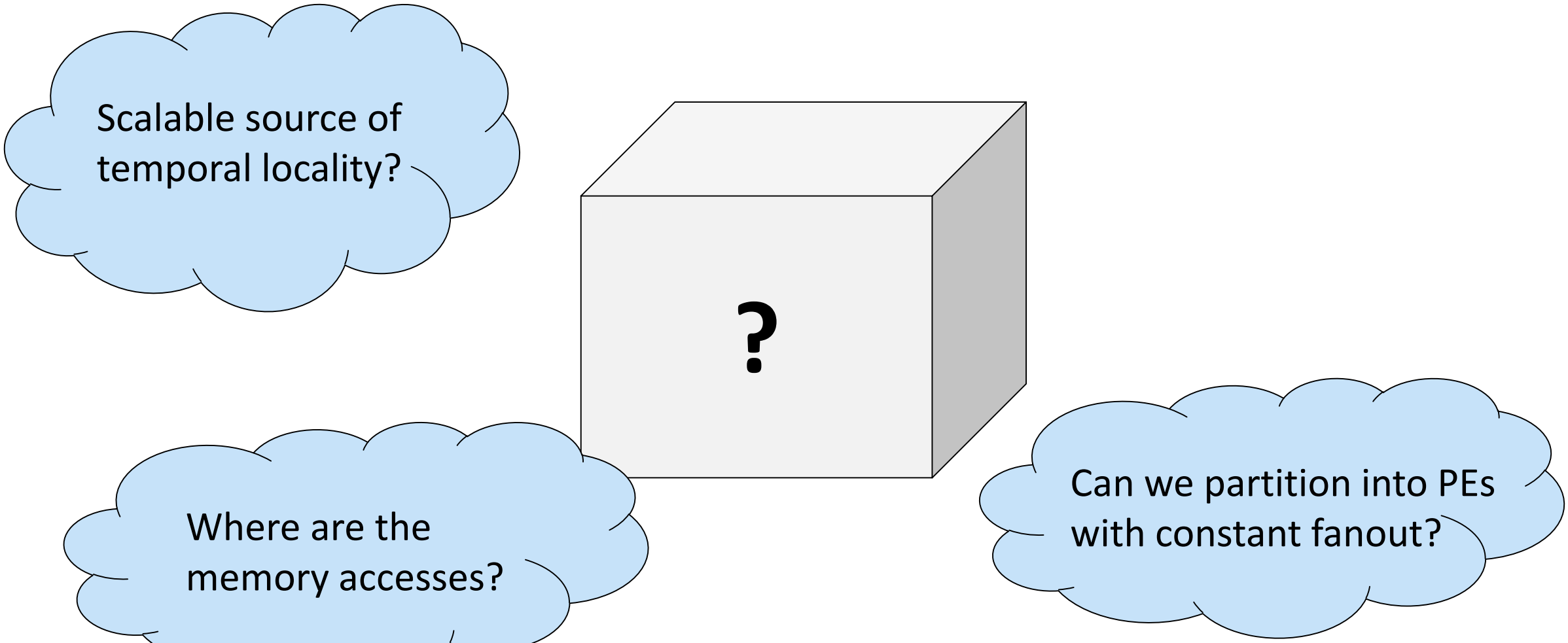

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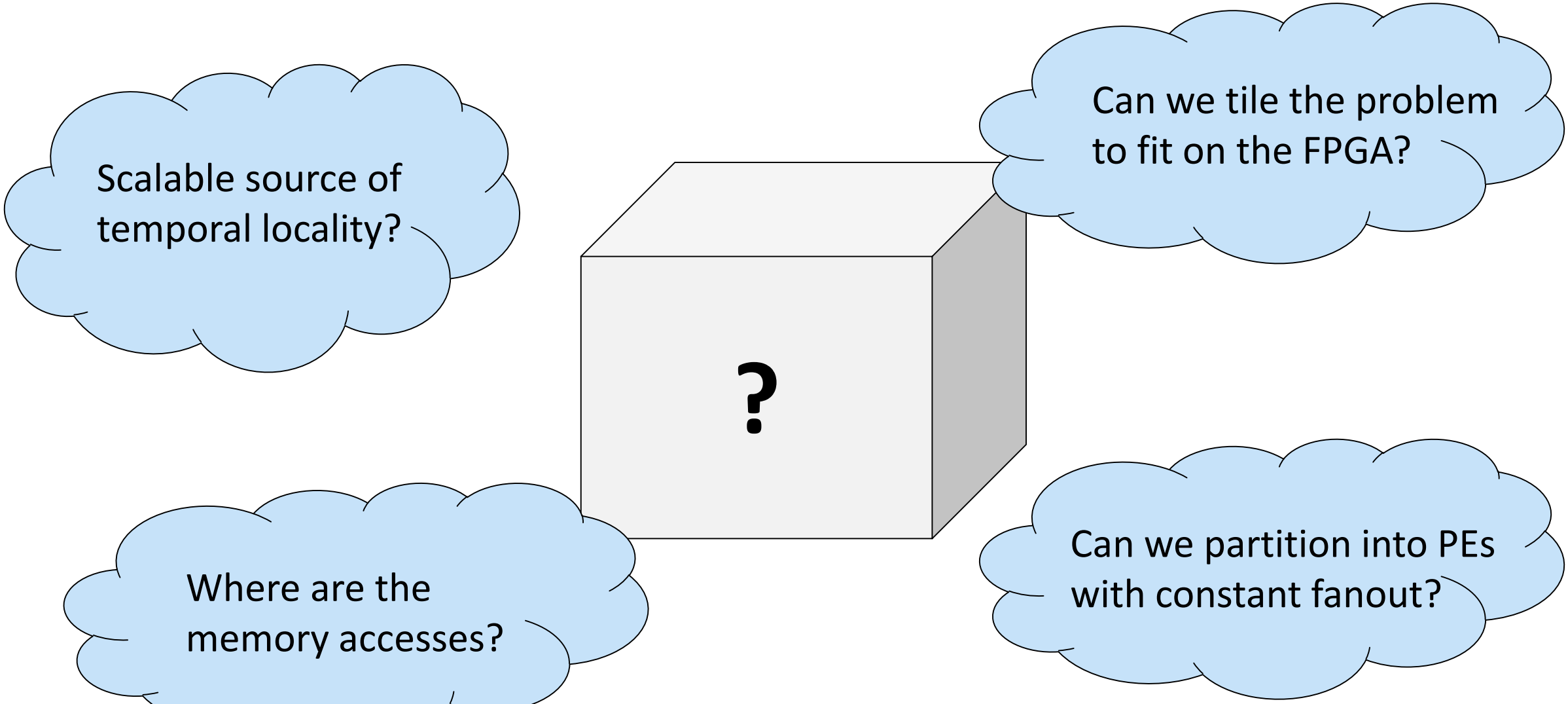

When HDL should be involved

```
always @(posedge ACLK) begin
    if (~ARESETN | system_reset) begin
        write_state <= WRITE_IDLE;
        write_addr <= 0;
        start_kernel_signal <= 1'b0;
        SC_reset <= 1'b0;
        icap_wr <= 1'b0;
        host2device_wr <= 1'b0;
        host2device <= 32'h0;
        system_reset <= 1'b0;
    end
    else begin
      AWREADY <= 1'b1;
      WREADY <= 1'b0;
      BVALID <= 1'b0;
      system_reset <= 1'b0;
```

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```

Latency critical optimizations

When HDL should be involved

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    end
    else begin
      AWREADY <= 1'b1;
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```

Latency critical optimizations

Interfacing

When HDL should be involved

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always @(posedge ACLK) begin
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        write_state <= WRITE_IDLE;
        write_addr <= 0;
        start_kernel_signal <= 1'b0;
        SC_reset <= 1'b0;
        icap_wr <= 1'b0;
        host2device_wr <= 1'b0;
        host2device <= 32'h0;
        system_reset <= 1'b0;
    end
    else begin
      AWREADY <= 1'b1;
      WREADY <= 1'b0;
      BVALID <= 1'b0;
      system_reset <= 1'b0;
```
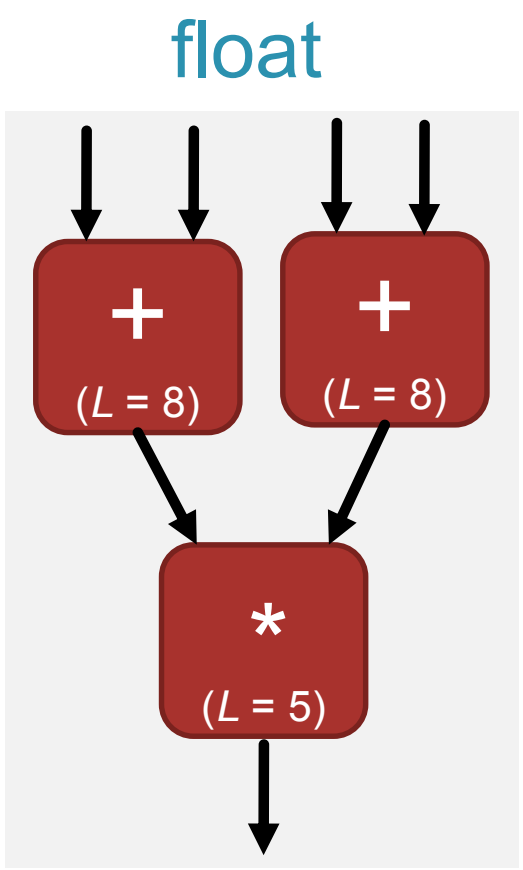

HDL and HLS can (and do often) happily co-exist!

```
for (int i = 1; i < N - 1; ++i) {
  for (int j = 0; j < M; ++j) {
    #pragma HLS PIPELINE II=1


    const auto above = above_buffer.read();
    const auto center = center_buffer.read();
                                mory_in[(i + 1)*M + j];

                              = 0.3333;

        factor * (above + center + below);

    above_buffer.write(center);
    center_buffer.write(below);

    memory_out[i * M + j] = average;
  }
}
```

Types on FPGA



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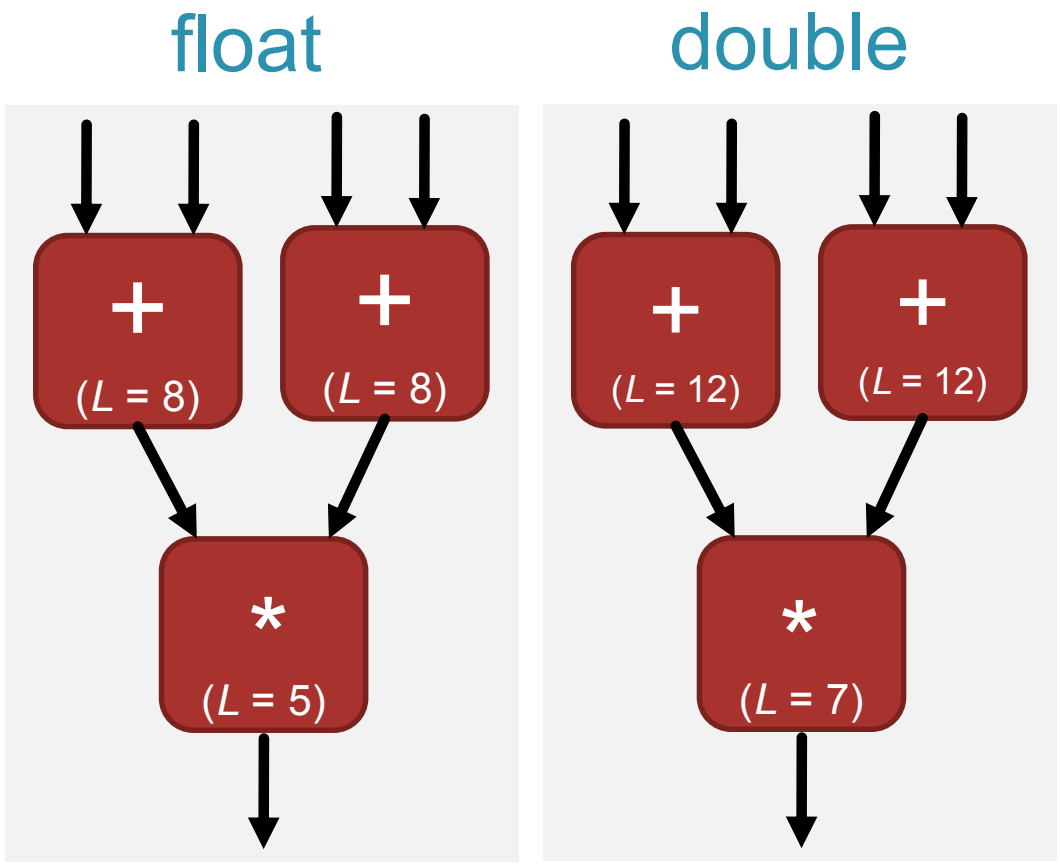
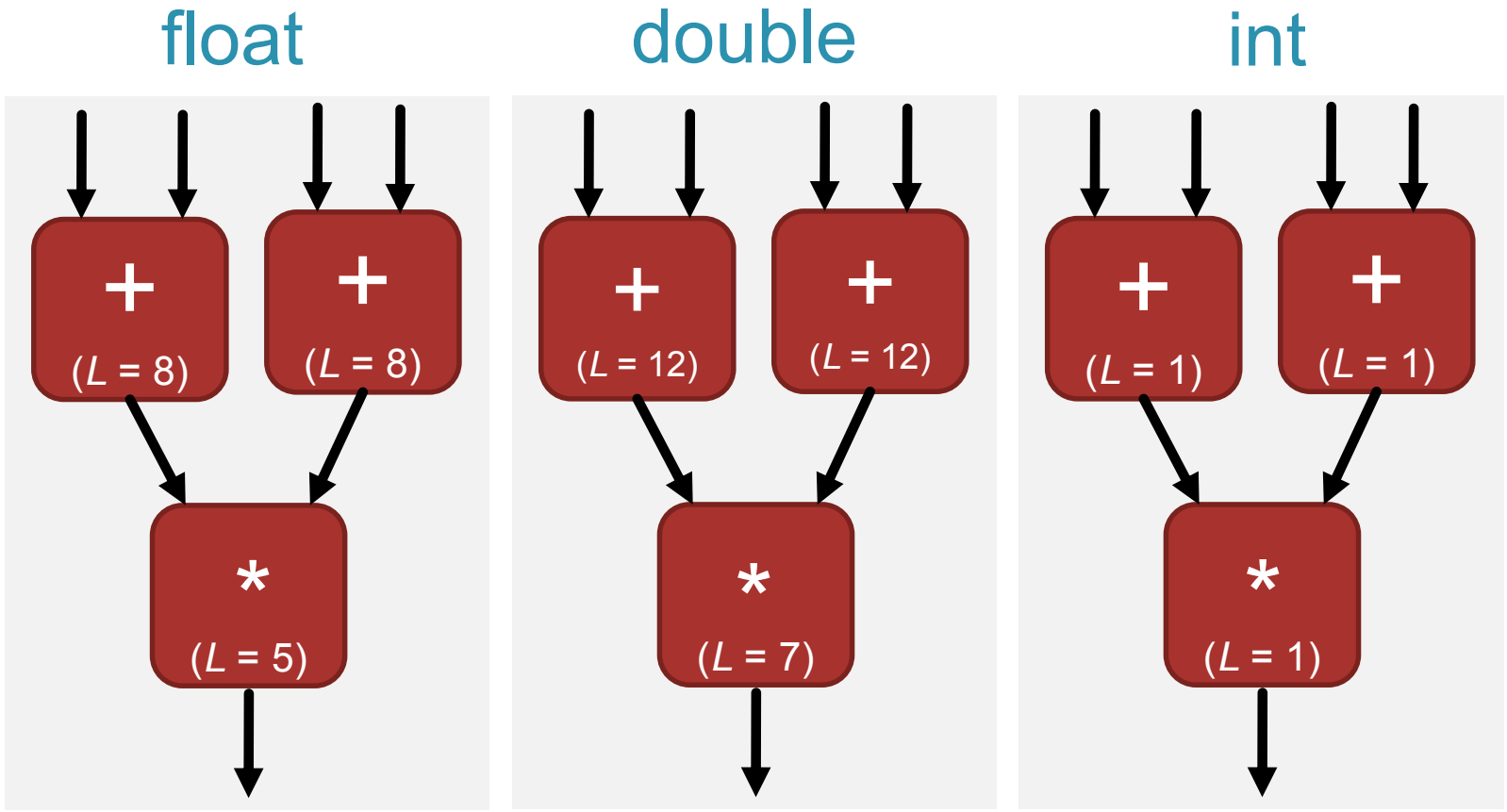


Types on FPGA



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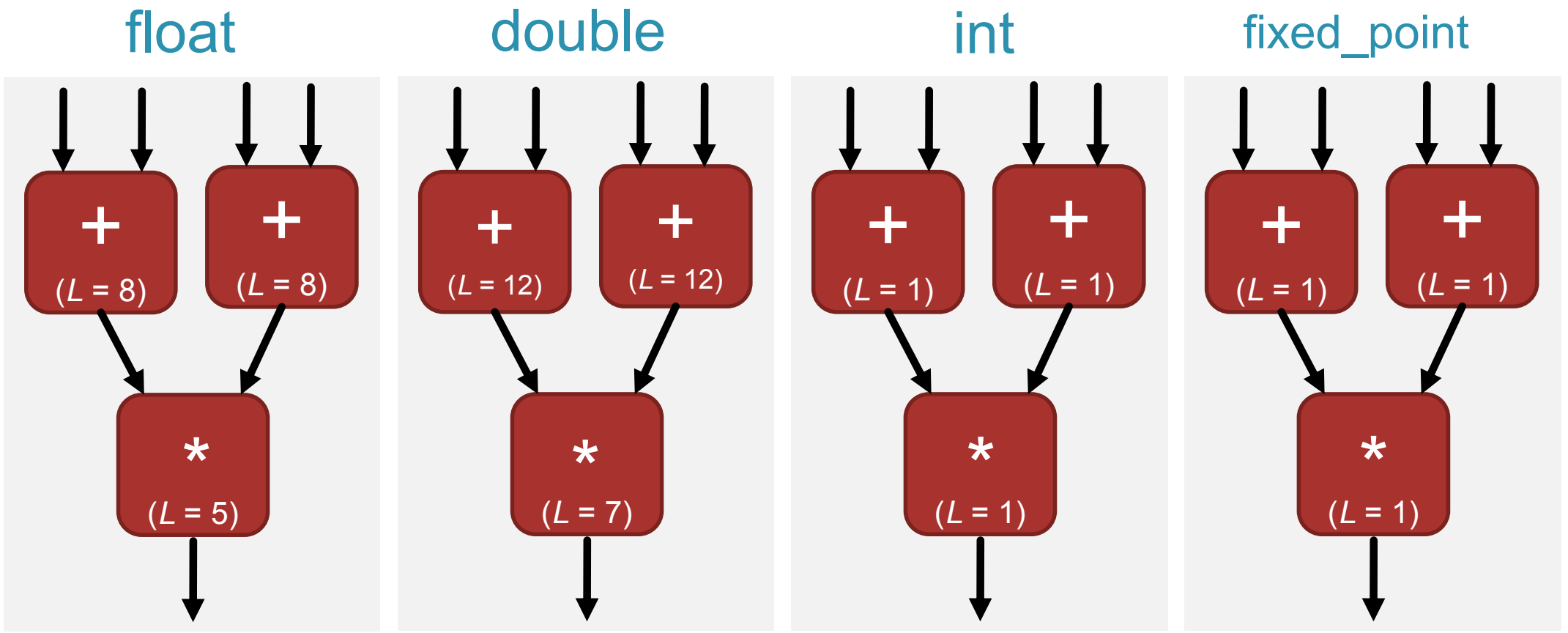

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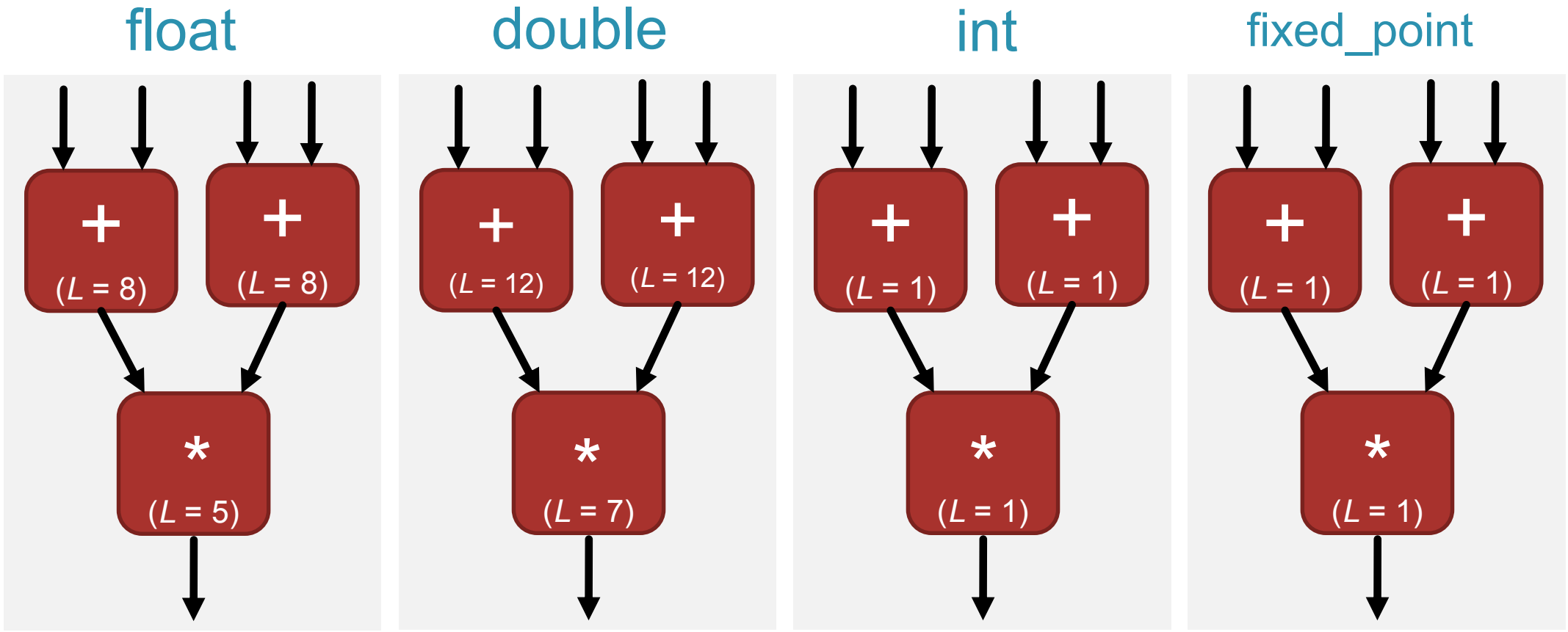

Same concepts, different latencies (some problems go away at $L = 1$).