CEG2136 LAB 2
Group 21

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1 Theoretical Implementation

1.1 Lab Objectives

This second lab continues to introduce students to the basic components of digital systems, namely JK flip flops and essential logical elements. Students will use *Altera Quartus II* to design, compile and run/verify two different sequential circuits.

1. From a given sequence, karnaugh maps and input equations for the JKs will be derived.
2. In *Altera Quartus II*, the JKs will be connected according to the derivations.
3. The counters will be tested using a push-button and a free-running clock that will be read using an oscilloscope.

1.2 Discussion of Requirements

The goal of the lab is to implement a '3 bit synchronous modulo 6' and '4 bit synchronous BCD' counters and have them run without errors on the *Altera DE2-115 FPGA*, with every set of inputs resulting in the output predicted by their karnaugh map. These two counters will be tested using one of two possible methods, either visualizing the output on an oscilloscope 14 or manually with a push-button and LEDs on the *Altera DE2-115 FPGA*.

Required equipment and items:

1. An x86-compatible PC running *Quartus II*.
2. The *Altera DE2-115 FPGA*.
3. CEG2136 lab manual.
4. Oscilloscope and required interface.

1.3 Proposed Algorithmic Solution

1.3.1 Karnaugh Maps for Counter A

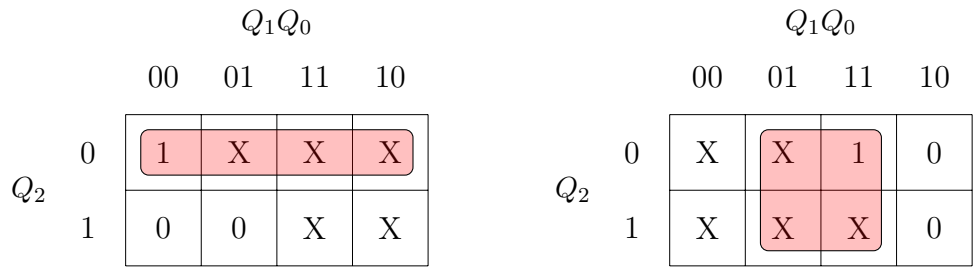
Q_2 \ Q_1Q_0	00	01	11	10
0	0	X	X	0
1	0	X	X	1

$$J_0 = Q_2Q_1$$

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	0	X
1	X	1	X	X

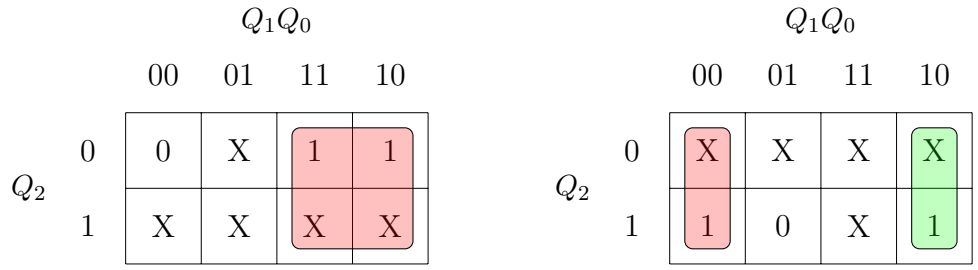
$$K_0 = Q_2$$

Figure 1: Karnaugh Maps for A-JK_0



$J_1 = Q_2'$ $K_1 = Q_0$

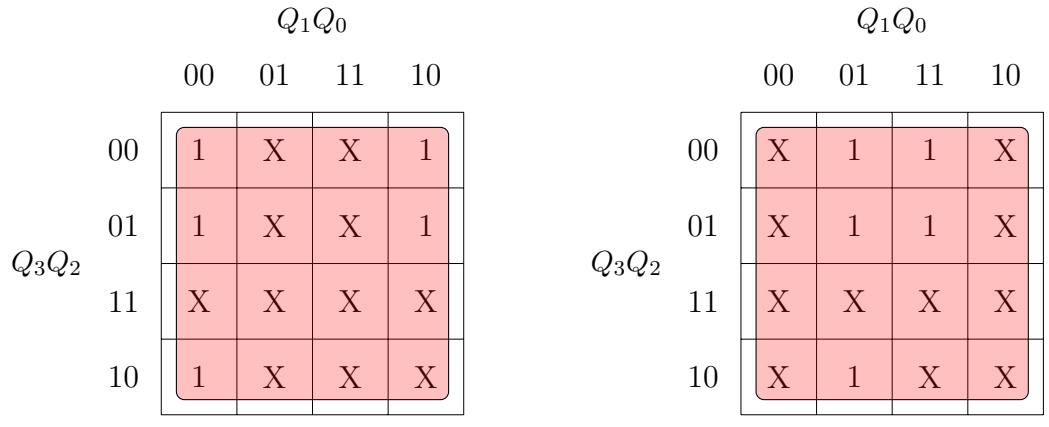
Figure 2: Karnaugh Maps for A-JK_1



$J_2 = Q_1$ $K_2 = Q_0'$

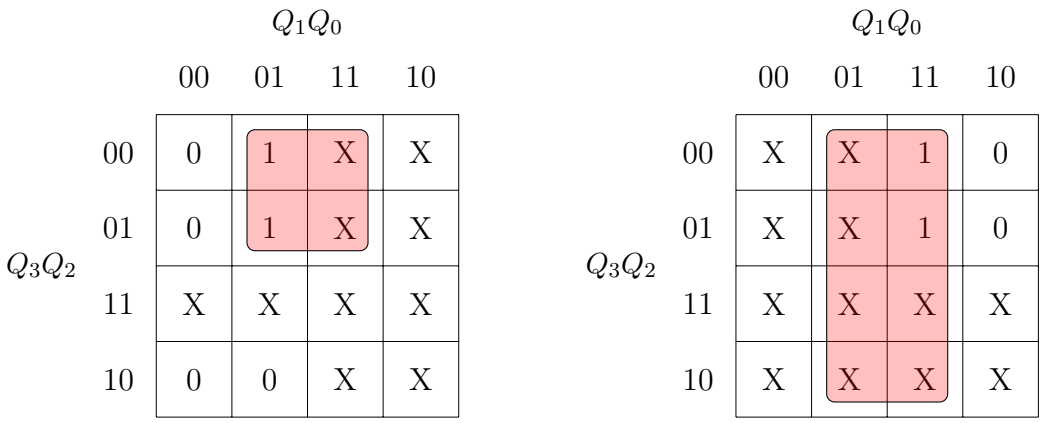
Figure 3: Karnaugh Maps for A-JK_2

1.3.2 Karnaugh Maps for Counter B



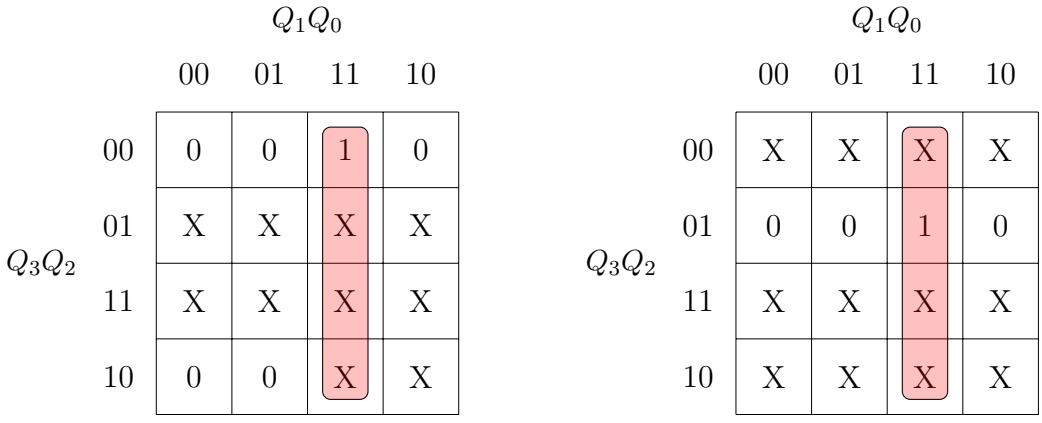
$J_0 = 1$ $K_0 = 1$

Figure 4: Karnaugh Maps for B-JK_0



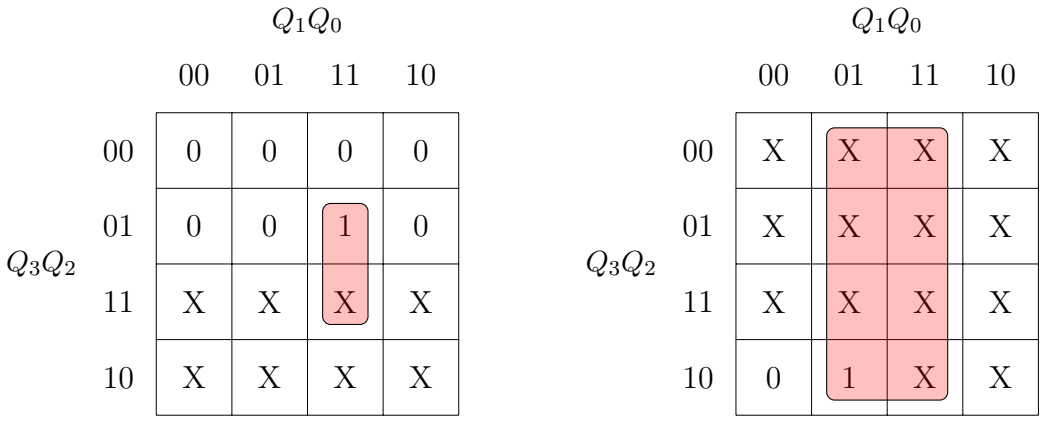
$$J_1 = Q_3' Q_0 \qquad K_1 = Q_0$$

Figure 5: Karnaugh Maps for B-JK_1



$$J_2 = Q_0 Q_1 \qquad K_2 = Q_0 Q_1$$

Figure 6: Karnaugh Maps for B-JK_2



$$J_3 = Q_2 Q_1 Q_0 \qquad K_3 = Q_0$$

Figure 7: Karnaugh Maps for B-JK_3

2 Design

2.1 QUARTUS II Circuit Diagrams

The circuits were implemented in *Altera Quartus II* using components chosen by reading the Karnaugh maps from *Figure 1* through to *Figure 7*.

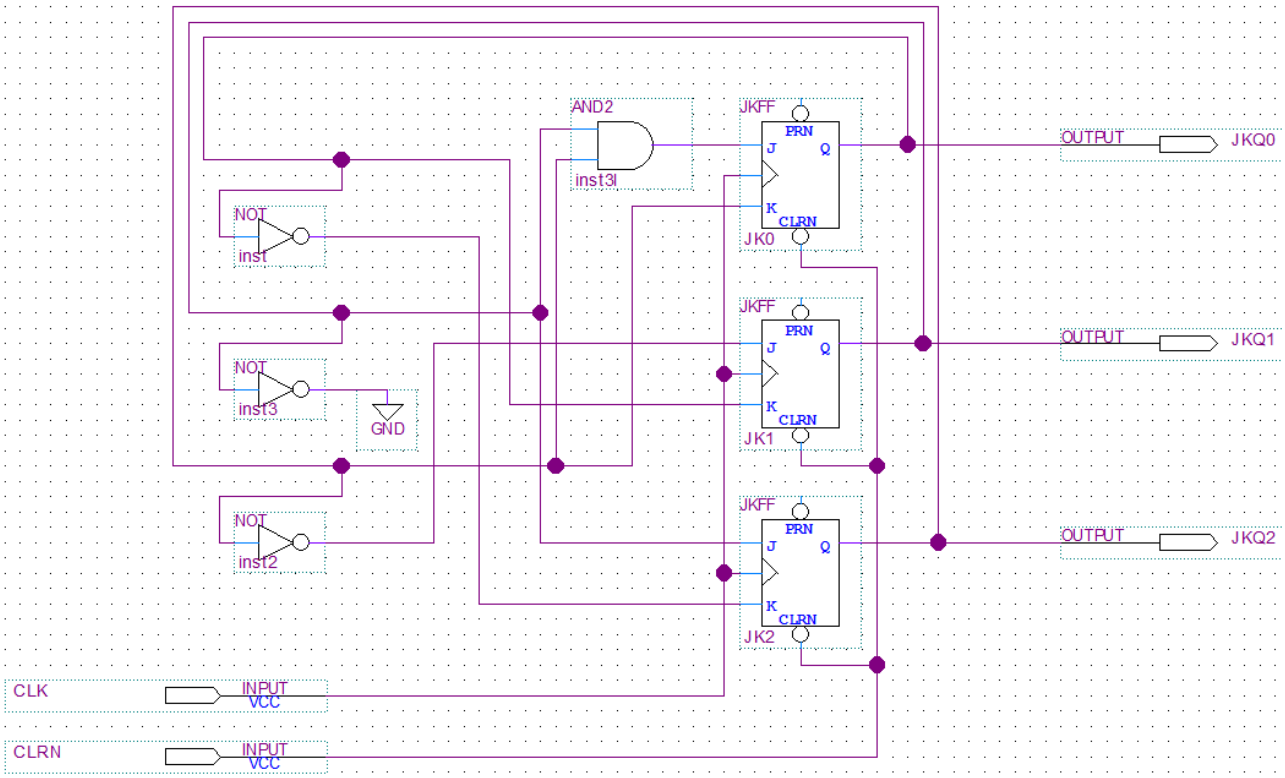


Figure 8: Circuit 'A', a 3-bit counter.

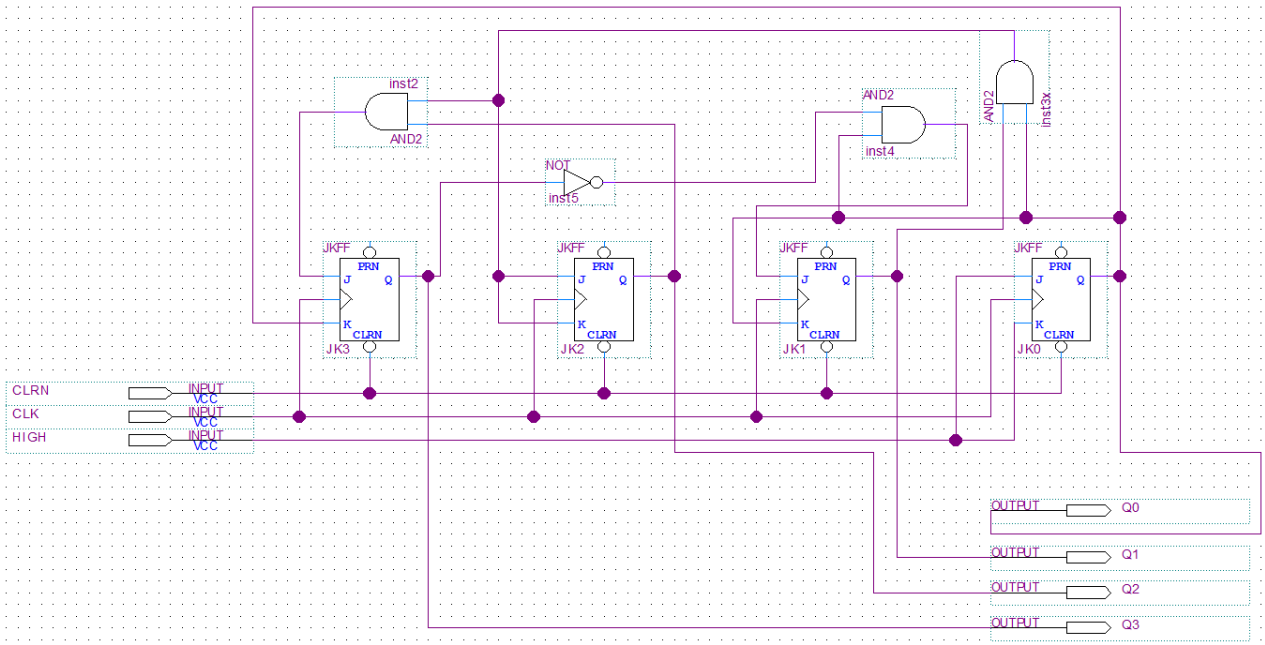


Figure 9: Circuit 'B', a 4-bit counter.

2.2 Components Utilized

Our designs, as shown in as shown in **Figure 8** and **Figure 9**, were implemented as intended with simple AND,OR and NOT logic gates and JK Flipflops. No alternative components, that is, similar components with different part numbers (than those specified in the lab manual,) were used to create the logical circuit.

2.3 Implemented Solution

When implementing our solution, we took the following steps:

1. *Altera Quartus II* was opened and the file was initialized.
2. Both circuits were implemented according to the karnaugh maps.
3. Pins were added and assigned correctly.
4. The file was compiled.
5. At this point, the circuits were ready to simulate/verify/apply test procedures.

2.4 Challenging Problems Encountered

No major problems were encountered in this section of the lab. However, we did rush this portion of the lab, as we failed to fully complete the karnaugh maps for the 4-bit BCD counter in time for the lab. Our only major hangups were encountered

3 Implementation

3.1 Simulation Results

Figure 12 Figure 13 both show a set of 16 clock cycles, enough to fully visualize a single full run of a 4-bit sequential counter and two 8-step runs of a generic 3-bit sequential counter. Both simulated cycles ran as expected, and we didn't encounter any errors in this part of our testing.

3.2 Block Diagrams

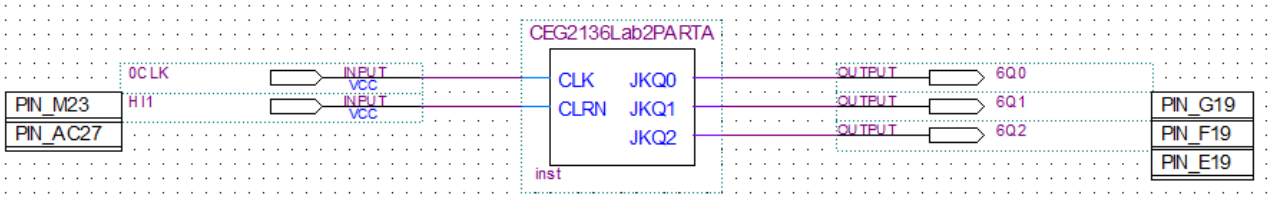


Figure 10: Block Diagram for Circuit A

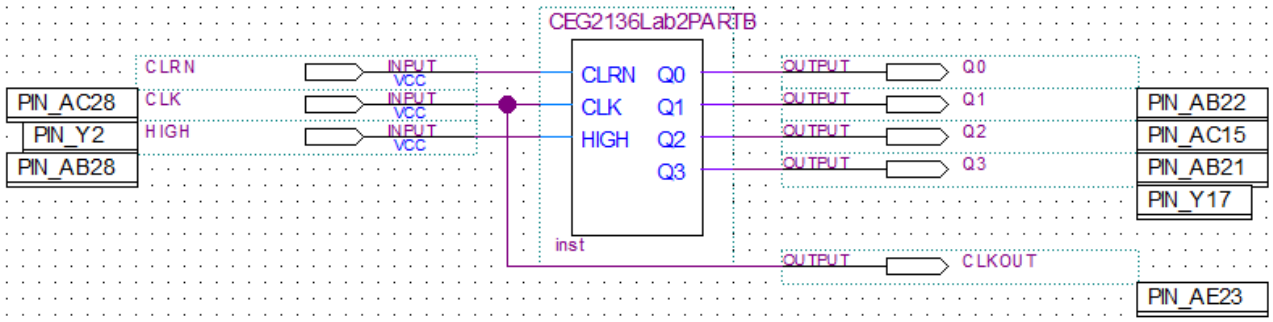


Figure 11: Block Diagram for Circuit B

3.3 Simulated Waveforms

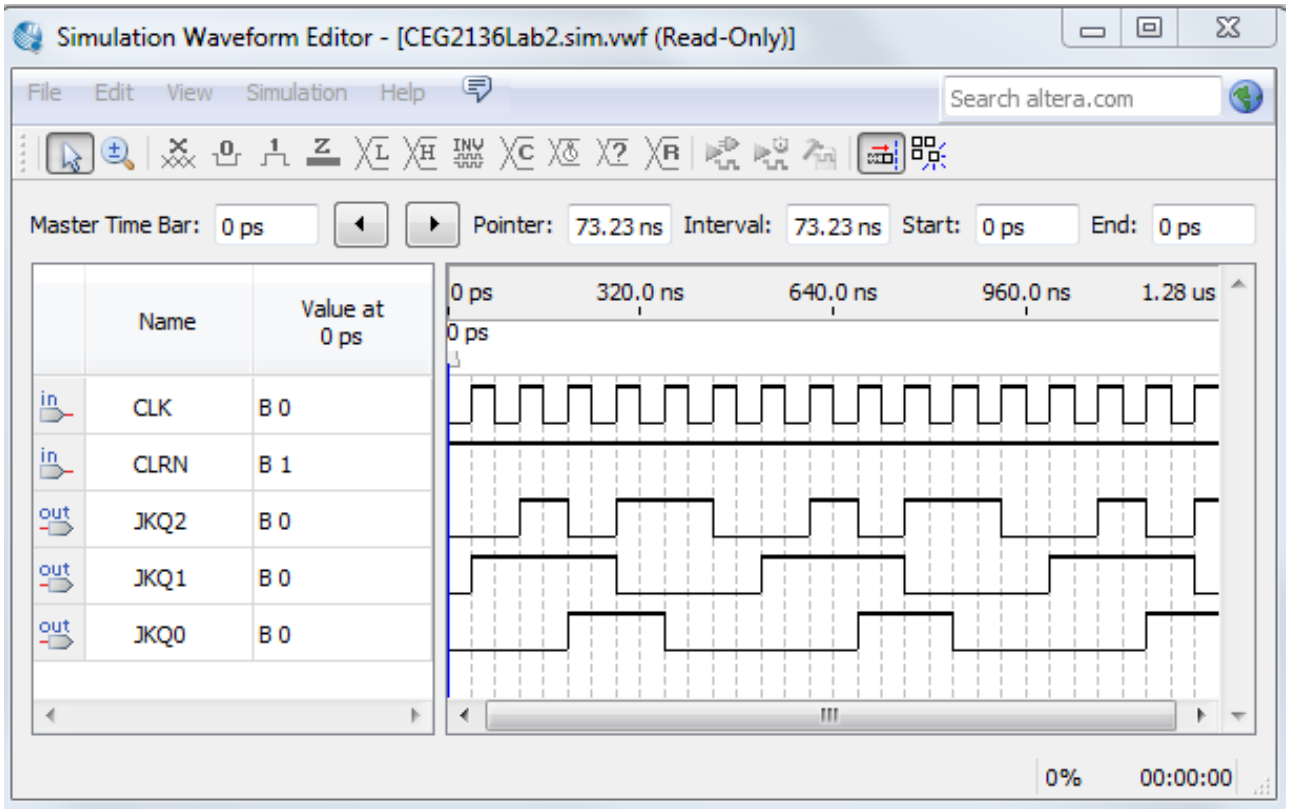


Figure 12: Logical Circuit Waveform Output for Circuit A

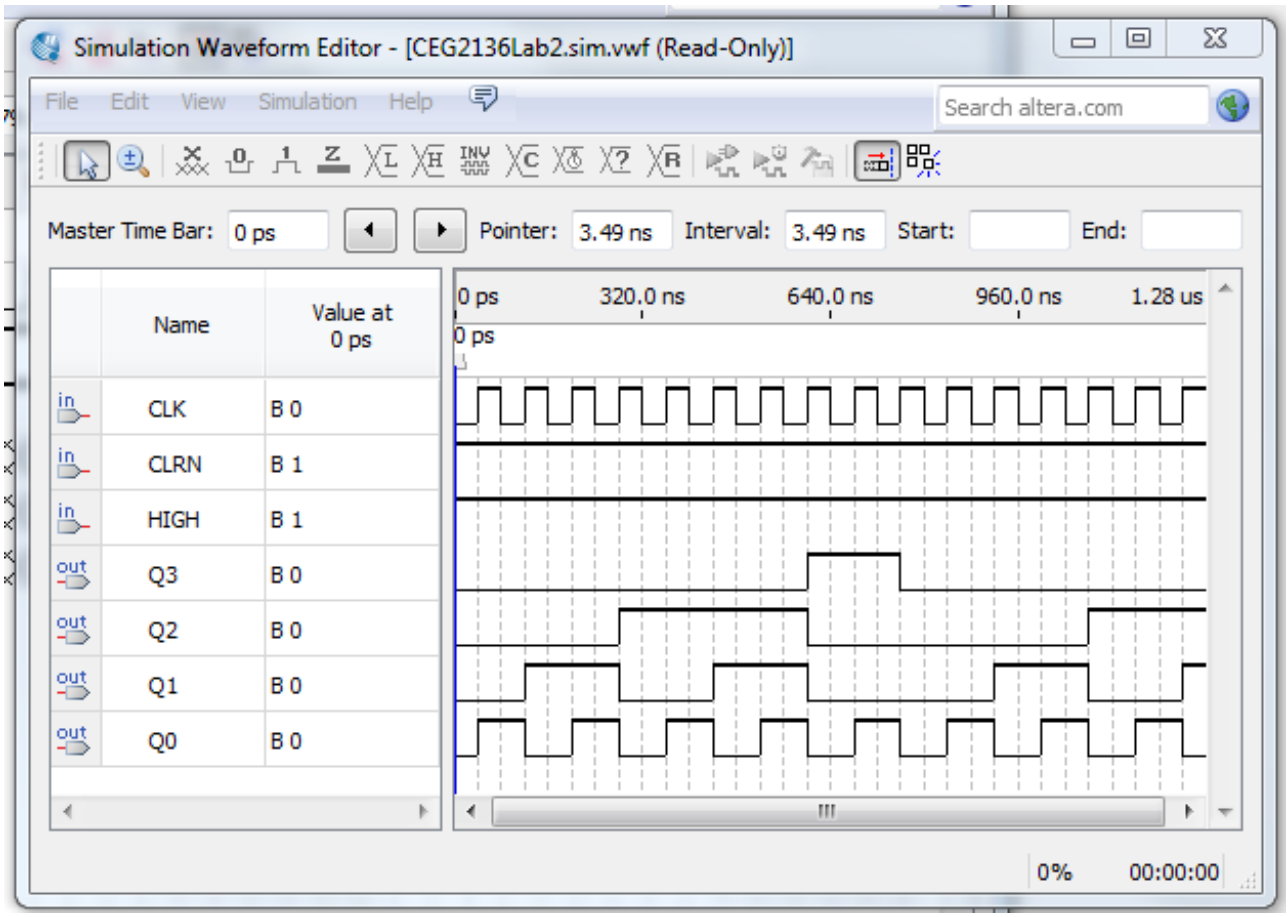


Figure 13: Logical Circuit Waveform Output for Circuit B

3.4 Oscilloscope Output

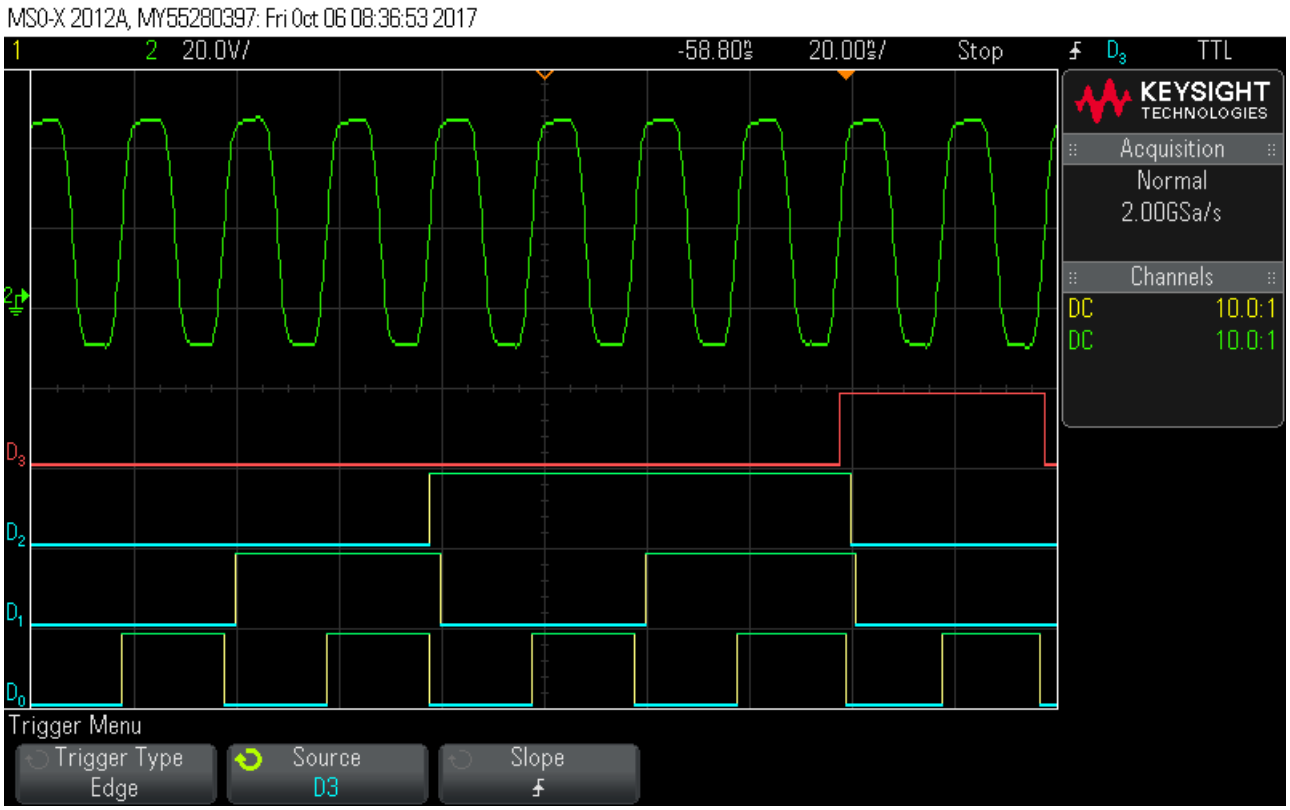


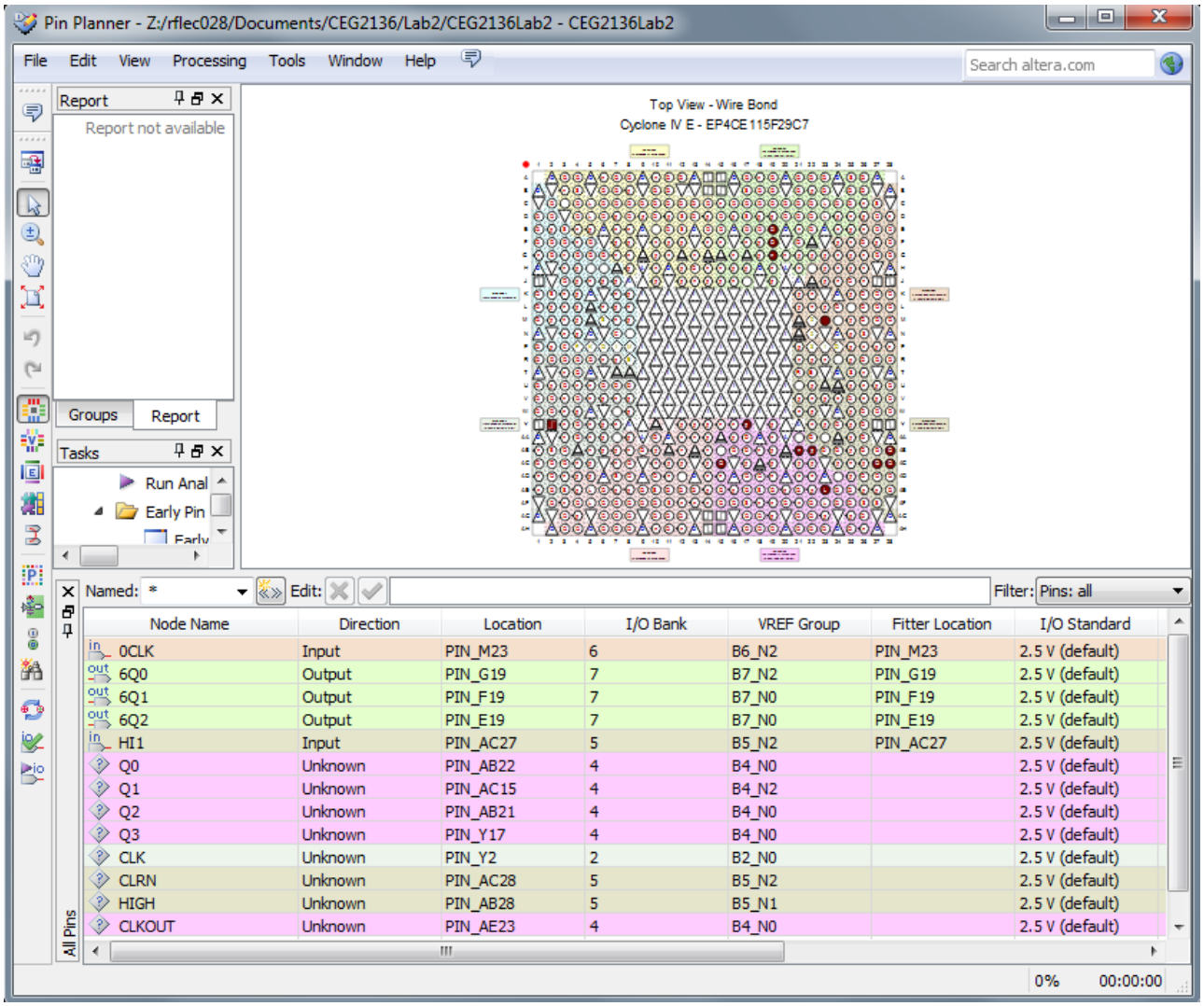
Figure 14: Oscilloscope Output from 4-Bit Synchronous BCD Counter

4 Discussion

After exhaustive testing of our running logical circuit, we simulated the BCD counter using *Altera DE2-115 FPGA* and, by connecting *GPIO 40-pin assignments*, we managed to output the counter signal to Oscilloscope, while the clock frequency was transfered by the coaxial cable. The dynamic images we got from Oscilloscope' screen (See **Figure 14**) was perfect and precise, showing the exactly how the BCD counter would work. After we had done with Oscilloscope experiment, we began our simulation of the 3-bit counter with the 'push-button' method, in which we assigned the CLK pin from the modulo 6 counter to a button switch on the *Altera DE2-115 FPGA* board. In this case, each time of push-and-release to the button acted as a clock cycle, going from 0 to 1 then back to 0. After LED pins were assigned for the three digits as well as compilation done, we can advance the cycle manually by pressing the button switch. Each press and release advanced the 3-bit counter by one clock period and we could observe the state of the simulated counter via the Altera board's LED outputs.

4.1 Errors Encountered

Figure 15 shows our final pin plan. This is where we had the most difficulty - At one point, our lab group had the oscilloscope up and running, but didn't have any output. After checking the pin planner again, we found that it simply hadn't saved the assignments at all.



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
0CLK	Input	PIN_M23	6	B6_N2	PIN_M23	2.5 V (default)
6Q0	Output	PIN_G19	7	B7_N2	PIN_G19	2.5 V (default)
6Q1	Output	PIN_F19	7	B7_N0	PIN_F19	2.5 V (default)
6Q2	Output	PIN_E19	7	B7_N0	PIN_E19	2.5 V (default)
HI1	Input	PIN_AC27	5	B5_N2	PIN_AC27	2.5 V (default)
Q0	Unknown	PIN_AB22	4	B4_N0		2.5 V (default)
Q1	Unknown	PIN_AC15	4	B4_N2		2.5 V (default)
Q2	Unknown	PIN_AB21	4	B4_N0		2.5 V (default)
Q3	Unknown	PIN_Y17	4	B4_N0		2.5 V (default)
CLK	Unknown	PIN_Y2	2	B2_N0		2.5 V (default)
CLRN	Unknown	PIN_AC28	5	B5_N2		2.5 V (default)
HIGH	Unknown	PIN_AB28	5	B5_N1		2.5 V (default)
CLKOUT	Unknown	PIN_AE23	4	B4_N0		2.5 V (default)

Figure 15: Implemented Pin Plan for EP4CE115F29 Device.

4.2 Conclusions

During lab 2 we continued to experiment with sequential circuits, and learned how to use Oscilloscope kit to visualize their outputs. The oscilloscope was new content introduced to this course, so was our first time contacting with such expensive equipment. It seems using Oscilloscope to simply be a real-time waveform simulator is a over-kill, but we expect further discovery on it, along with more complex course content we will encounter. Lab 2 emphasized on the structure and functionality of sequential circuits, and by utilizing K-maps and various lab equipment we had the possibility to visualize the entire scene, from designing to simulating. These visualizations greatly enhanced our understanding towards our current circuit knowledge, and will continue serve as crucial tools of our further study. Learning to build and simulate these simple JK-based synchronous counters both allows students to apply their knowledge of these components, building skills for the workplace, and will help with building more complex designs based on ICs in the future. Conclusively, the implementation of simple 3 and 4-bit counters in Lab 2 was an excellent way to familiarize students with the function of JKff synchronous counters and the mighty oscilloscope.

Implemented by Ryan and Xiuzhu with LaTeXand TeXmaker version 4.5.