# CEG2136 LAB 3
# Group 21

Ryan Fleck - 8276723
Xiuzhu Li - 8571645

November 6, 2017

# Contents



# List of Figures

# 1 Theoretical Implementation

## 1.1 Lab Objectives

The general objectives for this lab are as follows:

- Students will design an ALU.
- The designed ALU will be implemented in *Altera Quartus II*.
- The ALU will be tested using simulated waveforms.
- The ALU's operations will be verified on an *Altera DE2-115 FPGA*.

## 1.2 Discussion of Requirements

## 1.3 Proposed Algorithmic Solution

# 2 Design

## 2.1 QUARTUS II Circuit Diagrams

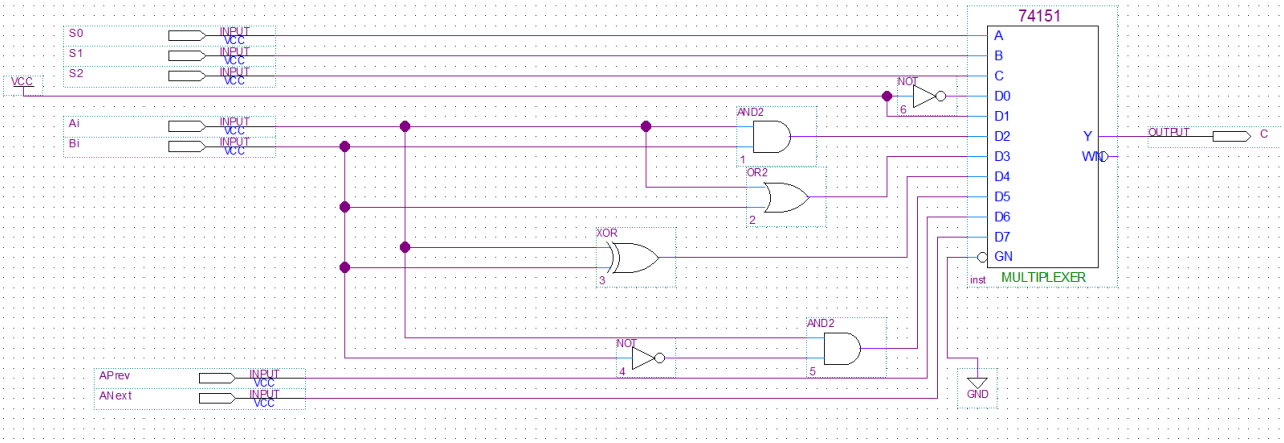


Figure 1: One-Bit Logic and Shift Circuit

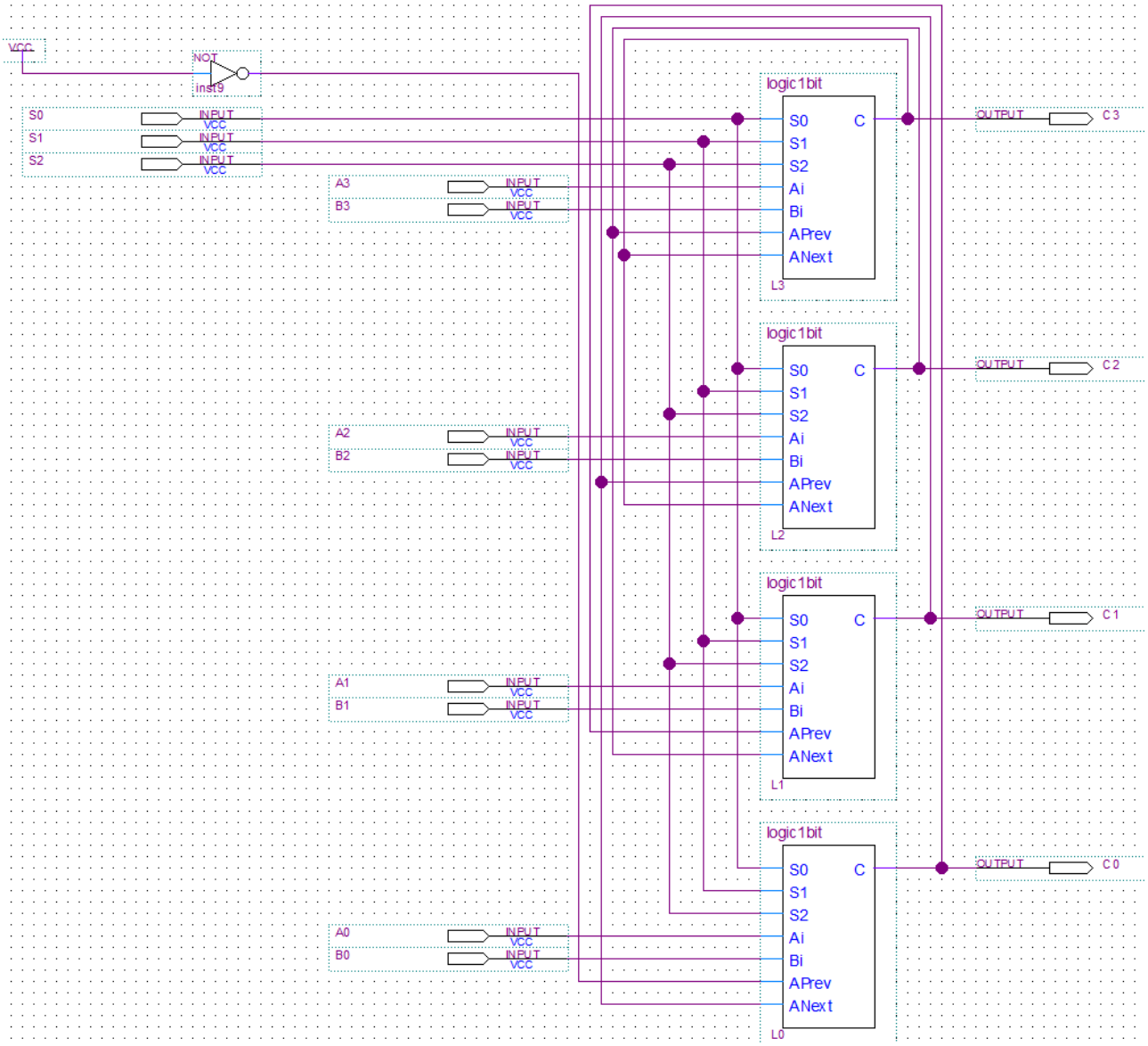


Figure 2: Four-Bit Logic and Shift Circuit

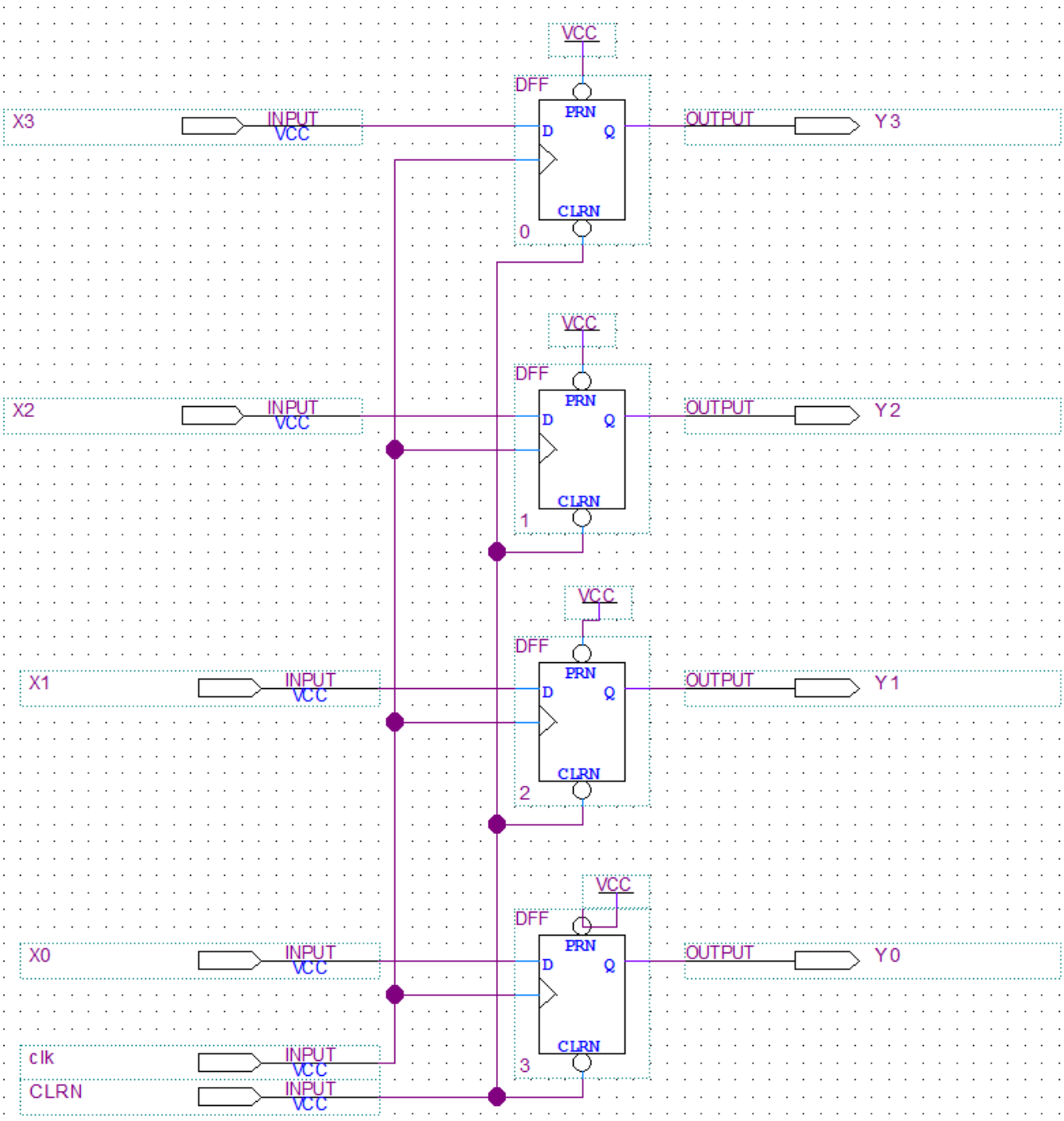


Figure 3: Four-Bit Register

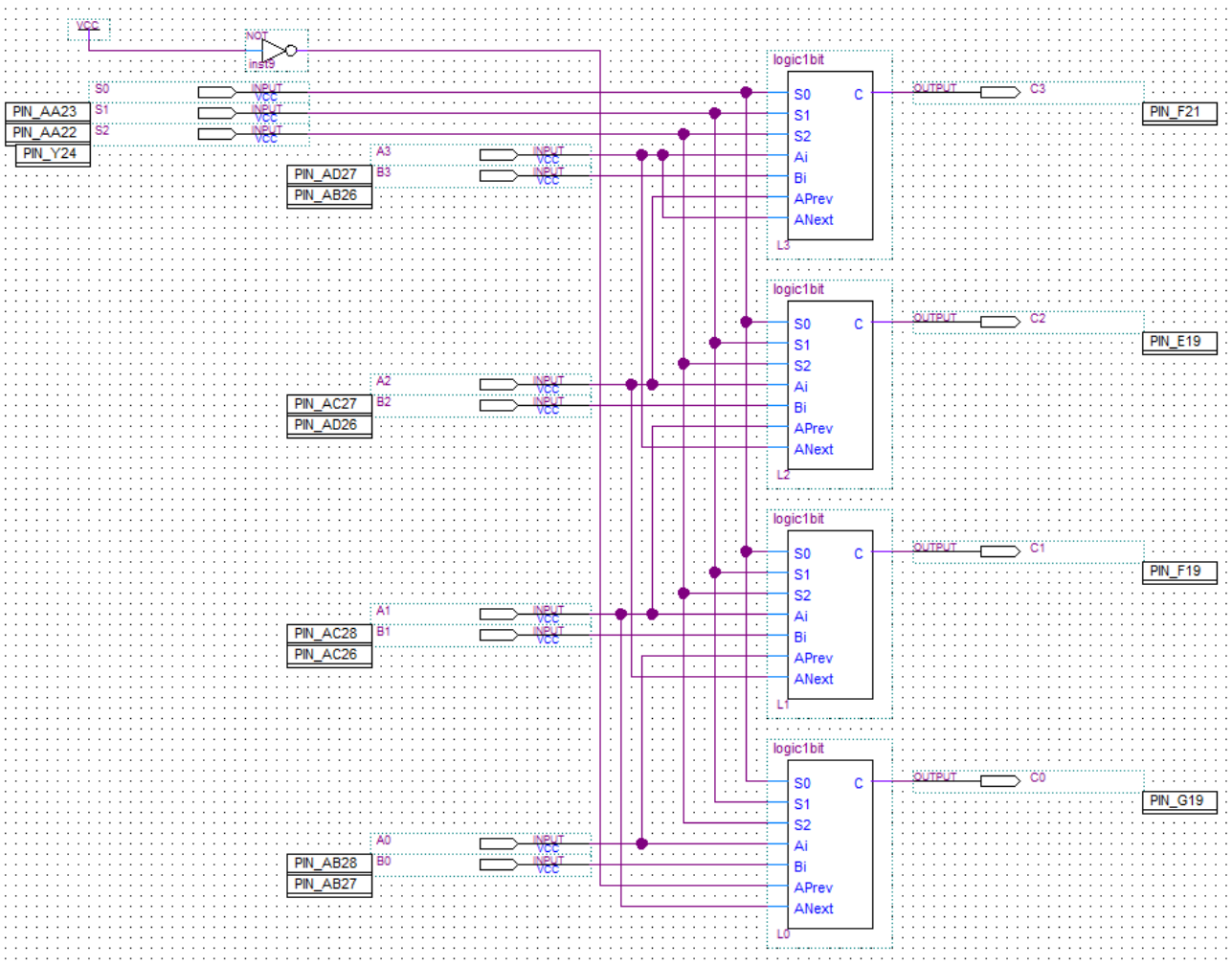


Figure 4: Second Iteration of the Four-Bit Register

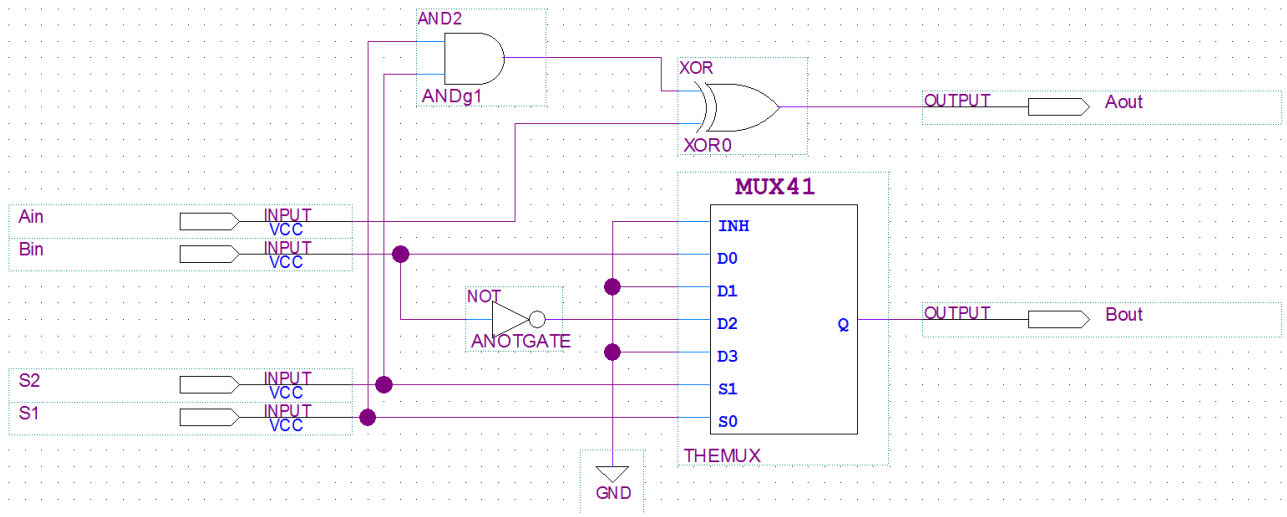


Figure 5: One-Bit Arithmetic Circuit "ABXIO"

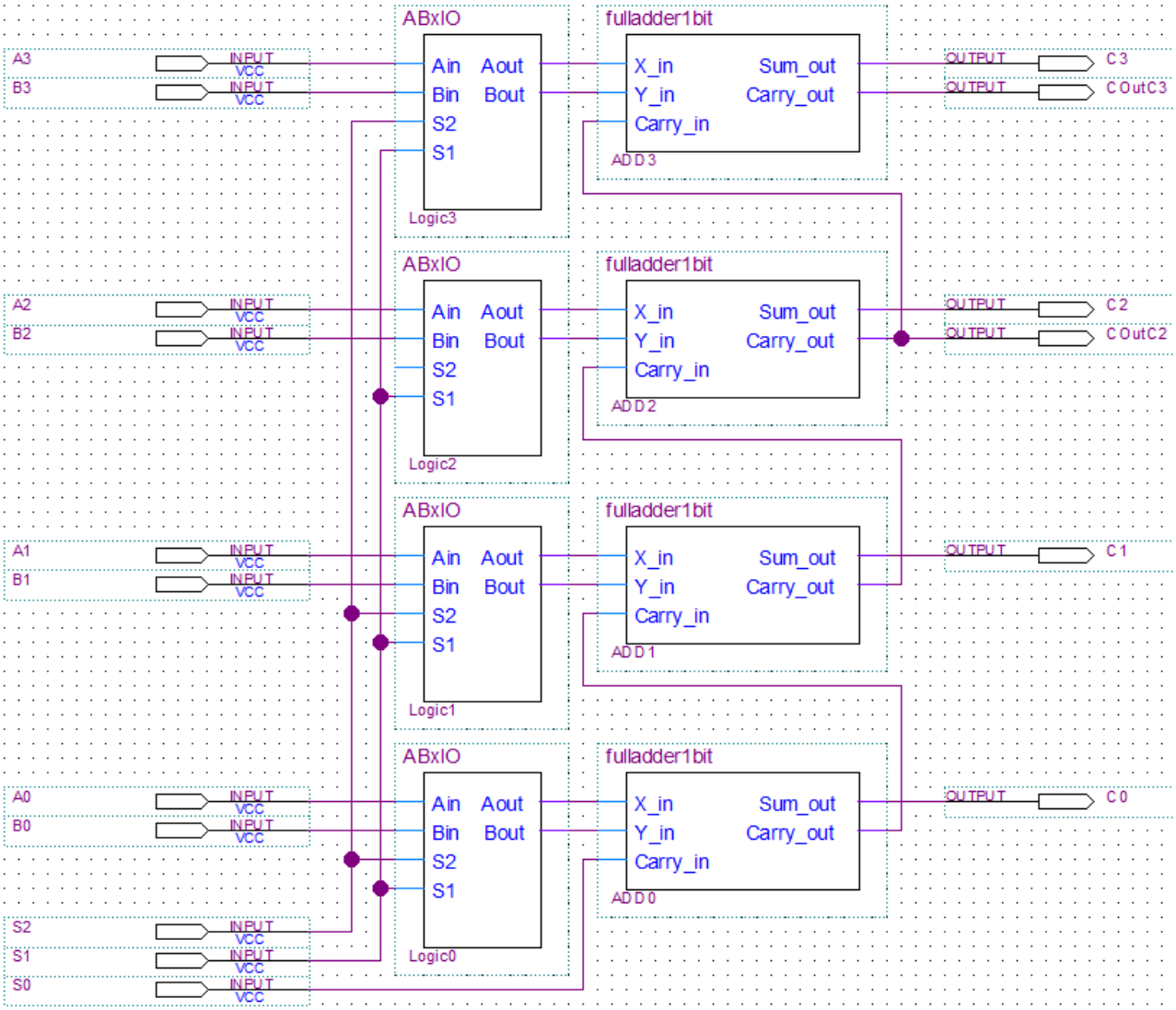


Figure 6: Four-Bit Arithmetic Circuit

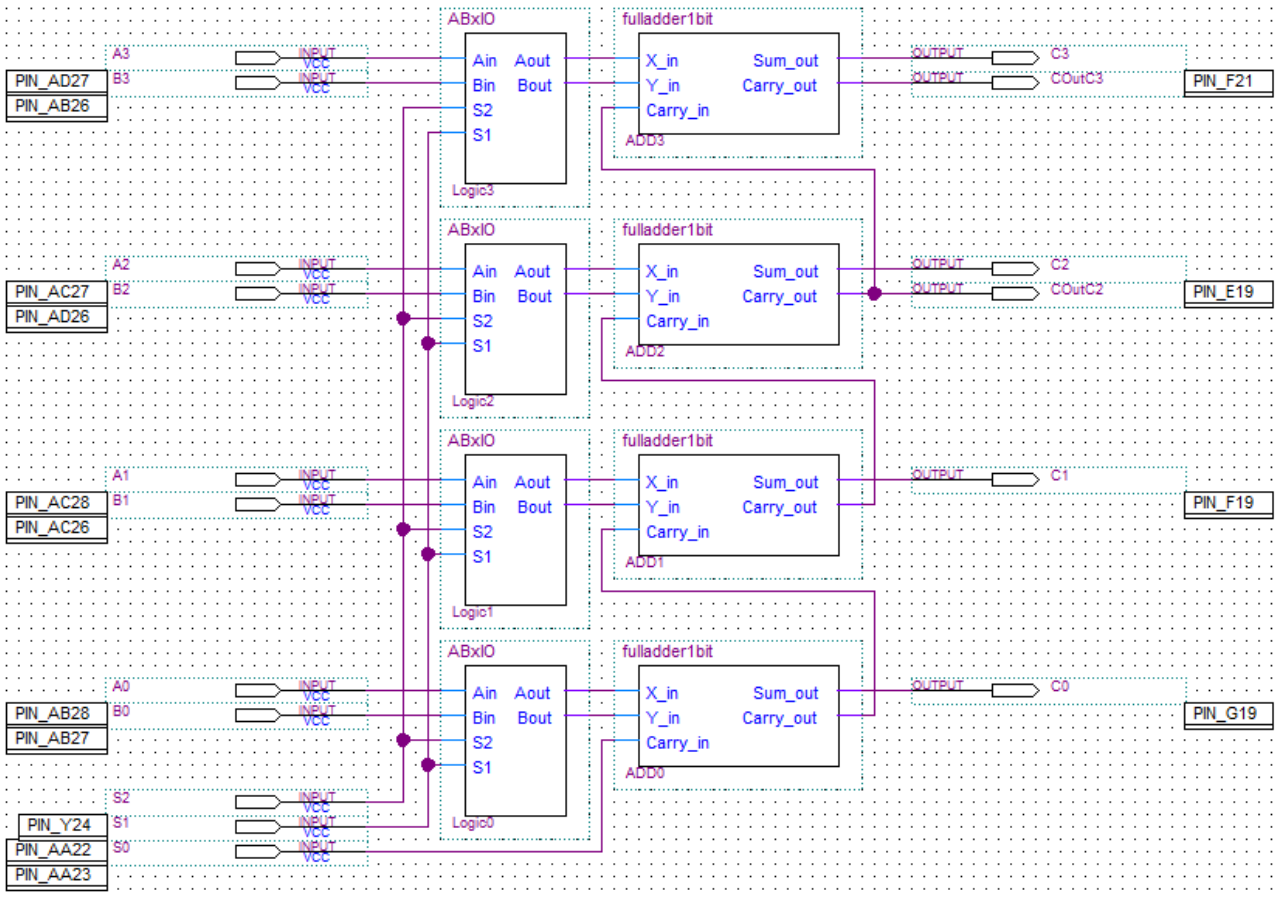


Figure 7: Second Iteration of the Four-Bit Arithmetic Circuit

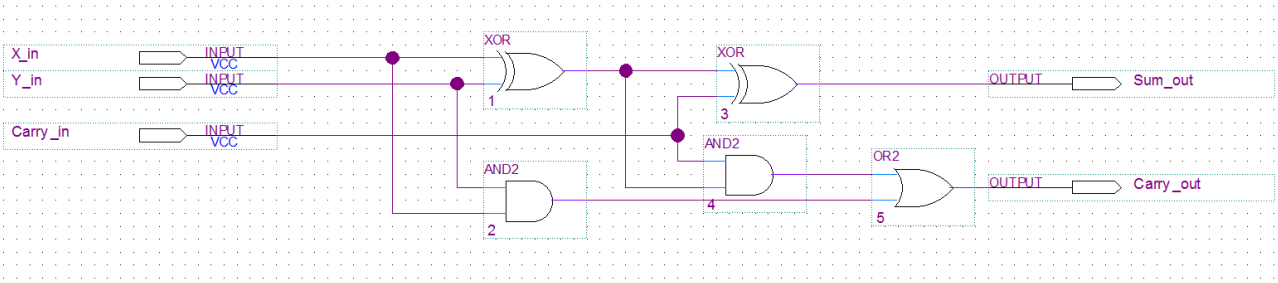


Figure 8: Full Adder

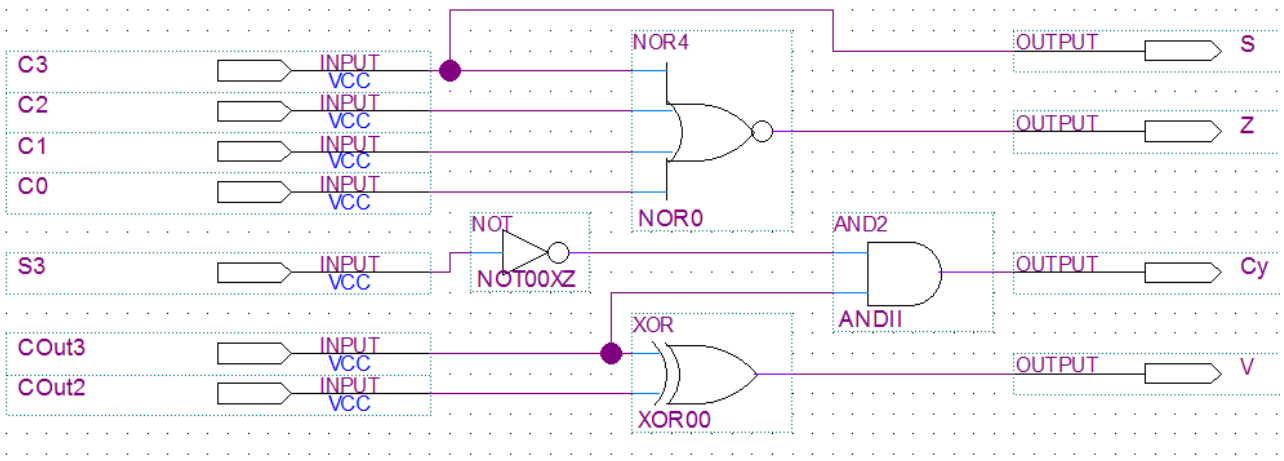


Figure 9: Status Indicator Circuit

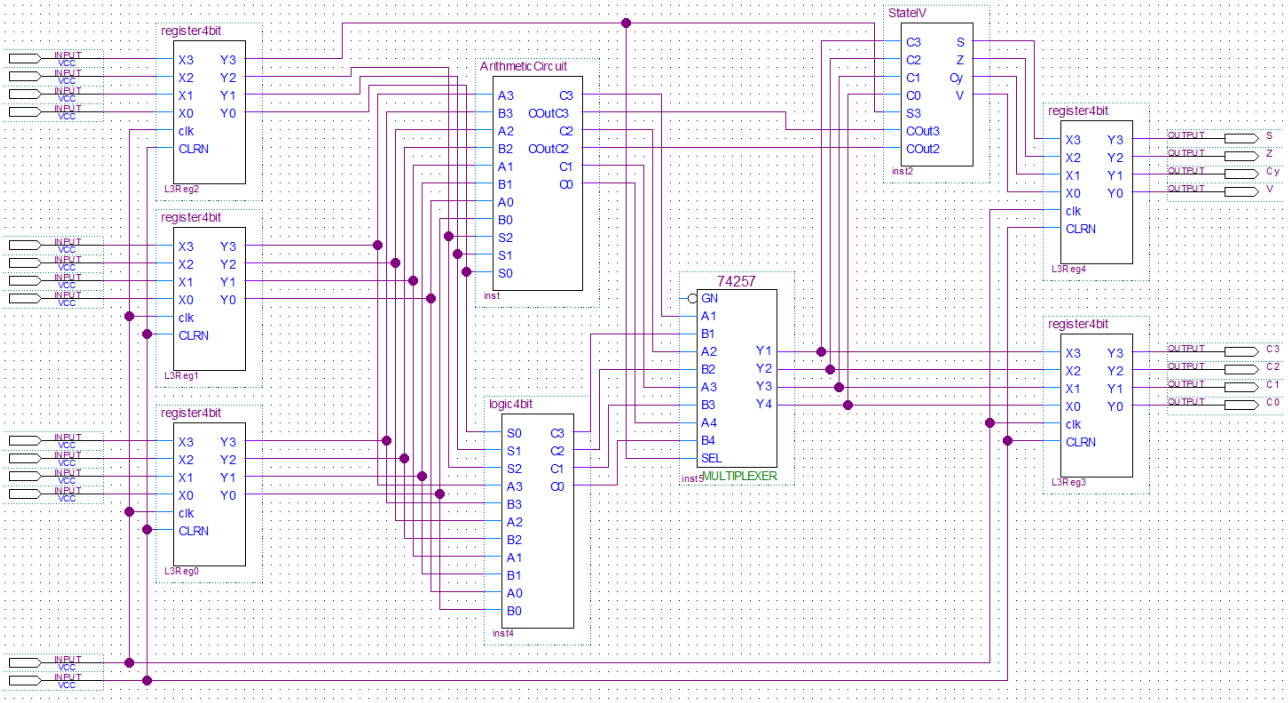


Figure 10: ALU

## 2.2 Implemented Solution

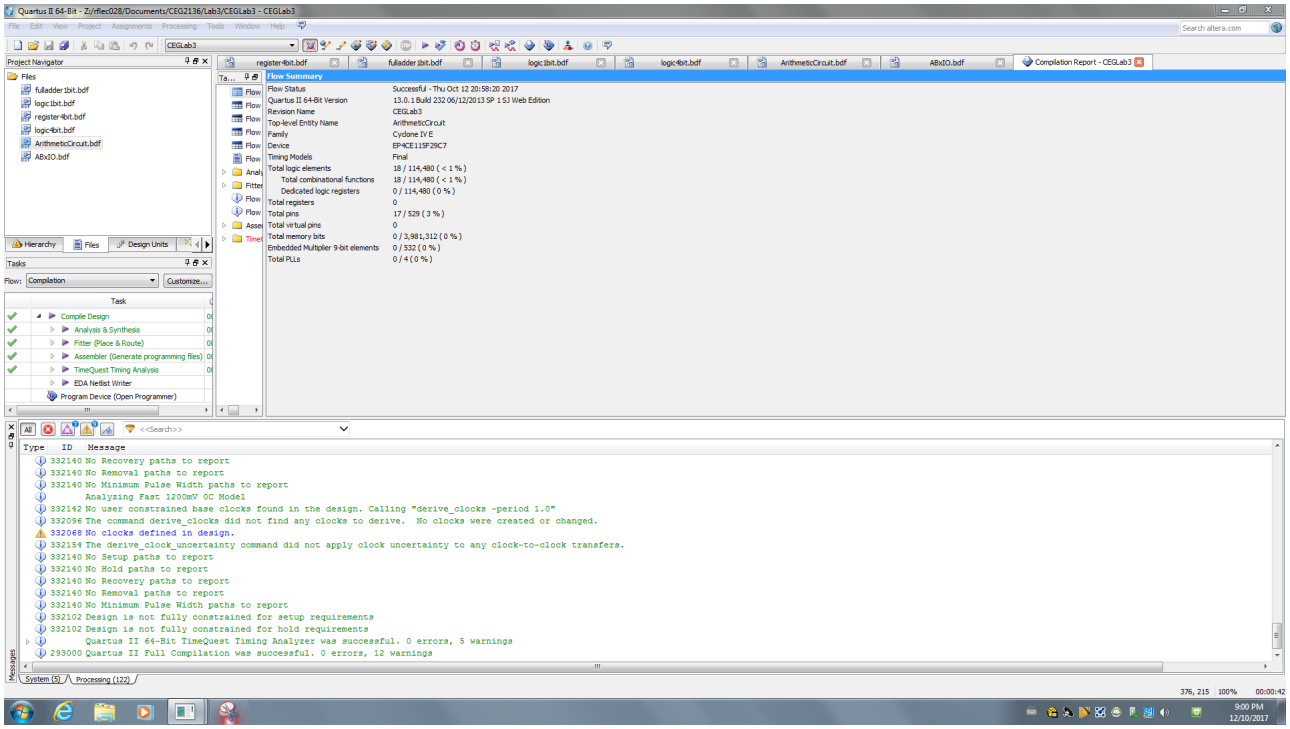


Figure 11: Successful Compilation

## 2.3 Challenging Problems Encountered

# 3 Implementation

As seen in Figure 10, our fully implemented ALU, we were able to successfully design and connect all of the lower-level circuits to create a functional final product.

## 3.1 Simulation Results

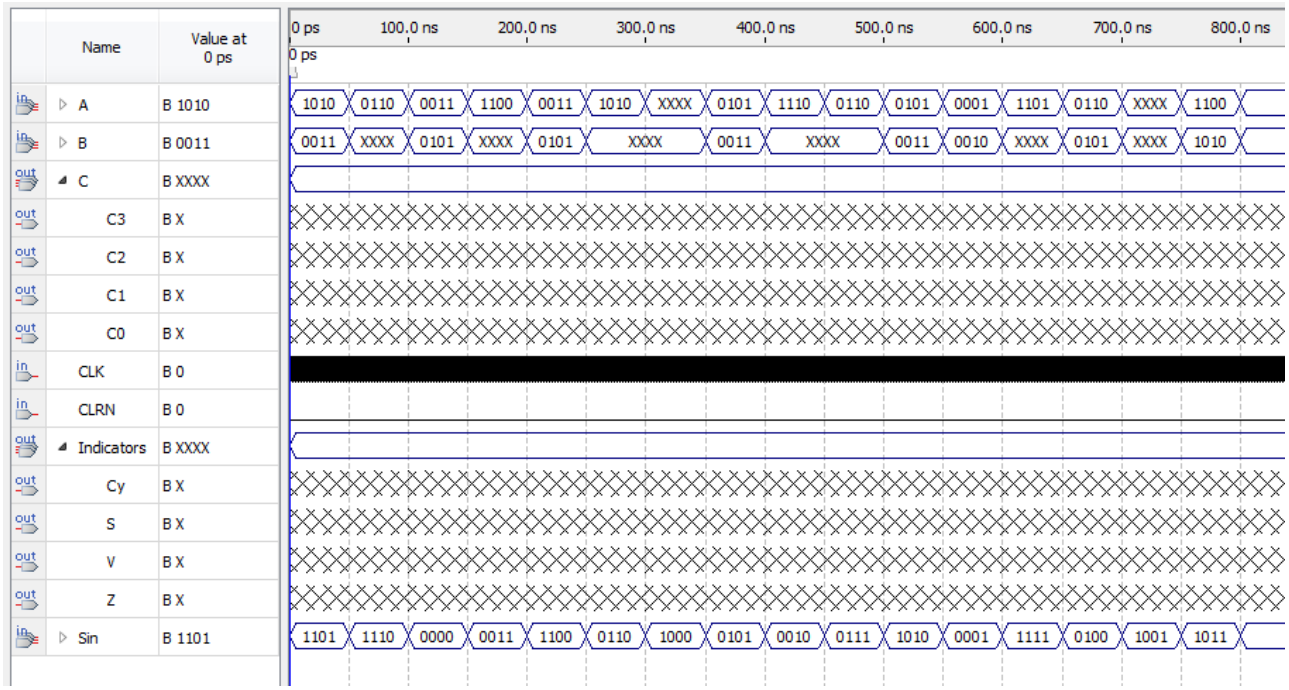


Figure 12: Complete Waveform File and Failed Waveform Generation

# 4 Design And Implementation Log

1. When performing the prelab...

# 5 Discussion

## 5.1 Errors Encountered

## 5.2 Conclusions