Sky1\_CGC\_Testplan

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Room13101, Building 13, No.498 Guoshoujing Road, Pudong District, Shanghai, China

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# Plan owners

|  |  |
| --- | --- |
| Role | Owner |
| Scoping Plan Author | Ryan |
| SOC Arch | Fan Ding |
| SOC designer | Zhongwen Wang |
| Test plan implementor | Ryan Huang |

# Overview

CGC Design Overview(TBD)

## PLLs

S5 domain PLLs are inside of PMCTRL\_S5, other PLLs are located in SMU\_PM clock controller, including PLL setting registers, root gating registers, PLL instances and CLOCK MUX, we are using pll\_wrapper to handle it.

PLL registers can be accessed by SE/PM/AP secure masters.

non-CPU/GPU PLL wrapper

Diagram

Description automatically generated

CPU/GPU wrapper

Diagram

Description automatically generated

FoutVCO = FREF(24M) \*(fbdiv + frac/2^24) / refdiv;

FoutPostDIV = FoutVCO/(postdiv1 \* postdiv2??)

We have below PLLs in SKY1 SOC.

1. Dsu\_pll(SCLK)
2. Cpu\_pll[4:0](CORE11:0]\_CLK);
3. Cpu\_pll\_800M;
4. System\_pll(400M), for SMN NI-700 and RCSUs.
5. Mmhub\_pll(max 1G);
6. Dpu\_pll(100-700M)
7. Npu\_pll(100-1300M)
8. Isp\_pll(100-1200M)
9. Vpu\_clk(?)
10. Gpupll\_top(350-1100M)
11. Gpupll\_core(350-1100M)
12. Ci700\_pll(2G)
13. Pcie\_axi\_pll(1G)
14. Pcie\_phy\_pll
15. Syshub\_pll(500M)
16. Pll\_s4\_800M(not present in CSU\_PM)

# Scope of Plan

## What this testplan is intended to cover

1. All internal CSU\_PM subsystem IPs’ access, including SRAM/Mailbox/Timer/I2C/WDT/SOC PLLs/DMA-350/PVT\_CNTL/GPIO/UART;

**List host here:**

1. Outsides SMN requests to other Ips with Secure/NonSecure requests.
2. SysHub DMA access to DRAM paths with TLB configuration.
3. Internal AEB/Security fencing/AEB features.
4. Most of the sequences will include positive and negative sequences, interrupts will be enabled as well.
5. PM power feature.
6. Debug bus signal toggles.

## What this testplan is NOT intended to cover

1. DFT TDR testing involves Jtag TAP master/Slave would be covered by SOC DFT testplan.
2. DFD coresight or debug bus testing would be covered CSU\_PM DFD sub testplan. [callout with DFD]
3. Outside of CSU\_PM SMN/DMA access would be covered in CSU\_PM deployment testplan or SOC PM testplan.
4. PM firmware authorization, loading and execution would be tested in SOC security testplan or EMU/FGPA.
5. All Reset related sequences would be covered by SE or SOC bootflow testing.
6. Security gasket SMN testing with different Lifecycles would be tested in SOC security Testplan.
7. AEB control and Override is covered in CSU\_SE TP.

# Verification Methodology

## Configuration

csu\_tb: all the CSU\_PM subsystem Ips are presented with RTL view, other IPs will be UVCs.

## Stimulus generation

1. LX7 core based sequences based on SW codes to send core request with/without DMA access.
2. Using CSU\_PM UVM(TestPort to send requests through NIC450)

## Checker

1. Case self-check to make sure register access or SRAM access are done correctly.
2. Case self-check to make sure the sequence or violations are generated correctly.
3. Backdoor checker will also be injected into cases.
4. Turn on all Subsystem checker/assertions if present.
5. [Jason] add clock-frequency checker from Rock.

## Coverage

1. External Interfaces coverage should be all toggled. (DMA/SMN)
2. Internal Interfaces coverage should be all toggled as well.

(SRAM/Mailbox/Timer/I2C/WDT/SytemPLL/DMA-350/PVT\_CNTL/GPIO/UART).

1. Function coverage will be added if needed.

# Test Scenarios

Reference to DR\_VR table.

# Meeting notes