

amba router

[specification]

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1. purpose

This design is created just for creating UVM based examples, so the application of this design is non sense.

1. features

* support apb4 interface to receive register configurations, this block works in 200MHz.
* supports ahb5 interface to receive requests, and will be stored in a fifo.
* exec unit is configured by register unit and will fetch requests from the fifo and send out.
* support 4 output request ports by this design to select which one to deliver the stored requests
* each request port is just a simple set of self-defined, address/data interfaces
  1. regUnit

this unit will receive apb4 write request and store the information into reg signals and giving it out to execUnit.

configurable features

* indicate the start of execUnit
* selectable priority of output
* TODO
  1. rcvUnit

The rcvUnit is going to receive requests from an AHB5 bus, and stores them and waiting for execUnit to fetch.

* 1. execUnit

Which is an executing unit to get configurations from regUnit and going to fetch the requests from rcvUnit, and then send it to downstream ports according to an arbitrator.

* starts fetch requests after has an input start level signal (iActive).
* supports maximum 4 downstream ports
* configurable priority of each port, the larger value, the higher priority.

1. implementation
   1. downstream port protocol

* Clk, the sample clock
* reqValid, the valid signal of request asserted by initiator
* reqCmd, the command signal contains address/rw/data information.
  1. regUnit
     1. apbIf

The apbIf module to receive and process the apb register request and translated to simple register control signals (which has VALID/ADDR/RW/WDATA/RDATA).

* + 1. regBlock

A module to receive register control and give out corresponding control signals or reg read data.

* 1. rcvUnit
     1. ahbIf

This module will process ahb requests, then converts these commands into a packet and stores into fifo. In current design, for easy development, this module support ahb write only. Every kind of read will respond an error to the bus.

* + 1. fifoInst

FIFO to store commands, and wait for execUnit to fetch the commands.

* 1. execUnit