CMOS Inverter

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Introduction and Physical Properties

Cell Description

An inverter is a logic gate that produces a high output when the input is low, and a low output when the input is high. This CMOS inverter is made up of two MOSFETs. The top one is a PMOS, and the bottom one is an NMOS. These inverters are a valuable building block for digital ICs and other computer systems today due to their high speed, low power dissipation, and high noise margins.

Cell Symbol

This is the symbol for the CMOS inverter created and used by Cadence. Port A is the input. Port Y is the output.

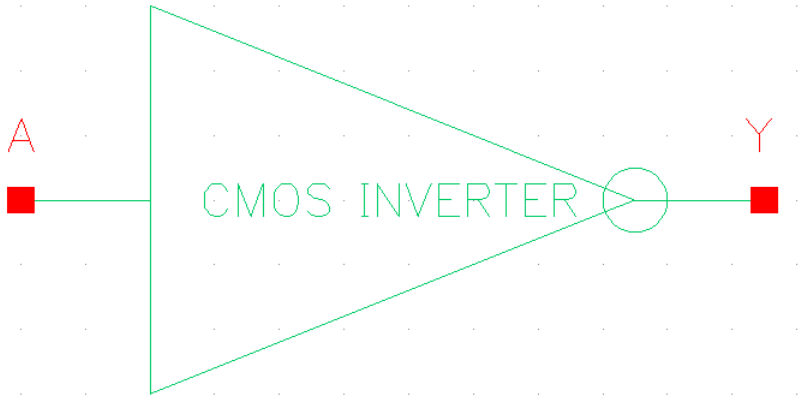


Figure 1: CMOS Inverter symbol from Cadence Virtuoso.

Cell Truth Table

Cell Truth Table	
Cell Inputs {0,1}	Cell Outputs {L,H}
0	H
1	L

Cell Schematic Diagram

Figure 2 is the schematic of the CMOS inverter behind the symbol. The PMOS is on top connected to Vdd. The NMOS is on the bottom connected to ground. Port A is the input. Port Y is the output.

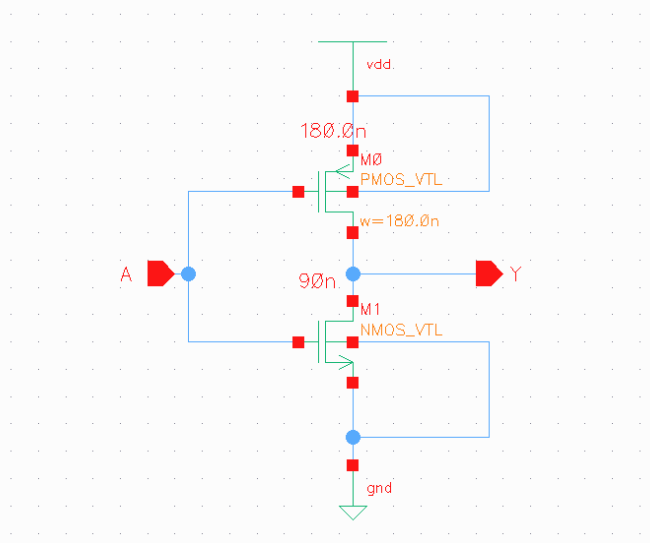


Figure 2: CMOS inverter schematic.

Cell Layout Diagram and Dimensions

Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
M0 (PMOS)	50nm	180nm
M1 (NMOS)	50nm	90nm

CMOS Inverter PMOS and NMOS Width Variation Table					
DUT		**Rise/Fall and Delay Time (ps)**			
W_pmos	**W_nmos**	**Tr**	**Tf**	**Tplh**	**Tphl**
90	90	33. 5	18.7	34.9	13.5
135	90	26.0	18.9	27.7	14.5
180	90	23.6	19.2	23.6	15.9

The inverter design started with both the PMOS and NMOS width of 90nm. Simulations were run with the PMOS width increasing by increments of 45nm while fixing the NMOS width at 90nm. The goal was to achieve rise and fall times at the output of less than 30ps, and propagation delays less than 40ps at both edges, with a fanout load of 4 inverters. Although the 135nm width was in spec, we chose the highlighted widths above of 180nm. The performance is better with this sizing across all loads and brings the rise time into spec at FO8 as well.

Performance Analysis

Rise and Fall Times

The propagation delays and transition times for our CMOS inverter were measured with 5 different output loads FOx, where x denotes the number of identical CMOS inverters connected to its output. The load inverters had both PMOS and NMOS with width of 90nm and length of 50n, and a 15fF capacitor at each output. The FO0 simulation was done with only a 15fF capacitor to ground at the output. The transition times were measured between 20% and 80%. The delay measurements were taken from the 600mV crossing point of each edge. The input pulse was a 5ns, 1.2V pulse with a 50ps rise time and a 50ps fall time.

Output Rise Time Data t_r (ps)

Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	187.0.0	16.6	18.9	23.6	31.5

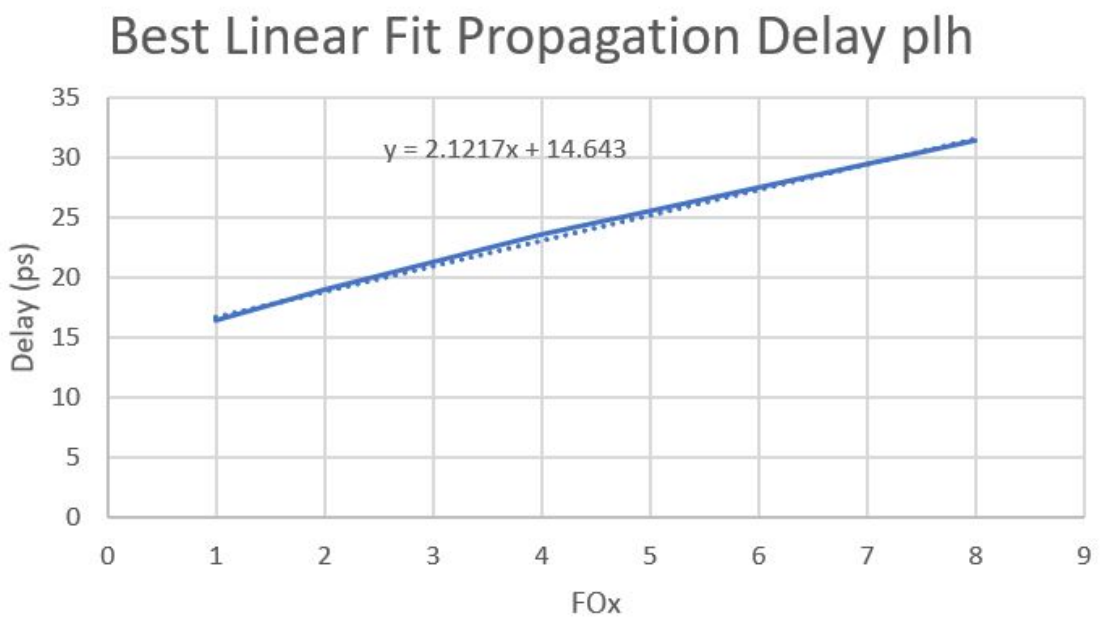
Output Fall Time Data t_f (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	118.0	14.7	16.2	19.2	24.7

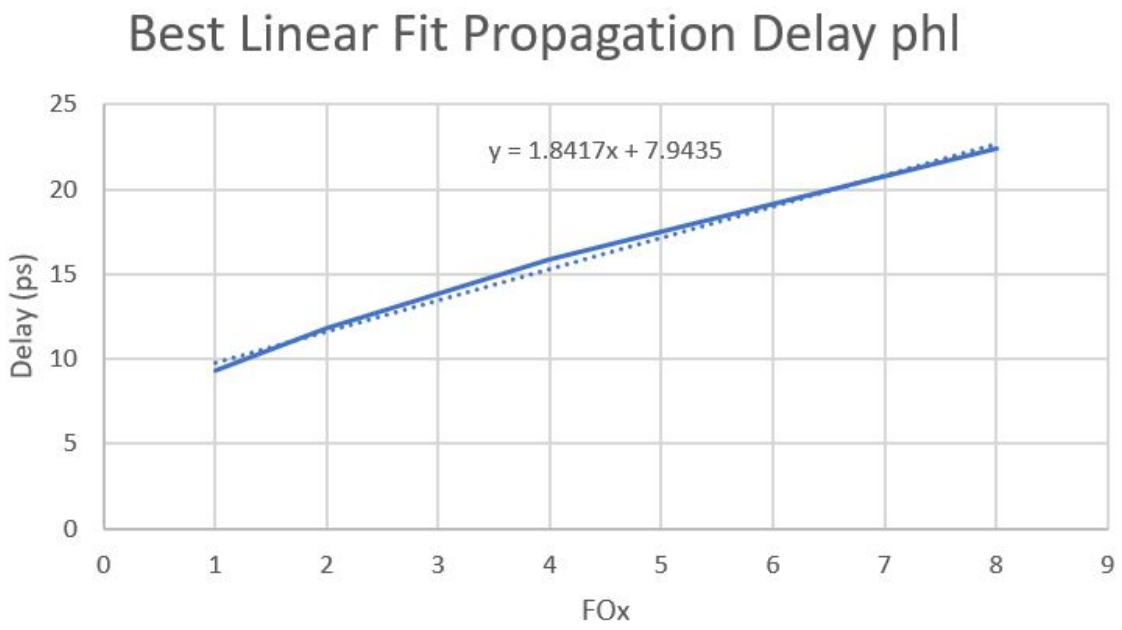
Propagation Delays

A best fit linear equation was computed to predict the propagation delays at different loads. The no load values for both edges were omitted as outliers for this calculation.

Data Worst Case Low to High Propagation Delay Data t_{plh} (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	137.9	16.4	19.0	23.6	31.4

Data Worst Case High to Low Propagation Delay Data t_{phl} (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	110.5	9.3	11.8	15.9	22.4





Each member did the entire lab independently and compared results. The results were collaboratively edited to these two reports.

Appendix

This appendix contains all the simulation plots for the CMOS inverter for all loads tested.

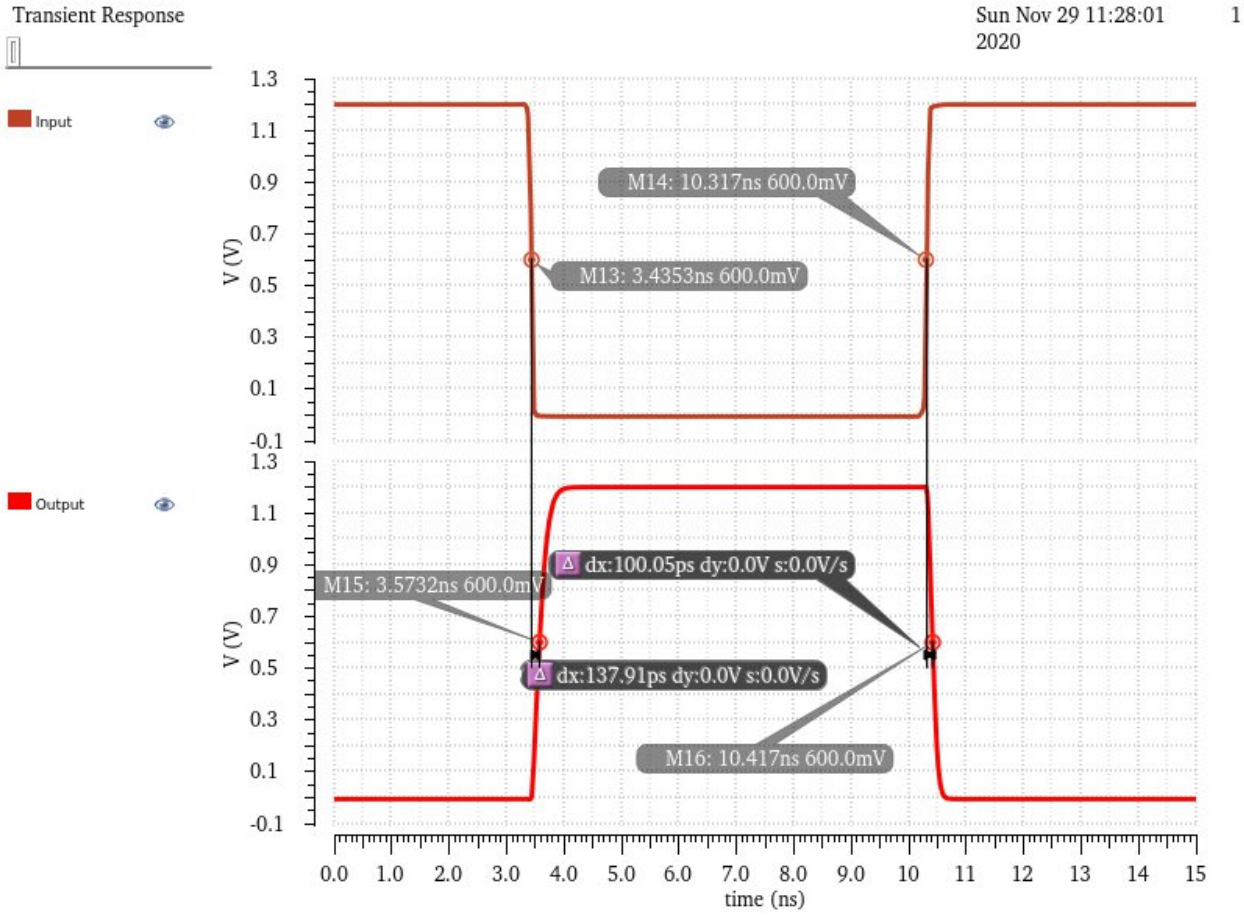


Figure 3: FO0 Delay plh = 137.9ps. phl = 100.0ps

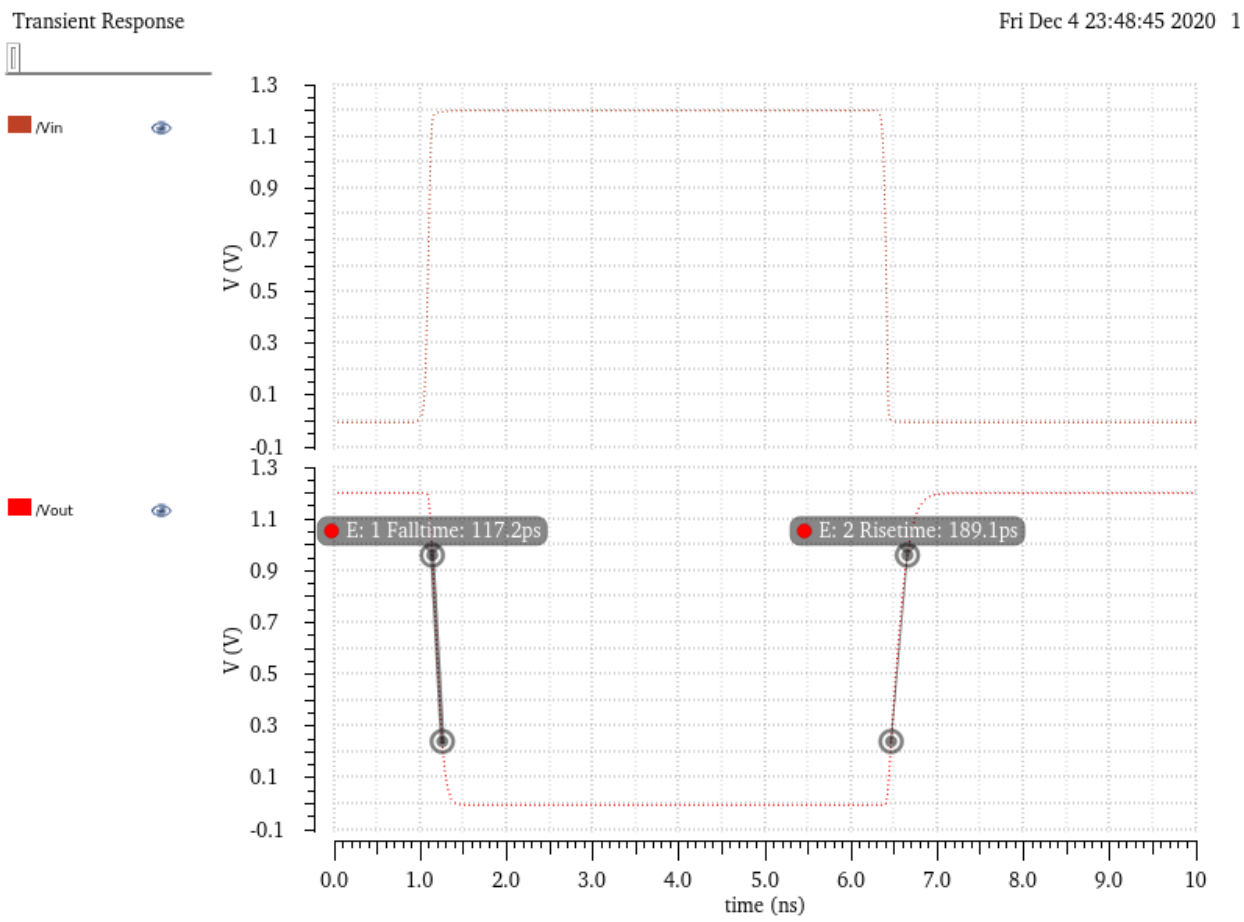


Figure 4: FO0 RiseTime/FallTime Tr = 189ps. Tf = 117ps

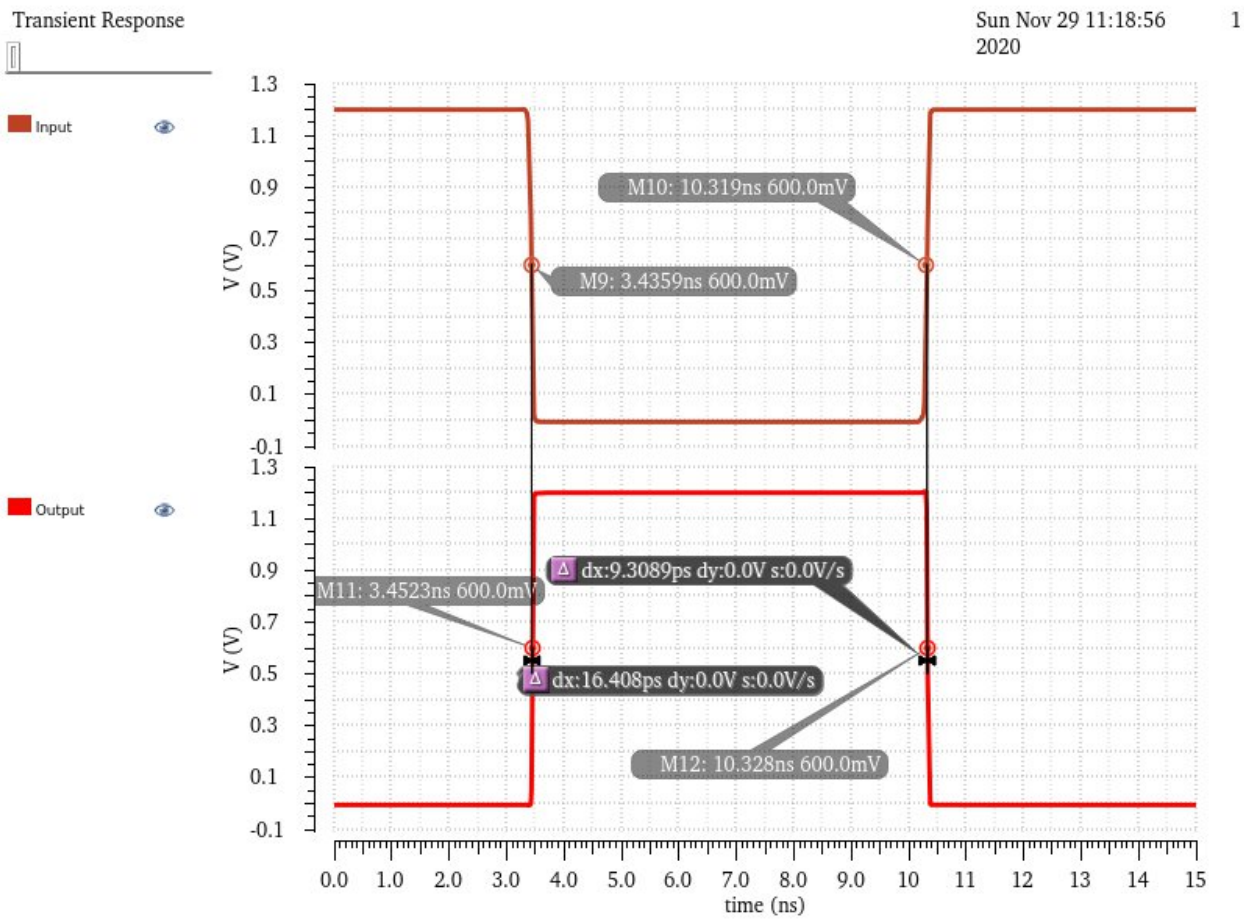


Figure 5: FO1 Delay plh = 16.4ps. phl = 9.3ps

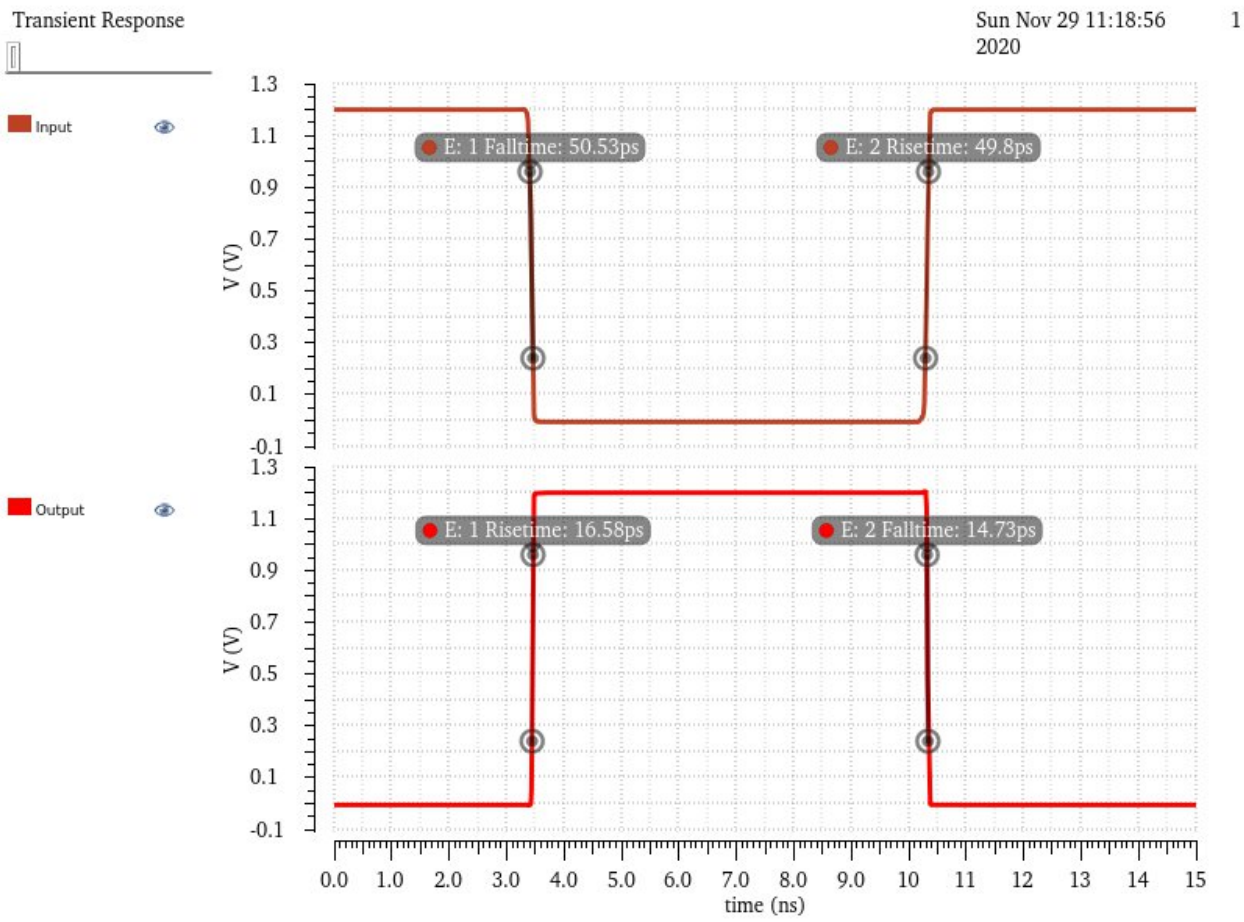


Figure 6: FO1 RiseTime/FallTime Tr = 16.58ps. Tf = 14.73ps

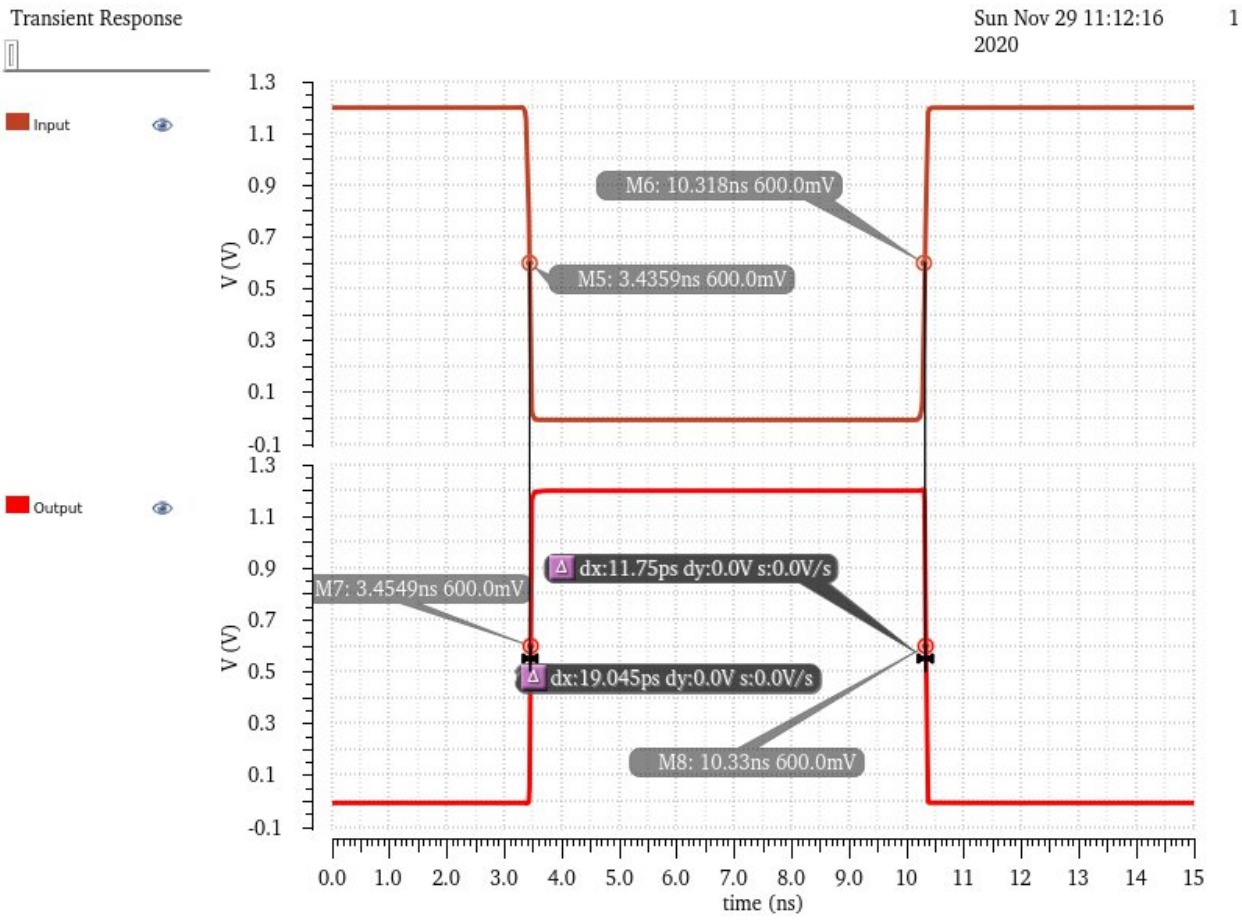


Figure 7: FO2 Delay plh = 19.0ps. phl = 11.7ps

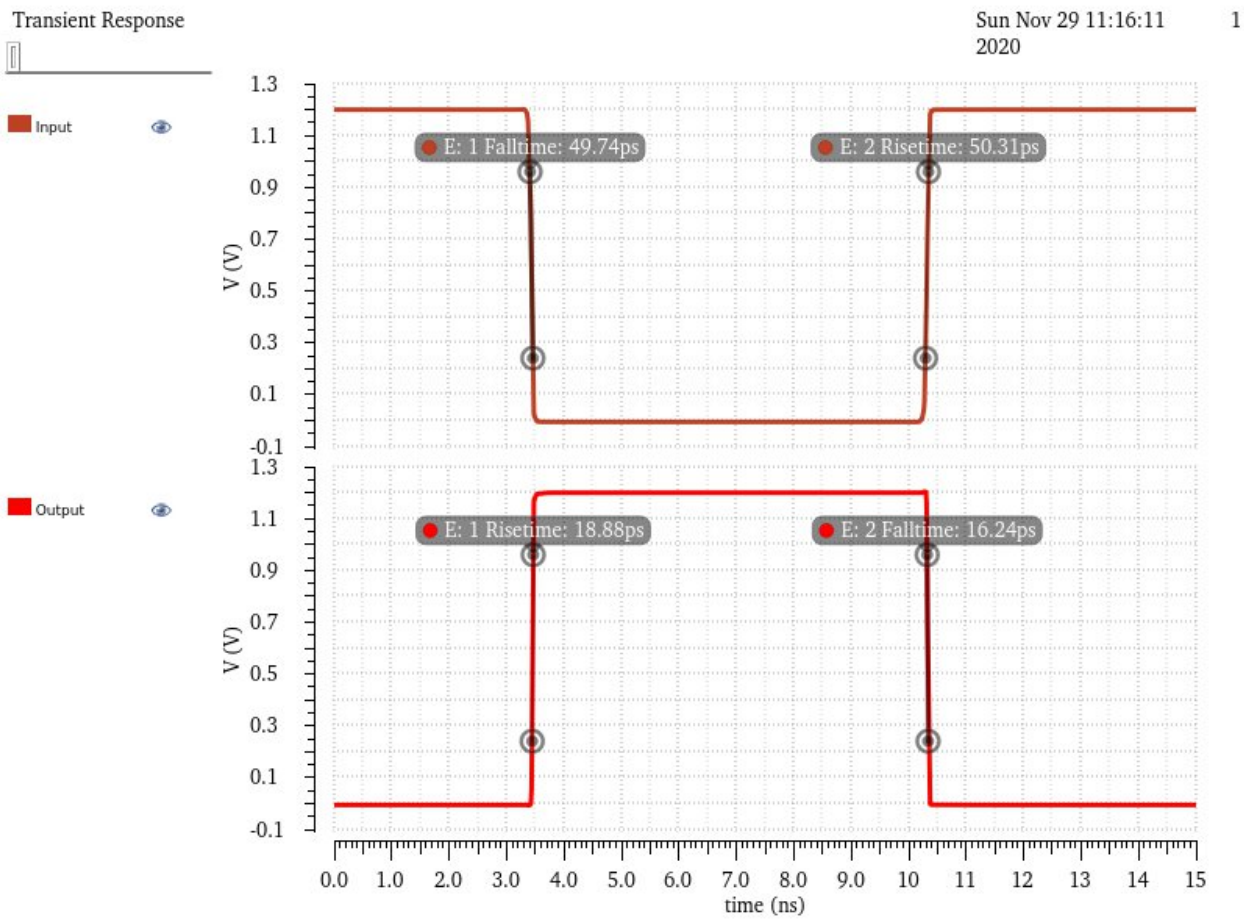


Figure 8: FO2 RiseTime/FallTime Tr = 18.9ps. Tf = 16.2ps

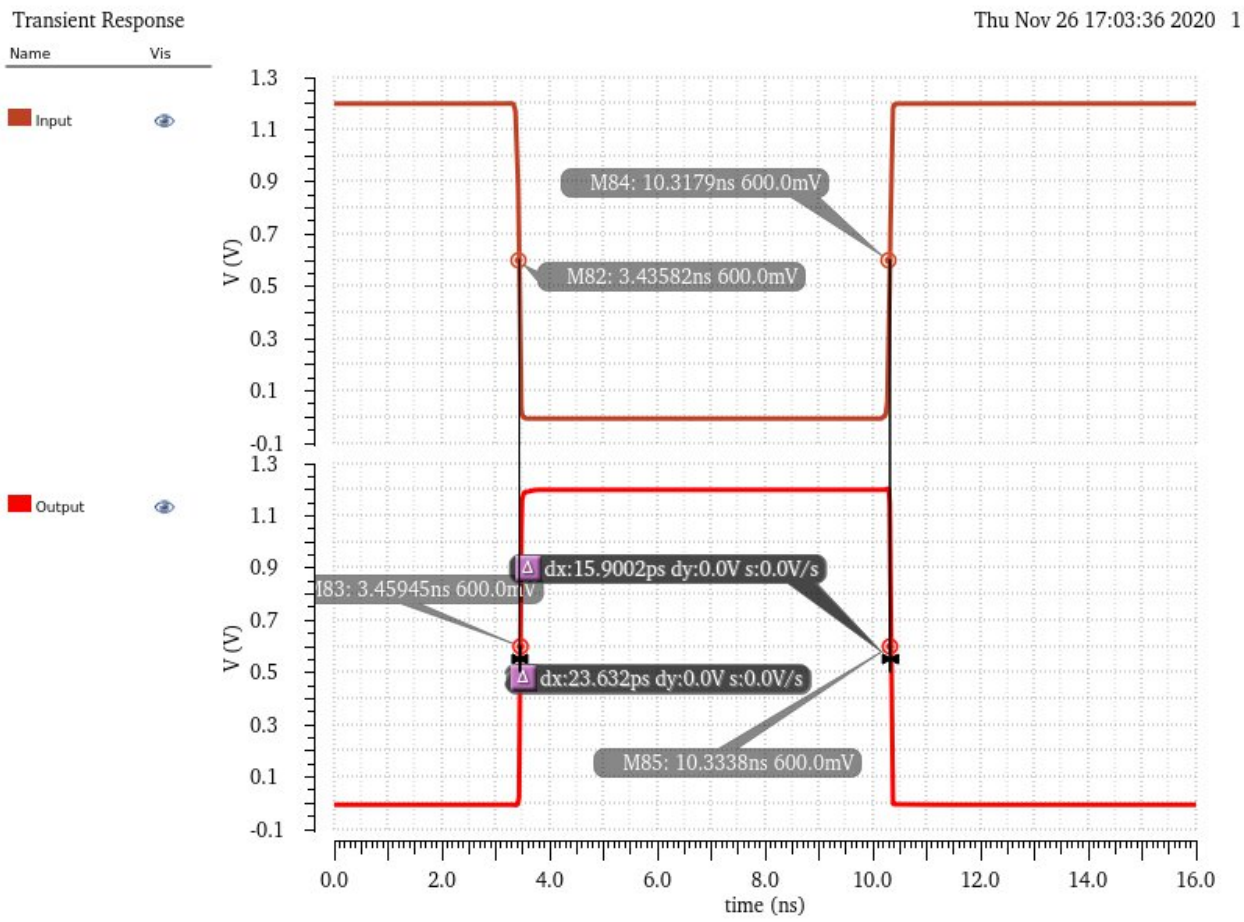


Figure 9: FO4 Delay plh = 23.6ps. phl = 15.9ps

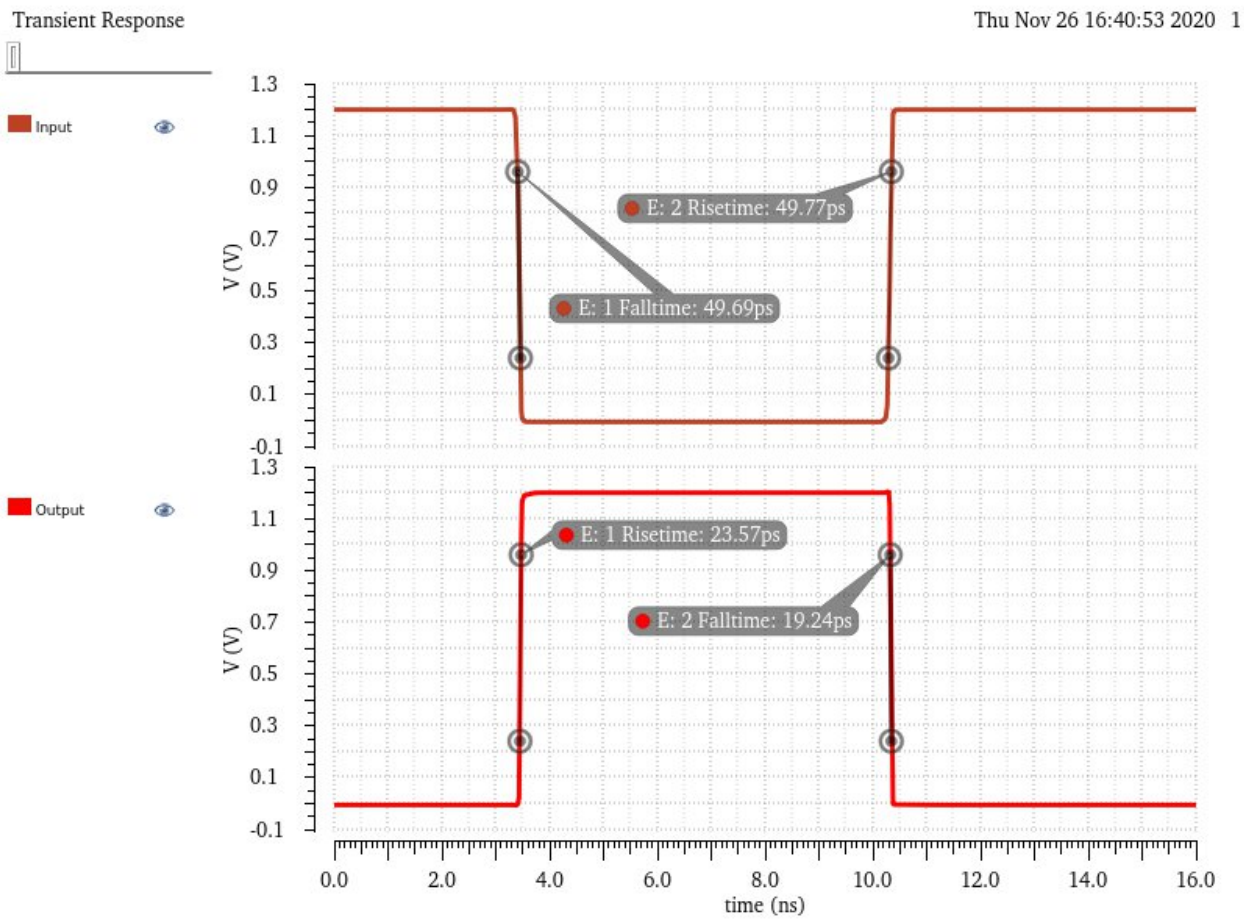


Figure 10: FO4 RiseTime/FallTime Tr = 23.7ps. Tf = 19.2ps

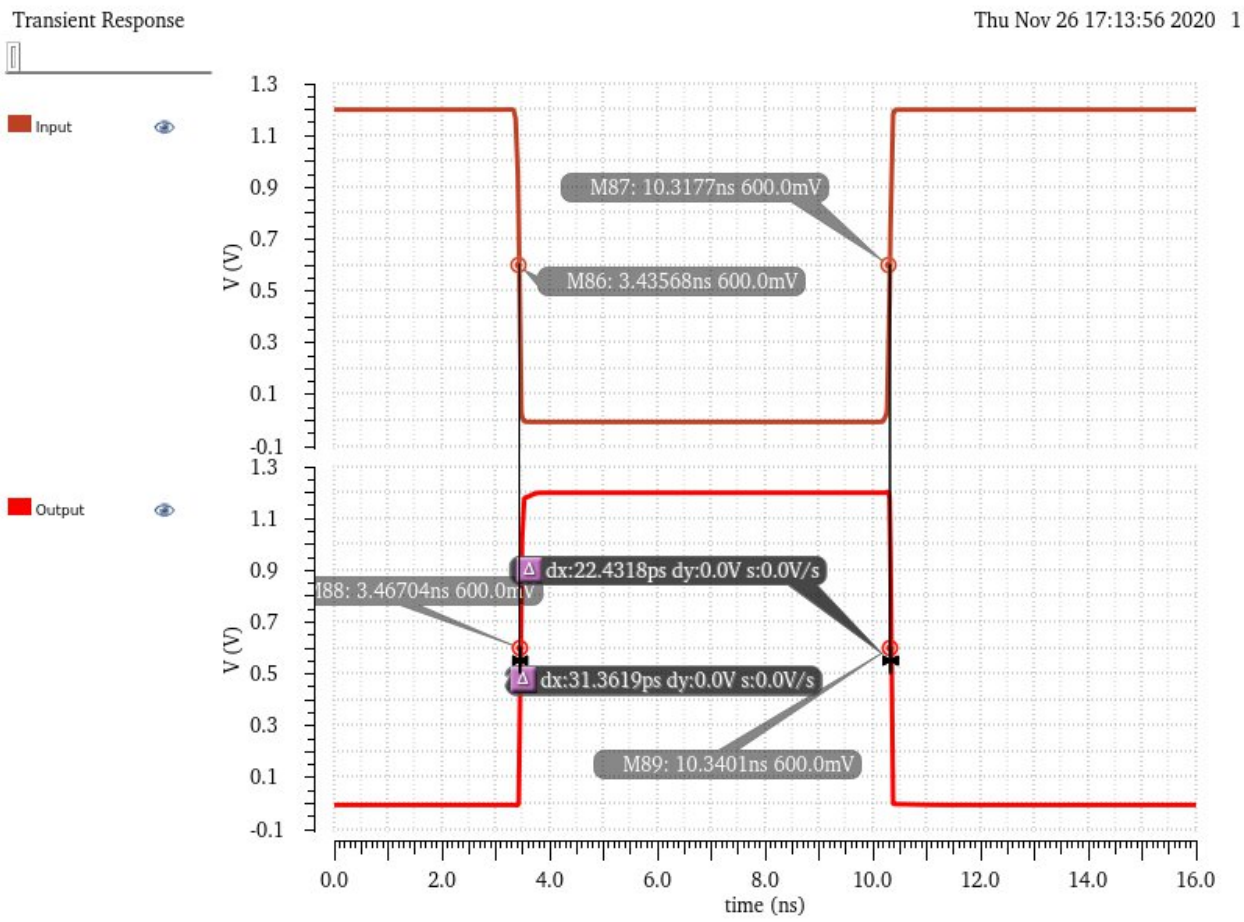


Figure 11: FO8 Delay plh = 31.4ps. phl = 22.4ps

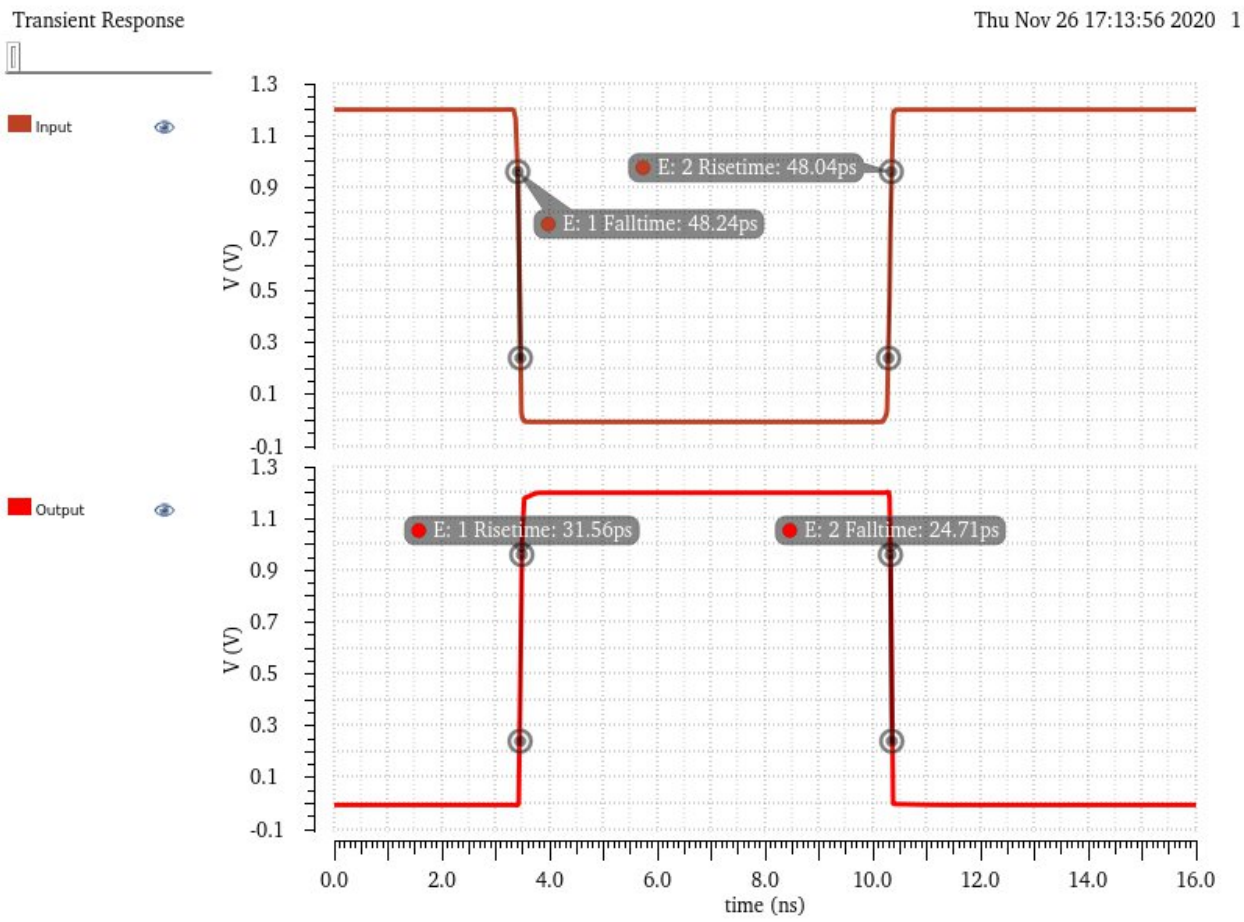


Figure 12: FO8 RiseTime/FallTime Tr = 31.5ps. Tf = 24.7ps

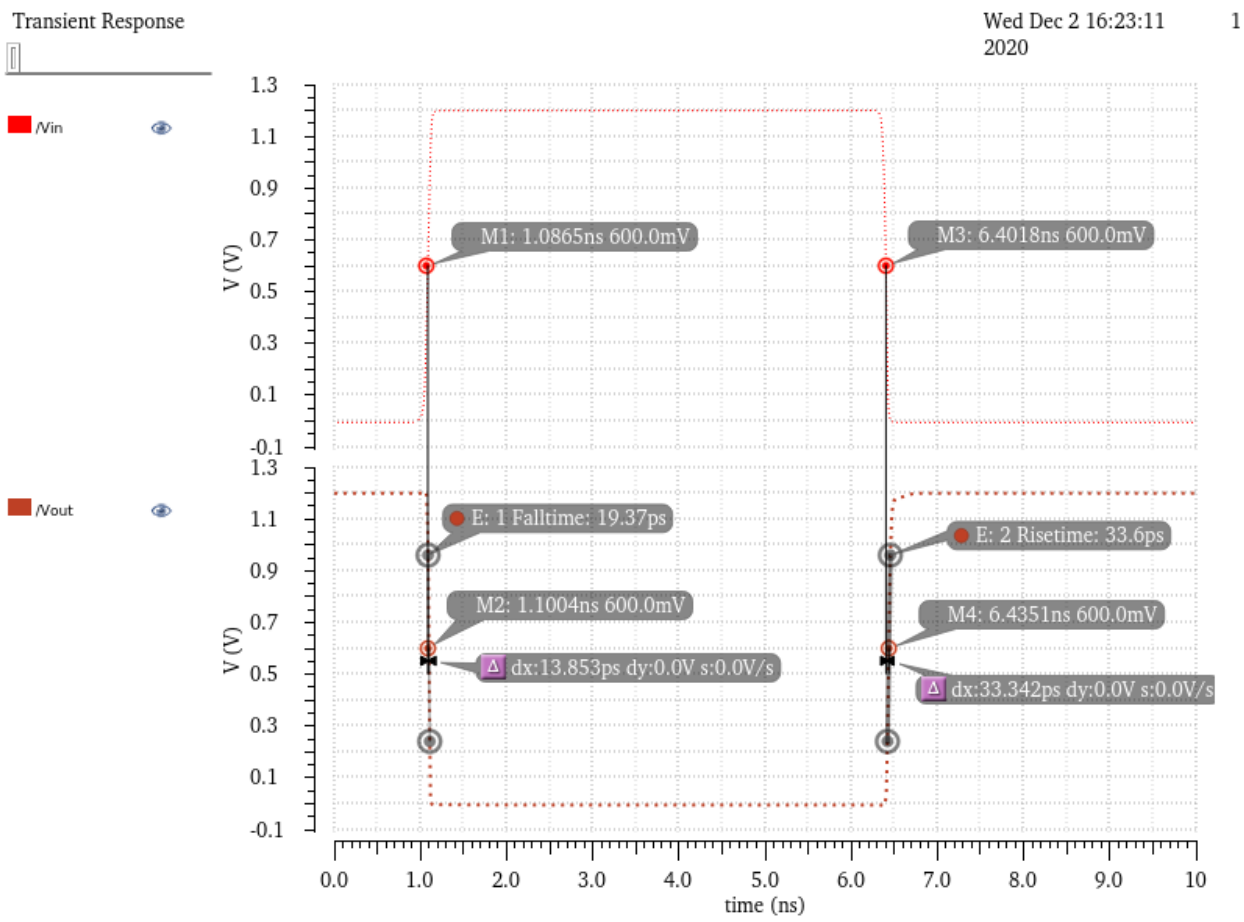


Figure 13: Transient Response for DUT (W_pmos = 90, W_nmos = 90) FO4 Load

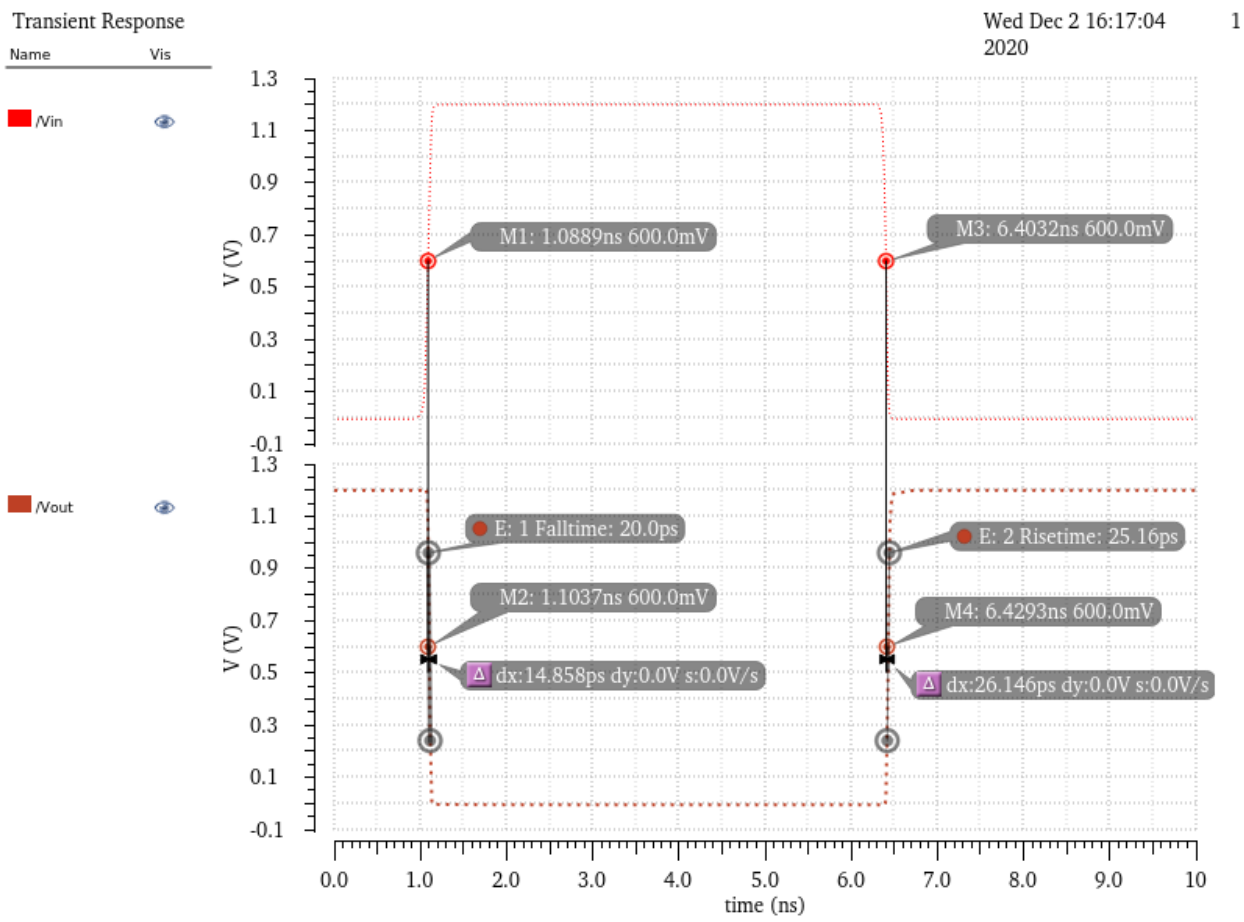


Figure 14: Transient Response for DUT (W_pmos = 135, W_nmos = 90) FO4 Load

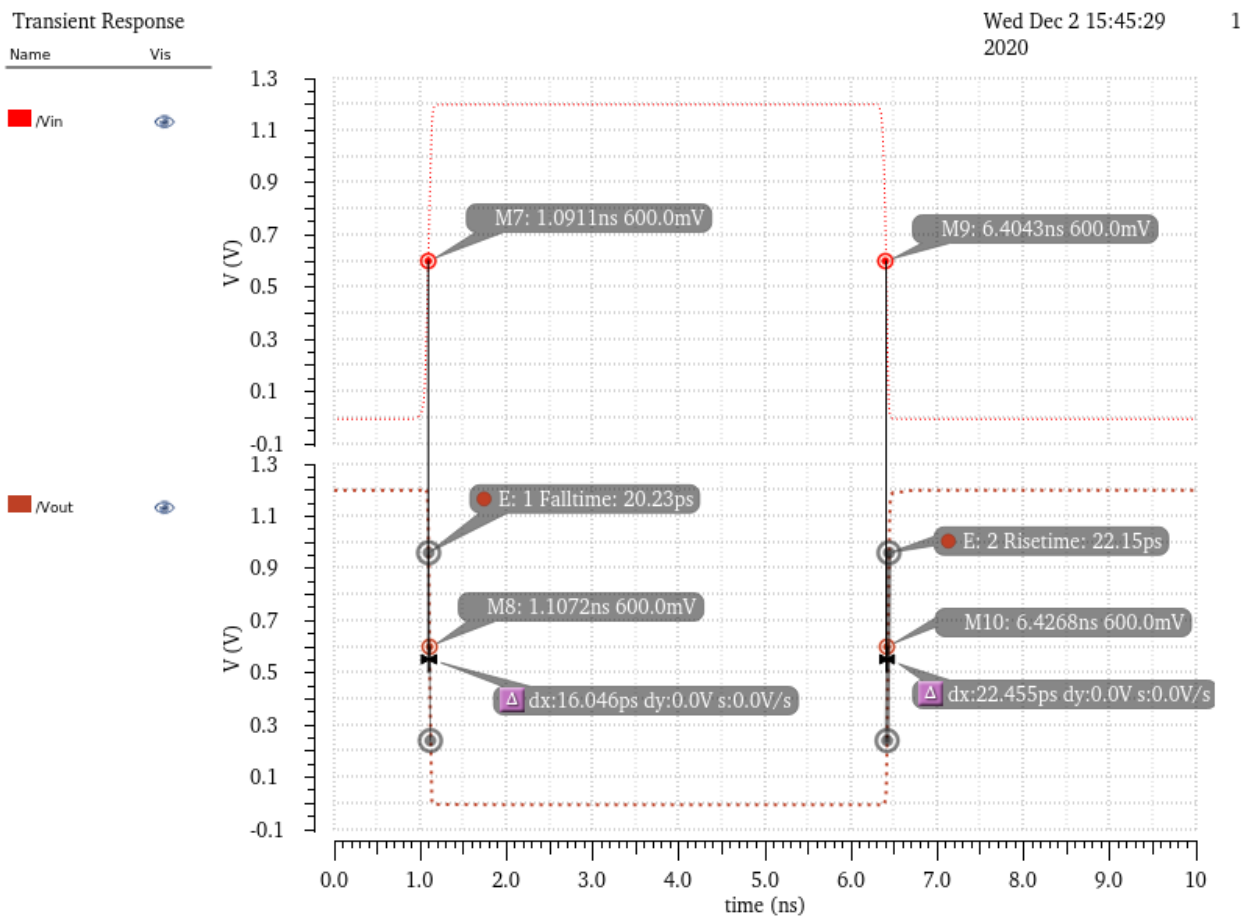


Figure 15: Transient Response for DUT (W_pmos = 180, W_nmos = 90) FO4 Load

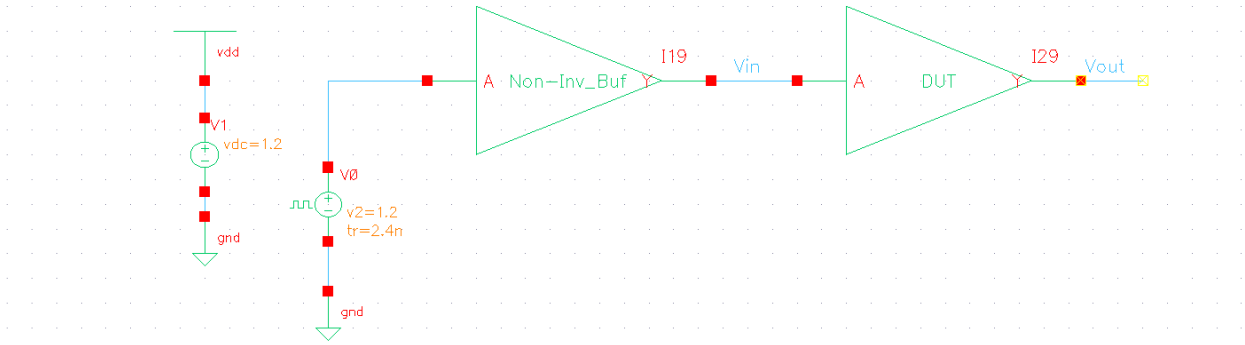


Figure 16: CMOS FO0 Inverter Schematic

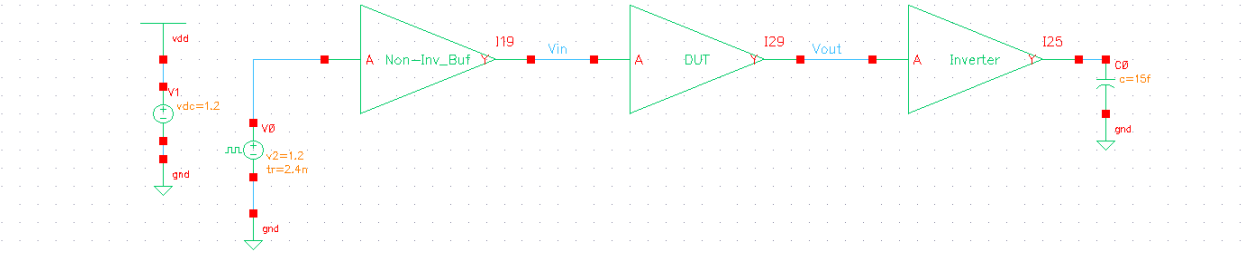


Figure 17: CMOS FO1 Inverter Schematic

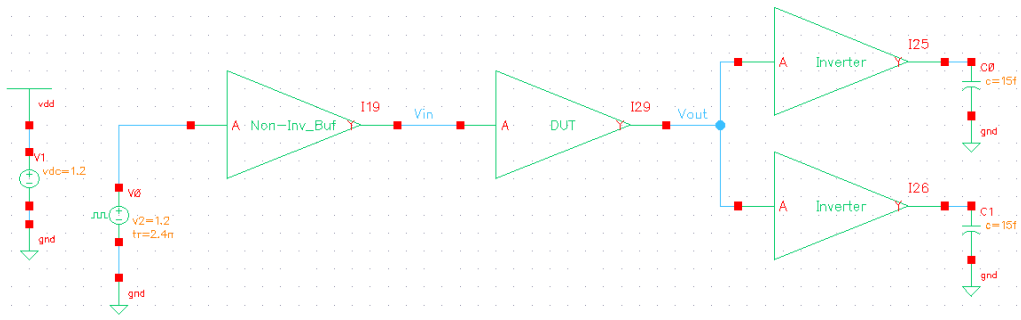


Figure 18: CMOS FO2 Inverter Schematic

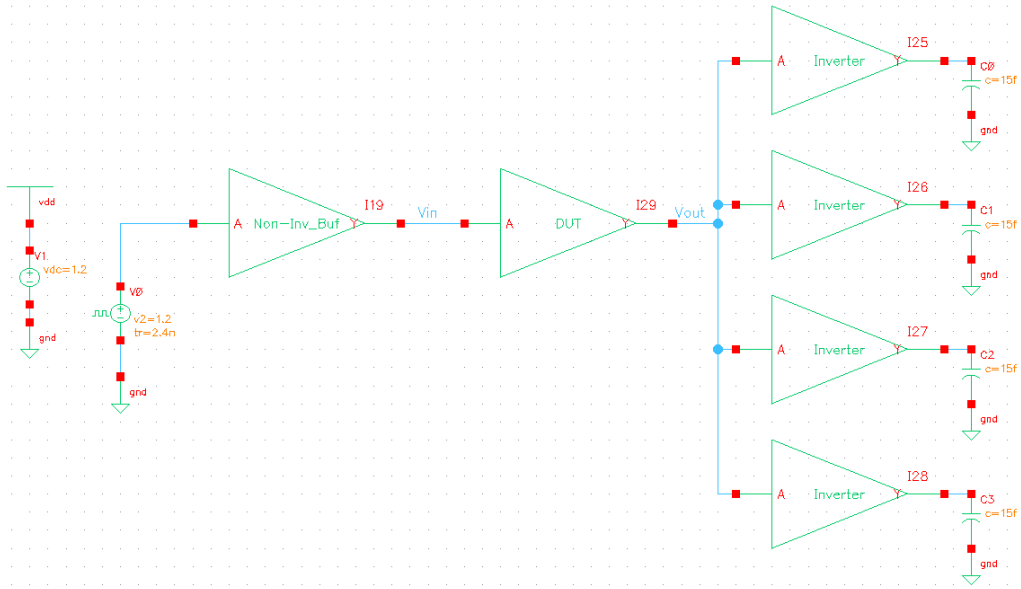


Figure 19: CMOS FO4 Inverter Schematic

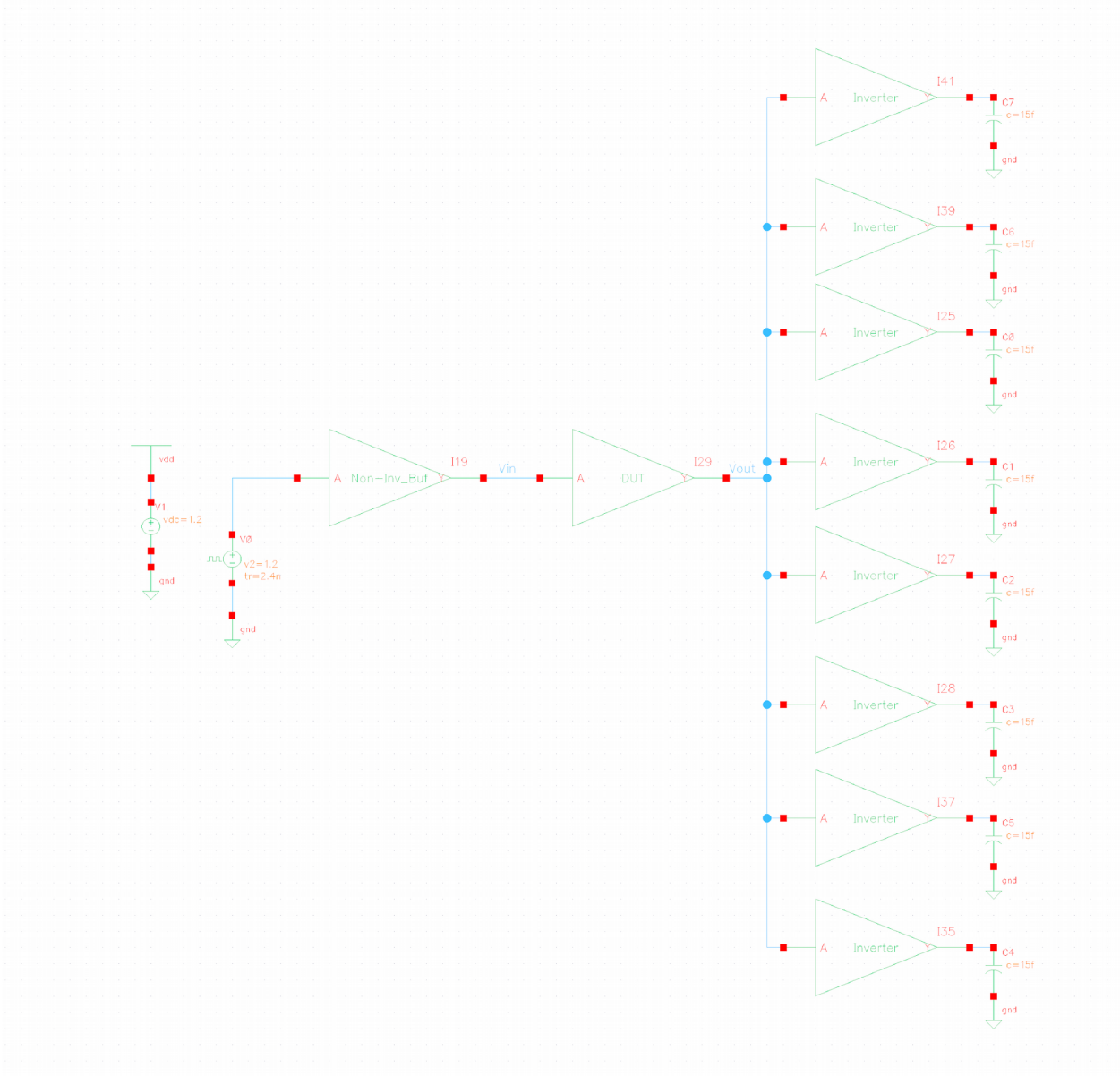


Figure 20: CMOS FO8 Inverter Schematic