Project 2

A "Mini" Op Amp

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Electronics II

Contents

List of Figures

1 Introduction

This project is about designing and simulating a "mini" op amp. We begin the design of the mini operational amplifier by separating the internal connections into stages. The stages typically are the input stage, gain stage, and the output stage. Further details will be in the design portion. The design will be using theoretical calculations and then afterwards there will be simulation using LTspice. Throughout the report there will discussions and comparisons of the findings as we move along. To make this report efficient in learning the concepts, derivations of calculations will not be provided in this report.

2 Part I: Differential Amplifier

The first stage or the input stage of the operational amplifier is the differential amplifier. Equations used in theory are below, followed by the schematic. Some of the equations will have exact theoretical calculations, followed by their respective approximations. A table at the end will summarize the findings.

Q-Point

$$I_C = \alpha_F \frac{V_{EE} - V_{BE}}{2R_{EE}} \approx \frac{V_{EE} - V_{BE}}{2R_{EE}} \tag{1}$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C \tag{2}$$

Differential Mode Gain

$$A_{dd} = g_m R_C \tag{3}$$

$$A_{single} = \frac{-g_m R_C}{2} \tag{4}$$

where

$$g_m = \frac{I_C}{V_A} \approx 40 I_C \tag{5}$$

Differential Mode Input Resistance

$$R_{id} = 2r_\pi \tag{6}$$

where

$$r_\pi = \frac{\beta}{g_m} \tag{7}$$

Differential Mode Output Resistance

$$R_{od} = 2(R_C || r_o) \approx 2R_C \tag{8}$$

where

$$r_o = \frac{V_A + V_{CE}}{I_C} \tag{9}$$

Common Mode Gain

$$A_{cc} = \frac{\beta R_C}{r_\pi + 2(beta+1)R_{EE}} \approx \frac{-R_C}{2R_{EE}} \tag{10}$$

Common Mode Input Resistance

$$R_{ic} = \frac{r_\pi}{2} + (\beta + 1)R_{EE} \tag{11}$$

Differential Amplifier Output Resistance

$$R_{single} = R_C \tag{12}$$

$$R_{differential} = 2(R_C||r_o) \approx 2R_C \tag{13}$$

where

$$r_o = \frac{V_A + V_{CE}}{I_C} \tag{14}$$

Common Mode Rejection Ratio

$$CMRR = \frac{\frac{A_{dd}}{2}}{A_{cc}} \tag{15}$$

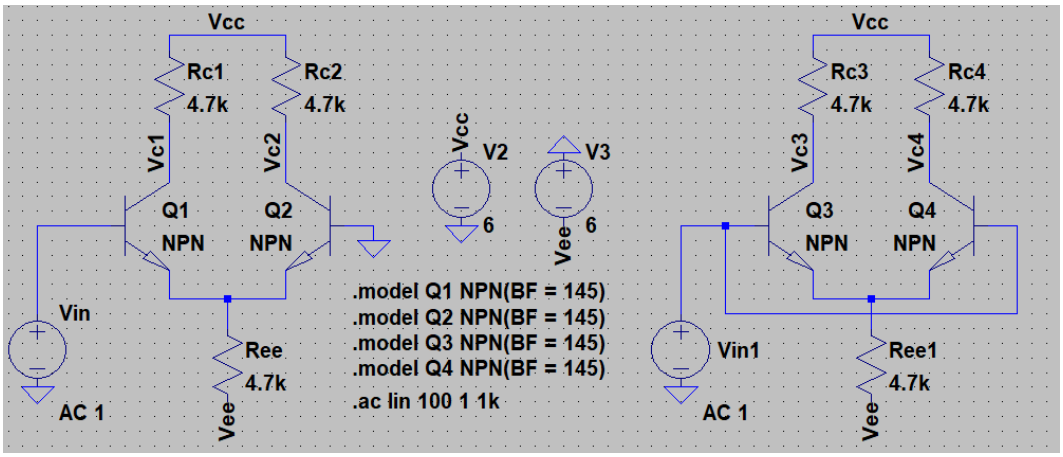

Figure 1: Differential Amplifier Schematic

In the schematic above, we have the differential mode on the left and the common mode on the right. The bipolar junction transistor used is a MPQ3904. To model this in the simulation, we used the average beta value of the range given in the datasheet. The following plots show the AC characteristics of the two. The methods

of finding the AC characteristics are identical to the methods in the first project.

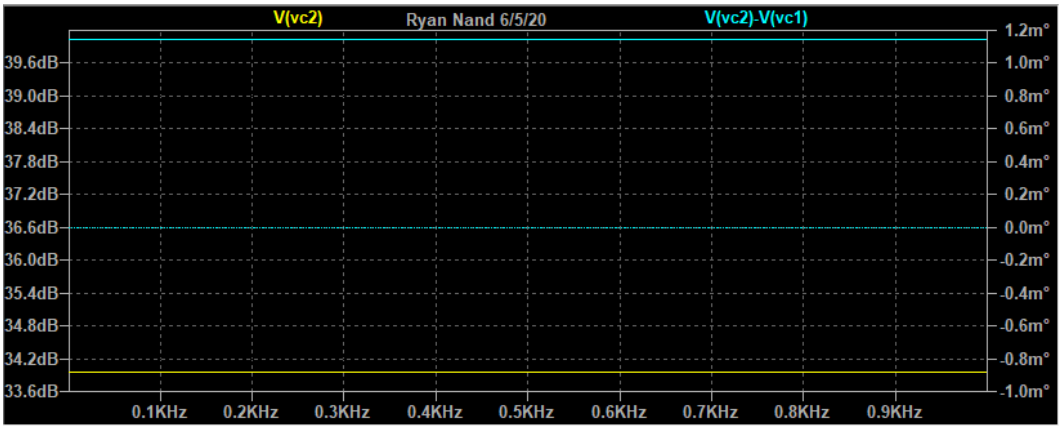

Figure 2: Differential Mode Gain

In the plot above, we have single output gain in yellow and differential output in blue.

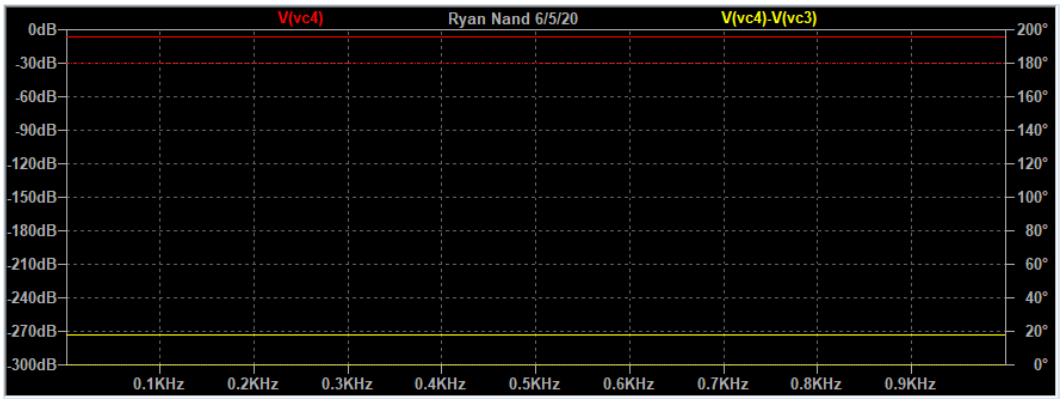

Figure 3: Common Mode Gain

In the plot above, we have single output gain in red and differential output in yellow.

The next two plots show the input impedance for each mode.

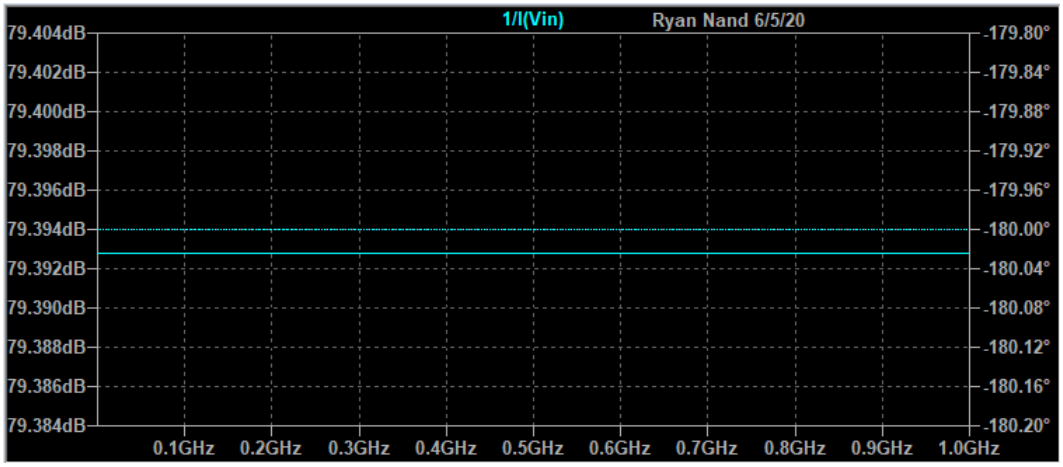

Figure 4: Differential Mode Input Impedance

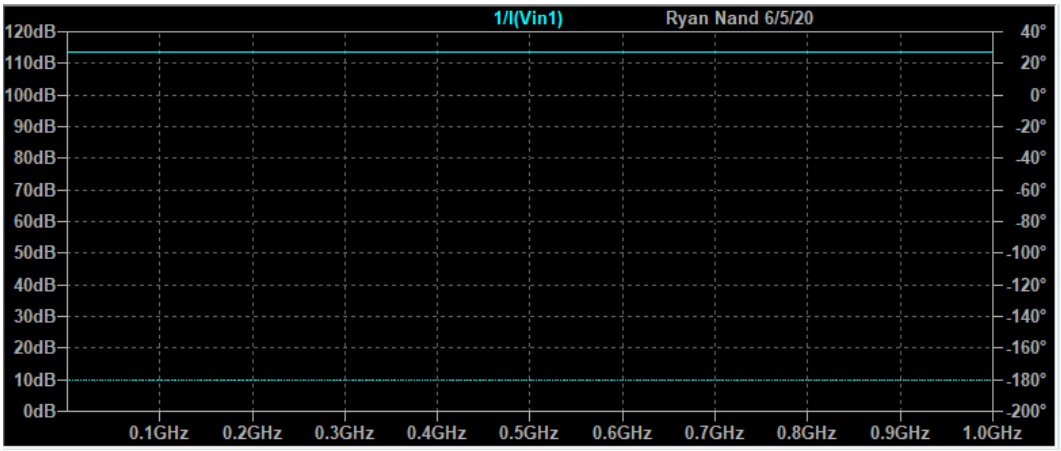

Figure 5: Common Mode Input Impedance

The next two plots show the output impedance of the differential amplifier. Realize that they are the same amongst the two modes, therefore isolation is not needed.

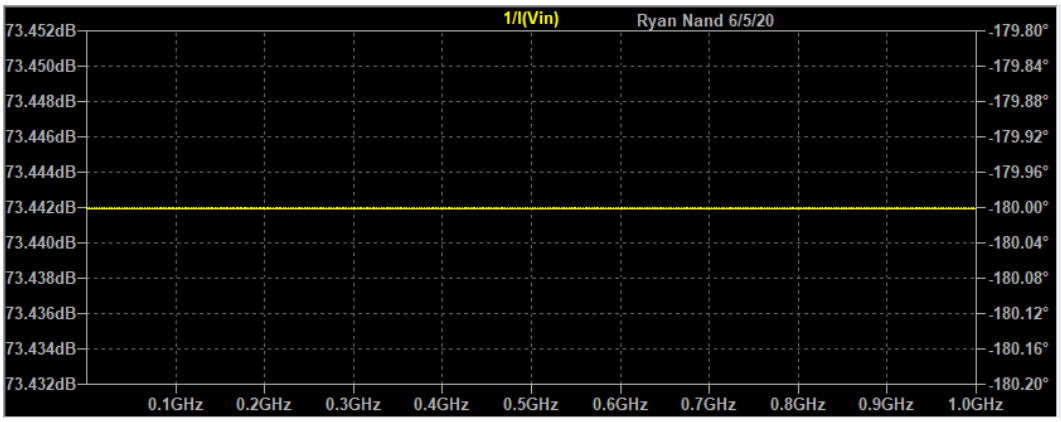

Figure 6: Differential Amp Output Impedance with Single Output

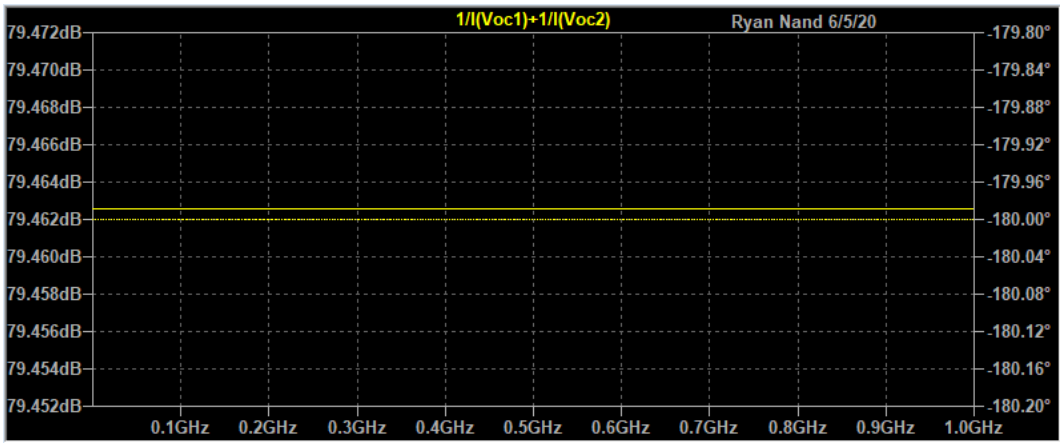

Figure 7: Differential Amp Output Impedance with Differential Output

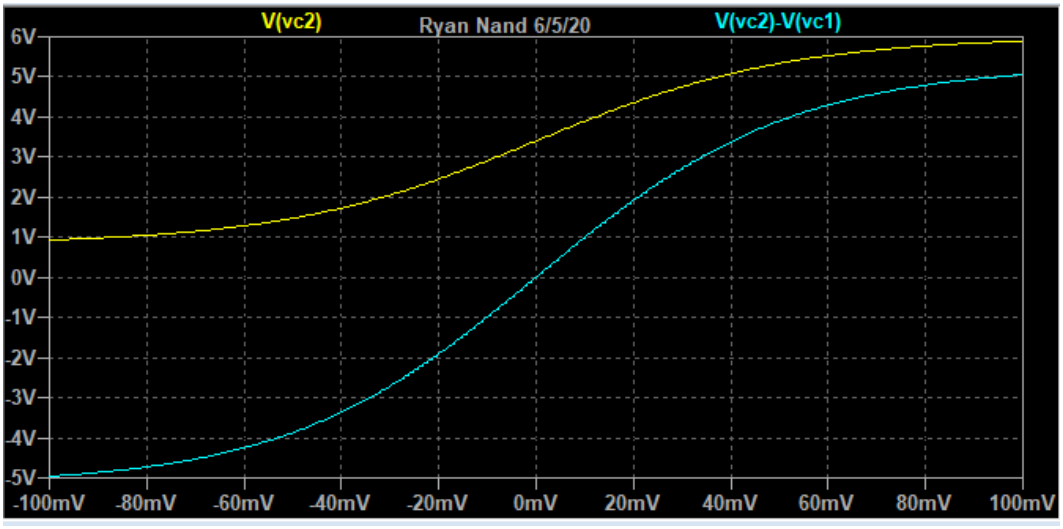

Figure 8: Linear Range of Differential Amplifier

The plot above shows the linear range of the amplifier including both differential and single output. The range is about -40mV to 40mV.

The calculated Q-point is: $I_C = .564$ mA and $V_{CE} = 4.0492$ V

The following table summarizes the values from the plots with the calculations.

	Differential Mode				Common Mode			
	Single Output		Differential Output		Single Output		Differential Output	
	Calculated	Simulated	Calculated	Simulated	Calculated	Simulated	Calculated	Simulated
Gain	53	50	106	100	.5	2	∞	3e13
Input Impedance	12854.6	8912.5	12854.6	8912.5	689413.6	398107	689413.6	398107
Output Impedance	4700	4467	9400	9332	4700	4467	9400	9332

From the table we can that the simulated gain and output impedance are very close to their calculated values. However, it is safe to say that is true only for the differential mode. The common mode differs significantly, especially for input impedance. From the plots we can calculate CMRR using equation (15), which turns out to be 12.5.

3 Current Source

Here we will design the current source to be used with the differential amplifier. This is used because we don't know the load of the operational amplifier. Therefore, a constant current that does not change will benefit the design.

Here are the equations used to design the system.

Current Mirror Equations

$$I_{ref} = \frac{V_{CC} + V_{EE} - V_{BE}}{R} \tag{16}$$

$$I_o = \frac{I_{ref}}{1 + \frac{2}{\beta}} \tag{17}$$

The design is to have 1mA as I_{ref}. The following schematic and plots resulted from that requirement. We have a standard resistor value of 11kΩ placed where R1 is.

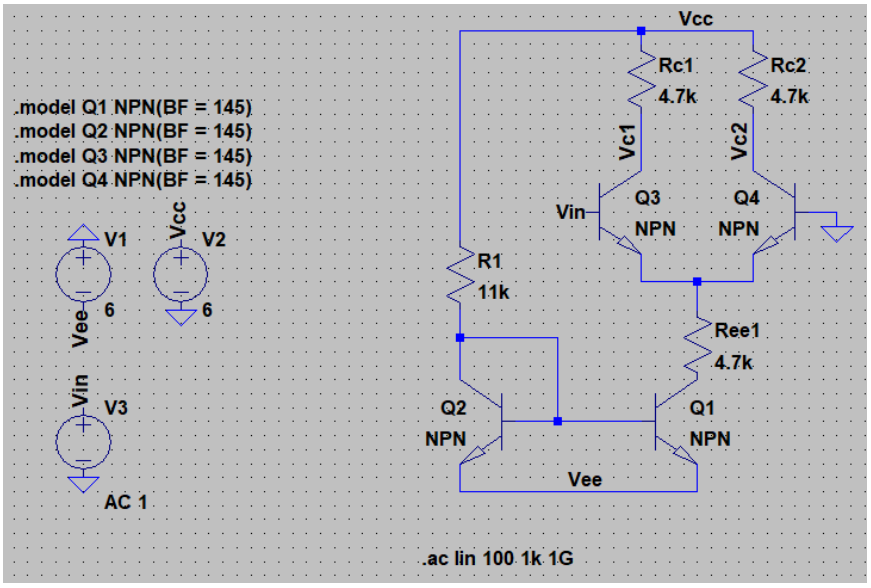

Figure 9: Differential Amplifier with Current Biasing

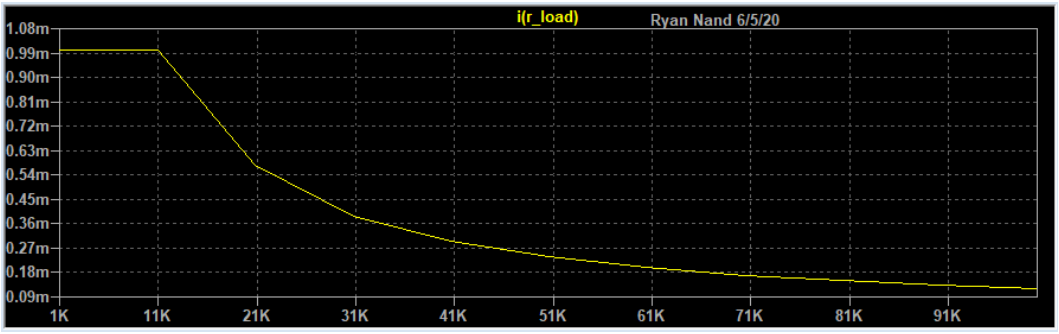

Figure 10: Current Mirror with R_{load} Varying

The plot above shows the current mirror's response to a varying load. In other words, if the differential amplifier changes it's input resistance how would the current mirror respond? The plot shows that response, where the error is .001%

The next few plots show the AC characteristics for the schematic above.

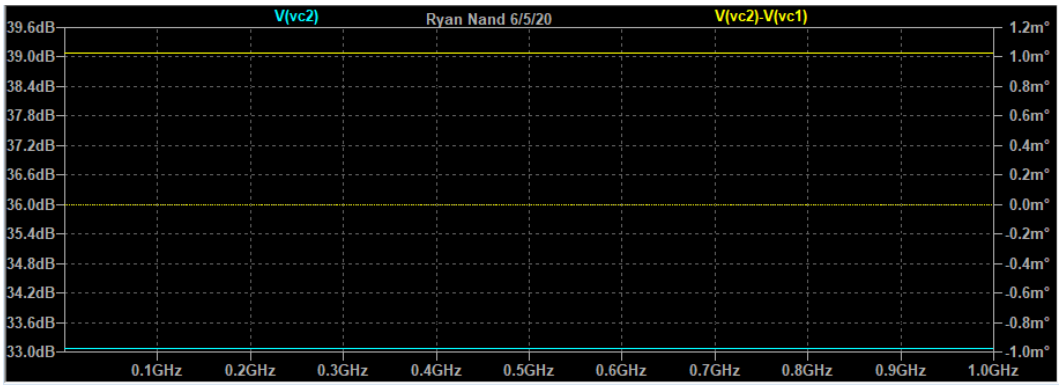

Figure 11: Biased Differential Mode Gain

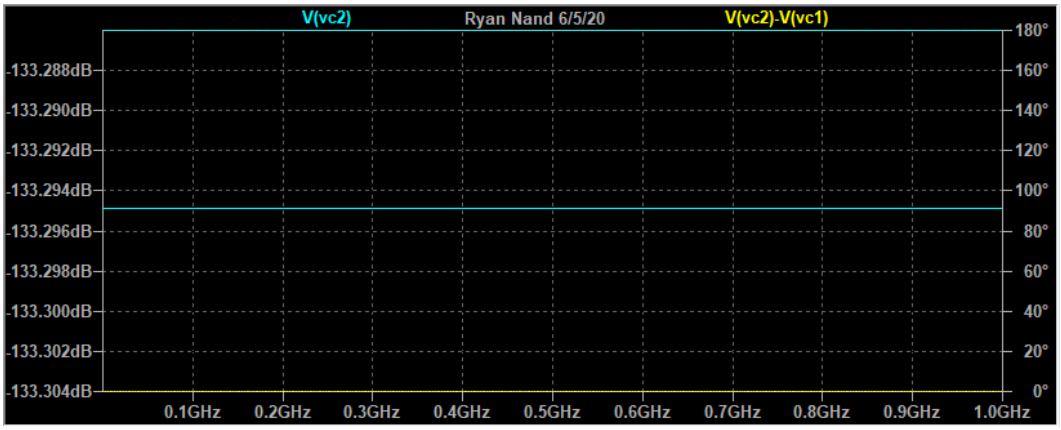

Figure 12: Biased Common Mode Gain

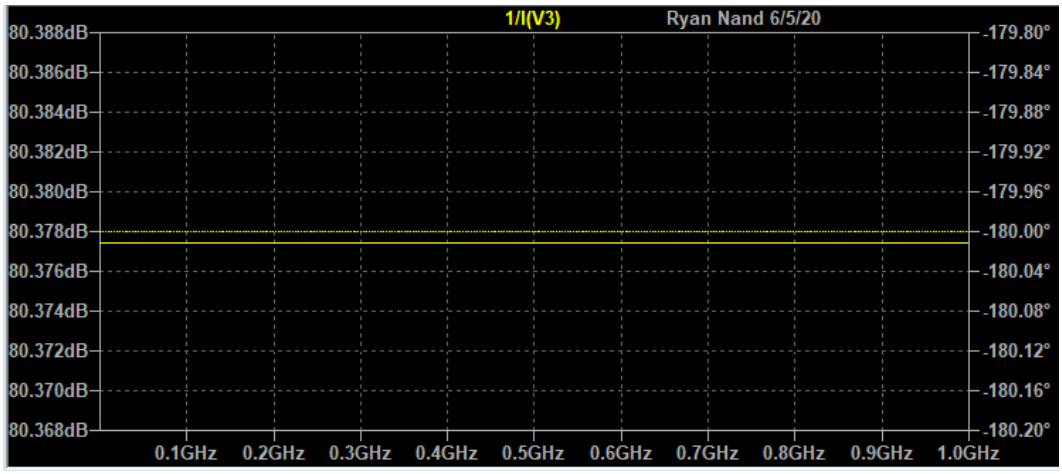

Figure 13: Biased Differential Mode Input Impedance

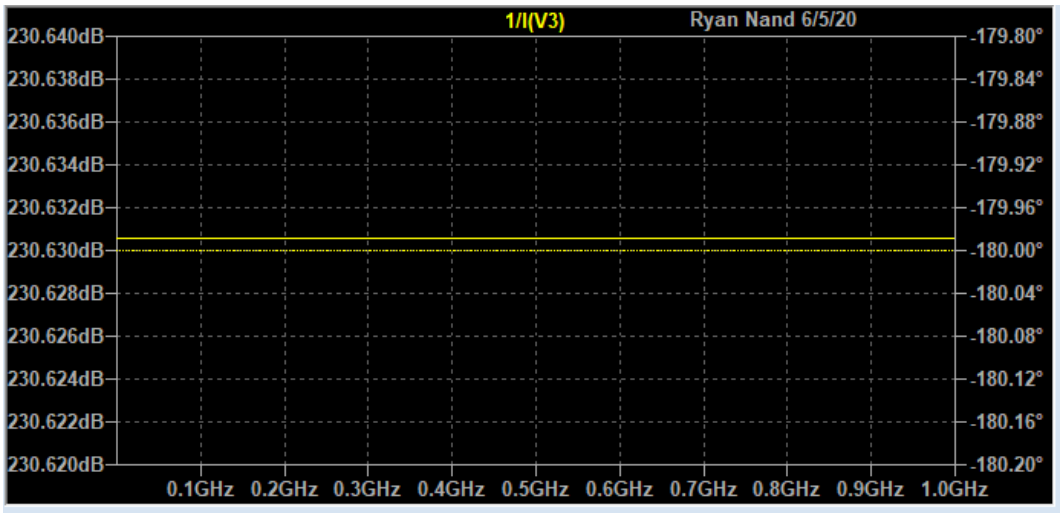

Figure 14: Biased Common Mode Input Impedance

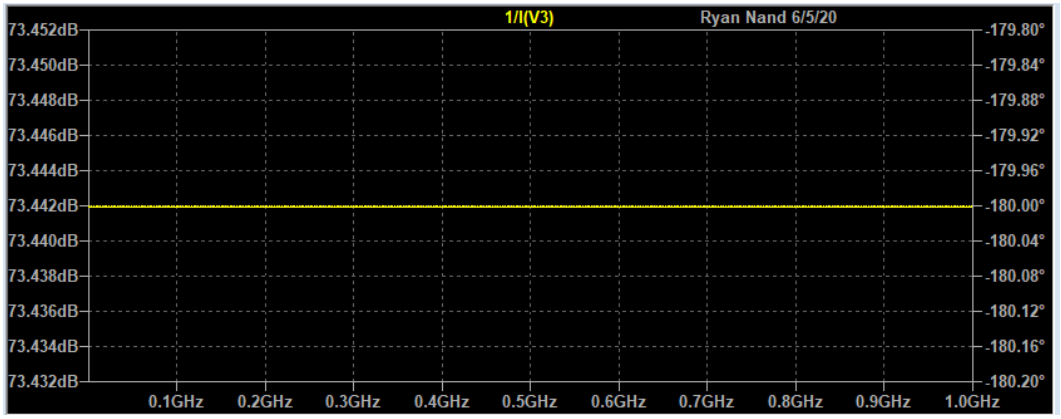

Figure 15: Differential Amplifier Output Impedance Single Output

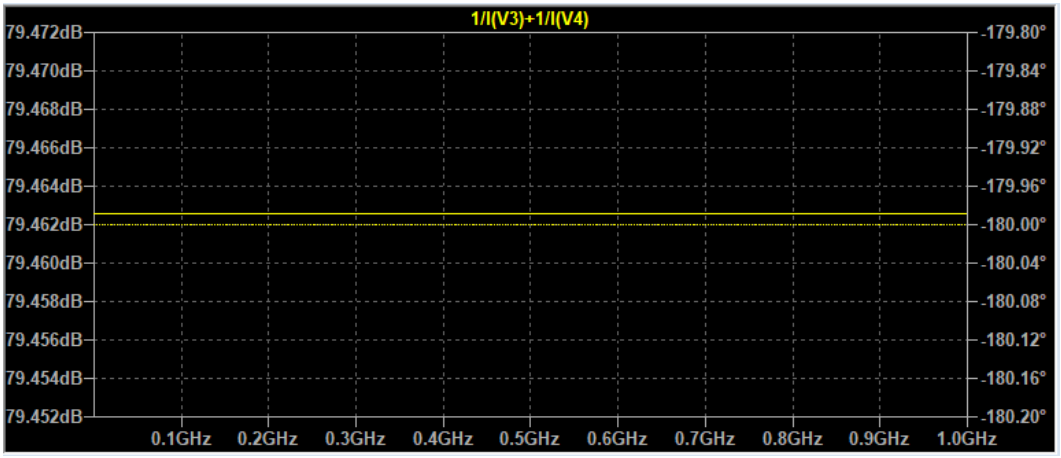

Figure 16: Differential Amplifier Output Impedance Differential Output

Again, we can see that the gain for the differential mode is very close. The same cannot be said for the common mode. There is a greater difference between this biased values when compared with the previous simulations. This is because the current I_C has changed from .563mA to .5mA. For a better design, we can recalculate the values using .5mA which will result in closer approximations.

4 Active Load

Now we will install an active load to the differential amplifier. This removes the resistor R_C from the circuit. The schematic is below, along with the AC characteristics this schematic produces.

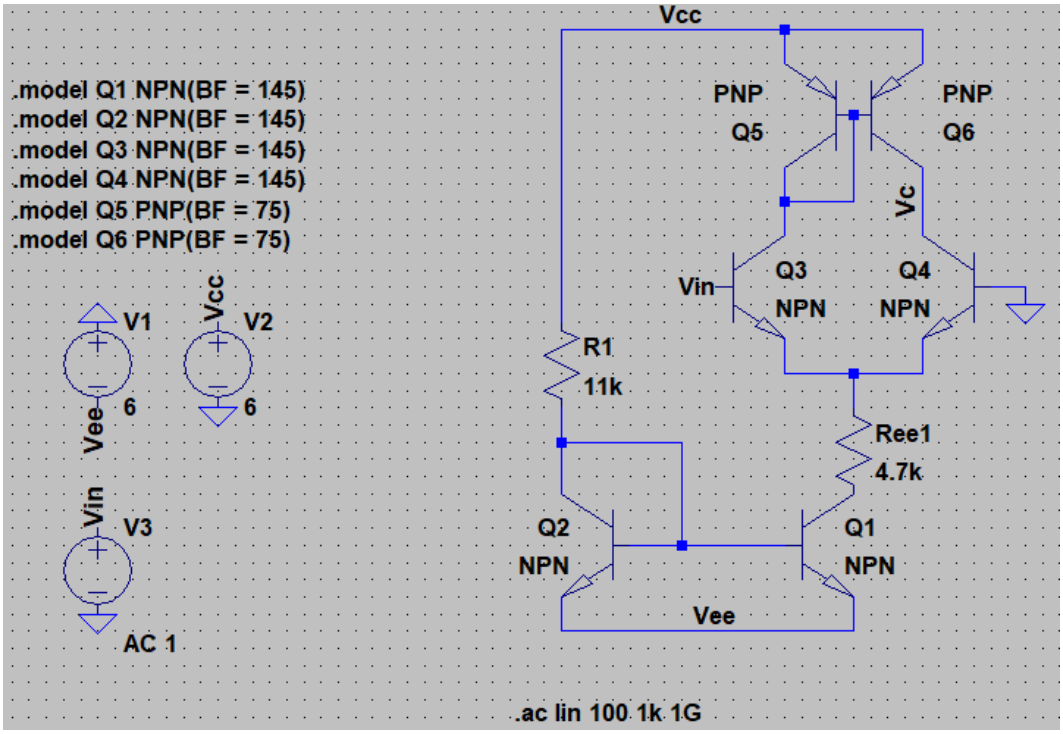

Figure 17: Differential Amplifier with Active Load

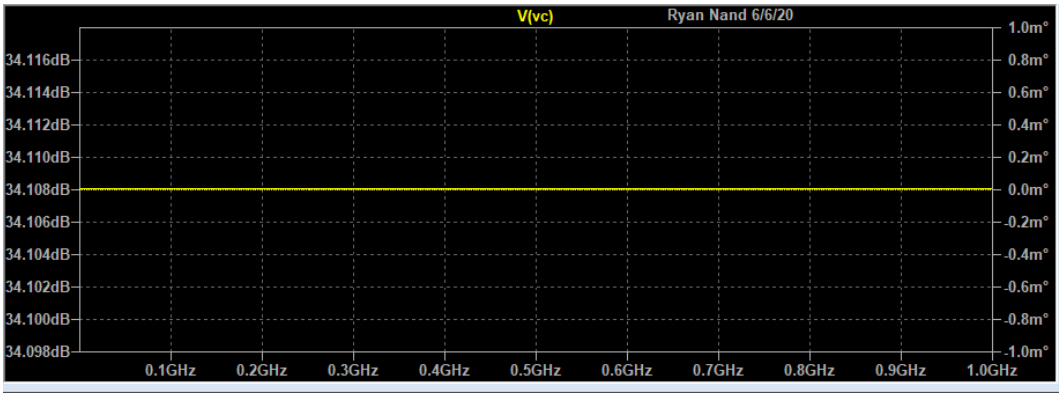

Figure 18: Differential Amplifier with Amplifier Gain

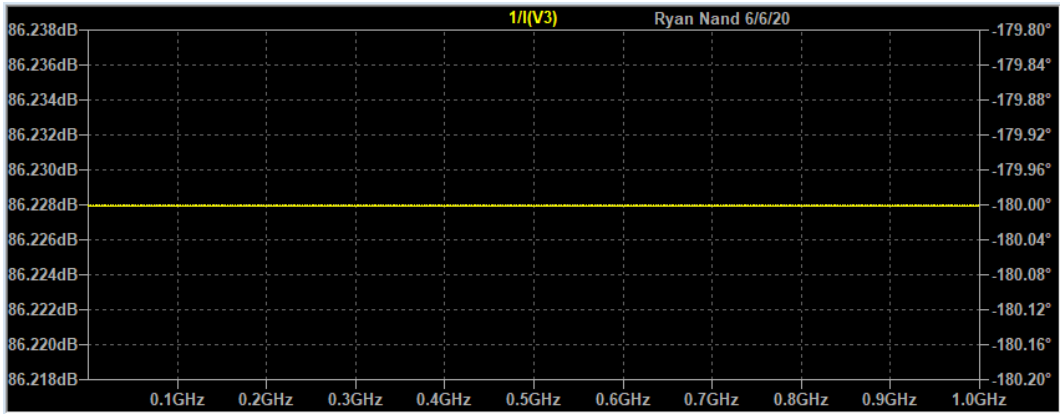

Figure 19: Differential Amplifier with Active Load Input Impedance

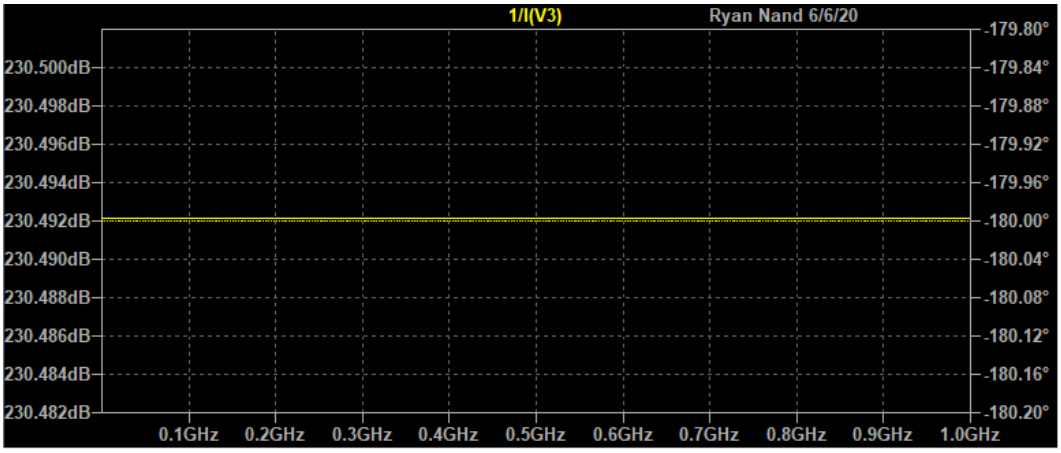

Figure 20: Differential Amplifier with Active Load Output Impedance

These AC characteristics are very close to theory. In fact, the gain is very much ideal. In addition, the input impedance increased since the previous schematic. This is a side effect of adding the active load, which is a good thing. However, the output impedance is very high. This is a problem that will be solved using an output stage.

Next we will be adding a quick output. The goal of this is to lower the output resistance. The next plot will show why that is.

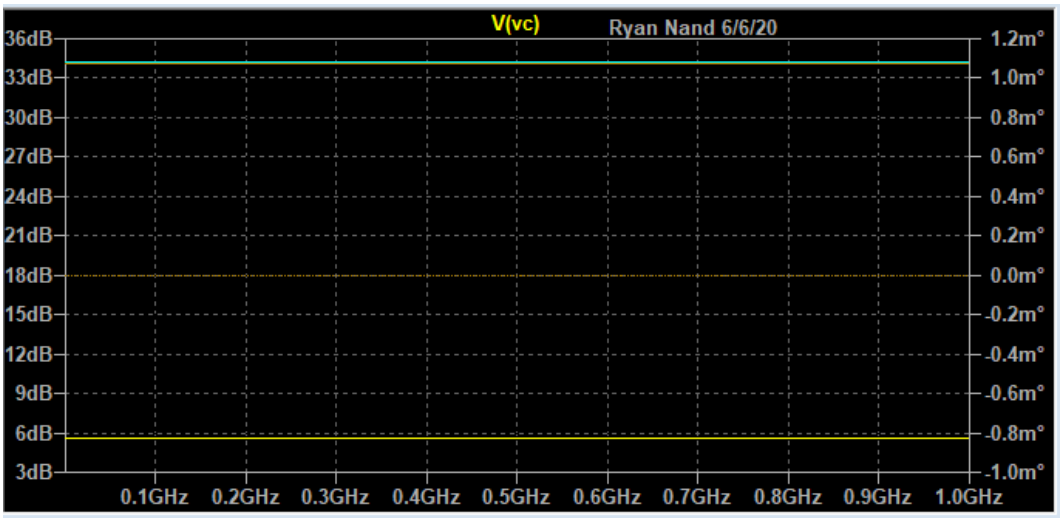

Figure 21: Gain vs. R_{Load}

The above plot does not show it clearly, but when the load resistance is very low the gain is close to zero. As the resistance of the load increased the gain increased. This is because when the load resistance is close to zero, the circuit is basically shorted to ground. With the addition of the output stage seen in the next figure, we can try to lower the output resistance.
This output stage was designed using diode drops with the intent of lowering the dc offset. However, the dc offset is quite large. About 5V instead of the ideal less than 100mV. Since the design of the offset is out of the scope of this class we will not ponder on it. The next plot shows the dc offset.

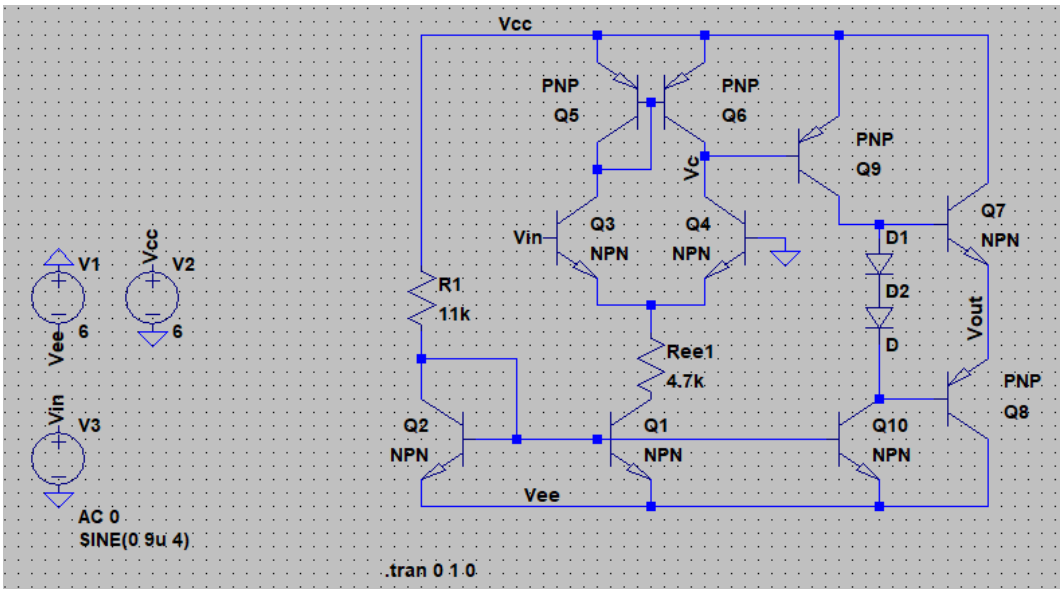

Figure 22: Differential Amplifier with Output Stage

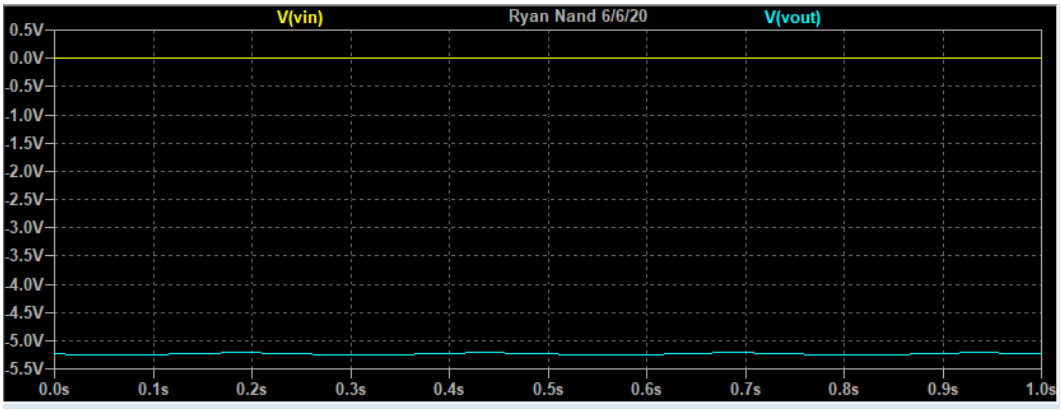

Figure 23: Amplifier DC Offset

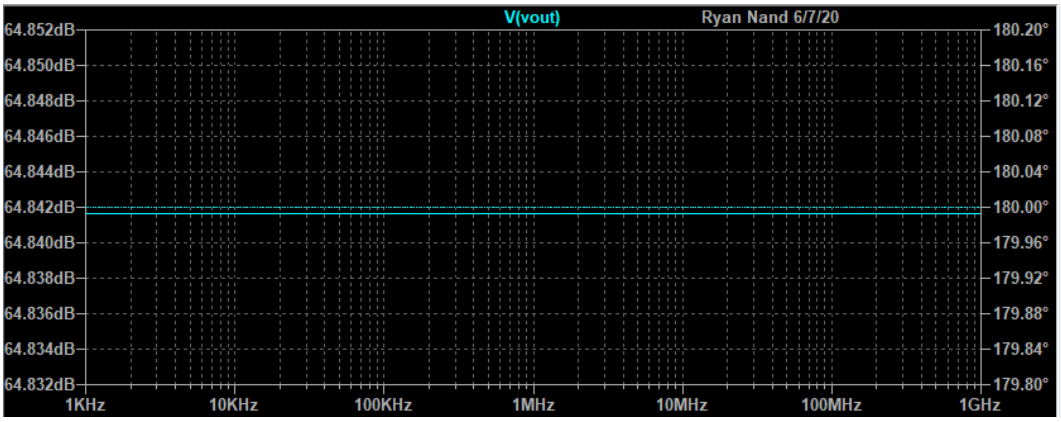

Figure 24: Amplifier Gain

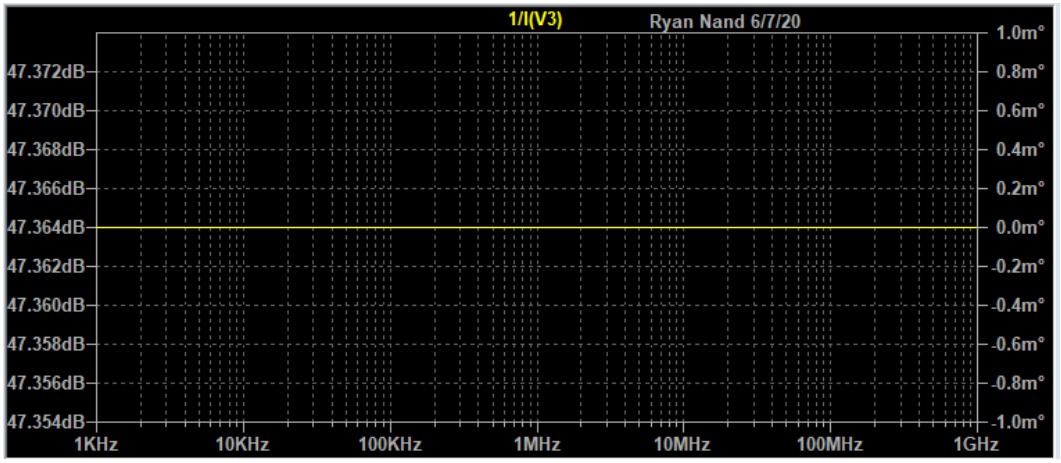

Figure 25: Amplifier Input Impedance

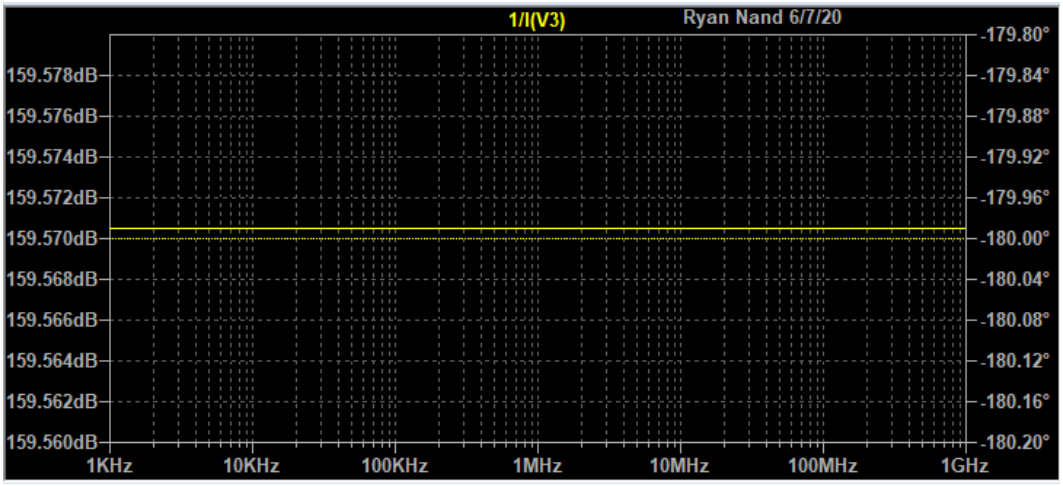

Figure 26: Amplifier Output Impedance

As you can see, the output stage did not work as intended. Further studying will have to be put in place to better design the output stage. Not quite sure where the issue is, since everything worked fine up until the addition of the output stage. The input and output impedance's do not fall in line with the calculation results. In this case, the opposite of the intention happened. Where the input impedance is low and the output impedance is high. Lastly, the gain skyrocketed from expectations.

5 Improvement

This next section is to look at ways to improve the design. However, since the output stage did not work as intended. We will be moving forward without the output stage connected. We will be testing the buffered current mirror. The purpose of the buffered current mirror is to have the system less reliant on the beta effect. Therefore, we would like to see if the system becomes less reliant on the beta value. In other words, to see if the AC characteristics from simulation gets closer to the theoretical values from calculations. Here is the schematic with the buffered current source.

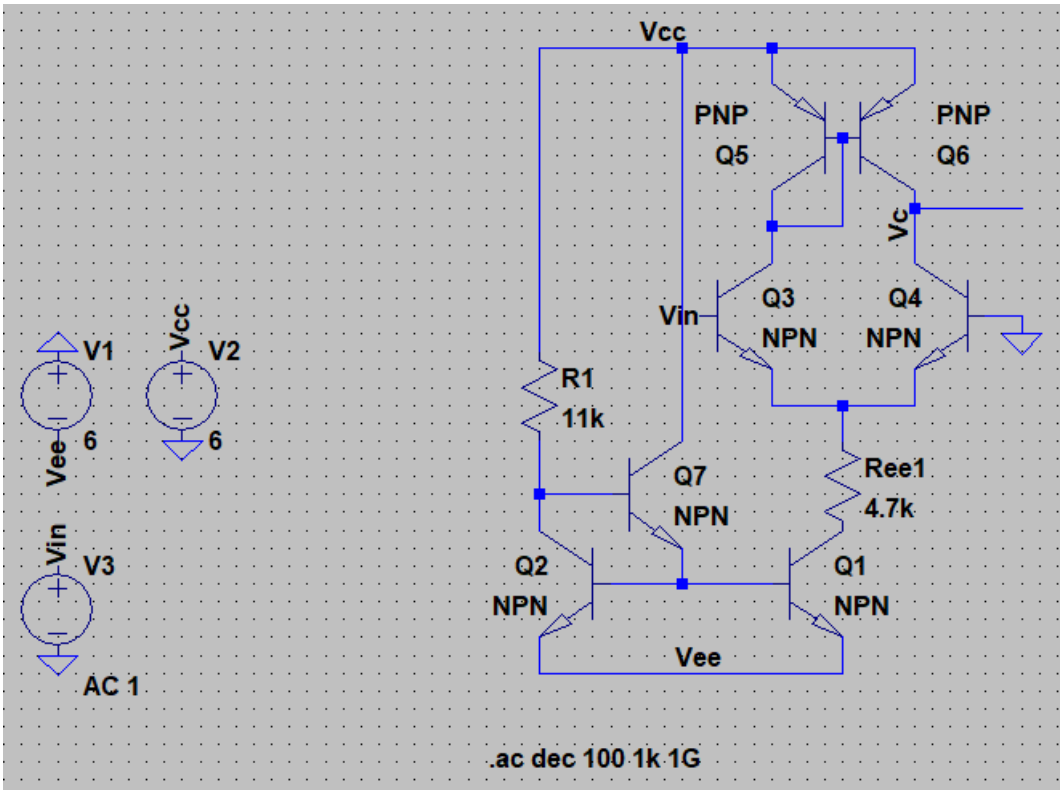

Figure 27: Buffered Current Source

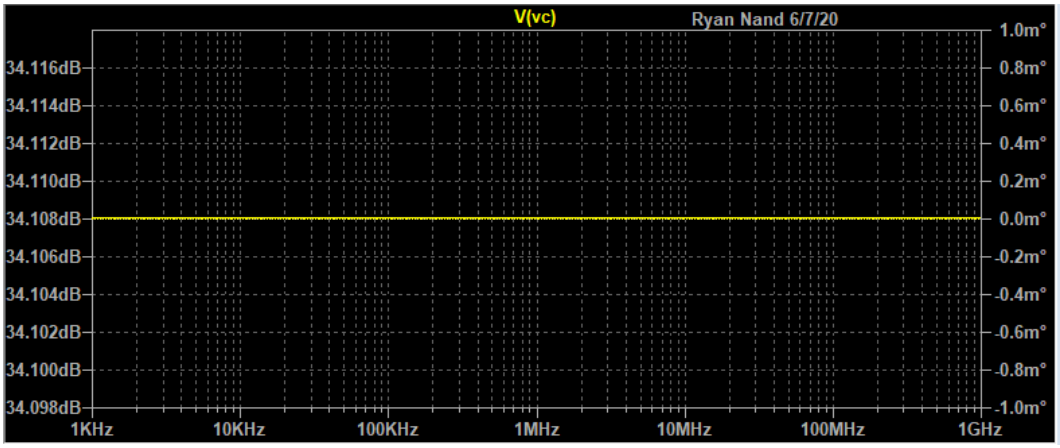

Figure 28: Gain with Buffered Current Source

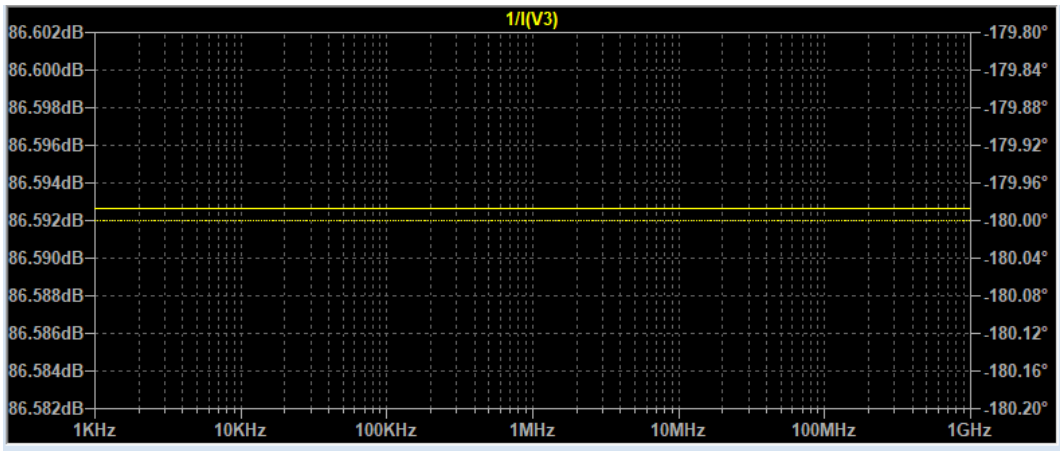

Figure 29: Input Impedance with Buffered Current Source

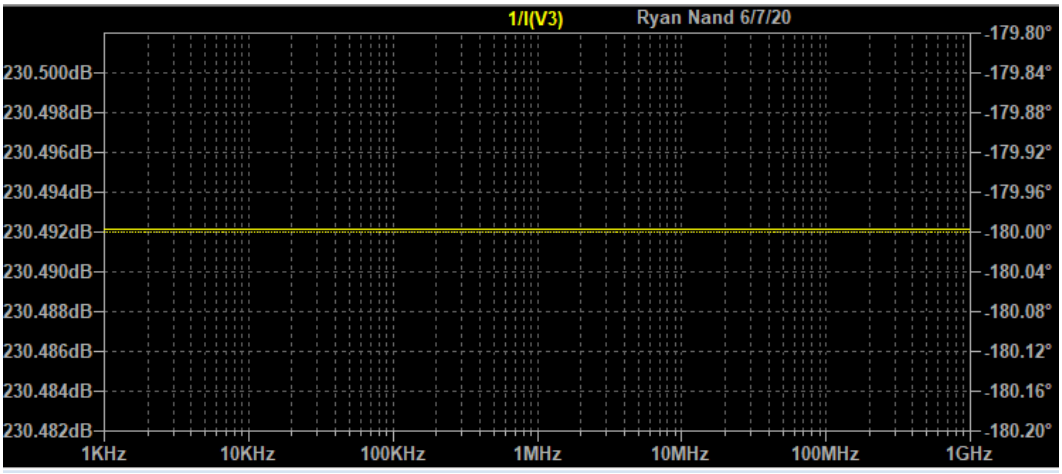

Figure 30: Output Impedance with Buffered Current Source

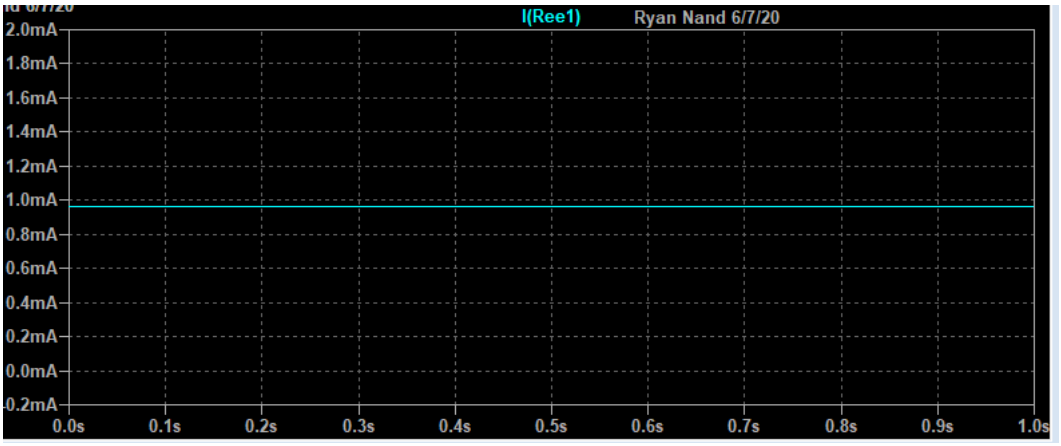

Figure 31: Current in Differential Amplifier

6 Conclusion

In this project, we looked at the design and simulation of a "mini" op amp. We started with the differential amplifier, moved onto the current source using a current mirror, then went to the active load, and then ending with the output stage. Looking at the results everything added up and made sense up until the output stage, where things fell apart. We found that the input impedance was low and the output impedance was still high. The main reason why we even installed that output stage. In addition, the gain skyrocketed. As for the sections of stages before the output stage, everything was close to the theoretical calculation values. Except for some common mode input resistances.

Since the output stage was not in line with the intention. Saving the symbol and using the symbol did not go according to theory as well. I am not sure why everything went well up until the output stage. Therefore, I would like to spent more time on the studying of that portion and redesigning the system at a later time in the near future. Leading to the improvement stage I decided to fall back to when the design was actually working. This way when establishing the improvement we have a initial working circuit to work on. Otherwise, it might just lead to further confusion.

Lastly, for the final portion of this lab which was the improvement of the the op amp. Looking back at the plots I noticed only a slight improvement. If we compare the plots from earlier with these buffered plots, we can see that only the input resistance has changed. The input resistance was increased by 1. That being said, I still think that slight variations within the designs are very important. Especially, in the real world, because each design as tolerance levels. If one system had strict tolerances we cannot fallout every slight change. Also, looking back at the schematic, R_{EE} was left in the circuit for the sole purpose of measuring DC current. The resistor does not effect the system in terms of gain. Would remove when simulating AC characteristics though.

In the end, I feel like I learned the basics of this project. I would have liked to go more in depth at a more proper environment. But considering the case of current situations, this was better than nothing at all. Seeing how I would like to go the analog circuit design route, I hope in later courses we get to touch up on a few things

here and there. Especially, since some of the topics of this report were out of scope of the class. If I were to do this project again, I would like to spend less time on creating plots and formatting this report and more time on the concepts. Along with working on this project with real components in a lab setting.