5.1

A) This new adder has two clocks (clock1 and clock2). Clock2 is in dff_sum where the rest have clock1. Also, the new adder is implemented using system verilog where “always_ff” is used instead of “always”.

B) For the worst setup, there are three paths to consider. They all seem to have the same slack.

```
dc_shell> report_timing -from dff_b/q -to dff_cout/d -significant_digits 3
 Startpoint: dff_cin/q_reg
             (rising edge-triggered flip-flop clocked by CLK1)
 Endpoint: dff_cout/q_reg
           (rising edge-triggered flip-flop clocked by CLK1)
 Path Group: CLK1
 Path Type: max

 Des/Clust/Port     Wire Load Model       Library
 ------------------------------------------------
 adder              ForQA                 saed32hvt_ff0p95v125c

 Point                                                   Incr       Path
 ------------------------------------------------------------------------
 clock CLK1 (rise edge)                                 0.000      0.000
 clock network delay (ideal)                            0.000      0.000
 dff_cin/q_reg/clocked_on (**SEQGEN**)                  0.000      0.000 r
 dff_cin/q_reg/Q (**SEQGEN**)                           0.000      0.000 r
 dff_cin/q (dff) <-                                     0.000      0.000 r
 C13/Z (GTECH_AND2)                                     0.039      0.039 r
 C11/Z (GTECH_OR2)                                      0.003      0.042 r
 C10/Z (GTECH_OR2)                                      0.003      0.045 r
 dff_cout/d (dff) <-                                    0.000      0.045 r
 dff_cout/q_reg/next_state (**SEQGEN**)                 0.003      0.048 r
 data arrival time                                                 0.048

 clock CLK1 (rise edge)                                 0.200      0.200
 clock network delay (ideal)                            0.000      0.200
 dff_cout/q_reg/clocked_on (**SEQGEN**)                 0.000      0.200 r
 library setup time                                     0.000      0.200
 data required time                                                0.200
 ------------------------------------------------------------------------
 data required time                                                0.200
 data arrival time                                                -0.048
 ------------------------------------------------------------------------
 slack (MET)                                                       0.152
```

```
dc_shell> report_timing -from dff_b/q -to dff_cout/d -significant_digits 3 -dela
y min
```

```
Startpoint: dff_b/q_reg
            (rising edge-triggered flip-flop clocked by CLK1)
Endpoint: dff_cout/q_reg
          (rising edge-triggered flip-flop clocked by CLK1)
Path Group: CLK1
Path Type: min

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
adder              ForQA                 saed32hvt_ff0p95v125c

Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock CLK1 (rise edge)                                  0.000      0.000
clock network delay (ideal)                             0.000      0.000
dff_b/q_reg/clocked_on (**SEQGEN**)                     0.000      0.000 r
dff_b/q_reg/Q (**SEQGEN**)                              0.000      0.000 r
dff_b/q (dff) <-                                        0.000      0.000 r
C12/Z (GTECH_AND2)                                      0.039      0.039 r
C11/Z (GTECH_OR2)                                       0.003      0.042 r
C10/Z (GTECH_OR2)                                       0.003      0.045 r
dff_cout/d (dff) <-                                     0.000      0.045 r
dff_cout/q_reg/next_state (**SEQGEN**)                  0.003      0.048 r
data arrival time                                                  0.048

clock CLK1 (rise edge)                                  0.000      0.000
clock network delay (ideal)                             0.000      0.000
dff_cout/q_reg/clocked_on (**SEQGEN**)                  0.000      0.000 r
library hold time                                       0.000      0.000
data required time                                                 0.000
-----------------------------------------------------------------------------
data required time                                                 0.000
data arrival time                                                 -0.048
-----------------------------------------------------------------------------
slack (MET)                                                        0.048
```

C) Looks like the period increases the slack time for setup.

```
dc_shell> report_timing -from dff_b/q -to dff_sum/d -significant_digits 3
```

```
Startpoint: dff_b/q_reg
            (rising edge-triggered flip-flop clocked by CLK1)
Endpoint: dff_sum/q_reg
          (rising edge-triggered flip-flop clocked by CLK2)
Path Group: CLK2
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
adder              ForQA                 saed32hvt_ff0p95v125c

Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock CLK1 (rise edge)                                  0.200      0.200
clock network delay (ideal)                             0.000      0.200
dff_b/q_reg/clocked_on (**SEQGEN**)                     0.000      0.200 r
dff_b/q_reg/Q (**SEQGEN**)                              0.000      0.200 r
dff_b/q (dff) <-                                        0.000      0.200 r
C9/Z (GTECH_XOR2)                                       0.039      0.239 r
C8/Z (GTECH_XOR2)                                       0.003      0.242 r
dff_sum/d (dff) <-                                      0.000      0.242 r
dff_sum/q_reg/next_state (**SEQGEN**)                   0.003      0.245 r
data arrival time                                                  0.245

clock CLK2 (rise edge)                                  0.400      0.400
clock network delay (ideal)                             0.000      0.400
dff_sum/q_reg/clocked_on (**SEQGEN**)                   0.000      0.400 r
library setup time                                      0.000      0.400
data required time                                                 0.400
-----------------------------------------------------------------------------
data required time                                                 0.400
data arrival time                                                 -0.245
-----------------------------------------------------------------------------
slack (MET)                                                        0.155
```