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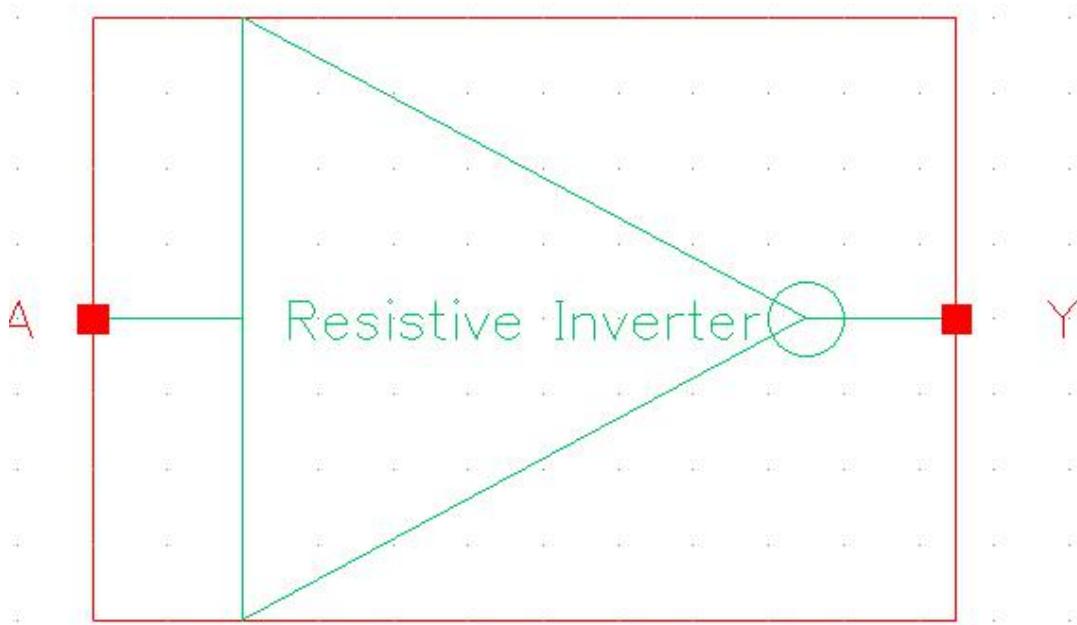
**Introduction and Physical Properties**

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**1) Cell Description**

A Resistive inverter is used in the same way as other kinds of inverters (i.e. the output is the inversion of the input) but is constructed differently than say a CMOS inverter. The inverter's schematic, shown in Fig. 2, has a pull-up resistor (in place of a resistor) and a pull-down nMOS transistor. While nMOS transistors are good at pulling signals down to ground they are not good at delivering strong high signals nor as fast as pMOS transistors which is why a resistor is used to obtain a strong pull-up to the high signal.

**2) Cell Symbol**

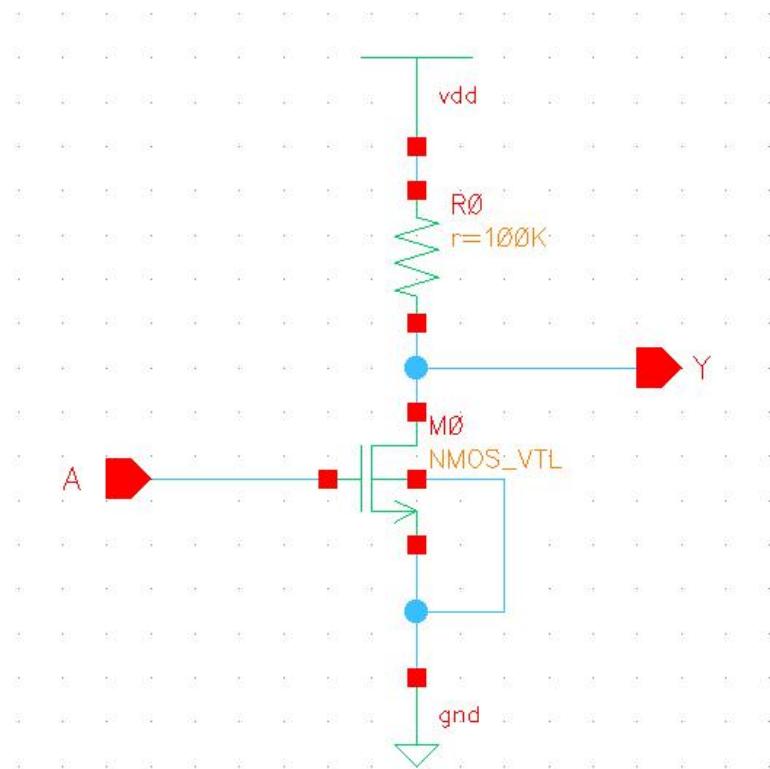


**Figure 1:** Resistive inverter symbol from Cadence Virtuoso. Used for both resistive and resistive long inverters.

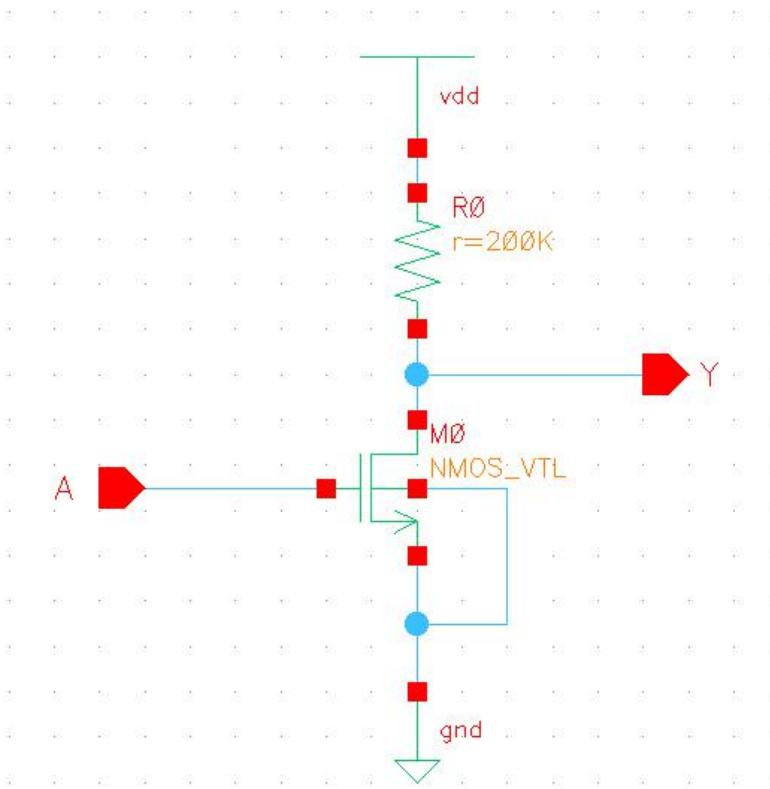
**Cell Truth Table**

Cell Truth Table	
Cell Inputs {0,1}	Cell Outputs {L,H}
0	H
1	L

### 3) Cell Schematic Diagram



**Figure 2: Schematic of the resistive inverter with minimum transistor dimensions and a 100k pull-up resistor.**



**Figure 3: Schematic of the resistive long inverter with a 200k ohm pull-up resistor.**

#### 4,5) Cell Layout Diagram and Dimensions

Transistor Dimensions of Resistive Inverter		
Transistor Instance Number	Length (nm)	Width (nm)
M0	50	90

Transistor Dimensions of Resistive Long Inverter		
Transistor Instance Number	Length (nm)	Width (nm)
M0	50	90

#### Performance Analysis

##### 6,7) Rise and Fall Times

Input X: Output Rise Time Data $t_r$ (ns)		Output Load (FO <sub>X</sub> )				
		0	1	2	4	8
0.04	Resistive				2.092	
0.04	Resistive Long				4.189	

S, Input X: Output Fall Time Data $t_f$ (ns)		Output Load (FO <sub>X</sub> )				
		0	1	2	4	8
0.04	Resistive				0.116	
0.04	Resistive Long				0.123	

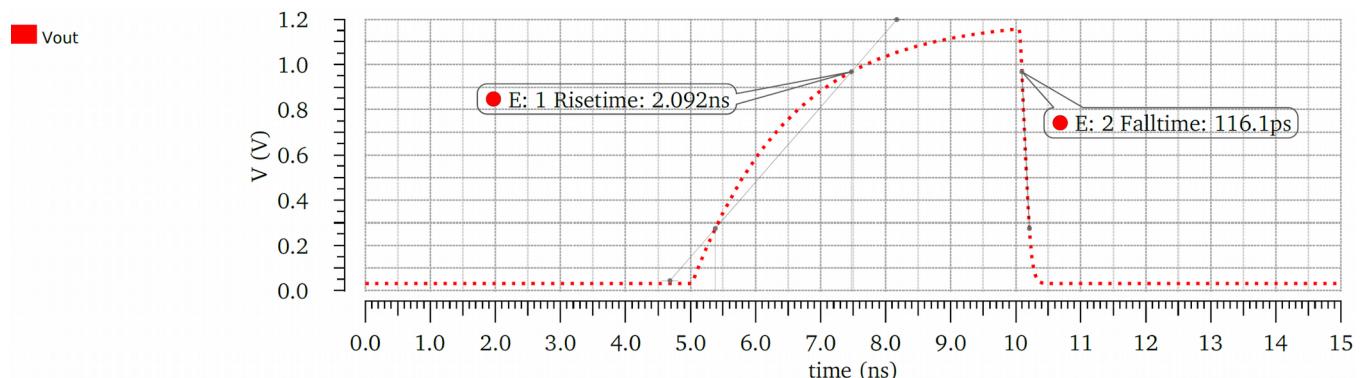
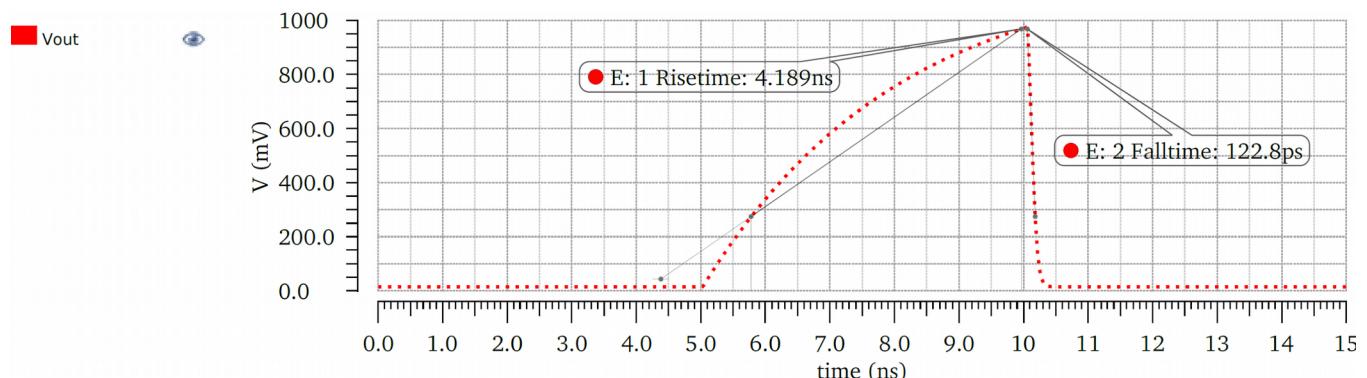


Figure 4: Transient analysis of the resistive inverter showing the rise and fall time of the output.

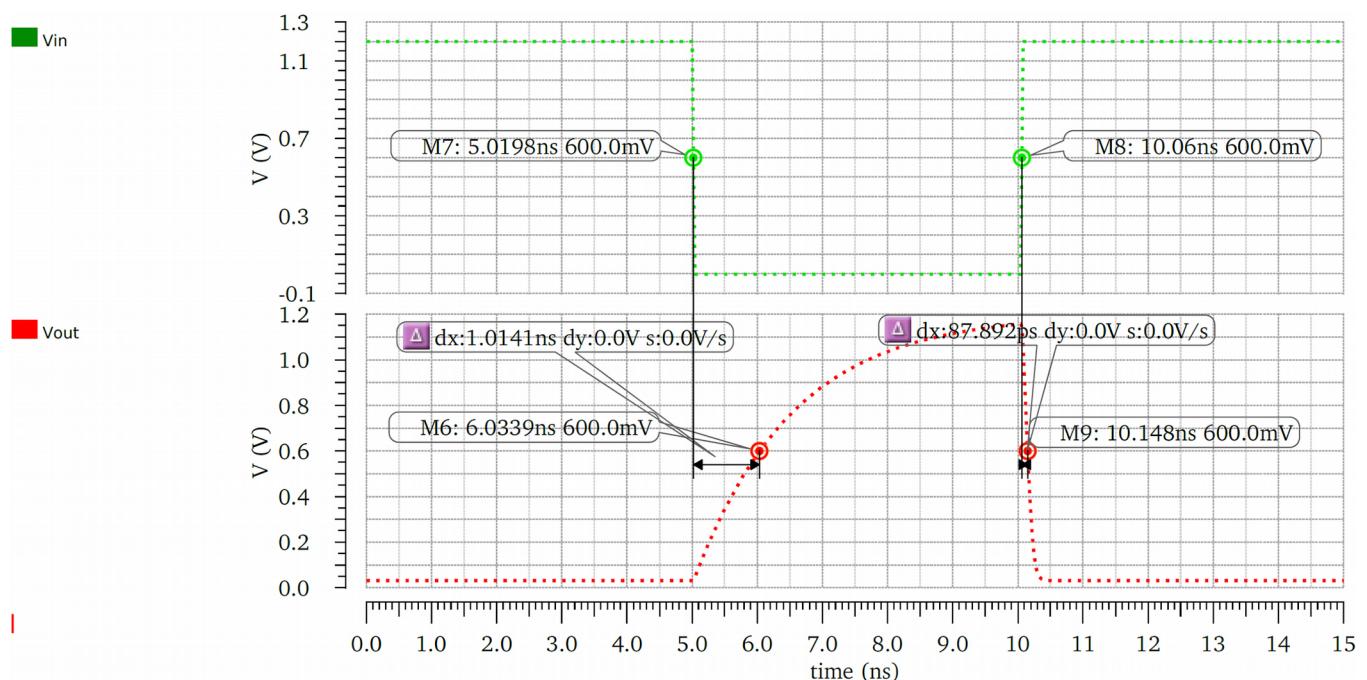


**Figure 5: Transient analysis of the resistive long inverter showing the rise and fall time of the output.**

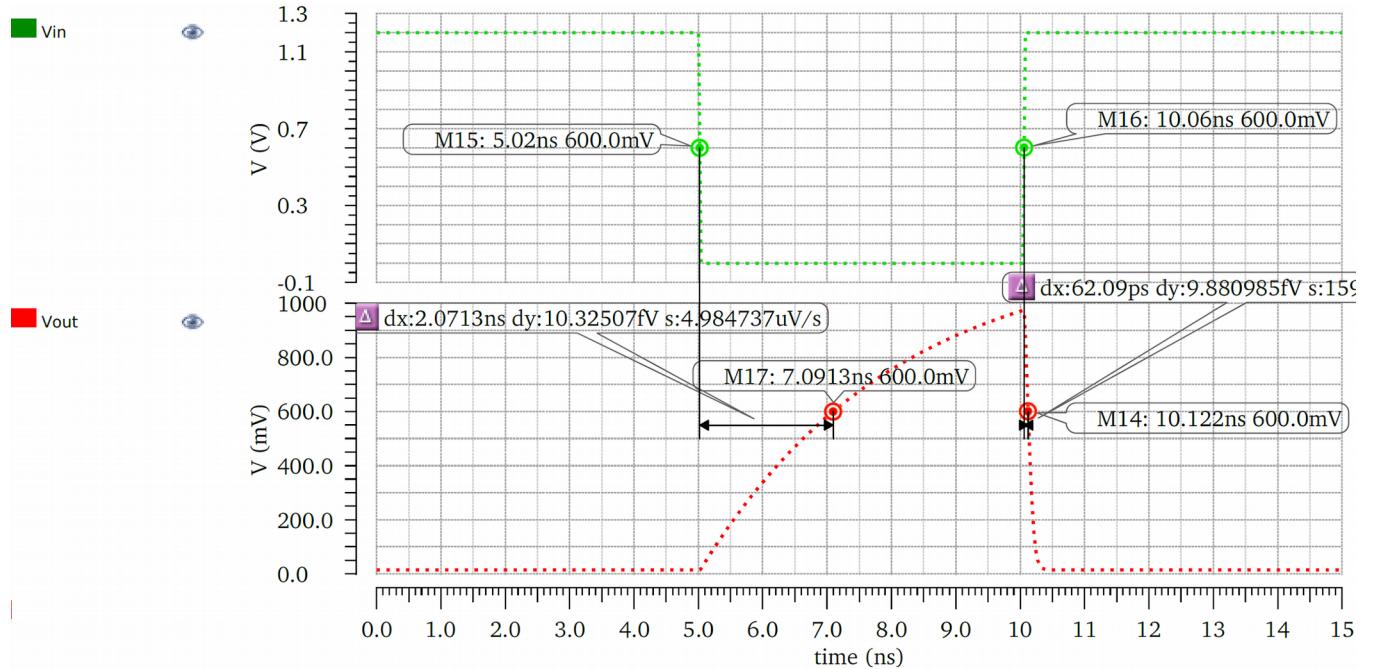
### 8,9) Propagation Delays

Input rise/fall time (ns)	Inverter Configuration	Data Worst Case Low to High Propagation Delay Data $t_{ph}$ (ns)				
		Output Load (FO <sub>x</sub> )				
		0	1	2	4	8
0.04	Resistive				1.014	
0.04	Resistive Long				2.071	

Input rise/fall time (ns)	Inverter Configuration	Data Worst Case High to Low Propagation Delay Data $t_{phl}$ (ns)				
		Output Load (FO <sub>x</sub> )				
		0	1	2	4	8
0.04	Resistive				0.088	
0.04	Resistive Long				0.062	



**Figure 6: Transient analysis of the resistive inverter showing the propagation delays.**

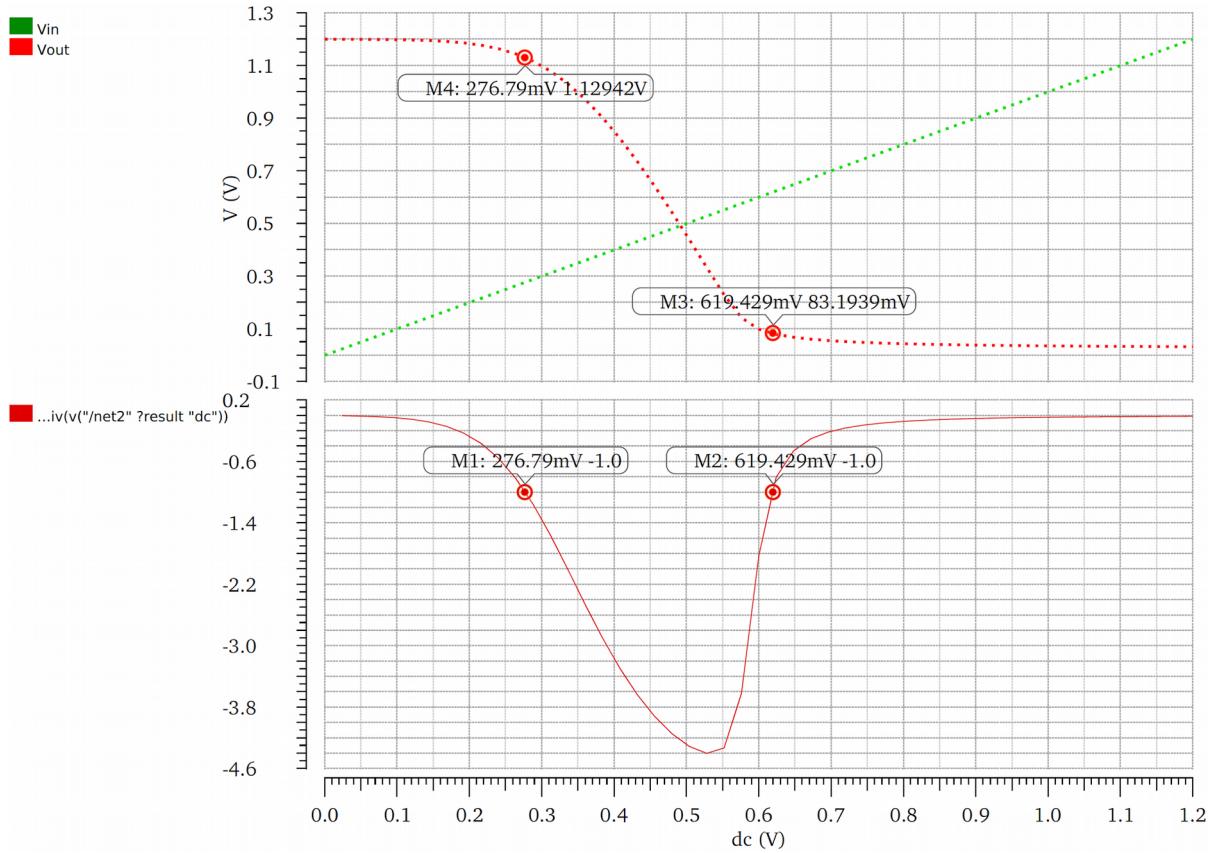


**Figure 7: Transient analysis of the resistive long inverter showing the propagation delays.**

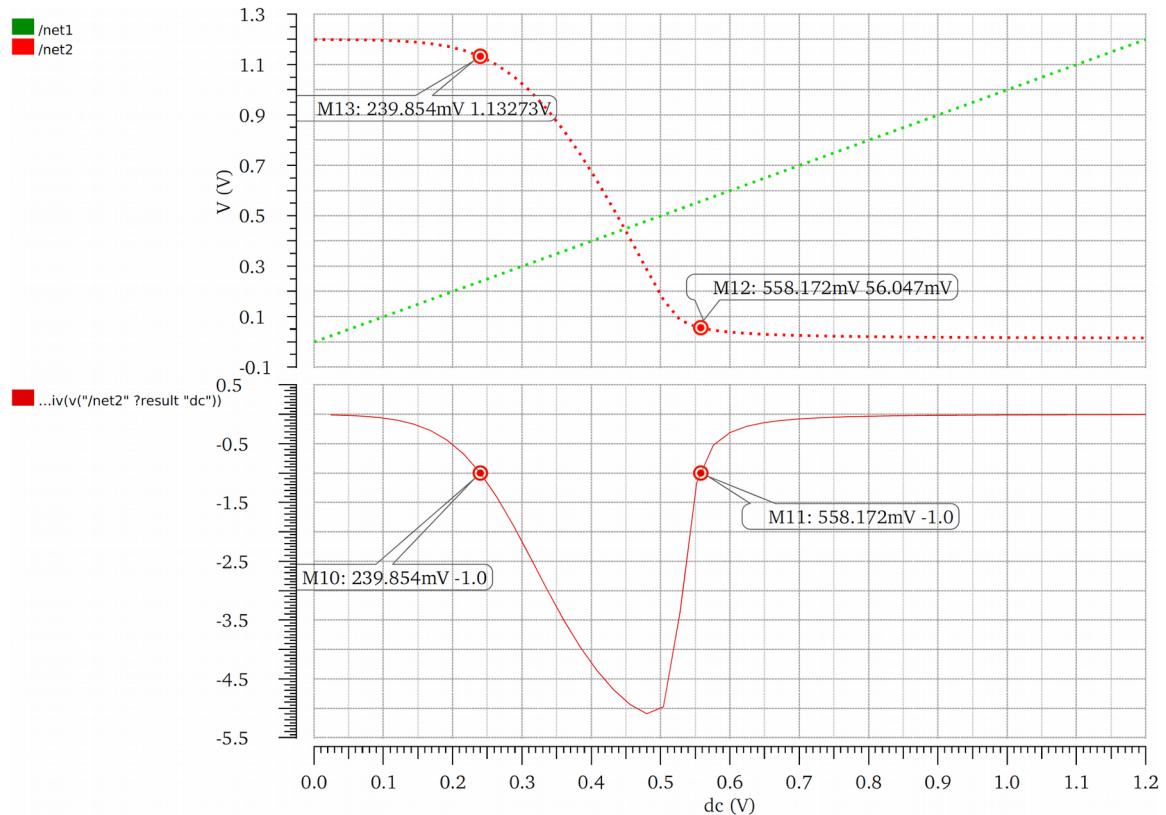
## 10, 11) DC and Transient Analysis

### DC analysis

Type	$V_{IH\_DC}$	$V_{IL\_DC}$	$V_{OH\_DC}$	$V_{OL\_DC}$
<b>CMOS</b>	0.613	0.369	1.129	0.053
<b>CMOS_Wide</b>	0.614	0.370	1.129	0.054
<b>Enhancement mode NFET</b>	0.625	0.345	0.509	0.117
<b>Enhancement mode NFET_Long</b>	0.551	0.271	0.529	0.066
<b>Resistive load (100k)</b>	<b>0.619</b>	<b>0.277</b>	<b>1.129</b>	<b>0.083</b>
<b>Resistive load_long (200k)</b>	<b>0.558</b>	<b>0.240</b>	<b>1.132</b>	<b>0.056</b>



**Figure 8: DC Analysis of the resistive inverter.**



**Figure 9: DC Analysis of the resistive long inverter.**

### Transient analysis

Type	$t_{p_{lh}}$	$t_{p_{hl}}$	$t_r$	$t_f$
<b>CMOS</b>	0.273	0.092	0.395	0.116
<b>CMOS_Wide</b>	0.071	0.028	0.095	0.029
<b>Enhancement mode NFET</b>	N/D	N/D	1.231	0.076
<b>Enhancement mode NFET_Long</b>	N/D	N/D	2.028	0.082
<b>Resistive load (100k)</b>	<b>1.014</b>	<b>0.088</b>	<b>2.092</b>	<b>0.116</b>
<b>Resistive load_long (200k)</b>	<b>2.071</b>	<b>0.062</b>	<b>4.189</b>	<b>0.123</b>