
Introduction and Physical Properties

Cell Description

The CMOS compound gate shown below in Figure 2, is a 3-Input NAND gate in which all three inputs must be low for the output to go high, or the negation of a traditional AND gate. Compared to a basic inverter, the 3-input NAND gate has a greater delay due to the increased complexity of the cell (i.e. additional transistors). Initially a NMOS stack of transistors was given that was then reduced down to a 3 input NAND gate. A hand derivation of the NAND gate is shown in figure 13.

Cell Symbol

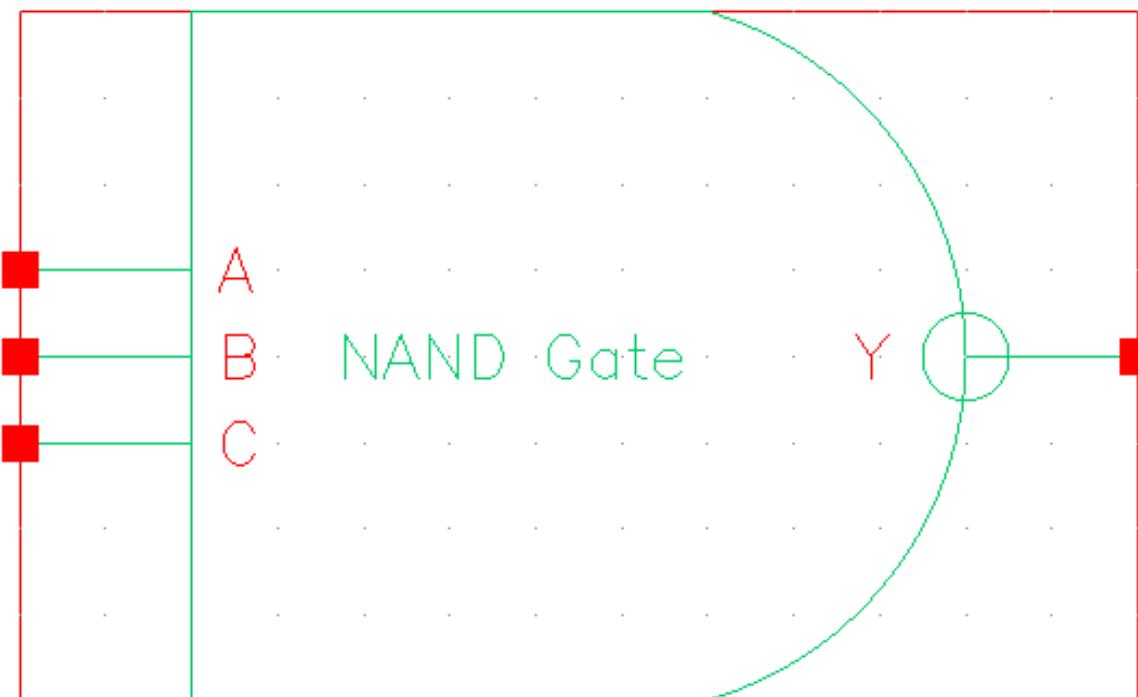


Figure 1: CMOS Compound Gate (3-Input NAND) symbol from Cadence Virtuoso.

Cell Truth Table

Cell Truth Table			
Cell Inputs {0,1}			Cell Outputs {L,H}
0	0	0	H
0	0	1	L
0	1	0	L
0	1	1	L
1	0	0	L
1	0	1	L
1	1	0	L
1	1	1	L

Cell Schematic Diagram

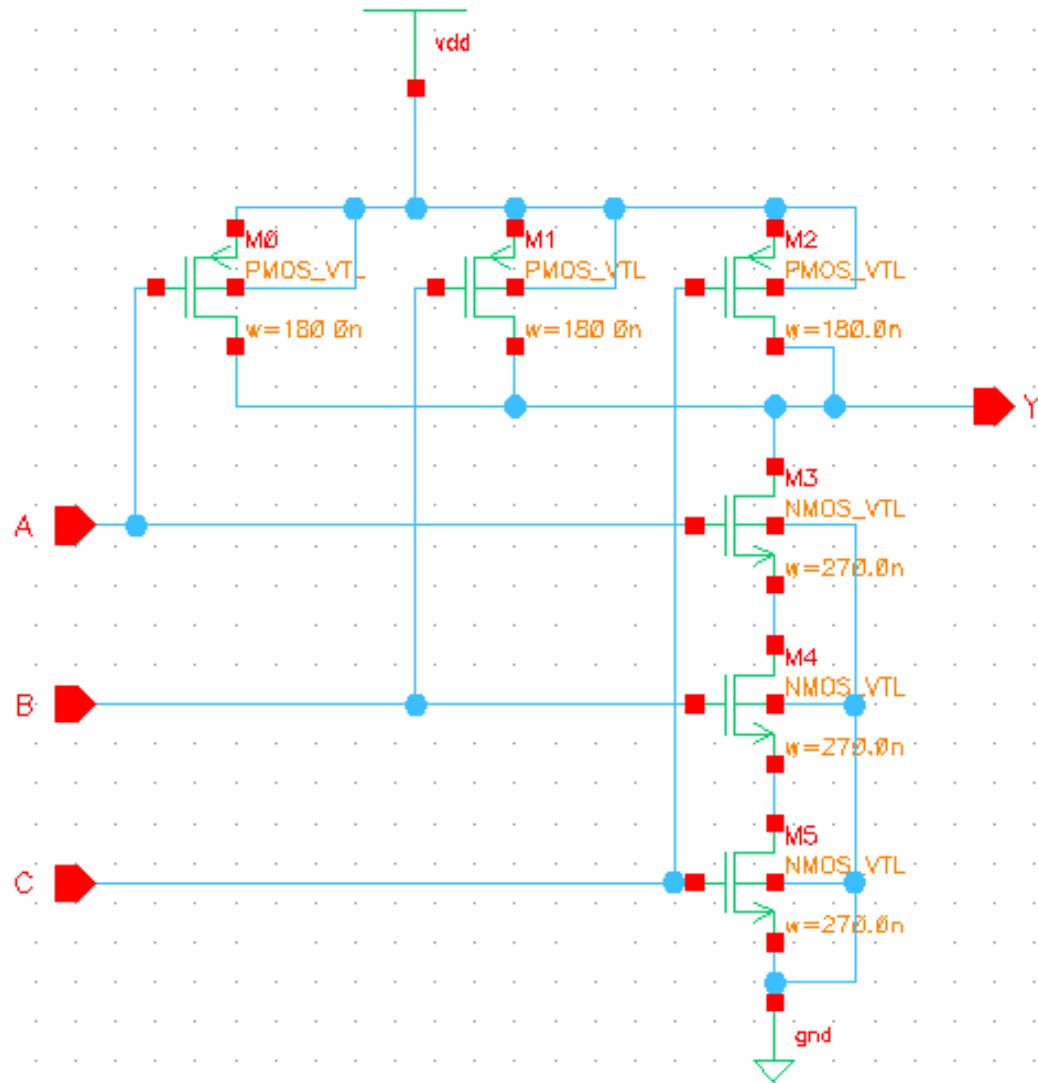


Figure 2: Schematic of CMOS compound gate (3-Input NAND) with minimum dimensions to obtain 50 ps rise and fall time.

Cell Layout Diagram and Dimensions

The following table shows the final sizing that was used for the NAND gate and was determined by using the initial sizing from part 1 of this lab assignment.

Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
M0	50	180
M1	50	180
M2	50	180
M3	50	270
M4	50	270
M5	50	270

Performance Analysis

Rise and Fall Times

Initially the NAND gate was set up with a FO4 load and the input voltage sources were adjusted to obtain input fall and rise times of 50 picoseconds. Once this was achieved the sizing of the NMOS and PMOS transistors were examined and adjusted to obtain an output fall and rise time of equal to or less than 30 picoseconds and a high to low and low to high propagation delay of 35 picoseconds with a FO4 load. Then the fall and rise times and propagation delays were measured with the following additional loads FO0, FO1, FO2 and FO8. The results are tabulated below.

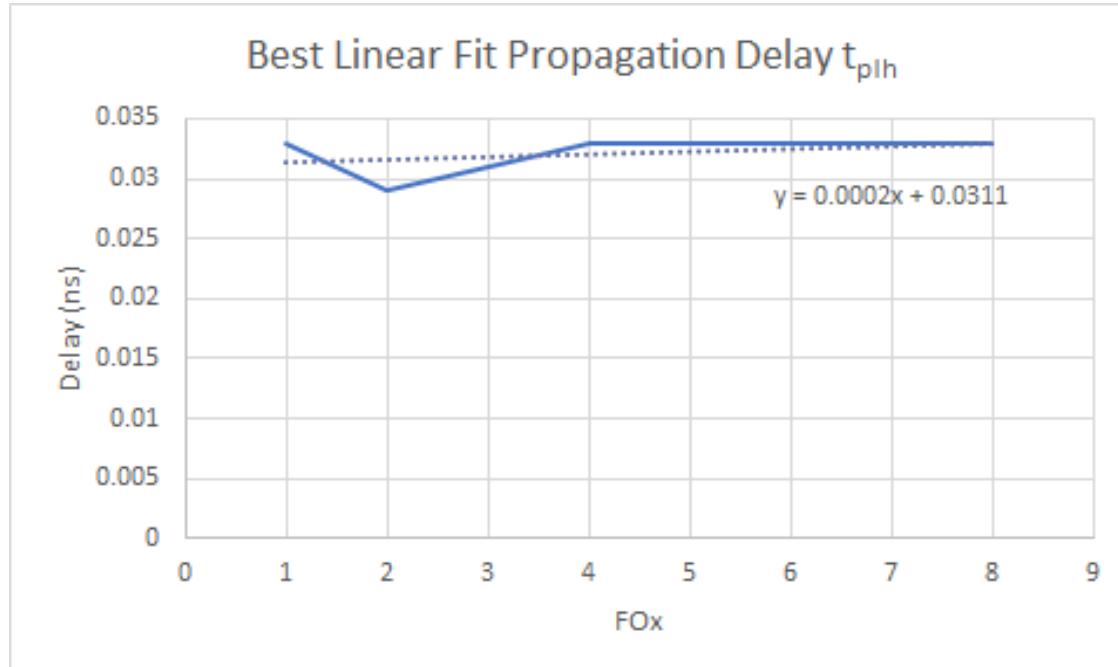
Input X: Output Rise Time Data t_r (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	0.096	0.016	0.017	0.19	0.023

Stack S, Input X: Output Fall Time Data t_f (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	0.195	0.023	0.025	0.30	0.038

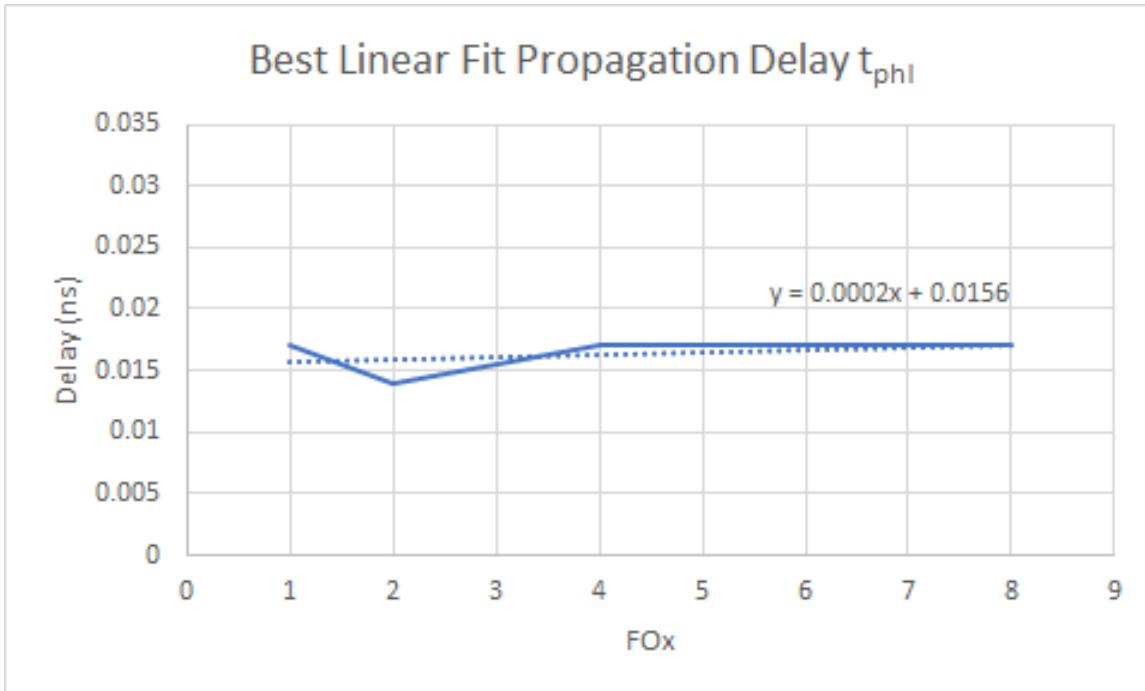
Propagation Delays

The propagation delay for the FO0 inverter load was determined to be outliers as shown in the following table and thus were emitted from the following plots for the best linear fit of the propagation delay. Both plots show the delay to be very stable regardless of the number of fanout loads.

Data Worst Case Low to High Propagation Delay Data t_{phl} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	0.147	0.033	0.029	0.033	0.033



Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	0.018	0.017	0.014	0.017	0.017



CMOS Inverter PMOS and NMOS Width Variation Table (FO4)					
PMOS and NMOS Width		Rise/Fall and Delay Time (ns)			
W _p	W _n	T _r	T _f	T _{plh}	T _{phl}
180	270	0.017	0.025	0.033	0.017

Using the initial sizing determined from part 1 of this lab (MaxSeriesP*invP & MaxSeriesN*invN, which was 1*180 and 3*90 respectively) the required rise and fall times and propagation delays were met. Thus no additional adjustments were made to the widths of the PMOS and NMOS transistors.

Please answer the following question:

What is the roles and responsibility of each member of your lab team? Who did what part of the lab? Please list the individual contribution to the lab.

Each member did the entire lab independently and compared results. The results were collaboratively edited to these two reports.

Appendix

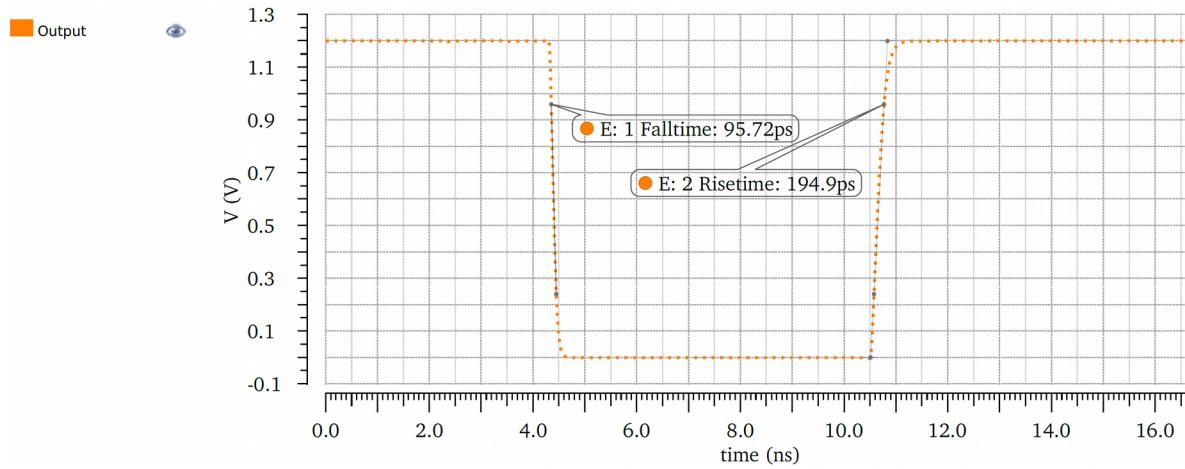


Figure 3: Transient analysis of the CMOS compound gate (3-Input NAND) showing the rise and fall time of the output with a FO0 (zero CMOS inverters) load.

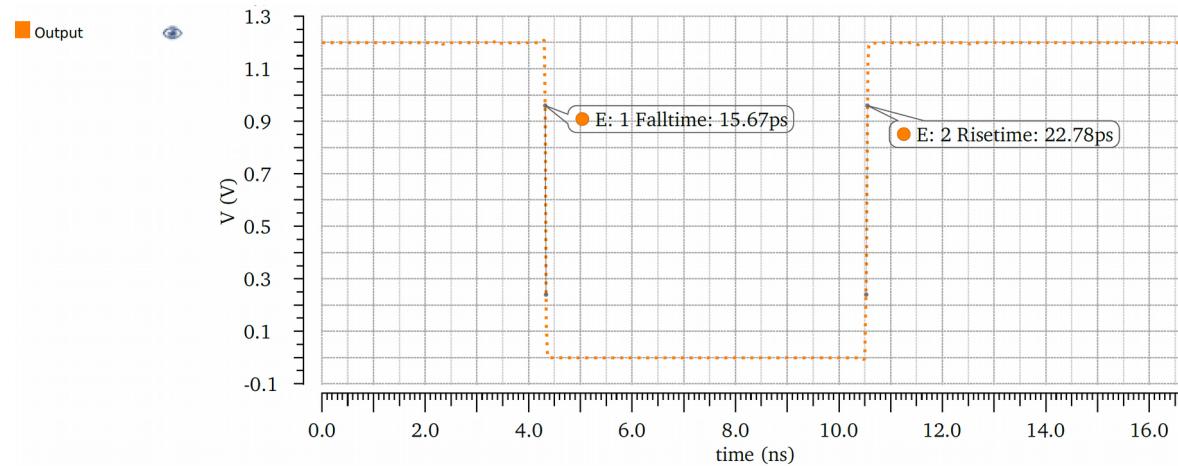


Figure 4: Transient analysis of the CMOS compound gate (3-Input NAND) showing the rise and fall time of the output with a FO1 (one CMOS inverters) load.

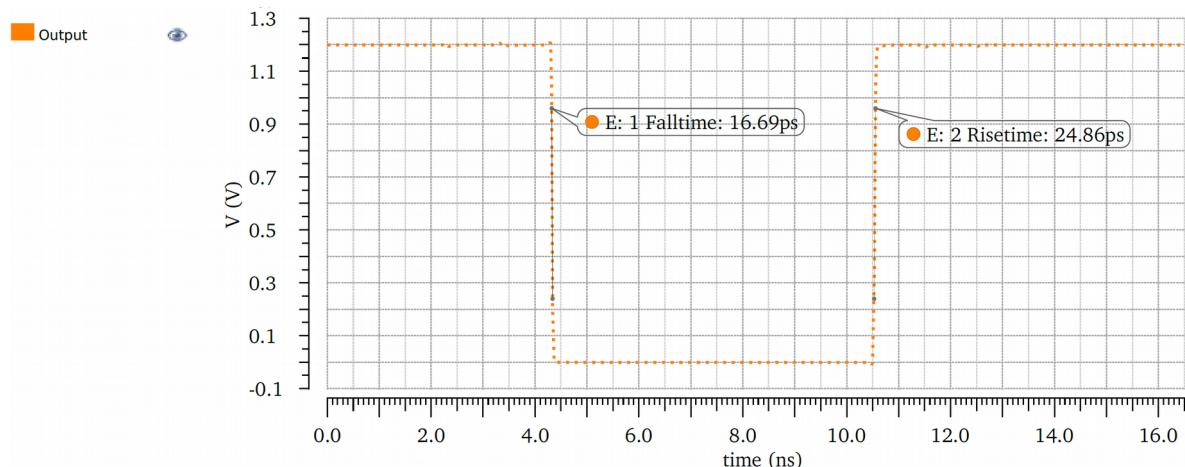


Figure 5: Transient analysis of the CMOS compound gate (3-Input NAND) showing the rise and fall time of the output with a FO2 (two CMOS inverters) load.

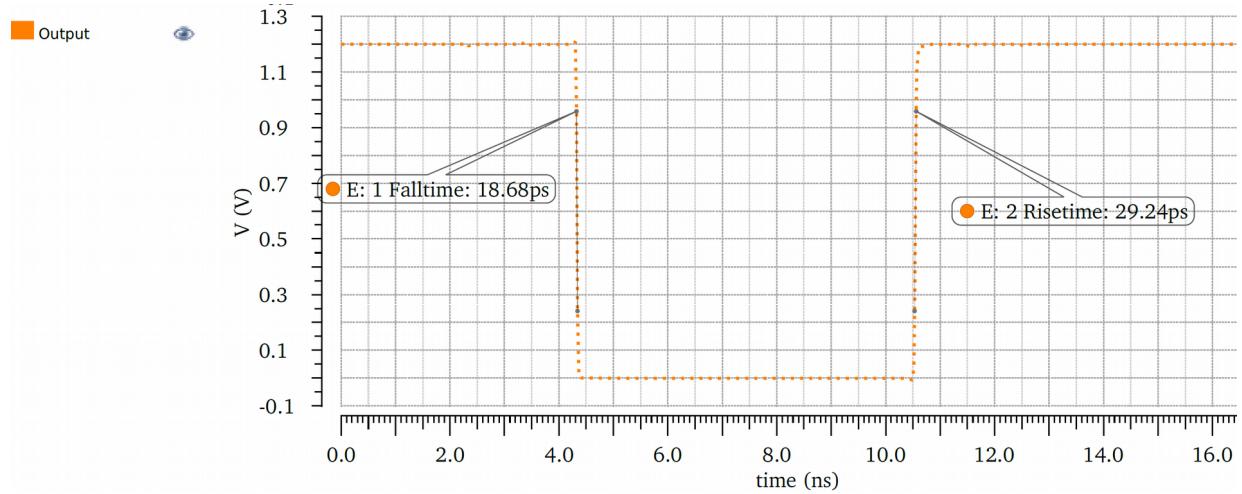


Figure 6: Transient analysis of the CMOS compound gate (3-Input NAND) showing the rise and fall time of the output with a FO4 (four CMOS inverters) load.

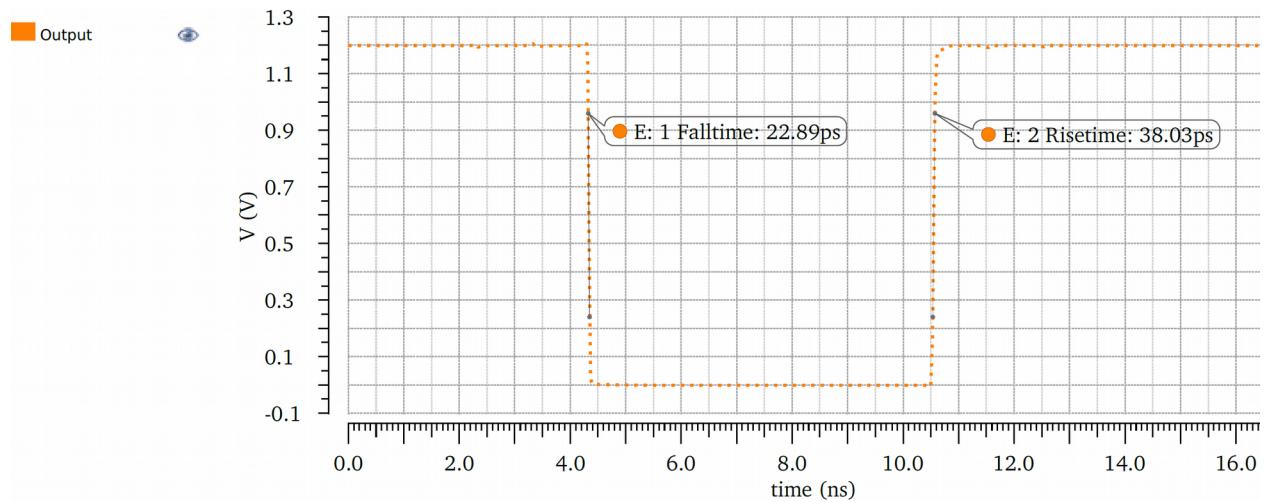


Figure 7: Transient analysis of the CMOS compound gate (3-Input NAND) showing the rise and fall time of the output with a FO8 (eight CMOS inverters) load.

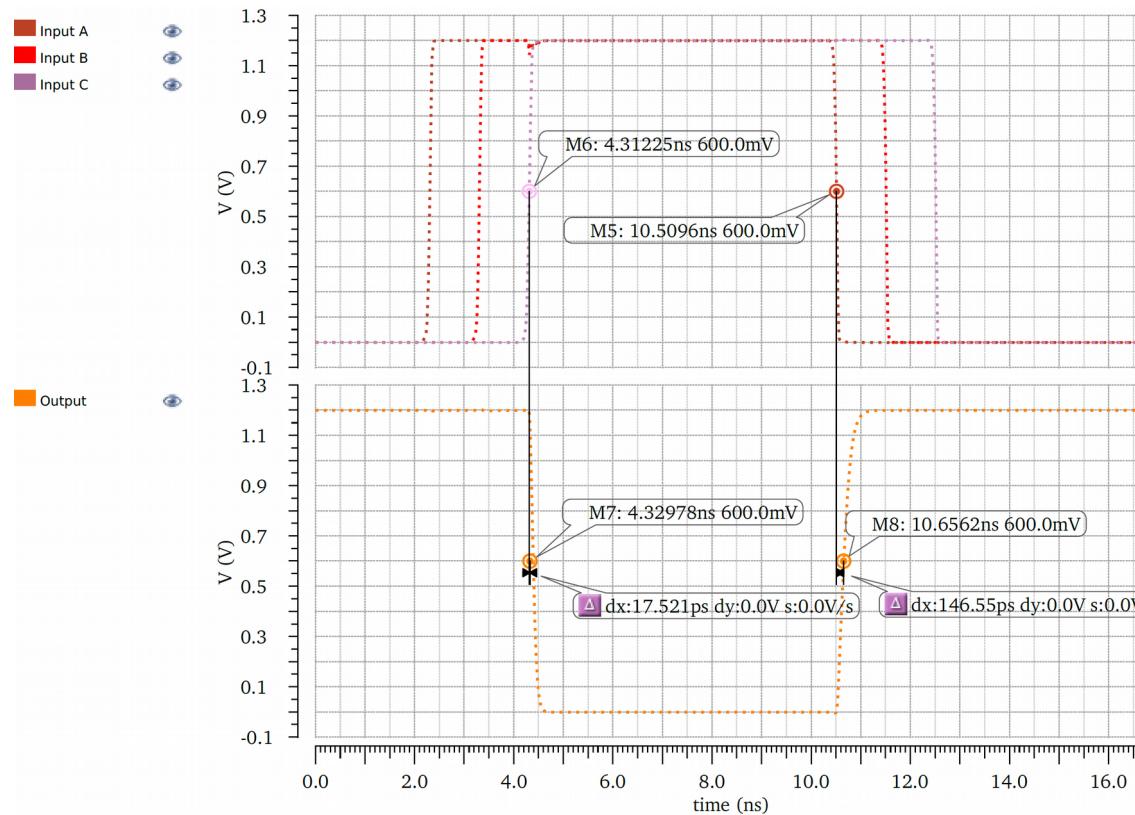


Figure 8: Transient analysis of the CMOS compound gate (3-Input NAND) showing the propagation delays with a FO0 (zero CMOS inverters) load.

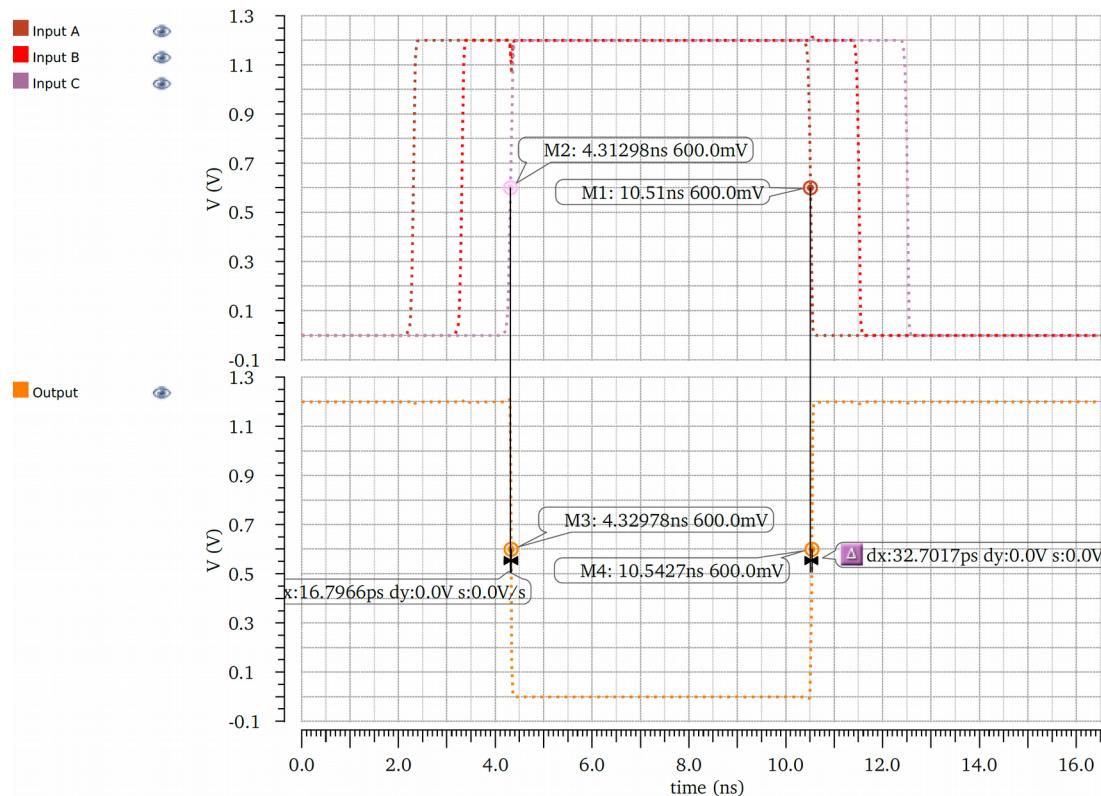


Figure 9: Transient analysis of the CMOS compound gate (3-Input NAND) showing the propagation delays with a FO1 (one CMOS inverters) load.

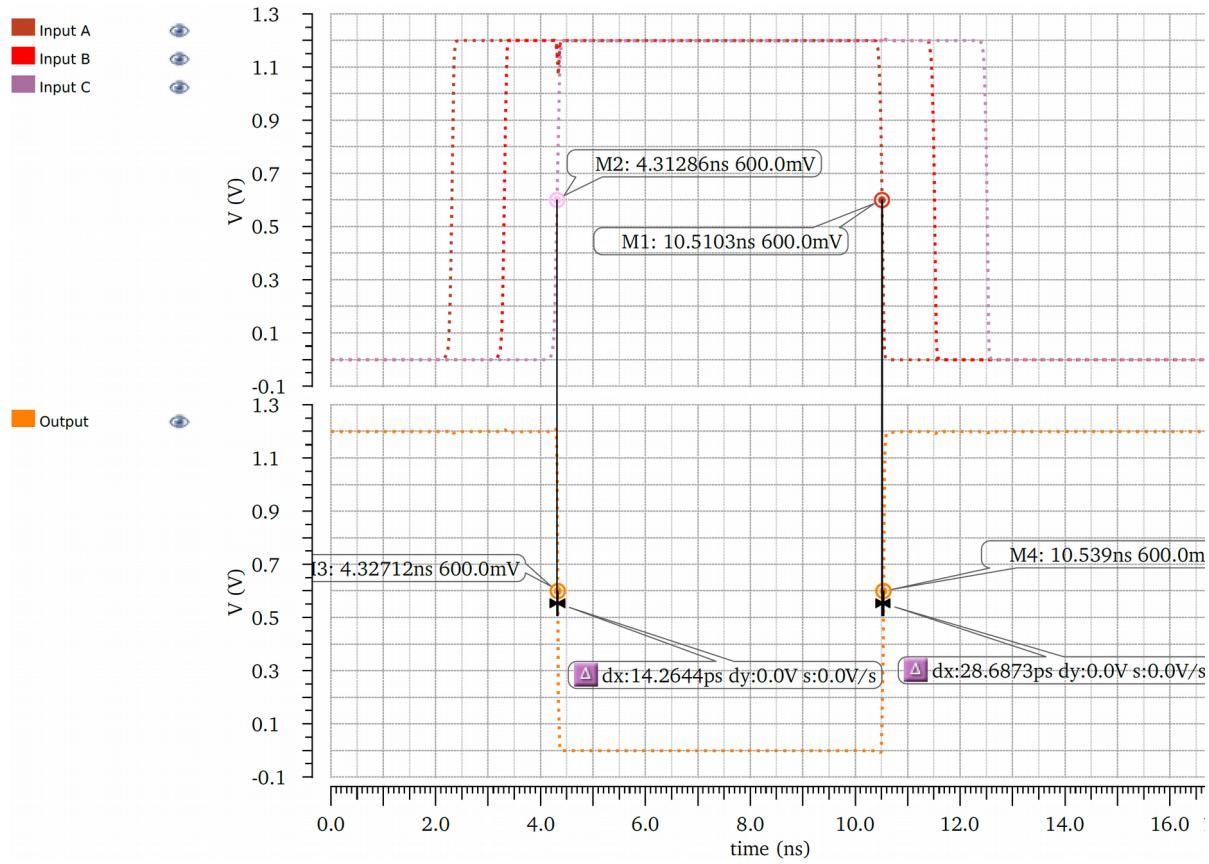


Figure 10: Transient analysis of the CMOS compound gate (3-Input NAND) showing the propagation delays with a FO2 (two CMOS inverters) load.

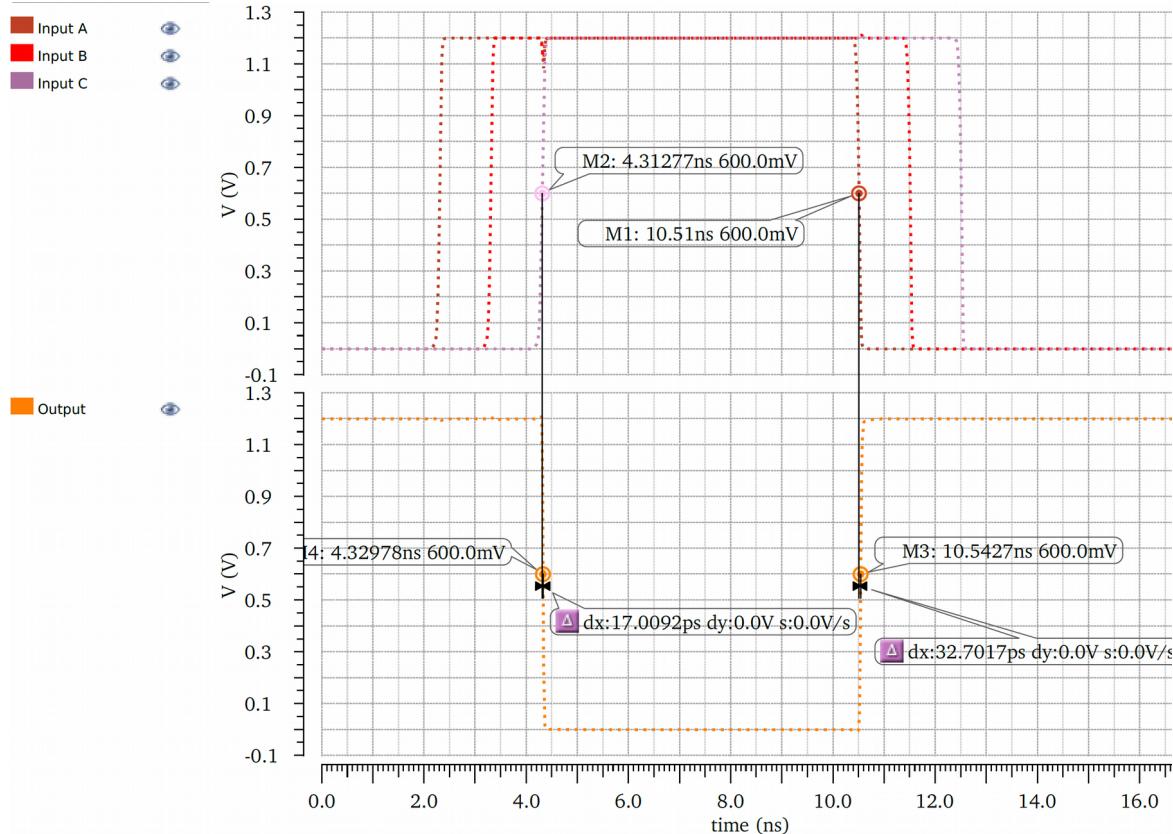


Figure 11: Transient analysis of the CMOS compound gate (3-Input NAND) showing the propagation delays with a FO4 (four CMOS inverters) load.

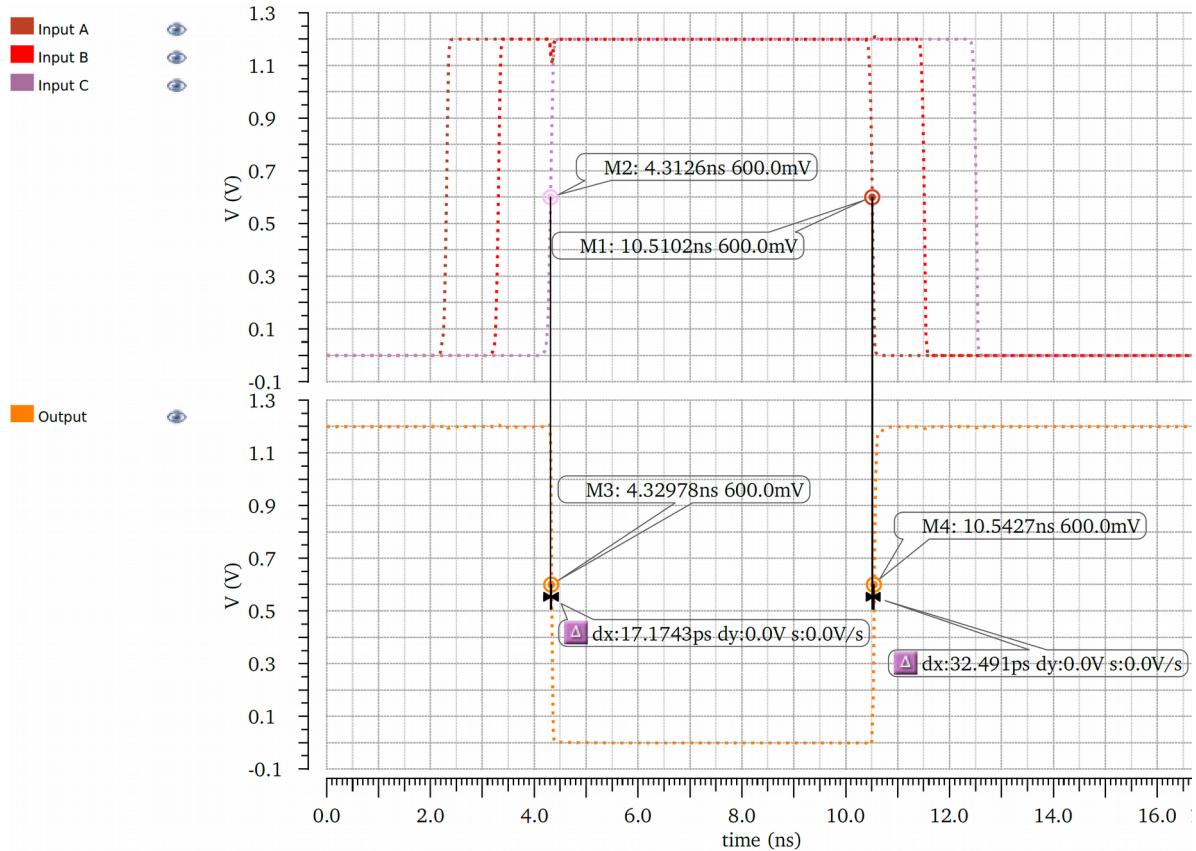
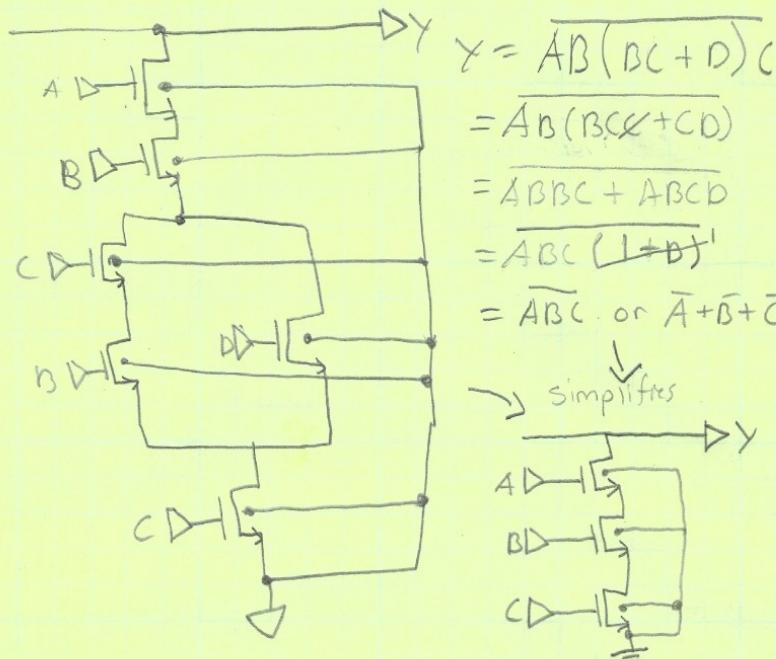
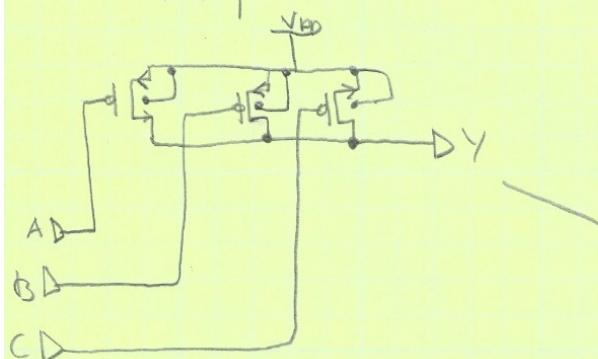


Figure 12: Transient analysis of the CMOS compound gate (3-Input NAND) showing the propagation delays with a FO8 (eight CMOS inverters) load.

CMOS Complement Gate

series = AND
parallel = OR

PMOS complement stack

complement of $Y = \overline{ABC} \rightarrow Y = A + B + C$ 

Complete CMOS Design

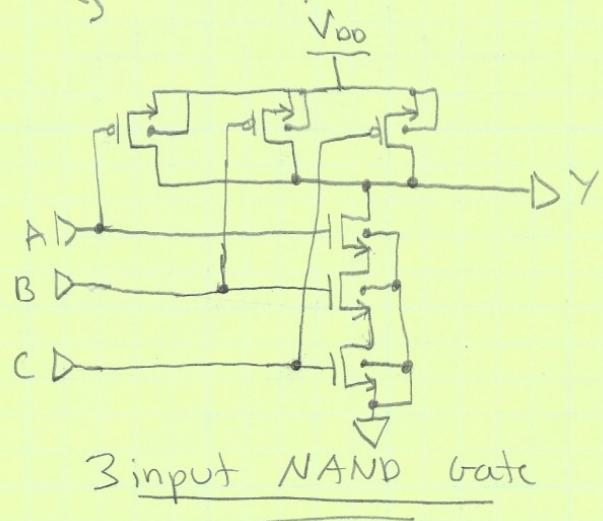


Figure 13: Hand derivation minimizing the initial NMOS stack given for Part 2 of this lab.