Laboratory #4: Open loop system construction and testing: the Buck dc-to-dc converter

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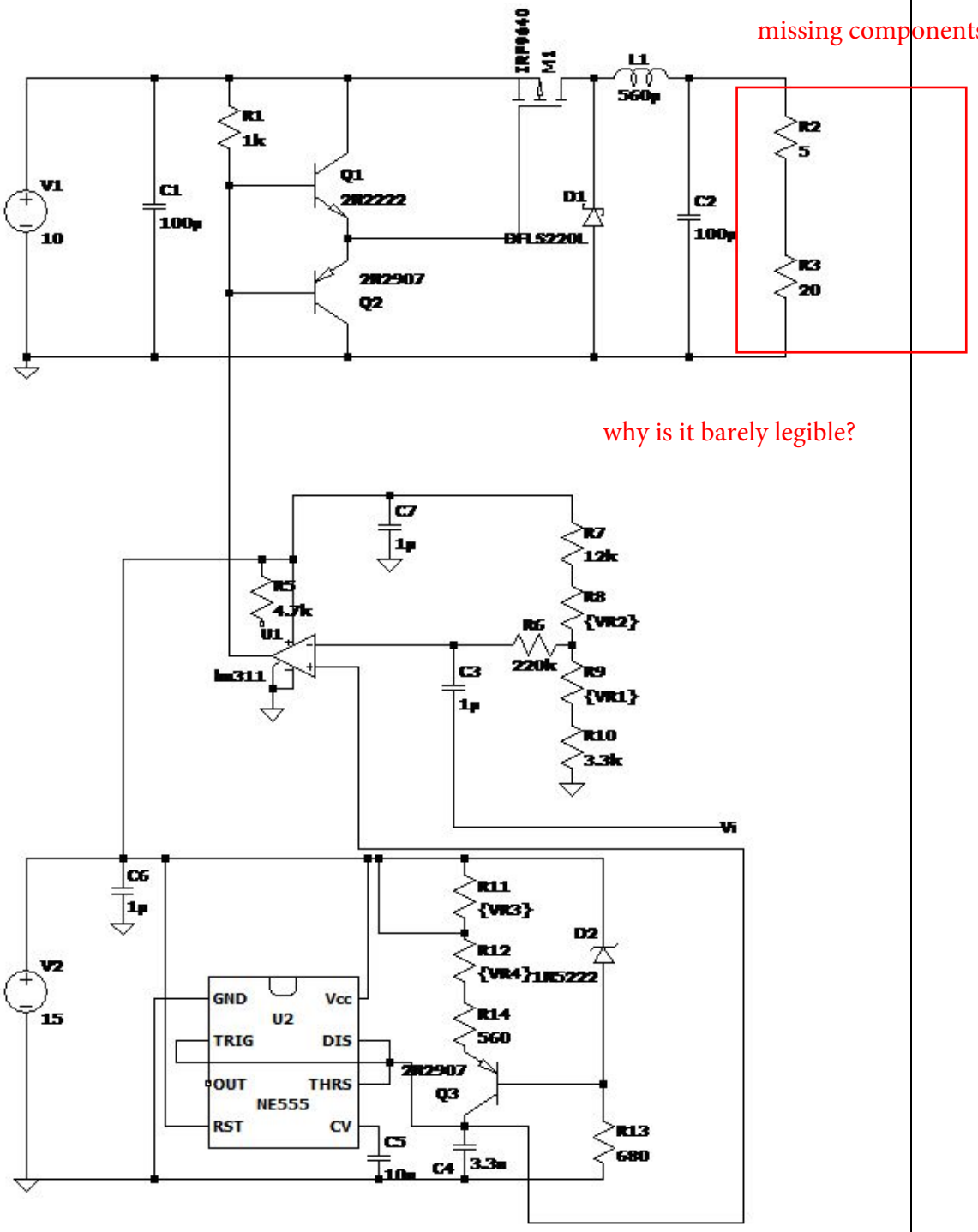
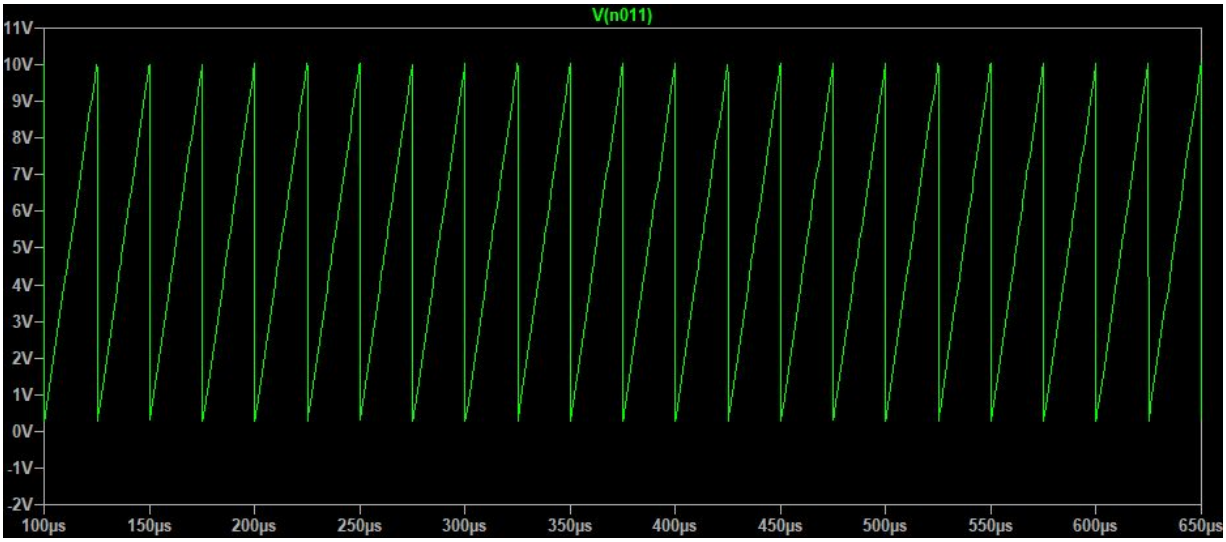
missing components



LTSpice schematic of Buck dc-to-dc converter

Task 1b:



LTSpice simulation plot of 40 kHz sawtooth waveform

Minimum sawtooth voltage	277 mV
Maximum sawtooth voltage	10 V
Peak-to-peak sawtooth voltage	9.73 V

Task 2b:

The potentiometer VR1 in the lab assignment is represented with the resistors R8 and R9 in the LTSpice schematic shown above. R8 is determined by the wiper value, W, multiplied by the resistance of the entire potentiometer and R9 is determined by $1 - W$, multiplied by the resistance of the entire potentiometer.

$$R8 = W * 10\ k\Omega$$

$$R9 = (1 - W) * 10\ k\Omega$$

$$0 < W < 1$$

The maximum voltage at the non-inverting input of the potentiometer is given when the wiper on the potentiometer VR1 in the lab assignment is 0%. This means that there is $10\ k\Omega$ in series with the R10 resistor and the voltage at the inverting input is:

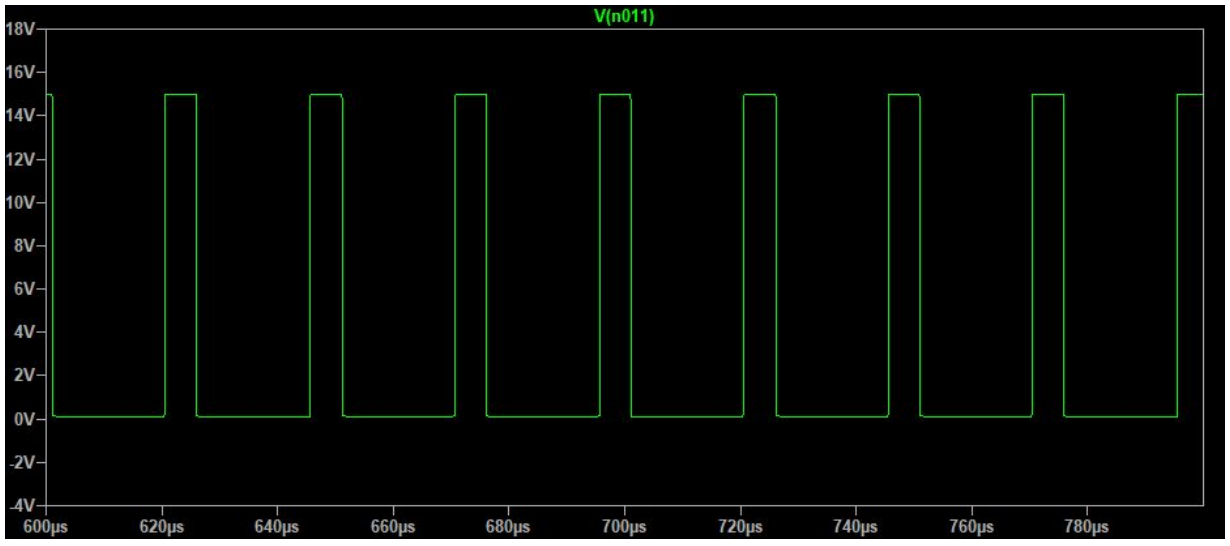
$$V_{max\ inverting} = 15\ V\ \frac{R10+10\ k\Omega}{(R10+10\ k\Omega)+R7} = 7.89\ V$$

The minimum voltage at the non-inverting input of the potentiometer is given when the wiper of the potentiometer is 100%. This means that there is $10\ k\Omega$ in series with the R7 resistor and the voltage at the inverting input is:

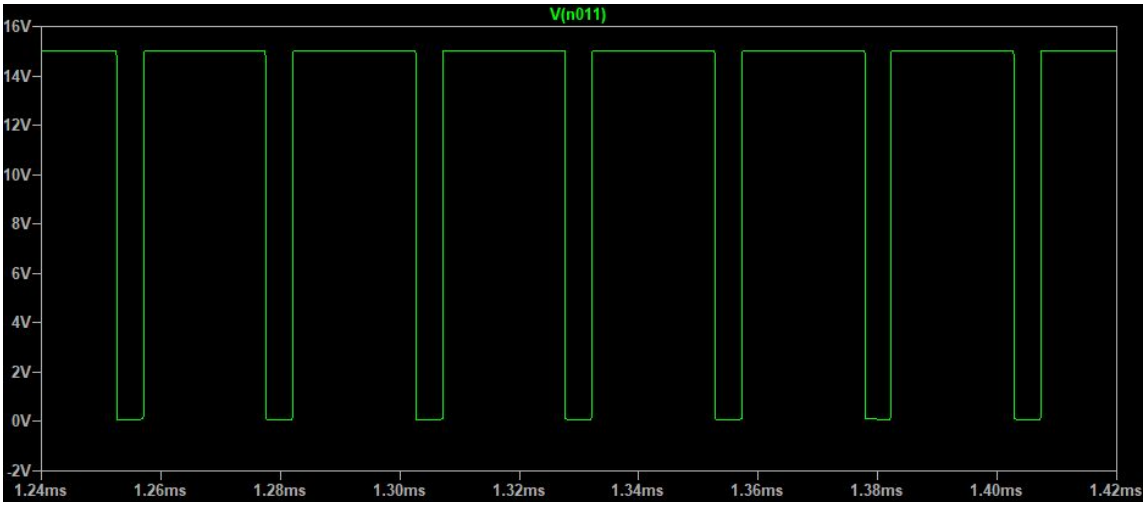
$$V_{min\ inverting} = 15\ V\ \frac{R10}{R10+(R7+10\ k\Omega)} = 1.96\ V$$

Therefore the minimum and maximum achievable duty ratios are determined by the peak-to-peak voltage of the sawtooth waveform and the voltage applied to the inverting input of the LM311 comparator.

$$D_{max} = 1 - \frac{1.96\ V}{9.73\ V} = 0.8 \qquad D_{min} = 1 - \frac{7.89\ V}{9.73\ V} = 0.19$$



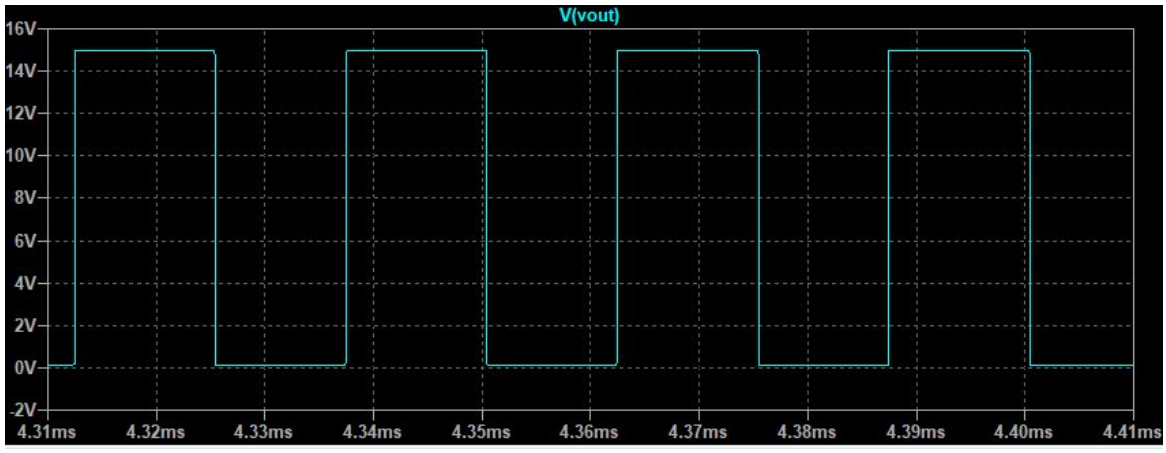
Simulation of minimum duty ratio



Simulation of maximum duty ratio

Minimum Duty Ratio (Calculated)	0.19
Maximum Duty Ratio (Calculated)	0.8
Minimum Duty Ratio (Simulation)	0.21
Maximum Duty Ratio (Simulation)	0.82

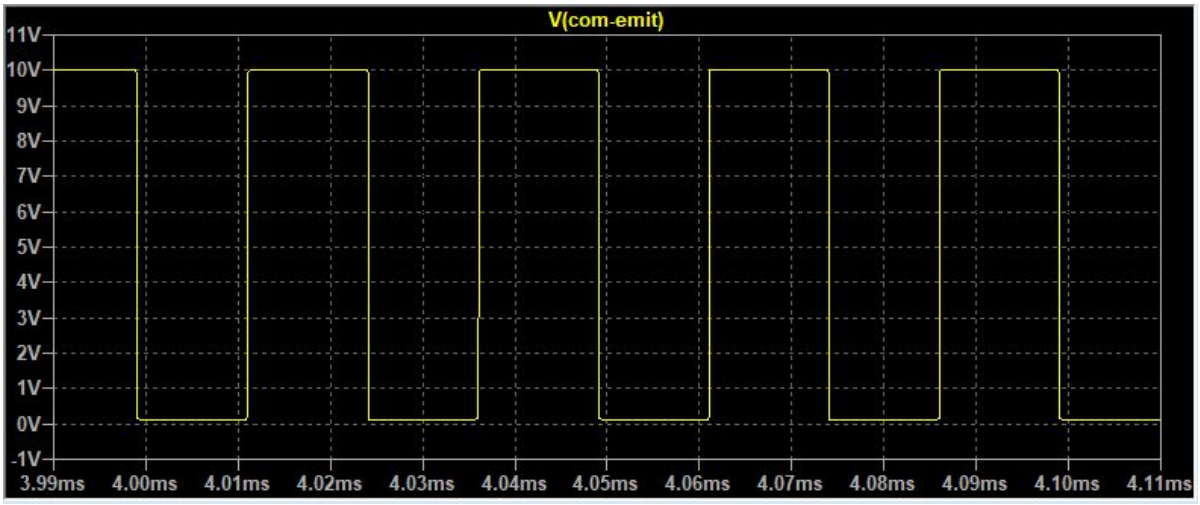
Task 2c:



Output of LM311

From the simulation plot above, we can see a output voltage of 15Vpp with a 50% duty ratio.

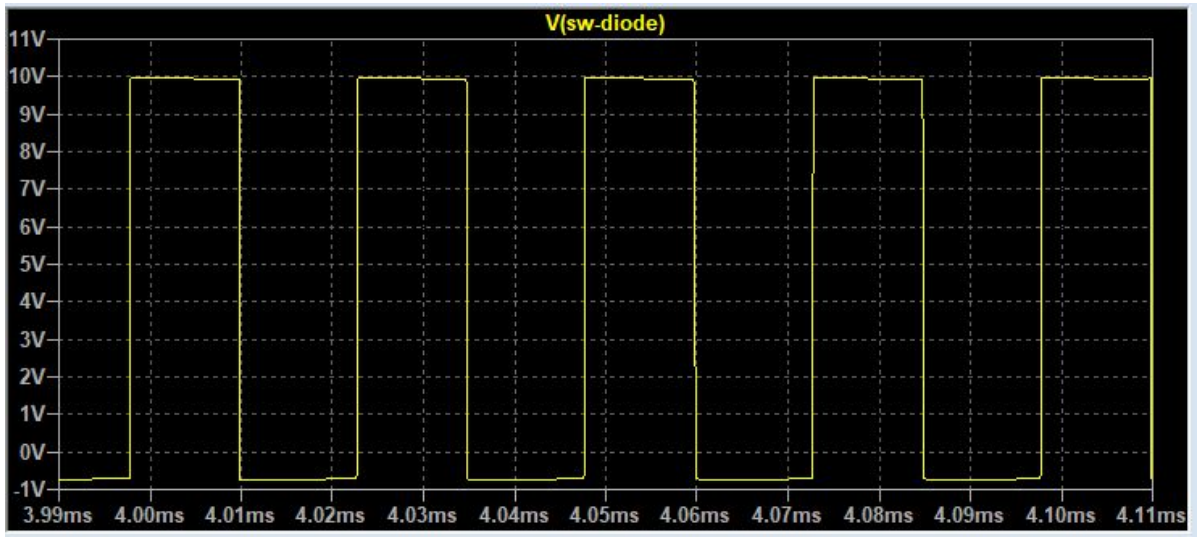
Task 3b:



Voltage at Common Emitter of Driver Stage

From the simulation plot above, the common emitter voltage between the two transistors of the driver stage is 10Vpp.

Task 4b:



Voltage Across Switching Diode

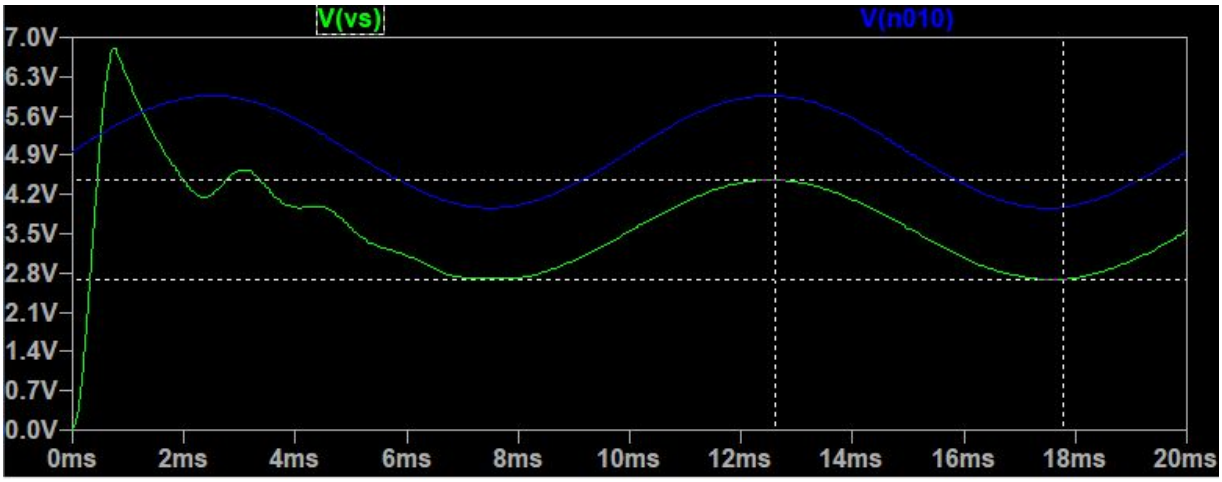
From the above simulation plot, we can see a voltage of about 10Vpp across the switching diode in the buck converter.

Task 4c:

With a duty cycle of 0.5 I am measuring 4.48 volts after transients settle down.

One would expect an average value of 5 volts however there are some losses in each non ideal component in the circuit. This would need to be compensated by slightly increasing the duty ratio for a given output voltage.

Task 4d:



Input and output sinusoid

Output peak-to-peak	1.78V
Input peak-to-peak	2V
Gain $(\frac{output}{input})$	0.89

This represents the forward gain of the open loop system.

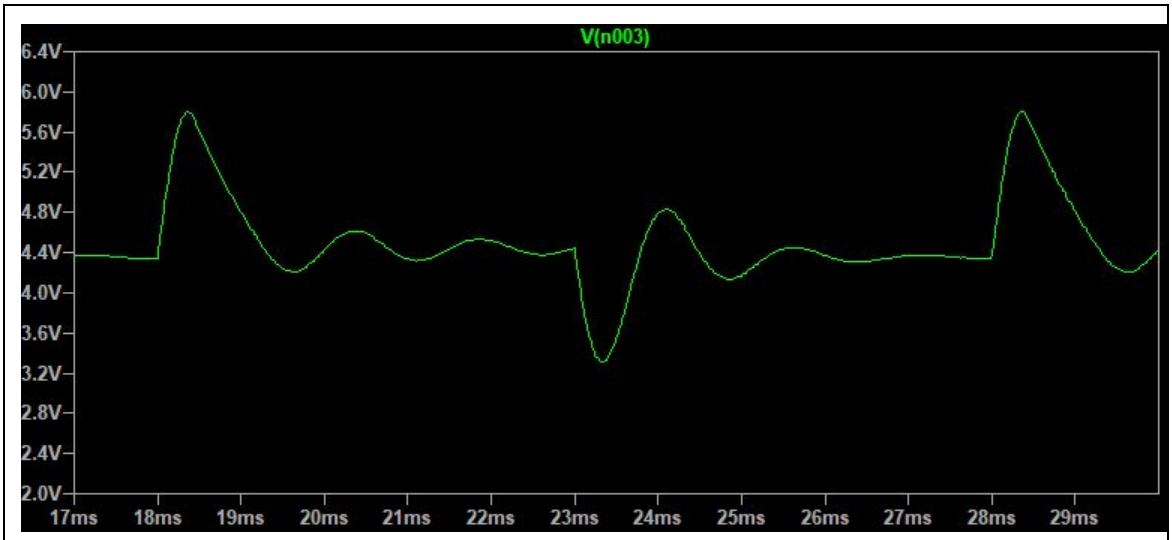
$$G_{vd} \cdot G_{PWM} = \frac{\hat{v}}{\hat{vc}}$$

Where, $G_{PWM} = \frac{\hat{d}}{\hat{vc}} = \frac{1}{Vm}$

The gain consists of two components, the duty ratio to output voltage transfer function of the buck converter power stage (G_{vd}) and the pulse width modulator transfer function (G_{PWM}). Together, $G_{vd} \cdot G_{PWM}$ form the control to output transfer function ($\frac{\hat{v}}{\hat{v}c}$).

The input and output are in-phase. The compensator does not need to provide phase inversion because the output is in-phase with the input for small AC signals.

Task 5b:



Output voltage response to stepped load change

Δv , maximum pk-pk output voltage deviation = 3.31V

SSE, steady state error = 220mV

Results:

Sawtooth table

	Minimum Value	Maximum Value	Vm = pk-pk voltage
Sawtooth (Task 1b)	277 mV	10V	9.73 V

Duty ratio table

Task 2b	Duty Ratio (D)
Min. D: formula to determine min. D	$D_{min} = 1 - \frac{7.89\ V}{9.73\ V} = 0.19$
Min D: formula evaluated	0.19
Min. D: measured in lab	0.21
Max D: formula to determine max. D	$D_{max} = 1 - \frac{1.96\ V}{9.73\ V} = 0.8$
Max D: formula evaluated	0.8
Max D: measured in lab	0.82

Sinusoid table

Input Sine Voltage (Task 4d)	pk-to-pk = 2V
Output Sine Voltage (Task 4d)	pk-to-pk = 1.78V
Output/Input Ratio (Task 4d)	0.89

Δv and SSE table

	From Hardware from Lab 4, Task 5b	Using PECS from Lab 3, Task 5	Using Matlab from Lab 3, Task 6e
Δv	3.31V	2.9V	3.41V
SSE	220mV	177mV	183mV

The change in output voltage is proportional to changes in the load. This is because there are losses in the circuit. The discrepancies in our values can be explained by the difference in modeling among the three simulations. The main variation between

the PECS simulation and the LTspice simulation was the use of a clock controlled switch and a voltage controlled mosfet, respectively.

Lab 4 Grading Sheet

1. One photo of constructed circuit (power stage on perf board and the rest on solderless board?) 6 /7
2. Task 1b:
   - (i) Screenshot of sawtooth (40 kHz?) _____/1
   - (ii) Minimum values of sawtooth _____/1
   - (iii) Maximum values of sawtooth _____/1
3. Task 2b:
   - (i) Minimum achievable duty ratio calculation _____/2
   - (ii) Maximum achievable duty ratio _____/2
   - (iii) Minimum achieved duty ratio value obtained in the lab _____/1
   - (iv) Maximum achieved duty ratio value obtained in the lab _____/1
4. Task 2c:
   - (i) Screenshot of output of LM311 (15 V pk-pk? and 50% duty ratio?) ____/1
5. Task 3b:
   - (i) Screenshot of output of mosfet driver (10 V pk-pk?) _____/1
6. Task 4b:
   - (i) Screenshot of diode voltage (10 V pk-pk? Sharp transitions?) _____/1
7. Task 4c:
   - (i) Measured value of average output voltage _____/1
   - (ii) Expected value of average output voltage (why?) _____/1
8. Task 4d:
   - (i) Screenshot of input and output sinusoidal _____/1
   - (ii) Measured pk-pk value of output sinusoid _____/1
   - (iii) Measured pk-pk value of input _____/1
   - (iv) Gain = ratio of output/input calculated _____/1
   - (v) What does this gain represent? _____/1
   - (vi) What are the components of this gain? _____/2
   - (vii) In-phase or out-of-phase? _____/1
   - (viii) Will the compensator need to provide phase inversion so as to provide negative feedback? 0 /1
9. Task 5b:
   - (i) Screenshot of output voltage response to stepped load change _____/1
   - (ii) Δv, maximum pk-pk output voltage deviation _____/1
   - (iii) *SSE*, steady state error _____/1

10. Results (summary):

(i) Sawtooth table _____/1

(ii) Duty ratio table _____/1

(iii) Sinusoid table _____/1

(iv) Δv and SSE table _____/5

(v) Observations concerning step response _____/4

Report: 4 /5

Total: 47 /50