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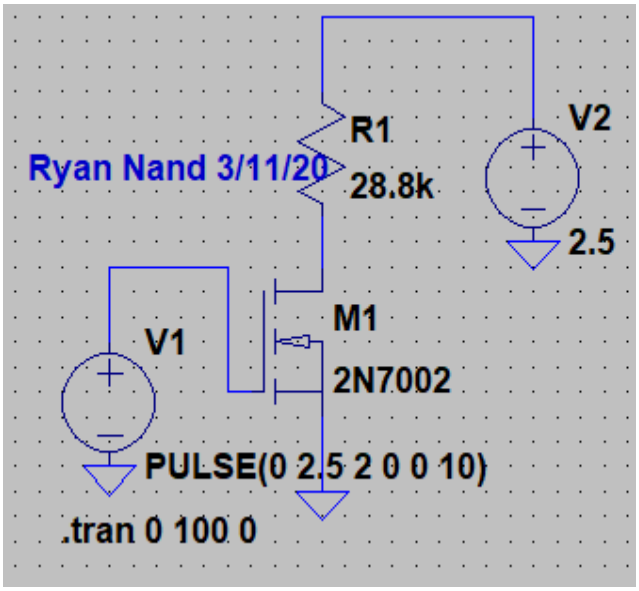
ECE 321

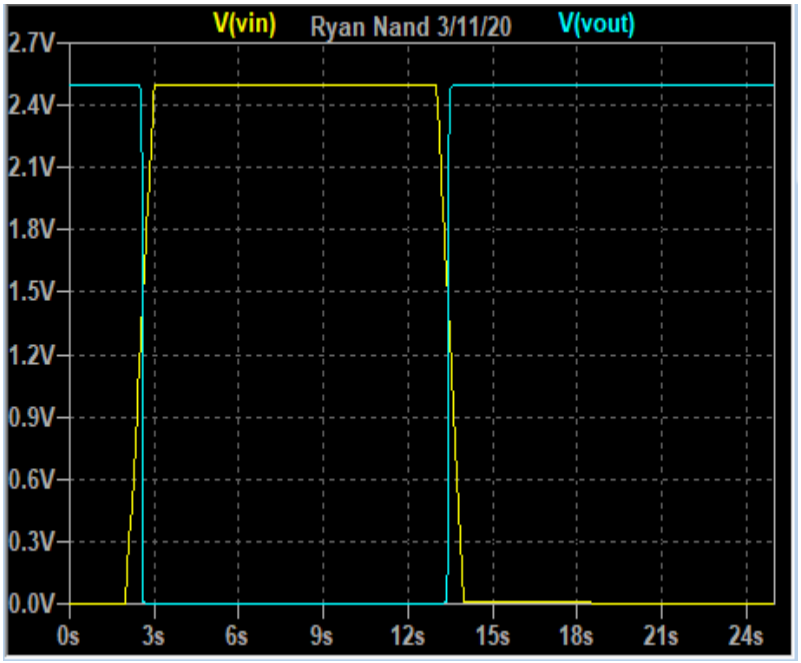
Lab 4: Logic Gates

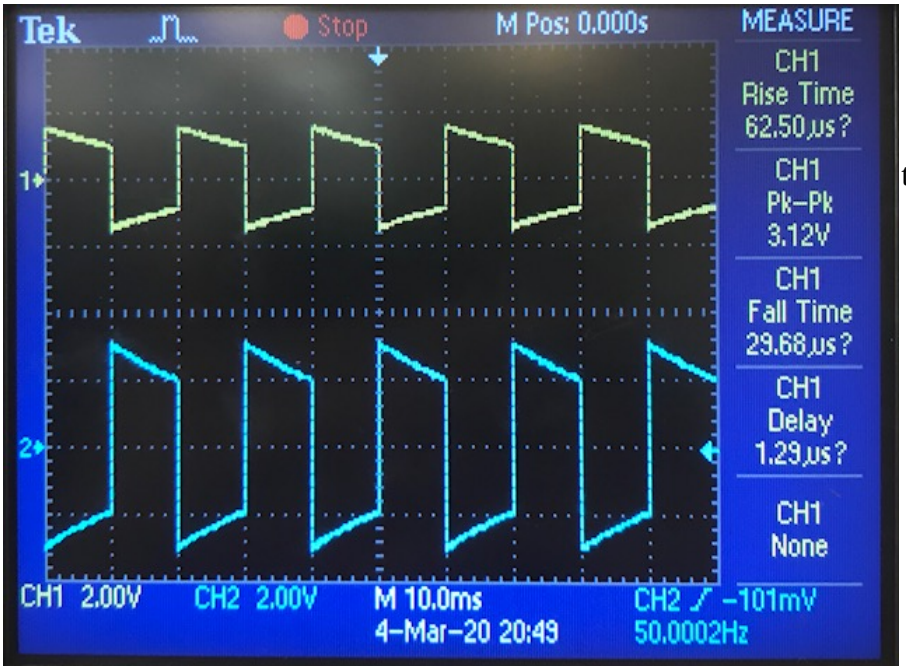
Introduction

The purpose of this lab is to design and build logic gates using MOSFETs. There will be four inverter circuits, one NAND circuit, and one NOR circuit. Both the NAND and NOR will be implemented using CMOS. The inverters will have various types of circuits. There will be an implementation and simulation for each circuit.

Circuit 1: Inverter circuit with resistance load







As you can see, both the simulation and design has the inputs inverted as the outputs. So the circuit works as intended. For the design, the rise time, fall time, and delay are all in the microsecond range. However, in the simulation those are in the millisecond range. This is due to the transistor characteristics and input differences (could not implement the exact input with both the simulation and signal generator.

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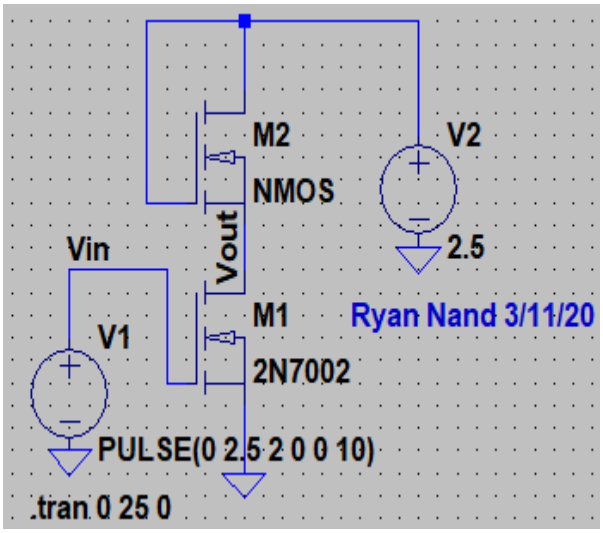
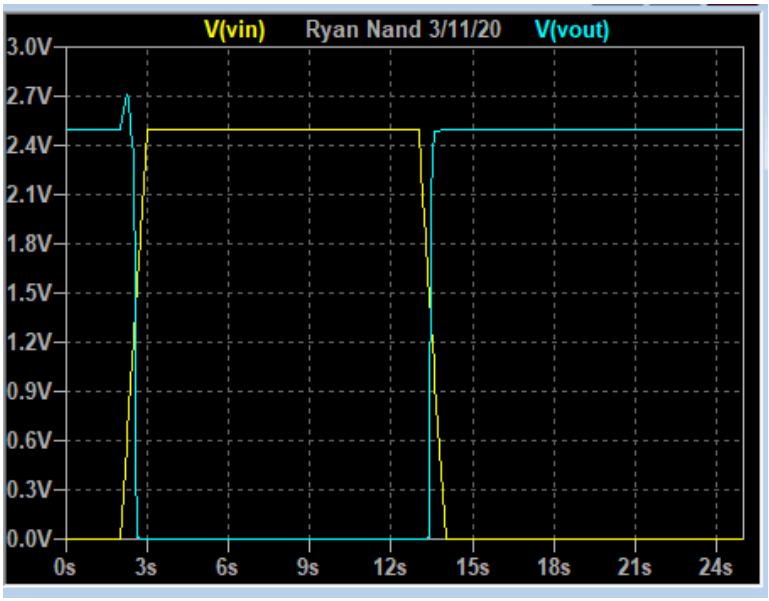
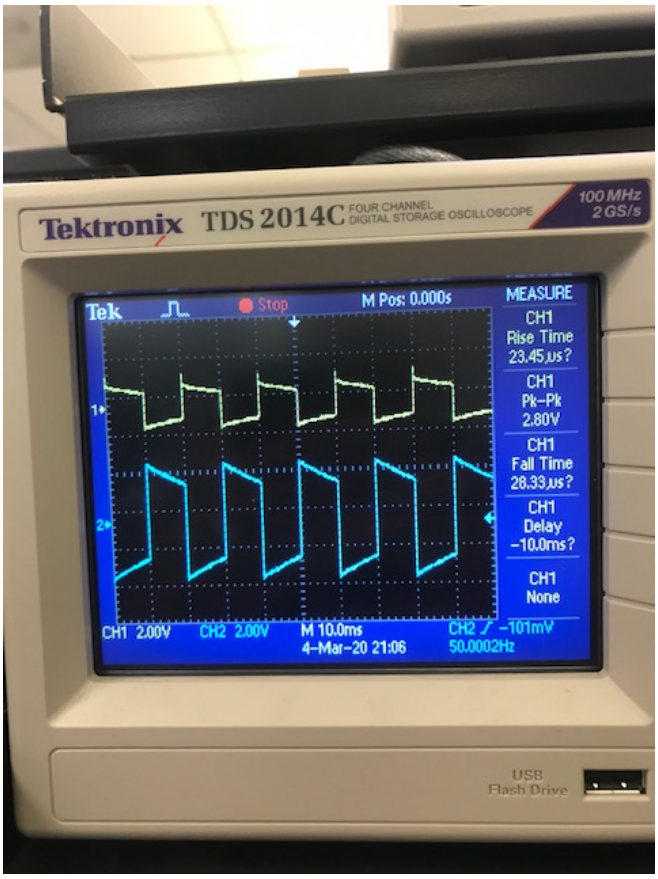
Circuit 2-3: Inverter with enhancement and depletion mode

Enhancement mode







This circuit produced some overshoot at the output. However, the circuit still inverts the input at the output and works as intended. That being said, the delay, fall time, and rise time is very similar to what the previous circuit provided.

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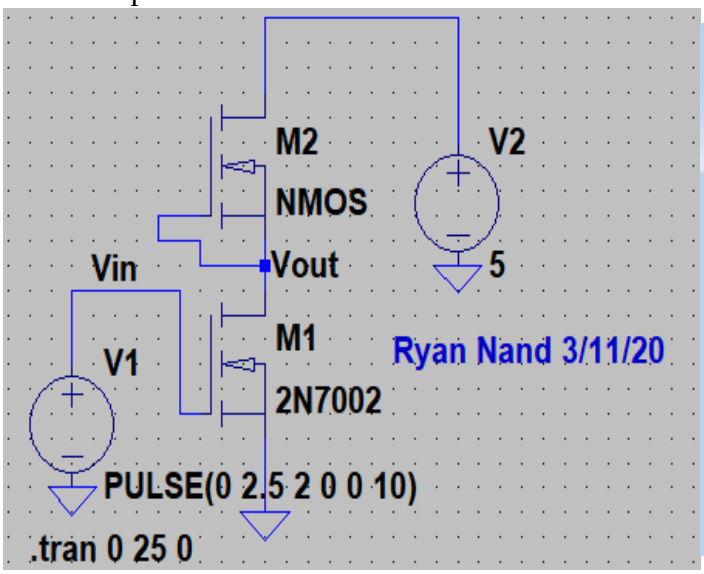
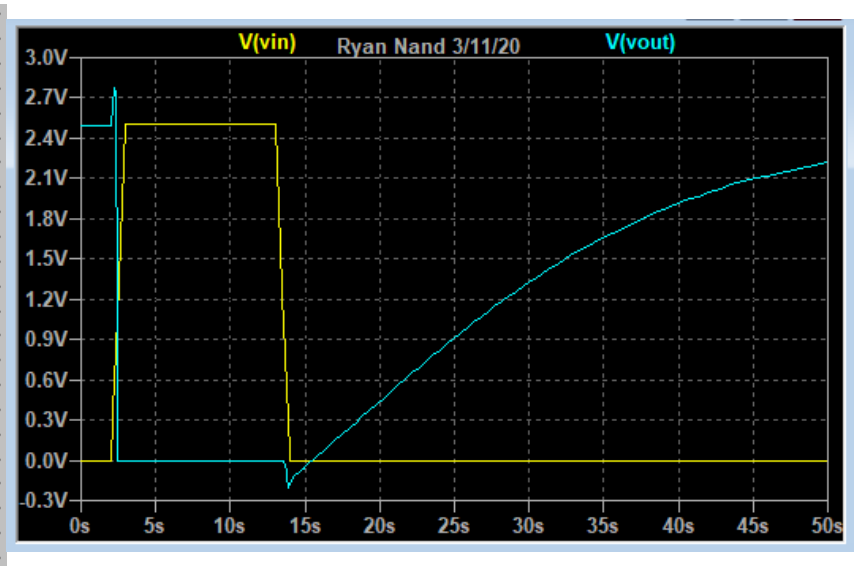
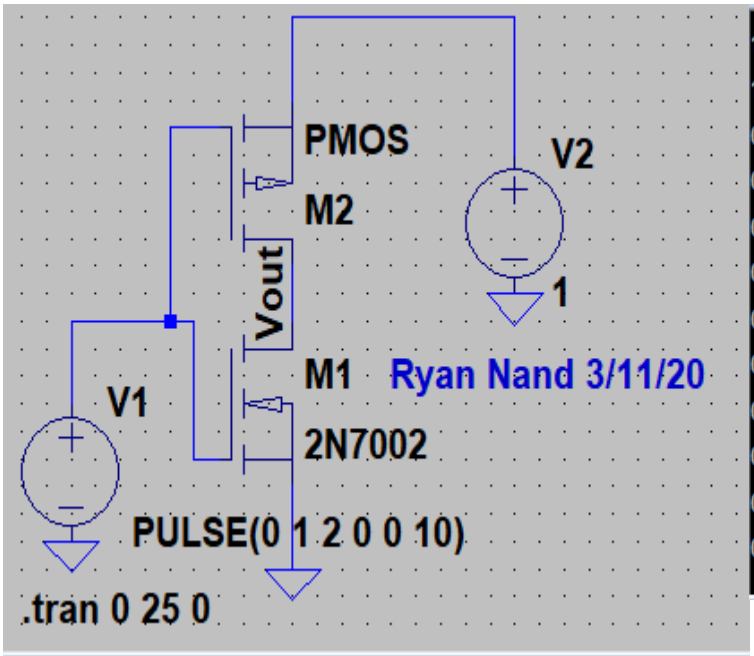
Depletion mode

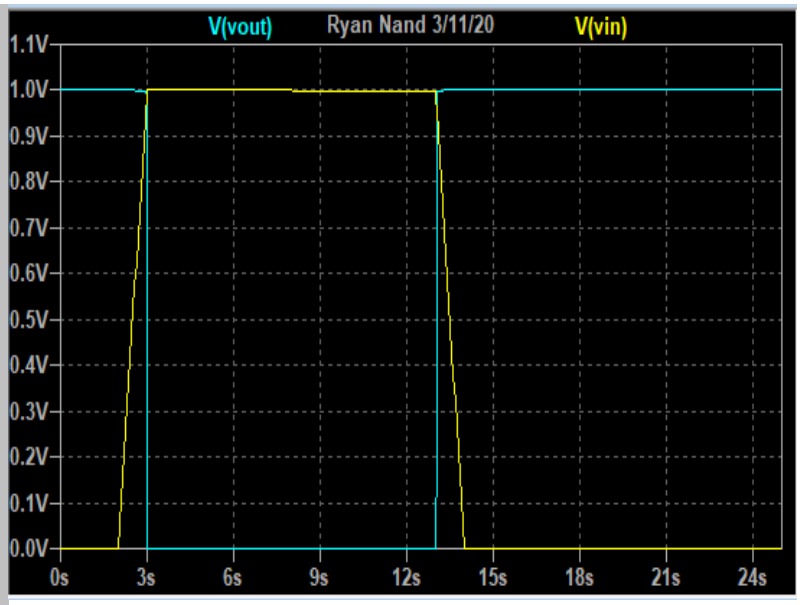




This circuit does not work as well as the others. In depletion mode, there is a big rise time. It is displayed in the simulations. There is the overshoot in the output as well. It is not an ideal inverter, however, it is still inverting the output. Therefore, being an inverter.

Circuit 4: CMOS Inverter





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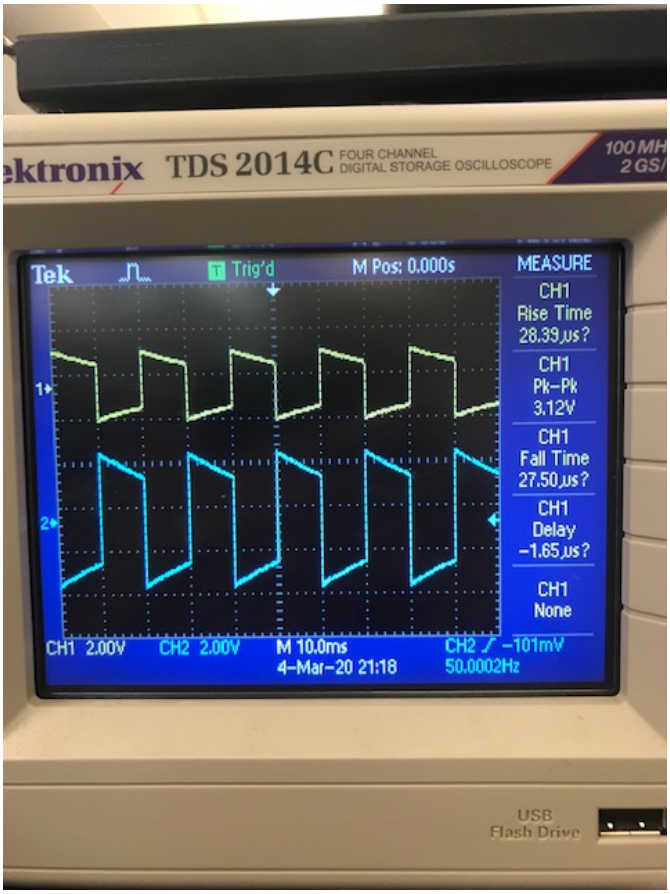
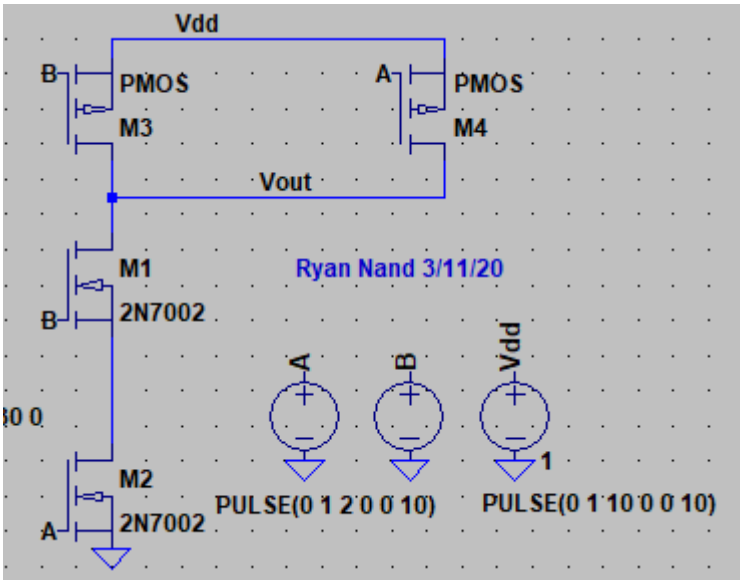


As you can see from the simulation and the implementation, the rise time and fall time are worse than compared with the previous circuits. However, the design and implementation is much more convenient in design. There is also, no overshoot, thanks to the capacitor. This capacitor effects the rise and call time of the output. It seemed like the capacitor increased the rise time but decreased the fall time.

Circuit 5: CMOS NAND GATE



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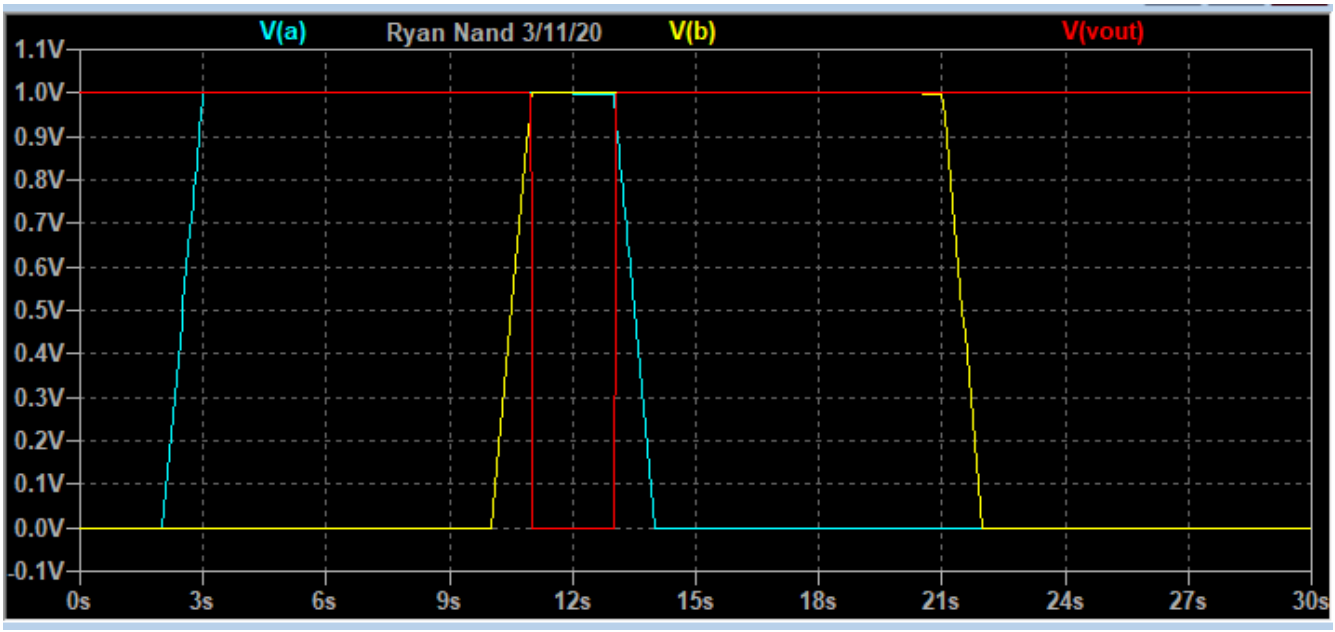
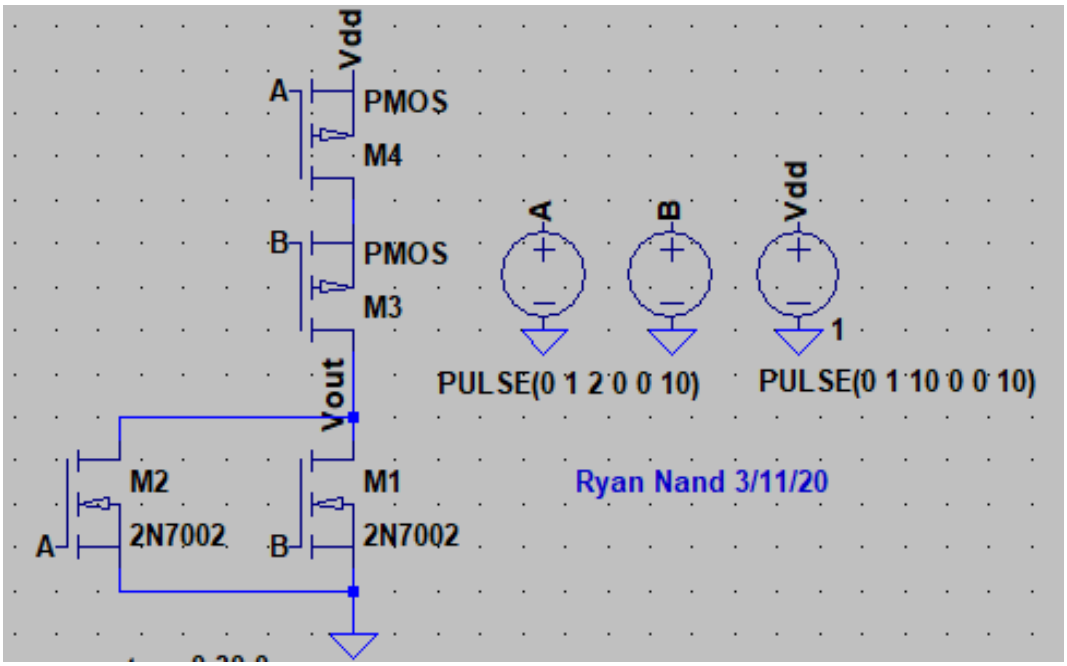


The implemented circuit worked just as well. There were no issues. The logic table turned out to be true for the NAND gate.

Circuit 6: NOR GATE



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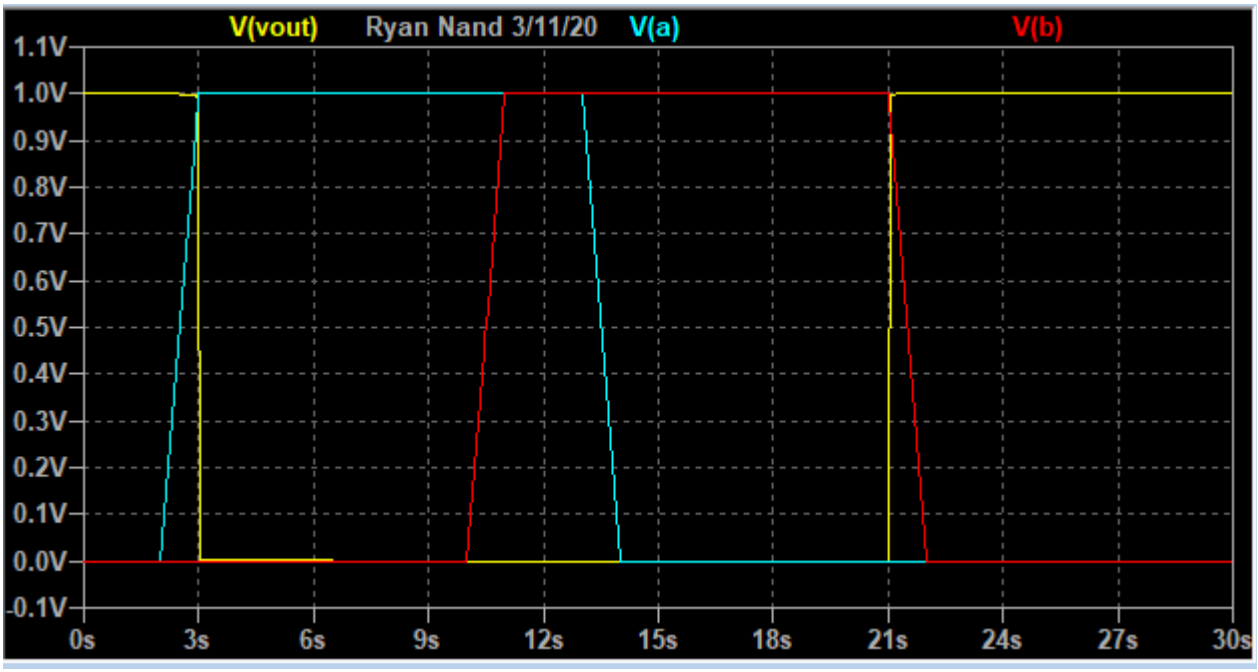

This simulation follow the logic for the NOR gate. The implementation went accordingly as well.

Discussion

For the most part, the logic behind the theory followed through in the results. There were some differences in the fall time, rise time, and delays for each circuit. This is due to differences in spice models and the actual components used. That being said, all results were expected, for example, inverters inverted and the logic gates followed their respective logic tables.

I excluded the results for the implementation from the logic gates because we used only the digital multi-meter. Therefore, only either high or low was the results for each combination of inputs. That being said, for each combination of inputs the expected results did show for both logic circuits. It is obvious that the signal generator was not used for the inputs.

So if we were to conduct this experiment again, I would use the signal generator for the inputs of the logic circuits so that the oscilloscope can show the proper outputs. Also, I would try to spend more time in the simulation stage to set up proper spice models for the transistors used. All in all, the experiment went smoothly and as expected.