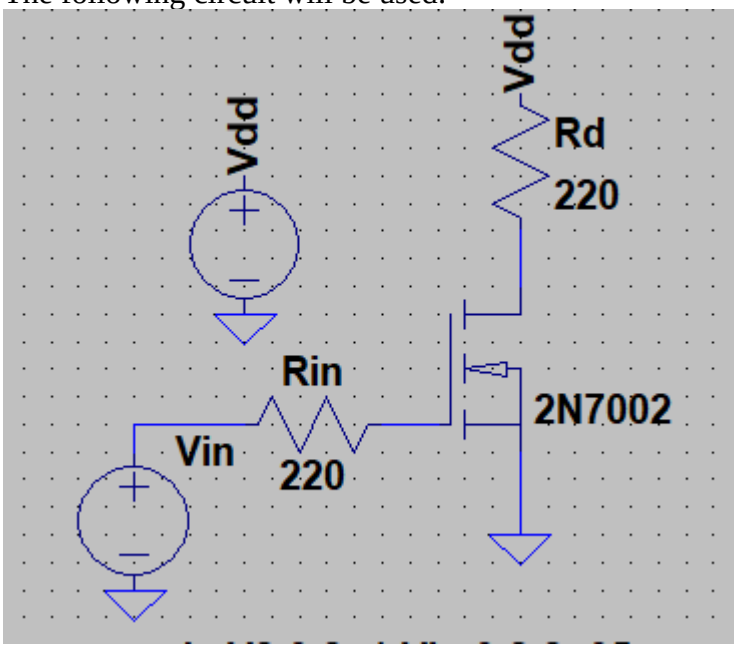
Ryan Nand Lab 3 MOSFETs

Part 1 I_D vs. V_{DS} plot of a MOSFET

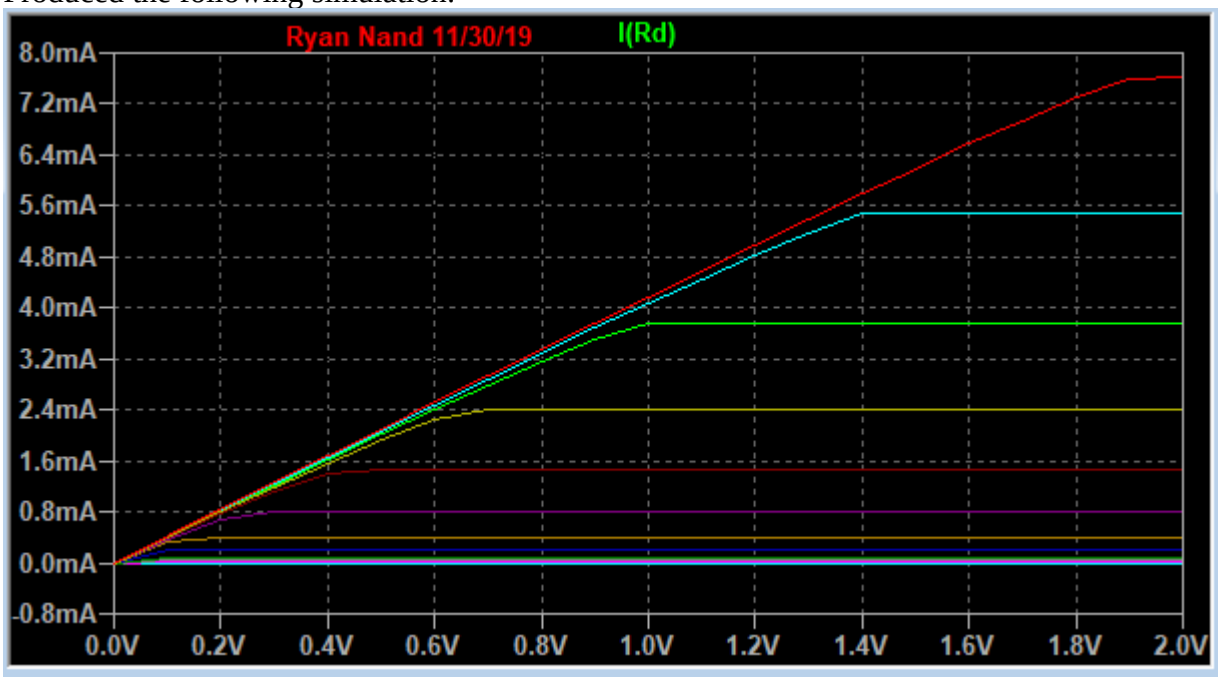
The following circuit will be used:



Real values were used for the resistors so that practical application and testing could be applied.

2N7000 is the MOSFET that will be used. An N-channel with a threshold voltage of .8V minimum and 3V maximum.

Produced the following simulation:



Vgs = 0 to 1.9

Part 2 Biased MOSFETs

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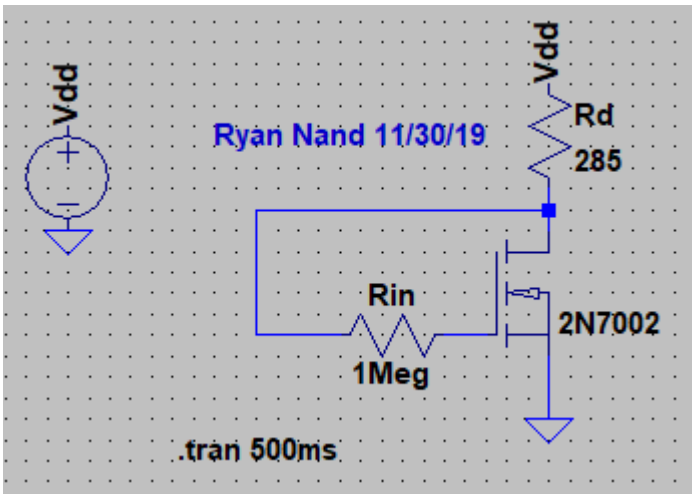
Two resistor bias:



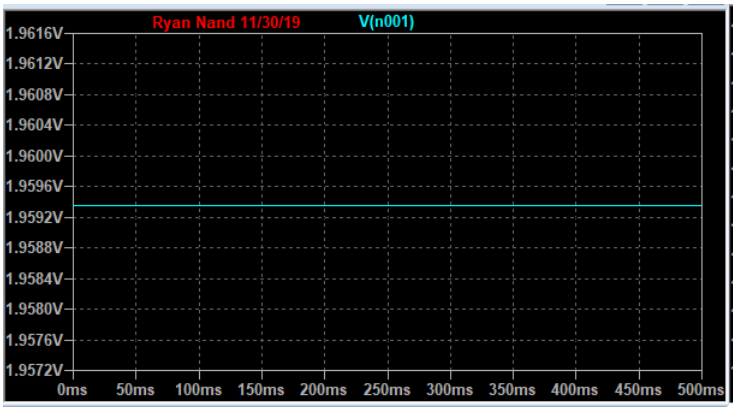
Vdd = 5V

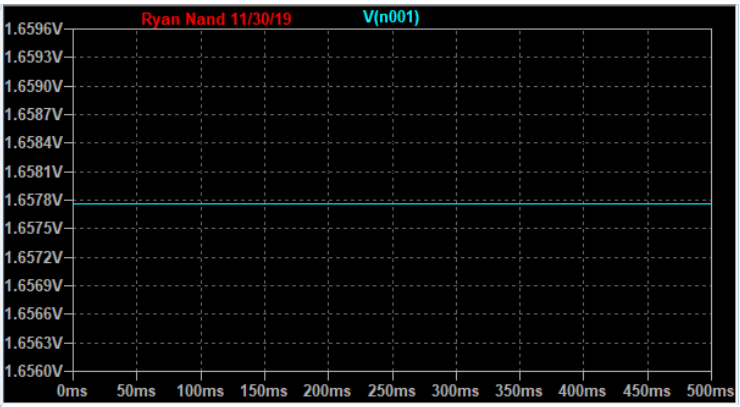
$I_D = .0657(V_{DS} - V_T)^2$

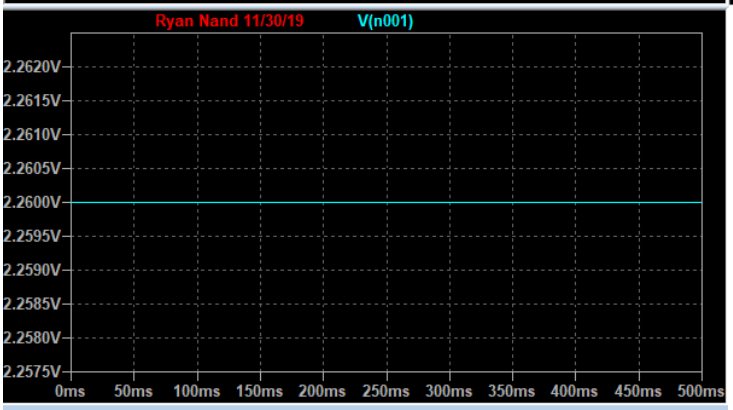
$V_{DS} = V_{GS}$

$V_{DS} = V_{DD} - I_D R_D$

Here the $V_{GS} = 2V$







Above from left to right: normal V_T and V_T-20% respectively.
Left is V_T is +20%.
The change in value is as expected.

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Four resistor bias: