
Introduction and Physical Properties

1) Cell Description

A NFET Enhancement inverter is used in the same way as other kinds of inverters (i.e. the output is the inversion of the input) but is constructed differently than say a CMOS inverter. The inverter's schematic, shown in Fig. 2, has a pull-up and a pull-down nMOS transistor. While nMOS transistors are good at pulling signals they are not good at delivering strong high signals nor as fast as pMOS transistors which will be shown in transient analysis below.

2) Cell Symbol

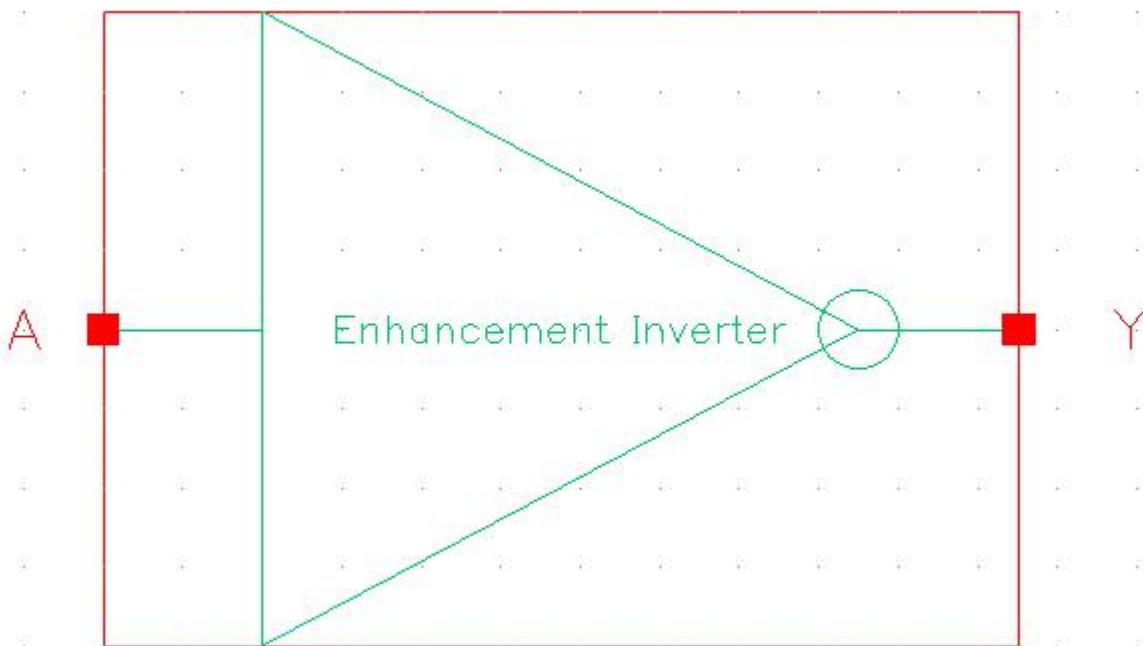


Figure 1: NFET enhancement inverter symbol from Cadence Virtuoso. Used for both NFET enhancement and NFET enhancement long inverters.

Cell Truth Table

Cell Truth Table	
Cell Inputs {0,1}	Cell Outputs {L,H}
0	H
1	L

3) Cell Schematic Diagram

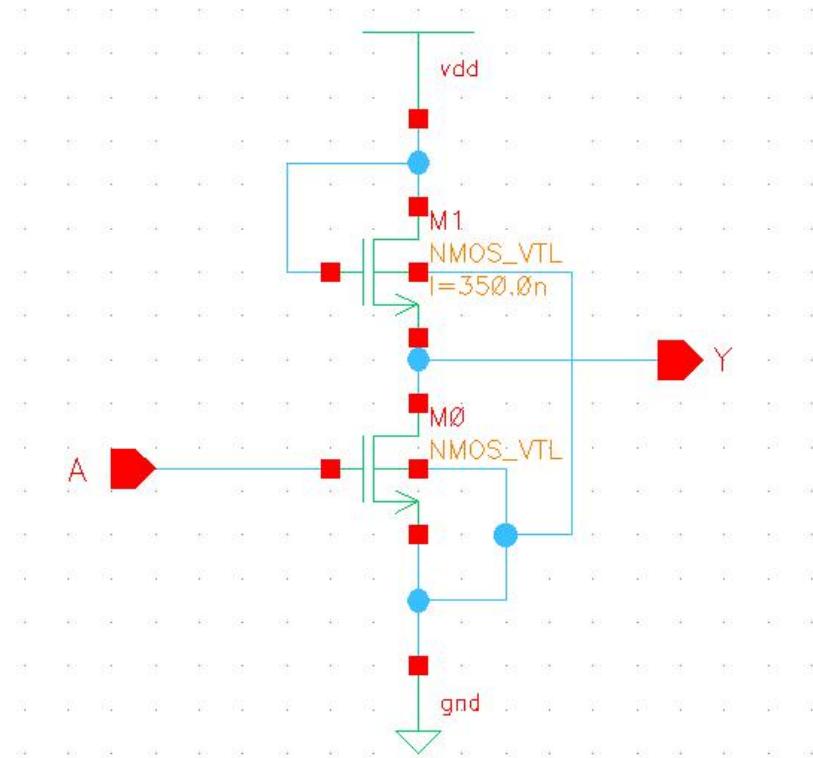


Figure 2: Schematic of the NFET enhancement inverter with minimum dimension pull-down nMOS transistor and 350nm long pull-upnMOS transistor.

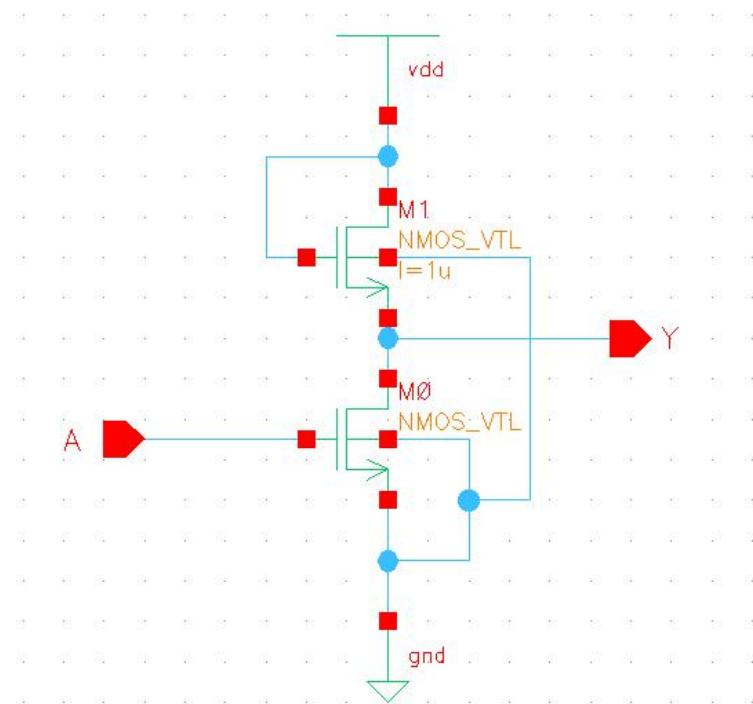


Figure 3: Schematic of the NFET enhancement long inverter with minimum dimension pull-down nMOS transistor and 1um long pull-upnMOS transistor

4,5) Cell Layout Diagram and Dimensions

Transistor Dimensions of NFET Enhancement		
Transistor Instance Number	Length (nm)	Width (nm)
M0	350	90
M1	50	90

Transistor Dimensions of NFET Enhancement Long		
Transistor Instance Number	Length (nm)	Width (nm)
M0	1000	90
M1	50	90

Performance Analysis

6,7) Rise and Fall Times

Input X: Output Rise Time Data t_r (ns)						
Input rise/fall time (ns)	Inverter Configuration	Output Load (FOx)				
		0	1	2	4	8
0.04	NFET Enhancement				1.231	
0.04	NFET Enhancement Long				2.028	

S, Input X: Output Fall Time Data t_f (ns)						
Input rise/fall time (ns)	Inverter Configuration	Output Load (FOx)				
		0	1	2	4	8
0.04	NFET Enhancement				0.076	
0.04	NFET Enhancement Long				0.082	

8,9) Propagation Delays

Data Worst Case Low to High Propagation Delay Data t_{phl} (ns)						
Input rise/fall time (ns)	Inverter Configuration	Output Load (FOx)				
		0	1	2	4	8
0.04	NFET Enhancement				N/D	
0.04	NFET Enhancement Long				N/D	

Data Worst Case High to Low Propagation Delay Data t_{phi} (ns)						
Input rise/fall time (ns)	Inverter Configuration	Output Load (FOx)				
		0	1	2	4	8
0.04	NFET Enhancement				N/D	
0.04	NFET Enhancement Long				N/D	

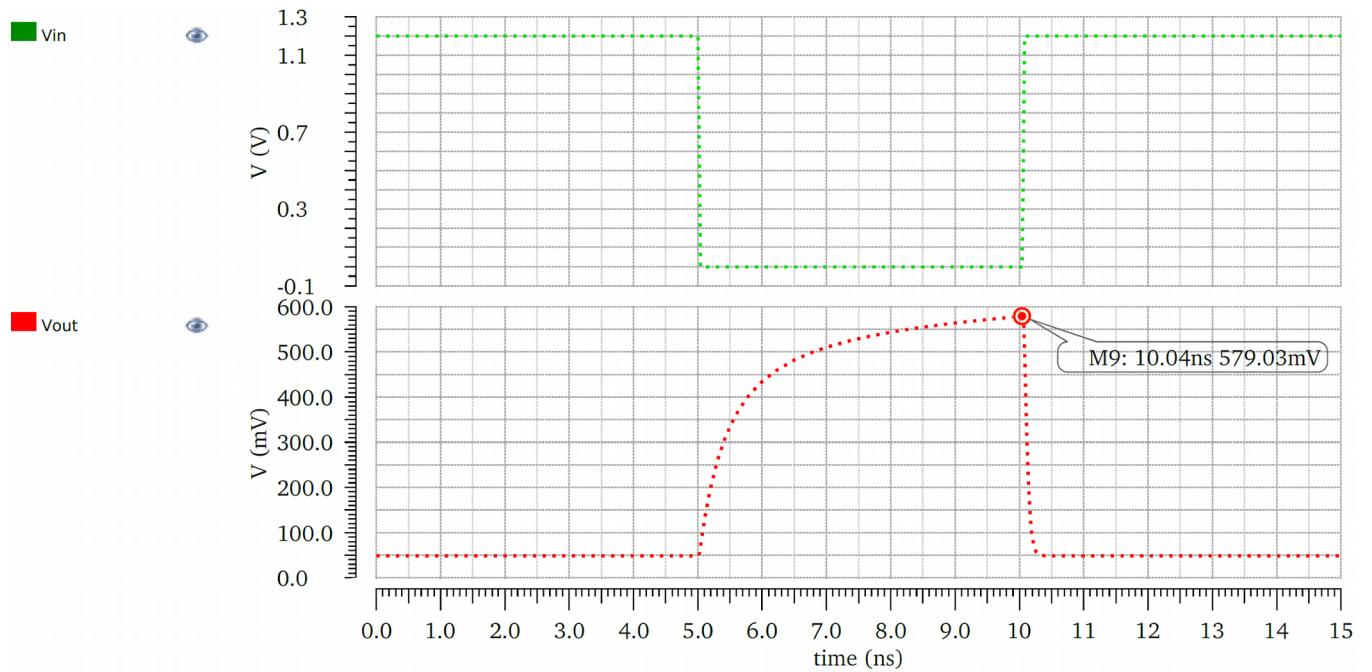


Figure 4: Transient analysis of the NFET enhancement inverter showing the propagation delays. The output never reached 80% of the input so the delay is not determinable.

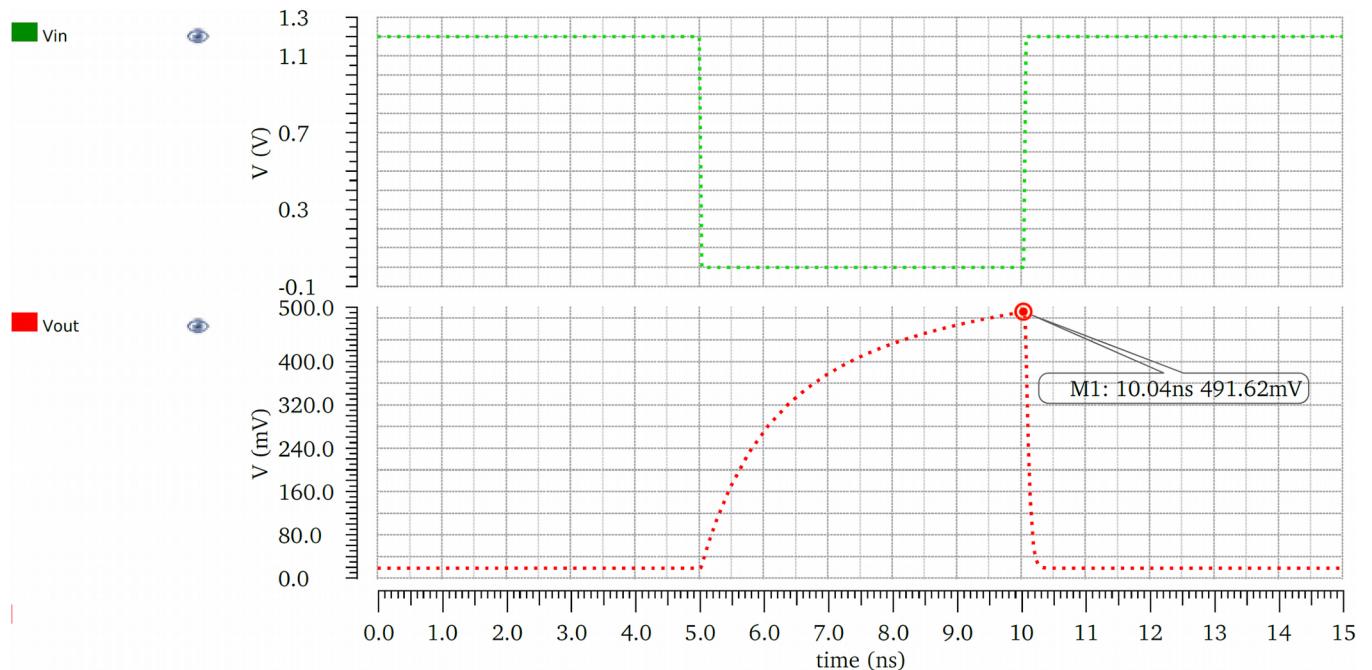


Figure 5: Transient analysis of the NFET enhancement long inverter showing the propagation delays. The output never reached 80% of the input so the delay is not determinable.

**10, 11) Prepare two additional tables (shown below) comparing the performance of the six inverters.
DC analysis**

Type	V_{IH_DC}	V_{IL_DC}	V_{OH_DC}	V_{OL_DC}
CMOS	0.613	0.369	1.129	0.053
CMOS_Wide	0.614	0.370	1.129	0.054
Enhancement mode NFET	0.625	0.345	0.509	0.117
Enhancement mode NFET_Long	0.551	0.271	0.529	0.066
Resistive load (100k)	0.619	0.277	1.129	0.083
Resistive load_long (200k)	0.558	0.240	1.132	0.056

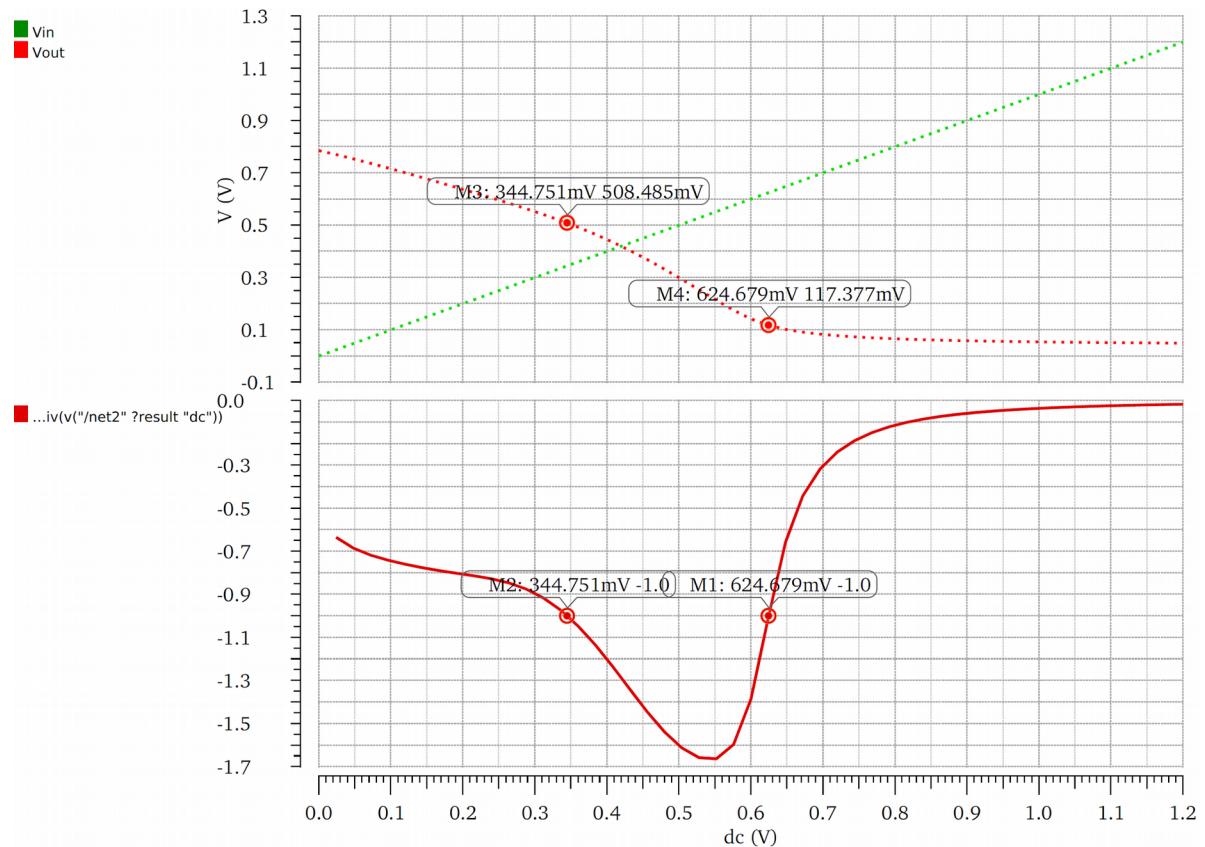


Figure 6: DC analysis of the NFET enhancement inverter.

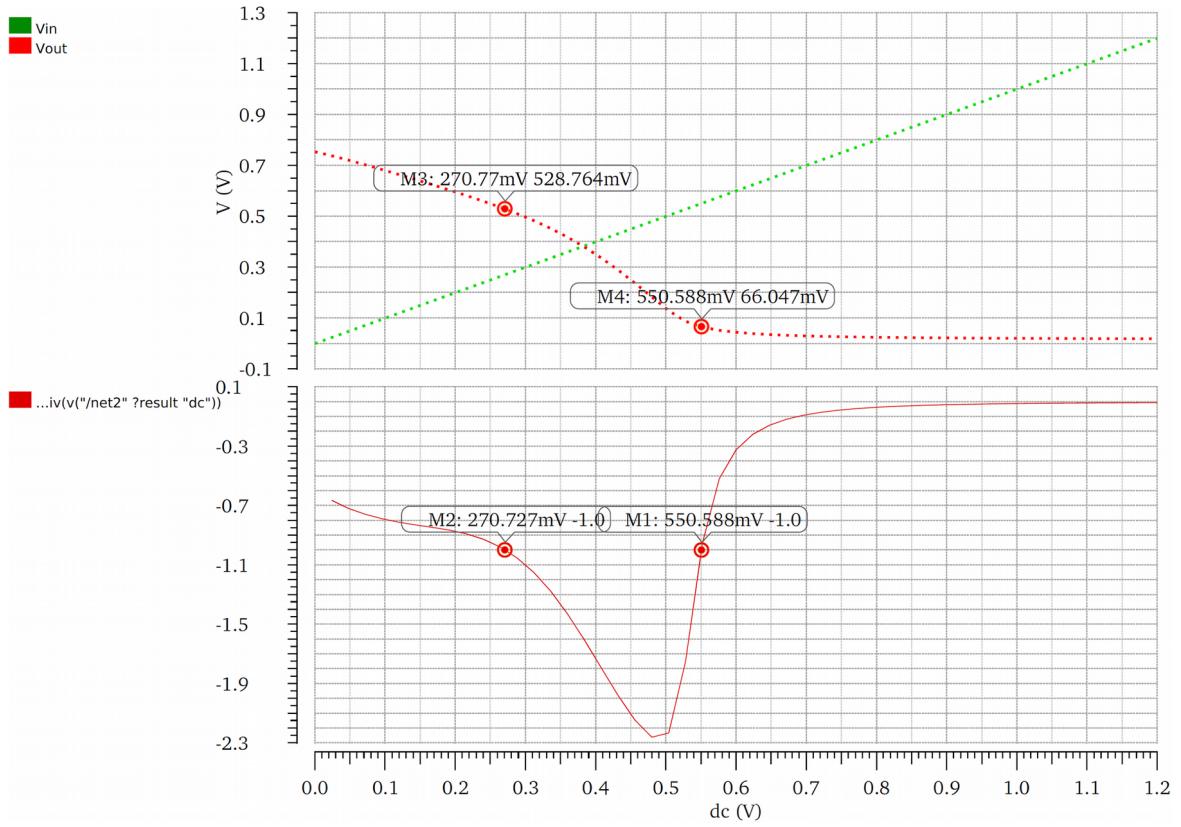


Figure 7: DC analysis of the NFET enhancement long inverter.

Transient analysis

Type	$t_{p_{lh}}$	$t_{p_{hl}}$	t_r	t_f
CMOS	0.273	0.092	0.395	0.116
CMOS_Wide	0.071	0.028	0.095	0.029
Enhancement mode NFET	N/D	N/D	1.231	0.076
Enhancement mode NFET_Long	N/D	N/D	2.028	0.082
Resistive load (100k)	1.014	0.088	2.092	0.116
Resistive load_long (200k)	2.071	0.062	4.189	0.123

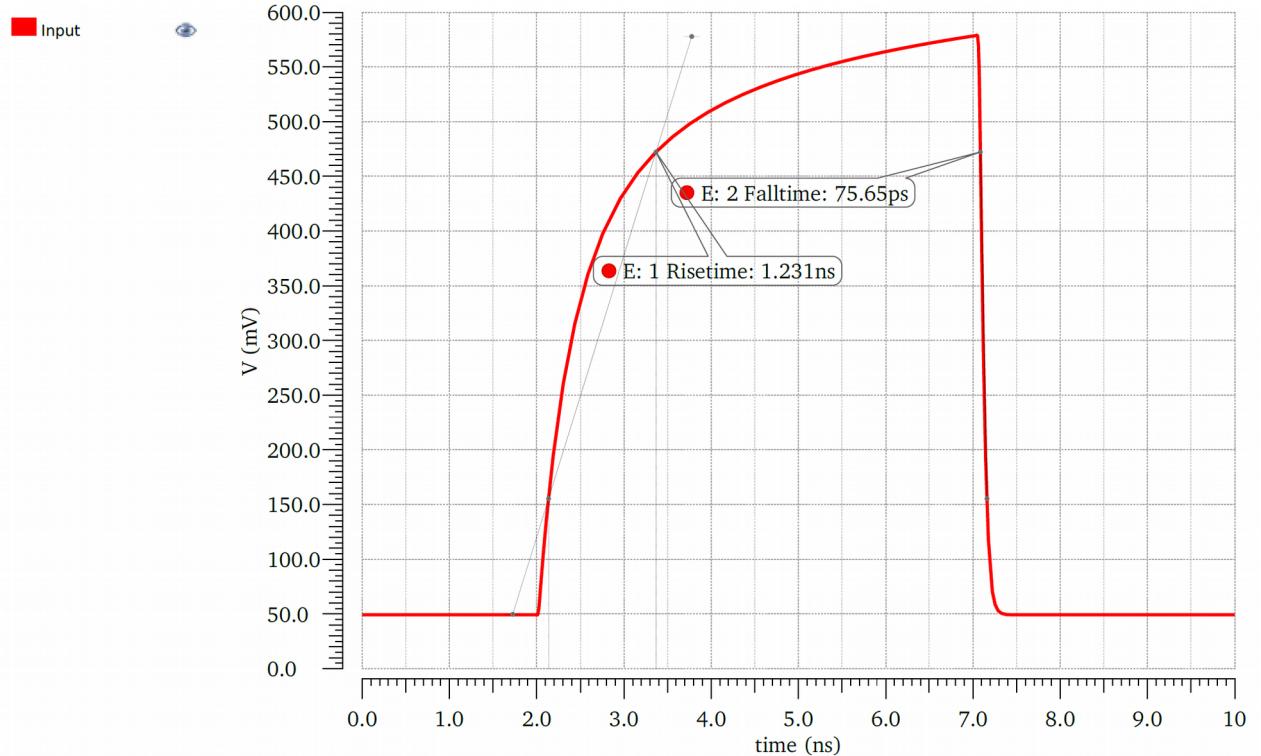


Figure 8: Transient analysis of the NFET enhancement inverter showing the rise and fall time of the output. The output never reached 80% of the input so the rise and fall times are not useful for an accurate comparison to the other inverters.

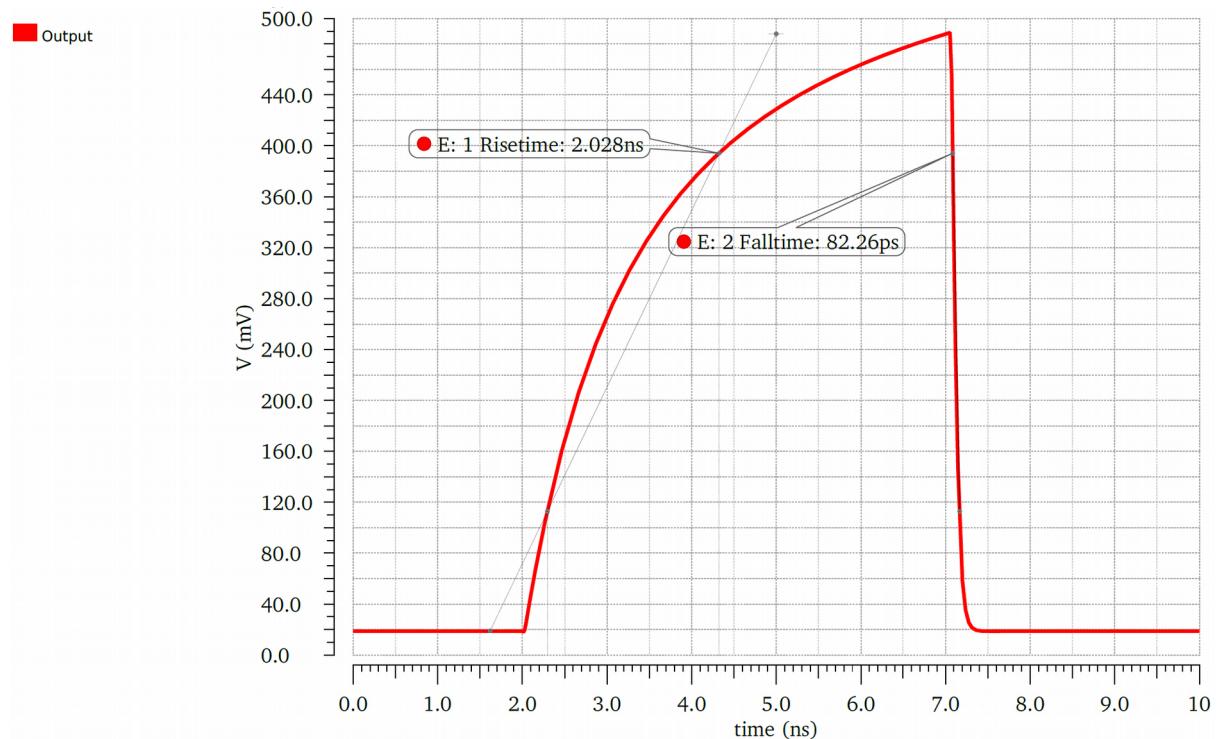


Figure 9: Transient analysis of the NFET enhancement long inverter showing the rise and fall time of the output. The output never reached 80% of the input so the rise and fall times are not useful for an accurate comparison to the other inverters.

A meaningful propagation delay measurement can not be made with this inverter. The output swing is less than half of the input. When we measure the propagation delay, we compare the time that the input transition crosses the 600mV mark, since this is half of the input voltage, with the time the output transition crosses the same voltage level. The output voltage never reaches this level, so a meaningful measurement can't be taken.