
Lab 1

Intro to PECS: DC-DC Power Conversion

PORTLAND STATE UNIVERSITY
MASEEH COLLEGE OF ENGINEERING & COMPUTER SCIENCE
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

Authors:

RYAN NAND

April 13, 2020



Maseeh College of Engineering
and Computer Science

PORTLAND STATE UNIVERSITY

ECE 317
SIGNALS AND SYSTEMS III LABORATORY

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1 Introduction

This lab is to establish the understanding of how to utilize PECS (Power Electronics Circuit Simulator). This will be done using DC-DC power conversion circuits. There will be four circuits where simulation and analysis will be done. This lab will introduce various components within PECS describing how to build the circuit, while configuring those components to the desired values. Finally, an introduction to simulation plots and how to edit those plots to see desired results.

2 Circuit 1

This circuit is a rectangular wave generator with a LC low pass filter. The rectangular waveform is generated by two switches triggered by two separate clocks. Then the filter filters out high frequencies providing a steady state. The schematic:

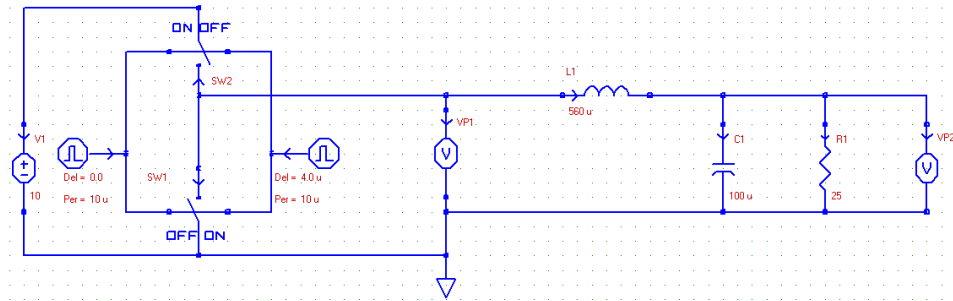


Figure 1: Circuit 1 Schematic

The values of the schematic are:

$V1 = 10 \text{ V}$, $L1 = 560 \mu\text{H}$, $C1 = 100 \mu\text{F}$, $R1 = 25 \Omega$

The periods of the clocks are $10 \mu\text{s}$ and one of the clocks has a $4 \mu\text{s}$ delay.

Here is the steady state output taken across the load resistor R1 (seen at VP2):

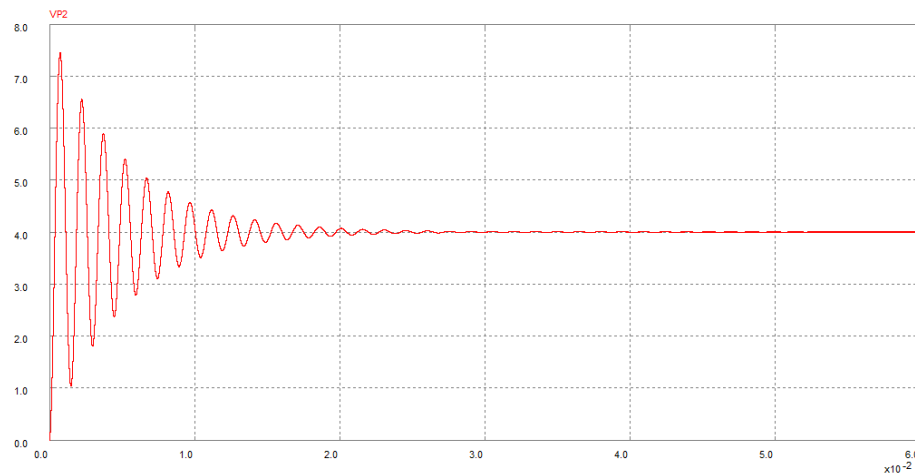


Figure 2: Circuit 1 Steady State Output

As you can see from the plot above the steady state value is 4 V.

This next plot shows a closer look at the steady state output and the rectangular waveform input for comparison.

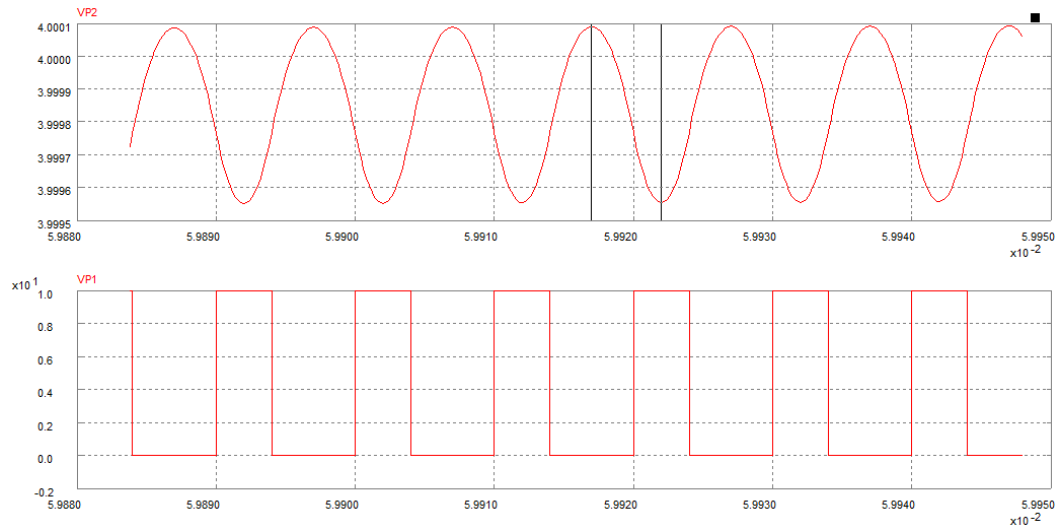


Figure 3: Circuit 1 Magnified Steady State Output

The following figure shows the measured peak-to-peak ripple voltage of VP2. This is from using the PECS measurement tool.

| Measure | | | |
|---------|-------------|--------------|--------------|
| | Left Button | Right Button | Difference |
| Time | 5.99170e-02 | 5.99220e-02 | 5.00000e-06 |
| VP2 | 4.00009e+00 | 3.99955e+00 | -5.36000e-04 |

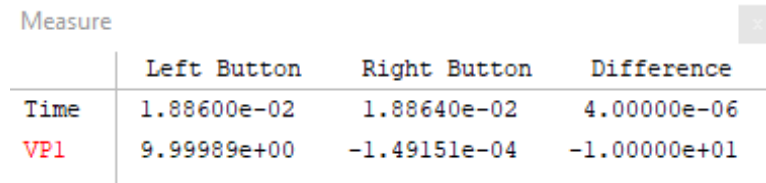
Figure 4: Circuit 1 Peak-to-Peak Ripple Measurement

The value is seen under the difference column. A ripple voltage of $536 \mu\text{V}$.

Also, looking at figure 3, we can see the values for the rectangular waveform generated (VP1).

There is a amplitude of 10 V and a period of $10 \mu\text{s}$.

The pulse width is found from the measurement tool displayed in the next table under time difference. The same measurement tool that found the ripple voltage for VP2.



| | Left Button | Right Button | Difference |
|------|-------------|--------------|--------------|
| Time | 1.88600e-02 | 1.88640e-02 | 4.00000e-06 |
| VP1 | 9.99989e+00 | -1.49151e-04 | -1.00000e+01 |

Figure 5: Circuit 1 Pulse Width Measurement

As you can see the pulse width is 4 μs .

Using the gathered values, one can find the duty ratio using the following equation:

$$DutyRatio = PulseWidth / Period * 100 \quad (1)$$

In this case, the duty ratio is 40 %.

Notice that the pulse width and the delay in one of the clocks are equivalent. The pulse width was actually set by that particular delay. Therefore, changing the delay changes the duty ratio.

This duty ratio explains why there was a steady state value of 4 V. The duty ratio is the time the output is on or high. To put it simply the duty ratio has the following effect on the input voltage:

$$OutputVoltage = InputVoltage * DutyRatio \quad (2)$$

In words, the duty ratio takes the average of the input voltage and that is what is seen at the output. In this case, 40 % of 10 (the input voltage for the filter implemented by source V1) is 4. Therefore a steady state value of 4 V.

3 Circuit 2

This circuit uses a modulator to form a saw-tooth waveform. The capacitor charges until the modulator turns off. That is where the capacitor starts to discharge, thus forming a saw-tooth waveform. The discharge has to be faster than both the charging rate and the period of the modulator for this to happen.

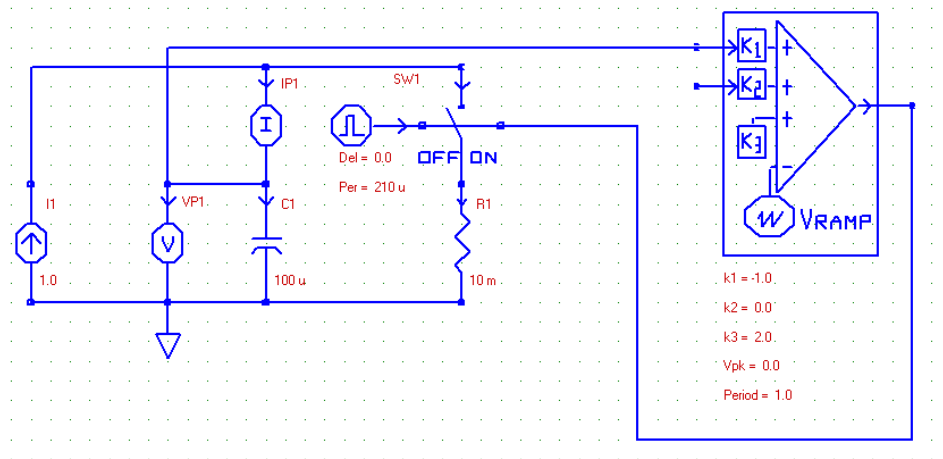


Figure 6: Circuit 2 Schematic

Schematic values:

$V1 = 1 \text{ V}$, $C1 = 100 \mu\text{F}$, $R1 = 10 \text{ m}\Omega$, $K1 = -1$, $K3 = 2$, and clock period is $210 \mu\text{s}$.

The following plot shows the current and voltage at the capacitor.

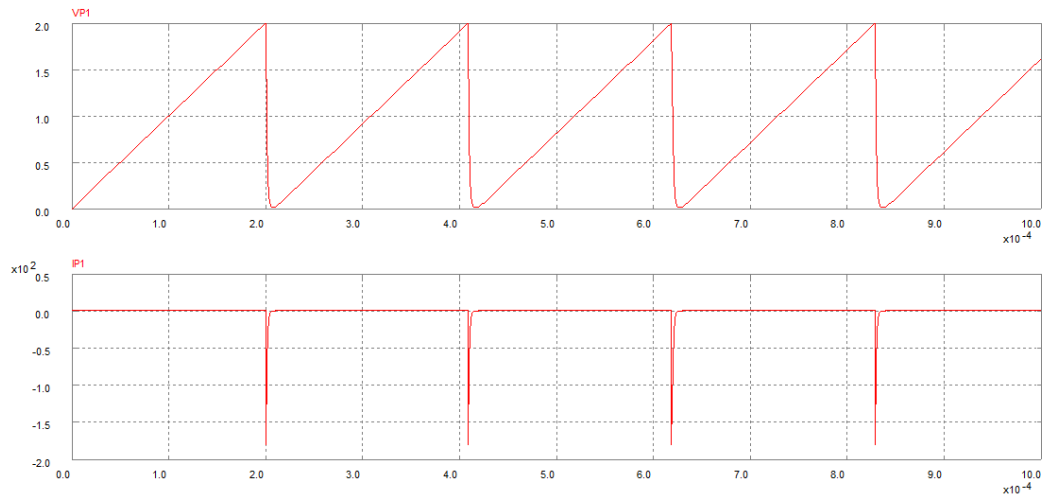


Figure 7: Circuit 2 Output

From the plot above, we can see the amplitude is 2 V with a period of 210 μ s.

The factor that determines the amplitude (other than K1) is: K3

This was found by testing different variables of the circuit, and the logic behind this is similar to a counter. Once the target voltage (the value of K3) is matched by the increasing value (in this case K1 which is equivalent to the voltage charging at C1) the modulator turns off. So the capacitor discharges to turn the modulator back on. The cycle repeats continuously.

However, there are several factors that determine the period. Such as the period of the clock, the value of the capacitor, etc.

4 Circuit 3

This circuit is just like circuit 1, however, one of the clocks was replaced by a modulator attached to a voltage source. The schematic is below.

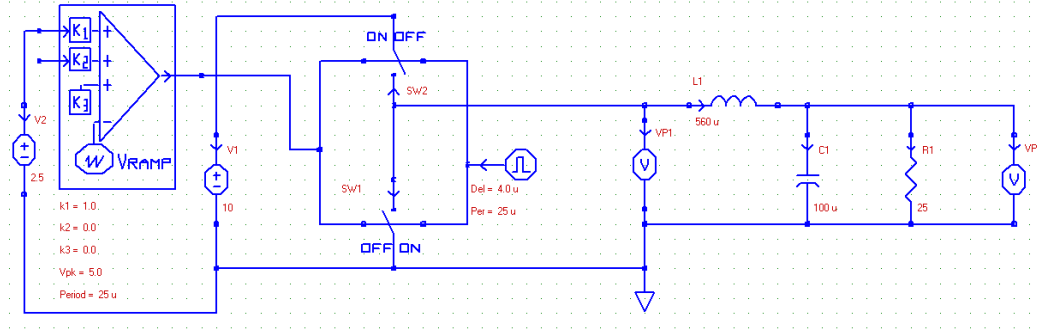


Figure 8: Circuit 3 Schematic

The new values of the system includes a period of 25 μs and a V_{pk} of 5 V for the modulator.

We were asked to find a voltage for V2 that would produce a 50 % duty ratio.

After some further testing of the modulator's response and the circuit's response to the modulator's response, I have determined the equation needed to solve for the voltage required at V2. The equation is as follows:

$$Voltage = (100 - DutyRatio)/100 * V_{pk} \quad (3)$$

Using the equation above and the values of the required duty ratio along with the given V_{pk} , one can solve for the voltage required for the desired output. In this case, the voltage comes out to be 2.5 V, so $V2 = 2.5 \text{ V}$.

The next plot shows the steady state output across the load resistor R1 (VP2).

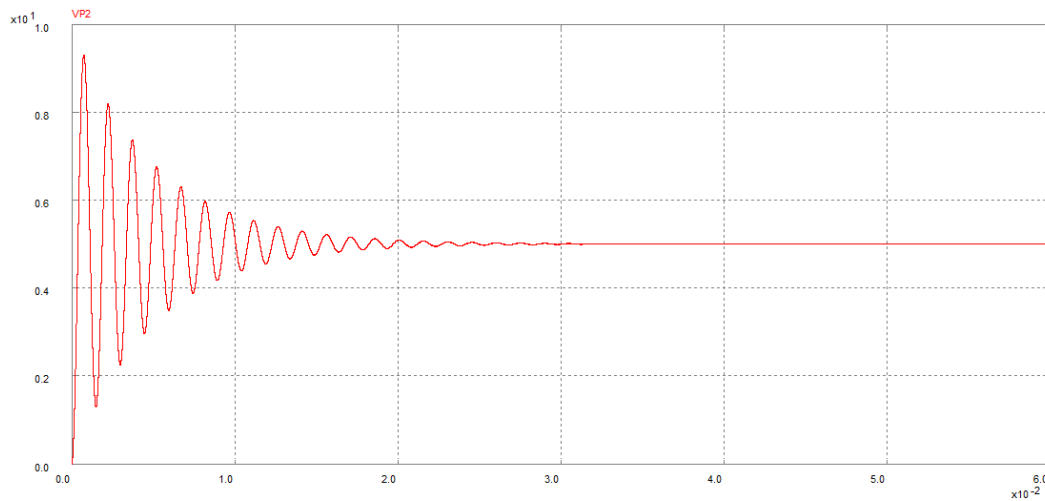


Figure 9: Circuit 3 Steady State Output

Looking at the plot we can see a convergence to the steady state value. The steady state value can be determined using equation (2), which is 5 V.

This next plot shows the zoomed in steady state output and the rectangular wave-form input for comparison.

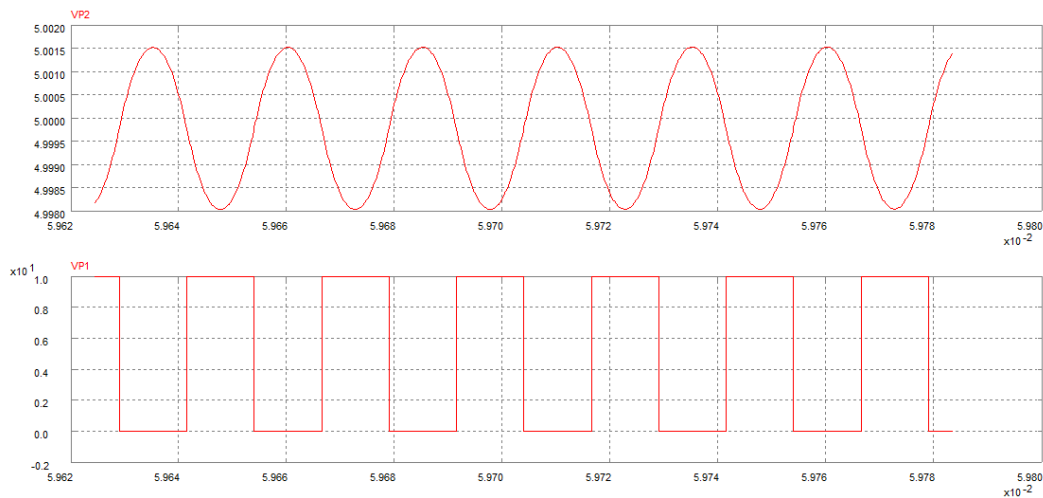


Figure 10: Circuit 3 Magnified Steady State Output

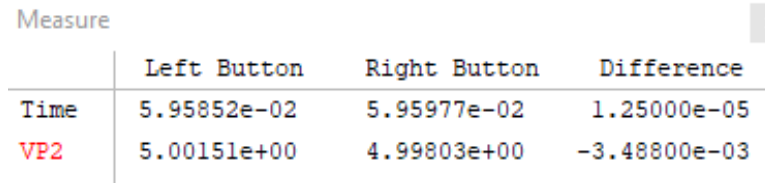
The figure below shows the pulse width of the rectangular waveform generated at VP1.

| Measure | | | |
|---------|-------------|--------------|--------------|
| | Left Button | Right Button | Difference |
| Time | 5.97165e-02 | 5.97290e-02 | 1.25000e-05 |
| VP1 | 9.99986e+00 | -2.55807e-04 | -1.00001e+01 |

Figure 11: Circuit 3 Pulse Width Measurement

To check if the pulse width is correct and that the waveform generated is indeed a 50 % duty ratio, we can go back to equation (1). The pulse width given by the measuring tool is under the time difference (1.25e-05 seconds). Using equation (1), the period (25 μ s), and the duty ratio (50 %), we get a pulse width of 12.5 μ s. Both values match. Therefore, we have a 50 % duty ratio.

This last figure below is of the ripple voltage in this particular circuit.



| | Left Button | Right Button | Difference |
|------|-------------|--------------|--------------|
| Time | 5.95852e-02 | 5.95977e-02 | 1.25000e-05 |
| VP2 | 5.00151e+00 | 4.99803e+00 | -3.48800e-03 |

Figure 12: Circuit 3 Peak-to-Peak Ripple Measurement

A ripple voltage of 3.488 mV.

To recap here are the specifications of VP1:

Amplitude = 10 V

Period = 25 μ s

Pulse width = 12.5 μ s

Duty ratio of 50 %.

A table to compare the rectangular waveform from both circuit 1 and circuit 3 is below.

| | Switching Frequency | Duty Ratio | Peak-to-Peak Input Voltage to Filter | Steady State Output Voltage | Peak-to-Peak Output Voltage Ripple |
|-----------|---------------------|------------|--------------------------------------|-----------------------------|------------------------------------|
| Circuit 1 | 100 kHz | 40 % | 10 V | 4 V | 536 μ V |
| Circuit 2 | 40 kHz | 50 % | 10 V | 5 V | 3.488 mV |

Table 1: Rectangular Waveform Generator Comparison

The switching frequency is determined simply by the frequency of the clocks.

$$F = 1/T \quad (4)$$

Where T is the period of the clock.

5 Conclusion

So there is a difference of about 2.952 mV between the ripple voltages from the two circuits. This is to be expected after looking at the switching frequencies of the two circuits.

The logic behind that claim is the following. For example, in a set amount of time (in this case it was 6 μ s) there are one hundred thousand data points converging to some value with random outliers, let's call this trial one. Trial two will be the same but with forty thousand data points instead. The random outliers will cause some small tolerance in the system. Taking the average of both trials will result with trial one being much closer to the convergence point. It is simple statistics.

Therefore, a higher switching frequency will result with a smaller ripple voltage, which is a good thing.