
Introduction and Physical Properties

1) Cell Description

An inverter is designed to take an input low voltage and produce an output high voltage, and vice versa. A CMOS inverter is used in the same way as other kinds of inverters but has the ability to produce strong high and low signals due to the use of both PMOS and NMOS transistors. The inverter's schematic, shown in Fig. 2, has a pull-up pMOS transistor and pull-down nMOS transistor which allows the inverter to quickly transition between high and low output states and thus helps reduce delay in large integrated circuits.

2) Cell Symbol

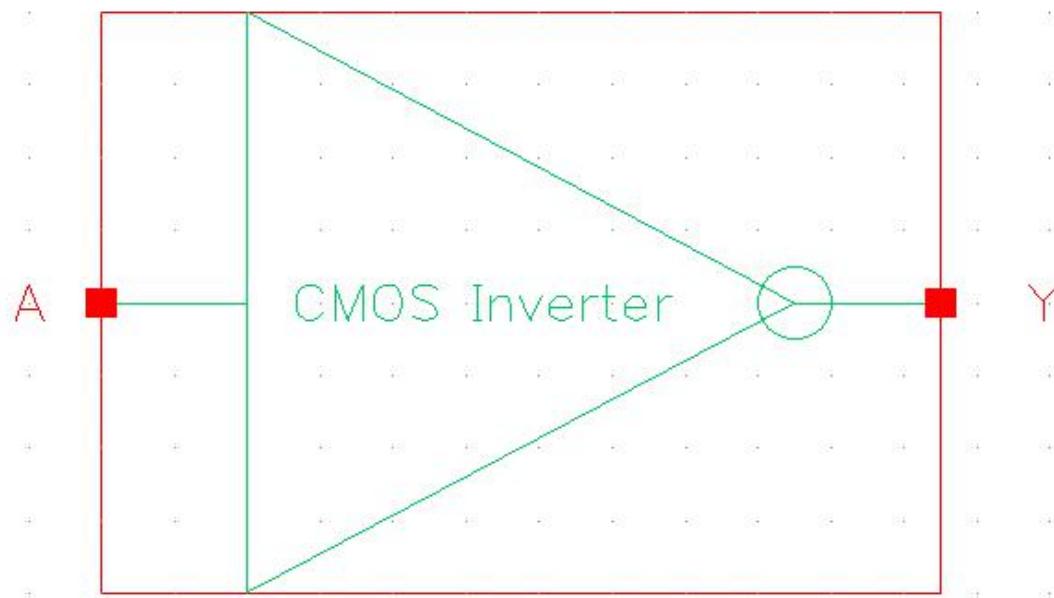


Figure 1: CMOS inverter symbol from Cadence Virtuoso. Used for both CMOS and CMOS wide inverters.

Cell Truth Table

Cell Truth Table	
Cell Inputs {0,1}	Cell Outputs {L,H}
0	H
1	L

3) Cell Schematic Diagram

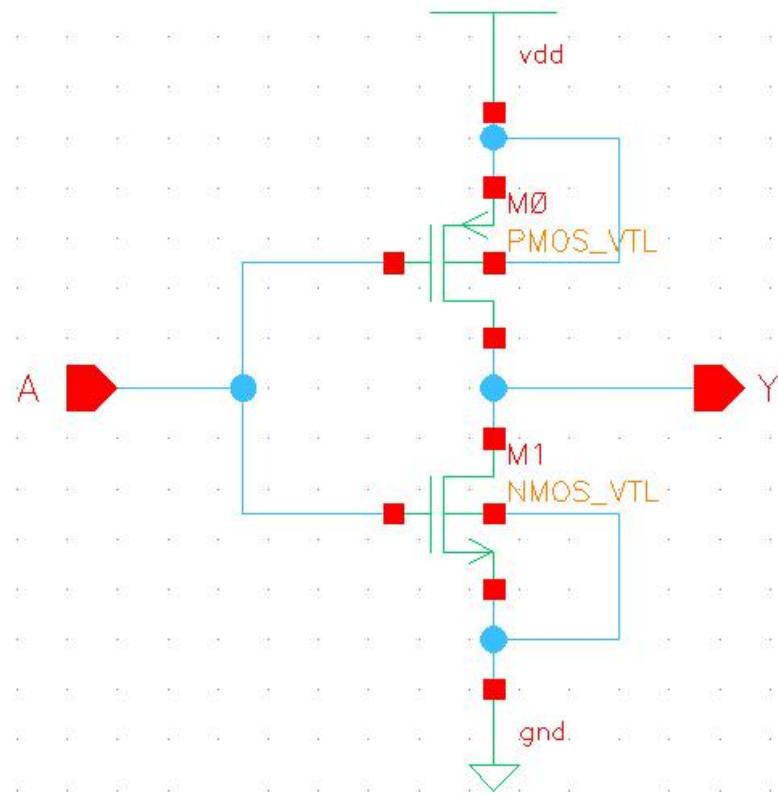


Figure 2: Schematic of the CMOS inverter with minimum transistor dimensions.

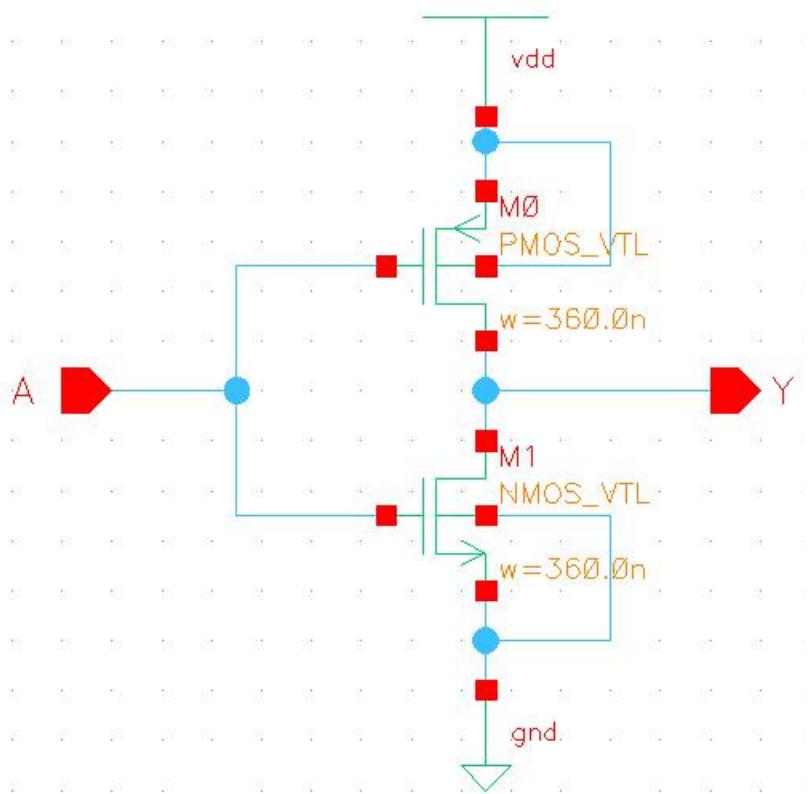


Figure 3: Schematic of the CMOS wide inverter with increased width of both transistors.

4,5) Cell Layout Diagram and Dimensions

Transistor Dimensions of CMOS		
Transistor Instance Number	Length (nm)	Width (nm)
M0	50	90
M1	50	90

Transistor Dimensions of CMOS Wide		
Transistor Instance Number	Length (nm)	Width (nm)
M0	50	360
M1	50	360

Performance Analysis

6,7) Rise and Fall Times

Input X: Output Rise Time Data t_r (ns)					
Input rise/fall time (ns)	Inverter Configuration	Output Load (FO _{Ox})			
		0	1	2	4
0.04	CMOS				0.395
0.04	CMOS Wide				0.095

S, Input X: Output Fall Time Data t_f (ns)					
Input rise/fall time (ns)	Inverter Configuration	Output Load (FO _{Ox})			
		0	1	2	4
0.04	CMOS				0.116
0.04	CMOS Wide				0.029

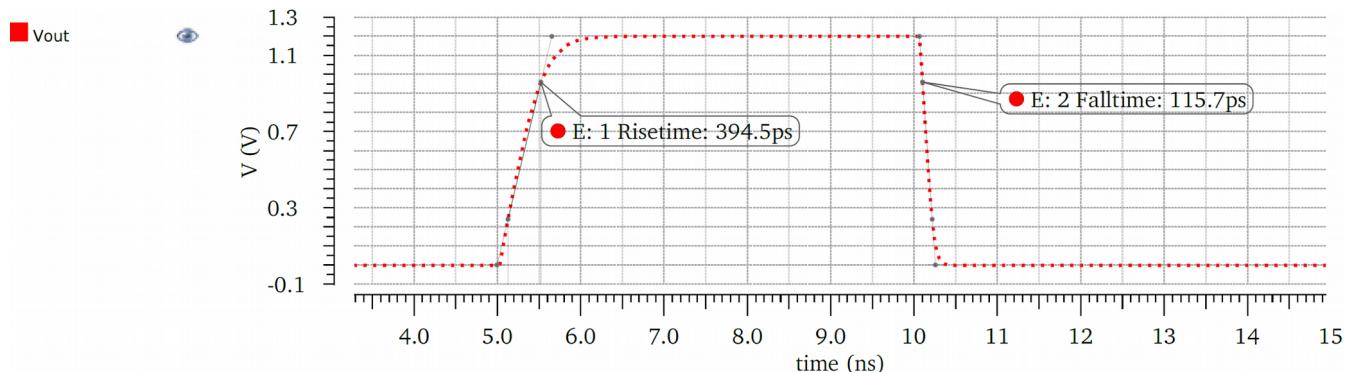


Figure 4: Transient analysis of the CMOS inverter showing the rise and fall time of the output.

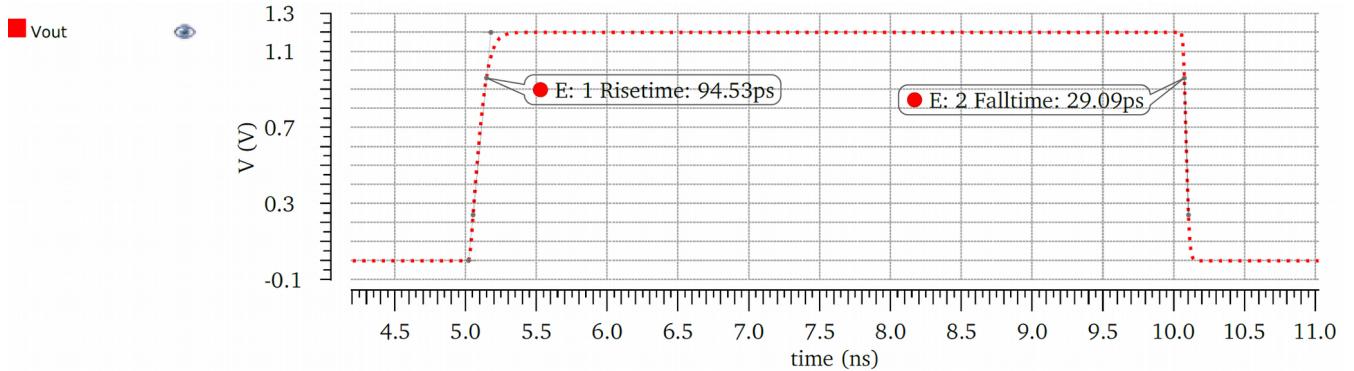


Figure 5: Transient analysis of the CMOS wide inverter showing the rise and fall time of the output.

8,9) Propagation Delays

Data Worst Case Low to High Propagation Delay Data t_{phl} (ns)					
Input rise/fall time (ns)	Inverter Configuration	Output Load (FO _x)			
		0	1	2	4
0.04	CMOS				0.273
0.04	CMOS Wide				0.071

Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
Input rise/fall time (ns)	Inverter Configuration	Output Load (FO _x)			
		0	1	2	4
0.04	CMOS				0.092
0.04	CMOS Wide				0.028

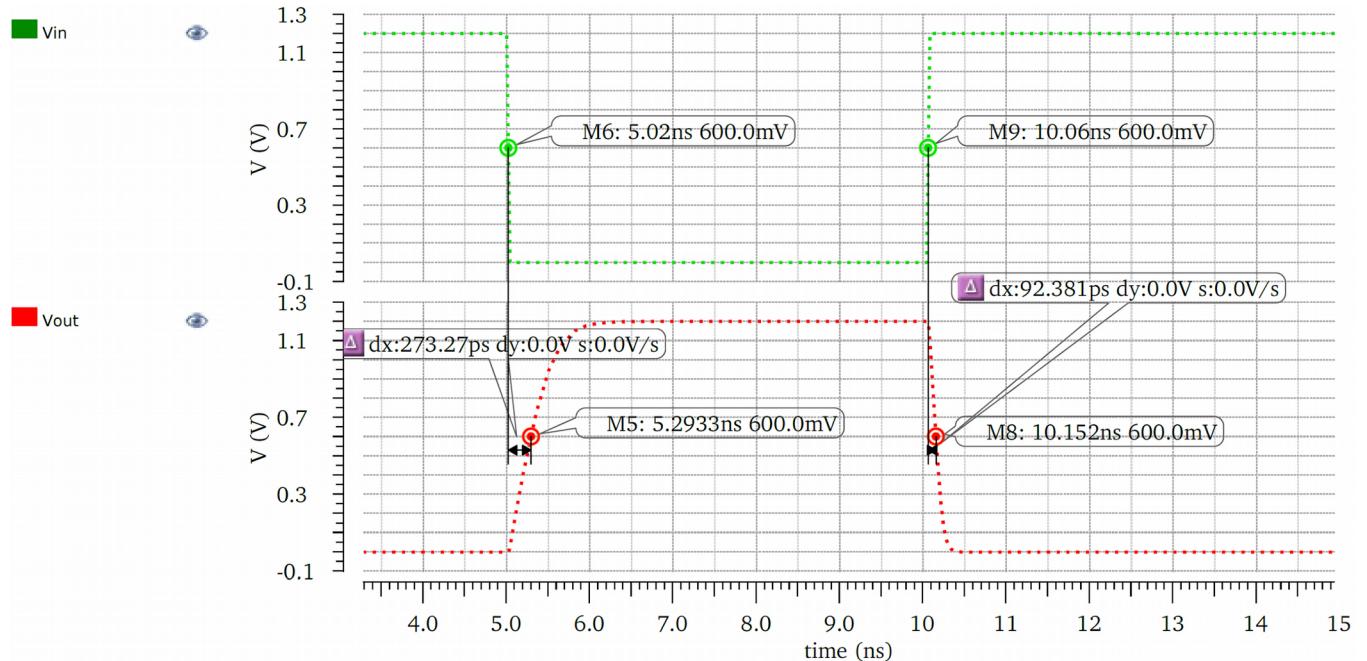


Figure 6: Transient analysis of the CMOS inverter showing the propagation delays.

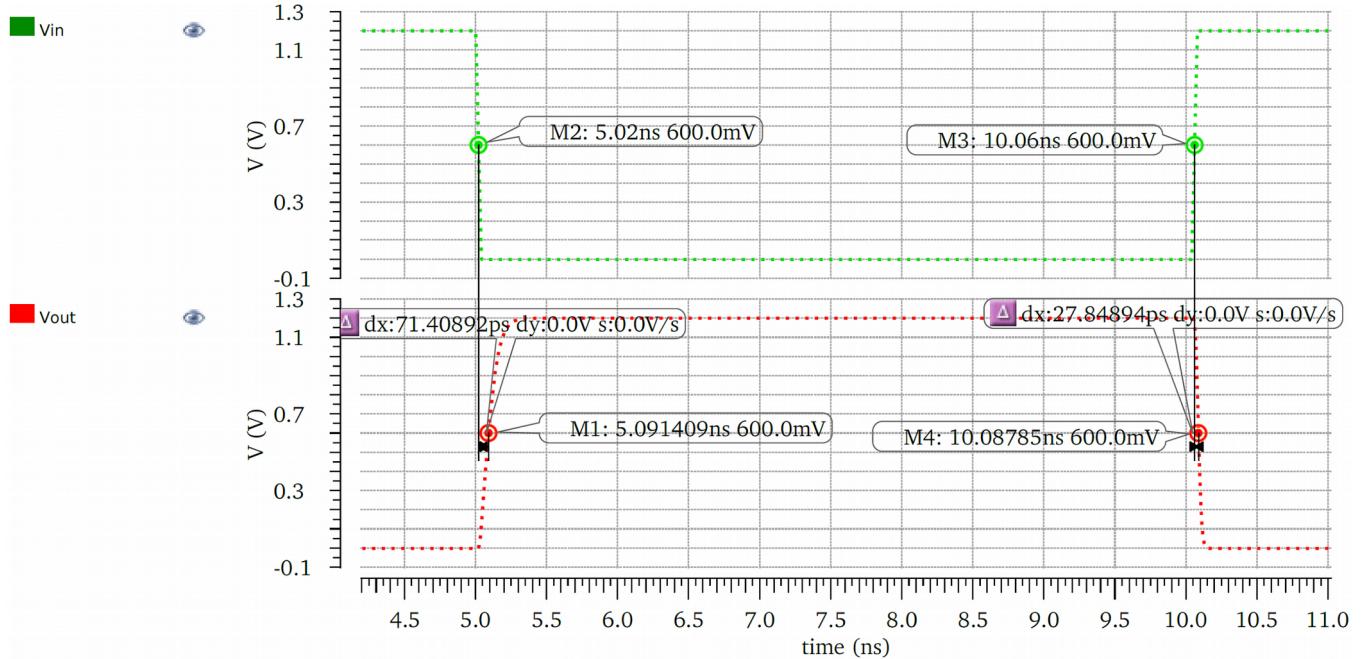


Figure 7: Transient analysis of the CMOS wide inverter showing the propagation delays.

10, 11) DC and Transient Analysis

DC analysis

Type	V_{IH_DC}	V_{IL_DC}	V_{OH_DC}	V_{OL_DC}
CMOS	0.613	0.369	1.129	0.053
CMOS_Wide	0.614	0.370	1.129	0.054
Enhancement mode NFET	0.625	0.345	0.509	0.117
Enhancement mode NFET_Long	0.551	0.271	0.529	0.066
Resistive load (100k)	0.619	0.277	1.129	0.083
Resistive load_long (200k)	0.558	0.240	1.132	0.056

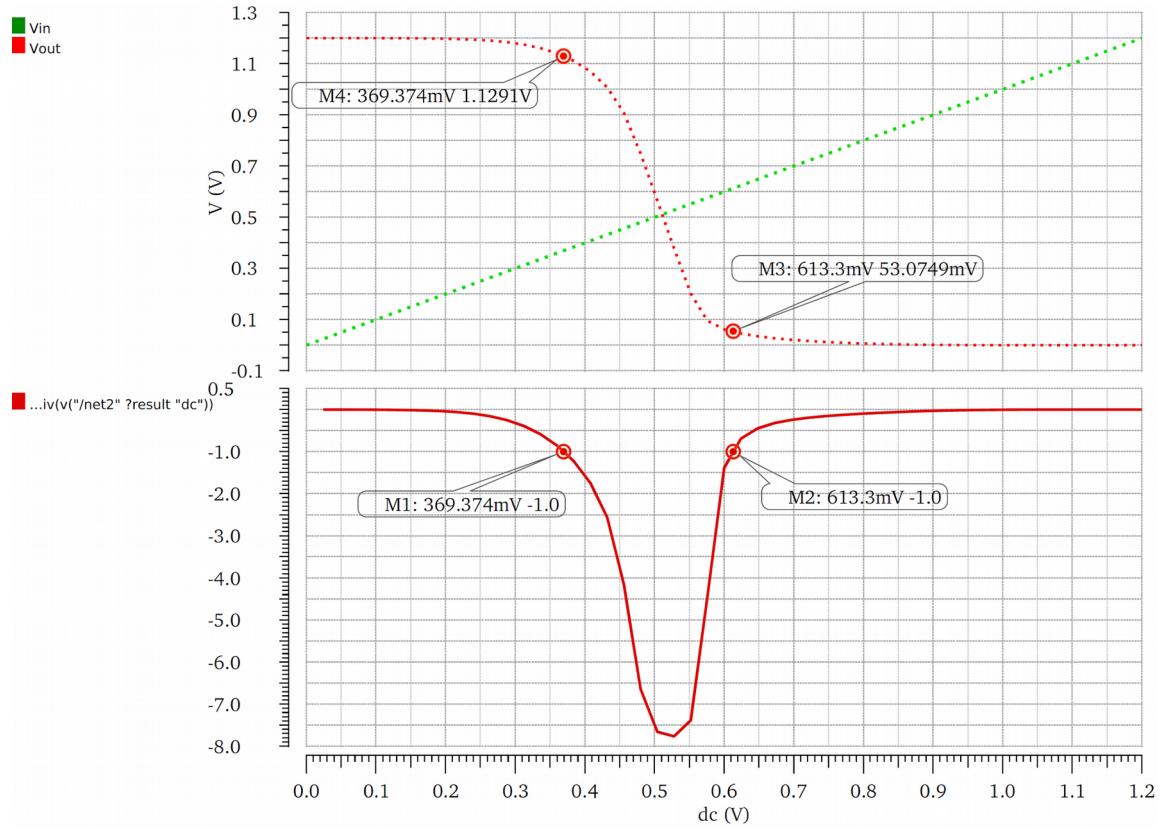


Figure 8: DC analysis of the CMOS inverter.

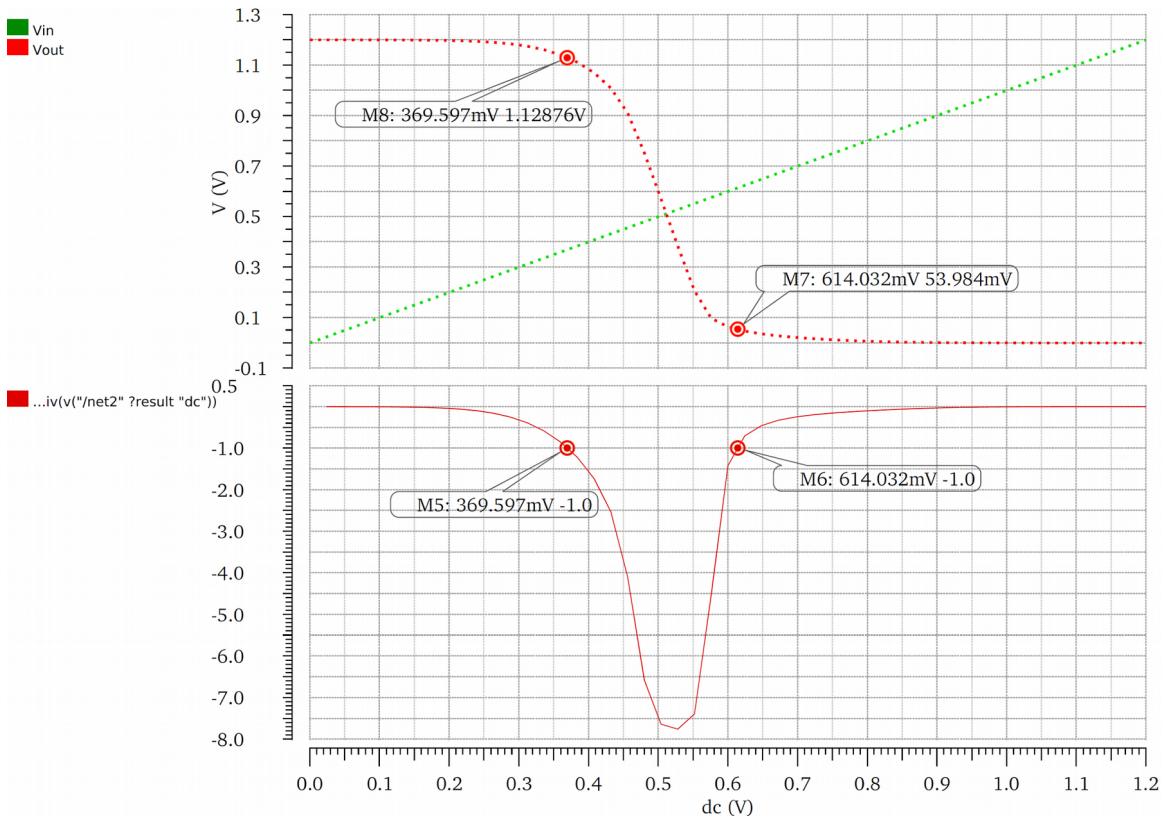


Figure 9: DC analysis of the CMOS wide inverter.

Transient analysis

Type	t_{plh}	t_{phl}	t_r	t_f
CMOS	0.273	0.092	0.395	0.116
CMOS_Wide	0.071	0.028	0.095	0.029
Enhancement mode NFET	N/D	N/D	1.231	0.076
Enhancement mode NFET_Long	N/D	N/D	2.028	0.082
Resistive load (100k)	1.014	0.088	2.092	0.116
Resistive load_long (200k)	2.071	0.062	4.189	0.123

1. Explain in your own words the variation of the DC output voltages V_{OH} and V_{OL} for the four inverters? In particular focus on the differences noted earlier in the NFET connected inverters and explain in your own words the variation of the switching times for all the inverters?

The V_{OH} for both the resistive load and CMOS inverters are close to V_{DD} , which means the inverters will output a strong inverted signal. Whereas the V_{OH} for the enhancement mode nMOS inverter may give a weak inverted signal output.

As for the switching times the CMOS is by far the fastest among the group in regards to rise time. This is in part due to the pMOS pull-up transistor which delivers a strong high signal. This shows why the CMOS is such a popular solution for inverters. The fall times for all the inverters are very close in comparison. This can be attributed to the fact that all three inverters have pull-down nMOS transistors and thus resulting in similar fall times.

2. List out the major drawbacks and benefits of using a NFET load and resistor for signal inversion from area, VTC, noise margin, leakage and fabrication point of view. Why do you think CMOS has become so popular in the recent times?

The Enhancement Mode nMOS inverter's voltage transfer characteristics show that V_{OH} and V_{IH} are too close together, creating a very small noise margin. When the noise margin is small, any noise at the input could cause it to not recognize the input level. While the other two inverters have a V_{OH} close to V_{DD} , the Enhancement Mode nMOS inverter has a V_{OH} of less than half of V_{DD} . Ideally the value of V_{OH} should be close to V_{DD} . This is proof that the nMOS can not pass a strong 1 (aka high signal).

The Enhancement Mode nMOS inverter has a non zero leakage current through the enhancement transistor when the inverter is not switching. This results in unwanted power consumption. A smaller area and ease of fabrication are the benefits of this nMOS design. The Resistive Load inverter performs better than the Enhancement Mode nMOS inverter, but resistors are more expensive and take up a lot more space which limits flexibility in the design and fabrication.

The CMOS is the superior inverter design as we have improved our fabrication methods. They have lower static power consumption, faster rise times and are less susceptible to noise. The complimentary pMOS and nMOS transistors in a CMOS are part of the key to its design as they each perform the function they are best at: the pMOS pulls the output high and the nMOS pulls the output low.

3. What happens if PMOS and NMOS are interchanged in an inverter connection? Where should you measure the output to get the desired inverted signal after interchanging their positions?

We believe this is a trick question. If the NMOS and PMOS were interchanged in an CMOS inverter configuration, the inverter would simply act as a buffer. The output will not be significantly different from the input though it would be a "weaker version" of the input. The trick part is that there is no location to measure to get the desired inverted output.

4. What is the roles and responsibility of each member of your lab team? Who did what part of the lab?

Each member did the entire lab independently and compared results. The results were collaboratively edited to these three

reports.