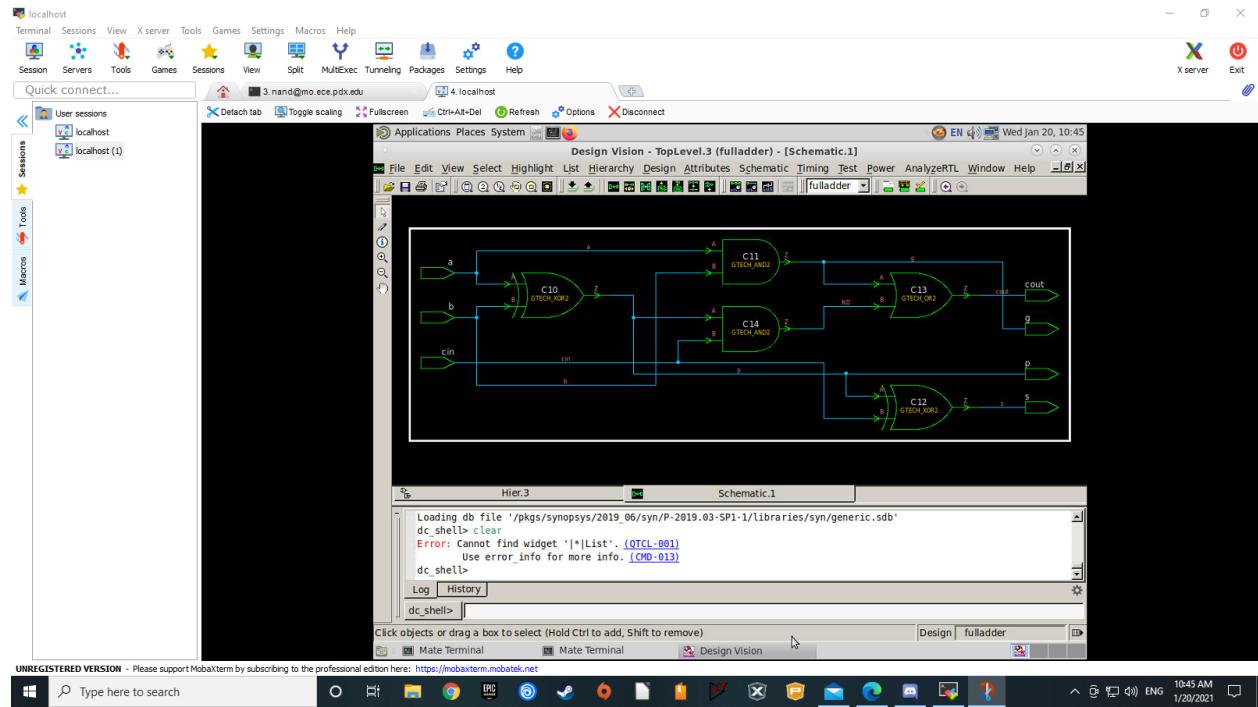


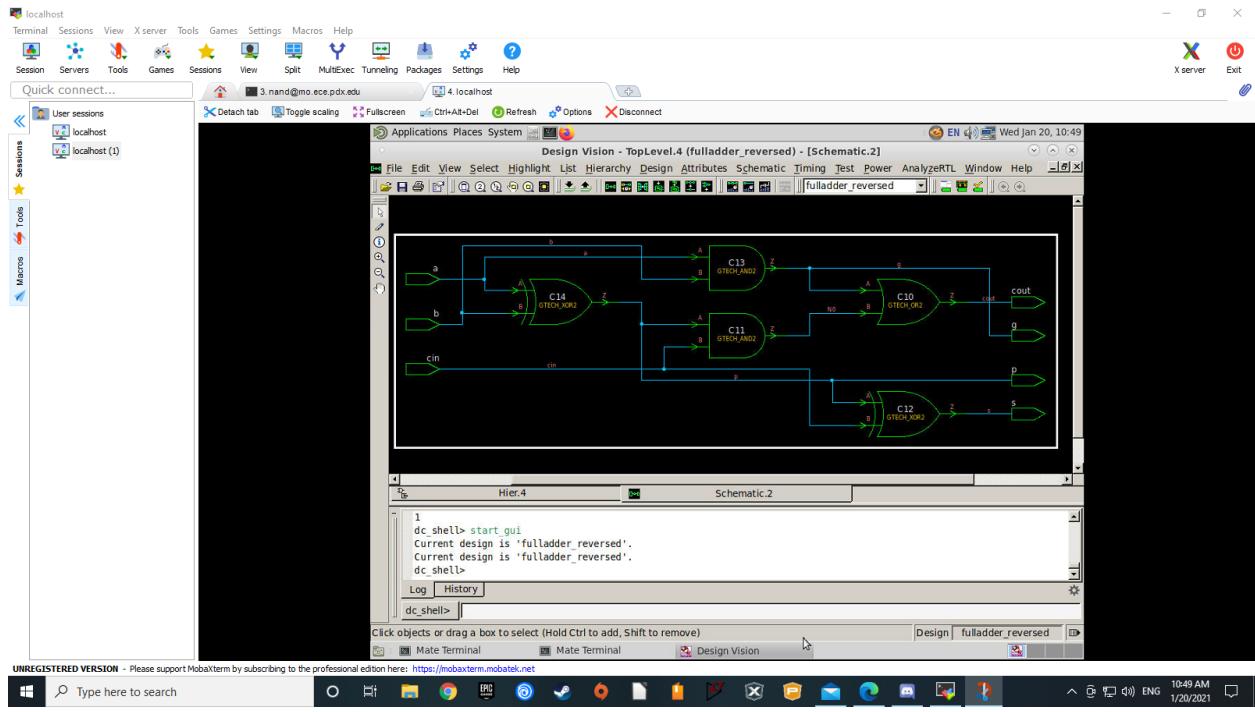
HW_LAB_3.1: Concurrency in SystemVerilog

A)

i) p-g-s-cout order



ii) cout-s-g-p order



Both modules produced the same schematics as can be seen in the images above.

B)

The created test bench used:

```

`timescale 1ns/1ns
module tb();

reg a, b, cin;
wire s;
wire cout;
wire p;
wire g;

fulladder fulladder(a, b, cin, p, g, s, cout);

initial begin
#4 a = 1'b0; b = 1'b0; cin = 1'b0;
#4 a = 1'b1; b = 1'b0; cin = 1'b1;
#4 a = 1'b0; b = 1'b1; cin = 1'b1;
#4 a = 1'b0; b = 1'b0; cin = 1'b0;

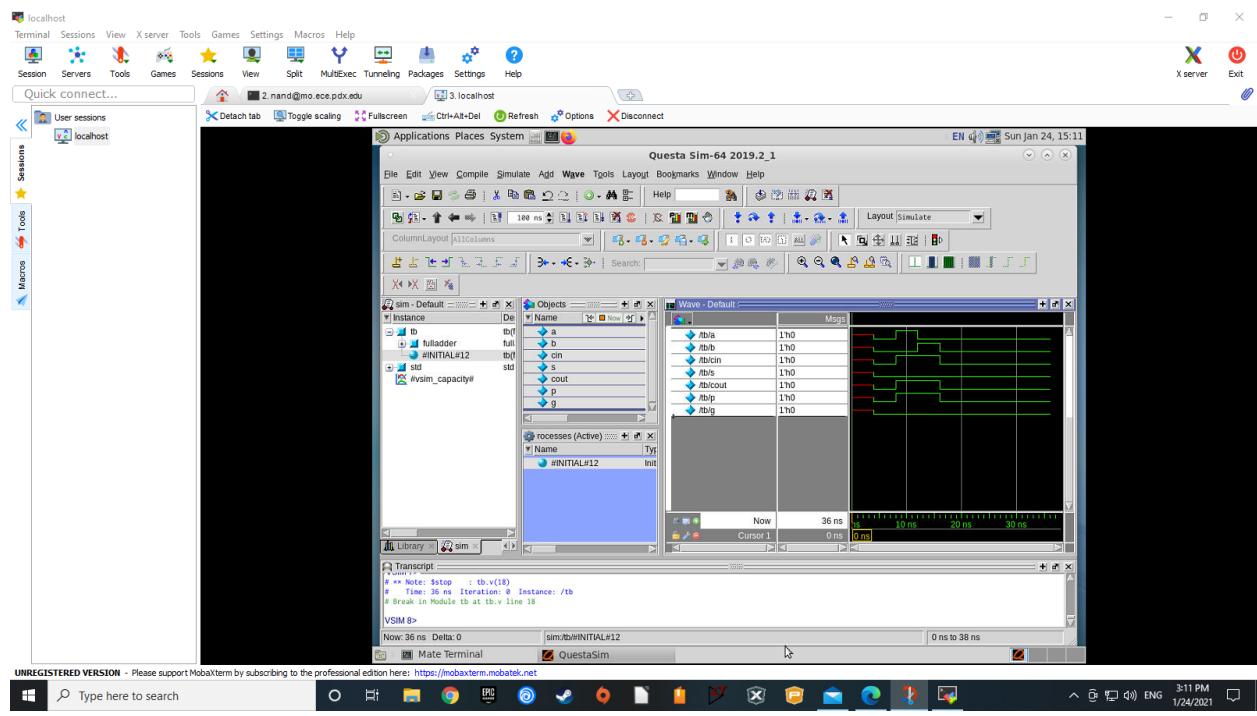
#20 $stop;

end

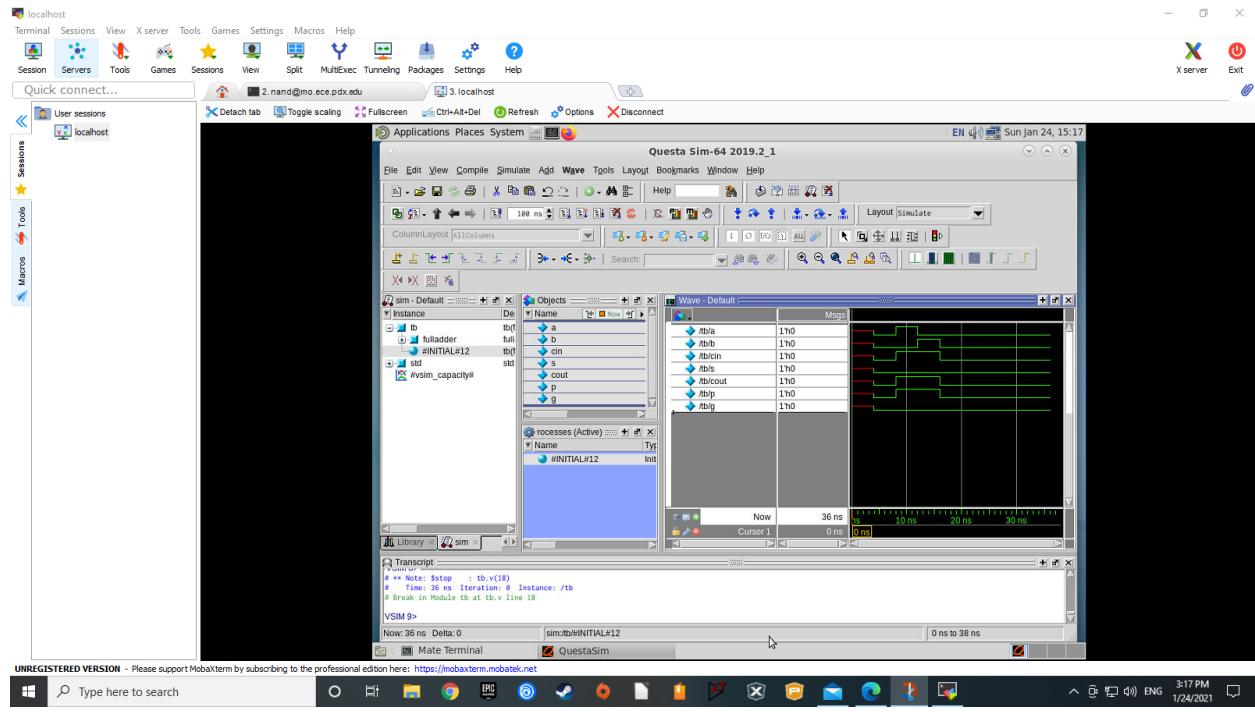
endmodule

```

fulladder.sv using testbench above



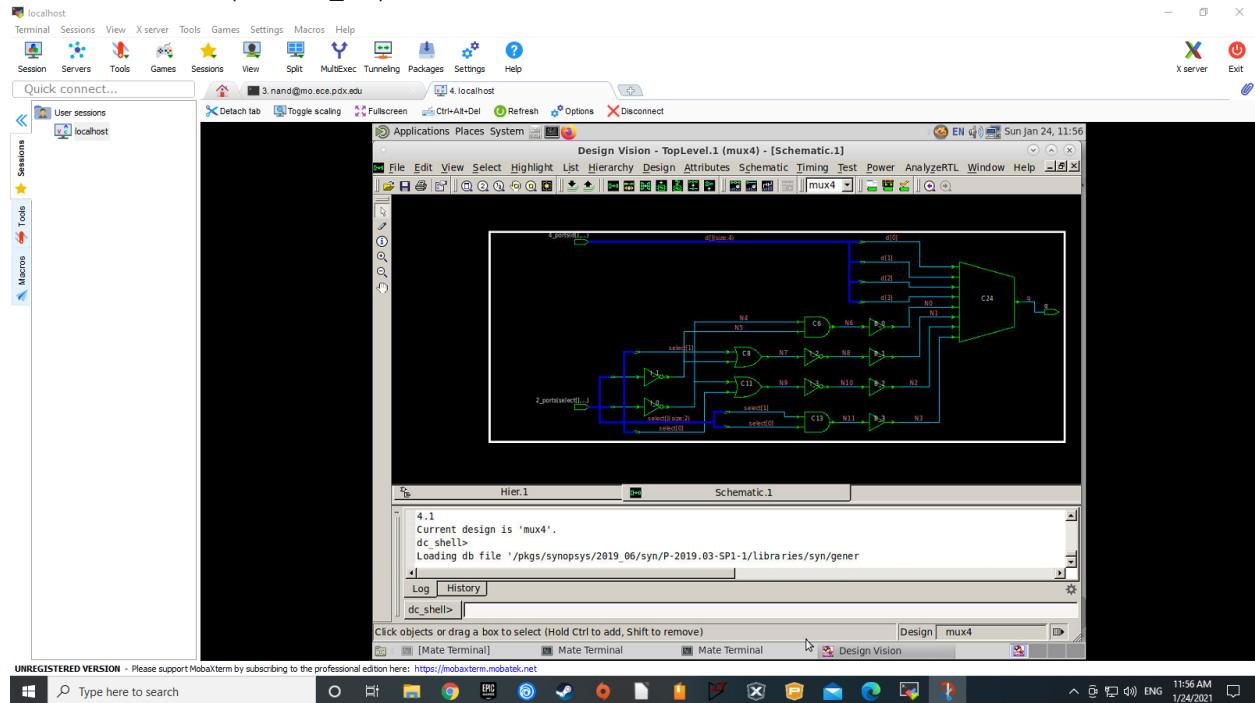
fulladder_reversed.sv using the same testbench above.



HW_LAB_3.2: SELECT_OP vs MUX_O

A)

Elaboration GTECH (SELECT_OP)



report_cell:

```

File Edit View Search Terminal Help
dc_shell> Loading db file '/pkgs/synopsys/2019_06/syn/P-2019.03-SP1-1/libraries/syn/generic.sdb'
dc_shell> report cell
Information: Updating graph... (UID-83)

*****
Report : cell
Design : mux4
Version: P-2019.03-SP1-1
Date   : Sun Jan 24 11:57:05 2021
*****


Attributes:
b - black box (unknown)
c - control logic
h - hierarchical
n - noncombinational
r - register
s - synthetic operator
u - contains unmapped logic

Cell          Reference      Library       Area Attributes
+-----+-----+-----+
B_0           GTECH BUF    gtech        0.000000 C, u
B_1           GTECH BUF    gtech        0.000000 C, u
B_2           GTECH BUF    gtech        0.000000 C, u
B_3           GTECH BUF    gtech        0.000000 C, u
C6           GTECH AND2   gtech        0.000000 C, u
C8           GTECH OR2    gtech        0.000000 C, u
C11          GTECH OR2    gtech        0.000000 C, u
C13          GTECH AND2   gtech        0.000000 C, u
C24          *SELECT OP 4.1_1.1 0.000000 S, u
I_0           GTECH NOT   gtech        0.000000 u
I_1           GTECH NOT   gtech        0.000000 u
I_2           GTECH NOT   gtech        0.000000 u
I_3           GTECH NOT   gtech        0.000000 u
+-----+
Total 13 cells                                0.000000
1
dc shell>

```

```

File Edit View Search Terminal Help
Elaborated 1 design.
Current design is now 'mux4'.
1
dc shell> report area
Information: Updating graph... (UID-83)

*****
Report : area
Design : mux4
Version: P-2019.03-SP1-1
Date   : Sun Jan 24 15:46:56 2021
*****


Information: Updating design information... (UID-85)
Library(s) Used:
gtech (file: /pkgs/synopsys/2019_06/syn/P-2019.03-SP1-1/libraries/syn/gtech.db)

Number of ports: 7
Number of nets: 19
Number of cells: 13
Number of combinational cells: 12
Number of sequential cells: 1
Number of macros/black boxes: 0
Number of buf/inv: 8
Number of references: 5

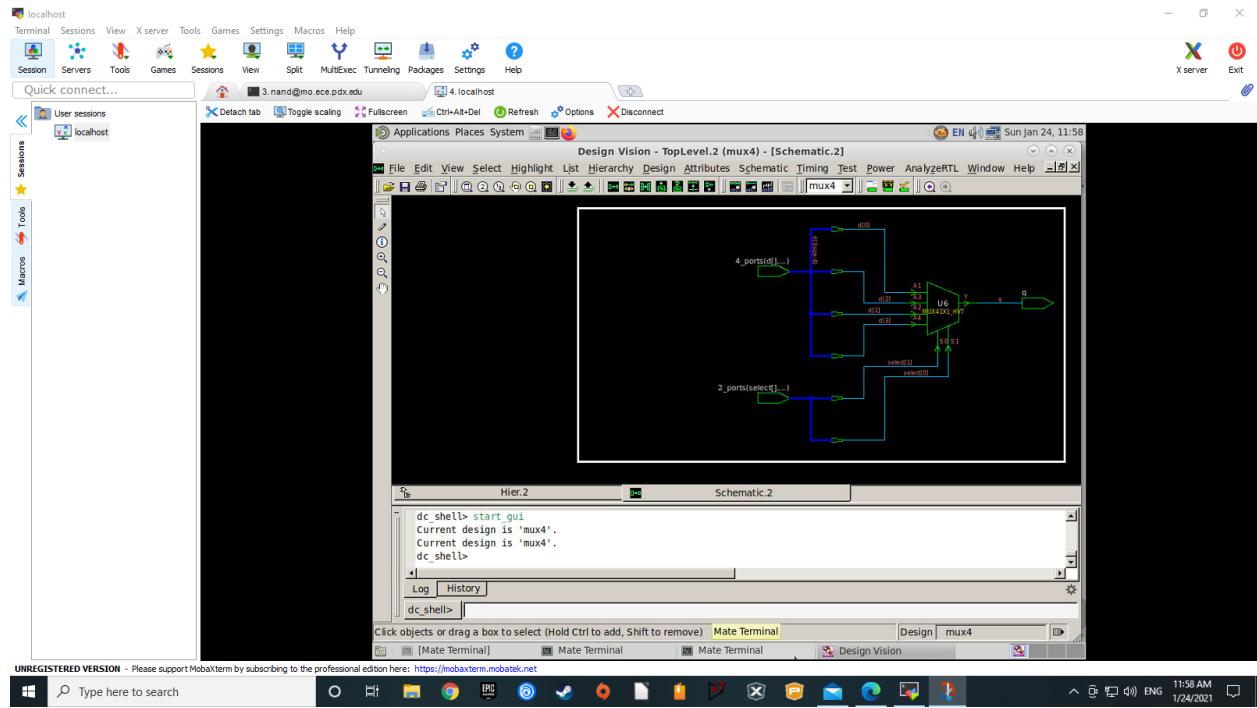
Combinational area: 0.000000
Buf/Inv area: 0.000000
Noncombinational area: 0.000000
Macro/Black Box area: 0.000000
Net Interconnect area: 2.199148

Total cell area: 0.000000
Total area: 2.199148

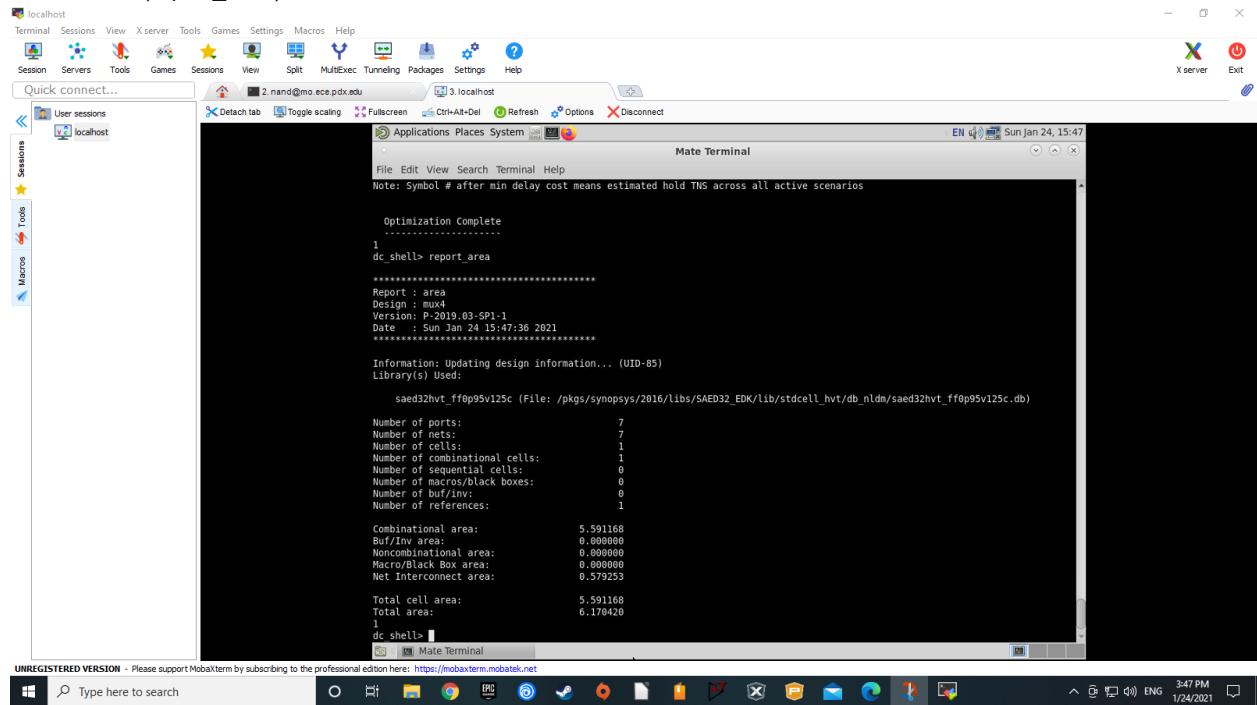
Information: This design contains unmapped logic. (RPT-7)
1
dc shell>

```

compile (cell reference is now MUX41X1_HVT)

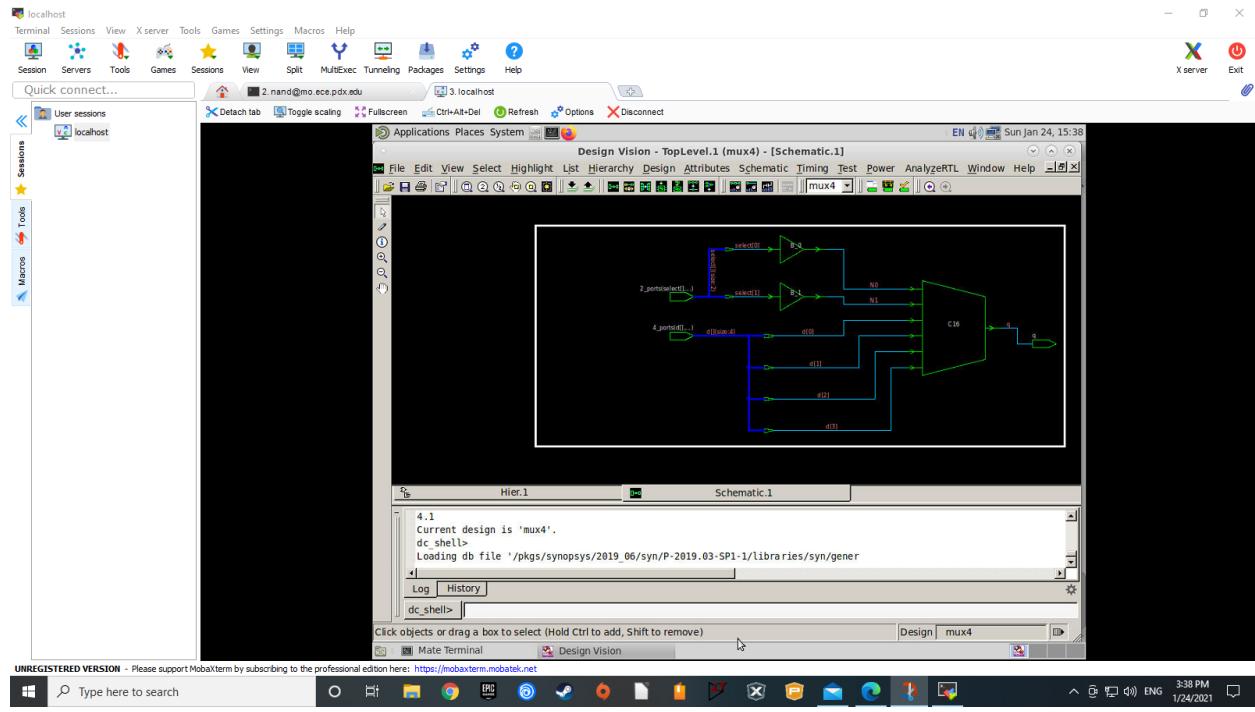


Area is now (report_area):



B)

Elaboration GTECH (MUX_OP)



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The screenshot shows a terminal window titled "Mate Terminal" with the command "dc_shell> report_cell" being run. The output shows the compilation results and the detailed cell report for the "mux4" design. The report includes information about cells, references, library assignments, and attributes. The terminal window is part of a desktop environment with a taskbar at the bottom.

```

4.1
Current design is 'mux4'.
dc_shell>
Loading db file '/pkgs/synopsys/2019_06/syn/P-2019.03-SP1-1/libraries/syn/gener
<| Log | History |
dc_shell>
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
Design | mux4 | Schematic.1

```

```

=====
mux4/8 | 4 | 1 | 2 |
=====
Presto compilation completed successfully. (mux4)
Elaborated 1 design.
Current design is now 'mux4'.
1
dc_shell> start gui
dc_shell> Current design is 'mux4'.
4.1
Current design is 'mux4'.
dc_shell> Loading db file '/pkgs/synopsys/2019_06/syn/P-2019.03-SP1-1/libraries/syn/generic.sdb'
dc_shell> report cell
Information: Updating graph... (UID=83)

*****
Report : cell
Design : mux4
Version: P-2019.03-SP1-1
Date : Sun Jan 24 15:40:03 2021
*****


Attributes:
  b - black box (unknown)
  c - control logic
  h - hierarchical
  n - noncontrollable
  r - removable
  s - synthetic operator
  u - contains unmapped logic

Cell Reference Library Area Attributes
-----
B_0 GTECH BUF gtech 0.000000 C, U
B_1 GTECH BUF gtech 0.000000 C, U
C16 *MUX OP 4 2 1 0.000000 S, U
-----
Total 3 cells 0.000000
dc_shell>

```

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report_area:

localhost

Terminal Sessions View X server Tools Games Settings Macros Help

Sessions

Quick connect...

2.nand@mo.ece.pdx.edu 3.localhost

Detach tab Toggle scaling Fullscreen Ctrl+Alt+Del Refresh Options Disconnect

Applications Places System Mate Terminal

File Edit View Search Terminal Help

```
C16          *MUX OP 4 2_1      0.000000 s, u
.
Total 3 cells          0.000000
1
dc_shell> report_area
*****
Report : area
Design : mux4
Version : P-2019.03-SP1-1
Date : Sun Jan 24 15:11:02 2021
*****
Information: Updating design information... (UID-85)
Library(s) Used:
gttech (file: /pkgs/synopsys/2019_06/syn/P-2019.03-SP1-1/libraries/syn/gttech.db)

Number of ports: 7
Number of nets: 9
Number of cells: 3
Number of combinational cells: 2
Number of sequential cells: 1
Number of macros/black boxes: 0
Number of buf/inv: 2
Number of references: 2

Combinational area: 0.000000
Buf/Inv area: 0.000000
Noncombinational area: 0.000000
Macro/Black Box area: 0.000000
Net Interconnect area: 0.744753

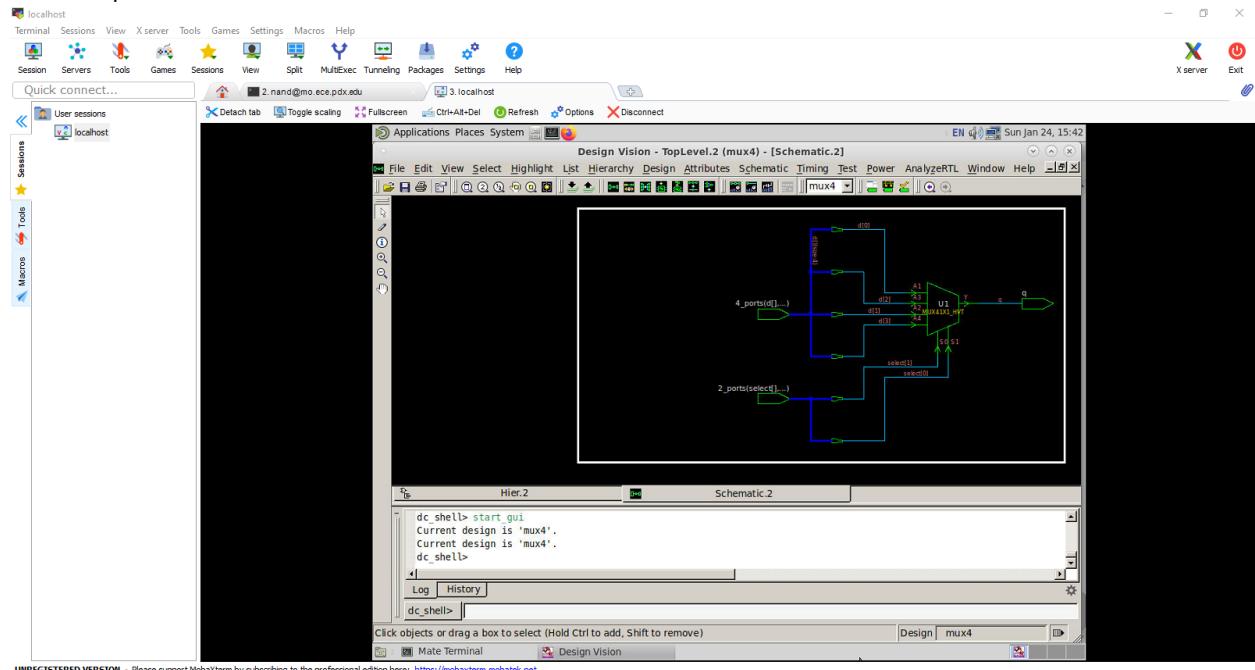
Total cell area: 0.000000
Total area: 0.744753

Information: This design contains unmapped logic. (RPT-7)
1
dc_shell> Mate Terminal
```

UNREGISTERED VERSION - Please support MobaTerm by subscribing to the professional edition here: <https://mobaterm.mobatek.net>

3:41 PM 1/24/2021

After compile:



report_area:

```

Optimization Complete
-----
1
dc_shell> startgui
dc_shell> Current design is 'mux4'.
Current design is 'mux4'.
dc_shell> dc_shell> report area
*****
Report : area
Design : mux4
Version : P-2019.03-SPI-1
Date : Sun Jan 24 15:43:27 2021
*****
Information: Updating design information... (UID-85)
Library(s) Used:
saed32hvt_ff0p95v125c (File: /pkgs/synopsys/2016/libraries/SAED32_EDK/lib/stdcell_hvt/db_nldm/saed32hvt_ff0p95v125c.db)

Number of ports: 7
Number of nets: 7
Number of cells: 1
Number of combinational cells: 1
Number of sequential cells: 0
Number of macros/black boxes: 0
Number of buf/inv: 0
Number of references: 1

Combinational area: 5.591168
Buf/Inv area: 0.000000
Noncombinational area: 0.000000
Macro/Black Box area: 0.000000
Net Interconnect area: 0.579253

Total cell area: 5.591168
Total area: 6.179420
1
dc_shell>

```

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3:43 PM 1/24/2021

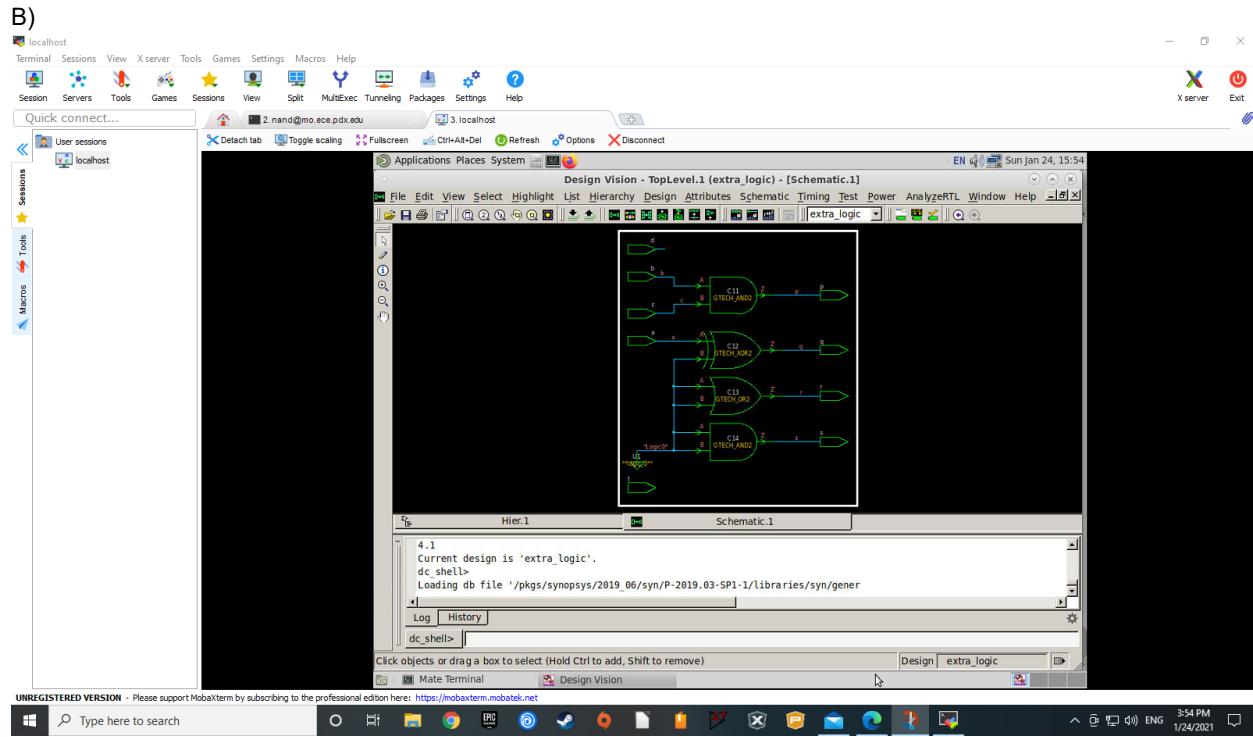
C)

	SELECT_OP		MUX_OP	
	Elaborate	Compile	Elaborate	Compile
Cell Area	0.000	5.591	0.000	5.591
Total Area	2.198	6.170	.744	6.170

Comparing the elaboration schematics for both cases (SELECT_OP and MUX_OP) we can see that the SELECT_OP schematic does indeed have “select logic” (or more gates). The MUX_OP elaboration schematic has just the MUX_OP cell (with select buffers) as expected. This is why the total area for the SELECT_OP implementation is higher (there are more gates in total).

However, after compilation both cases have the same schematic. In addition, the same cell areas (as shown in the table above). It seems the program simplified both schematics to utilize the MUX41X1_HVT mux from the library which explains the same area.

HW_LAB_3.2: Extra/Unconnected/Undriven Logic:



C) check_design:

```
dc_shell> check_design

*****
check_design summary:
Version:      P-2019.03-SP1-1
Date:        Sun Jan 24 15:56:10 2021
*****

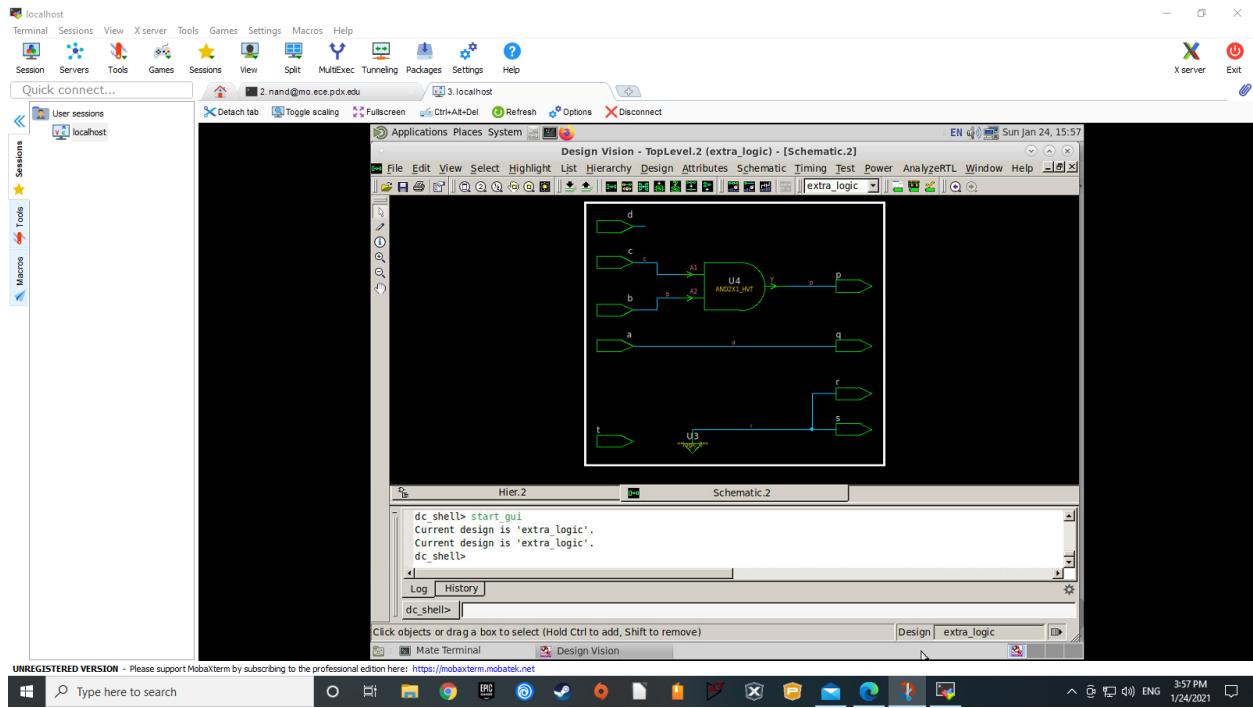
          Name          Total
Inputs/Outputs
  Unconnected ports (LINT-28)      2
                                2

Warning: In design 'extra_logic', port 'd' is not connected to any nets. (LINT-28)
Warning: In design 'extra_logic', port 't' is not connected to any nets. (LINT-28)
1
```

LINT-28

Both warnings point to the same concern, which is both port 'd' and port 't' are not connected to anything. This can easily be seen from the schematic above.

E) Schematic after compile



F) check_design after compile:

```
dc_shell> check_design
*****
check_design summary:
Version: P-2019.03-SP1-1
Date: Sun Jan 24 15:58:07 2021
*****
Name Total
-----
Inputs/Outputs
  Unconnected ports (LINT-28) 6
  Feedthrough (LINT-29) 2
  Shorted outputs (LINT-31) 1
  Constant outputs (LINT-52) 1
-----
Warning: In design 'extra_logic', port 'd' is not connected to any nets. (LINT-28)
Warning: In design 'extra_logic', port 't' is not connected to any nets. (LINT-28)
Warning: In design 'extra_logic', input port 'a' is connected directly to output port 'q'. (LINT-29)
Warning: In design 'extra_logic', output port 'r' is connected directly to output port 's'. (LINT-31)
Warning: In design 'extra_logic', output port 'r' is connected directly to 'logic 0'. (LINT-52)
Warning: In design 'extra_logic', output port 's' is connected directly to 'logic 0'. (LINT-52)
1
```

The additional warnings here are:

LINT-29 is saying that output 'q' has a short to input 'a' where there is no logic in between. Typically, a short isn't desirable therefore it has a warning.

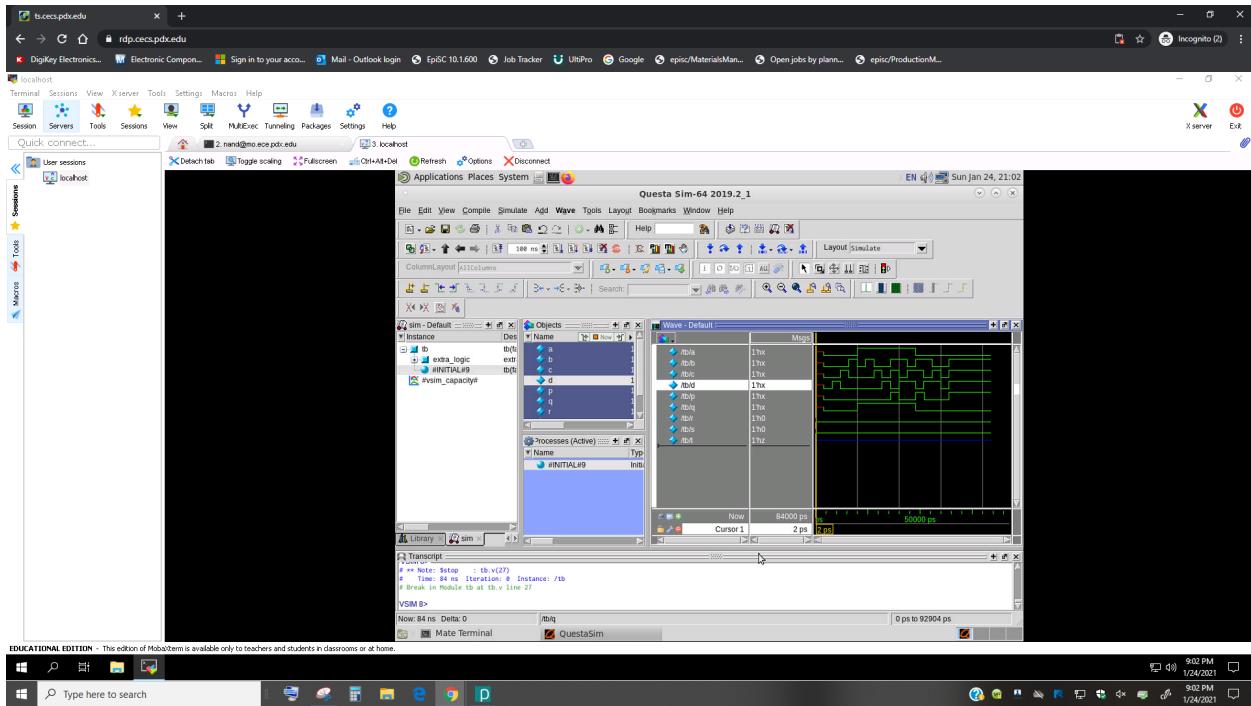
LINT-31 is saying that both outputs 's' and 'r' are connected on the same wire. Therefore, $r = s$ which may not be desirable either. So the program displays a warning.

LINT-52 is saying that both outputs 's' and 'r' are essentially grounded permanently. These outputs will not change since there is no logic connected. In other words, it is redundant.

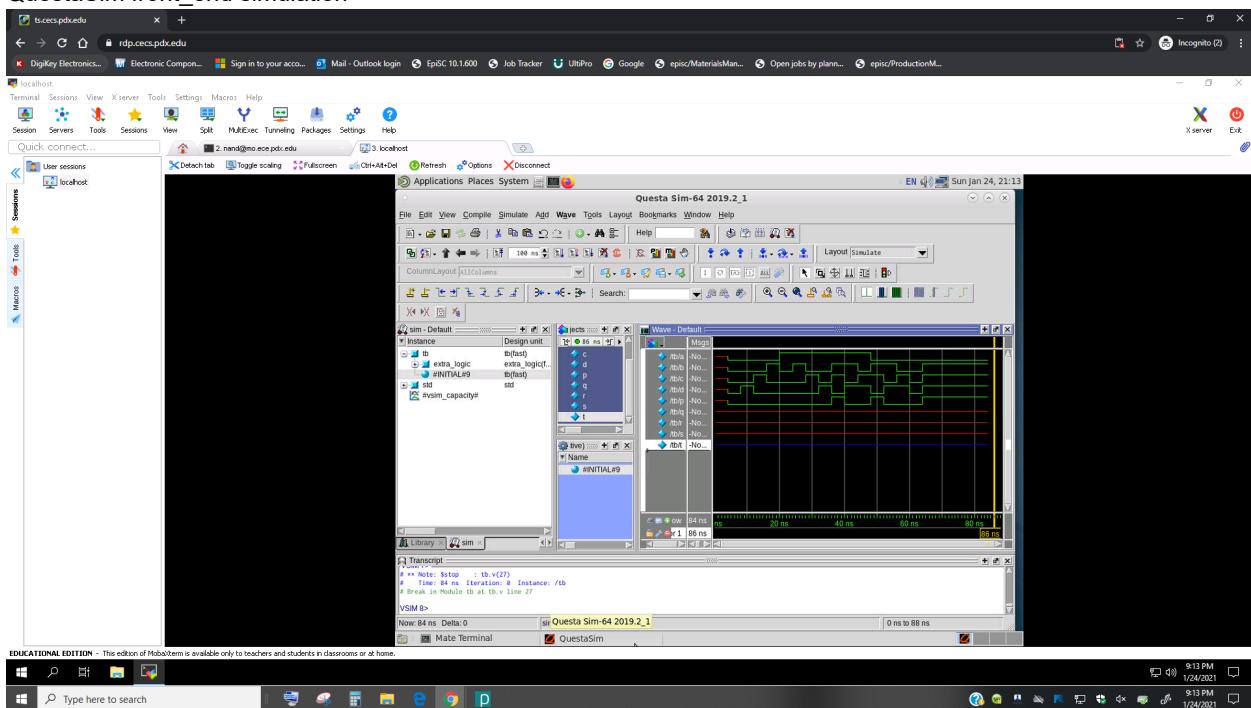
All of these warnings can easily be seen in the schematic.

G)

QuestaSim back_end simulation

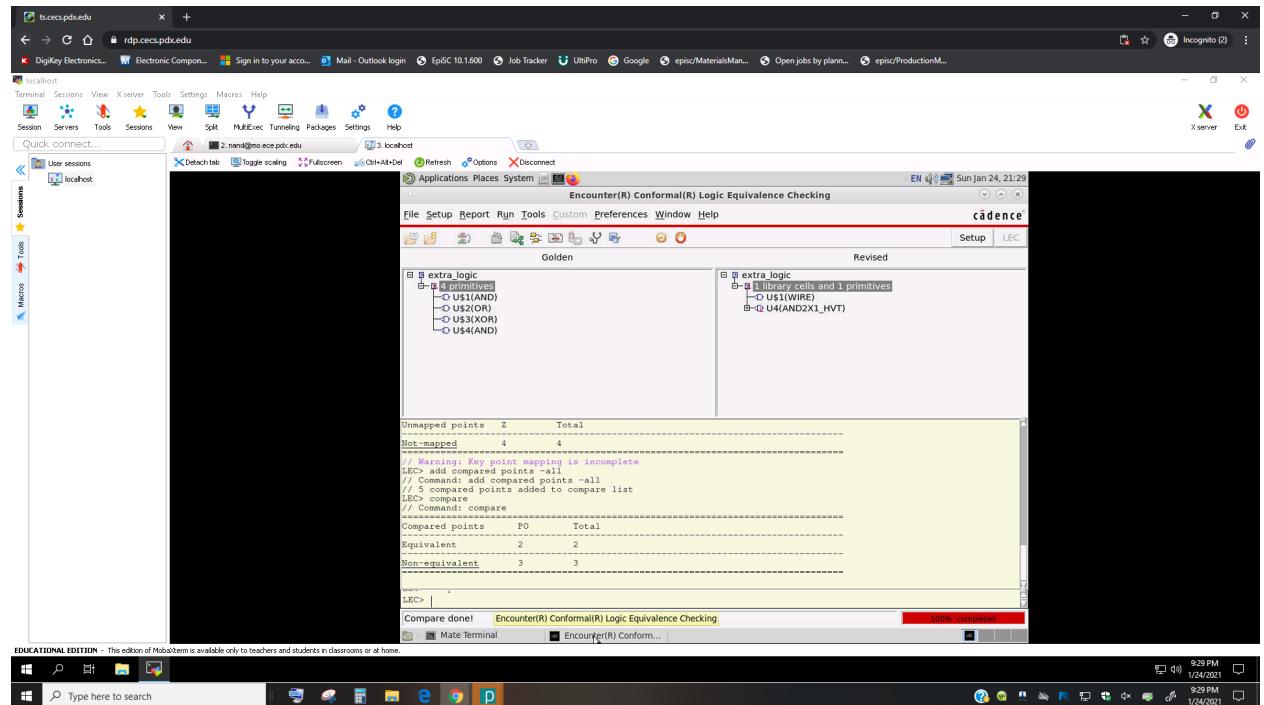


QuestaSim front_end simulation



If we look and analyze the waveforms whilst comparing them with their respective schematics these make sense. I believe the difference is that compilation of the RTL simplifies and eradicates any redundancies from the logic. For example, after compilation output q is simply equivalent to input a (as seen in the waveforms/schematics above after compilation). Whereas, those red lines in the front_end are the XORs that have the grounded inputs (in the elaborated schematic including the output q).

Cadence Conformal



I believe the non-equivalents show that the netlists do not match. To be expected after looking at the waveforms from the Questa simulations.