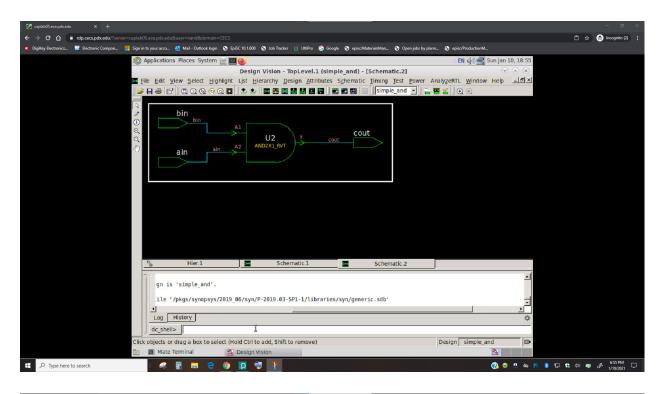
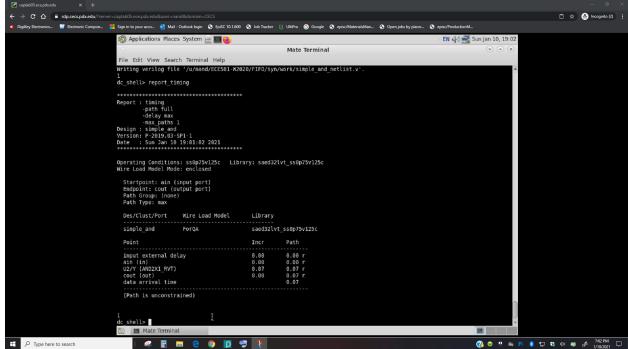
ASIC MODELING AND SYNTHESIS ECE - 4/581 Winter 2021

HW_Lab1

Ryan Nand 1/10/2021

Synthesis using Design Compiler





Questa Sim FE and BE (I accidentally added two FE waveforms in one plot)

